VX3060-S2 - User Guide

3U VPX Computing Node

D291771-V1.0 - April 2024

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⚠CAUTION	Handling and operation of the product is permitted only for trained personnel within a work place that is access controlled. Please follow the “General Safety Instructions” supplied with the system.
NOTICE	You find the most recent version of the “General Safety Instructions“ online in the download area of this product.
NOTICE	This product is not suited for storage or operation in corrosive environments, in particular under exposure to sulfur and chlorine and their compounds. For information on how to harden electronics and mechanics against these stress conditions, contact Kontron Support.

Revision History

Revision	Brief Description of Changes	Date of Issue	Author
1.0	New User Guide dedicated to the VX3060-S2 product. Information related to the VX3060 non SOSA product removed This new user guide is based on the previous D247914-1.8 User Guide	2024-April-09	MRI

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For contact information, refer to the corporate offices contact information on the last page of this user guide or visit our website CONTACT US.

Customer Support

Please contact our support team at support.KFR@kontron.com .

Customer Service

As a trusted technology innovator and global solutions provider, Kontron extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly experienced support enables Kontron to provide exceptional peace of mind to build and maintain successful products.
For more details on Kontron's service offerings such as: enhanced repair services, extended warranty, Kontron training academy, and more visit https://www.kontron.com/support-and-services.

Customer Comments

If you have any difficulties using this user guide, discover an error, or just want to provide some feedback, contact Kontron support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user guide on our website.

Symbols

The following symbols may be used in this user guide

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
NOTICE	NOTICE indicates a property damage message.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
	**Electric Shock!** This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	**ESD Sensitive Device!** This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	**HOT Surface!** Do NOT touch! Allow to cool before servicing.
	**Laser!** This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol indicates important information which must be read carefully.
	This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning
All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!
Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.
Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

⚠CAUTION

Danger of explosion if the battery is replaced incorrectly.
Replace only with same or equivalent battery type recommended by the manufacturer.
Dispose of used batteries according to the manufacturer's instructions.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Quality and Environmental Management

Kontron aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding Kontron's quality and environmental responsibilities, visit https://www.kontron.com/about-kontron/corporate-responsibility/quality-management.

Disposal and Recycling

Kontron's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Environmental protection is a high priority with Kontron.
Kontron follows the WEEE directive
You are encouraged to return our products for proper disposal.

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1. Introduction

The Kontron VX3060-S2 is a 3U VPX computing blade for data and signal processing application focusing on application domains such as Military & Aerospace, Transportation and Energy/Industry.
The Kontron VPX blade VX3060-S2 is the ideal building block for intensive parallel computing workloads where a cluster of Kontron VX3060-S2 can be used in switched OpenVPX environments.

In this document:
VX3060-S2 stands for the product/board without any option or variant considerations.
SA/WA/RA are air-cooled variants whereas RC variant is conduction-cooled.

Ordered product manufacturing options and ECL may alter the product features.
Contact Kontron.

The VX3060-S2 board comes with EFI BIOS and supports Linux. It is covered by Kontron's long term supply program, which guarantees customers multi-year supply of the product beyond its active life.

The VX3060-S2 offers a rich set of I/O features such as a 4-lane PCIe Gen3, XMC slot, a 4-lane PCI Express Gen 3 expansion plane, dual 10 Gigabit Ethernet control planes, along with USB (2 and 3), serial links, DP, GPIOs, and XMC I/O mapping to the backplane. The result is a powerful, flexible, single board computing platform suitable for a wide range of embedded applications.

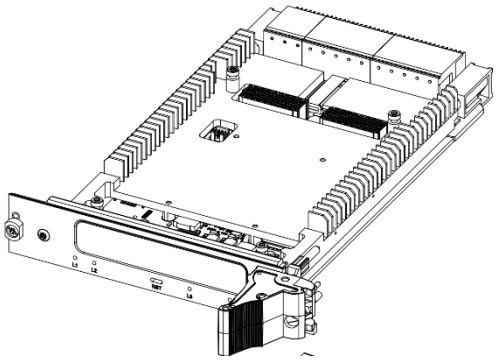
The highly integrated 4-core architecture with Dual 10 Gigabit Ethernet, high bandwidth PCI Express 3.0, high-speed DDR4 memory, and versatile mezzanine options, is consequently SWaP-C optimized and simply the best choice for high performance embedded computing platforms.

The VX3060-S2 variant features a VITA 46.11 compatible Intelligent Platform Management Controller (IPMC) for centralized system health management.

The VX3060-S2 RC variant is a conduction-cooled VITA 48.2 Type 2, Secondary Side Retainer plug-in unit.

Figure 1: VX3060-S2 3U VPX view – Conduction-cooled variant

Figure 2: VX3060-S2 3U VPX view – Air-cooled variants



1.1. Manual Overview

1.1.1. Objective

This guide provides general information, installation instructions, operating instructions and functional description of the VX3060-S2 board. The onboard programming, onboard firmware and other software (e.g. drivers and BSPs) are described in detail in separate guides (see section "Related Publications").

This hardware technical documentation reflects the most recent version of the product. The “Release Notes" (see section "Related Publications") might help to keep track of potential evolutions or available features.

In this document, E.C. Level or ECL means Engineering Change Level. ECLs are the exact technical definitions of the product.

The features of the VX3060-S2 have evolved and improved with successive board revisions.
The A digit in the ECL number (ABCDEFG) codes the PCB revision.
ECL 1xxxxyy means the initial PCB revision A, referred to as PCB-A in this document
ECL 2xxxxyy means PCB revision B, named PCB-B in this document
ECL 3xxxxyy means PCB revision C, named PCB-C in this document

Product features affected by the major hardware ECL changes can be found in this document by searching the “ECL-” keyword.

1.1.2. Audience

The scope of this guide is intended to cover, as far as possible, the range of people who will be handling or using the VX3060-S2, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, system, cabling, grounding and communications.

1.1.3. Scope

This guide describes the VX3060-S2 product, without any optional mezzanines equipped.
The VX3060-S2 variants described in this guide are fully compatible with system architectures developed in alignment with the SOSA™ technical standard.

1.1.4. Terminology, Definitions and Abbreviations

- Environmental classes terminology:
  - VX3060-S2 SA will be associated to the standard air-cooled version of the board.
  - VX3060-S2 WA will be associated to the extended air-cooled version of the board.
  - VX3060-S2 RA will be associated to the rugged air-cooled version of the board.
  - VX3060-S2 RC will be associated to the rugged conduction-cooled version of the board.

In this document, VX3060-S2 refers to the product/board without any options or variants considerations.

- Terms, acronyms and abbreviations

Table 1: Terms, acronyms and abbreviations

Term or Acronym	Definition
1 GbE	Abbreviation for 1-Gbit Ethernet interface (1000BASE-T).
Core	A processing unit including instruction cache, data cache, and often L2 cache.
COTS	Commercial Off The Shelf.
CPLD	Complex Programmable Logic Device
F-RAM	Ferroelectric Random Access Memory
LPC	Low Pin Count bus interface.
MTBF	Mean Time Between Failure.
OD	Open Drain Output
Option	A feature which requires a specific order code.
PCB	Printed Circuit Board.
PCH	Platform Controller Hub. The PCH is integrated in the SoC.
Processor	According to Intel® terminology, the processor - synonymous with SoC Refers to the Intel® Core™ XEON-D2700 processor.
PCIe	A synonym for PCI Express.
Provision	A feature not yet available.
PTU (Intel®)	Intel® Performance Test Utility.
SBC	Single Board Computer (the term defaults to VM606x).
SKU	Stock Keeping Unit: A catalog's product and service identification code.
SMBus	System Management Bus.
SoC (Intel®)	System on chip. According to Intel® terminology, the SoC - synonymous with processor
SWaP, SWaP-C	Seize, Weight and Power - Cost: an acronym to summarize the capabilities of an embedded system in Military or Aerospace.
TDP	Thermal Design Power: the target power level of the processor. It represents the maximum sustained power expected from realistic applications. It is an input to the thermal design of the board.
TPM	Trusted Platform Module: An international standard for a secure cryptoprocessor based on a dedicated hardware device and integrating cryptographic keys. Promoted by consortium TCG (Trusted Computing Group).
Turbo Boost Technology (Intel®)	A feature that opportunistically allows the processor to run at a higher frequency. This results in increased performance of both single and multi-threaded applications.

Term or Acronym	Definition
Uncore	In Intel® architecture, a unit of the SoC which includes the Ring, the Caching Agent Cbo, the Last Level Cache (LLC), the Home Agent (HA), the Integrated Memory Controller (IMC), the Integrated IO Module (IIO), the Power Control Unit (PCU).
2LM	Top/bottom covers for the 2 Maintenance level as defined per VITA 48 REDI standards
ECL	E.C. Level or ECL means Engineering Change Level. ECLs are the exact technical definitions of the product. Known product limitations are identified by the ECL number of a board

› Abbreviations:

TBD	To Be Defined. Information not available at the time this document was released.
TDP	Thermal Design Power
PTU	Power Thermal Utility

1.2. About VPX

VPX (VITA 46) specifications establish a new direction for the next revolution in bus boards. VPX is an ANSI standard which breaks out from the traditional connector scheme of VMEbus to merge the latest in connector and packaging technology with the latest in bus and serial fabric technology. VPX combines best-in-class technologies to assure a very long technology cycle similar to that of the original VMEbus solutions. Traditional parallel VMEbus will continue to be supported by VPX through bridging schemes that assure a solid migration pathway.

For further information regarding this standards and its use, visit the home page of the VITA - Open Standards, Open Markets (http://www.vita.com)

1.3. Board Overview

1.3.1. Manual Overview

› 11th Gen Intel® Core™ processor

The VX3060-S2 computing node is a VPX computing blade for parallel data and signal processing applications. The VX3060-S2 is the ideal building block for intensive parallel computing workloads where a cluster of VX3060-S2 is used in full mesh or switched OpenVPX environments. Target applications include radar, sonar, imaging systems, airborne fighters, and unmanned aerial vehicle (UAV) radar, as well as rugged multi-display consoles. It is also well suited for transport applications.

The processing node of the VX3060-S2 implements an 11th Gen Intel® Core™ processor coupled with single or dual channel DDR4 memory. The highly integrated platform hub provides numerous Ethernet, PCIe channels, USB and SATA channels.

Some of the VX3060-S2 features depends on the variant engineering level (ECL).
Refer also to the Hardware-Release-Note (D291798) for detailed information.

Table 2: Features overview

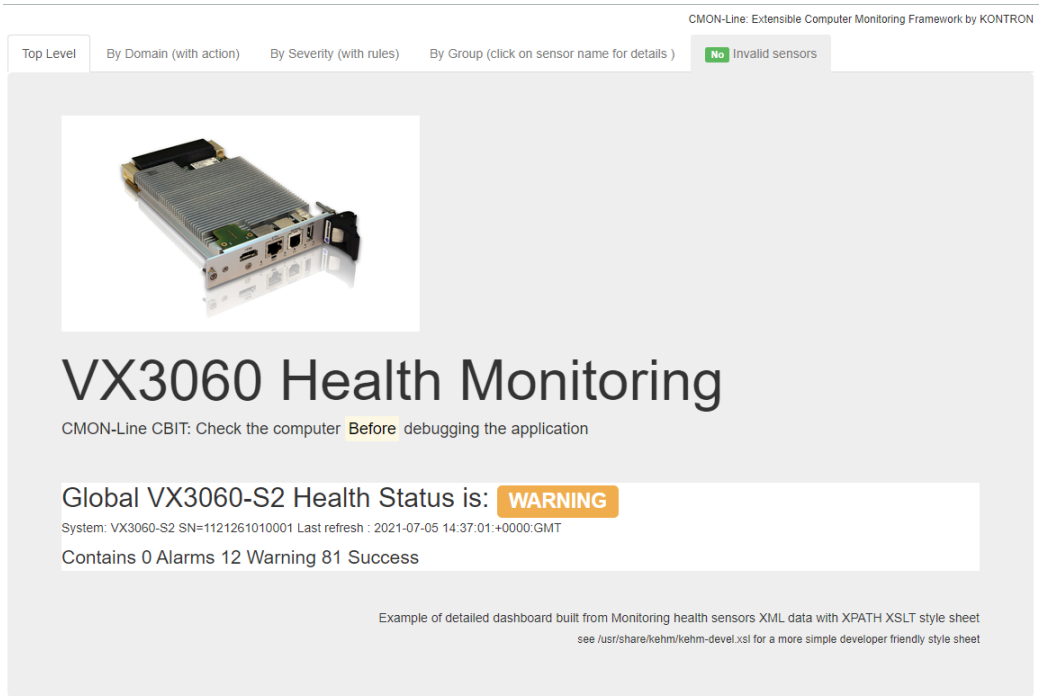
Features overview	
Processor	11th Gen Intel® Core™ Processor Family, enhanced AI, AVX-512, up to DDR4-3200 dual channel memory with In-Band ECC, up to 32 Gbytes Numerous USB-C, USB2/3, PCIe/SATA options to front panel, VPX rear panel and XMC slot.
Platform Controller Hub	Integrated Intel® 500 Series Chipset Family On-Package Platform Controller Hub.
Onboard Controllers	
Gigabit Ethernet controllers	One Intel® Ethernet Controller E810-XXVAM2 to the VPX rear panel One or two Intel® Ethernet Controller I225 to front/rear panels depending on variant Note: i225 controller may be replaced by the i226 controller (new generation) depending on the variant delivered.
Watchdog	CPLD-based, timeout ranging from 4 ms to 510s, IRQ, Reset, dual-stages
RTC	Separate low power RTC
System CPLD	Power - on/ off control, Reset control, Local environmental control/monitoring, I2C interfaces to I2C bus IPMB A/B (rear P0), LEDs control, Serial lines multiplexer, Serial VPD and user memories, User and system GPIOs, Internal registers that allow system management
IPMC	FRU subsystem management: Local environmental control/monitoring, IPMB A/B interfaces, FRU memory, system event log
Memory	
System Memory	Up to 32 GB dual channel DDR4 SDRAM running at up to 3200 MT/s, with IBECC, soldered
Flash (uEFI BIOS)	Two boot FLASH devices, with recovery image and uEFI BIOS settings ECL < ECL-3xxxxyy: two 256 Mbit devices equipped by default ECL= ECL-3xxxxyy: two 512 Mbit devices equipped by default
EEPROM	One I2C serial EEPROM dedicated to system data One I2C serial EEPROM dedicated to application data ECL < ECL-3xxxxyy: two 256 Kbit devices equipped by default ECL= ECL-3xxxxyy: two 512 Kbit devices equipped by default
F-RAM	One SPI F-FRAM dedicated to user data, up to 2M-bit
Front Interfaces 5HP (1")	
LEDs	Five LEDs reporting the board CPU health status and activity
Reset	Reset push button
Optional front panel	Front panel with serial, dual 1GbE RJ45, USB-C, and mDP connectors
Optional XDP interface	Processor XDP interface option restricted to lab use/conditions - on demand only Min ECL= ECL-3xxxxyy required for that XDP option.
Onboard Interfaces	
Top M.2 option (M2S1)	Top/Bottom M.2 module option: Type M, 22 mm x 42 mm form factor Supported: 2242-S1-M, 2242-S2-M, 2242-S3-M, 2242-D1-M,2242-D2-M, 2242-D3-M, 2242-D4-M, 2242-D5-M Slot interface: x1 PCIe up to Gen3 (8Gb/s) or SATA link up to 6 Gb/s.

Features overview	
Bottom M.2 option (M2S2)	**Not equipped on standard VX3060-S2 COTS product. Contact Kontron.**
XMC Slot	One x1 or x4 PCIe up to Gen3 (8Gb/s) to the XMC slot. with XMC I/O routing. Refer to the pin assignment tables in this document.
VPX Interface	
VPX Slot Profiles	SOSA S2 profile Compatible with the following as per Vita 65: Slot profile: SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16 Profile name: MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15-2 SLT3-PAY-2F2U-14.2.3 , SLT3-PAY-1F1F2U-14.2.4, SLT3-PAY-1F1U-14.2.10
Rear I/O via P1&P2	Refer to the pin assignment tables in this document.
Supervisory Functions	Non Maskable RESET NVMRO, Master SMBus and Master/Slave SMBus interfaces for system management. Compatible with Kontron CMB (Monitoring Board), temperature and voltage sensors on the board
Power Supplies	On P0: VS1=12V; VS2&VS3 not used; +12V_AUX is optional in VITA 46 and not connected -12V_AUX is optional in VITA 46. It is not used internally on VX3060-S2 except for the XMC slot. 3.3V_AUX is mandatory in VITA 46. However, if absent, it will be generated internally.
OS Support	Linux, ask for: Windows, VxWorks
Mechanical size	VPX 3U form factor, 1 Inch Slot pitch according VITA 48.1 (air cooled) and VITA 48.2 (conduction cooled)

All the Flash and non-volatile memories onboard have a write protect mechanism taking into account the NVMRO (Non Volatile Memory Read Only) VPX signal. For further details, see “NVMRO” section

Software

Kontron is one of the few compact PCI, VME and VPX vendors providing in-house support for most of the industry-proven real-time operating systems that are currently available.
Thanks to its close relationship with the software editors, Kontron is able to locally produce and support BIOS, BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology which follow silicon evolution.
Finally, Kontron offers to its customers owners of a maintenance agreement a hotline software support and regular software updates.
A dedicated web site is also available for online updates and release downloads.
The VX3060-S2 is delivered with the UEFI BIOS from AMI which supports Secure Boot and TPM. This BIOS supports PBIT Expert mode option from Kontron CMON-Line (https://kfrlabs.kontron.com/monitoring.php)
The VX3060-S2 supports a live Linux distribution (a Fedora Core remix distribution) for instant evaluation and benchmarking. Based on Fedora Linux, it offers many turn-key features, such as Continuous BIT service (CBIT). Refer to our Kontron VME/VPX Fedora Remix Release Notes for details.
With this software image loaded on a USB stick, you get instant access to all the features of the board. The CBIT dashboard can be accessed at http://board-ip-address:8000/kehm-RESULTS.xml .



Contact Kontron for further information regarding other operating systems and software support

Tooling - Rear Transition Module

The VX3060-S2 is compatible with the PB-VX3-40G-602 rear transition module.
Refer to the “RTM Characteristics” section for more information.

1.3.2. Block Diagram

Figure 3: Block Diagram

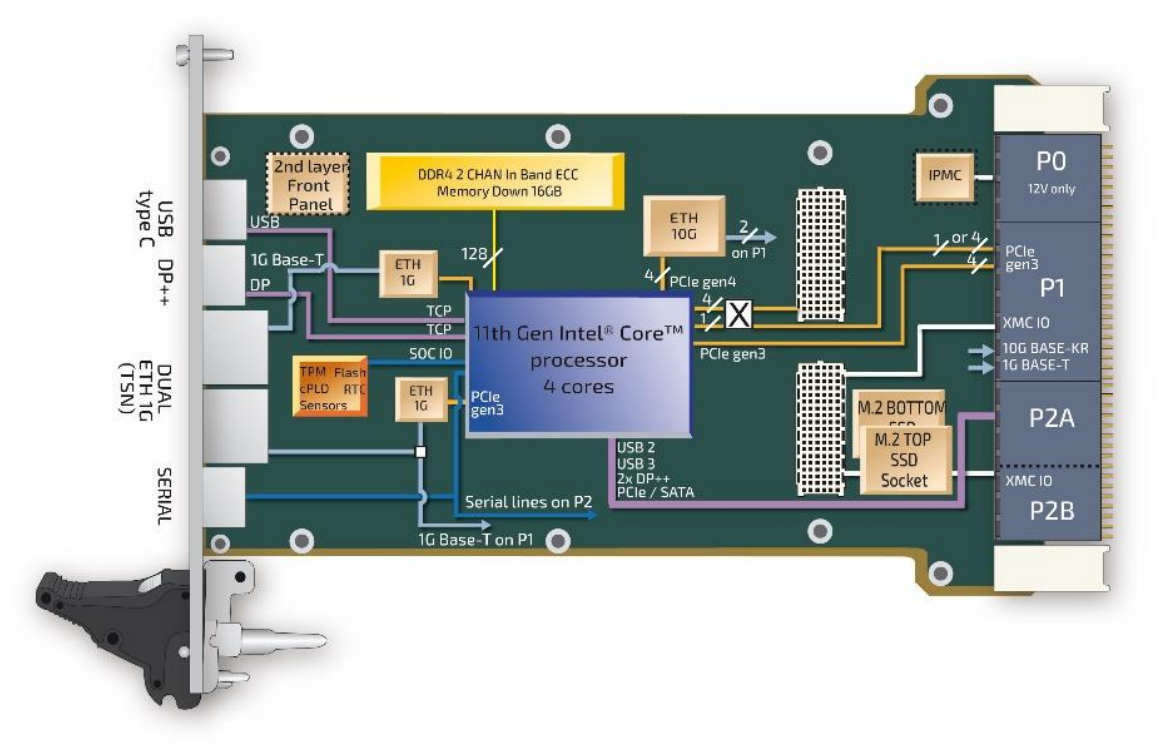
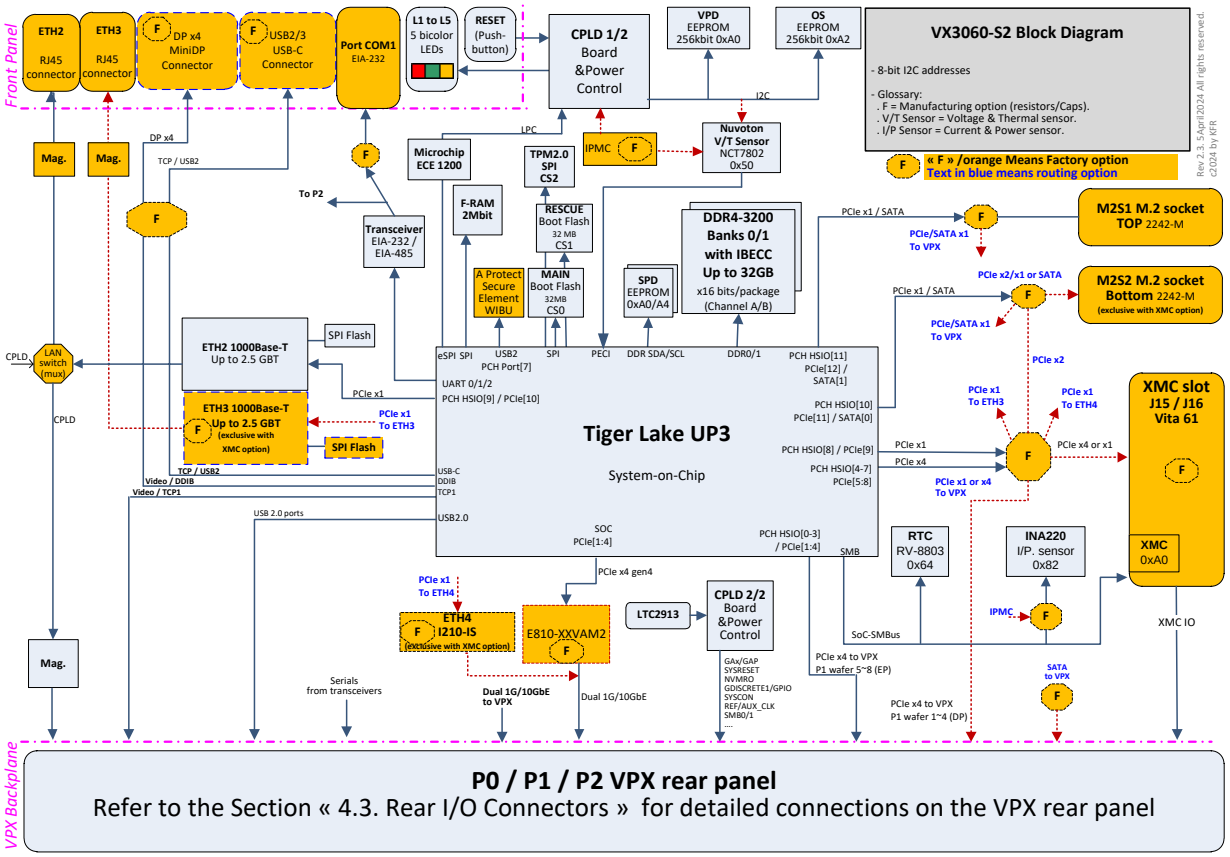


Figure 4: VX3060-S2- Detailed block diagram (ECL= ECL-3xxxxyy)



Refer to the product options and VPX pin assignments in Section 4 for detailed information
Ordered product manufacturing options and ECL affects the product features.
Contact Kontron.

Note related to PCIe bifurcation capabilities on Tiger Lake UP3:

x4 PCIe Data plane and expansion planes ports have PCIe bifurcation capabilities as follows

PCIe Lanes 1/2/3/4 in the following table are the lanes 0/1/2/3 of the VPX P1 Expansion plane

PCIe Lanes 5/6/7/8 in the following table are the lanes 0/1/2/3 of the VPX P1 Data plane

PCH-LP		PCIe* Controller #1				PCIe Controller #2			
Flex I/O Lanes		0	1	2	3	4	5	6	7
PCIe Lanes		1	2	3	4	5	6	7	8
Logical Link Lanes	1x4	0	1	2	3	0	1	2	3
	1x4 LR	3	2	1	0	3	2	1	0
	2x2	0	1	0	1	0	1	0	1
	2x2 LR	1	0	1	0	1	0	1	0
	1x2+2x1	0	1	0	0	0	1	0	0
	2x1+1x2	0	0	1	0	0	0	1	0
	4x1	0	0	0	0	0	0	0	0
Assigned Root Ports	1x4	RP1				RP5			
	1x4 LR	RP1				RP5			
	2x2	RP1		RP3		RP5		RP7	
	2x2 LR	RP3		RP1		RP7		RP5	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8

The PCIe* Lanes can be configured independently from one another but the max number of configured Root Ports (Devices) must not be exceeded. PCH-LP (UP3): A maximum of 6 PCIe* Root Ports (or devices) can be enabled.
In this table, “LR” stands for “Lane Reversal”.

1.3.3. Ordering information

› Main Manufacturing Options

Manufacturing Options	Description	Dependencies with other options
Environmental Class	Air cooled SA, WA, RA Conduction cooled RC3/RC4 EVAL/ Lab-grade for customer assessments and developments	Some covers options may not be available on standard air-cooled products.
Processor Type	11th Gen Intel® Core™ Tiger Lake processors (UP3)	
DDR4 SDRAM Size	8GB to 32GB	
XMC slot profile	Refer to the product order code definition	Front I/O Profile and Rear I/O Profile
Covers	With or without VITA 48.2 2LM covers	No 2LM covers on standard products
Rear I/O Profile	Refer to the product order code definition	XMC slot profile
Front I/O Profile	Refer to the product order code definition	XMC slot profile
M.2 slot profile	Refer to the product order code definition	Rear I/O Profile
On-Board RTC power	Powered from battery or VPX	Conduction cooled RC3/RC4
System Management	VITA 46.11 Tiers 2 Support	
Secure Element	TPM options	
SW Option	Power on Built in Test Run Time	
Preloaded SSD Option	Preloaded Eval Linux on M.2 256GB SSD	Environmental Class options
Slot pitch	1 inch / 5HP	

Dependencies with other options means the selection of an option may affect the other one. For instance, if XMC slot is ordered, Front I/O Profile will be force to “No Front I/O connectors”

› Available Order Codes – SOSA variants

Table 3: Available SOSA variants Order Codes – Air cooled

Environmental Class	Standard Order Codes (1)	Description
SA WA RA	VX3060-S2-SA4y-xxxx0xx1x VX3060-S2-WA4y-xxxx0xx1x(V) VX3060-S2-RA4y-xxxx0xx1x(V) (1)	3U Single slot 5HP (1") VPX SBC Air cooled @1.8GHz/15W Intel® Core™ I7-1185GRE Processor (TDP Software Configuration from 12W to 28W, 4 cores @ 2.8 GHz) with 96 EU Intel® Iris® Xe Graphics PCIe/SATA on Top 2242-M M.2 slot (M2S1), **no M.2 bottom slot (M2S2)** TPM 2.0 Secure element present **y option**: 8 or 16 or 32 GB soldered SDRAM with In-Band ECC **Other x options** XMC slot option and profile options VITA 48 2LM covers option Rear I/O profile option Front I/O profile On-board RTC Power VITA 46.11 option PBIT RT & Preloaded Linux on Eval M.2 256GB 3D TLC (3k cycles) SSD options (V)= Conformal coating option

Note (1): The maximum temperature allowed is processor TDP dependent.

The product datasheet presents the exhaustive list of the released product order codes. Refer to the Product datasheet for detailed information related to order codes.

Table 4: Available SOSA variants Order Codes – Conduction Cooled

Environmental Class	Standard Order Codes (1)	Description
RC3 RC4	VX3060-S2-RC34y-xxxx0xx1x(V) (1) VX3060-S2-RC44y-xxxx0xx1x(V) (1)	3U Single slot 5HP (1") VPX SBC Conduction cooled @1.8GHz/15W Intel® Core™ I7-1185GRE Processor (TDP Software Configuration from 12W to 28W, 4 cores @ 2.8 GHz) with 96 EU Intel® Iris® Xe Graphics PCIe/SATA on Top 2242-M M.2 slot (M2S1), **no M.2 bottom slot (M2S2)** TPM 2.0 Secure element present **y option**: 8 or 16 or 32 GB soldered SDRAM with In-Band ECC **Other x options** XMC slot option and profile options VITA 48 2LM covers option Rear I/O profile option Front I/O profile On-board RTC Power VITA 46.11 option PBIT RT & Preloaded Linux on Eval M.2 256GB 3D TLC (3k cycles) SSD options (V)= Conformal coating option

Note (1): The maximum temperature allowed is processor TDP dependent.

The product datasheet presents the exhaustive list of the released product order codes. Refer to the Product datasheet for detailed information related to order codes.

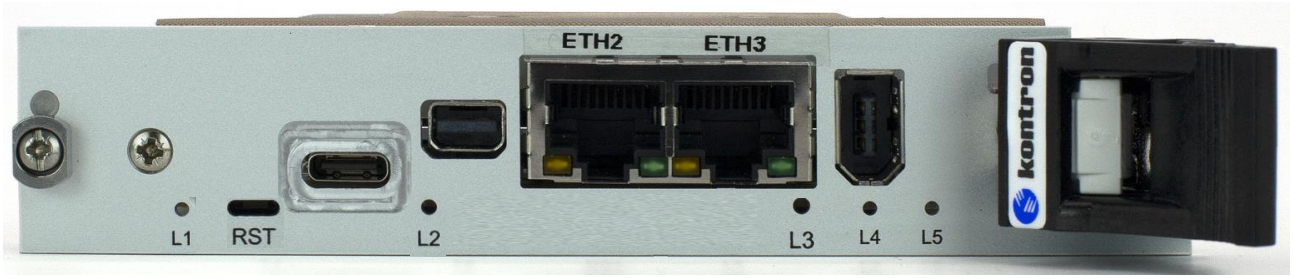
› Detailed description of each order code digit

VX3060-S2	3U Single slot 5HP (1") VPX SBC	Version : 09/04/2024
Environment Class	Air-Cooled 'SA' (0°C to 55°C)	SA
	Air-Cooled 'WA' (-20°C to +65°C) conformal coating	WA
	Rugged Air-Cooled 'RA' (-40°C to +70°C) conformal coating	RA
	Conduction-Cooled 'RC3' (-40°C to +70°C) conformal coating	RC3
	Conduction-Cooled 'RC4' (-40°C to +85°C) conformal coating	RC4
Processor	Intel(r) Core(tm) I7-1185GRE Processor (TDP Software Configuration from 12W to 28W, 4 core @ 2.8 GHz) with 96 EU Intel® Iris® Xe Graphics	4
SDRAM	8 GB soldered SDRAM with In-Band ECC	8
	16 GB soldered SDRAM with In-Band ECC	F
	32 GB soldered SDRAM with In-Band ECC	G
XMC Slot	No XMC mezzanine slot, FP1 x4 and FP2 x4 PCIe routed to P1	0
	XMC Mezzanine slot on x1 PCIe (VITA61, up to Gen3), FP1 x4 and FP2 x4 PCIe routed to P1, no front connectors	1
	XMC Mezzanine slot on x4 PCIe (VITA61, up to Gen3), FP1 x1 and FP2 x4 PCIe routed to P1, no front connectors	2
Covers	no VITA 48 2LM covers	0
	VITA 48 2LM covers	1
Rear I/O Profile	P1 = PCIe (see XMC option), 2* 1GbKX/10GbKR. P2 = 1x 1000BASE-T, 1x DP++, 1x SATA, 1x USB2, 1x USB3, XMCIOs, according to MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15-2 module profile	E
	P1 = PCIe (see XMC option), 2* 10Gb SFI. P2 = 1x 1000BASE-T, 1x DP++, 1x SATA, 1x USB2, 1x USB3, XMCIOs, according to MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15-2 module profile	O
Front I/O Profile	No Front I/O connectors	N
	Front I/O : 2x 1000BASE-T, 1x mDP, 1x USB-C, Serial	F
M.2 profile	PCIe/SATA on TOP 2242 up to D5 and M Key M.2 slot, no M.2 bottom slot	0
On-board RTC Power	RTC Power sourced from system VPX VBAT	0
	RTC Power sourced from battery	1
System Management	VITA 46.11 Support	V
	No system management for safety critical applications	S
Secure Element	TPM 2.0 Secure element	1
SW Option	No PBIT	0
	Power on Built in Test Run Time	P
	PBIT RT & Preloaded Linux on Eval M.2 256GB 3D TLC (3k cycles) SSD	Q

1.3.4. I/O Interfaces

› Front Interfaces

Figure 5: SA variant - Front Panel with LED indicators and reset button (front view of an ECL 3xxxxyy board)



LED indicators and the RST button locations may slightly differ depending on the product ECL. Please refer to the product release note for more information.

Figure 6: RC variant - Front Panel with LED indicators and reset button (front view of an ECL 3xxxxyy board)

LED indicators and the RST button locations may slightly differ depending on the product ECL. Please refer to the product release note for more information.

Table 5: Front Panel - Interfaces

FUNCTION	DESCRIPTION	SEE ALSO
RST	Reset push button	Front Interfaces
Lx	LED indicators reporting the board CPU health status and activity	Section 4.4 for LEDs Description

The front panel push button must be handled with care. Use a non-metallic and blunt tool with a rounded tip (tip diameter must be roughly equal to the front panel button surface)

› Rear Interfaces
VX3060-S2 SOSA variant with the Compute Intensive manufacturing options:
- Compatible with slot profile SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16
- Module profile MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15-2

Refer to Section 5.3 for detailed VPX pin assignments and interfaces.

1.3.5. Components Layout

Figure 7: Components Layout (Top view)

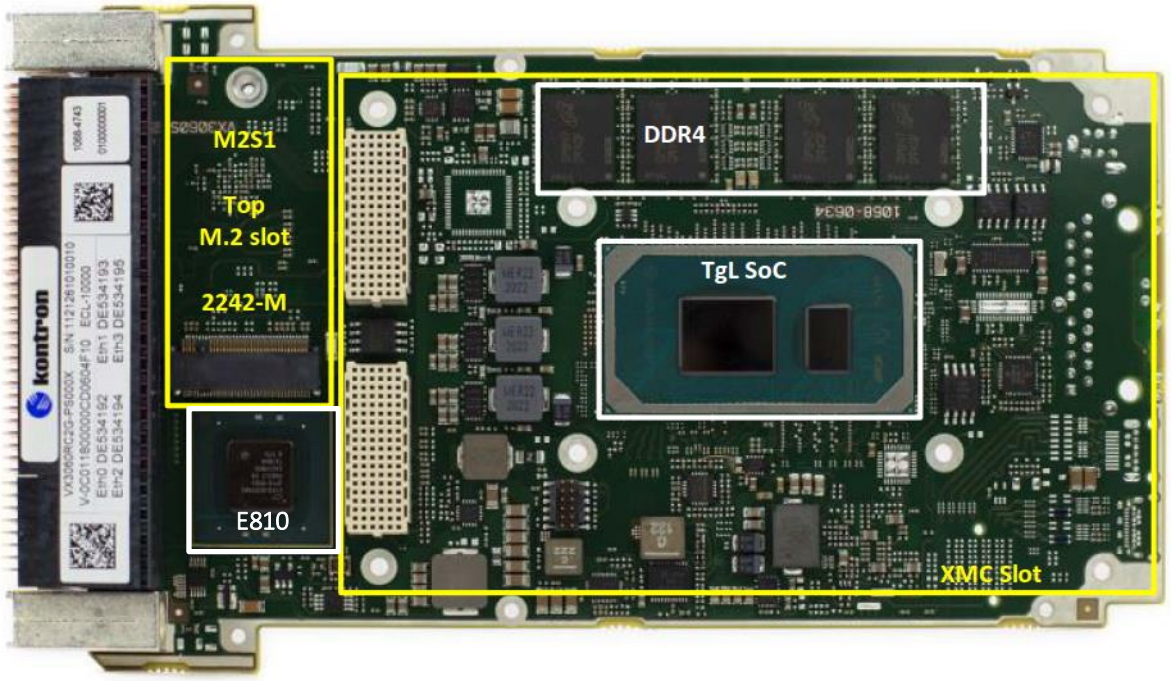
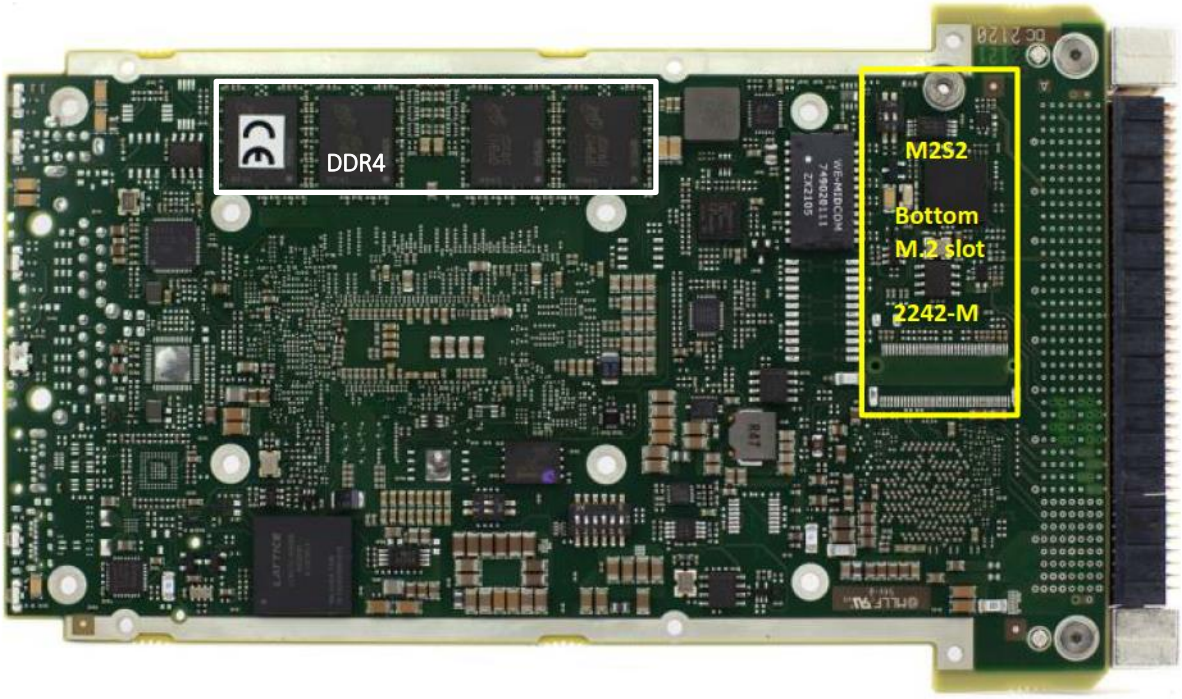


Figure 8: Components Layout (Bottom view)



Product aspect (mechanical covers and layout) may slightly differ depending on the product ECL.

Important note: the bottom M2S2 slot is not available on standard VX3060-S2 COTS variants. Contact Kontron.

1.3.6. Tested M.2 Module List

Table 6: Tested M.2 module list for the product (not exhaustive)

Module Type	Tested slot	Upstream interface option selected on the M.2 socket	Capacity	Memory Technology	Manufacturer	Part Number
SSD SATA, Type 2242 M	M2S1	SATA	256GB	3D TLC	Innodisk	DEM24-B56DK1GW1DL(-P62)
SSD SATA, Type 2242 M	M2S1	SATA	60GB	MLC	Virtium	VSFBM4XI060GB
SSD NVME, Type 2242 M	M2S1	PCIe x1	1TB	3D TLC	Innodisk	DEM24-01TDD1GWAQF

1.4. Environmental Specifications

The applicable environment class depends on the ordered VX3060-S2 variant

Table 7: VX3060-S2 –Environmental Specifications for Standard and Extended Classes

VX3060-S2 Environmental class	SA Standard Commercial	WA Extended Temperature
Plugin unit type	3U VPX Module Vita 46.0 October 2007 specification, Type2, corrected by REDI VITA 48.1 July 2010 (5HP)	3U VPX Module Vita 46.0 October 2007 specification, Type2, corrected by REDI VITA 48.1 July 2010 (5HP)
Conformal Coating	Optional	Standard
Airflow	Refer to section 5.7	Refer to section 5.7
Cooling Method	Convection	Convection
Operating	0 °C to +55 °C (1) (4)	-20 °C to +65 °C (1) (4)
Storage	-40 °C to +85 °C	-45 °C to +100 °C
Vibration Sine (Operating)	1 hour per axis: 5-20 Hz, displacement 1.25mm 20-500 Hz, 2g, Sweep rate 1 octave / minute	1 hour per axis: 5-20 Hz, displacement 1.25mm 20-500 Hz, 2g, Sweep rate 1 octave / minute
Random (Operating)	1 hour per axis: 5 Hz to 100 Hz, 0.04 g^2/Hz	1 hour per axis: 5 Hz to 100 Hz, 0.04 g^2/Hz
Shock (Operating)	20 g, 11 ms, half-sine	20 g, 11 ms, half-sine
Relative Humidity	90 % without condensation (95 % without condensation and with coating option)	95 % without condensation

Table 8: Environmental Specifications for Rugged classes

VX3060 Environmental class	RA Rugged Air-cooled	RC Rugged Conduction cooled
Plugin unit type	3U VPX Module Vita 46.0 October 2007 specification, Type2, corrected by REDI VITA 48.1 July 2010 (5HP)	5HP, Type 2, secondary side retainers
Conformal Coating	Standard	Standard
Airflow	Refer to section 5.7	NA
Cooling Method	Convection	Conduction
Operating	-40 °C to +70 °C (1) (3) (4)	Variant dependent (2) (3) (4) -40 °C to +70 °C or -40 °C to +85 °C
Storage	-50 °C to +100 °C	-50 °C to +100 °C
Vibration Sine (Operating)	1 hour per axis: 5-19 Hz, displacement 1.25 mm 19 -2000 Hz, 3g, Sweep rate 1 octave / minute	1 hour per axis: 5-22 Hz, displacement 2.5 mm 22-2000 Hz, 5 g
Random (Operating)	1 hour per axis: 5hz to 100Hz, +3dB/octave 100Hz to 1000Hz, 0.04g^2/Hz 1000Hz to 2000Hz, -6dB/octave	Product withstand vibration as defined below, 1 hour per axis: 5 Hz to 100 Hz PSD increasing at +3 dB/octave 100 Hz to 1000 Hz PSD = 0.1 g^2/Hz 1000 Hz to 2000 Hz PSD decreasing at -6 dB/octave
Shock (Operating)	20 g, 11 ms, half-sine	40 g / 11 ms, half sine
Altitude (Operating)	-1,500 to 60,000 ft	-1,500 to 60,000 ft
Relative Humidity	95 % without condensation	95 % without condensation

(1) According to Thermal characterization performed in laminar flow bench following Kontron procedure. The maximum allowed temperature depends on the processor TDP.

(2) Maximum temperature measured at card edge in the following conditions: processor performance rate @80% all cores, maximum processor TDP without CPU throttling. The maximum allowed temperature depends on the processor TDP.

(3) The maximum processor temperature range during operation is 90°C, starting from boot time temperature. This range can be extended to 110°C with PCIe Gen3 limitations. The behavior is described in Intel documents #734746 and #684987 as DTR = Dynamic Temperature Range. For more information, contact Kontron Support.

(4) Severity levels applicable to the baseboard without any M.2 or XMC module equipped on the board. Ask Kontron for product variants with M.2 or XMC module options equipped.

Table 9: Lab-grade Environmental Specifications for Prototypes or EVAL Variants

Lab-grade air-cooled version (1.5" single height passive module heat sink, forced air)	
Conformal Coating	optional
Inlet Airflow	3 m/s
Cooling Method	Convection or conduction
Operating	10 °C to +30 °C
Known product limitations	Refer to the active release note for detailed information. Ask Kontron.
Other specifications	According to standard lab conditions The use case as per EU directive is applicable: custom built evaluation kits destined for professionals to be used solely at research and development facilities for such purposes

Lab-grade conduction cooled version	
Conformal Coating	Optional
Cooling Method	Conduction
Max card edge Operating Temperature	0 °C to +30 °C
Known product limitations	Refer to the active release note for detailed information. Ask Kontron.
Other specifications	According to standard lab conditions The use case as per EU directive is applicable: custom built evaluation kits destined for professionals to be used solely at research and development facilities for such purposes

1.5. Board Weight/Mass

Table 10: Board Weight / Mass

VX3060-S2 Mass	
VX3060-S2-RC34G-21EN00V10 RC with XMC option & Without any module	~ 550 g
VX3060-SA4F-00PF01C1P SA without any module	~ 650 g

1.6. MTBF

Table 11: MTBF

MTBF at sea level Calculations according to MIL-HDBK-217F Notice 2 and ANSI/VITA 51.1-2008, corrected by Kontron field data	GB (Hours)	
	25 °C	40 °C
VX3060-S2-RC34G-21EN00V10 Without any M.2 module	410 000 hrs	325 000 hrs

Other profiles MTBF values on demand.

1.7. Related Publications

The publications listed below provide you with information about this product:

Table 12: Related publications

Standards	Version	Publication
ANSI/VITA 46.0	ANSI/VITA 46.0-2007[R2013]	VPX Baseline Standard
ANSI/VITA 46.9	March 2018	XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules
ANSI/VITA 46.10	ANSI/VITA 46.10-2009	Rear Transition Module for VPX
ANSI/VITA 46.11	June 2015	System Management on VPX
ANSI/VITA 65.0	ANSI/VITA 65.0-2019	OpenVPX™ System Specification
ANSI/VITA 65.1	November 2019	OpenVPX System Standard – Profile Tables
ANSI/VITA 48.2	ANSI/VITA 48.2-2010	Mechanical Specifications for Microcomputers using REDI Conduction Cooling Applied to VITA VPX
ANSI/VITA61	ANSI/VITA 61.0-2022	XMC 2.0

Product	Version	Publication
VX3060-S2	D291798	VX3060-S2 Hardware Release Note
VX3060	D258115	AMI-BIOS User Reference Manual
VX3060	D234669	PBIT User Guide
VX30xx product family	D218432	VITA 46.11 Firmware Release Note
VX3060	D275280	Kontron VME/VPX Fedora 36 Remix Release Notes
Kontron SSD Solution	D276285	Kontron SSD Solution
VX3060	D276230	VX3060-S2 how to use SFP+CAGE

2. Installation

The VX3060-S2 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

2.1. Safety Requirements

The following safety precautions must be observed when installing or operating the VX3060-S2. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

This board contains electrostatically sensitive devices. Observe the necessary precautions to avoid damage to your board:
Discharge your clothing before touching the assembly. Tools must be discharged before use.
Do not touch components, connector pins or traces.
We strongly recommend our customers to work in an environment equipped with antistatic workbenches with professional discharging equipment.

HOT Surface!
Special care shall be taken while handling the board: the heat sink or heat frame can get very hot during operation. Do not touch the heat sink when installing or removing the board.
In addition, the board should not be placed on any surface or in any form of storage container before the board and heat sink have cooled down to room temperature.

2.2. Board Identification

The VX3060-S2 boards can be identified by the labels on the top side of the board.
The E.C. Level format is "xxxxxLy" where

- The five digits "xxxxx" indicate the board E.C. Level (PCB revision included)
- "Ly" indicates the mechanical E.C. Level:
  - letter "L" varies with the environment class ("A" for SA, "B" for WA, "C" for RA and "D" for RC)
  - digit "y" gives the mechanical E.C. Level.

› Top Side

(A) "Identification" label: Order Code, Serial Number, Variant, E.C. Level, Ethernet MAC addresses

Figure 9: Main Product Label location (Top Side)

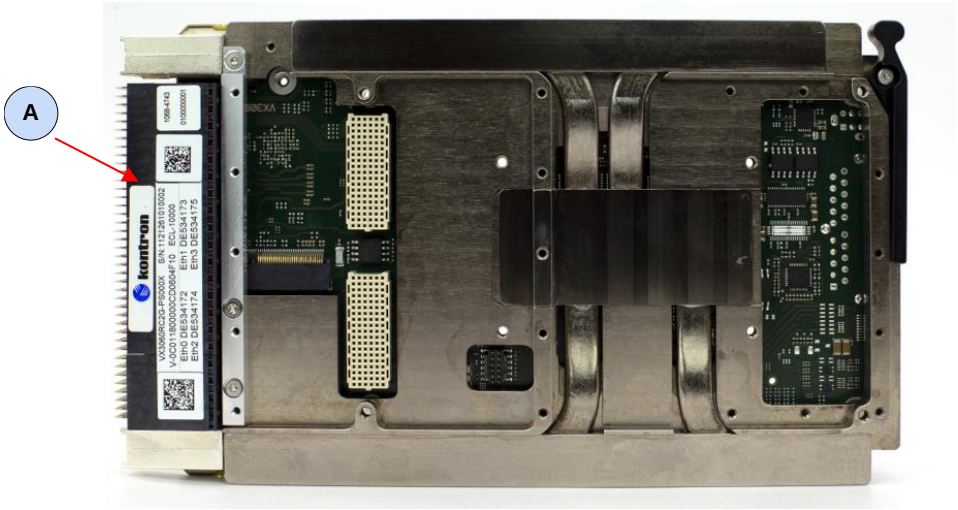
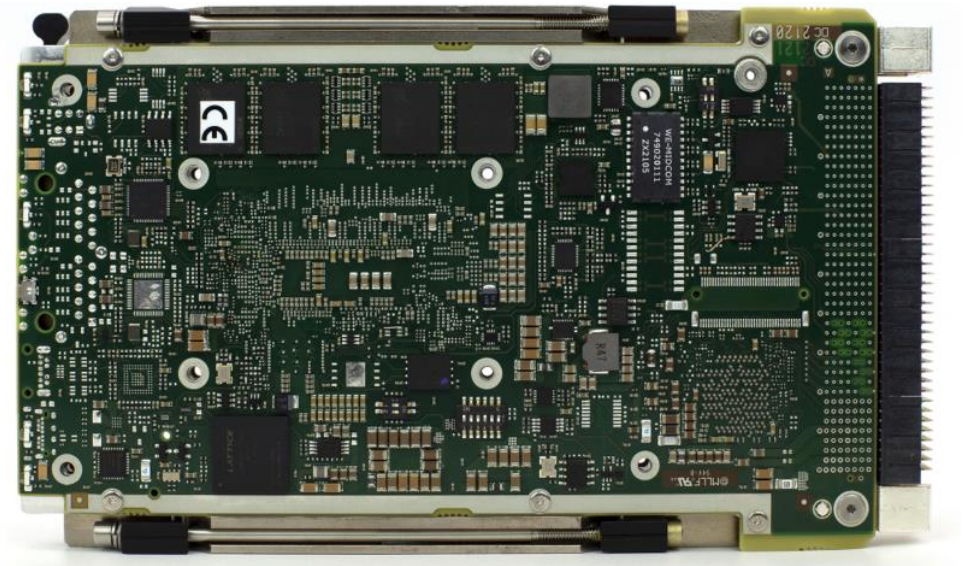


Figure 10: Product identification (Bottom Side)

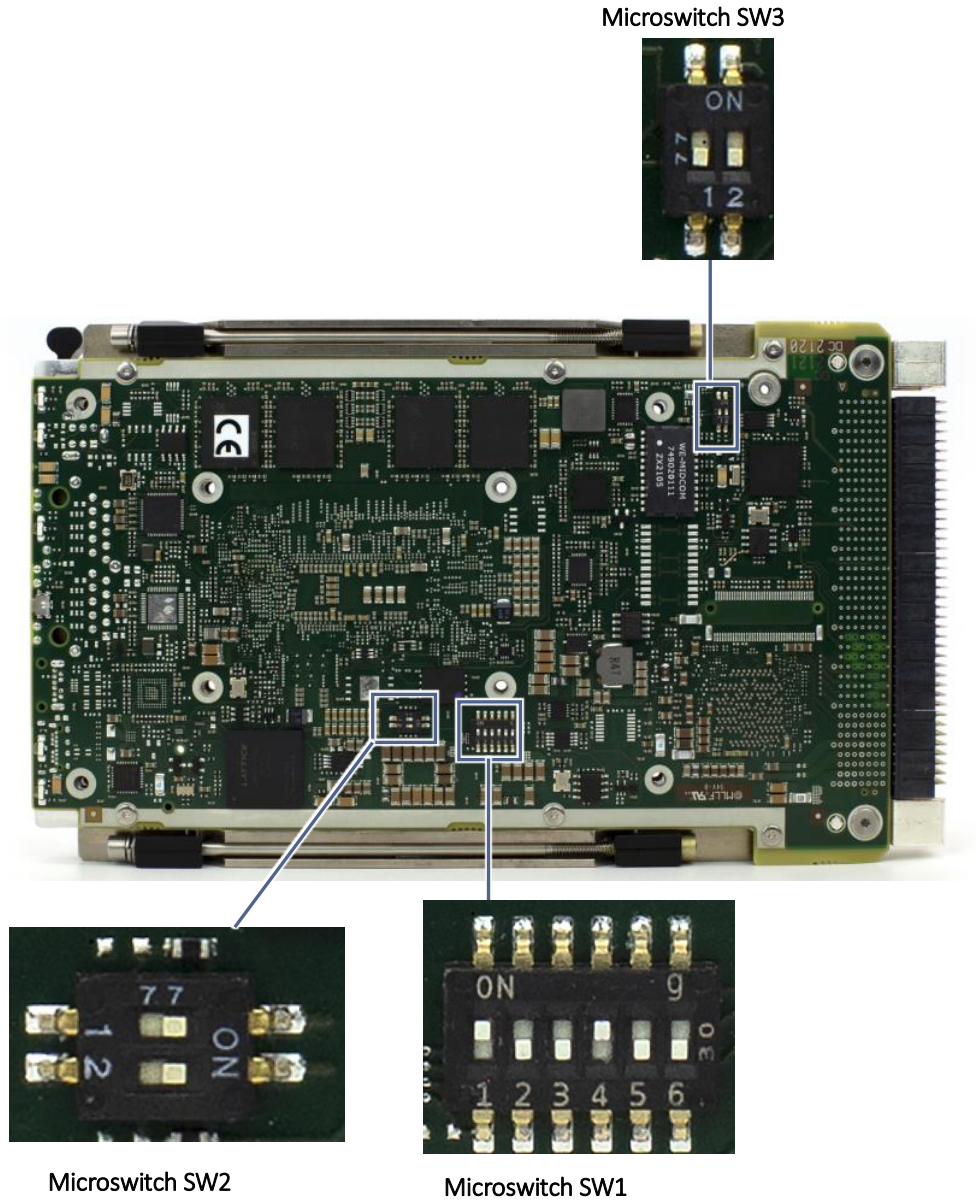


Product aspect (mechanical covers and layout) may slightly differ depending on the product ECL

2.3. Board Configuration

2.3.1. Microswitches Location

Figure 11: Board Configuration – Micro Switches location (Bottom view)



Product aspect (mechanical covers and layout) may slightly differ depending on the product ECL

2.3.2. SW1 Microswitch Description

Table 13: SW1 Microswitch Description

SW1		
#	Function	Description
1	FACTORY_MODE	OFF: default mode for normal operation ON : enable special config for factory tests (NVMRO masked, …)
2	VPD_WP	OFF: “VPD” domain protected as defined in section 3.8 ON : force **unprotection** of devices in “VPD” domain (see "Write protection")
3	USER_WP	OFF: “USER” domain not protected as defined in section 3.8 ON : force protection of devices in “USER” domain (see "Write protection")
4	DBG_MODE	OFF: default mode for normal operation ON : debug mode enabled
5	BIOS_FAILSAFE	OFF: default mode for normal operation ON : start software in failsafe mode for recovery purpose
6	CS_SWAP	OFF: boot on the normal BIOS flash device ON : boot on rescue BIOS flash device (swap of CS0/CS1 SPI boot flash chip select)

Refer to Section 3.8 for detailed information about the NVMRO and existing write protection levels

2.3.3. SW2 Microswitch Description

Table 14: SW2 Microswitch Description

SW2		
#	Function	Description
1	FORCE_PROCHOT	OFF: default mode for normal operation ON : PROCHOT (1) forced to CPU (through PLD_FORCE_PROCHOT#)
2	NVMRO_OFF	OFF: default mode for normal operation ON : force NVMRO off on backplane and on local board

Note (1): When configured as a bi-directional signal, PROCHOT# can be used for thermally protecting other platform components should they overheat as well. When PROCHOT# is driven by an external device:

- *The package will immediately transition to the lowest P-State (Pn) supported by the processor IA cores and graphics cores.*
- *Clock modulation is not activated.*

2.3.4. SW3 Microswitch Description

Table 15: SW3 Microswitch Description

SW3 only for VX3060-S2 with IPMI option		
#	Function	Description
1	BMC_PROG	OFF: default mode for normal operation ON : enable IPMC console to serial connector COM2 (default) or to Soc COM2 (for debug or programming)
2	SW3_SPARE	Spare switch

2.4. Package Contents

The package contents vary with the VX3060-S2 variant.

- VX3060-S2 variant - see section “Ordering Information”. Board equipment differs depending on the ordered Order Code.
- Bolt accessories for mezzanine/module mounting

2.5. Initial Installation Procedures

The following procedures are applicable only for the initial installation of the VX3060-S2 in a system. Procedures for standard removal operations are found in their respective chapters.

To perform an initial installation of the VX3060-S2 in a system, proceed as follows:

1. Ensure that the safety requirements indicated in section 2 are observed.

CAUTION: Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For the configuration and installation of VX3060-S2, specific peripheral devices and Rear I/O devices refer to the appropriate sections in current Chapter.

CAUTION: Care must be taken when applying the procedures below to ensure that neither the VX3060-S2 nor other system boards are physically damaged by the application of these procedures.

3. To install the VX3060-S2, perform the following:

a. Ensure that no power is applied to the system before proceeding.

b. Select the slot where the board should be inserted as per application requirements. Then carefully insert the board until it makes contact with the backplane connectors.

Conduction Cooled variants: when performing the next step and when the chassis accommodating the board is compliant with VITA48.2, it is recommended to use the ejector handles to seat the board into the backplane connectors. For the other chassis, simply push the board into the backplane connectors.

c. Engage the board with the backplane using the ejector handle until the handle is locked. In RC configurations (no handle or handle not locked), push the board until it is fully seated in the backplane.

d. RC class board type: Tighten the wedgelocks to the cold plate using a torque of 0.68 N.m on the wedgelock screw

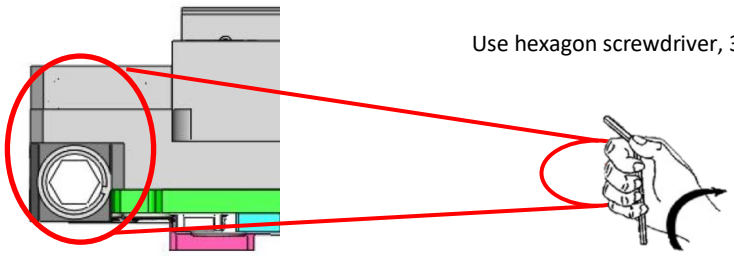
e. Ensure that the board is properly secured.

The VX3060-S2 is now ready for operation. Refer to the relevant VX3060-S2 software, application, and system documentation.

Figure 12: Air Cooled variant - Screws Location on the front panel

Use Phillips PH1 screwdriver or equivalent

Figure 13: Conduction Cooled variant - Wedgelock Screw Location



Use hexagon screwdriver, 3/32'' IMPERIAL

⚠CAUTION

Running the board at high temperature without tightening the wedgelocks to the cold plate may result in permanent damage to the board.

2.6. Standard Removal Procedure

ESD sensitive Device! Precautions are listed in Section 2

To remove the board from the chassis, proceed as follows:

1. Ensure that the safety requirements indicated in Section 2 are observed. Particular attention must be paid to the warning regarding the heat frame!

⚠CAUTION

CAUTION: Care must be taken when applying the procedures below to ensure that neither the VX3060-S2 nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Loosen the wedgelocks or front panel screws
4. Disengage the board from the backplane using the board ejection handle. Press the handle until the board is disengaged.
5. After disengaging the board from the backplane, pull the board out of the slot.

HOT Surface!
Due care should be exercised when handling the board due to the fact that the heat frame can get very hot. Do not touch the heat frame when changing the board.

6. Dispose of the board as required.

2.7. XMC Removal Procedure

ESD sensitive Device! Precautions are listed in Section 2

Apply "Loctite 222e" threadlock on each screw during reassembly of the XMC

Supported XMC type

The default XMC connectors are VITA 61 XMC 2.0 compliant and support PCI-Express interface.

XMC IOs connector (J16) is equipped by default.

The XMC stack is 12 mm.

XMC installation

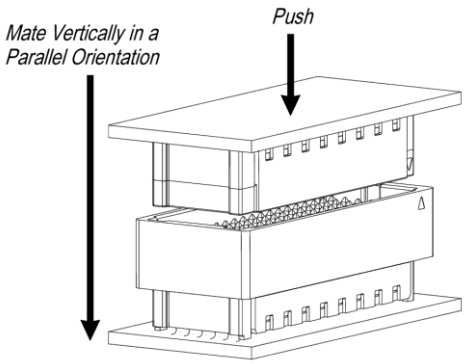
To install an XMC on a RC variant, proceed as follows:

1. If the VX3060-S2 board is plugged in the chassis, follow the procedure described in Section 2
2. For RC variants, remove the XMC cover mounted on the heat frame if any. Discard nylon washers.
3. Align the XMC connectors. Press to fully engage the XMC.

⚠CAUTION

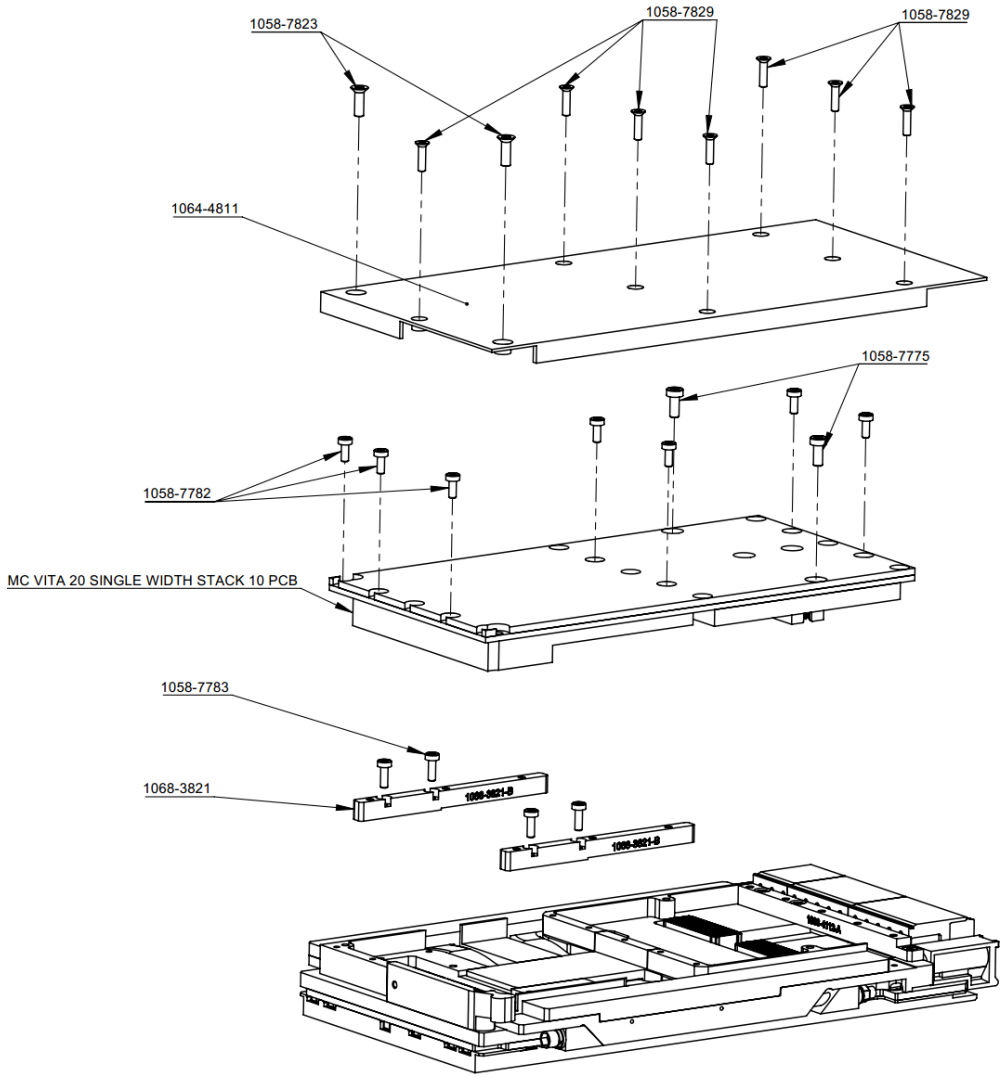
The XMC connectors should be mated straight: Align the connectors and when the keys start to enter the keyways, push at the approximate center of the connector into the mating connector until the face of the receptacle cover bottoms on the face of the plug. Because of the asymmetric keying, reverse mating is impossible (the key end of the receptacle cannot be inserted into the non-keyway end of the plug). Both connectors have a perimeter lead-in for blind mating.

Figure 14: XMC Module Insertion



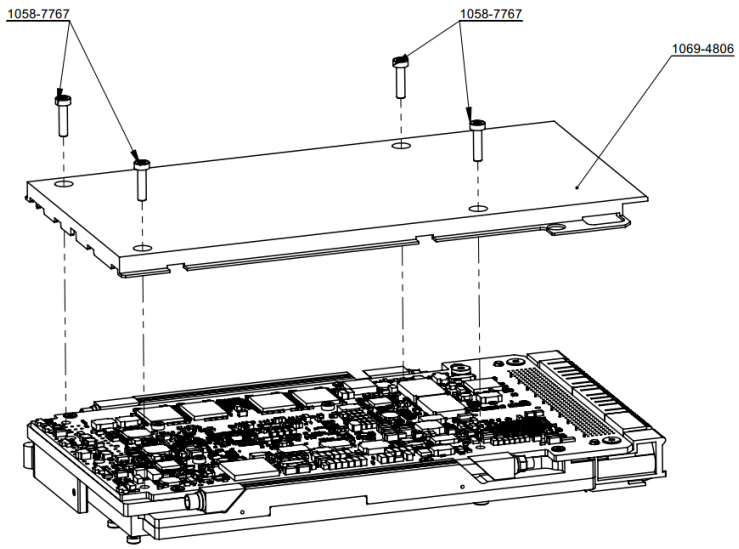
4. Screw the XMC in place using the appropriate mounting points as depicted in Figures 14 and 15. Screw the XMC cover if any using nine mounting points.

Figure 15: XMC and XMC cover Installation on a AFT board type



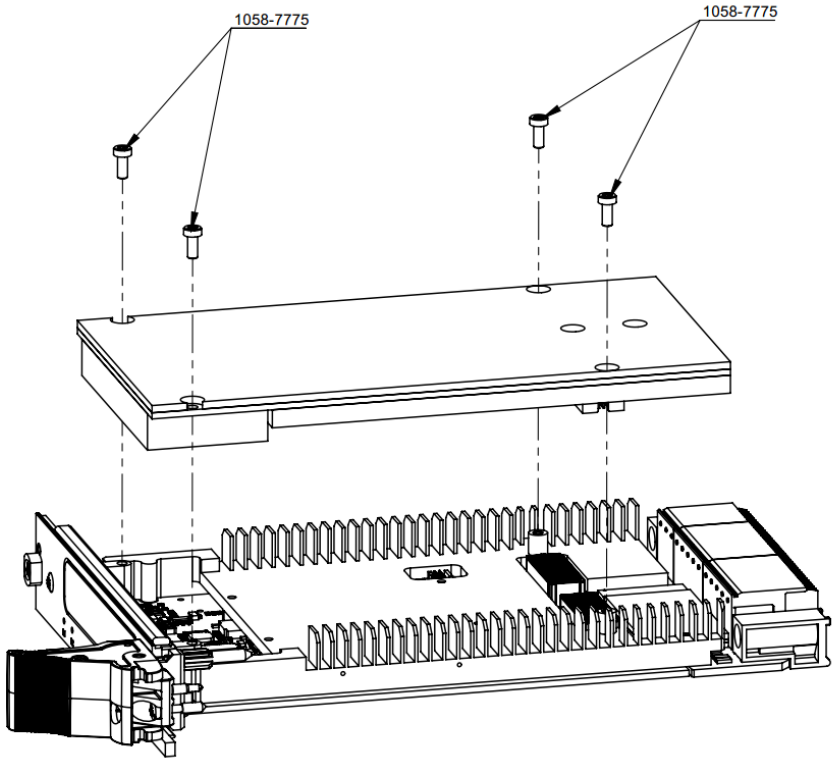
Article	Description	Qty	Torque	Thred lock
1064-4811	XMC cover	1	-	
1058-7782	HEXALOBULAR SOCKET CHEESE HEAD SCREW ISO 14580-M2X5-A4-70	7	0.14 N.m	Loctite 222e Or equivalent
1058-7775	HEXALOBULAR SOCKET CHEESE HEAD SCREW ISO 14580-M2.5X6-A4-70	2	0.28 N.m	
1058-7783	HEXALOBULAR SOCKET CHEESE HEAD SCREW ISO 14580-M2X6-A4-70	4	0.2 N.m	
1058-7829	COUNTERSUNK FLAT HEAD SCREW ISO 14581-M2X8-A4-70	7	0.2 N.m	
1068-3821	RIB VITA20	2	-	
1058-7823	COUNTERSUNK FLAT HEAD SCREW ISO 14581-M2.5X8-A4-70	2	0.4 N.m	Loctite 222e Or equivalent

Figure 16: Bottom cover Installation on a RC board type



Article	Description	Qty	Torque	Thred lock
1058-7767	HEXALOBULAR SOCKET CHEESE HEAD SCREW ISO 14580-M2.5X10-A4-70	4	0.4 N.m	Loctite 222e Or equivalent

Figure 17: XMC Installation on a SA class board type

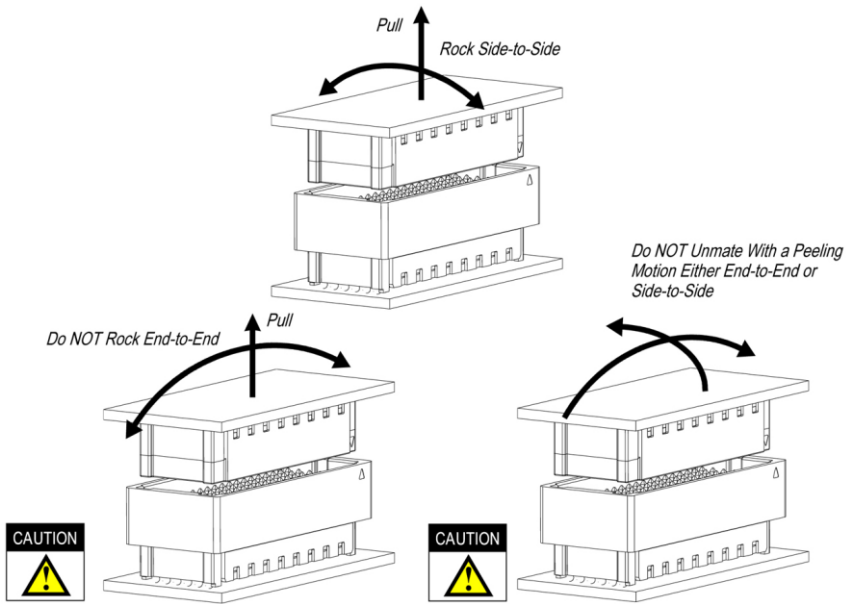


Article	Description	Qty	Torque	Thred lock
1058-7775	HEXALOBULAR SOCKET CHEESE HEAD SCREW ISO 14580-M2.5X6-A4-70	2	0.28 N.m	Loctite 222e Or equivalent

Unmating

The XMC connectors can be unmated by pulling them straight apart or by “rocking” the connectors from side-to-side while pulling them apart.

Figure 18: XMC Module Removal



2.8. M.2 Module Insertion / Removal Instructions

› M.2 Module Insertion Process

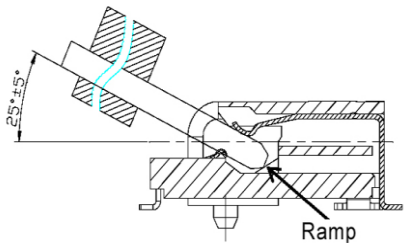
	ESD sensitive Device! Precautions are listed in Section 2
	Apply "Loctite 222" threadlock or equivalent on each screw during reassembly of the M.2 module

1. If 2LM cover option is present, Disassemble the bottom M.2 cover according to the bottom cover procedure. Remove flat washer and hexagon thin nut. See figures below.

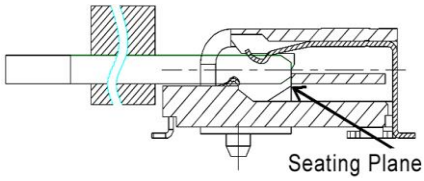
2. For VX3060-S2 variants requiring a standoff (in a separate bag included in packaging), place the standoff above the mounting hole.

M.2 Module Insertion

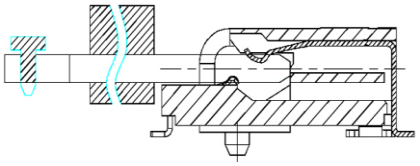
3. Insert the module at an angle of 25°±5° until the module makes contact with the ramp



4. Rotate the module to a horizontal position and ensure that the edge of the card is in contact with the seating plane.

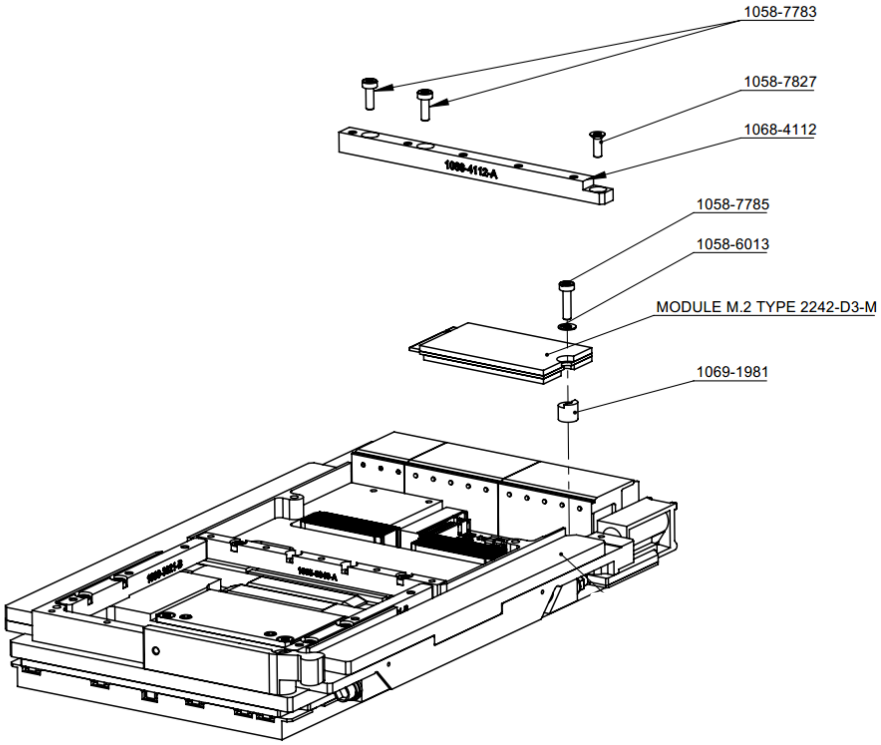


6. Attach the module using appropriate mechanical parts (washer, nut or screw) as described in figures below.



6. For rugged variants, adhesive is required as shown in pictures below.

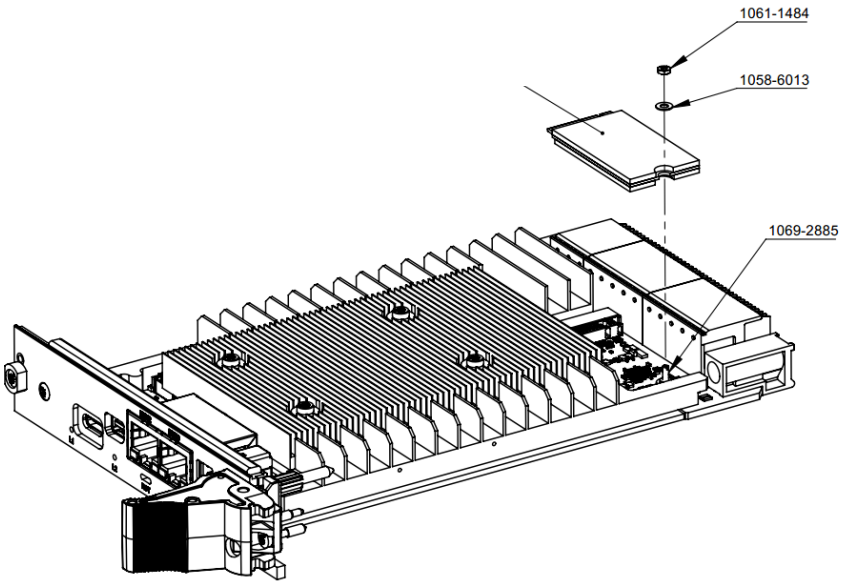
Figure 19: Top M.2 Module Insertion on a RC board type (M2S1 slot)



Article	DESCRIPTION	Qty	Torque	Thread lock
1058-6013	WASHER ISO 7092-2-200HV-A4	1	-	-
1069-1981	M.2 SSD H5.2 spacer	1	-	-
1058-7785	HEXALOBULAR SOCKET CHEESE HEAD SCREW ISO 14580-M2X8-A4-70	1	0.14 N.m	Loctite 222e Or equivalent
1058-7783	HEXALOBULAR SOCKET CHEESE HEAD SCREW ISO 14580-M2X6-A4-70	3	0.2 N.m	
1058-7827	COUNTERSUNK FLAT HEAD SCREW ISO 14581-M2X6-A4-70	1	0.2 N.m	

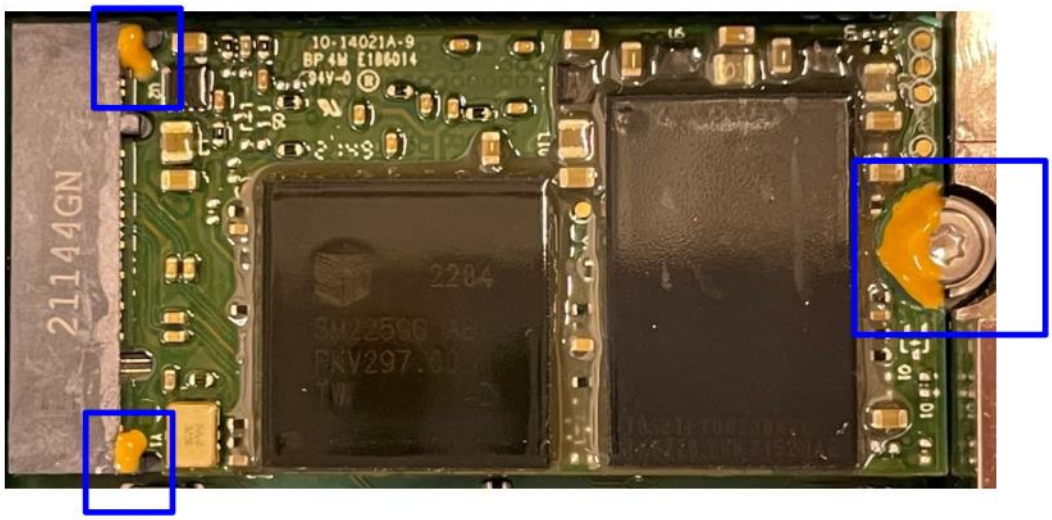
Figure 20: M.2 Module Insertion with threaded rod previously installed.

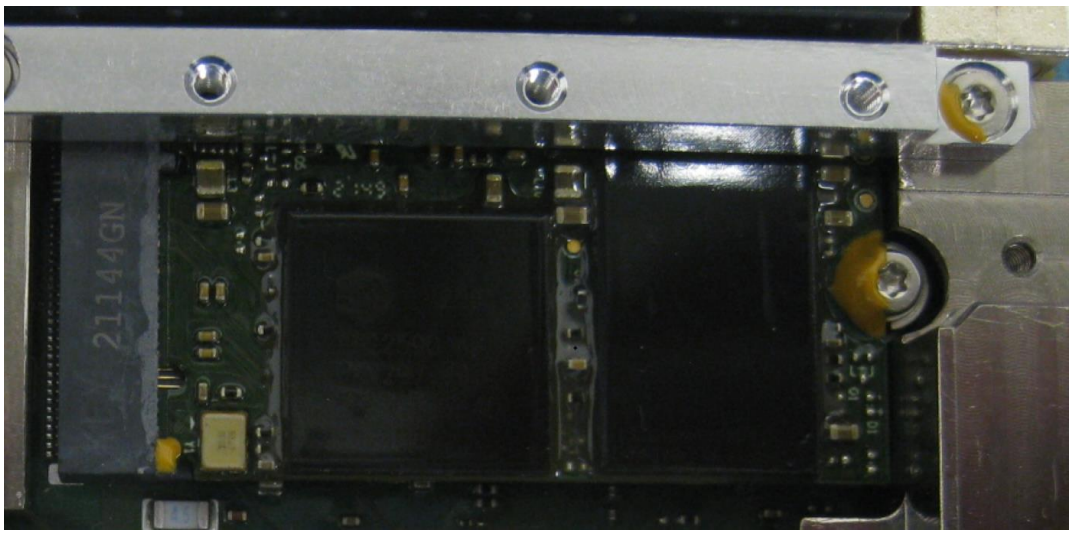
This figure shows an example of module assembly onto the top M2S1 slot.



Article	DESCRIPTION	Qty	Torque	Thread lock
1058-6013	WASHER ISO 7092-2-200HV-A4	1	-	-
1061-1484	HEXAGON THIN NUT ISO 4035-M1.6-A4-70	1	0.09 N.m	Loctite 222e Or equivalent

Figure 21: Adhesive application example to lock M.2 Module on AFT or RC class rugged boards

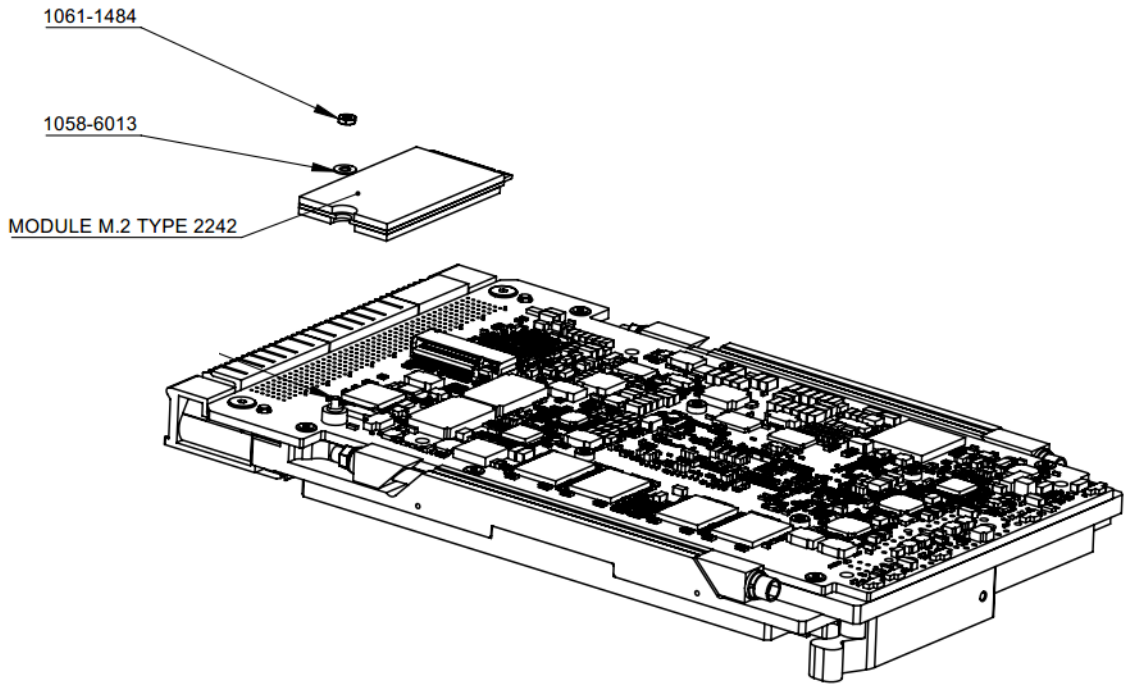




⚠CAUTION

For harsh environment applications, Kontron recommends to apply adhesives to lock the M.2 module. Such as 3M Scotch-Weld™ 7838, or equivalent: at the junction between the module and the M.2 connector/screw (Blue rectangles on the pictures above)
If a XMC mezzanine card is equipped above the M.2 module, the overall height (including adhesive) should not exceed the required 6.7 mm. This operation may be performed at Kontron on demand.
All screws must be locked with Loctite 222 or equivalent thread lockers

Figure 22: M.2 Module Insertion in Bottom Side M2S2 Slot (For Information Only)

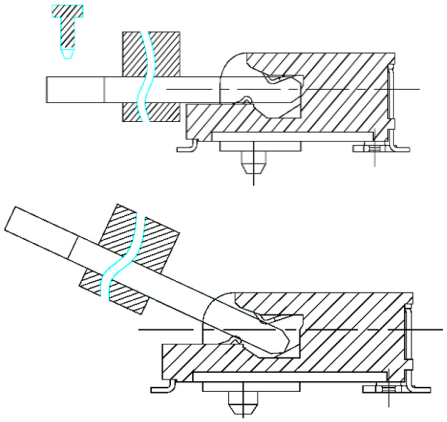


Article	DESCRIPTION	Qty	Torque	Thread lock
1058-6013	WASHER ISO 7092-2-200HV-A4	1	-	-
1061-1484	HEXAGON THIN NUT ISO 4035-M1.6-A4-70 (with threaded rod previously installed)	1	0.09 N.m	Loctite 222e Or equivalent

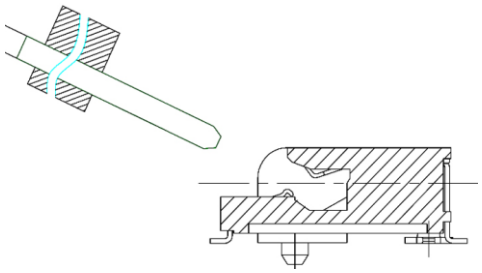
› M.2 Module Removal Process

Figure 23: M.2 Module Removal Process

1. After loosening the screw, the module will lift by itself due to the counterforce of the contacts in the connector.



2. Remove the module manually.



2.9. Software Installation

The installation of all on-board peripheral drivers is described in detail in the relevant Driver Kit files or Board Support Packages (BSP).
The installation of an operating system is dependent of the OS software and is not addressed in this manual.
Refer to appropriate OS software documentation for software installation.

2.10. On-Board Battery option

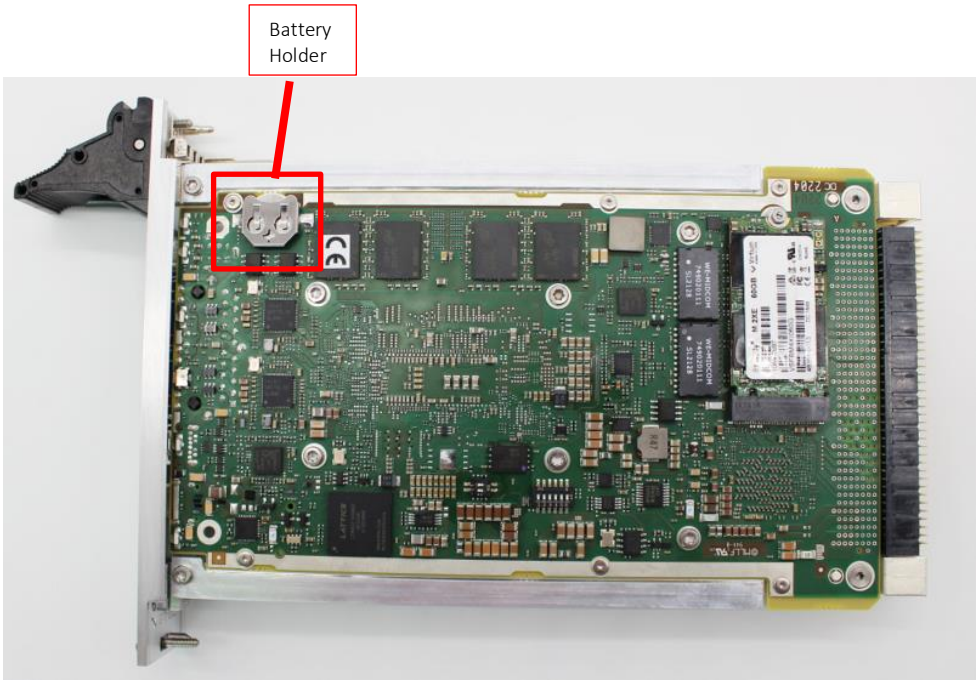
On VX3060-VX3060-S2, the battery is available only as an on-demand option.

- Battery Part Number

Reference of the battery for SA class product: RENATA CR1220 MFR (-30/+70°C)
Reference of the battery for RA class product: RAYOVAC BR1225X-BA (-40/+85°C)

- Battery Replacement

Figure 24: Battery Holder Location when the option is present



To replace the battery, proceed as follows:

1. Turn off power.
2. Use a thin plastic tool to push the battery out of its holder.

NOTICE Do not subject the holder to mechanical stress when inserting the tool to eject battery.

3. Remove the battery.
4. Place the new battery into the socket with positive side (+) upwards and negative side (-) closest to printed circuit board

⚠CAUTION Danger of explosion when replacing with wrong type of battery. Replace only with the same or equivalent type recommended by the manufacturer. The lithium battery type must be UL recognized.

NOTICE Do not subject the battery to extreme temperatures, such as in contact with fire or into an oven. Do not dispose the battery where it could be expose to extreme temperatures, or in contact with stuff susceptible to cut or crush the battery.
Do not expose the battery to extremely low air pressure.
Not respecting those warnings could cause an explosion and/or the leak of flammable substances.

Do not dispose of lithium batteries in general trash collection. Dispose of the battery according to the local regulations dealing with the disposal of these special materials, (e.g. to the collecting points for dispose of batteries).

3. Additional Board Feature

3.1. RTC, Watchdog, Timers

3.1.1. Real-Time Clock (RTC)

Two Real Time Clocks (RTC) are available on the VX3060-S2: one is embedded in the CPU while the other is a standalone, high-precision, low-power component (RV-8803) accessed through the PCH SMBus.

- **Standby power supplied to the RV-8803 RTC**
  When the VX3060-S2 is powered off, the RTC power supply comes either from the VPX 3.3V_AUX rail or from the VPX VBAT rail. To ensure data retention in the RV-8803 RTC, the VPX VBAT must be set in the range [2.5V - 5.5V]. The maximum current drawn over the -40 °C/+85 °C temperature range is 500 nA (VBAT= 3 V, no I2C activity) or 550 nA (VBAT=5 V, no I2C activity).

- **Internal Integrated PCH RTC**
  The integrated PCH RTC module provides a date and time keeping device with two banks of static RAM with 128 bytes each although the first bank has 114 bytes for general-purpose usage. The BIOS programs the RTC interrupt on Legacy IRQ8 that is never shared with other interrupts. It is clocked by an external 32.768 KHz oscillator with a parabolic coefficient of 0.4 ppm/°C² and a stability of +/-20 ppm at 25 °C. A 20 ppm stability is equivalent to a 10 mn/year drift.

- **Standalone low-power RTC RV-8803**
  The RV-8803 RTC by Micro Crystal includes an internal oscillator and a date and time keeping module with programmable alarm, timer and interrupt functions. It features an ultra low-power consumption in time keeping mode: 240 nA typical and 800 nA maximum in worst case conditions.
  RV-8803 offers a very high Time Accuracy (best in class): ±1.5 ppm 0 to +50°C, ±3.0 ppm -40 to +85°C, ±7.0 ppm +85 to +105°C.

- **RTC management by BIOS and OS**
  At each startup, the BIOS retrieves the date and time information from the high-precision RV-8803 RTC and copies it into the integrated PCH RTC.
  Any update of date and time in the BIOS settings will be done both in integrated PCH RTC and RV-8803 RTC.
  Regarding the RTC management by the OS, the OS should use the high-precision RV-8803 RTC driver. Failing to do so, the updates will be done only in integrated PCH RTC and will not be saved.
  If no power is applied on the RV-8803 RTC, the BIOS displays the BIOS build date and time instead of the current date and time.

- **Century flag**
  For compatibility reasons, the BIOS implements the century flag for the high-precision RTC as follows:
    - Century Flag C = 0 for 1900-1999 years
    - Century Flag C = 1 for 2000-2099 years.

  The user should check that the OS driver implements the same convention.

3.1.2. CPLD Watchdog

In addition to the standard watchdog timer included in the integrated PCH, the cPLD implements a hardware watchdog timer that can be used by the operating software to monitor the normal operation of the system.
It is enabled by software, and once enabled must be restarted at regular intervals. If not, its expiration sets off an interrupt (IRQ) to the local processor, a board reset or a board power-cycle.
The watchdog has the following features:

- timeout programmable from 1 to 511 clock periods, by steps of 2 periods
- clock periods of 1s or 1ms
- lock bit: when set, can only refresh (restart) the watchdog, but not change its settings
- 4 modes: timer, reset, interrupt or power-cycle
- restart counter: can manage the remaining number of resets or power-cycles done by the watchdog before giving-up.
- pre-timeout interrupt (dual-stages)

3.2. I2C Structure

The VX3060-S2 features several I2C busses.

- attached to the integrated Platform Hub Controller
- handled by the CPLD device and by the IPMC device
- Two IPMA/B to the VPX rear panel are handled by the cPLD or the IPMC (manufacturing option)

Figure 25: I2C Block Diagram for information (RES means manufacturing options)

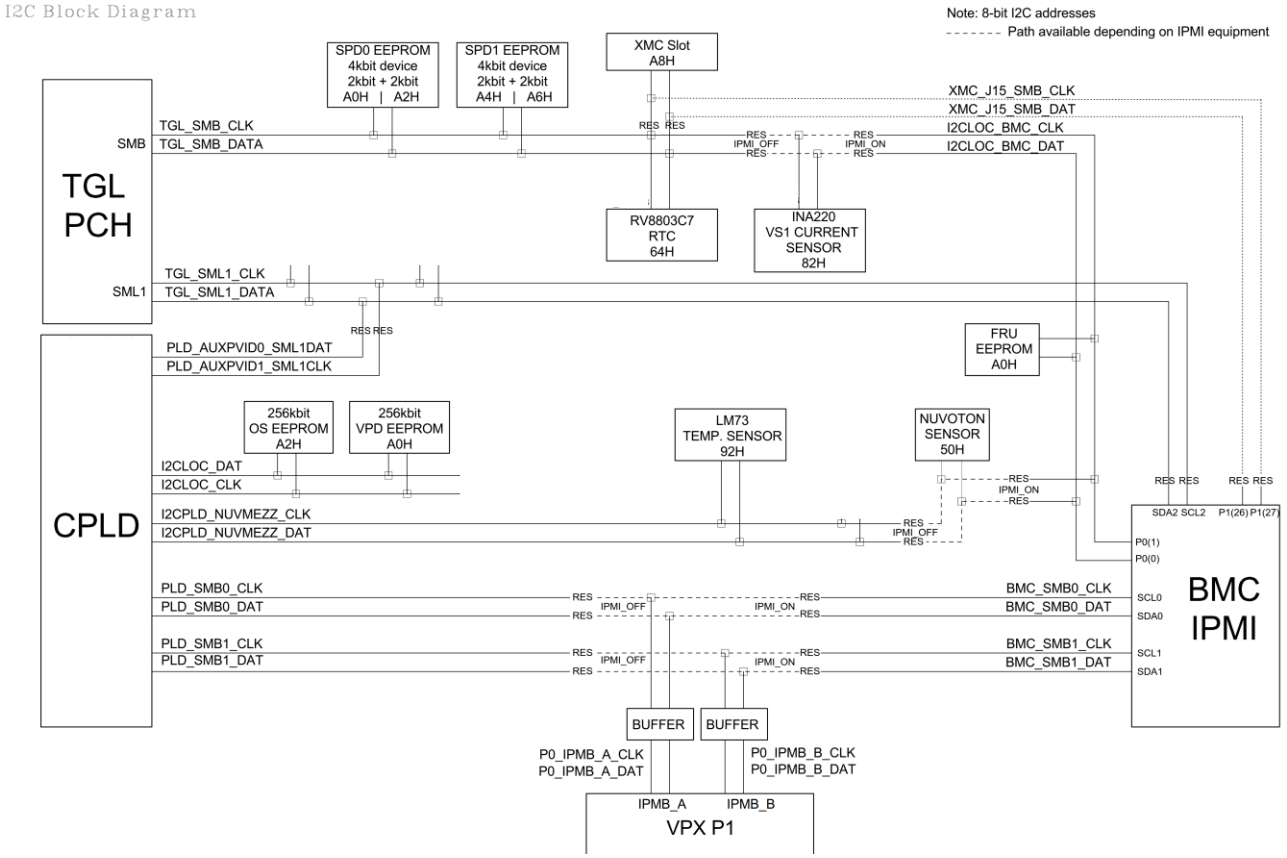


Table 16: End user I2C device list

End User Device	Size	Bus	SMBUS BASE ADDRESS (8-bit / 7-bit)	FEATURES
INA220	-	SMB Legacy	82H / 41H	VS1 Current Monitoring
RV-8803	-	SMB Legacy	64H / 32H	External RTC Device
XMC Slot	-	I2C IPMC (cPLD)	A8H / 54H	To XMC Mezzanine SMBus
VPD EEPROM	Up to 512 Kbit	I2C cPLD	A0H / 50H	ECL < ECL-3xxxxyy: 256 Kbit devices equipped by default ECL= ECL-3xxxxyy: 512 Kbit devices equipped by default
OS EEPROM	Up to 512 Kbit	I2C cPLD	A2H / 51H	ECL < ECL-3xxxxyy: 256 Kbit devices equipped by default ECL= ECL-3xxxxyy: 512 Kbit devices equipped by default
CY15B102QN F-RAM	2 Mbit	SPI	-	2 Mbit user F-RAM
NCT7802Y sensor	-	I2C IPMC (cPLD)	50H / 28H	Nuvoton Voltage / Temperature Sensor
LM73 temperature sensor	-	I2C cPLD	92H / 49H	ECL < ECL-3xxxxyy: LM73 is not option available ECL= ECL-3xxxxyy: LM73 is option available

3.3. EEPROM Mapping

On-board EEPROM mapping are in the following tables

Table 17: VPD and OS EEPROM mapping

VPD EEPROM I2c @ (A0H) Global Mapping

EEPROM addresses	Description
0x0000 – 0x100	Board Vital Product Data
0x100 - 0x300	Reserved (Optional VPD - MAC address …)
0x300 - 0x7FFF	Free Area
0x8000 - 0xFFFF	Free area (area available if ECL = ECL-3xxxxyy)

OS EEPROM I2c @ (A2H) Global Mapping

EEPROM addresses	Description
0x0000 – 0x1400	Free for OS (used by Linux BSP)
0x1400-0x2000	PBIT Reserved (Factory Test Information)
0x2000- 0x3000	PBIT Test List/Test/Rescue list …
0x3000-0x4000	Reserved PBIT
0x4000- 0x5000	PBIT System Test Config and Recorded Information
0x5000-0x6000	Reserved PBIT
0x60F0 -0x612F	CPLD Power ON Config Data
0x6130-0x7FFF	Free area
0x8000 - 0xFFFF	Free area (area available if ECL = ECL-3xxxxyy)

3.4. Main CPLD Features

The CPLD manages the following features:

- Power-on/off control
- Reset control
- LPC interface to processor (through eSPI/LPC bridge to eSPI processor interface)
- KCS interface to IPMC
- LEDs control
- Serial lines multiplexer
- Serial VPD and user memories
- User and system GPIOs
- Internal registers dedicated to system management
- I2C master/slave interfaces

› cPLD Register

cPLD registers are accessible from CPU through LPC bus. See cPLD registers overview in sections of Linux Kontron VME/VPX Fedora Remix – Release Note. Contact Kontron for a detailed description of the CPLD registers.

3.5. Serial Lines Modes

› Serial ports location

Serial lines are available both on front (see serial connector in section 4.1 Front Panel) and rear (VPX P1 & P2 connectors in sections 4.3.2 to 4.3.6).

› Serial ports pin assignment

Refer to section 4.1.1 - “Serial Connector” for front connector and sections 4.3.2 to 4.3.6 for rear P1 & P2.

› Protocol selection

COM1 port on VPX P1: default mode is EIA-232 protocol. Mode can be set to LVCMOS through BIOS settings
COM2 port on VPX P2: default mode is EIA-232 protocol. Mode can be set to EIA-422/485 through BIOS settings along with associated options (on-board 120 Ohms termination, half-duplex mode).

3.6. User GPIOs and GDISCRETE1

3.6.1. GPIOs

The VX3060-S2 variants offers up to four GPIOs and two LVDS GPI managed by the CPLD depending on the product variant. Refer to section related to VPX pin assignments for the exact location and availability. Refer also to the Software Release Notes for further details about the GPIO driver.

- One user GPIO is available on VPX P1 connector
- One GPIO with dual purpose GPIO/Maskable_Reset is available on VPX P1 connector
- Three user GPIOs are available on VPX P2 connector

These GPIOs are 3.3V logic and are NOT 5V tolerant (maximum voltage is 3.6V). When set as output, the drive strength is 8mA (sink or source). When set as input, there's a hysteresis of ~250mV. A weak pull-up of 47KOhms is present on all GPIOs

The GPIOs share the same interrupt in the CPLD.

CAUTION: GPIOs are not 5V tolerant. Maximum voltage on GPIOs is 3.6 V. Absolute maximum voltage is 3.75V and is not suitable for continuous operation. Appropriate voltage reduction (through resistor divider for instance) must be made to avoid permanent damage to the board.

3.6.2. GDISCRETE1

GDISCRETE1 is a bussed open-collector GPIO defined by OpenVPX VITA 65 and available on P1. See section “VPX P1 Connector” for detailed pinout.

It is handled by the CPLD and buffered by a SN74LVC1G125 buffer wired as an Open Collector to meet the electrical characteristics defined in VITA 65.

It has a dedicated interrupt in the CPLD.

3.6.3. Time-Aware GPIO (TGPIO)

VX3060-S2 hardware support the use of Intel® Time Coordinated Computing (Intel® TCC).

Intel® TCC Tools offer three feature categories which are real-time configuration and optimization, time synchronization and communication, and measurement and analysis.

Two Time Aware General Purpose IOs (TGPIOs) of the processor are connected to the cPLD.

If ECL = ECL-3xxxxyy, two additional TGPIO are available: one from the E810 controller and one from the i225/i226 Ethernet controller are also connected to the cPLD.

cPLD can be configured to connect de two processor TGPIOs to other GPIOs available on the VPX (GDISCRETE1, GPIO1…) or to the VPX clock sources (AUX_CLK, REF_CLK) to allow several time synchronization modes.

Please refer to software documentation in the related publication section for more information..

3.7. Reset

Table 18: Reset Management Table

RESET SOURCE	RESET ACTION	RESET CONTROL	RESET STATUS	NOTE
Front panel push button	Platform reset	Front panel push button	I2C_BOARD_STATUS @0x72	Reset propagation options and masks available in cPLD registers
VPX Sysreset	Platform reset	VPX P0 / Row B/ Wafer 4	I2C_BOARD_STATUS @0x72	See VPX Vita46.0 standard Reset propagation and mask options available in cPLD registers
VPX maskable reset	Platform reset	VPX P1 / Row G/ Wafer 15	I2C_BOARD_STATUS @0x72	See VPX Vita46.0 standard
cPLD watchdog reset	Platform reset	Refer to the Fedora Remix Release note	I2C_BOARD_STATUS @0x72	Refer to the Fedora Remix Release note
Processor watchdog reset	Platform reset	Refer to the Intel Tiger Lake watchdog feature and control registers	Refer to the Intel Tiger Lake watchdog feature and control registers	Refer to the Intel Tiger Lake watchdog feature and control registers
cPLD software reset	Platform reset	I2C_BOARD_CONTROL @0x73	I2C_BOARD_STATUS @0x72	Refer to the cPLD control/status registers

3.8. NVMRO

NVMRO is defined by the VITA 46.0 standard.
VX3060-S2 is designed to meet Standard for SOSA™ Reference Architecture, Edition 1 / Rule 6.4.2-4.

M.2 SSD may be protected if the installed SSD module supports the Write Protect signal (WP#) on the pin 58 of the M. 2 Socket. To achieve this, the Intel ME writes in the boot flash device when board is operating, preventing from a full boot flash hardware write protection in normal operation.
Please contact Kontron support for more information.

Table 19: NVMRO - Write Protections

Memory	Part Ref	Size	Fully Write protected when NVMRO is asserted	Write protected level	Possible HW Write Protections	Writable During Operation With HW Write protection disabled	Function	Existing Writing tool If HW Write protection is disabled	Proposed sanitization procedure
DC/DC controller MP2962	MP2962GVT-3001-Z (U5601) Monolithic Power Systems	Proprietary	-	VPD	None. No User access.	No	VR configuration	None	No user access. Sanitization not required.
USB Power Delivery CYPD5225	CYPD5225-96BZXI (U3501, U4501) CYPRESS	Proprietary	-	VPD	None. No User access.	No	VR configuration	None	No user access. Sanitization not required.
SDRAM EEPROM	M24C04-RMC6TG (U0301, U0401) ST MICROELECTRONICS	2 x 4 Kbit	Yes	VPD	NVMRO MicroSwitch SW4903[2] MEM_PROTECT Register (see product manuals)	Yes	SDRAM size and timing information storage	Kontron BIOS/kspd	Turn off WP and erase data. **The product will no longer work after sanitization.**
VPD EEPROM	24FC256T-I/SN or 24FC512T-I/SN MICROCHIP	Up to 512Kbit	Yes	VPD		Yes	Storage of board configuration data	Kontron BIOS/BSP commands	Turn off WP and erase data The product may no longer work or will behave badly after sanitization.
SYS EEPROM	24FC256T-I/SN or 24FC512T-I/SN MICROCHIP	Up to 512Kbit	Yes	SYSTEM	NVMRO MicroSwitch SW4903[2] MEM_PROTECT Register (see product manuals)	Yes	User/System data	Kontron BIOS/BSP commands	Turn off WP and erase data
i225/i226 Flash Memory	W25Q16CVSNIG (U2503, U2603) WINBOND	16 Mbit	**No**	VPD	**Intel proprietary, no direct user access when operating**	Yes	Config and Ethernet controller address	**Intel Lanconf/Eeupdate**	Turn off WP and erase data The product will behave badly after sanitization.
FLASH in cPLD	LCMXO2-4000HC-4BG256ITR (U4701) LATTICE	256Kbit	Yes	USER	NVMRO MicroSwitch SW4903[2] MEM_PROTECT Register (see product manuals)	Yes	Storage for cPLD configuration data	Kontron BIOS/kpld	Turn off WP and erase data **The product will no longer work after sanitization**.
FRAM	CY15B102QN-50SXE (U4007) CYPRESS	2 Mbit	Yes	USER		Yes	Storage of user data	Kontron PBIT/BSP commands	Turn off the WP and erase data using the API and driver provided in the Linux BSP.
BOOT FLASH	W25Q256JVEIQ Or W25Q512JVEIQ WINBOND	Up to 2x 512 Mbit	**No**	, USER	**Intel proprietary ME writes required**	Yes	Boot and Rescue Boot Flash devices	Kontron BIOS/kflash	Turn off WP and overwrite data with the BIOS/kflash command. **The product will no longer work after sanitization**.
E810/10GbE Flash Memory	W25Q128JVSIQ (U2702) WINBOND	128 Mbit	**No**	VPD	**Intel proprietary, no direct user access when operating**	Yes	Config and Ethernet controller address	**Intel Lanconf/Eeupdate**	Turn off WP and erase data. The product may no longer work or will behave badly after sanitization.
XMC module	Customer part	NA	Yes	SYSTEM	NVMRO MicroSwitch SW4903[2] MEM_PROTECT Register	Yes	Customer use case	Standard LinuxOS API	Turn off WP and overwrite data with the Standard LinuxOS API or customer API. The product may behave badly after sanitization.

3.9. IPMI Option

The IPMI option is implemented by default on VX3060-S2 variants.
Contact the Kontron Technical support for more information related to the product options.

The VX3060-S2 embeds an IPMI controller so that the VX3060-S2 is considered as a FRU as per VITA 46.11. The IPMI controller is accessible through an IPMB bus or through a host Keyboard Controller Style (KCS) interface.

The IPMC manages the following features:

- Local environmental control/monitoring
- I2C interfaces to I2C bus IPMB A/B (rear P0)
- KCS interface to CPLD
- Serial FRU memory
- IPMI watchdog
- System Event Log (SEL)
- Sensor Device functionality

For further detail about IPMI firmware, refer to VX3060-S2 IPMI Firmware Release Note D218432.

› VPX IPMB I2C interfaces

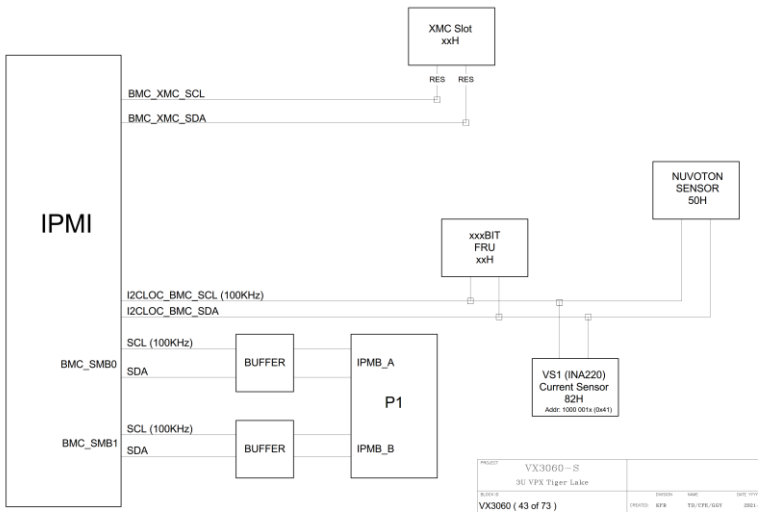
VX3060-S2 implements two I2C buses connected to P0 VPX connector. See section “VPX P0 Connector” for the detailed P0 pin assignments:

- IPMB A (I2C0) CLK on pin P0-B5, DATA on pin P0-A5
- IPMB B (I2C1): CLK on pin P0-G4, DATA on pin P0- F4

› IPMI commands available

The VX3060-S2 IPMI firmware supports all the Mandatory IPMC Tier-1 and Tier-2 commands. See the exhaustive list of IPMI supported commands in the VX3060-S2 IPMI Firmware Release Note.

IPMI block diagram overview



3.10. Security Solution

The VX3060-S2 answers digital security requirements with hardware enforced root of trust (secure elements). The VX3060-S2 supports SEC-Line computer security offering:

- **TRUSTED BOOT**: Detect system software alteration
- **AUTHENTICATION WITH TPM**: Secure network protocols

If needed customers can customize the solution to meet specific needs. For more information, contact Kontron Support.

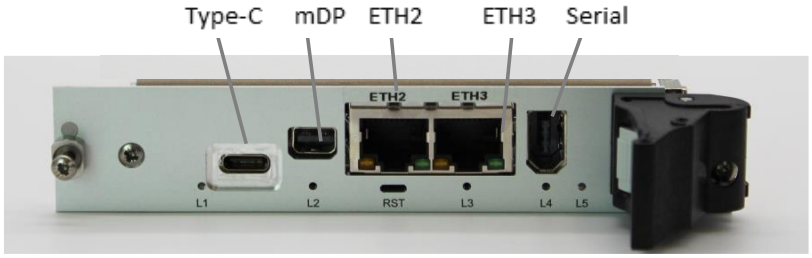
- **Trusted Platform Module (TPM 2.0)**

The VX3060-S2 is compliant with TPM 2.0 standard. A Trusted Platform Module (TPM) stores RSA encryption keys specific to the host system for hardware authentication.

4. Physical IO

4.1. Front panel

Front panel connectors equipment according to the ordered product variant.



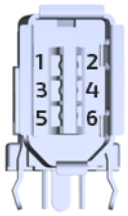
4.1.1. Front panel

This section describes the IEEE 1394 front connector carrying serial ports COM1

Table 20: Serial Connector Pin Assignment

Pin	Signal
1	Reserved
2	GND
3	COM1 RXD / RXD_485-
4	COM1 CTS / RXD_485+
5	COM1 TXD / TXD_485-
6	COM1 RTS / TXD_485+

Figure 26: Serial Connector (IEEE 1394 Type)



NOTICE

Serial lines are routed to both front panel connector and rear P2. Plugging a serial device to both connectors will lead to electrical contention. Be sure to use only one connector at a time.

Table 21: Serial Connector Signals Definition

Signal	Dir.	Definition
COM1 TXD / TXD_485-	O	EIA-232: Transmit Data of port COM1 EIA-485: Transmit Data minus of port COM1
COM1 RXD / RXD_485-	I	EIA-232 Receive Data of port COM1 EIA-485: Receive Data minus of port COM1
COM1 RTS / TXD_485+	O	EIA-232: RTS of port COM1 EIA-485: Transmit Data plus of port COM1
COM1 CTS / RXD_485+	I	EIA-232: CTS of port COM1 EIA-485: Receive Data plus of port COM1
Reserved	-	Reserved
GND	-	Logic ground
Shell	-	Chassis ground

Note: EIA-485 protocol requires special configuration. Contact Kontron.

- Serial Cable Description

Table 22: Standard Serial Cable Description

Conn. A IEEE1394	Signal	Conn. B SUBD9
5	TXD	2
3	RXD	3
2	GND	5

Standard Kontron serial cable : Order code 1064-4995 (SERIAL CABLE IEEE1394/SUBD9 F)

4.1.2. Gigabit Ethernet Connector - Ports ETH2 & ETH3

This section describes the dual RJ45 front connector carrying 1000BASE-T Ethernet ports ETH0 & ETH1.

- Front Gigabit Ethernet Connector Description

Table 23: Gigabit Ethernet Connector Pin Assignment

Pin	Signal
1	TX+ / BI_DA+
2	TX- / BI_DA-
3	RX+ / BI_DB+
4	BI_DC+
5	BI_DC-
6	RX- / BI_DB-
7	BI_DD+
8	BI_DD-
Shell	Chassis Ground

Figure 27: RJ45 Tab-down Ethernet Connector

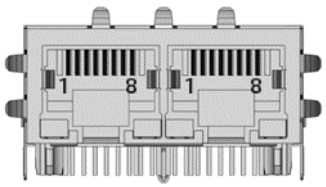


Table 24: Gigabit Ethernet Connector Signals Definition

Signal	Dir.	Definition
TX+/- / BI_DA+/-	I/O	10BASE-T & 100BASE-T: Transmit differential pair 1000BASE-T: BI_DA differential pair
RX+/- / BI_DB+/-	I/O	10BASE-T & 100BASE-T: Receive differential pair 1000BASE-T: BI_DB differential pair
BI_DC+/-	I/O	10BASE-T & 100BASE-T: NC 1000BASE-T: BI_DC differential pair
BI_DD+/-	I/O	10BASE-T & 100BASE-T: NC 1000BASE-T: BI_DD differential pair
Shell	-	Chassis ground

- Ethernet Cable Description

The Ethernet cable should be at least CAT5e, with a maximum length of 100 meters.

4.1.3. Standard FrontIO profile Option

4.1.3.1. miniDP Connector

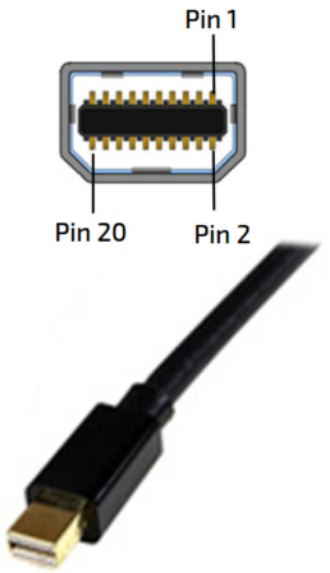
This section describes the front panel minDP connector carrying the Display port interface.

Table 25: miniDP connector – front panel

Table 7: Mini DisplayPort Pin Assignment

1	GND	Ground
2	HPD	Hot Plug Detect
3	Lane0+	Lane 0 Positive
4	Config1	Config1, dongle detect for dual-mode DP (mDP++)
5	Lane0-	Lane 0 negative
6	Config2	Config2, pulled low by XMC-GPU91
7	GND	Ground
8	GND	Ground
9	Lane1+	Lane 1 positive
10	Lane3+	Lane 3 positive
11	Lane1-	Lane 1 negative
12	Lane3-	Lane 3 negative
13	GND	Ground
14	GND	Ground
15	Lane2+	Lane 2 positive
16	Aux+	Auxilliary+
17	Lane2-	Lane 2 negative
18	Aux-	Auxilliary-
19	GND	Ground
20	PWR	Power (3.3V, 500 mA max)

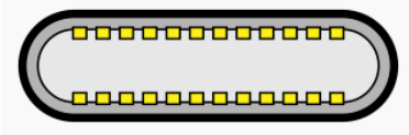
Figure 13: Mini DisplayPort Cable



4.1.3.2. Front panel USBC Connector – USB0

This section describes the USB-C front panel connector

Table 26: USB-C connector – front panel

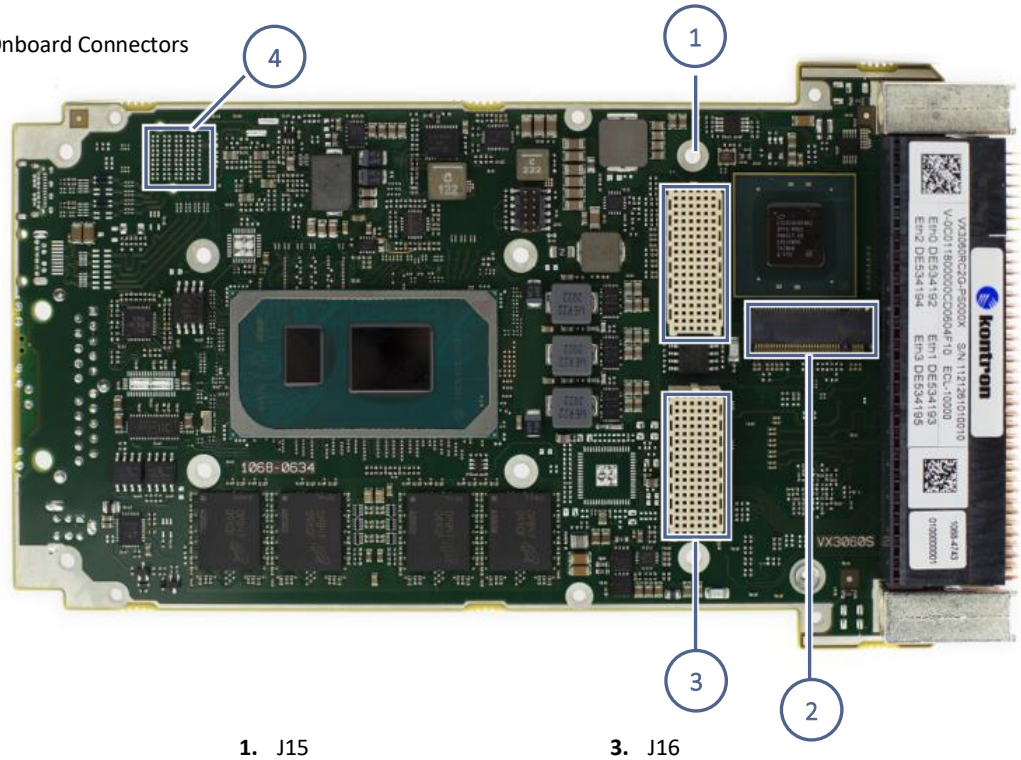


A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	NC	D1+	D1-	NC	VBUS	NC	NC	GND
GND	RX1+	RX1-	VBUS	NC	D2-	D2+	NC	VBUS	NC	NC	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Pin	Nom	Description	Pin	Nom	Description
A1	GND	Ground return	B12	GND	Ground return
A2	SSTXp1	SuperSpeed differential pair #1, TX, positive	B11	SSRXp1	SuperSpeed differential pair #1, RX, positive
A3	SSTXn1	SuperSpeed differential pair #1, TX, negative	B10	SSRXn1	SuperSpeed differential pair #1, RX, negative
A4	VBUS	Bus power	B9	VBUS	Bus power
A5	NC	CC1 Configuration channel	B8	NC	Sideband use (SBU2)
A6	D1+	USB 2.0 differential pair, position 1, positive	B7	D2-	USB 2.0 differential pair, position 2, negative
A7	D1-	USB 2.0 differential pair, position 1, negative	B6	D2+	USB 2.0 differential pair, position 2, positive
A8	NC	Sideband use (SBU1)	B5	NC	CC2 Configuration channel
A9	VBUS	Bus power	B4	VBUS	Bus power
A10	NC	SuperSpeed differential pair #2, RX, negative	B3	NC	SuperSpeed differential pair #2, TX, negative
A11	NC	SuperSpeed differential pair #2, RX, positive	B2	NC	SuperSpeed differential pair #2, TX, positive
A12	GND	Ground return	B1	GND	Ground return
USB 2.0 differential pair connects only in one position; position 2 is not physically present in the plug.					

4.2. Onboard Connectors

Figure 28: Onboard Connectors



1. J15
2. M2S1 slot **(**M.2 2242-M)
3. J16
4. Layer2 option

4.2.1. Optional - XMC J15 Connector Pin Assignments

The pin assignment of the J15 XMC PCI Express connector is compatible with VITA 61.0 pin definition. This interface is a PCI Express with 4 lanes coming from the CPU.

Table 27: XMC J15 Connector Pin Assignments

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	PCIe TX0+	PCIe TX0-	3.3V (3)	**[PCIe TX1+]**	**[PCIe TX1-]**	VPWR (1)
2	GND	GND	TRST#	GND	GND	MRSTI#
3	**[PCIe TX2+]**	**[PCIe TX2-]**	3.3V (3)	**[PCIe TX3+]**	**[PCIe TX3 -]**	VPWR (1)
4	GND	GND	TCK	GND	GND	N.C.
5	NC	NC	3.3V (3)	NC	NC	VPWR (1)
6	GND	GND	TMS	GND	GND	+12V
7	NC	NC	3.3V (3)	NC	NC	VPWR (1)
8	GND	GND	TDI	GND	GND	-12V
9	Reserved	Reserved	NC	Reserved	Reserved	VPWR (1)
10	GND	GND	TDO	GND	GND	GA0
11	PCIe RX0+	PCIe RX0-	MBIST (2)	PCIe RX01+	PCIe RX1-	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT#
13	**[PCIe RX2+]**	**[PCIe RX2-]**	3.3V AUX	**[PCIe RX3+]**	**[PCIe RX3-]**	VPWR (1)
14	GND	GND	GA2	GND	GND	MSDA
15	NC	NC	NC	NC	NC	VPWR (1)
16	GND	GND	NVMRO	GND	GND	MSCL
17	NC	NC	NC	NC	NC	NC
18	GND	GND	NC	GND	GND	NC
19	REFCLK+0	REFCLK-0	NC	WAKE#	N.C.	NC

(1) Note (1): VPWR is connected to +12V via a fuse.

(2) Note (2): MBIST only available if ECL = ECL-3xxxxyy

(3) Note (3): 3 Amps rated fuse protection on the XMC 3V3 Rail if VX3060-S2 in ECL < ECL-3xxxxyy, and 4 Amps if in ECL=ECL-3xxxxyy

Signals active when low.

The ordered product manufacturing options may alter the J15 pin assignment. Contact Kontron.
Important note: [….] means manufacturing options, signal present if the related option is ordered

Table 28: XMC J15 Signal Description

MNEMONIC	DIRECTION	SIGNAL DEFINITION
VPWR	O	+12 Volts DC power pin.
+12V	O	+12 Volts DC power pin.
-12V	O	-12 Volts DC power pin.
3.3V	O	+3.3 Volts DC power pin.
3.3V AUX	O	Auxiliary +3.3 Volts.
GA[0..2]	O	I2C channel select as per VITA42.0.
GND	-	Ground
MRSTI#*	O	XMC Reset In as per VITA42.0 (10 ms pulse min.) and PCIe PERST# as per VITA42.3.
MSDA	I/O	I2C serial data as per VITA42.0.
MSCL	O	I2C serial clock as per VITA42.0.
MPRESENT#	O	Module present as per VITA42.0.
NC	-	Not Connected
RFU	-	Reserved
NVMRO	O	XMC Write Prohibit as per VITA42.0.

MNEMONIC	DIRECTION	SIGNAL DEFINITION
TCK/TDI/TDO/ TMS/TRST#	O	XMC JTAG chain as per VITA42.0. VX3060-S2 in ECL = ECL-3xxxxyy : XMC JTAG chain connected to the VPX P0 pins G7, E7, D7, B7, A7 VX3060-S2 in ECL < ECL-3xxxxyy: XMC JTAG chain not connected to VPX P0 pins.
TRST#	O	JTAG Reset as per VITA42.0.
PCIe_xx	I/O	Up to PCIe x4 differential transmit/receive pairs (as per VITA42.3)
REFCLK+/-0	O	100MHz PCIe differential reference clock as per VITA42.3.
WAKE#	I	Open drain WAKE# signal.

4.2.2. Optional - XMC J16 Connector Pin Assignments

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	XMCIO DP0+	XMCIO DP0-	NC	XMCIO DP01+	XMCIO DP01-	NC
2	GND	GND	NC	GND	GND	NC
3	XMCIO DP02+	XMCIO DP02-	NC	XMCIO DP03+	XMCIO DP03-	NC
4	GND	GND	NC	GND	GND	NC
5	**[XMCIO DP04+]**	**[XMCIO DP04-]**	NC	**[XMCIO DP05+**	**[XMCIO DP05-]**	NC
6	GND	GND	NC	GND	GND	NC
7	**[XMCIO DP06+]**	**[XMCIO DP06-]**	NC	**[XMCIO DP07+**	**[XMCIO DP07-]**	NC
8	GND	GND	NC	GND	GND	NC
9	**[XMCIO DP08+]**	**[XMCIO DP08-]**	NC	**[XMCIO DP09+**	**[XMCIO DP09-]**	NC
10	GND	GND	NC	GND	GND	NC
11	XMCIO DP10+	XMCIO DP10-	NC	XMCIO DP11+	XMCIO DP11-	NC
12	GND	GND	**[XMCIO SE15]**	GND	GND	**[XMCIO SE16]**
13	XMCIO DP12+	XMCIO DP12-	**[XMCIO SE13]**	XMCIO DP13+	XMCIO DP13-	**[XMCIO SE14]**
14	GND	GND	**[XMCIO SE11]**	GND	GND	**[XMCIO SE12]**
15	**[XMCIO DP14+]**	**[XMCIO DP14-]**	**[XMCIO SE09]**	**[XMCIO DP15+]**	**[XMCIO DP15-]**	**[XMCIO SE10]**
16	GND	GND	**[XMCIO SE07]**	GND	GND	**[XMCIO SE08]**
17	**[XMCIO DP16+]**	**[XMCIO DP16-]**	**[XMCIO SE05]**	**[XMCIO DP17+]**	**[XMCIO DP17-]**	**[XMCIO SE06]**
18	GND	GND	XMCIO SE03	GND	GND	XMCIO SE04
19	**[XMCIO DP18+]**	**[XMCIO DP18-]**	XMCIO SE01	**[XMCIO DP19+]**	**[XMCIO DP19-]**	XMCIO SE02

XMCIO signals are routed to VPX P2 connector, see VPX P1 and P2 pin assignments.
Important note: [….] means manufacturing options, signal present if the related option is ordered

Table 29: XMC J16 Signal Description

MNEMONIC	DIRECTIO	SIGNAL DEFINITION
XMCIO DPn+/-	I/O	XMCIO differential pair n (X12d/X8d mapping as per VITA 46.9)
XMCIO SEn	I/O	XMCIO single-ended signal n (X16s mapping as per VITA 46.9)
NC	-	Not Connected

4.2.3. M.2 Connector Pin Assignments

The M.2 top/bottom sockets are used to connect M.2 modules, key M for storage. The M.2 socket supports only the 2242 form factor.

PCIe or SATA mode can be selected using BIOS settings, and according to the product options.
Refer to VX3060-S2 Software release notes.

The top M.2 slot is named M2S1.
The bottom M.2 slot is named M2S2 (not available on standard VX3060-S2 COTS variants)

Table 30: M.2 socket connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	3V3
3	GND	4	3V3
5	NC	6	NC
7	NC	8	NC
9	GND	10	DAS/DSS#LED1#
11	NC	12	3V3
13	NC	14	3V3
15	GND	16	3V3
17	NC	18	3V3
19	NC	20	NC
21	GND	22	NC
23	NC	24	NC
25	NC	26	NC
27	GND	28	NC
29	PER1- (1)	30	NC
31	PER1+(1)	32	UART_RXD
33	GND	34	NC
35	PET1-(1)	36	NC
37	PET1+(1)	38	DEVSLP
39	GND	40	NC
41	PER0-/SATA-B+	42	NC
43	PER0+/SATA-B-	44	NC
45	GND_45	46	NC
47	PET0-/SATA-A-	48	NC
49	PET0+/SATA-A+	50	PERST#
51	GND_51	52	CLKREQ#
53	REFCLK_N	54	PEWAKE#
55	REFCLK_P	56	NC
57	GND	58	WP#
59	CONNECTOR_KEY	60	CONNECTOR_KEY
61	CONNECTOR_KEY	62	CONNECTOR_KEY
63	CONNECTOR_KEY	64	CONNECTOR_KEY
65	CONNECTOR_KEY	66	CONNECTOR_KEY
67	NC	68	SUSCLK
69	PEDET	70	3V3_70
71	GND_71	72	3V3_72
73	GND_73	74	3V3_74
75	GND_75		

(1) Only available on the bottom M.2 socket if that specific feature is ordered.

Table 31: M.2 Module Socket Signal Description

MNEMONIC	DIRECTIO	SIGNAL DEFINITION
3.3V	O	I
GND	-	Logic ground.
LED1# / DAS_DSS#	I	- PCI Express: LED_1# indicator as per PCI Express M.2 specification. - SATA: Device Activity Signal /Disable Staggered Spinup as per SATA 3.2. DAS is not connected to a LED (which is the main purpose of this signal) and DSS is not used since the devices are SSD and not hard drives (no spinup). Signal connected to dedicated CPLD
PEDET	I	PEDET (PCI Express Detect) as per PCI Express M.2 specification is driven low by SATA modules and high-Z by PCI Express modules (seen as a logic 1 due to on-board pull-up resistor). This signal is connected to a dedicated CPLD pin.
PERn+/- SATA-B+/-	I	- PCI Express: Receive differential pair as per PCI Express M.2 & PCI Express 3.0 specifications. - SATA: Receive differential pair as per SATA 3.2.
PERST#	O	- PCI Express: PCI Express PERST# as per PCI Express M.2 specification, handled by CPLD. - SATA: NC.
PETn+/- SATA-A+/-	O	- PCI Express: Transmit differential pair as per PCI Express M.2 & PCI Express 3.0 specifications. - SATA: Transmit differential pair as per SATA 3.2.
PEWAKE#	I/O	- PCI Express: Open drain WAKE# signal as per PCI Express M.2. - SATA: NC..
REFCLKP/N	O	- PCI Express: PCIe 100MHz clock as per PCI Express M.2. - SATA: NC..
SUSCLK	O	Suspend Clock for low power mode handling as per PCI Express M.2 specification (32.768 kHz, duty cycle between 30% and 70%, 200ppm). Connected to SoC SUSCLK_GPIO62.
CLKREQ#	I/O	- PCI Express: Open drain reference clock request signal as per PCI Express M.2. - SATA: NC.
WP#	I (open drain)	SSD write protect input. Expected SSD behavior when Write-Protect (WP) signal is used: When WP is low, any writes by the host will be aborted by the SSD (any write command not acknowledged by the SSD will be aborted). When WP# is high or if unused by the SSD module: no write protection.

When PCI Express and SATA functions coexist, the following convention applies PCI Express function / SATA function.

signal active when low

4.2.4. Layer2 socket for optional mezzanine - Pin Assignment

Contact Kontron support for availability status

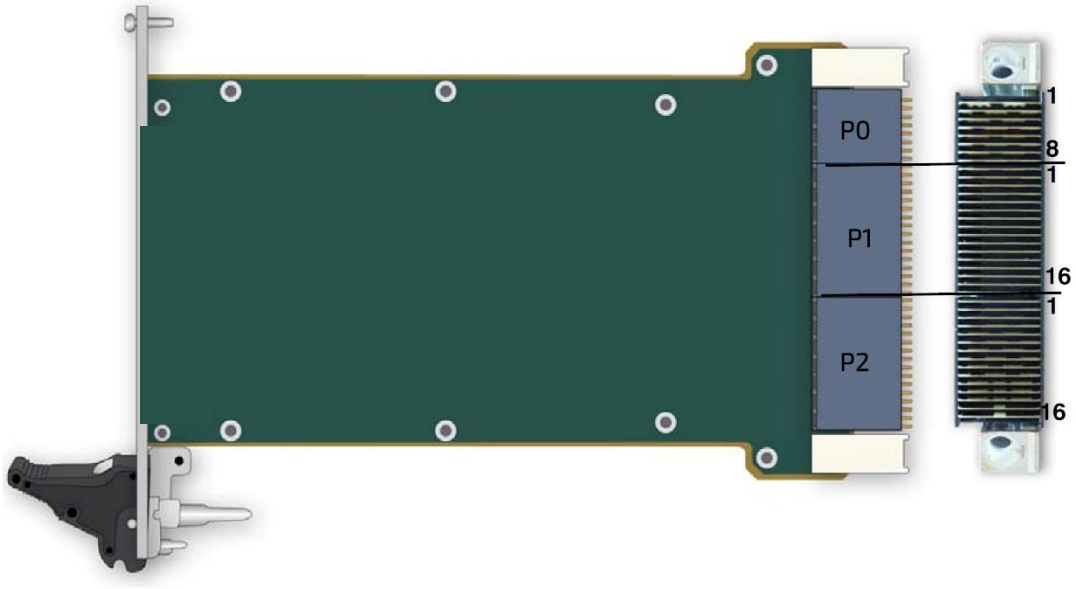
4.3. VPX Rear Connectors

VPX Bus Interface

The complete 3U VPX connectors configuration comprises three connectors named P0 to P2:

- P0: 8-wafer 7-row connector.
- P1 - P2: 16-wafer 7-row differential connectors.

Figure 29: VPX Connectors



4.3.1. VPX P0 Connector

Table 32: VPX Connector P0 Wafer Assignment

P0	G	F	E	D	C	B	A
1	VS1 (12V)	VS1 (12V)	VS1 (12V)	NC	NC (VS2)	NC (VS2)	NC (VS2)
2	VS1 (12V)	VS1 (12V)	VS1 (12V)	NC	NC (VS2)	NC (VS2)	NC (VS2)
3	NC (VS3)	NC (VS3)	NC (VS3)	NC	NC (VS3)	NC (VS3)	NC (VS3)
4	SMB1_CLK	SMB1_DAT	GND	-12V_AUX	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3V3_AUX	GND	SMB0_CLK	SMB0_DAT
6	GA3*	GA2*	GND	NC (+12V_AUX)	GND	GA1*	GA0*
7	TCK (to XMC slot only)	GND	TDO (from XMC slot only)	TDI (to XMC slot only)	GND	TMS (to XMC slot only)	TRST* (to XMC slot only)
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND

* signal active when low

REF_CLK-/+: 25MHz and 100MHz clock manufacturing options are available. Contact Kontron. Default is the 25MHz standard option.

The ordered product manufacturing options may alter the VPX P0 pin assignment. Contact Kontron.

Table 33: VPX Connector P0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
+12V	+12 Volts DC power (VS1 VPX supply). NC (+12V) pins are not connected (VS2 VPX supply)
-12V_AUX	-12 Volts auxiliary power. Only used to supply XMC if needed.
3V3_AUX	+3.3 Volts auxiliary power. Not required because it generate internally is 3V3_AUX power rail is not present on the backplane.
NVMRO	Non-Volatile Memory Read Only. When asserted (logical 1), prevents any non-volatile memory from being updated.
GAi	Geographical address pins
GAP	Geographical address parity
GND	Ground
IPMB A	I2C Bus 0
IPMB B	I2C Bus 1
REF_CLK+/-	The Reference Clock is a bussed differential pair. Output if the VX3060-S2 is plugged in the system controller slot, input otherwise. It enables the entire system to synchronize to a common time reference if desired. Counter/timer in the CPLD can use this clock
AUX_CLK+/-	1 PPS (one pulse per second) clock input. Can be programmed as an output on system controller slot. Can be used to phase the CPLD timer/counter clocked by REF_CLK+/-.
SYSRESET*	System Reset. Input and open collector output.
NC	“Not connected” factory option

4.3.2. VPX P1 Connector

Table 34: VPX Connector P1 Wafer Assignment

P1	G	F	E	D	C	B	A
1	Gdiscrete 1	GND	DP PCIe TX0-	DP PCIe TX0+	GND	DP PCIe RX0-	DP PCIe RX0+
2	GND	**[DP PCIe TX1-]**	**[DP PCIe TX1+]**	GND	**[DP PCIe RX1-]**	**[DP PCIe RX1+]**	GND
3	VBAT	GND	**[DP PCIe TX2-]**	**[DP PCIe TX2+]**	GND	**[DP PCIe RX2-]**	**[DP PCIe RX2+]**
4	GND	**[DP PCIe TX3-]**	**[DP PCIe TX3+]**	GND	**[DP PCIe RX3-]**	**[DP PCIe RX3+]**	GND
5	SYS_CON*	GND	EP PCIe TX0-	EP PCIe TX0+	GND	EP PCIe RX0-	EP PCIe RX0+
6	GND	EP PCIe TX1-	EP PCIe TX1+	GND	EP PCIe RX1-	EP PCIe RX1+	GND
7	USB1 PWR	GND	EP PCIe TX2-	EP PCIe TX2+	GND	EP PCIe RX2-	EP PCIe RX2+
8	GND	EP PCIe TX3-	EP PCIe TX3+	GND	EP PCIe RX3-	EP PCIe RX3+]	GND
9	COM1 TXD	GND	**[XMCIO DP_J16-A5]**	**[XMCIO DP_J16-B5]**	GND	**[XMCIO DP_J16-D5]**	**[XMCIO DP_J16-E5]**
10	GND	**[XMCIO DP_J16-A7]**	**[XMCIO DP_J16-B7]**	GND	**[XMCIO DP_DJ16-D7]**	**[XMCIO DP_J16-E7]**	GND
11	COM1 RXD	GND	**[XMCIO DP_J16-A9]**	**[XMCIO DP_J16-B9]**	GND	**[XMCIO DP_J16-D9]**	**[XMCIO DP_J16-E9]**
12	GND	**[XMCIO DP_J16-A15]**	**[XMCIO DP_J16-B15]**	GND	**[XMCIO DP_J16-D15]**	**[XMCIO DP_J16-E15]**	GND
13	GPIO1	GND	**[XMCIO DP_J16-A17]**	**[XMCIO DP_J16-B17]**	GND	**[XMCIO DP_J16-D17]**	**[XMCIO DP_J16-E17]**
14	GND	**[XMCIO DP_J16-A19]**	**[XMCIO DP_J16-B19]**	GND	**[XMCIO DP_J16-D19]**	**[XMCIO DP_J16-E19]**	GND
15	Msk RST/GPIO5	GND	**[ETH1 Tx-]**	**[ETH1 Tx+]**	GND	**[ETH1 Rx-]**	**[ETH1 Rx+]**
16	GND	ETH0 Tx-	ETH0 Tx+	GND	ETH0 Rx-	ETH0 Rx+	GND
CASE	GND						

* signal active when low

The ordered product manufacturing options may alter the VPX P1 pin assignment. Contact Kontron.
Important note: [….] means manufacturing options, signal present if the related option is ordered

Table 35: VPX Connector P1 Signal Definition

MNEMONIC	SIGNAL DEFINITION
DP PCIe DP	Data Plane (DP) x4 PCI Express Link. gen1, gen2 or gen3
EP PCIe DP	Expansion Plane (EP) x4 PCI Express Link. gen1, gen2 or gen3
USB PWR	USB Power
ETH0/ETH1	Dual 10GBASE-KR or 1000BASE-KX Ethernet auto negotiation)
GDISCRETE1	Open VPX GDISCRETE1 signal
GPIO1*	General Purpose I/O 1 (handled by the CPLD)
Maskable Reset* or GPIO5	Reset input or Optional general purpose I/O (handled by CPLD) (may be left unconnected if not used).
GND	Ground
SYS_CON	System Controller Slot Indication
VBAT	Battery Voltage Input, 3V. Optional alternated source for RTC backup voltage.
COM1	Maintenance port : serial Lines EIA-232 or 3V3 signal leveling COM1 shall support LVCMOS and TIA-232 modes
XMCIO DPxx	Differential pairs XMC I/O as per VITA 46.9 P1w9-X12d

4.3.3. VPX P2 Connector

Table 36: VPX Connector P2 Wafer Assignment

P2	G	F	E	D	C	B	A
1	COM2 TXD- (COM2 TXD)	GND	VID L1- (1)	VID L1+ (1)	GND	VID L0- (1)	VID L0+ (1)
2	GND	VID L3- (1)	VID L3+ (1)	GND	VID L2- (1)	VID L2+ (1)	GND
3	COM2 TXD+ (COM3 TXD)	GND	VID PWR	VID HPD (1)	GND	VID AUX- (1)	VID AUX+ (1)
4	GND	USB3 D0-	USB3 D0+	GND	USB2 D1-	USB2 D1+	GND
5	COM2 RXD- (COM2 RXD)	GND	USB1 (USBSS TX-)	USB1 (USBSS TX+)	GND	USB1 (USBSS RX-)	USB1 (USBSS RX+)
6	GND	[STO SATA/PCIe TX-]	[STO SATA/PCIe TX+]	GND	[STO SATA/PCIe RX-]	[STO SATA/PCIe RX+]	GND
7	COM2 RXD+ (COM3 RXD)	GND	ETH2 DB-	ETH2 DB+	GND	ETH2 DA-	ETH2 DA+
8	GND	ETH2 DD-	ETH2 DD+	GND	ETH2 DC-	ETH2 DC+	GND
9	USB PWR	GND	[XMCIO SE_J16-C12]	[XMCIO SE_J16-C13]	GND	[XMCIO SE_J16-F12]	[XMCIO SE_J16-F13]
10	GND	[XMCIO SE_J16-C14]	[XMCIO SE_J16-C15]	GND	[XMCIO SE_J16-F14]	[XMCIO SE_J16-F15]	GND
11	GPIO2	GND	[XMCIO SE_J16-C16]	[XMCIO SE_J16-C17]	GND	[XMCIO SE_J16-F16]	[XMCIO SE_J16-F17]
12	GND	[XMCIO SE_J16-C18]	[XMCIO SE_J16-C19]	GND	[XMCIO SE_J16-F18]	[XMCIO SE_J16-F19]	GND
13	GPIO3	GND	[XMCIO DP_J16-A1]	[XMCIO DP_J16-B1]	GND	[XMCIO DP_J16-D1]	[XMCIO DP_J16-E1]
14	GND	[XMCIO DP_J16-A3]	[XMCIO DP_J16-B3]	GND	[XMCIO DP_J16-D3]	[XMCIO DP_J16-E3]	GND
15	GPIO4	GND	[XMCIO DP_J16-A11]	[XMCIO DP_J16-B11]	GND	[XMCIO DP_J16-D11]	[XMCIO DP_J16-E11]
16	GND	[XMCIO DP_J16-A13]	[XMCIO DP_J16-B13]	GND	[XMCIO DP_J16-D13]	[XMCIO DP_J16-E13]	GND
CASE	GND						

* signal active when low

Note (1):
If ECL = ECL-3xxxxyy : the rear VPX P2 Video link is connected to the Tiger Lake TCP1 interface, and the front panel Video link is connected to the Tiger Lake DDIB interface

If ECL <ECL-3xxxxyy: the rear VPX P2 Video link is connected to the Tiger Lake DDIB interface, and the front panel Video link is connected to the Tiger Lake TCP1 interface

The ordered product manufacturing options may alter the VPX P1 pin assignment. Contact Kontron.
Important note: [….] means manufacturing options, signal present if the related option is ordered

Table 37: VPX Connector P2 Signal Definition

MNEMONIC	SIGNAL DEFINITION
COM2/COM3	Serial Lines, TIA-232/TIA-422/485. COM2 lines can be configured as a single COM2 TIA-422/485 serial port or split into two TIA-232 ports (COM2 and COM3).
ETH	Ethernet 1000BASE-T
VID	Display Port DP++ video Port
GND	Ground
GPIOx*	General Purpose I/O x (handled by the CPLD). GPIO3-4 signals are multiplexed with Ethernet LAN1 10G I2C bus signals for rear SFP+ operation. GPIO is default mode.
STO SATA/PCIe	SATA/PCIe port for an external storage device.
USB PWR	USB Power
USB2/3	USB2.0 ports
USB1	USB3.x port
XMCIO SExx	Single ended XMC I/O according to VITA 46.9 X16s
XMCIO DPxx	Differential pairs XMC I/O according to VITA 46.9 X8d

4.4. LEDs

4.4.1. LED indicators location

There are five bicolor LEDs (Red/Green) on the front panel of the VX3060-S2.

(view without 2LM cover option)

4.4.2. LEDs Activity – Normal Mode

When LED1 is red, the meaning of the other LEDs is changed. See Section "Power Sequencer"/"Error codes".
If “debug mode” is active, please refer to Section "Power Sequencer/Power states"
For "user mode" on LED3,LED4 and LED5, see Section "CPLD Registers"

During normal operation (not configured in "user mode", no fatal error, not in “debug mode”), their state is as follows:

Table 38: LEDs Description – Normal Mode

LED1		
OFF		Board fully off
GREEN		Board running. Blinking slow (@1Hz) when off/sleeping and no reset source is active.
ORANGE		Board reset asserted. Blinking slow (@1Hz) when off/sleeping and a reset source is active.
RED		Fatal error. See Section "Power Sequencer"/"Error codes"

LED2		
OFF		Board off or sleeping
GREEN		Normal operation. Blinking on CPLD activity (LPC or I2C0/1 slave)
ORANGE		Same than green, but when FACTORY_MODE switch is ON
RED		Watchdog timeout

LED3		
OFF		
GREEN		M2S1/M2S2 activity (off when no activity)
ORANGE		-
RED		Temperature alert

LED4		
OFF		
GREEN		Non-SOSA2 : at least one i225/i226 interface with link up and at max speed, blinking on activity SOSA2 : i225/i226 interface with link up at max speed, blinking on activity
ORANGE		Non-SOSA2 : at least one i225/i226 interface with link up but none at max speed, blinking on activity SOSA2 : i225/i226 interface with link up but not at max speed, blinking on activity
RED		PBIT error

LED5		
OFF		
GREEN		non-SOSA2 : i210S interface with link up at max speed, blinking on activity SOSA2 : at least one E810 interface with link up and at max speed, blinking on activity
ORANGE		non-SOSA2 : i210S interface with link up but not at max speed, blinking on activity SOSA2 : at least one E810 interface with link up but none at max speed, blinking on activity
RED		-

4.4.3. LEDs - Power States

When in "debug mode", the LEDs no more have their operational meaning, but **LED1 is blinking green fast (@2Hz),** and LED2, LED3, LED4, LED5 are displaying the current power state as follows :

Table 24: LEDs Description – Debug Mode / Error Codes

LEDs In "DEBUG MODE"					
Power state #	**Name**	**LED2**	**LED3**	**LED4**	**LED5**
0	POR_ST	OFF	OFF	OFF	OFF
1	V3V3PRIM_ST	GREEN	OFF	OFF	OFF
2	SLPSUS_ST	OFF	GREEN	OFF	OFF
3	V1V8PRIM_ST	GREEN	GREEN	OFF	OFF
4	VCCINAUX_ST	OFF	OFF	GREEN	OFF
5	RSMRST_ST	GREEN	OFF	GREEN	OFF
6	WAITBPPWR_ST	OFF	GREEN	GREEN	OFF
7	PWRBTN_ST	GREEN	GREEN	GREEN	OFF
8	WAITS4_ST	OFF	OFF	OFF	GREEN
9	WAITS3_ST	GREEN	OFF	OFF	GREEN
10	V2V5DDR_ST	OFF	GREEN	OFF	GREEN
11	V1V2DDR_ST	GREEN	GREEN	OFF	GREEN
12	V3V3_ST	OFF	OFF	GREEN	GREEN
13	E810_1_ST	GREEN	OFF	GREEN	GREEN
14	E810_2_ST	OFF	GREEN	GREEN	GREEN
15	VCCIN_ST	GREEN	GREEN	GREEN	GREEN
16	FORCEOFF_ST	OFF	OFF	OFF	RED
23	RUNNING_ST	GREEN	GREEN	GREEN	RED

4.4.4. LEDs – Error Codes

The current error code can be read back from I2C20 in the I2C_ERROR_STATUS register (regnum = 2).
Values from 12 to 17 are the generic ones expected by a CMB board.

The implemented error codes are as follows :

Table 24: LEDs Description – Error codes

ERROR CODES ON LEDs						
Error code #	**Name**	**LED1**	**LED2**	**LED3**	**LED4**	**LED5**
0	ERR_NO_ERROR	-	-	-	-	-
1	ERR_3V3PRIM	RED	RED	OFF	OFF	OFF
2	ERR_SLPSUS	RED	OFF	RED	OFF	OFF
3	ERR_1V8PRIM	RED	RED	RED	OFF	OFF
4	ERR_VCCINAUX	RED	OFF	OFF	RED	OFF
5	ERR_2V5DDR	RED	RED	OFF	RED	OFF
6	ERR_1V2DDR	RED	OFF	RED	RED	OFF
7	ERR_VCCSTSTG	RED	RED	RED	RED	OFF
8	ERR_3V3	RED	OFF	OFF	OFF	RED
9	ERR_5V0	RED	RED	OFF	OFF	RED
10	ERR_E810VDD	RED	OFF	RED	OFF	RED
11	ERR_E810AVDD	RED	RED	RED	OFF	RED
12	ERR_PECI_CRIT	RED	OFF	OFF	RED	RED
13	ERR_THERM_PROT	RED	RED	OFF	RED	RED
14	ERR_THERMTRIP	RED	OFF	RED	RED	RED
15	ERR_CATERR	RED	RED	RED	RED	RED
16	ERR_BP_UV_PWRGD	RED	OFF	OFF	OFF	GREEN
17	ERR_BP_OV_PWRGD	RED	RED	OFF	OFF	GREEN
18	ERR_VCCINRDY	RED	OFF	RED	OFF	GREEN

5. Power and Thermal Specifications

5.1. Power considerations

The considerations presented in the ensuing sections must be taken into account by system integrators when specifying the VX3060-S2 system environment.

5.1.1. Backplane

Backplanes to be used with the VX3060-S2 must be adequately specified and comply with VITA 65.0. The backplane must provide optimal power distribution for the VPX VS1 and 3V3 AUX power inputs.
Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided

5.1.2. Power Supplies

Power supplies for the VX3060-S2must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires.
An industrial power supply unit should be able to provide at least twice as much power as the entire system requires.
An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.
Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for die resistance variations.

› Tolerance

The following table provides information regarding the required characteristics for each board input voltage.

Table 39: VPX Input Voltage Tolerance

POWER RAIL	NOMINAL VALUE	TOLERANCE*	MAX RIPPLE (p-p)	REMARKS
+12V VPX VS1	+12VDC	+/-5%	50mV over a range of 0-20MHz	Main voltage
+3.3V VPX VS2	*+3.3VDC*	*3.25V min 3.45V max*	*50mV over a range of 0-20MHz*	*Not used*
+5V VPX VS3	*+5VDC*	*+5%/-2.5%*	*50mV over a range of 0-20MHz*	*Not used*
VPX 3.3V AUX	+3.3VDC	+/-5%	50mV over a range of 0-20MHz	Optional
GND	Ground, not directly connected to potential earth (PE)			

(*)Tolerance values include ripple.

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

› Rise Time

As per VITA 46.0, section 3.2.2, the system power supply ramp-up phase should be between 20 and 150 msec. However, Kontron recommend a ramp-up phase below 25ms.

› Regulation

The system power supplies should be monotonic as they ramp to their specified final values during power up conditions as per VITA 46.0, section 3.2.2.

The system power supplies shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it went below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

5.1.3. Power Supplies Monitoring

The VX3060-S2 embeds three voltage sensors monitoring power rails and internal power supply voltage.

- NCT7802Y by Nuvoton
- LTC2913 by Linear Technology
- INA220 by Texas Instruments

The voltage sensor NCT7802Y is programmed by the IPMC to monitor VS1 and internal voltages, it asserts an alert signal whenever either voltages get out of its specified range. This alert is routed to a maskable interrupt in the cPLD. For detailed specification of NCT7802Y, refer to section 5.3.

The voltage sensor LTC2913 monitors VS1 voltage with a 10 % tolerance. The thresholds are set by hardware on the board. Undervoltage and overvoltage conditions on VS1 are reported to the cPLD which in turn shuts down all VX3060-S2 internal power supplies. There is no mechanism for masking these alerts.

The current sensor INA220 monitors VS1 input current.

5.1.4. Output Power Supplies Protections

On the VX3060-S2, all the output power supplies provided on connectors are protected by fuse or current-limiting devices as described in the following table.

Table 40: Output Powers Supplies Protection

Port	Function	Location	Voltage	Protection	Rated Current*	Trip current	Characteristics
M2. Slot	M2. Slot power supply	On-Board	+3.3V	Non resettable fuse	4.5 A	-	-
XMC slot	VPWR XMC slot power supply	On-Board	+12V	Non resettable fuse	4.5 A	-	-
XMC slot	3.3V power supply	On-Board	+3.3V	Non resettable fuse	Up to 4 A (1)	-	-
XMC slot	-12V power supply	On-Board	-12V_AUX	Non resettable fuse	1.5 A	-	-
VPX P2 rear DP power pins	P2 DP power supply	On-Board	+3.3V	Non resettable fuse	1.5 A	-	-
VPX P2 rear USB power pins	P2 USB power supply	On-Board	+5V	USB power distribution switches	900 mA	-	-

* Worst Case Hold Rated Current* for maximum operation temperature

Note (1): 3 Amps rated fuse protection on the XMC 3V3 Rail if VX3060-S2 in ECL < ECL-3xxxxyy, and 4 Amps if in ECL=ECL-3xxxxyy

5.2. VPX Input Power Rails Specification

The VX3060-S2 board has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

› Absolute Maximum Input Voltage
The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the VX3060-S2 should be carefully tested to ensure compliance with these ratings.

Table 41: Absolute maximum input voltage

POWER RAIL	ABSOLUTE MAXIMUM INPUT VOLTAGE
VPX 3.3V AUX	3.5V
+12V VPX VS1	13V

⚠WARNING

The maximum permitted voltage indicated in the table above must not be exceeded.
Failure to comply with these figures may result in damage to your board.

› Recommended Operating Input voltage
The following table specifies the recommended operating conditions of the different input power voltages within the board as per VITA46.0, section 3.2.2. The VX3060-S2 is not guaranteed to function if the board is not operating within the prescribed limits.

Table 42: Recommended Operating Input Voltage

POWER RAIL	RECOMMENDED OPERATING INPUT VOLTAGE
VPX 3.3V AUX	3.3V +/-5%
+12V VPX VS1	+12V +/-5% inclusive of ripple

VPX 3.3V AUX shall be used on VX3060-S2 boards as per VITA 46.0 and VITA 65.0.
However, this power rail input could be optional on VX3060-S2 boards because it is internally generated from the +12V VS1 power input when it is not present on the backplane.
If both, VBAT and 3.3V AUX are not present on the backplane, the date and time retention is not ensured.

› Input Power Supply Protection
The input power rails are protected on the VX3060-S2 by fuse as described in the following table.

To prevent safety hazards, the chassis power supply must not exceed the Voltage Rating and Interrupt Rating of the fuse.

Table 43: Input Powers Supplies Protection

POWER RAIL	VPX VS1	VPX 3.3 V AUX	VPX -12V AUX
LOCATION	Near P0 power input pins	Near P0 power input pins	Near P0 power input pins
VOLTAGE	+12 V	+3.3 V	-12 V
PROTECTION	Non resettable fuse	Non resettable fuse	Non resettable fuse
RATED CURRENT	12 A	1.5 A	1.5 A
VOLTAGE RATING	32VDC	32VDC	32VDC
MANUFACTURER / PN	LITTELFUSE / 0501012.WR	LITTELFUSE / 043501.5KR	LITTELFUSE / 043501.5KR

5.3. Power Consumption Specification

5.3.1. Thermal Power

The following data show total board consumption for different processor configuration and Thermal Design Power. These data help for thermal power dissipation analysis.

Table 44: Thermal Power: board power based on current measurements

Order code	Power Mode	Measured CPU package power	Average VPX VS1 Thermal Power (W)	Max VPX VS1 Thermal Power 100ms sampling (W)	Test Condition
VX3060-S2-RC34G-21EN00V10	100 % all cores	28W *15W (1)*	48 (*) *34 (1)*	51 (*) *37 (1)*	VPX VS1= 12V, SoC TDP @28W Turbo Off 11th Gen Intel(R) Core(TM) i7-1185GRE @ 2.80GHz Dual 10GbE links active No USB, M.2 and XMC devices present Intel TAT and glmark2 Gfx benchmarks
	100 % all cores	28W	52 (*)	67 (*)	VPX VS1= 12V, SoC TDP @28W Turbo On 11th Gen Intel(R) Core(TM) i7-1185GRE @ 2.80GHz Dual 10GbE links active No USB, M.2 and XMC devices present Intel TAT and glmark2 Gfx benchmarks
	Linux Idle	-	20 (*)	-	VPX VS1= 12V 11th Gen Intel(R) Core(TM) i7-1185GRE @ 2.80GHz No USB, M.2 and XMC devices present

(*) One USB2.x device @500mA using board power source will add 2.7W. One USB2.x device @900mA using board power source will add 4.8W.
(1) Not measured. Based on estimates.

	Voltage Rail Name	Max Current	Max Continuous Power Consumption (W)	Test condition
Board without VPX VS1 power supply Board in stand-by mode	VPX +3V3_AUX	< 500mA	< 1.7	VPX +3V3_AUX power rail is present and VPX VS1 power rail not present. VPX +3V3_AUX power rail must support peak current condition at power-on.

5.3.2. Maximum Peak Current

The following data provide maximum continuous and worst case current values on VPX VS1 (12V) power supply. These maximum includes margin to guarantee worst-case part behavior.

Table 45: Maximum VS1 Current

Order code	Max VPX VS1 current 100ms sampling	Measured VPX VS1 Inrush current	Test Condition
VX3060-S2-RC34G-21EN00V10	6.5 A (*)	15A (< 1ms)	11th Gen Intel(R) Core(TM) i7-1185GRE @ 2.80GHz No USB, M.2 and XMC devices present

(*) Calculated value based on measurements and for CPU @ 1.25*TDP

Maximum and peak current draw are intended as without enabled Turbo mode and without any XMC mezzanine card or M.2 device plugged on board.

5.4. Board - Thermal Monitoring

To ensure long-term reliability of the VX3060-S2, onboard components must not operate beyond their specified maximum temperature. The most critical component on the VX3060-S2 is the processor. Operating the VX3060-S2 above the maximum operating limits will result in permanent damage to the board.

The VX3060-S2 includes a temperature sensor (NCT7802Y by Nuvoton) managed by the IPMC through I2C.

Depending on the board ECL, an additional LM73CIMK managed through the cPLD can be available.

Figure 30: Temperature Sensor Location

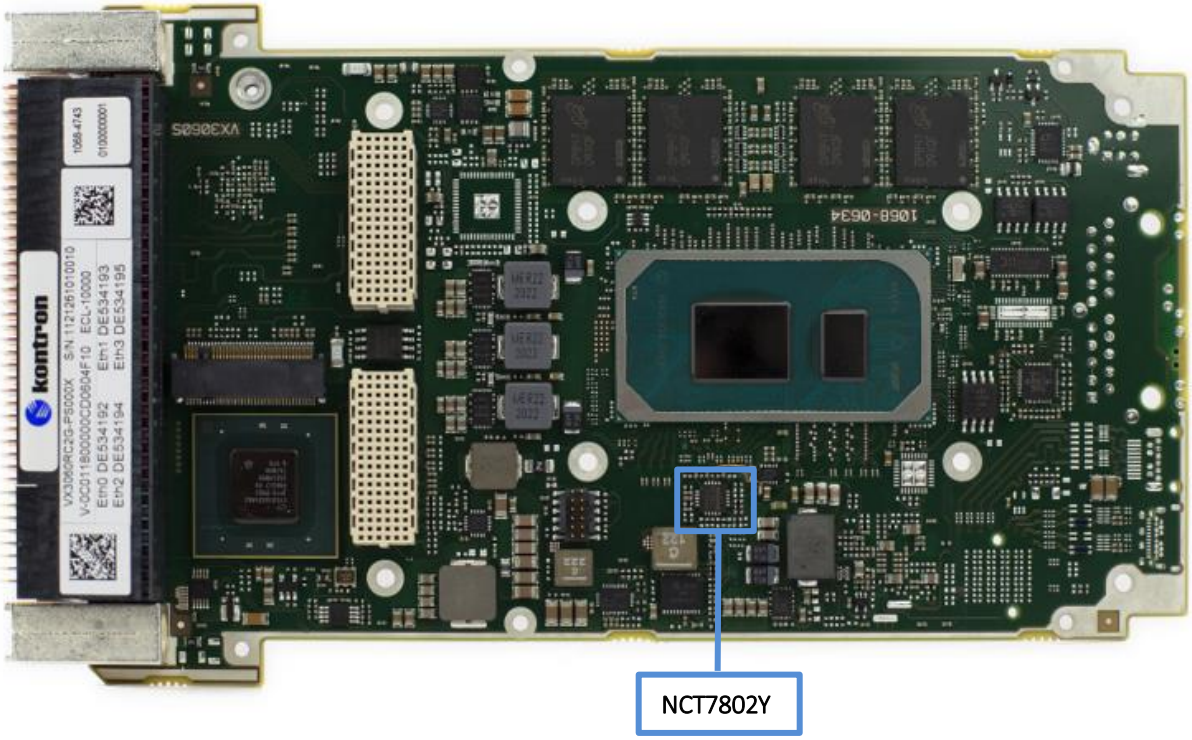
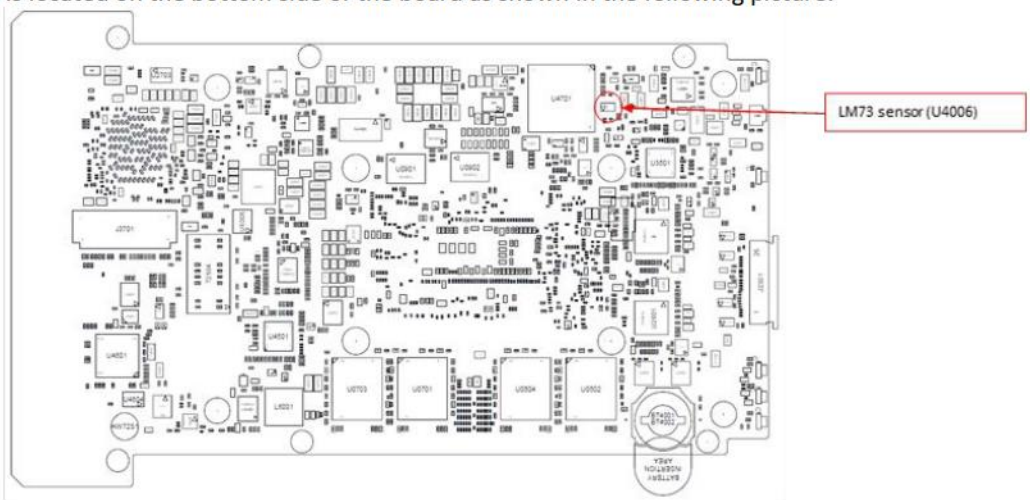


Figure 31: LM73 Temperature Sensor Location – only applicable to variants in ECL = ECL-3xxxxyy

LM73CIMK is located on the bottom side of the board as shown in the following picture:



In addition to monitoring several internal power supplies, the NCT7802Y supports one on-die temperature sensor and can also get the processor temperature directly via the Intel® PECI interface. The NCT7802Y temperature and voltages monitoring data may be viewed with the Linux "ipmitool" command.

The NCT7802Y has 2 alarm outputs connected to the CPLD:

- ALERT#: logged in CPLD to generate a maskable interrupt.
  The low threshold may also be used as the lower threshold for high temperature hysteresis.
- T_CRIT#: logged in CPLD reg @0x74, leads to fatal error with all internal PSUs power supplies being switched off and the error status is being displayed on the front panel LEDs.

ALERT and T_CRIT thresholds may be modified by the Shelf Manager using the IPMI command or locally by using Linux “ipmitool” command. To know default value and further details about these thresholds, refer to VITA 46.11 Firmware Release Note document (see section “Related Publications”)

› NCT7802Y Key specifications:

- Voltage monitoring accuracy +-10 mV
- Temperature Sensor Accuracy
  - On-chip Temperature Sensor Accuracy (25~70 °C) +- 2 °C typ.
  - On-chip Temperature Sensor Resolution 1 °C
- Operating Temperature Range -40 °C ~ 85 °C

› LM73CIMK Key specifications (only applicable to variants with ECL = ECL-3xxxxyy)

Additional LM73CIMK is available for temperature monitoring. Link to the Online Datasheet : https://www.ti.com/
This sensor is supported by the Board Support Packages (BSP) provided by Kontron as a standard I2C local sensor.
The CPLD also keeps a copy of the temperature from this sensors in the cPLD register @0x7B offering a direct temperature reading (from CPU or backplane I2C bus) as follows:

Figure 32: LM73 – cPLD Read access (only applicable to variants in ECL= ECL-3xxxxyy)

cPLD Register I2C_TEMP @ 0x7B Can also be accessed from I2C slave interface with regnum 9				
BIT(s)	**Name**	**Description**	**Reset**	**Access**
7-0	Temp	This is the temperature read by the CPLD every second from the LM73 I2C sensor. The temperature is in Celsius on a 8 bit signed value (-127°C to +127°C). An invalid or undefined value is reported with the reserved value 0x80 (-128°C). If the sensor can not be read for more than 8s, the value resets to 0x80. On IPMI boards, this register has always value 0x80	0x80	RO

5.5. SoC - Thermal Monitoring

To allow optimal operation and long-term reliability of the VX3060, the processor must remain within the maximum junction temperature specifications. The maximum operating temperature for the processor die (TJMAX) is 100°C. The TJMAX temperature is the temperature not to exceed, to avoid entering the throttling mode with reduced performance.

The THERMTRIP# temperature threshold is the temperature not to exceed to protect processor from catastrophic overheating. The processor will stop all executions when THERMTRIP# is reached. This threshold is 130°C.

The processor uses the Adaptive Thermal Monitor feature to protect the processor from overheating and includes the following on-die temperature sensors:

- One Digital Thermal Sensor (DTS) for monitoring each processor core
- Catastrophic Cooling Failure Sensor (THERMTRIP#)

These sensors are integrated in the processor and work without any interoperability of the uEFI BIOS or the software application. Thermal Control Circuit allows the processor to maintain a safe operating temperature without the need for special software drivers or interrupt handling routines.

› Digital Thermal Sensor (DTS)

The processor includes on-die Digital Thermal Sensors (DTS), one per processor cores. They can be read via an internal register of the processor.

The temperature returned by the Digital Thermal Sensor will always be at or below the maximum operating junction temperature. Via the Digital Thermal Sensors, the uEFI BIOS or the application software can measure the processor die temperature.

The Max DTS temperature is 100°C.

› Catastrophic Cooling Failure Sensor

The Catastrophic Cooling Failure Sensor protects the processor from catastrophic overheating.
The Catastrophic Cooling Failure Sensor threshold is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds this threshold. Once activated, the event remains latched until the VX3060-S2 undergoes a power-on restart (all power off and then on again).
This function cannot be enabled or disabled in the uEFI BIOS. It is always enabled to ensure that the processor is protected in any event.

5.6. Thermal Performance

› Board Level Thermal Performance
The CPU core maximum DTS temperature is the maximum temperature allowed before entering into throttling mode. The maximum operating temperature for the processor die is 100°C.
This core temperature is accessible through the Linux sensors driver. Refer to the Kontron VME/VPX Fedora Remix Release Notes for information about the "sensors" command, RC class specific features, and power management.

The user can modify several parameters to optimize board thermal performance:

- Processor load: Kontron advises to keep some margin for real time behavior and stay within 80% of processor load.
- Turbo boost mode: for a better control of thermal performance, it is advised to disable this mode for real-time applications.

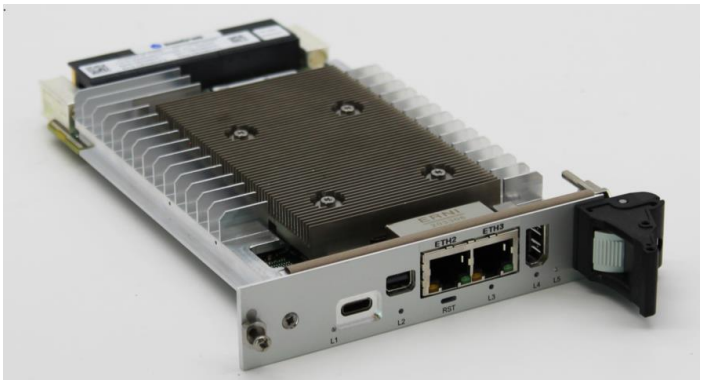
The processor junction temperature shall never exceed 100°C at any time.

The maximum processor temperature range during operation is 90°C, starting from boot time temperature. This range can be extended to 110°C with PCIe Gen3 limitations. The behavior is described in Intel documents #734746 and #684987 as DTR = Dynamic Temperature Range. For more information, contact Kontron Support.

5.6.1. Air cooled - Thermal Performance

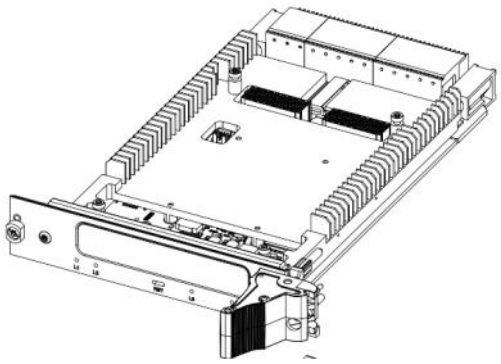
Figures below illustrates the operational limits of the VX3060-S2 air cooled variants.
The junction temperature of processor is kept below the maximum allowed to avoid the processors entering the throttling mode.
The measurements were made based on a 5HP slot (1 inch height) and using Power Thermal Utility (PTU) software from Intel to adjust processor workload.

Table 46: VX3060-S2 / Air cooled Typical Functional Points



Air cooled Order Codes VX3060-S2-SA4x-Yxxx0xx1x VX3060-S2-WA4x-Yxxx0xx1x VX3060-S2-RA4x-Yxxx0xx1x **With Y= 0 or 3**	SoC TDP Set to 12W (1)			SoC TDP Set to 15W (1)			SoC TDP Set to 28W (1)			SoC TDP Set to 28W (1)			Test conditions
CPU Core Frequency	1200 MHz			1800 MHz			2800 MHz			2800 MHz			**No XMC slot option** Standard SA Kontron test bench., running Intel TAT with cpu workload@80% on the four processor cores. Processor turbo Off. No CPU throttling Max Processor junction Temperature < 100°C
CPU workload Typical Processor dissipation	80 % **10 W**			80 % **13 W**			80 % **23 W**			100 % **28 W**			
Max inlet air temperature (°C)	**55**	**65**	**70**	**55**	**65**	**70**	**55**	**65**	**70**	**55**	**65**	**70**	
Min inlet air flow (CFM) (2)	**8**	**8**	**10**	**8**	**10**	**12**	**13**	**16**	**19**	**14**	**18**	**22**	

The processor junction temperature shall never exceed 100°C at any time.
Contact Kontron support for additional thermal design data



Air cooled Order Codes VX3060-S2-SA4x-Yxxx0xx1x VX3060-S2-WA4x-Yxxx0xx1x VX3060-S2-RA4x-Yxxx0xx1x **With Y= 1 or 2**	SoC TDP Set to 12W [1]	SoC TDP Set to 15W [1]	SoC TDP Set to 28W [1]	Test conditions
CPU Core Frequency	1200 MHz	1800 MHz	2800 MHz	**XMC slot option available and no XMC module equipped on the XMC slot.** Standard SA Kontron test bench., running Intel TAT with cpu workload@80% on the four processor cores. Processor turbo Off. No CPU throttling Max Processor junction Temperature < 100°C
CPU workload Typical Processor dissipation	100 % **12 W**	100 % **15 W**	**17 W**	
Max inlet air temperature (°C)	**55**	**55**	**55**	
Min inlet air flow (CFM) [2]	**10**	**12**	**40**	

Note [1]: TDP set through BIOS settings Refer to the AMI-BIOS User Reference Manual (D258115)
Note [2]: Inlet processor junction temperature shall never exceed 100°C at any time.

The processor junction temperature shall never exceed 100°C at any time.
Contact Kontron support for additional thermal design data

5.6.2. Conduction cooled - Thermal Performance

› Card Edge Temperature Measurement
The card edge temperature is measured as follows: the middle left point in the wedgelock channel on the heat frame for the RC3 variants, and Front left for the RC4 variants (refer to the red arrow). The wedgelock channel is the channel between the edge of the heat frame and the cold wall of the rack. Refer to probe locations in the following views.

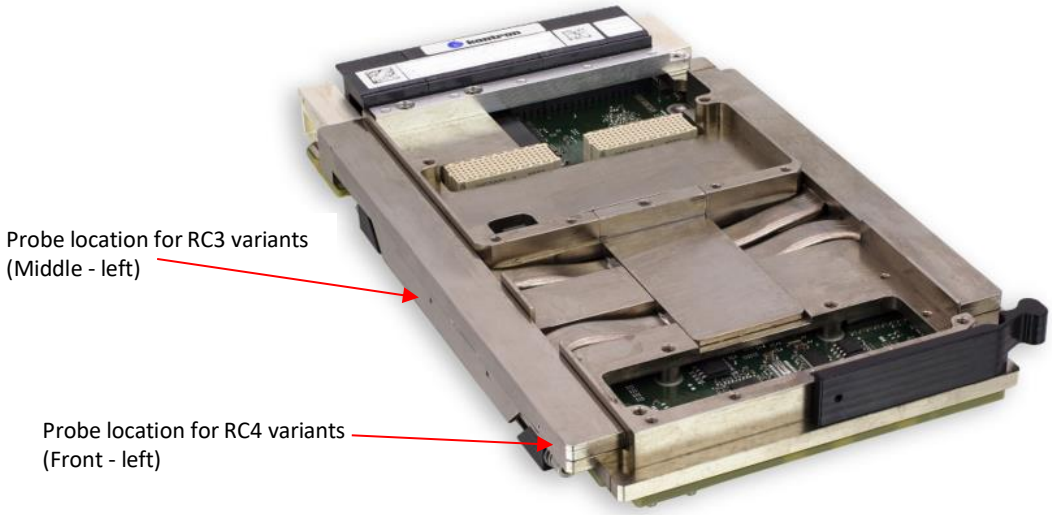


Table 47: VX3060-S2 / Conduction cooled Typical Functional Points

Order Codes	SoC TDP @12W (1)	SoC TDP @15W (1)	SoC TDP @28W (1)	SoC TDP @28W (1)	Test conditions
CPU Core Frequency	1200 MHz	1800 MHz	2800 MHz	2800 MHz	No XMC module equipped. No M.2 module equipped. Standard RC Kontron test bench., running Intel TAT with cpu workload@80% on the four processor cores. Maximum temperature measured at card edge. Processor turbo Off. No CPU throttling Max Processor junction Temperature : 100°C
CPU workload Typical Processor dissipation	100% **12 W**	100% **15 W**	80% **23 W (2)**	100% **28 W**	
VX3060-S2-RC34x-xxxx0xx1x **Max card edge temperature**	**70 °C**	**70 °C**	**63 °C**	**47 °C**	
VX3060-S2-RC44x-xxxx0xx1x **Max card edge temperature**	**85 °C**	**85 °C**	**83 °C**	**80 °C**	

Note (1): TDP set through BIOS settings Refer to the AMI-BIOS User Reference Manual (D258115)
Note (2): Typical processor dissipation measured on a few i7-1185GRE parts with TAT tool. Non-contractual data and for information only.

The processor junction temperature shall never exceed 100°C at any time.
Contact Kontron support for additional thermal design data.
According to ANSI/VITA 47 standard, the plug-in unit edge surface temperature is measured on the plug-in unit.
The maximum processor temperature range during operation is 90°C, starting from boot time temperature. This range can be extended to 110°C with PCIe Gen3 limitations. The behavior is described in Intel documents #734746 and #684987 as DTR = Dynamic Temperature Range. For more information, contact Kontron Support

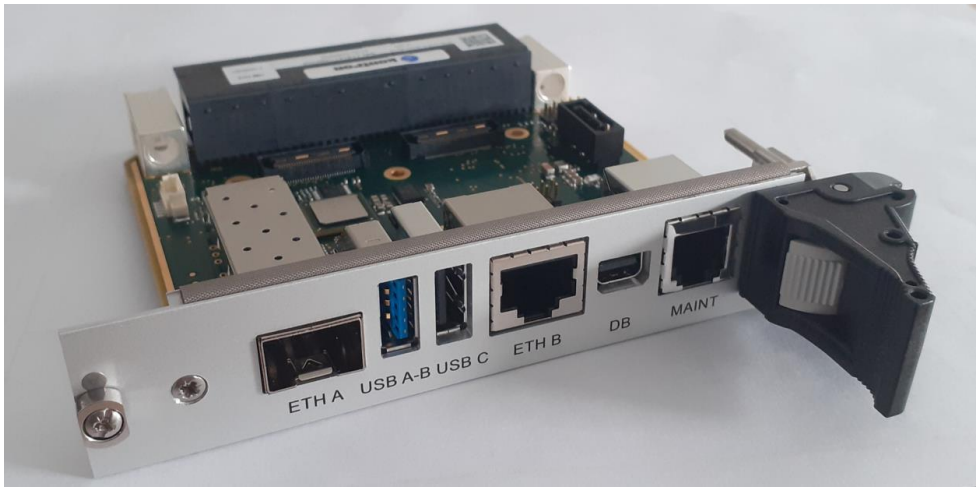
6. RTM compatible with the VX3060-S2 Compute Intensive profile

6.1. Introduction

6.1.1. Overview

The Kontron PB-VX3-40G-602 is a 3U VPX Rear Transition Module compliant with the definition of the Rear Transition Module on VPX Standard –VITA 46.10.
It provides rear I/O peripherals connectivity for Kontron VX3060-S2 Single Board Computers.

Figure 48: PB-VX3-40G-602 3U VPX Overview



6.1.2. Ordering Information

Table 48: RTM tooling - Order Codes

Standard Order Codes	Description
PB-VX3-40G- 602	3U single slot 5 HP (1.0") VPX Rear Transition Module providing provides seria lines, USB2.0 and USB3.0, SATA, 1000Base-T Ethernet, mDP++ VX3060-S2 Tooling equipment for lab use.

This RTM is compatible with VX3060-S2 Compute Intensive Variants.
Do not use with I/O Intensive boards and other VPX ecosystems.
When plugged in an existing VPX ecosystem, the available and usable interfaces of the RTM will depend on the VX3060-S2 variant and the backplane used.

6.1.3. Identification and labels

The RTM is identified by labels fitted to the VPX connector on the top side of the board.
Example on the picture below.

Table 49: RTM tooling - Identification

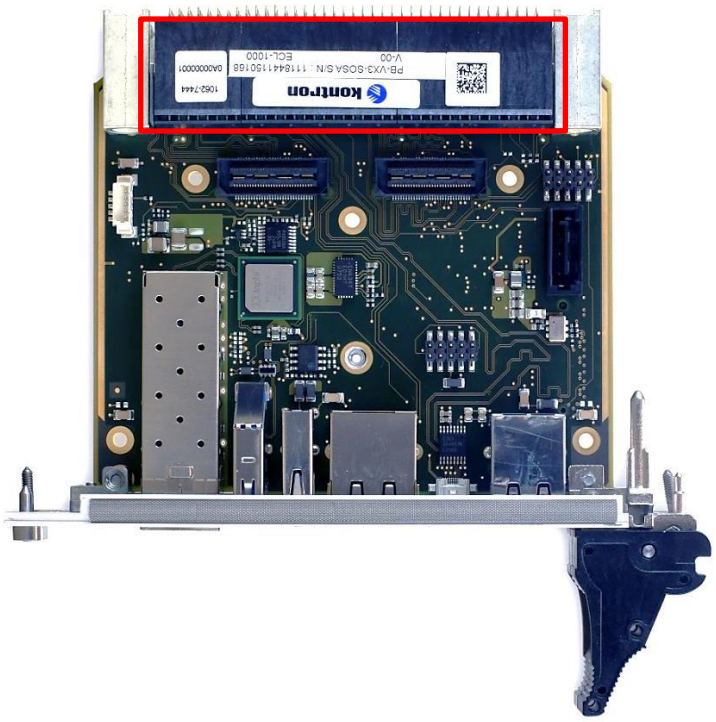


Table 50: PB-VX3-40G-602 Technical Specifications

TECHNICAL SPECIFICATIONS	
Power Specification	
Supply Voltage	5V VS3 VPX, 12V VS1 VPX
Consumption	< 1A
USB Ports maximum current	1 A
Mechanical Specification	
Front Panel size	1 slot (5HP) for PB-VX3-40G-602
Dimension (mm)	100 x 81.5
Weight (g)	~200
Environmental Specification	
Conformal coating	Not available
Operating temperature	10°C/35°C (lab use)

5V VS3 VPX power supply must be provided to RTM for full operating

6.1.4. Front Panel Interfaces

Figure 33: PB-VX3-40G- 602 Front Panel I/O Interfaces

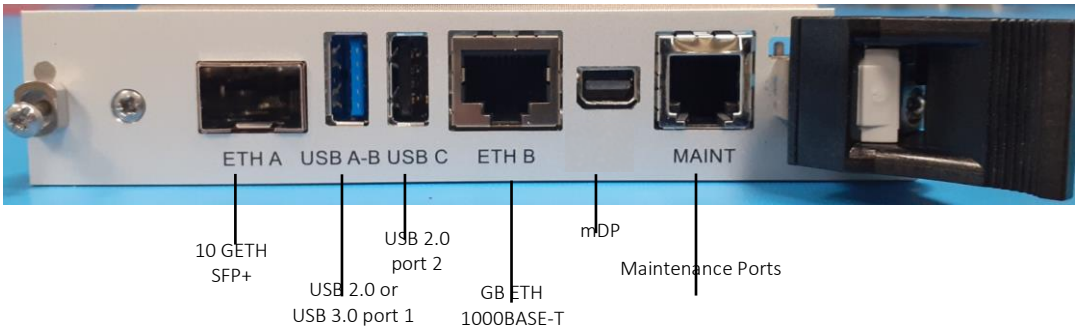


Table 51: PB-VX3-40G-602 Front Panel Connector Descriptions

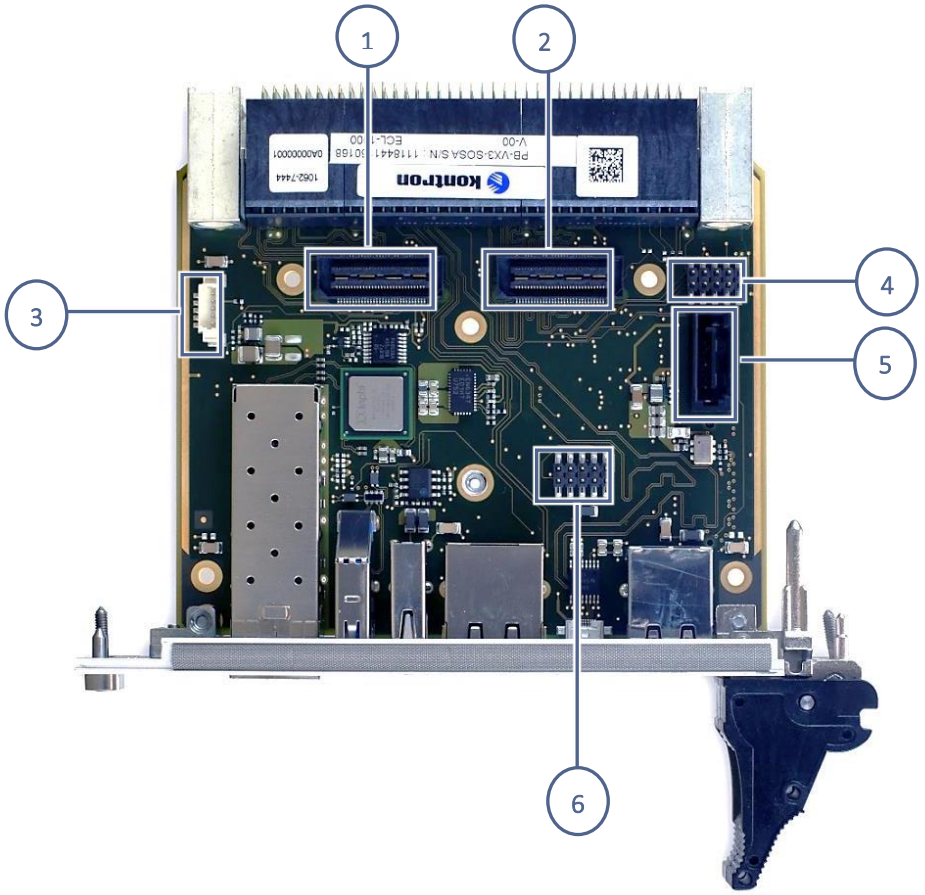
Front Panel Name	Description	Comment
USB A-B	USB 3.0 Legacy interface Or USB 2.0 interface (port 1)	
USB C	USB 2.0 interface (port 2)	
ETH A	10 Gigabit Ethernet interface ETH0 implemented on SFP+ cage	**Contact Kontron support for availability status.** Refer also to the D276230 document for more information.
ETH B	Gigabit Ethernet interface implemented on RJ-45 connector (1000BASE-T)	
MAINT	COM1/2: maintenance port , EIA-232 or 3.3V LVCMOS level signaling - RJ-12 connector	
mDP	Graphics: mini Display Port	

⚠CAUTION Total current of USBs ports (draw simultaneously) must not exceed 1A to avoid RTM damage.

6.1.5. On-boards Interfaces

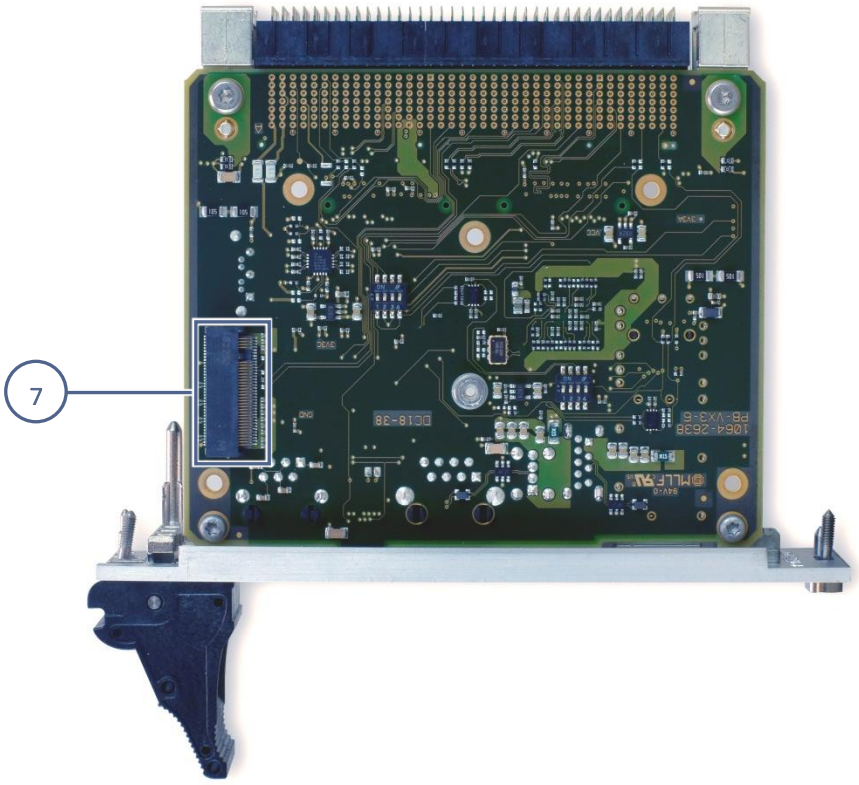
The PB-VX3-40G-602 implements on-boards connectors in order to provide access to additional I/O interfaces such as SATA, COM2 serial line, GPIOs and PCIe.

Figure 34: PB-VX3-40G-602 On-board I/O Interfaces (top)



1. J0602
2. J0601
3. J0403
4. J0402
5. P1101
6. J0401
7. J1801

Figure 35: PB-VX3-40G-602 On-board I/O Interfaces (bottom)



1. J0602
2. J0601
3. J0403
4. J0402
5. P1101
6. J0401
7. J1801

Table 52: PB-VX3-40G-602 On-boards Connector Descriptions

Connector Name	Description	Comment
J0602	XMC IO PIM2 connector	Refer to section 6.3.2.4 for the pinout assignment.
J0601	XMC IO PIM1 connector	Refer to section 6.3.2.4 for the pinout assignment.
J0403	I2C connector for PHY EEPROM reprogramming or for IPMB-B access depending on SW0401[1-4] microswitch position	Refer to section 6.2.4 for the detailed of microswitch position and to section for pinout assignment.
J0402	GPIOs connector up to 8 GPIOs access and maskable reset access	Refer to section 6.3.2.2 for the pinout assignment.
P1101	SATA connector	Refer to section 6.3.2.3 for the pinout assignment.
J0401	COM2 serial port, EIA-232/485/422 – HE10 connector	Refer to section 6.3.2.1 for the pinout assignment.
J1801	PCIe 4x interface on M.2 key M type 3 slot	Refer to section 6.3.2.6 for the pinout assignment.

6.2. Installation

The standard precautions, installation procedures must also be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

6.2.1. Safety Requirements

The following safety precautions must be observed when installing or operating the RTM. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

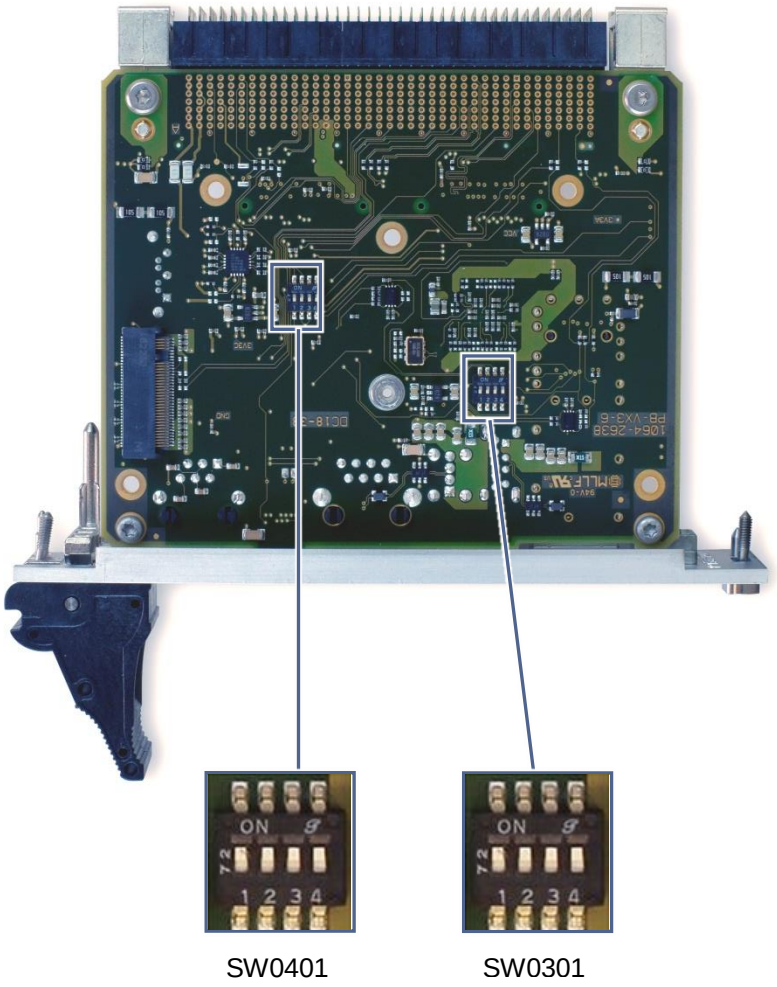
NOTICE

ESD Sensitive Device!
This RTM contains electrostatically sensitive devices. Observe the necessary precautions to avoid damage to your board:
Discharge your clothing before touching the assembly. Tools must be discharged before use.
Do not touch components, connector pins or traces.
We strongly recommend our customers to work in an environment equipped with anti-static workbenches with professional discharging equipment

6.2.2. Microswitches location

Two microswitches are available on the PB-VX3-40G-602: SW0301 and SW0401

Figure 36: PB-VX3-40G-602 Microswitch Location



6.2.3. SW0301 Microswitch Description

Table 53: SW0301 Microswitch Description

FUNCTION	DESCRIPTION
1 – EEPROM WP	off: The 10Gb Ethernet retimer EEPROM is write protected Default setting on: The EEPROM is not write protected
2 – Reserved	Used for test and debug purpose only. Default setting is OFF
3 – Reserved	Must be OFF
4 – Reserved	Must be OFF

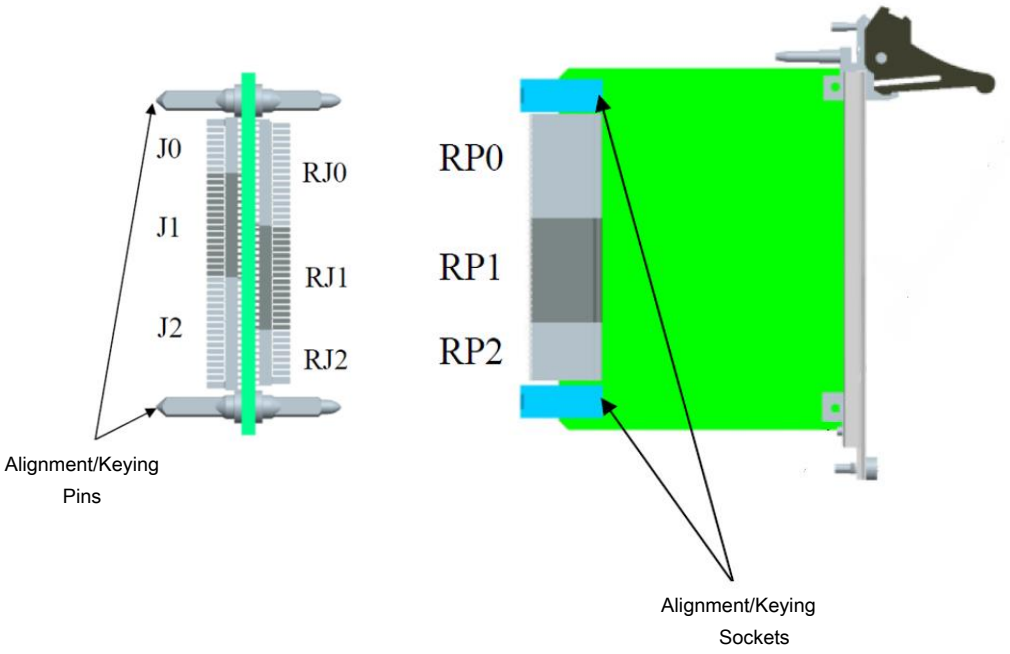
6.2.4. SW0401 Microswitch Description

SW0401 microswitch is used for test and debug purpose only. Default setting is OFF for all switches.

To access to IPMB-B bus on J0403 connector the SW0401[1] and SW0401[2] microswitch have to be set ON.

6.2.5. RTM Connectors Identification

Figure 37: Connectors Identification for PB-VX3-40G-602



6.2.6. Initial Installation Procedure

The following procedures are applicable only for the initial installation of the PB-VX3-40G-602 in a system. Procedures for standard removal operations are found in their respective chapters.
To perform an initial installation of the PB-VX3-40G-602 in a system proceed as follows:

1. Ensure that the safety requirements indicated in section 2 are observed.

⚠CAUTION	Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the RTM is properly configured for operation in accordance with application requirements before installing.

⚠CAUTION	Care must be taken when applying the procedures below to ensure that neither the PB-VX3-40G-602 nor other system boards are physically damaged by the application of these procedures.

3. To install the PB-VX3-40G-602, perform the following:

a. Ensure that no power is applied to the system before proceeding.

b. Carefully insert the RTM into the slot designated by the application requirements for the RTM until it makes contact with the backplane connectors.

	When performing the next step DO NOT push the RTM into the backplane connectors. It is recommended to use the ejector handles to seat the RTM into the backplane connectors.

c. Engage the RTM with the backplane using the ejector handle. When the ejector handle is locked, the RTM is engaged.

d. Fasten the front panel retaining screws.

e. Connect all external interfacing cables to the board as required.

f. Ensure that the RTM and all required interfacing cables are properly secured.

The PB-VX3-40G-602 is now ready for operation.

6.2.7. Standard Removal Procedure

ESD sensitive Device! Precautions are listed in Section 2.

To remove the board from the chassis proceeds as follows:

1. Ensure that the safety requirements indicated in section 2 are observed.

⚠CAUTION Care must be taken when applying the procedures below to ensure that neither the PB-VX3-40G-602 nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the RTM.
4. Unscrew the front panel retaining screws.
5. Disengage the RTM from the backplane by first unlocking the RTM ejection handles and then by pressing the handles as required until the RTM is disengaged.
6. After disengaging the RTM from the backplane, pull the RTM out of the slot.
7. Dispose of the RTM as required.

6.3. Physical I/Os

The following section lists the physical I/Os that are different from RTMs variant.

6.3.1. Front Panel

6.3.1.1. Maintenance Port Connector

The PB-VX3-40G-602 provides one serial maintenance port, COM1 on front panel RJ12 connector. COM1 operate either in EIA-232 mode only (simplified RX/TX) or in 3.3V LVCMOS level signaling without hardware modification.

Defaults setting are:

- Processor console is redirected on COM1
- Serial mode is simplified EIA-232 serial line mode Rx/Tx only, 115200 bauds

Serial port is configurable via the BIOS setup menu as EIA-232 or 3.3V LVCMOS level signaling. Serial port operates in full duplex mode.

› Pin Assignment

Table 54: Serial Connector Pin Assignment

PIN	SIGNAL
1	Reserved
2	Shell
3	COM1 TXD
4	COM1 RXD
5	GND
6	Reserved

Figure 38: Serial Connector

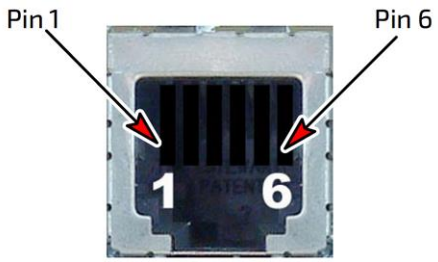


Table 55: Serial Connector Signal Description

MNEMONIC	DESCRIPTION
COM1 RXD	COM1 Receive Data
COM1 TXD	COM1 Transmit Data
GND	Ground
Shell	Chassis Ground

› Serial Cable Designation

The Serial cable shall be shielded and shall provide a good shielding continuity between each end. The Serial cable length should not exceed 10 m.

Serial cable is a RJ-12 (6 pin, 6 conductors). A RJ-12 to DB9 male or DB9 female adapter is available from multiple sources, such as:

- Kontron Order Code KIT-RJ12DB9
- Triangle Cable http://www.trianglecables.com/db9m-rj12.html

Table 56: Serial Cable Pin Assignment

DB9 A Pin Connector	Signal	RJ-12 Pin Connector
-	-	1
2	TXD0	3
3	RXD0	4
-	-	6
5	GND	5

Figure 39: Serial Cable

DB9 A of cable RJ12DB9 shall be used with PB-VX3-40G-602 to access to maintenance port (COM1) of VX3060-S2 board.

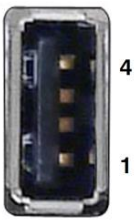
6.3.1.2. USB 2.0 Connector

USB cable shall be compliant to Universal Serial Bus Specification, Revision 2.0.
This USB cable shall have double shielding.
The USB cable length should not exceed 3 m.

Table 57: USB 2.0 Connector Pin Assignment

PIN	SIGNAL	function	I/O
1	VCC	VCC (+5V Protected)	O
2	USB_D-	Differential USB-	I/O
3	USB_D+	Differential USB+	I/O
4	GND	GND	--

Figure 40: USB 2.0 Connector



USB

6.3.1.3. USB 3.0 Connector

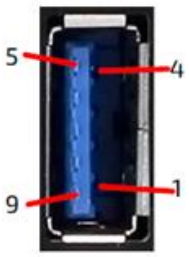
The PB-VX3-40G-602 provides an USB front connector carrying USB 2.0 port and USB 3.0 port USBSS.

USB cable shall be compliant to Universal Serial Bus Specification, Revision 3.0.
This USB cable shall have double shielding.
The USB cable length should not exceed 3 m.

Table 58: USB 3.0 Connector Pin Assignment

PIN	SIGNAL	function	I/O
1	VBUS	+5V Protected by 1.5A fuse	O
2	USB_D-	Differential USB-	I/O
3	USB_D+	Differential USB+	I/O
4	GND	Logic Ground	-
5	STDA_SSRX-	Negative SuperSpeed receiver differential pair	I
6	STDA_SSRX+	Positive SuperSpeed receiver differential pair	I
7	GND_DRAIN	Logic Ground	-
8	STDA_SSTX-	SuperSpeed transmitter differential pair	O
9	STDA_SSTX+	SuperSpeed transmitter differential pair	O

Figure 41: USB 3.0 Connector



6.3.1.4. SPF+ Connector

Contact Kontron for pin assignment and availability of SFP+ cage feature.

6.3.1.5. Gigabit Ethernet Connector

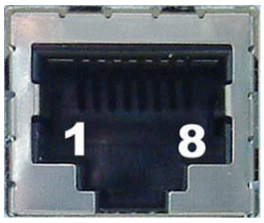
The Ethernet cable shall be CAT6 compliant.
This Ethernet cable shall be S/FTP type at least (Shielded Foiled Twisted Pair), providing shielding continuity between each end.
The Ethernet transmission should operate using a CAT6 cable with a maximum length of 100 m.

The Ethernet connectors are available as RJ-45 connectors with tab down. The interface provides automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

Table 59: Gigabit Ethernet Connector Pin Assignment

pin	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-		I/O	BI_DC+
5	-	-	-		I/O	BI_DC-
6	I	RX-	I	RX-	I/O	BI_DB-
7	-	-	-		I/O	BI_DD+
8	-	-	-		I/O	BI_DD-
Shell	Chassis Ground					

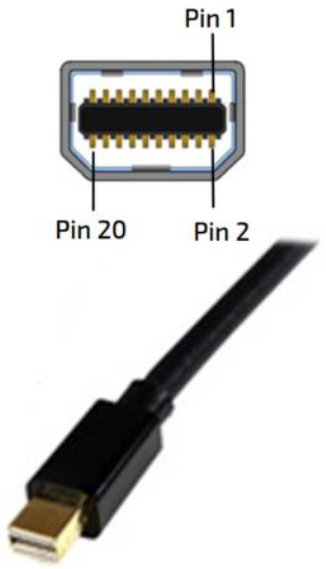
Figure 42: RJ45 Ethernet Connector



6.3.1.6. Mini DisplayPort Connector

The PB-VX3-40G-602 provides a mini DP front connector offering DP graphics interface on front panel.

PIN	SIGNAL	FUNCTION
1	GND	Ground
2	HPD	Hot Plug Detect
3	Lane0+	Lane 0 Positive
4	Config1	Config1, dongle detect for dual-mode DP (mDP++)
5	Lane0-	Lane 0 negative
6	Config2	Config2, pulled low by XMC-GPU91
7	GND	Ground
8	GND	Ground
9	Lane1+	Lane 1 positive
10	Lane3+	Lane 3 positive
11	Lane1-	Lane 1 negative
12	Lane3-	Lane 3 negative
13	GND	Ground
14	GND	Ground
15	Lane2+	Lane 2 positive
16	Aux+	Auxilliary+
17	Lane2-	Lane 2 negative
18	Aux-	Auxilliary-
19	GND	Ground
20	PWR	Power (3.3V, 500 mA max)



6.3.2. On-board Connectors

In addition of front panel connectors, the PB-VX3-40G-602 implements on-boards connectors in order to provide access to extra I/O interfaces such as SATA, COM2 serial line, GPIOs and PCIe.

6.3.2.1. COM2 Serial line

The PB-VX3-40G-602 implements a HE10 connector offering COM2 serial interface.

Table 60: HE10 J0401 Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	COM2_RXD-	2	NC
3	NC	4	COM2_TXD-
5	NC	6	GND
7	COM2_RXD+	8	COM2_TXD+
9	NC	10	NC

Figure 43: HE10 J0401 Connector

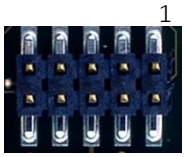


Table 61: Serial Connector Signal Description

MNEMONIC	DESCRIPTION
COM2 TXD+	COM2 Transmit Data+ or Hi-Z in EIA-232 mode
COM2 TXD-	COM2 Transmit Data- or COM2 Transmit Data in EIA-232 mode
COM2 RXD+	COM2 Receive Data+ or Hi-Z in EIA-232 mode
COM2 RXD-	COM2 Receive Data- or COM2 Transmit Data in EIA-232 mode
GND	Ground

6.3.2.2. GPIO connector

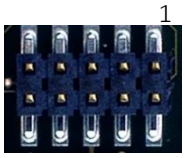
The PB-VX3-40G-602 integrates a HE10 connector providing up to 8 GPIOs access and maskable reset access.

Table 62: HE10 J0402 Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	GPIO5	2	GPIO7
3	GPIO6	4	MRST/GPIO8*
5	GND	6	GND
7	GPIO2	8	GPIO1
9	GPIO4	10	GPIO3

* GPIO8 or maskable reset

Figure 44: HE10 J0402 Connector



6.3.2.3. SATA connector

The onboard SATA standard connector is used to connect a SATA HDD. The following table provides pinout information for the onboard SATA connector P1101:

Table 63: SATA onboard P1101 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	GND	Ground Signal	--
2	SATA2 TX+	Differential Transmit +	O

Figure 45: SATA onboard Connector

3	SATA2 TX-	Differential Transmit -	O
4	GND	Ground Signal	--
5	SATA2 RX-	Differential Receive -	I
6	SATA2 RX+	Differential Receive +	I
7	GND	Ground Signal	--

6.3.2.4. XMC IO PIM Connectors

The onboard PIM connectors provide access to single-ended and differential XMC IO, the XMC IO are available on two connectors J0601 and J0602.

Figure 46: PIM onboard Connector

Table 64: PIM1 onboard J0601 Pinout

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	GND
3	VCC	4	NC
5	VCC	6	XMCIO_DP15-
7	VCC	8	XMCIO_DP15+
9	VCC	10	GND
11	GND	12	XMCIO_DP16-
13	XMCIO_DP17-	14	XMCIO_DP16+
15	XMCIO_DP17+	16	GND
17	GND	18	XMCIO_DP18-
19	XMCIO_DP19-	20	XMCIO_DP18+
21	XMCIO_DP19+	22	GND
23	GND	24	XMCIO_DP10-
25	XMCIO_DP9-	26	XMCIO_DP10+
27	XMCIO_DP9+	28	GND
29	GND	30	XMCIO_DP8-
31	XMCIO_DP7-	32	XMCIO_DP8+
33	XMCIO_DP7+	34	XMCIO_DP6-
35	GND	36	XMCIO_DP6+
37	+12V	38	NC
39	GND	40	NC
41	+3V3_AUX	42	GND
43	GND	44	NC
45	NC	46	NC
47	GND	48	GND
49	XMCIO_DP5-	50	NC
51	XMCIO_DP5+	52	NC
53	GND	54	GND
55	NC	56	NC
57	NC	58	NC
59	GND	60	GND

Table 65: XMCIO PIM1 Connector Signal Description

MNEMONIC	DESCRIPTION
XMCIO_DP5-10 XMCIO_DP15-19	Differential pairs XMC I/O 5 to 10 and 15 to 19 as per to VITA 46.9 P1w9-X12d

VCC	+5 Volts DC power (VS3 VPX supply).
+12V	+12 Volts DC power (VS1 VPX supply).
+3V3_AUX	+3.3 Volts DC auxiliary power
NC	Not Connected
GND	Ground

Table 66: PIM2 onboard J0602 Pinout

Figure 47: PIM onboard Connector

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	GND
3	VCC	4	+12V
5	VCC	6	GND
7	GND	8	+3V3_AUX
9	XMCIO_DP20-	10	GND
11	XMCIO_DP20+	12	XMCIO_SE15
13	NC	14	XMCIO_SE16
15	SYSRESET*	16	XMCIO_SE13
17	GND	18	XMCIO_SE14
19	XMCIO_SE11	20	XMCIO_SE12
21	XMCIO_SE9	22	XMCIO_SE10
23	GND	24	GND
25	XMCIO_SE8	26	XMCIO_SE7
27	XMCIO_SE6	28	XMCIO_SE5
29	GND	30	GND
31	XMCIO_SE3	32	XMCIO_SE4
33	XMCIO_SE1	34	XMCIO_SE2
35	GND	36	GND
37	XMCIO_DP2-	38	XMCIO_DP1-
39	XMCIO_DP2+	40	XMCIO_DP1+
41	GND	42	GND
43	XMCIO_DP4-	44	XMCIO_DP3-
45	XMCIO_DP4+	46	XMCIO_DP3+
47	GND	48	GND
49	XMCIO_DP12-	50	XMCIO_DP11-
51	XMCIO_DP12+	52	XMCIO_DP11+
53	GND	54	GND
55	XMCIO_DP14-	56	XMCIO_DP13-
57	XMCIO_DP14+	58	XMCIO_DP13+
59	GND	60	GND

* signal active when low

Table 67: XMCIO PIM2 Signal Description

MNEMONIC	DESCRIPTION
XMCIO_DP20	Differential pairs XMC I/O 20 as per to VITA 46.9 P1w9-X12d
XMCIO_DP1-8	Differential pairs XMC I/O 1 to 8 as per VITA 46.9 P2-X8d
XMCIO_SE1-16	Single-Ended XMC I/O 1 to 16 as per VITA 46.9 P2w9-X16s
VCC	+5 Volts DC power (VS3 VPX supply).
+12V	+12 Volts DC power (VS1 VPX supply).
+3V3_AUX	+3.3 Volts DC auxiliary power

SYSRESET#	System Reset. Input and open collector output.
NC	Not Connected
GND	Ground

6.3.2.5. I2C connector

The onboard I2C connector (J0403) provide IMPB-B bus access. The following table provides pinout information for the onboard I2C connector J0403:

Table 68: I2C onboard J0403 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	SMB_CLK	I2C serial clock	I
2	GND	Ground Signal	--
3	SMB_DAT	I2C bi-directional serial data	I/O
4	+3.3V	+3.3V power supply	I/O
5	GND	Ground Signal	--

Figure 48: I2C onboard Connector

6.3.2.6. M.2 PCIe Slot

The M.2 bottom socket (J1801 connector) is used to connect a M.2 module, key M for SSD storage. PCIe 4x Gen3 is the default interface of SSD storage module.

The M.2 socket supports only 2242 form factor.

Table 69: J2801 M.2 Socket Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	3V3
3	GND	4	3V3
5	PER3-	6	NC
7	PER3+	8	NC
9	GND	10	NC
11	PET3-	12	3V3
13	PET3+	14	3V3
15	GND	16	3V3
17	PER2-	18	3V3
19	PER2+	20	NC
21	GND	22	NC
23	PET2-	24	NC
25	PET2+	26	NC
27	GND	28	NC
29	PER1-	30	NC
31	PER1+	32	NC
33	GND	34	NC
35	PET1-	36	NC
37	PET1+	38	NC
39	GND	40	NC
41	PER0-	42	NC
43	PER0+	44	NC
45	GND	46	NC
47	PET0-	48	NC

PIN	SIGNAL	PIN	SIGNAL
49	PET0+	50	PERST#
51	GND	52	CLKREQ# (PU)
53	REFCLK_N	54	PEWAKE# (PU)
55	REFCLK_P	56	NC
57	GND	58	NC
59	CONNECTOR_KEY	60	CONNECTOR_KEY
61	CONNECTOR_KEY	62	CONNECTOR_KEY
63	CONNECTOR_KEY	64	CONNECTOR_KEY
65	CONNECTOR_KEY	66	CONNECTOR_KEY
67	NC	68	NC
69	NC	70	3V3
71	GND	72	3V3
73	GND	74	3V3
75	GND		

Table 70: M.2 Module Socket Signal Description

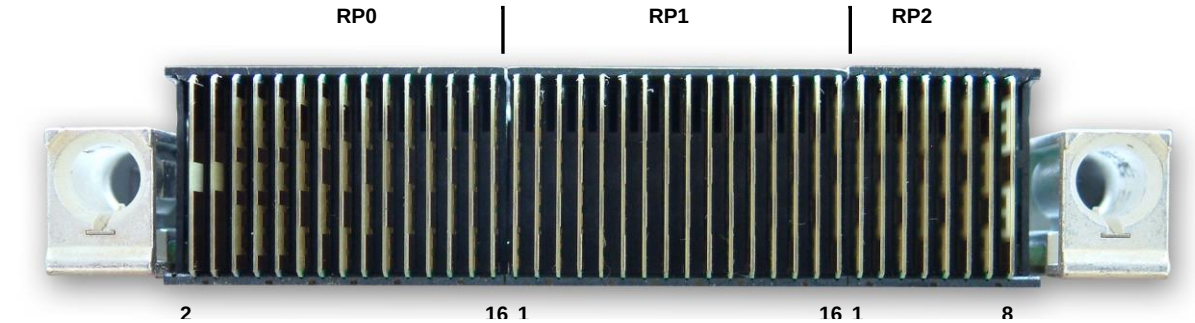
MNEMONIC	DIRECTIO	SIGNAL DEFINITION
3.3V	O	+3.3V power supply.
GND	-	Logic ground.
PERn+/-	I	PCI Express: Receive differential pair as per PCI Express M.2 & PCI Express 3.0 specifications.
PERST#	O	PCI Express: PCI Express PERST# as per PCI Express M.2 specification, handled by CPLD (SYSRESET).
PETn+/-	O	PCI Express: Transmit differential pair as per PCI Express M.2 & PCI Express 3.0 specifications.
PEWAKE#	I	PCI Express: Opain drain WAKE# signal as per PCI Express M.2.
REFCLKP/N	O	
CLKREQ#	O	

6.3.3. Rear I/O Connectors

The PB-VX3-40G-602 Rear Transition Module conducts a wide range of I/O signals through the rear I/O connectors RP0, RP1 and RP2.

- RP0: 15-wafer 7-row mixed connector.
- RP1: 16-wafer 7-row differential connector.
- RP2: 8-wafer 7-row differential connectors.

Figure 49: Rear I/O VPX Connectors



RP0 Wafer Assignment

Table 71: Rear I/O VPX Connector RP0 Wafer Assignment

Legend for Table 71:

IPMB_B/A	IPMB I2C bus	GPIO7	GPIO7
USB1	USB1 power	PCIe0 Lx-Tx/Rx	x4 PCI-Express

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	No wafer						
2	+12V	+12V	+12V	NC	NC	NC	NC
3	+5V	+5V	+5V	NC	+5V	+5V	+5V
4	IPMB_B CLK	IPMB_B DAT	GND	NC	GND	SYSRESET*	NC
5	NC	NC	GND	NC	GND	IPMB_A CLK	IPMB_A DAT
6	NC	NC	GND	NC	GND	NC	NC
7	GPIO7	GND	NC	NC	GND	GPIO5	GPIO6
8	GND	NC	NC	GND	NC	NC	GND
9	NC	GND	NC	NC	GND	NC	NC
10	GND	NC	NC	GND	NC	NC	GND
11	NC	GND	NC	NC	GND	NC	NC
12	GND	NC	NC	GND	NC	NC	GND
13	NC	GND	PCIe0 L0-TX-	PCIe0 L0-TX+	GND	PCIe0 L0-RX-	PCIe0 L0-RX+
14	GND	PCIe0 L1-TX-	PCIe0 L1-TX+	GND	PCIe0 L1-RX-	PCIe0 L1-RX+	GND
15	USB1 PWR	GND	PCIe0 L2-TX-	PCIe0 L2-TX+	GND	PCIe0 L2-RX-	PCIe0 L2-RX+
16	GND	PCIe0 L3-TX-	PCIe0 L3-TX+	GND	PCIe0 L3-RX-	PCIe0 L3-RX+	GND
CASE	GND						

* signal active when low

Table 72: Rear I/O VPX Connector RP0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
+12V	+12 Volts DC power (VS1 VPX supply). NC (+12V) pins are not connected (VS2 VPX supply)
+5V	+5 Volts DC power (VS3 VPX supply).
GND	Ground
PCIe0 Lx-RX+/-	x4 PCI Express Link. Receive +/-, gen1, gen2 or gen3 routed to on-board M.2 connector, see section 6.3.2.6 May also be used as a 4 x2 links on customer request.
PCIe0 Lx-TX+/-	x4 PCI Express Link. Transmit +/-, gen1, gen2 or gen3 routed to on-board M.2 connector, see section 6.3.2.6 May also be used as a 4 x2 links
GPIO 5, 6, 7*	General purpose I/O (handled by CPLD). GPIO 5 and 6 not connected by default, and they are multiplexed with Ethernet 10G I2C bus signals for rear SFP+ operation. See BIOS User Manuel Section 6.1.1 for configuration (GPIO is default mode). Contact Kontron support for availability.
IPMB A	I2C Bus 0
IPMB B	I2C Bus 1
SYSRESET*	System Reset. Input and open collector output.
NC	Not connected

RP1 Wafer Assignment

Table 73: Rear I/O VPX Connector RP1 Wafer Assignment

Legend for Table 73:

SATA	SATA link 3 from PCH	GPIOx / Maskable Reset	General Purpose I/O x and maskable reset
ETH1 TX/RX	10GBASEKR link 1 from integrated 10 GbE controller as per VITA 46.7.	ETH2 DA/DB/DC/DD	1000BASE-T link from I210IT GbE controller
COM1/COM2	Maintenance Port / COM2 serial line	DP++	Graphics DP++ interface
USBSS USB2	USB 3.0 link from PCH USB 2.0 link from PCH	XMCIO X12d	Differential XMC IO pins according VITA46.9 X12d

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	COM1 TXD	GND	XMCIO_DP5-	XMCIO_DP5+	GND	XMCIO_DP6-	XMCIO_DP6+
2	GND	XMCIO_DP7-	XMCIO_DP7+	GND	XMCIO_DP8-	XMCIO_DP8+	GND
3	COM1 RXD	GND	XMCIO_DP9-	XMCIO_DP9+	GND	XMCIO_DP10-	XMCIO_DP10+
4	GND	XMCIO_DP15-	XMCIO_DP15+	GND	XMCIO_DP16-	XMCIO_DP16+	GND
5	GPIO1	GND	XMCIO_DP17-	XMCIO_DP17+	GND	XMCIO_DP18-	XMCIO_DP18+
6	GND	XMCIO_DP19-	XMCIO_DP19+	GND	XMCIO_DP20-	XMCIO_DP20+	GND
7	Maskable Reset*	GND	ETH1 TX-	ETH1 TX+	GND	ETH1 RX-	ETH1 RX+
8	GND	NC	NC	GND	NC	NC	GND
9	COM2 TXD-	GND	DP++ L1-	DP++ L1+	GND	DP++ L2-	DP++ L2+
10	GND	DP++ CLK-	DP++ CLK+	GND	DP++ L0-	DP++ L0+	GND
11	COM2 TXD+	GND	DP++ PWR	DP++ HPD	GND	DP++ AUX-	DP++ AUX+
12	GND	USB2 D-	USB2 D+	GND	USB1 D-	USB1 D+	GND
13	COM2 RXD-	GND	USBSS TX-	USBSS TX+	GND	USBSS RX-	USBSS RX+
14	GND	SATA TX-	SATA TX+	GND	SATA RX-	SATA RX+	GND
15	COM2 RXD+	GND	ETH2 DB-	ETH2 DB+	GND	ETH2 DA-	ETH2 DA+
16	GND	ETH2 DD-	ETH2 DD+	GND	ETH2 DC-	ETH2 DC+	GND
CASE	GND						

* signal active when low

Table 74: Rear I/O VPX Connector RP1 Signal Definition

MNEMONIC	SIGNAL DEFINITION
XMCIO_DP5-10 XMCIO_DP15-20	Differential pairs XMC I/O 5 to 10 and 15 to 20 as per VITA 46.9 P1w9-X12d
ETH1 RX+/-	10GBASE-KR or 1000BASE-KX Ethernet 1: Receive data +/- (auto negotiation)
ETH1 TX+/-	10GBASE-KR or 1000BASE-KX Ethernet 1: Transmit data +/- (auto negotiation)
COM1	Maintenance port : serial Lines EIA-232 or 3V3 signal leveling
COM2	Serial Lines, EIA-232/EIA-485
GPIO1*	Not connected (General Purpose I/O 1 (handled by the CPLD))
Maskable Reset* or GPIO8	Reset input or Optional general purpose I/O 8 (handled by CPLD) (may be left unconnected if not used).
ETH2 DA+/-	Ethernet 1000BASE-T: First pair of transmit/receive data.
ETH2 DB+/-	Ethernet 1000BASE-T: Second pair of transmit/receive data
ETH2 DC+/-	Ethernet 1000BASE-T: Third pair of transmit/receive data.
ETH2 DD+/-	Ethernet 1000BASE-T: Fourth pair of transmit/receive data
DP++	DP++ Port
SATA RX+/-	Serial ATA. Receive +/-
SATA TX+/-	Serial ATA. Transmit +/-
USBSS TX+/- RX+/-	Differential Data transmit and receive of USBSS link
USBx D+/-	Differential Data pair of USB x
NC	Not connected
GND	Ground

RP2 Wafer Assignment

Table 75: Rear I/O VPX Connector RP2 Wafer Assignment

Legend for Table 36:

USB2 PWR	USB 2 power	XMCIO_DP1-8	Differential XMC IO pins according VITA46.9 X8d
GPIOx	General Purpose I/O x	XMCIO_SE1-16	Single ended XMC IO according VITA46.9 X16s

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	USB2 PWR	GND	XMCIO_SE15	XMCIO_SE13	GND	XMCIO_SE16	XMCIO_SE14
2	GND	XMCIO_SE11	XMCIO_SE9	GND	XMCIO_SE12	XMCIO_SE10	GND
3	GPIO2	GND	XMCIO_SE7	XMCIO_SE5	GND	XMCIO_SE8	XMCIO_SE6
4	GND	XMCIO_SE3	XMCIO_SE1	GND	XMCIO_SE4	XMCIO_SE2	GND
5	GPIO3	GND	XMCIO_DP1-	XMCIO_DP1+	GND	XMCIO_DP2-	XMCIO_DP2+
6	GND	XMCIO_DP3-	XMCIO_DP3+	GND	XMCIO_DP4-	XMCIO_DP4+	GND
7	GPIO4	GND	XMCIO_DP11-	XMCIO_DP11+	GND	XMCIO_DP12-	XMCIO_DP12+
8	GND	XMCIO_DP13-	XMCIO_DP13+	GND	XMCIO_DP14-	XMCIO_DP14+	GND
CASE	GND						

* signal active when low

Table 76: Rear I/O VPX Connector RP2 Signal Definition

MNEMONIC	SIGNAL DEFINITION
GPIOx*	General Purpose I/O x (handled by the CPLD).
USB PWR	USB Power limited to 1 Amps
XMCIO_SE1-16	Single ended XMC I/O 1 to 16 according to VITA 46.9 X16s
XMCIO_DP1-4/11-14	Differential pairs XMC I/O 1 to 4 and 11 to 14 according to VITA 46.9 X8d
NC	Not connected
GND	Ground

7. Technical Support

For technical support, contact our Support Department:
E-Mail: support.KFR@kontron.com
Phone: +33-498-163-400

Make sure you have the following information available when you call:
Product ID Number (PN),
Serial Number (SN)

The serial number can be found on the Type Label, located on the product's rear side.

Be ready to explain the nature of your problem to the service technician.

8. Warranty

Due to their limited service life, parts that by their nature are subject to a particularly high degree of wear (wearing parts) are excluded from the warranty beyond that provided by law. This applies to the CMOS battery, for example.

If there is a protection label on your product, then the warranty is lost if the product is opened.

9. Returning Defective Merchandise

All equipment returned to Kontron must have a Return of Material Authorization (RMA) number assigned exclusively by Kontron. Kontron cannot be held responsible for any loss or damage caused to the equipment received without an RMA number. The buyer accepts responsibility for all freight charges for the return of goods to Kontron's designated facility. Kontron will pay the return freight charges back to the buyer's location in the event that the equipment is repaired or replaced within the stipulated warranty period. Follow these steps before returning any product to Kontron.
Visit the RMA Information website: https://www.kontron.com/en/support/rma-information

TO REQUEST A RETURN MATERIAL AUTHORIZATION (RMA) NUMBER

1. E-mail to repair.KFR@kontron.com with the following information:
2. Part number, serial number of the material to be returned,
3. Failure description or reason for return
4. Once everything is completed, an RMA form will be sent to you if your equipment is under warranty. If your equipment is not under warranty, a quote will be sent and the RMA will be sent when we receive your PO.
5. Print the RMA form and put it with the material to be returned
6. Ship the goods to the address indicated on the RMA form

The goods for repair must be packed properly for shipping, considering shock and ESD protection.

Goods returned to Kontron Modular Computers S.A.S in non-proper packaging will be considered as customer caused faults and cannot be accepted as warranty repairs.

About Kontron

Kontron is a global leader in IoT/Embedded Computing Technology (ECT) and offers individual solutions in the areas of Internet of Things (IoT) and Industry 4.0 through a combined portfolio of hardware, software and services. With its standard and customized products based on highly reliable state-of-the-art technologies, Kontron provides secure and innovative applications for a wide variety of industries. As a result, customers benefit from accelerated time-to-market, lower total cost of ownership, extended product lifecycles and the best fully integrated applications.

For more information, please visit: **www.kontron.com**

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