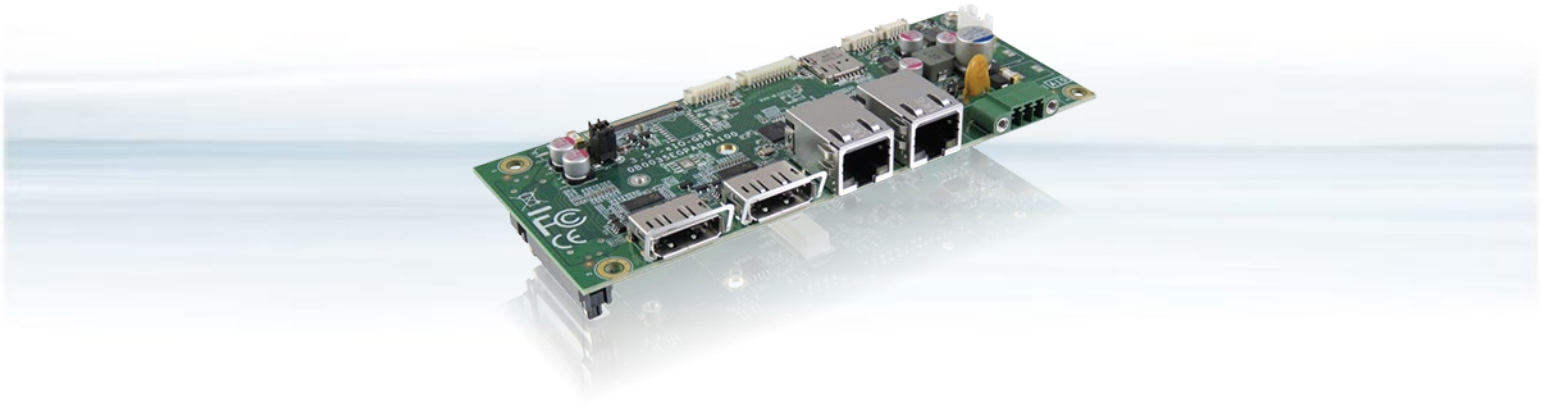
USER GUIDE



# 3.5"-eIO-GPA

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# 3.5"-EIO-GPA - USER GUIDE

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## Revision History

| Revision | Brief Description of Changes | Date of Issue | Author/ Editor |
|---|---|---|---|
| 1.0 | Initial Issue | 2022-Aug-26 | YS |
| 1.1 | Update Ethernet controller I225-IT → I226-IT | 2022-Oct-20 | YS |
| 1.2 | Update Ethernet controller I225-LM → I226-LM | 2023-Mar-14 | YS |
| 1.3 | Add connectors' availability info | 2024-Mar-18 | YS |

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# Symbols

The following symbols may be used in this user guide

| | |
|---|---|
| **⚠DANGER** | DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury. |
| **⚠WARNING** | WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury. |
| ***NOTICE*** | NOTICE indicates a property damage message. |
| **⚠CAUTION** | CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury. |
|  | Electric Shock!<br>This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material. |
|  | ESD Sensitive Device!<br>This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times. |
|  | HOT Surface!<br>Do NOT touch! Allow to cool before servicing. |
|  | Laser!<br>This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing. |
|  | This symbol indicates general information about the product and the user guide.<br>This symbol also indicates detail information about the specific product configuration. |
|  | This symbol precedes helpful hints and tips for daily use. |

# For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

## High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

**⚠CAUTION**

Warning

**All operations on this product must be carried out by sufficiently skilled personnel only.**

**⚠CAUTION**

Electric Shock!

**Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.**

**Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.**

## Special Handling and Unpacking Instruction

***NOTICE***

ESD Sensitive Device!

**Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.**

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

### Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

**⚠CAUTION**

**Danger of explosion if the battery is replaced incorrectly.**

- Replace only with same or equivalent battery type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer's instructions.

## General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

## Quality and Environmental Management

Kontron aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding Kontron's quality and environmental responsibilities, visit https://www.kontron.com/about-kontron/corporate-responsibility/quality-management.

### Disposal and Recycling

Kontron's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

### WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

**Environmental protection is a high priority with Kontron.**

**Kontron follows the WEEE directive**

**You are encouraged to return our products for proper disposal.**

# Table of Contents



# List of Tables

## List of Figures

# 1/ Introduction

This user guide describes the 3.5"-eIO-GPA board made by Kontron. This board will also be denoted 3.5"-eIO-GPA within this user guide.

Use of this user guide implies a basic knowledge of PC-AT hardware and software. This user guide focuses on describing the 3.5"-eIO-GPA board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in the following chapter before switching on the power.

All configuration and setup of the 3.5"-eIO-GPA is either carried out automatically or manually by the user via the BIOS setup menus of the applicable Kontron's 3.5" single board computer that accommodates the board.

Latest revision of this user guide, datasheet, mechanical drawings (2D and 3D) can be downloaded from Kontron's Web Page.

# 2/ Installation Procedures

## 2.1. Installing the Board

**NOTICE**

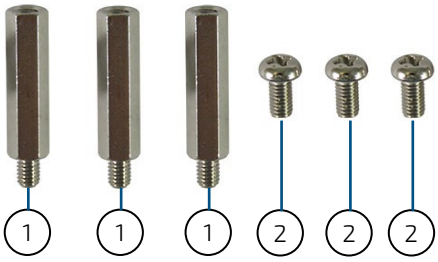
**ESD Sensitive Device!**

**Electrostatic discharge (ESD) can damage equipment and impair electrical circuitry.**

- Wear ESD-protective clothing and shoes
- Wear an ESD-preventive wrist strap attached to a good earth ground
- Check the resistance value of the wrist strap periodically (1 MΩ to 10 MΩ)
- Transport and store the board in its antistatic bag
- Handle the board at an approved ESD workstation
- Handle the board only by the edges

3.5"-eIO-GPA is supplied with three fixing bolts with M3 x 4 mm screw (Figure 1, pos. 1) and three screws (Figure 1, pos. 2).

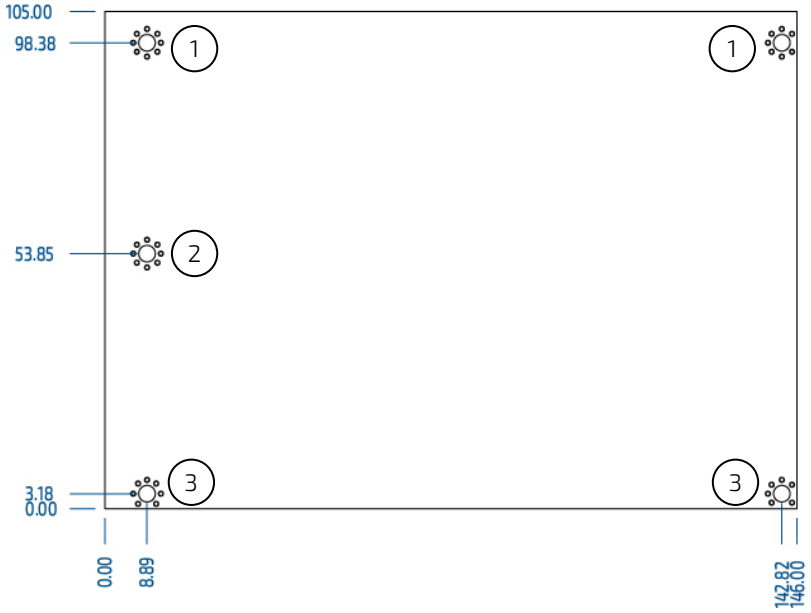
**Figure 1: Accessories of 3.5"-eIO-GPA**




1 Fixing Bolt
2 Screw

To install 3.5"-eIO-GPA, the chassis must have the screw hole pattern shown as Figure 2.

**Figure 2: Screw Hole Pattern for Install 3.5"-eIO-GPA & Applicable 3.5" SBC**



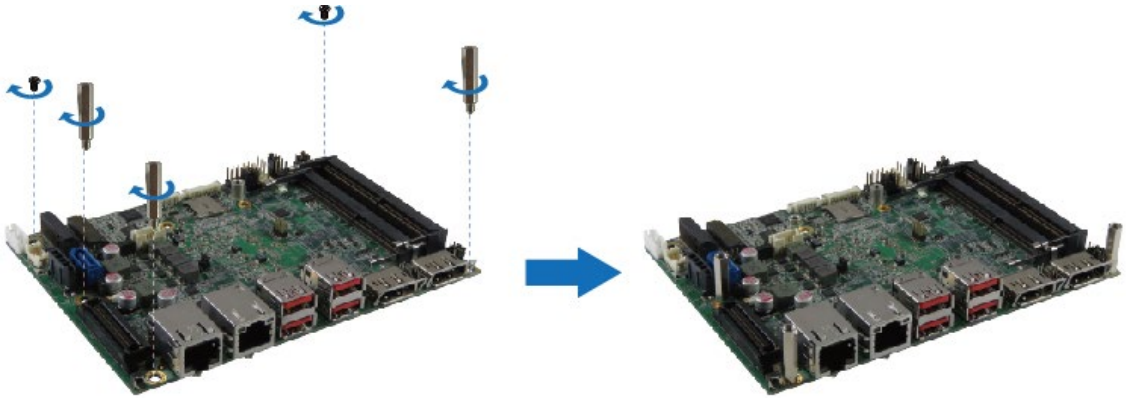

unit: mm

1 Hole for Securing 3.5" Single Board Computer
2 Hole for Securing 3.5"-eIO-GPA
3 Hole for Securing 3.5" Single Board Computer & 3.5"-eIO-GPA

To get the 3.5"-eIO-GPA running follow these steps. Depending on the ordered configuration, the board may be pre-installed on the applicable Kontron's 3.5" single board computer. If the board shipped from KONTRON already has been installed on the 3.5" single board computer, then skip the relevant steps below or uninstall them first for installation into the chassis.

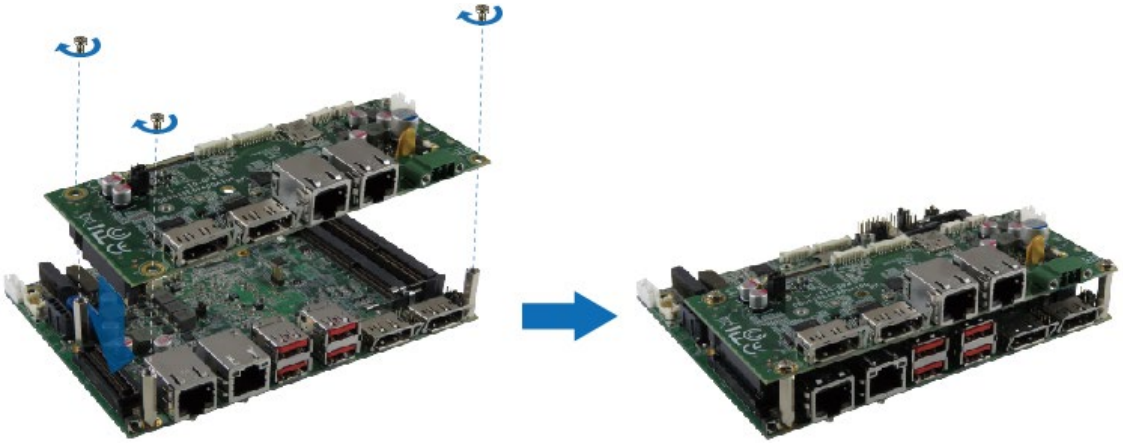
1. Secure the fixing bolts onto the SBC
   Place the applicable single board computer onto the chassis by aligning the screw holes on the single board computer (Figure 2, pos. 1 & 2) with the screw holes on the chassis. Secure the single board computer with the three supplied fixing blots (Figure 1, pos. 1) via three corresponding holes (Figure 2, pos. 2 & 3) and two additional screws via the other holes.

Figure 3: Secure Fixing Bolts Onto SBC



2. Secure the 3.5"-eIO-GPA onto to the SBC
   Insert the 3.5"-eIO-GPA onto the single board computer by connecting the board-to-board connectors of two boards. Concurrently align the screws holes on the 3.5"-eIO-GPA with the screw holes on the fixing bolts (Figure 1, pos. 1) secured on the single board computer. Secure the 3.5"-eIO-GPA with three supplied screws (Figure 1, pos. 2) via the three corresponding holes.

Figure 4: Secure Fixing Bolts Onto SBC



3. **Follow the instructions described for the applicable single board computer to boot up the boards**
   Follow the instructions described for the applicable single board computer to connect a power supply unit, boot up the boards, configure the BIOS and mount the boards in chassis. In case the power supply is input from the power terminal block on the 3.5"-eIO-GPA, DC power voltage should be within the range between 11 V and 32 V.

**NOTICE**

**Make sure to turn off PSU (Power Supply Unit) completely (no mains power connected to the PSU) or leave the Power Connectors unconnected before connecting to the PSU. Otherwise, components (RAM, LAN cards etc.) on the 3.5"-eIO-GPA and the applicable single board computer might get damaged.**

**NOTICE**

**The power supply unit shall comply with the requirements as defined in IEC 62368-1 according Clause 6.2.2 to power source category PS2 "Limited Power Source".**

## 2.2. Chassis Safety Standards

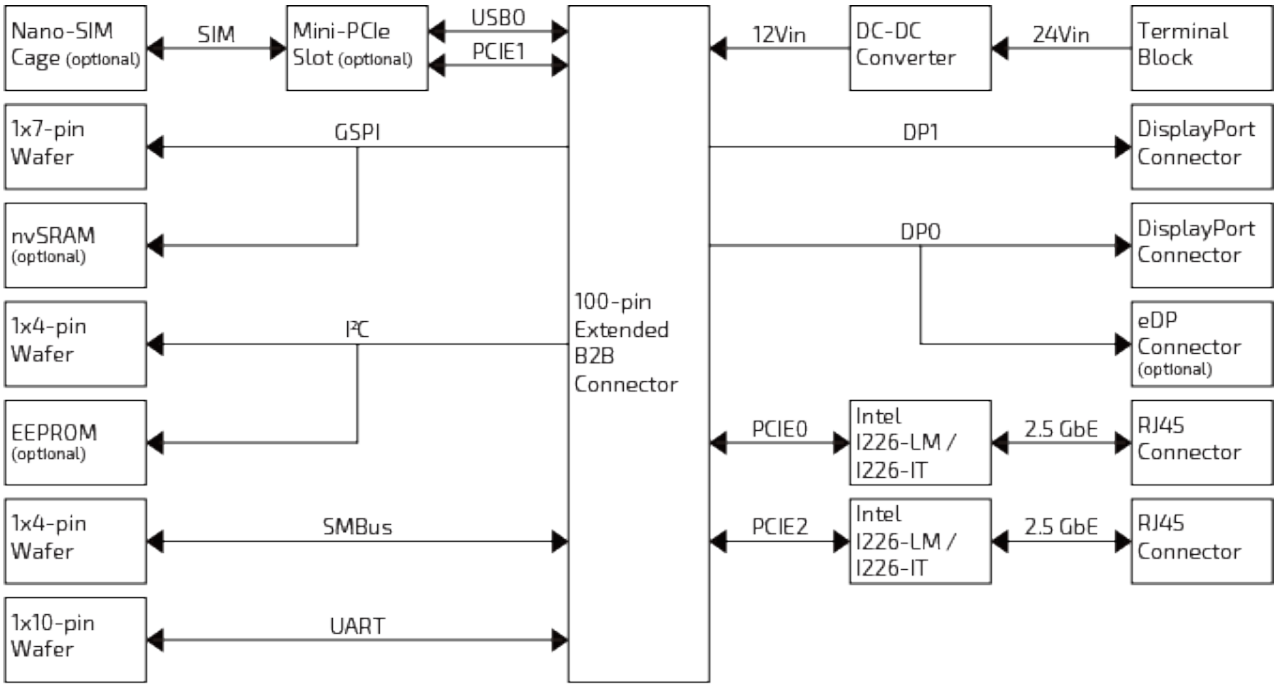
Before installing the 3.5"-eIO-GPA and the applicable single board computer in the chassis, users must evaluate the end product to ensure compliance with the requirements of the IEC60950-1 safety standard:

- The boards must be installed in a suitable mechanical, electrical and fire enclosure.
- The system, in its enclosure, must be evaluated for temperature and airflow considerations.
- The board must be powered by a CSA or UL approved power supply that limits the maximum input current.
- For interfaces having a power pin such as external power or fan, ensure that the connectors and wires are suitably rated. All connections from and to the product shall be with SELV circuits only.
- Wires have suitable rating to withstand the maximum available power.
- The peripheral device enclosure fulfils the IEC60950-1 fire protecting requirements.

# 3/ Specifications

## 3.1. Block Diagram

Figure 5: Block Diagram 3.5"-eIO-GPA



## 3.2. Component Main Data

The table below summarizes the features of the 3.5"-eIO-GPA.

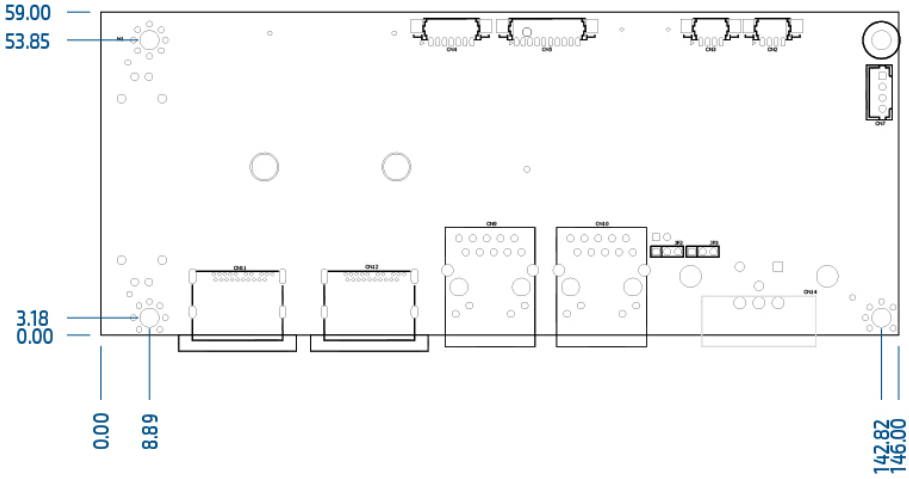
**Table 1: Component Main Data**

| | |
|---|---|
| **Video** | |
| **Display Interface** | ▶ 2x DP (on rear, availability depending on variants)<br>▶ 1x eDP (optional, trade off with 1x DP) |
| Network Connection | |
| **Ethernet** | ▶ 2x 2.5 GbE LAN (RJ45 on rear, Intel® I226-LM / I226-IT) |
| Peripheral Connection | |
| **Serial Port** | ▶ 1x UART (by header, availability depending on variants) |
| **Other I/Os** | ▶ 1x $I^2C$ (by header, availability depending on variants)<br>▶ 1x SMBus (by header, availability depending on variants)<br>▶ 1x GSPI (by header, availability depending on variants) |
| Storage & Expansion | |
| **Memory** | ▶ 1 MByte nvSRAM (optional, trade off with GSPI)<br>▶ 32 KByte EEPROM (optional, trade off with $I^2C$) |
| **mPCIe** | ▶ 1x mPCIe (optional, Full Size, w/ PCIe x1 & USB 2.0, trade off with 2nd 2.5 GbE) |
| **SIM Card Holder** | ▶ 1x SIM Card Holder (optional, Nano size, Push-Push type, connected to mPCIe) |
| Power | |
| **Input Voltage** | ▶ DC 11 V ~ 32 V (w/ reserve polarity protection, DC input from terminal block)<br>▶ DC 12 V / 5 VSB / 3.3 VSB (DC input from Board-to-board connector) |
| **Connector** | ▶ 1x3-pin 3.5 mm pitch terminal block (availability depending on variants)<br>▶ Board-to-board Connector |
| Mechanical | |
| **Dimension (L x W)** | ▶ 146 mm x 59 mm / 5.75" x 2.32" |
| **Connection** | ▶ 100-pin extended board-to-board connector |
| Application | |
| **Supported Baseboard** | ▶ Kontron 3.5"-SBC with 100-pin extended board-to-board connector |

## 3.3. Dimensions

The dimensions of the 3.5"-eIO-GPA are 146 mm x 59 mm.

**Figure 6: Board Dimensions**




unit: mm

## 3.4. Environmental Conditions

The 3.5"-eIO-GPA is compliant with the following environmental conditions. It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within the allowed temperature range.

**Table 2: Environmental Conditions**

| | |
|---|---|
| **Operating Temperature** | ▶ 0 °C ~ 60 °C / 32 °F ~ 140 °F (Standard)<br>▶ -40 °C ~ 85 °C / -40 °F ~ 185 °F (Extreme) |
| **Storage Temperature** | ▶ -20 °C ~ 80 °C / -4 °F ~ 176 °F (Standard)<br>▶ -55 °C ~ 85 °C / -67 °F ~ 185 °F (Extreme) |
| **Humidity** | ▶ 0 % ~ 95 % |

## 3.5. Power Supply Voltage

The 3.5"-eIO-GPA is powered either by the DC input delivered from the single board comouter via the board-to-board connector or by the input power supply delivered from a power supply unit via the 1x3-pin 3.5 mm pitch terminal block located on rear I/O panel, which will be further delivered via the board-to-board connector to power the single board computer. In case of the latter, the input power supply must monitor the supply voltage and shut down if the supply is out of range – refer to the actual power supply specification, in order to ensure safe operation of the 3.5"-eIO-GPA and the single board computer. Please note, in order to keep the power consumption to a minimal level, boards do not implement a guaranteed minimum load. The input power supply delivered via the terminal block to the 3.5"-eIO-GPA must be within the range between DC 11 V and DC 32 V.

**NOTICE**

**Hot Plugging power supply is not supported. Hot plugging might damage the board.**

The requirements to the supply voltages are as follows:

**Table 3: Supply Voltages**

| Supply | Min. | Max. | Note |
|---|---|---|---|
| 11 V ~ 32 V | 10.45 V | 33.6 V | Should be ±5 % tolerance |

# 4/ Connector Locations

## 4.1. Top Side

Figure 7: Top Side

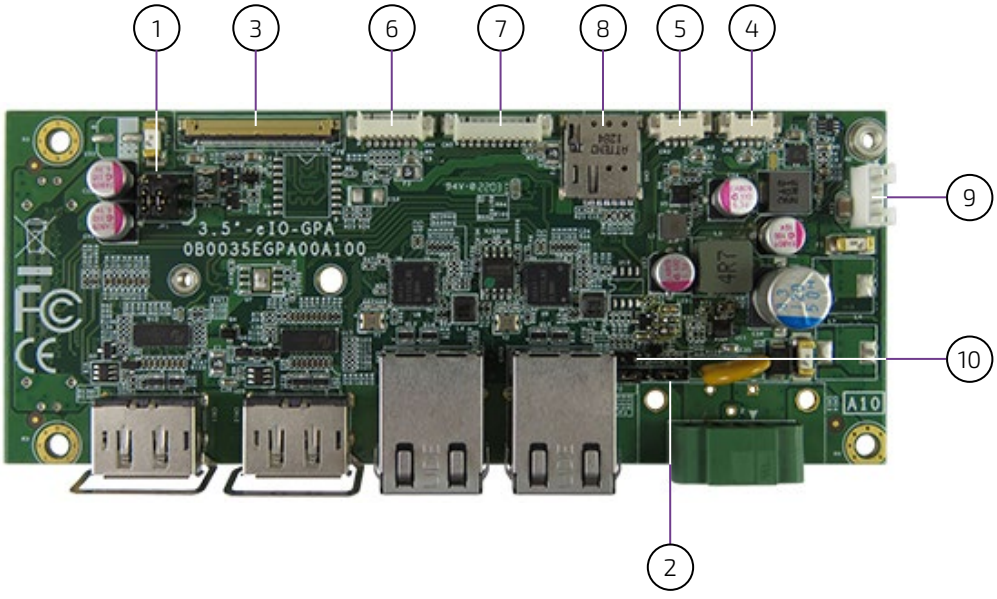



Table 4: Jumper List

| Item | Designation | Description | See Chapter |
|---|---|---|---|
| 1 | JP1 | eDP Backlight & Panel Power Selection (optional) | - |
| 2 | JP3 | Power Mode Selection | 7.7.1 |

Table 5: Top Side Internal Connector Pin Assignment

| Item | Designation | Description | See Chapter |
|---|---|---|---|
| 3 | CN1 | eDP Panel Connector (optional) | - |
| 4 | CN2 | SMBus Wafer (availability depending on variants) | 7.1 |
| 5 | CN3 | $I^2C$ Wafer (availability depending on variants) | 7.2 |
| 6 | CN4 | GSPI Wafer (availability depending on variants) | 7.3 |
| 7 | CN5 | UART Wafer (availability depending on variants) | 7.4 |
| 8 | CN6 | Nano SIM Card Holder for MPCIE1 (optional) | - |
| 9 | CN7 | Power Output Wafer | 7.5 |
| 10 | CN8 | Activity Indicator Header for MPCIE1 (optional) | - |

## 4.2. Rear Side

**Figure 8: Rear Side**

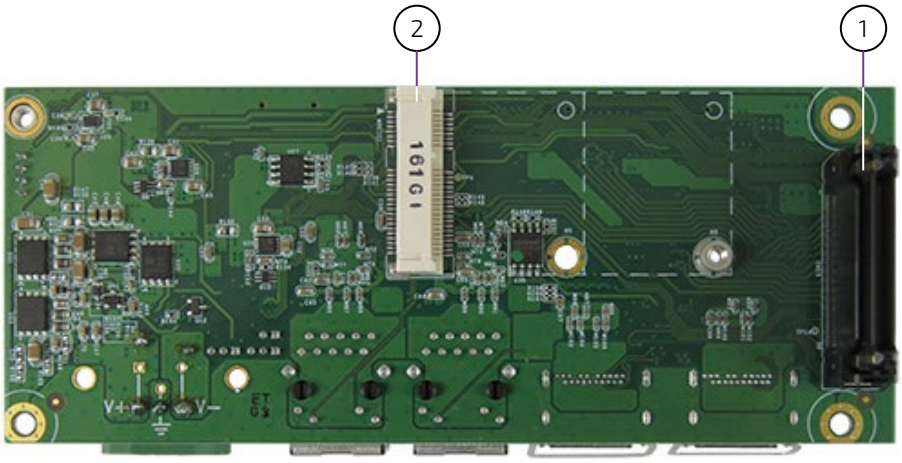



**Table 6: Rear Side Internal Connector Pin Assignment**

| Item | Designation | Description | See Chapter |
|---|---|---|---|
| 1 | CN15 | B2B Connector | 7.6 |
| 2 | MPCIE1 | Mini-PCI Express Socket (optional) | - |

## 4.3. Connector Panel Side

Figure 9: Connector Panel Side

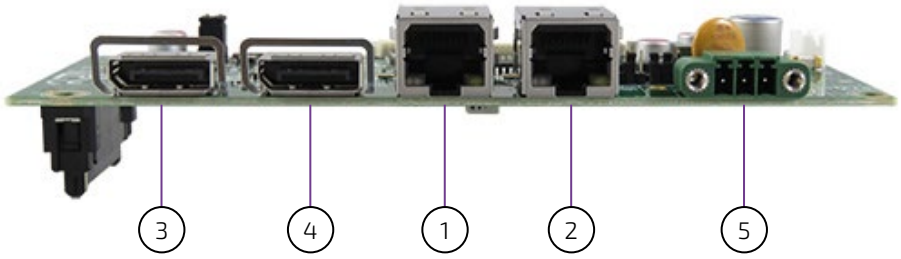



Table 7: Connector Panel Side Connector List

| Item | Designation | Description | See Chapter |
|---|---|---|---|
| 1 | CN9 | 2.5 GbE LAN1 RJ45 Connector | 6.3 |
| 2 | CN10 | 2.5 GbE LAN2 RJ45 Connector | 6.3 |
| 3 | CN11 | DP Port 1 Connector (availability depending on variants) | 6.2 |
| 4 | CN12 | DP Port 2 Connector (availability depending on variants) | 6.2 |
| 5 | CN14 | 11 V ~ 32 V Power Input Connector (availability depending on variants) | 6.1 |

# 5/ Connector Definitions

The following defined terms are used within this user guide to give more information concerning the pin assignment and to describe the connector's signals.

| Defined Term | Description |
|---|---|
| **Pin** | Shows the pin numbers in the connector |
| **Signal** | The abbreviated name of the signal at the current pin<br>The notation "XX#" states that the signal "XX" is active low |
| **Note** | Special remarks concerning the signal |
| **Designation** | Type and number of item described |
| **See Chapter** | Number of the chapter within this user guide containing a detailed description |

The abbreviation TBD is used for specifications that are not available yet or which are not sufficiently specified by the component vendors.

# 6/ I/O-Area Connectors

## 6.1. Power Input Connector (CN14)

Power input connector can provide the board with the DC power within the range between 11 V and 32 V. It is available for partial variants.

**NOTICE**

**Hot plugging any of the power connector is not allowed.**

**Hot plugging might damage the board. In other words, turn off main supply etc. to make sure all the power lines are turned off when connecting to the motherboard.**

Figure 10: Power Input Connector CN14

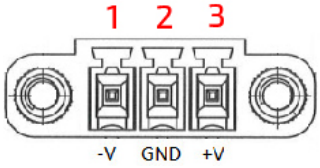



Table 8: Pin Assignment Power Input Connector CN14

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | +Vin | Positive power input voltage (DC 11 V ~ 32 V) | |
| 2 | GND | Earth Ground | |
| 3 | -Vin | Negative power input voltage (DC 0 V) | |
| **Connector Type** | | | |
| B2W, 1x3-pin, 3.5 mm pitch | | | |

## 6.2. DP Connector (CN11 & CN12)

The DP (DisplayPort) connectors are based on standard DP female port. They are available for partial variants.

**Figure 11: DP Connector CN11, CN12**

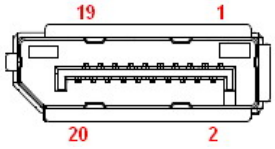



**Table 9: Pin Assignment DP Connector CN11, CN12**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | ML_Lane0p | DisplayPort Lane 0 transmitter differential pair (+) | |
| 2 | GND | Ground | |
| 3 | ML_Lane0n | DisplayPort Lane 0 transmitter differential pair (-) | |
| 4 | ML_Lane1p | DisplayPort Lane 1 transmitter differential pair (+) | |
| 5 | GND | Ground | |
| 6 | ML_Lane1n | DisplayPort Lane 1 transmitter differential pair (-) | |
| 7 | ML_Lane2p | DisplayPort Lane 2 transmitter differential pair (+) | |
| 8 | GND | Ground | |
| 9 | ML_Lane2n | DisplayPort Lane 2 transmitter differential pair (-) | |
| 10 | ML_Lane3p | DisplayPort Lane 3 transmitter differential pair (+) | |
| 11 | GND | Ground | |
| 12 | ML_Lane3n | DisplayPort Lane 3 transmitter differential pair (-) | |
| 13 | Config1 | Connected to ground, either directly or through a pulldown device | |
| 14 | Config2 | Connected to ground, either directly or through a pulldown device | |
| 15 | AUX_CHp | DisplayPort Auxiliary channel differential pair (+) | |
| 16 | GND | Ground | |
| 17 | AUX_CHn | DisplayPort Auxiliary channel differential pair (-) | |
| 18 | Hot_Plug | DisplayPort hot plug detect | |
| 19 | GND | Ground | |
| 20 | DP_PWR | Power for connector | |

## 6.3. Ethernet Connectors (CN9 & CN10)

The 3.5"-eIO-GPA supports two channels of 10/100/1000/2500 Mbit Ethernet, which are based Intel® I226-LM/ I226-IT controllers.

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100 MByte and Category 5E, 6 or 6E with 1 Gbit/2.5Gbit LAN networks.

The signals for the Ethernet ports are as follows:

**Figure 12: Ethernet Connector CN9, CN10**

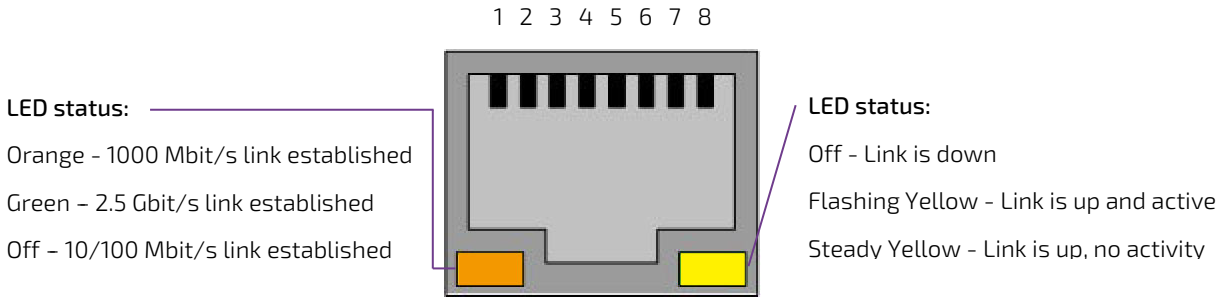



**Table 10: Pin Assignment Ethernet Connectors CN9, CN10**

| Pin | Signal | Note |
|---|---|---|
| 1 | TX1+ | |
| 2 | TX1- | |
| 3 | TX2+ | |
| 4 | TX3+ | |
| 5 | TX3- | |
| 6 | TX2- | |
| 7 | TX4+ | |
| 8 | TX4- | |

**Signal Description**

| Signal | Description |
|---|---|
| **TX1+ / TX1-** | In MDI mode, this is the first pair in 2.5GBase-T and 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. |
| **TX2+ / TX2-** | In MDI mode, this is the second pair in 2.5GBase-T and 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. |
| **TX3+ / TX3-** | In MDI mode, this is the third pair in 2.5GBase-T and 1000Base-T, i.e. the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair. |
| **TX4+ / TX4-** | In MDI mode, this is the fourth pair in 2.5GBase-T and 1000Base-T, i.e. the BI_DD+/- pair.In MDI crossover mode, this pair acts as the BI_DC+/- pair. |

'MDI' – media dependent Interface

# 7/ Internal Connectors

## 7.1. SMBus Wafer (CN2)

The 1x4-pin 1.25 mm pitch SMBus wafer (CN2) is used for system management communications. It is available for partial variants.

**Figure 13: SMBus Wafer CN2**

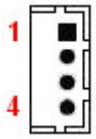



**Table 11: Pin Assignment CN2**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | SMB_CLK | SMBus clock | |
| 2 | SMB_DATA | SMBus data | |
| 3 | GND | Power supply ground signal | |
| 4 | +3.3V | + 3.3 V power supply | |
| **Connector Type** | | | |
| B2W, 1x4-pin, 1.25 mm pitch | | | |

## 7.2. I²C Wafer (CN3)

The 1x4-pin 1.25 mm pitch I²C wafer (CN3) is used for sensor or other control function. It is available for partial variants.

**Figure 14: SMBus Wafer CN3**

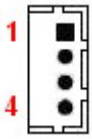



**Table 12: Pin Assignment CN3**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | I2C_CLK | I²C clock | |
| 2 | I2C_DATA | I²C data | |
| 3 | GND | Power supply ground signal | |
| 4 | +3.3V | + 3.3 V power supply | |
| **Connector Type** | | | |
| B2W, 1x4-pin, 1.25 mm pitch | | | |

## 7.3. GSPI Wafer (CN4)

The 1x7-pin 1.25 mm pitch GSPI wafer (CN4) is used for synchronous serial communications. It is available for partial variants.

**Figure 15: GSPI Wafer CN4**

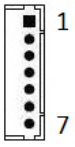



**Table 13: Pin Assignment CN4**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | GSPI_CLK | Generic Serial Peripheral Interface clock | |
| 2 | GSPI_MOSI | Generic Serial Peripheral Interface date transmission from master to slave (master output, slave input) | |
| 3 | GSPI_MISO | Generic Serial Peripheral Interface data transmission from slave to master (master input, slave output) | |
| 4 | GSPI_CS0# | Generic Serial Peripheral Interface chip select bit 0 | |
| 5 | GSPI_CS1# | Generic Serial Peripheral Interface chip select bit 1 | |
| 6 | GND | Power supply ground signal | |
| 7 | +3.3V | + 3.3 V power supply | |
| **Connector Type** | | | |
| B2W, 1x7-pin, 1.25 mm pitch | | | |

## 7.4. UART Wafer (CN5)

The 1x10-pin 1.25 mm pitch UART wafer CN5 provides asynchronous serial communications. It is available for partial variants.

Figure 16: UART Wafer CN5

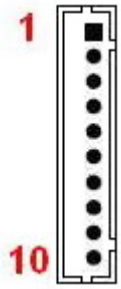



Table 14: Pin Assignment CN5

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | - | | |
| 2 | - | | |
| 3 | UART_RXD | Universal Asynchronous Receiver / Transmitter received data | |
| 4 | UART_RTS# | Universal Asynchronous Receiver / Transmitter request to send | |
| 5 | UART_TXD | Universal Asynchronous Receiver / Transmitter transmitted data | |
| 6 | UART_CTS# | Universal Asynchronous Receiver / Transmitter clear to send | |
| 7 | - | | |
| 8 | - | | |
| 9 | GND | Power supply ground signal | |
| 10 | +3.3V | + 3.3 V power supply | |
| **Connector Type** | | | |
| B2W, 1x10-pin, 1.25 mm pitch | | | |

## 7.5. Power Output Wafer (CN7)

The 1x4-pin 2.0 mm pitch power output wafer CN7 provides power supply to other device integrated in the system for possible application expansion. It is available only for the variants with the power input connector (CN14).

**Figure 17: Power Output Wafer CN7**


**Table 15: Pin Assignment CN7**

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | GND | Power supply ground signal | |
| 2 | GND | Power supply ground signal | |
| 3 | +VOUT* | Power supply output | |
| 4 | +VOUT* | Power supply output | |
| **Connector Type** | | | |
| B2W, 1x4-pin, 2.0 mm pitch | | | |

* +Vout comes from +Vin (CN14).

## 7.6. B2B Connector (CN15)

The board-to-board connector provides connection to an applicable Kontron single board computer to deliver signals between the 3.5"-eIO-GPA and the single board computer.

Figure 18: B2B Connector CN15

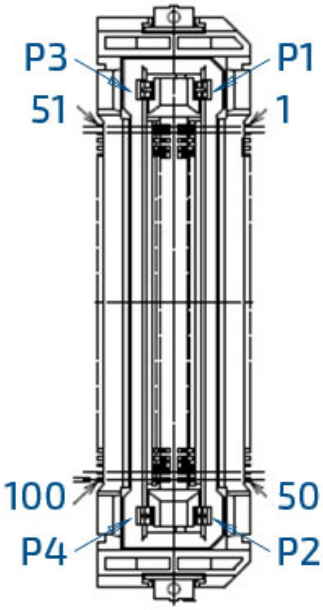



Table 16: Pin Assignment CN15

| Pin | Signal | Description | Note |
|---|---|---|---|
| 1 | +3.3VSB_IN | 3.3 V standby power input | 400 mA max. |
| 2 | +3.3VSB_IN | 3.3 V standby power input | 400 mA max. |
| 3 | +3.3VSB_IN | 3.3 V standby power input | 400 mA max. |
| 4 | +3.3VSB_IN | 3.3 V standby power input | 400 mA max. |
| 5 | +3.3VSB_IN | 3.3 V standby power input | 400 mA max. |
| 6 | GND | Ground | |
| 7 | eDP_DP0_TX0+ | eDP / DP 0 Lane 0 transmitter pair (+) | |
| 8 | eDP_DP0_TX0- | eDP / DP 0 Lane 0 transmitter pair (-) | |
| 9 | GND | Ground | |
| 10 | eDP_DP0_TX1+ | eDP / DP 0 Lane 1 transmitter pair (+) | |
| 11 | eDP_DP0_TX1- | eDP / DP 0 Lane 1 transmitter pair (-) | |
| 12 | GND | Ground | |
| 13 | eDP_DP0_TX2+ | eDP / DP 0 Lane 2 transmitter pair (+) | |
| 14 | eDP_DP0_TX2- | eDP / DP 0 Lane 2 transmitter pair (-) | |
| 15 | GND | Ground | |
| 16 | eDP_DP0_TX3+ | eDP / DP 0 Lane 3 transmitter pair (+) | |
| 17 | eDP_DP0_TX3- | eDP / DP 0 Lane 3 transmitter pair (-) | |
| 18 | GND | Ground | |

| Pin | Signal | Description | Note |
|---|---|---|---|
| 19 | eDP_DP0_AUX+ | eDP / DP 0 Auxiliary channel pair (+) | |
| 20 | eDP_DP0_AUX- | eDP / DP 0 Auxiliary channel pair (-) | |
| 21 | GND | Ground | |
| 22 | PCIE0_CLK_REF+ | PCIe Lane 0 clock reference pair (+) | |
| 23 | PCIE0_CLK_REF- | PCIe Lane 0 clock reference pair (-) | |
| 24 | GND | Ground | |
| 25 | PCIE0_TX+ | PCIe Lane 0 transmitter pair (+) | |
| 26 | PCIE0_TX- | PCIe Lane 0 transmitter pair (-) | |
| 27 | GND | Ground | |
| 28 | PCIE0_RX+ | PCIe Lane 0 receiver pair (+) | |
| 29 | PCIE0_RX- | PCIe Lane 0 receiver pair (-) | |
| 30 | GND | Ground | |
| 31 | PCIE2_TX+ | PCIe Lane 2 receiver pair (+) | |
| 32 | PCIE2_TX- | PCIe Lane 2 receiver pair (-) | |
| 33 | GND | Ground | |
| 34 | PCIE2_RX+ | PCIe Lane 2 receiver pair (+) | |
| 35 | PCIE2_RX- | PCIe Lane 2 receiver pair (-) | |
| 36 | GND | Ground | |
| 37 | USB0_D- | USB 2.0 differential pair (-) | |
| 38 | USB0_D+ | USB 2.0 differential pair (+) | |
| 39 | GND | Ground | |
| 40 | UART_TXD | UART transmitted data | +3.3 V |
| 41 | UART_RXD | UART received data | +3.3 V |
| 42 | UART_CTS# | UART clear to send | +3.3 V |
| 43 | UART_RTS# | UART request to send | +3.3 V |
| 44 | GND | Ground | |
| 45 | eDP_PWM | eDP backlight PWM (Pulse Width Modulation) signal | |
| 46 | eDP_VDDEN | eDP panel power enable signal | |
| 47 | eDP_BKLTEN | eDP backlight enable signal | |
| 48 | eDP_DO0_HPD | eDP / DP 0 hot plug detect | |
| 49 | eDP_DP0_EN# | eDP / DP 0 enable | |
| 50 | NC | Not connected | |
| 51 | GSPI_CLK | Generic SPI clock | +3.3 V |
| 52 | GSPI_MOSI | Generic SPI master output / slave input | +3.3 V |
| 53 | GSPI_MISO | Generic SPI master input / slave output | +3.3 V |
| 54 | GSPI_CS0# | Generic SPI chip select bit 0 | +3.3 V |
| 55 | GSPI_CS1# | Generic SPI chip select bit 1 | +3.3 V |
| 56 | GND | Ground | |
| 57 | DP1_TX0+ | DP 1 Lane 0 transmitter pair (+) | |
| 58 | DP1_TX0- | DP 1 Lane 0 transmitter pair (-) | |
| 59 | GND | Ground | |
| 60 | DP1_TX1+ | DP 1 Lane 1 transmitter pair (+) | |

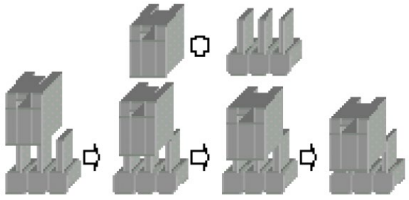
| Pin | Signal | Description | Note |
|---|---|---|---|
| 61 | DP1_TX1- | DP 1 Lane 1 transmitter pair (-) | |
| 62 | GND | Ground | |
| 63 | DP1_TX2+ | DP 1 Lane 2 transmitter pair (+) | |
| 64 | DP1_TX2- | DP 1 Lane 2 transmitter pair (-) | |
| 65 | GND | Ground | |
| 66 | DP1_TX3+ | DP 1 Lane 3 transmitter pair (+) | |
| 67 | DP1_TX3- | DP 1 Lane 3 transmitter pair (-) | |
| 68 | GND | Ground | |
| 69 | DP1_AUX+ | DP 1 Auxiliary channel pair (+) | |
| 70 | DP1_AUX- | DP 1 Auxiliary channel pair (-) | |
| 71 | GND | Ground | |
| 72 | PCIE1_CLK_REF+ | PCIe Lane 1 clock reference pair (+) | |
| 73 | PCIE1_CLK_REF- | PCIe Lane 1 clock reference pair (-) | |
| 74 | GND | Ground | |
| 75 | PCIE1_TX+ | PCIe Lane 1 transmitter pair (+) | |
| 76 | PCIE1_TX- | PCIe Lane 1 transmitter pair (-) | |
| 77 | GND | Ground | |
| 78 | PCIE1_RX+ | PCIe Lane 1 receiver pair (+) | |
| 79 | PCIE1_RX- | PCIe Lane 1 receiver pair (-) | |
| 80 | GND | Ground | |
| 81 | NC | Not connected | |
| 82 | NC | Not connected | |
| 83 | GND | Ground | |
| 84 | NC | Not connected | |
| 85 | NC | Not connected | |
| 86 | GND | Ground | |
| 87 | NC | Not connected | |
| 88 | NC | Not connected | |
| 89 | GND | Ground | |
| 90 | I2C_CLK | I2C clock | +3.3 V |
| 91 | I2C_DATA | I2C data | +3.3 V |
| 92 | SMB_CLK | SM bus clock | +3.3 V |
| 93 | SMB_DATA | SM bus data | +3.3 V |
| 94 | GND | Ground | |
| 95 | NC | Not connected | |
| 96 | PCIE_WAKE# | PCIe wake | |
| 97 | PCIE_PLTRST# | PCIe platform reset | |
| 98 | DP1_HPD | DP 1 hot plug detect | |
| 99 | DP1_EN# | DP 1 enable | |
| 100 | PS_ON# | Power supply enable / disable | |
| P1 | +5VSB_IN | 5 V standby power input | 2 A max. |
| P2 | +12V_IN / +12V_OUT | 12 V power input / 12 V power output | 3 A max. |

| Pin | Signal | Description | Note |
|---|---|---|---|
| P3 | +12V_IN / +12V_OUT | 12 V power input / 12 V power output | 3 A max. |
| P4 | +12V_IN / +12V_OUT | 12 V power input / 12 V power output | 3 A max. |
| **Connector Type** | | | |
| B2B, 2x50-pin, 0.5 mm pitch | | | |

## 7.7. Switches and Jumpers

The product has several jumpers which must be properly configured to ensure correct operation.

**Figure 19: Jumper Connector**



For a three-pin jumper (see Figure 19), the jumper setting is designated "1-2" when the jumper connects pins 1 and 2. The jumper setting is designated "2-3" when pins 2 and 3 are connected and so on. You will see that one of the lines surrounding a jumper pin is thick, which indicates pin No.1.

To move a jumper from one position to another, use needle-nose pliers or tweezers to pull the pin cap off the pins and move it to the desired position.

### 7.7.1. Power Mode Selection (JP3)

The 2.0 mm pitch "Power Mode Selection" jumper (JP3) can be used to specify whether to enable the +12 V controller in order to determine the system is powered by the power supply from the power input connector (CN14) on the 3.5"-eIO-GPA or from the single board computer. It is available only for the variants with the power input connector (CN14).

**Figure 20: Power Mode Selection JP3**

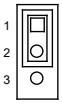



**Table 17: Pin Assignment JP3**

| Jumper 1 Position | | Description |
|---|---|---|
| Pin 1-2 | Pin 2-3 | |
| X | - | +12V Controller ENABLE (the system is powered by the power supply from CN14) |
| - | X | +12V Controller DISABLE (the system is powered by the power supply from SBC) |

"X" = Jumper set (short) and "-" = jumper not set (open)

# Appendix A: List of Acronyms

**The following table does not contain the complete acronyms used in signal names, signal type definitions or similar. A description of the signals is included in the I/O Connector and Internal connector chapters within this user guide.**

Table 18: List of Acronyms

| | |
|---|---|
| 2D | Two-Dimensional |
| 3D | Three-Dimensional |
| AT | Advanced Technology |
| ATX | Advanced Technology eXtended |
| BGA | Ball Grid Array |
| BIOS | Basic Input / Output System |
| BSP | Board Support Package |
| CMOS | Complementary Metal Oxide Semiconductor |
| CPU | Central Processing Unit |
| DC | Direct Current |
| DDC | Display Data Channel |
| DIO | Digital Input / Output |
| DP | DisplayPort |
| ECC | Error-Correcting Code |
| EEE | Electrical and Electronic Equipment |
| EOS | Electrical OverStress |
| ESD | ElectroStatic Discharge |
| GbE | Gigabit Ethernet |
| HDD | Hard Disk Drive |
| HDMI | High Definition Multimedia Interface |
| LAN | Local Area Network |
| LED | Light Emitting Device |
| LVDS | Low-Voltage Differential Signaling |
| ME F/W | Management Engine Firmware |
| mPCIe | mini Peripheral Component Interconnect express |
| NGFF | Next Generation Form Factor |
| PC-AT | Personal Computer - Advanced Technology |
| PCB | Printed Circuit Board |
| PSU | Power Supply Unit |
| PVC | PolyViny Chloride |
| PWM | Pulse Width Modulation |
| RAM | Random Access Memory |
| ROM | Read-Only Memory |
| RTC | Real-Time Clock |
| SATA | Serial Advanced Technology Attachment |
| SD | Secure Digital memory card |
| SDP | Serial Download Protocol |
| SELV | Safety Extra-Low Voltage |
| SIM | Subscriber Identity Module |
| SMBus | System Management Bus |
| SoC | System on Chip |
| SO-DIMM | Small Outline Dual In-line Memory Module |
| SPD | Serial Presence Detect |
| SPI | Serial Peripheral Interface |
| TDP | Thermal Design Power |
| TPM | Trusted Platform Module |
| UEFI | Unified Extensible Firmware Interface |
| USB | Universal Serial Bus |
| UTP | Update Transfer Protocol |
| VGA | Video Graphics Array |
| WDT | WatchDog Timer |
| WEEE | Waste Electrical and Electronic Equipment |
| | |
| | |
| | |
| | |
| | |

## About Kontron

Kontron is a global leader in IoT / Embedded Computing Technology (ECT) and offers individual solutions in the areas of Internet of Things (IoT) and Industry 4.0 through a combined portfolio of hardware, software and services. With its standard and customized products based on highly reliable state-of-the-art technologies, Kontron provides secure and innovative applications for a wide variety of industries. As a result, customers benefit from accelerated time-to-market, lower total cost of ownership, extended product lifecycles and the best fully integrated applications.

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