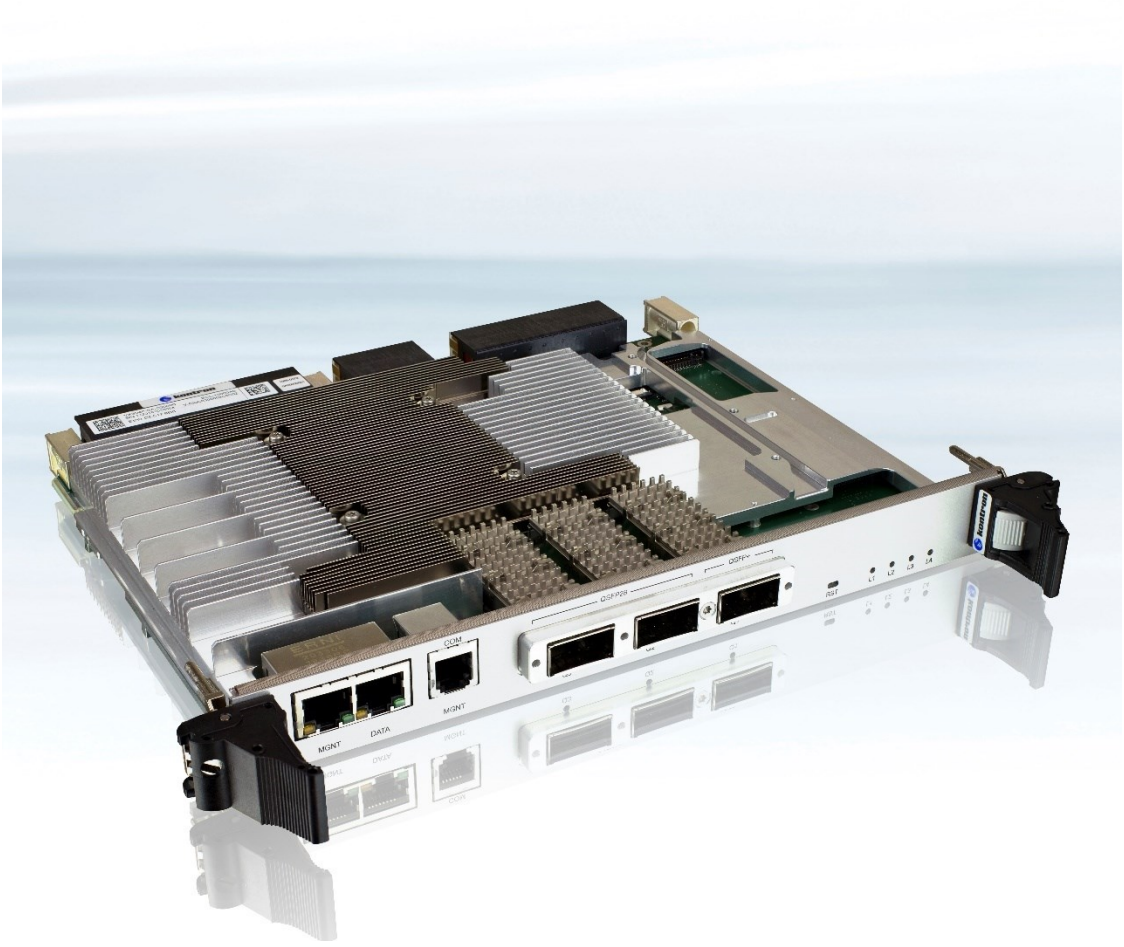
USER GUIDE



VX6940

6U Open VPX 10/40/100 GbE Managed Ethernet Switch

1.5 - February 2025

POSSIBILITIES START HERE kontron S&T Group

VX6940 – User Guide

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1.1	Update. Minor wording changes. Fixed CTL+F search.	August 2020
1.2	- Chap. 2.4: Added RTM part numbers in Table 4. Added RC code in Table 5. - Chap. 2.6: SDCard holder no longer present on board. - Chap. 3.8 updated. - Chap. "3.9 Quick Start" added. - Chap. 5.3.4: Typo fixed in Table 31 TSCE0_RD0+ corresponds to DPfp10-R0+, not to DPfp09-R0+ - Chap. "8 MPO RTM" added. - Chap. "9 SFP RTM" added. - Chap. "10 Software" added. - Chap. "11 Conduction-Cooled VX6940-RC" added. - Appendix A "Detailed Ethernet Ports Mappings" added. Tables moved from 2.2.1.	July 2021
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1.5	- Fixed search command issue in pdf document. - In RC Class variants, Ethernet ETH0 and serial COM management ports along with Ethernet ETH1 data port are available only on rear VPX. Modified chapters: . Chap. 2.3 - Block Diagram, Figures 9 (P6 optical link suppressed) & 10 (Front/rear configurations description updated). . Chap. 2.4 - Ordering Information, Table 3. . Chap. 2.5 - IO Interfaces. . Chap. 2.7 - Technical Specification, Table 8. . Chap. 5.1 - Front Panel Connectors. . Chap. 5.3.4 - VPX P3 ConnectorTable 32. . Chap. 5.3.7 - VPX P6 Connector, Table 36. . Chap. 11.2 - VX6940-RC Order Codes, Table 81. . Chap. 11.5 - VX6940-RC Peripheral Connectivity and Daughter Cards. . Chap. 10.5.6 and 10.5.7 – Configuration of ETH0 and ETH1	February 2025

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Symbols

The following symbols may be used in this user guide

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
NOTICE	NOTICE indicates a property damage message.
	Electric Shock! This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

ESD Sensitive Device!

This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.

HOT Surface!

Do NOT touch! Allow to cool before servicing.

Laser!

This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.

This symbol indicates general information about the product and the user guide.

This symbol also indicates detail information about the specific product configuration.

This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!

Before installing a non-hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

General Instructions on Usage

In order to maintain Kontron's product warranty and CE compliance, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty and CE compliance.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide. Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Environmental protection is a high priority with Kontron.

Kontron follows the WEEE directive

You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

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1. Document Overview

1.1 Objective

This guide provides general information, hardware instructions, operating instructions and functional description of the VX6940 board. The onboard programming, onboard firmware and other software (e.g. drivers and BSPs) are described in detail in separate guides (refer to section 1.6"Related Publications").

This hardware technical documentation reflects the most recent version of the product. The "Hardware Release Notes" (refer to section 1.6 "Related Publications") keeps track of the successive product evolutions.

Changes from previous version of the document are identified by a vertical bar in the margin.

1.2 Audience

The intended audience for this guide ranges from the unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, system, cabling, grounding and communications.

1.3 Scope

This guide describes the SA (air-cooled commercial), WA (extended air-cooled commercial), RA (rugged air-cooled) and RC (rugged conduction-cooled) variants of the VX6940.

1.4 Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with a brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- Chapter 1 - User Guide Overview (this chapter)
- Chapter 2 - Board Overview
- Chapter 3 - Installation
- Chapter 4 - Additional Board Features
- Chapter 5 - Physical IOs
- Chapter 6 - Electrical Specifications
- Chapter 7 - Power and Thermal Management
- Chapter 8 - Power and Thermal Management
- Chapter 9 - SFP Rear Transition ModulePower and Thermal Management
- Chapter 10 - SoftwarePower and Thermal Management
- Chapter 11 - Conduction-Cooled VX6940-RCPower and Thermal Management

1.5 Terminology, Definitions and Abbreviations

- Environment classes terminology:

The environment class is encoded in a two-digit suffix:

- VX6940-SA: commercial air-cooled.
- VX6940-WA: extended temperature air-cooled.
- VX6940-RA: ruggedized air-cooled.
- VX6940-RC: ruggedized conduction-cooled.

- Terms and acronyms

Term or Acronym	Definition
API	Application Programming Interface
BMC	Base Management Controller
CLI	Command-Line Interface
DHCP	Dynamic Host Configuration Protocol
FPGA	Field-Programmable Gate Array
FRU	Field Replaceable Unit
Gbps	Gigabit per second
Hub	Switch with Shelf Management Controller
IFC	Integrated Flash Controller
IOL	IPMI-Over-LAN
IPMI	Intelligent Platform Management Interface
GND	Electrical reference or logic ground or digital ground
GNDC	Chassis ground or mechanical ground or safety ground
KCS	Keyboard Controller Style interface. A communication interface between host CPU and IPMI controller
LPC	Low Pin Count Interface.
MAC	Medium Access Control
MDC/MDIO	MDC/MDIO interface. An alternate term for MIIM.
MIB	Management Information Base
MII	Media Independant Interface
MIIM	MII Management Interface. An alternate term for MDC/MDIO interface.
MSP node	Modular Server Processing Node
MTBF	Mean Time Between Failure
NC	Not Connected.
NTP	Network Time Protocol
PCB	Printed Circuit Board
PCIe	PCI-Express
QSFP	Quad Small Form-factor Pluggable
RCW	Reset Configuration Words (QorIQ T1042 configuration bits stored in SPI Flash)
RTC	Real Time Clock
SEL	System Event Log
ShMC	Shelf Management Controller (on VX6940, Aspeed AST2520 micro controller)
SM	System Monitor Web Interface
SMBUS	System Management Bus
SNMP	Simple Network Management Protocol

Term or Acronym	Definition
SODIMM	Small Outline Dual In-line Memory Module (on VX6940, UC DDR3L memory module)
SOL	IPMI based Serial-Over-LAN
SSH	Secure Shell
STP	Spanning Tree Protocol
TBD	To Be Defined
TIPC	Transparent Inter-process Communication
TPM	Trusted Platform Module
UC	Unit Computer (NXP T1042 QorIQ)
VLAN	Virtual Local Area Network

1.6 Related Publications

The following publications contain information relating to this product.

Table 1: Related Publications

Standards	**Publication**
ANSI/VITA 46.0	VPX Baseline Standard - 2019
ANSI/VITA 47-2005 (R2007)	Environments, Design and Construction, Safety, and Quality for Plug-In Units Standard ANSI/VITA 47-2005/2007
VITA 65-2010 (R2012)	OpenVPX™ System Specification - ANSI/VITA - 2012
VITA65.1-2017	VITA 65.1 OpenVPX Standard - Profiles Table
IEC62380	Reliability data handbook – Universal model for reliability prediction of electronics components, PCBs and equipment - IEC IEC62380-2004
IEEE 802.3	- Clause 40 and other clauses related to 1000BASE-T: IEEE 802.3 Physical Layer specification for a 1000 Mb/s CSMA/CD LAN using four pairs of Category 5 balanced copper cabling. - Clause 40 and other clauses related to 1000BASE-T: IEEE 802.3 Physical Layer specification for a 1000 Mb/s CSMA/CD LAN using four pairs of Category 5 balanced copper cabling. - Clause 70 and other clauses related to 1000BASE-KX: IEEE 802.3 Physical Layer specification for 1 Gb/s using 1000BASE-X encoding over an electrical backplane. - Clause 72 and other clauses related to 10GBASE-KR: IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-R encoding over an electrical backplane. - Clauses 82 & 84: 40GBASE-KR4 - Clause 93: 100GBASE-KR4 - Clauses 72 & 85 : training - Clauses 22 & 45: MDC/MDIO
I2C	I2C-bus Specification and User Manual - UM10204 - Rev 6 - 2014
MIL-HDBK-217	Military Handbook - Reliability Prediction of Electronic Equipment - Department Of Defense MIL-HDBK-217-1991
MIL-STD-810-G	Environmental Engineering Considerations and Laboratory Tests - Department Of Defense MIL-STD-810-G w/ Change 1 - 2014
PCI Express M.2	PCI Express M.2 Specification - PCI SIG-2013
Serial ATA	Serial ATA Revision 3.2 - SATA IO-2013
Trusted Platform Module	TPM Main Specification Level 2 Version 1.2, Revision 116
Hardware	**Publication**
VX6940	VX6940 Hardware Release Notes: D242701
Software	**Publication**
FastPath	VX6940 CLI Reference Manual: D244939
FastPath	Fastpath 8.10 Web Configuration Guide: D271525

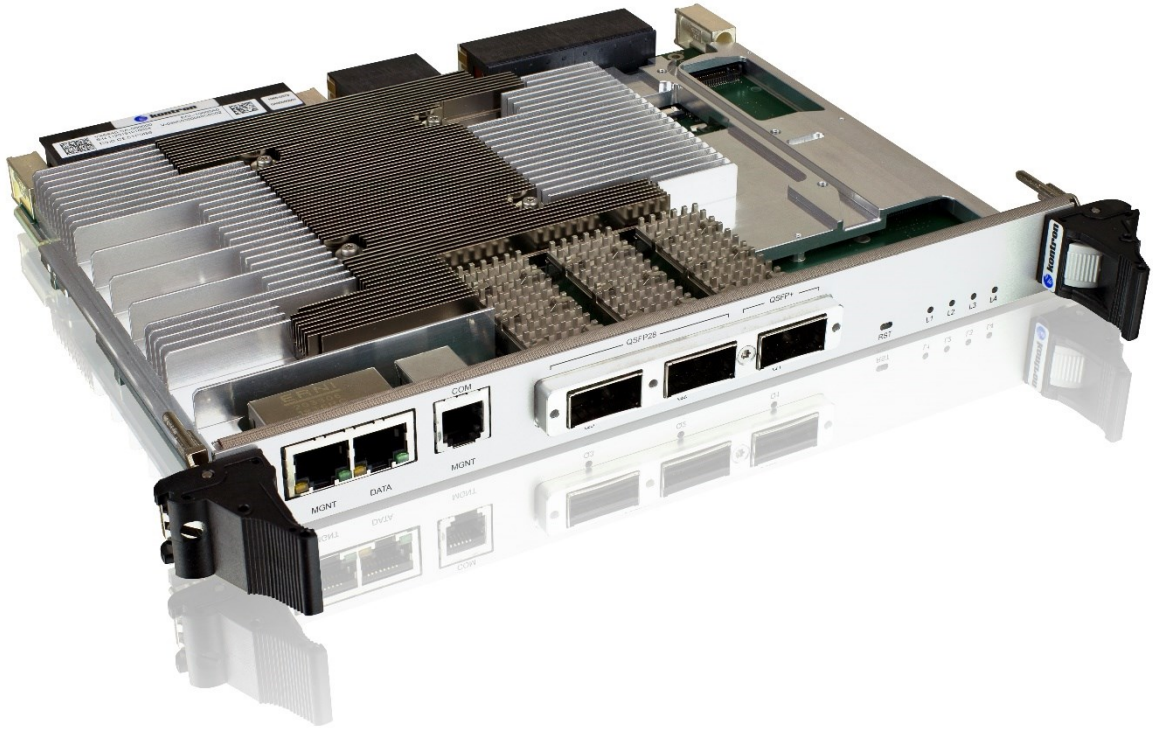
2 Board Overview

2.1 Introduction

The VX6940 is a non-blocking, fully managed, 1/10/40/100 Gigabit Ethernet switch. It is based on the Broadcom® BCM56760 StrataGX Multilayer Ethernet Switch featuring 4x 100G (or 16x 25G) ports along with 12x 40G (or 48x 10G) ports. It implements a quad core QorIQ processor NXP T1042 to run the Broadcom® FASTPATH® networking software and a powerful IPMI shelfmanager. It is ideally suited for the transition from 10G to 25G of embedded Ethernet fabrics requiring outstanding bandwidth.

This high-performance, SWaP-C optimized, 6U switch is compatible with the latest VPX system open architecture specifications (SOSA) and designed for the most demanding applications in harsh environments.

Figure 1: VX6940



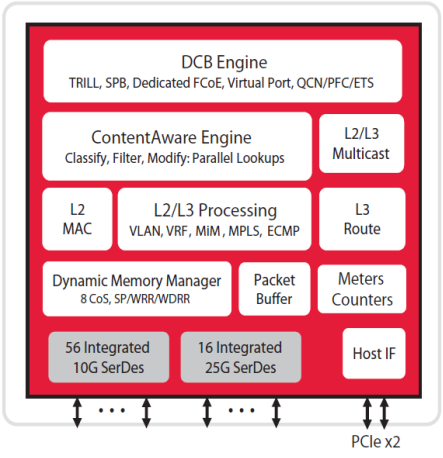
2.2 Main Features

2.2.1 Ethernet Management

- **Ethernet Switch BCM56760**

The VX6940 is structured around the BCM56760 switch which offers native support of 25 GbE links and 100 GbE links, smart hashing, a very large Layer 2 and Layer 3 forwarding capacity supporting numerous multipathing and tunneling technologies.

Figure 2: Ethernet Switch BCM56760 Block Diagram



BCM56760 features:

- Standards-compliant 10GbE/40GbE switch with support for up to 18 ports of 40GbE, 16 ports of 25GbE, and four ports of 100GbE.
- Advanced SmartHash engine for optimal and resilient load distribution across HiGig™, LAG, and ECMP trunk groups.
- Smart-NV technology featuring support for VxLAN, NVGRE overlays, IEEE 802.1Qbg Edge Virtual Bridging, IEEE 802.1BR Bridge Port extension, and per-virtual machine traffic-shaping.
- RIOT for VxLAN and SPB tunnels in a single pass.
- Integrated SmartBuffer supporting lossless performance and high burst absorption using innovative traffic-load. awareness and dynamic allocation schemes.
- ContentAware™ engine for scalable, high-density ingress and egress packet classification.
- Data center bridging support: PFC, QCN, ETS.
- Dedicated FCoE forwarding engine enabling FC-BB-5 and FC-BB-6 deployment models.
- Hardware-based tunneling services including MPLS, VPLS, ISATAP, MAC-in-MAC, TRILL, SPB, and Q-in-Q.
- Energy Efficient Ethernet (EEE) support including customizable, low-power idle (LPI) control policies.
- Integrated 1588v2 processor for Precision Time Protocol and IEEE 802.1AS for timing and synchronization.

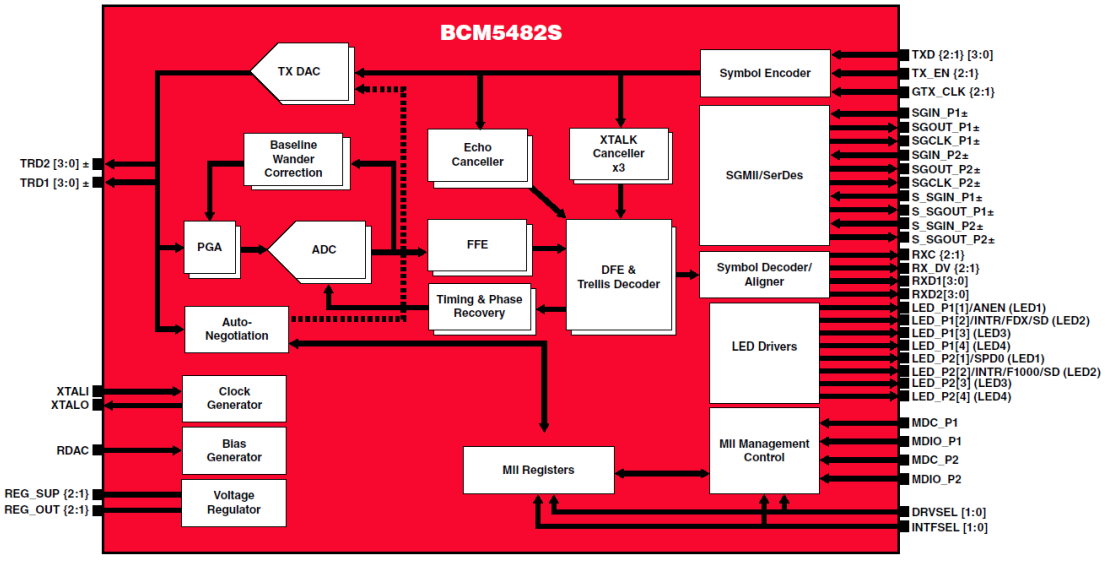
Ethernet Port Mapping

FASTPATH port mappings are described in section 10.4.
A detalied hardware description of the Ethernet Ports allocation may be found in Appendix A.

Dual PHY BCM5482S

The dual Gigabit Ethernet PHY BCM5482S consists of two 10/100/1000BASE-T Gigabit Ethernet transceivers. It supports SGMII & SerDes protocols to interface with the BCM56760 switch or the T1042 UC, as well as RGMII protocol to interface with the ShMC.

Figure 3: Ethernet Switch BCM56760 Block Diagrams



Its flexibility allows multiple configurations for the connection of two 1GbE links:

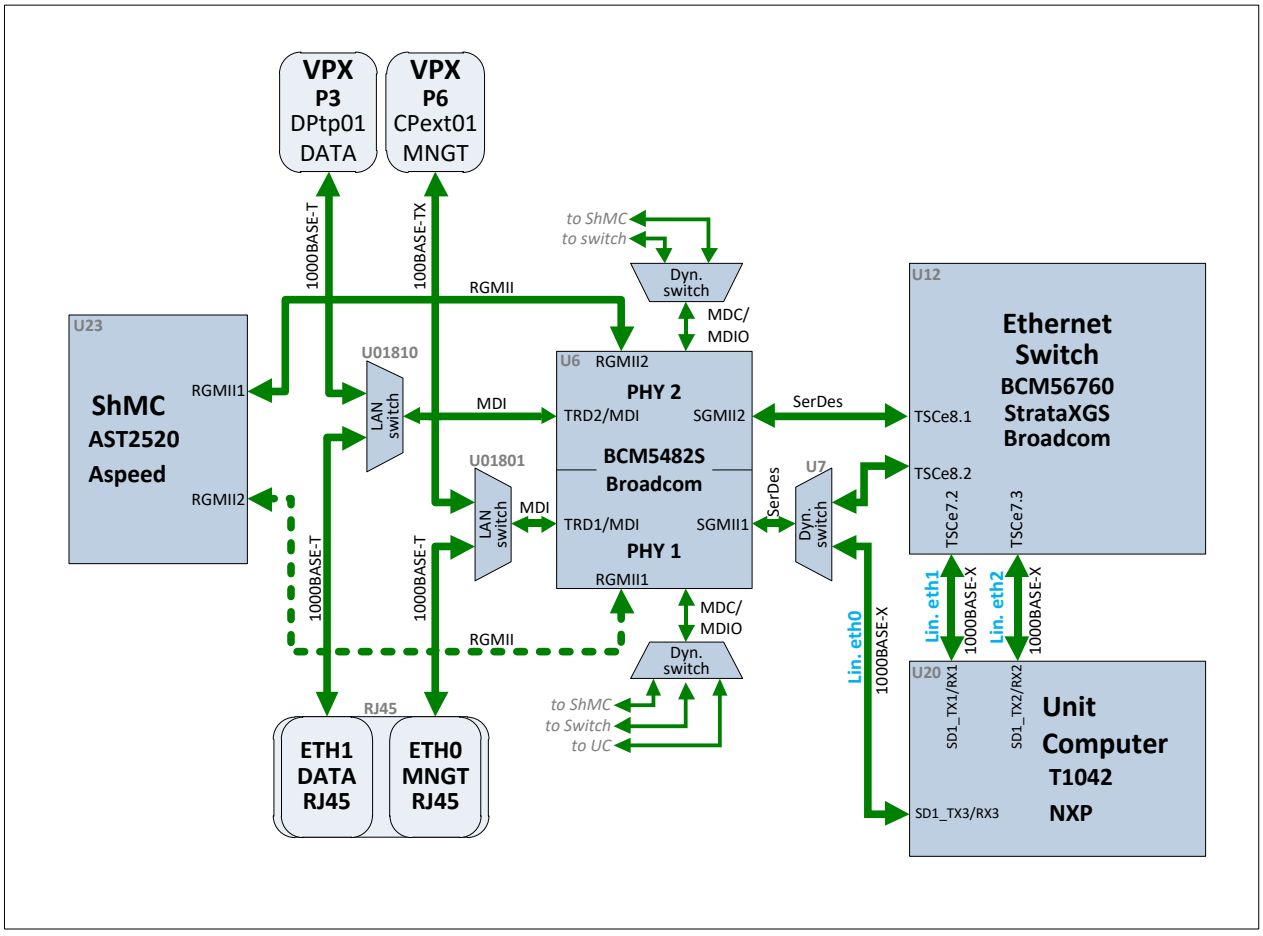
- The 1GbE management port: it is available as a 1000BASE-T port on front RJ45 or as a 100BASE-TX port on rear VPX connector P6. This port handled by the PHY #1 for the BCM5482S can be assigned either to the T1042 UC (default) or the BCM56760 switch or the ShMC on its RGMII2 interface.

- The 1GbE link primarily intended for the connection of the BCM56760 switch to the ShMC but which can be used as an additionnal switched link managed by the BCM56760 and available as a 1000BASE-T port on front or rear. This link is referred to as ETH1 or DATA 1GbE port, as opposed to the ETH0 MNGT port.

Figure 4 - an excerpt from the complete VX6940 Block Diagram - illustrates these configurations.

The BCM5482S is configured through MDC/MDIO links described in section 46.

Figure 4: VX6940 1GBe Ethernet links



MAC Addresses Allocation

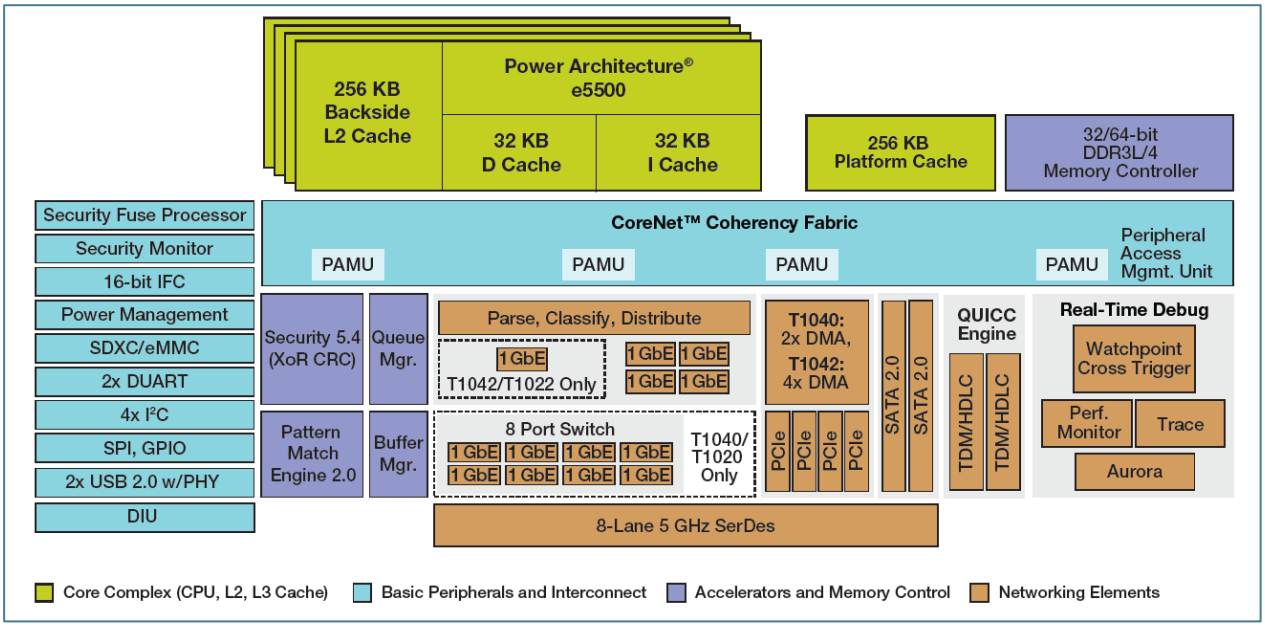
Table 2: MAC Addresses Allocation

Offset from base MAC address	Use case
0	Service port, typically first physical CPU Ethernet MAC and mapped by Linux to eth0
1	Unit computer Ethernet port connected to the fast data path (switch) and mapped by Linux to eth1
2	Unit computer Ethernet port connected to the fast data path (switch) and mapped by Linux to eth2
3	Network port, logical Ethernet MAC used by the network OS
4	Reserved
5	Reserved
6	Reserved by the ShMC (eth0)
7	Reserved by the ShMC (eth1)

2.2.2 Unit Computer QorIQ T1042

The Broadcom® FASTPATH software (8.7.x) operates on the Linux operating system run by the T1042 Unit Computer. It is a QorIQ communication processor supporting four integrated 64-bit e5500 Power Architecture® cores and featuring a high-performance data path acceleration architecture (DPAA).

Figure 5: T1042/22 Family Architecture



The Unit Computer Function includes:

- Freescale QorIQ T1042 quad core 1500 MHZ.
- 8GB SODIMM, DDR3-1600 with ECC.
- NOR Flash: 4 MBytes SPI Flash.
- NAND Flash: 8 GB eMMC 5.1 (possibly replaced by MicroSDcard socket).
- M.2 2242 socket conntected to SATA II (3 Gbps) interface.
- RTC wit h battery on I2C interface #3.
- SerDes ports configured as:
  - One PCI Express gen2 x2 for main interface with BCM56760 switch.
  - Two 1GbE 1000BASE-X links also to the BCM56760.
  - One 1GbE 1000BASE-X links connected to BCM5482S PHY to handle 1000BASE-T management port ETH0.
- IFC Interface with FPGA.
- Serial Lines connected to FPGA for redirection to front or rear.
- Two serial lines connected to FPGA, one being configured as management RS-232 serial port on front or rear.

2.2.3 Shelf Manager AST2520

The VX6940 supports an IPMI service processor which can act as a Shelf Manager (ShMC).

The Shelf Manager function includes:

- Service processor: AST2520 based on a 32-bit RISC ARM1176JZS CPU, 800MHz ,16 KB instruction & data cache.
- DDR3L memory: 2 Gbit DDR3-1600 memory-down device.
- NOR Flash: 4 MBytes SPI Flash .
- NAND Flash: 8 GB eMMC 5.1 (possibly replaced by MicroSDcard socket).
- EEPROM: 512kbit FRU EEPROM on I2C #2.
- Temperature monitoring: TMP423 sensor on I2C #1.
- Voltage monitoring: through integrated ADC.
- IPMI SMBus: SMB0 and SMB1 on I2C #4 and I2C #5 respectively routed to VPX.
- Two RGMII interfaces to BCM5482S to take control of 1GbE Management Port ETH0 and to connect to SerDes port of BCM56760 switch.
- Serial, SPI, LPC interfaces to FPGA.

The ShMC can connect with serveral ressources of the VX6940 for configuration or update :

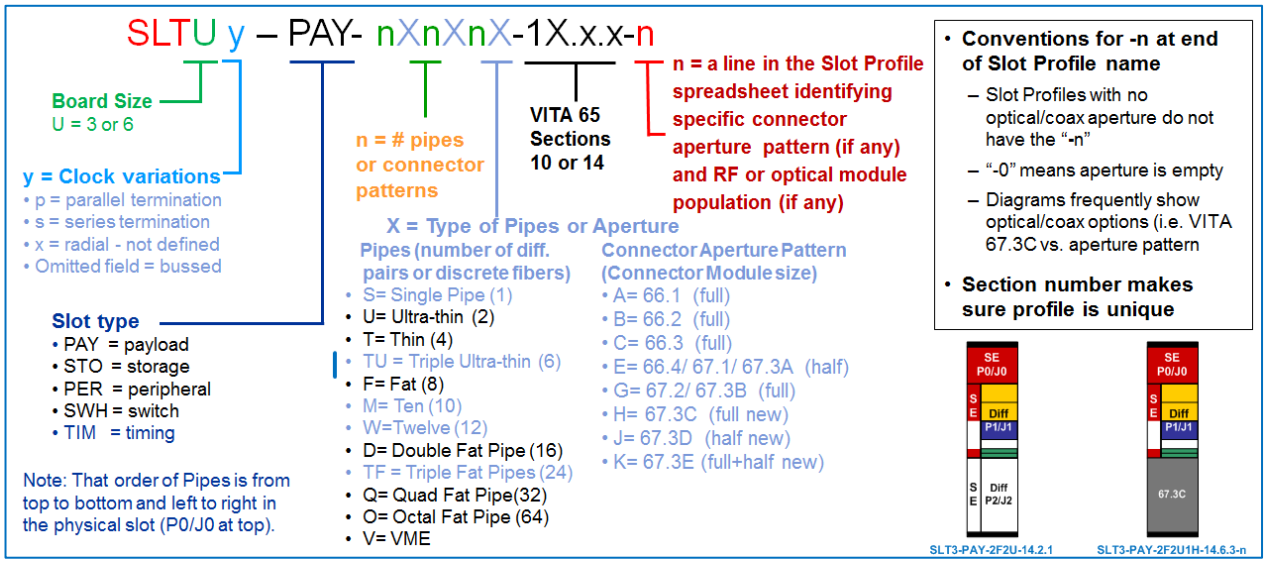
- T1042 UC SPI Flash (dynamic switching).
- FPGA SPI Flash (dynamic switching).
- BMC5482S MDC/MDIO (dynamic switching) for PHY configuration.
- RTC (resistors equipment).
- NOR Flash: 4 MBytes SPI Flash.
- NOR Flash: 4 MBytes SPI Flash.

2.2.4 Rear I/O Ports Allocation

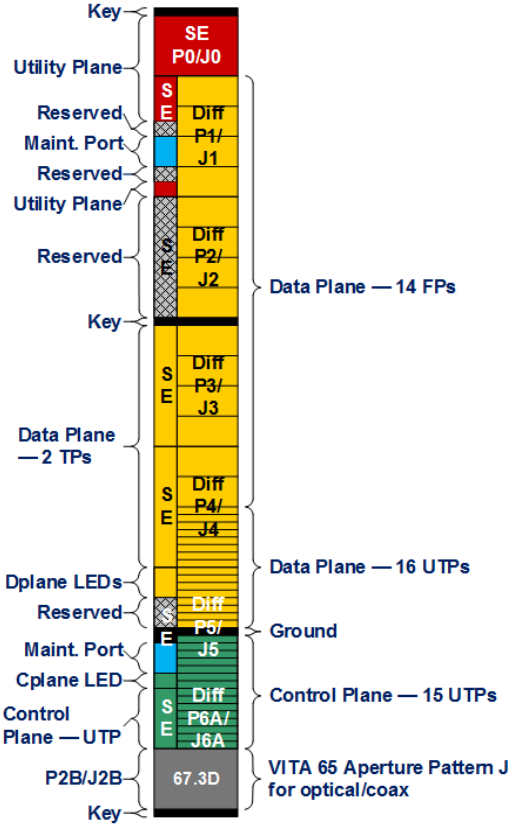
VPX Slot Profiles Definition

The VITA slot profile name construction is shown in Figure 6.

Figure 6: VPX Slot Profiles Name Consctruction



VX6940 VPX Slot Profile



MOD6-SWH-14F16U1U15U1J-10.8.1-n which stands for:

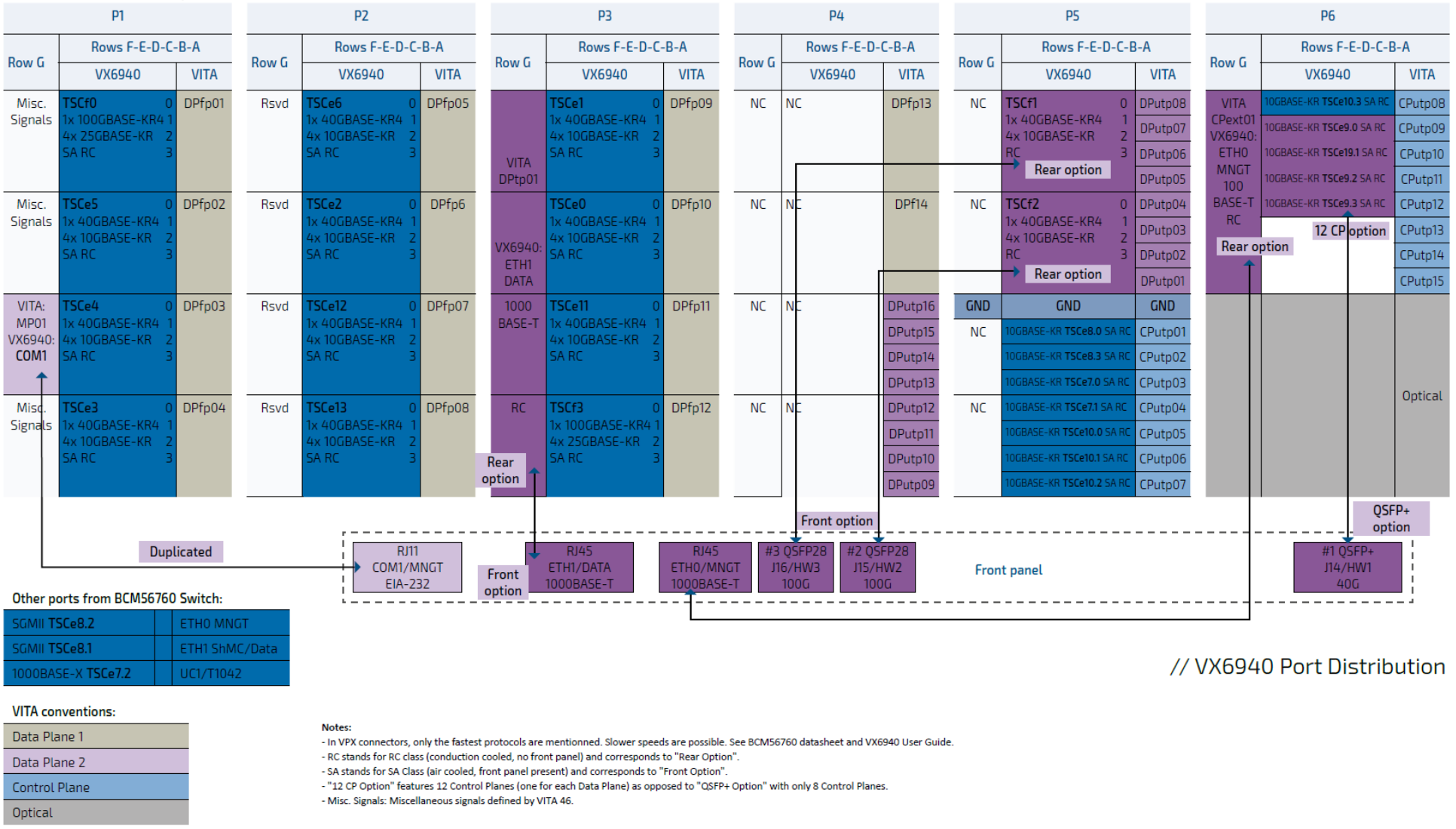
- Module (MOD)
- 6U form factor (6)
- Switch (SWH)
- 14 Fat pipes + 16 Ultra Thin Pipes + 1 Ultra Thin Pipe (GND) + 15 Ultra Thin Pipes + 1 half new (14F16U1U15U1J)
- VITA 65 section 10.8.1 (10.8.1)
- optical/coax aperture (-n)

VITA terminology defines the following SerDes links sizes and functions:

- Ultra Thin Pipe (utp): An Ultra Thin Pipe is made of 1 lane i.e. 1 SerDes link with one Transmit and one Receive differential pair.
- Fat pipe (fp): A Fat Pipe is made of 4 lanes i.e. 4 SerDes links which amount to 8 differential pairs.
- Data Plane: A Data Plane carries data and is carried either by a Ultra Thin Pipe or by a Fat Pipe. Except when they are intentionnally split, the Data Planes of VX6940 are all Fat Pipes.
- Control Plane: The Control Plane associated to its Data Plane is carried by a Ultra Thin Pipe.

Allocation of the BCM56760 SerDes Lanes on the rear VPX connectors and front QSFP cages

Figure 8: BCM56760 SerDes Lanes Allocation



Notes:
- In VPX connectors, only the fastest protocols are mentionned. Slower speeds are possible. See BCM56760 datasheet and VX6940 User Guide.
- RC stands for RC class (conduction cooled, no front panel) and corresponds to "Rear Option".
- SA stands for SA Class (air cooled, front panel present) and corresponds to "Front Option".
- "12 CP Option" features 12 Control Planes (one for each Data Plane) as opposed to "QSFP+ Option" with only 8 Control Planes.
- Misc. Signals: Miscellaneous signals defined by VITA 46.

2.3 Block Diagram

Figure 9: VX6940 Block Diagram

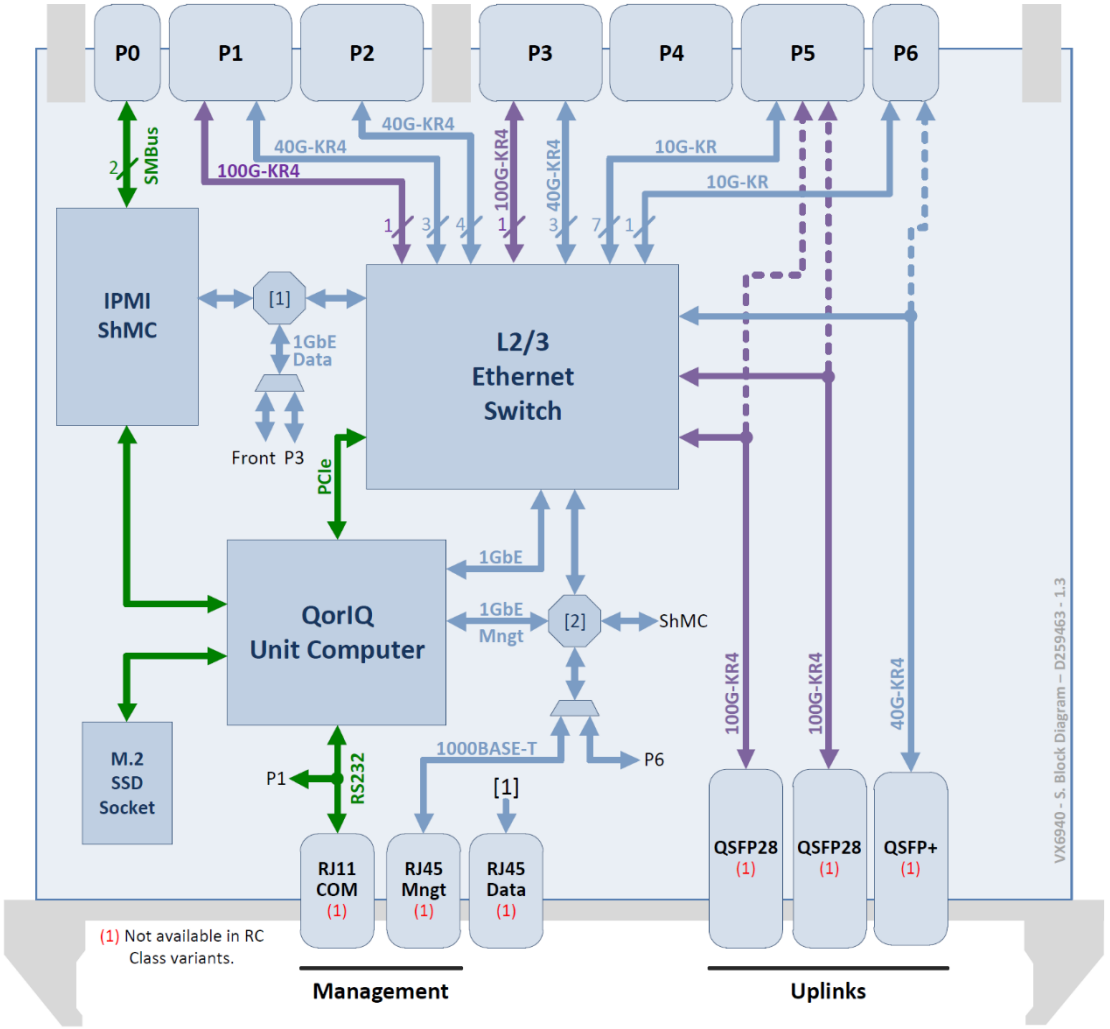
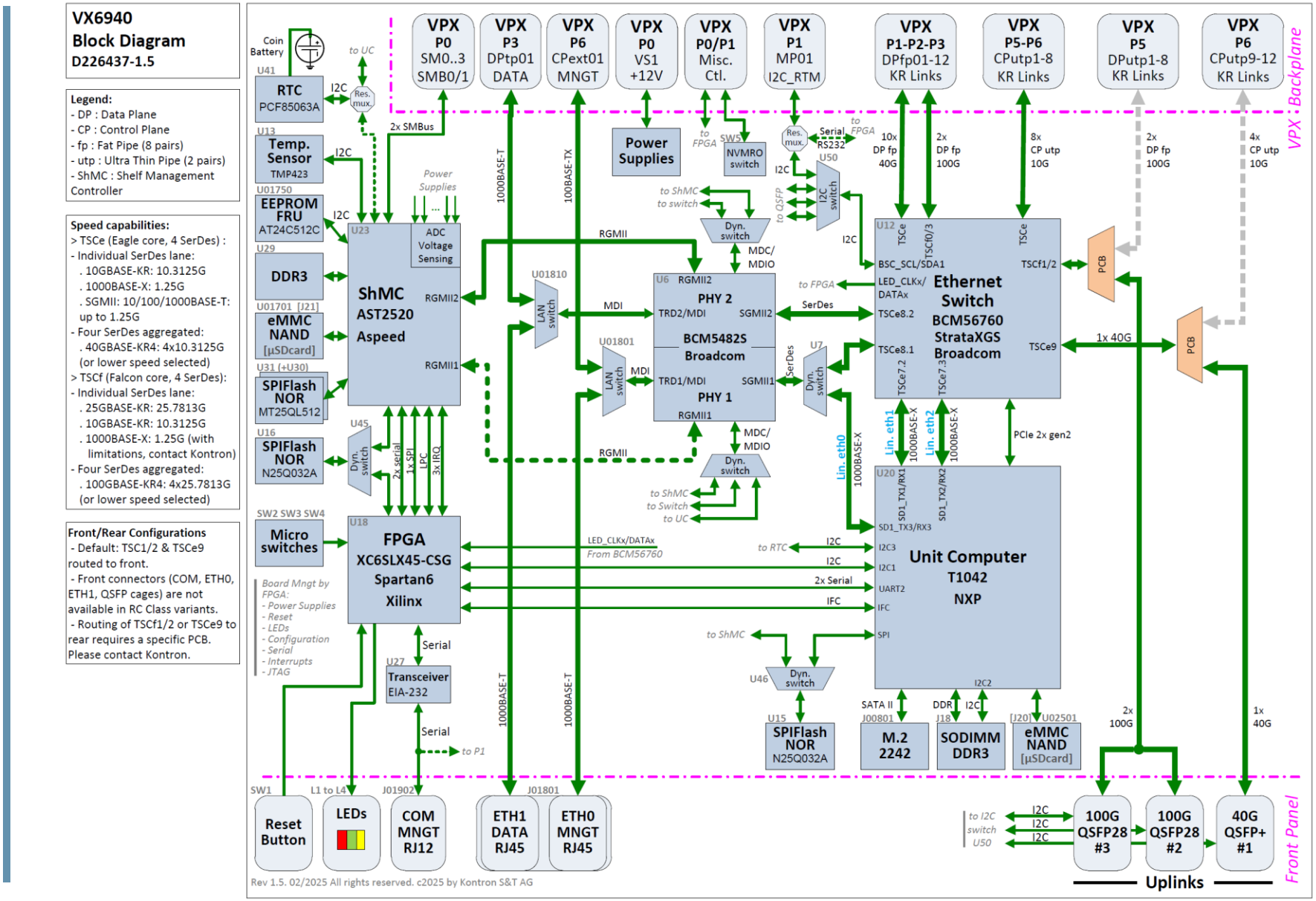


Figure 10: VX6940 Detailed Block Diagram



2.4 Ordering Information

Order Codes

Examples of VX6940 order codes are listed in Table 3. For actual availability, please contact Kontron.

Table 3: VX6940 Order Codes

Order Code	Description
VX6940-SA-00A00	6U Open VPX 10/40/100 GbE Managed Ethernet Switch. Based on the Broadcom switch BCM56760, the NXP QorIQ T1042 and the Aspeed AST2520. eMMC, M.2 2242 Socket. Switched Ethernet Lanes: - 12 rear VPX Fat Pipe Data Planes (12 quad Ethernet SerDes) - 8 rear VPX Ultra Thin Pipe Control Planes (8 Ethernet SerDes) - 2 front QSFP28 (4 Ethernet Lanes each) for 10G/40G/100G optical or passive copper connections - 1 front QSFP+ (4 Ethernet Lanes) for 1G/10G/40G optical or passive copper connections - 1 front RJ45 for 1000BASE-T connection Management ports: 1000BASE-T RJ45 ETH0 on front (default) or on rear (through LanSwitch configuration). RS-232 RJ12 COM link available on front and rear. Battery equipped. Standard Air-Cooled "SA" (0°C to +55°C). No conformal coating.
VX6940-RC-00A00	6U Open VPX 10/40/100 GbE Managed Ethernet Switch. Based on the Broadcom switch BCM56760, the NXP QorIQ T1042 and the Aspeed AST2520. eMMC, M.2 2242 Socket. Switched Ethernet Lanes: - 12 rear VPX Fat Pipe Data Planes (12 quad Ethernet SerDes) - 8 rear VPX Ultra Thin Pipe Control Planes (8 Ethernet SerDes) Rear data port: 1000BASE-T ETH1. Rear management ports: 100BASE-TX ETH0 & RS-232 COM link. Battery not equipped. Rugged Conduction-cooled RC3 (-40°C to +70°C). Conformal coating.

The associated products include two Rear Transition Modules listed in Table 4.

Table 4: Associated Products Order Codes

Order Code	Description
RTM-EZVX6940-MPO	6U VPX Air-Cooled Rear Transition Module. 8x 1000BASE-T ports. 12x Firefly optical transceivers.
RTM-EZVX6940-SFP	6U VPX Air-Cooled Rear Transition Module. 48x SFP ports, 4x 1000BASE-T ports.

Coding of the Manufacturing Options

Table 5 shows how the manufacturing options are coded in the order code.

This table is for information only. Please contact Kontron for available order codes.

Table 5: Coding of the Manufacturing Options

		VX6940 - Code	SA	-	0	0	A	0	0	V
Environment Class	Extended Air Cooled 0° +55°C Operating	SA								
	Extended Air Cooled -20° +55°C Operating	WA								
	Rugged Conduction-Cooled 'RC3/RC4' (-40°C to +70°C/85°C) with conformal coating	RC								
Software	Standard Feature set	0								
Front Panel	Yes	0								
Port Scheme	Standard Scheme	A								
System Management	Kontron Management Slave	0								
	Reserved (customization profile)	0								
Coating	-	0								
	Conformal Coating option on 'SA' build	V								

2.5 IO Interfaces

Front IO Interfaces

Front connectors are available in SA, WA and RA variants. For RC variants, please refer to Section 11.

Figure 11: Front Panel Connectors and LEDs

Table 6: Front IO Interfaces

Port ID	Description	Full Description
MNGT, DATA	Two 1000BASE-T ports on a dual RJ-45 connector : Management port ETH0 (MNGT) and port ETH1 (DATA).	Section 5.1.2
COM	Management EIA-232 port.	Section 5.1.1
Q3, Q2, Q1	Two QSFP28 & one QSFP+ for through optical or copper uplinks.	Section 5.1.3
RST	Reset push-button.	
L1 to L4	Four LEDs reporting the board health status and activity.	Section 5.4

Rear IO Interfaces

VPX rear connectors: P4 is not used. The second half of P6 is reserved for a future optical link.

Figure 12: Rear Connectors

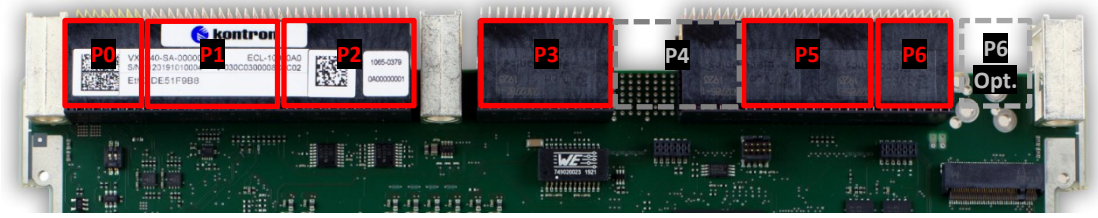


Table 7: Rear IOs Distribution

Port ID	Location	Description	Full Description
Ethernet KR lanes	P1, P2, P3, P5, P6	Switches Ethernet Ports: - 12 Data Plane / Fat Pipes - 8 Control Planes / Ultra Thin Pipes	Sections 5.3.2 to 5.3.7
ETH0 / MNGT	P6	100BASE-TX Management Ethernet port	Section 5.3.7
ETH1 / DATA	P3	1000BASE-T Switched Ethernet port	Section 5.3.4
SMB0/SMB1	P0	Two SMBus defined by IPMI standard	Section 5.3.1
VPX Controls	P0, P1	Miscellaneous VPX management signals: - GEOID, JTAG, SYSRESET#, NVMRO, VS1 power rail (P0) - GDISCRETE1, SYS_CON#, Maskable Reset#, RTM Reset# (P1)	Sections 5.3.1 & 5.3.2
Power Supplies	P0	Power supplies: - +12V VS1 power rail (P0) - +3.0V (P1) VBAT	Section 5.3.1
RTM Mngt	P1, P2	RTM management: - RTM_RST#, RTM_I2C (P1) - MDC/MDIO, LED_LCK/DATA (P2)	Section 5.3.2 & 5.3.3

2.6 Components Layout

Figure 13: VX6940 Components Layout (Top side)

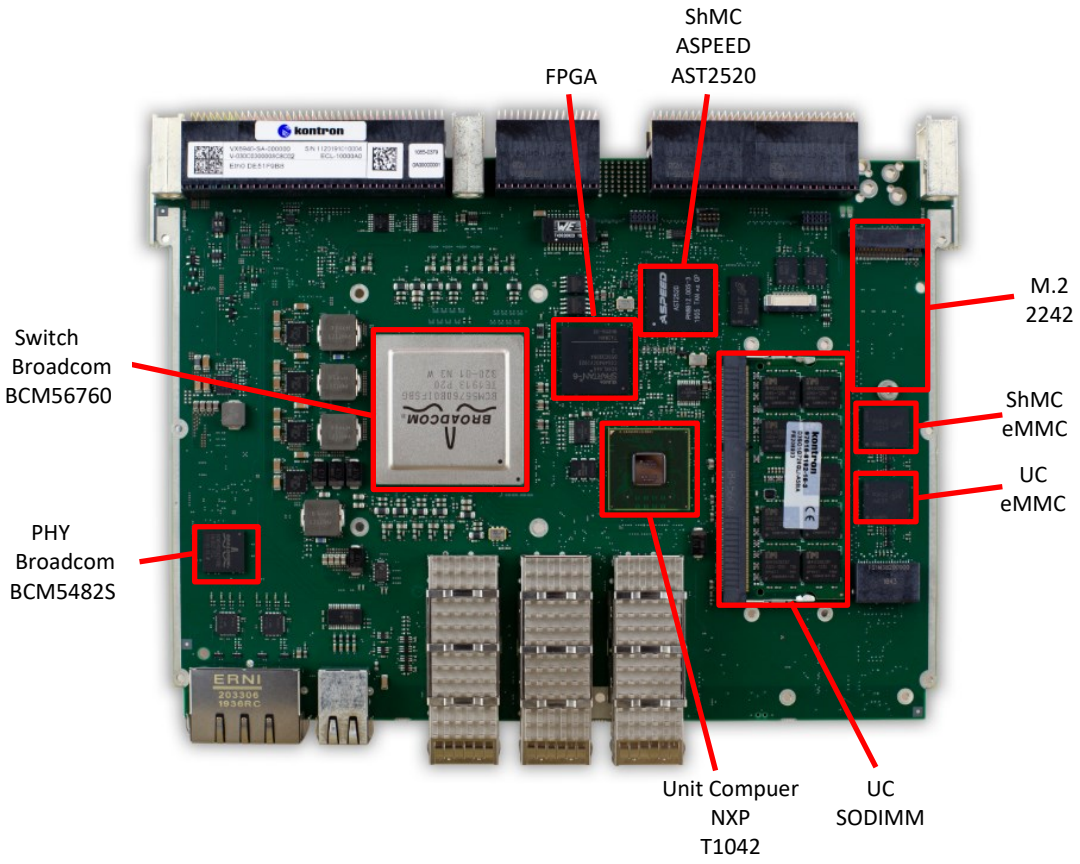
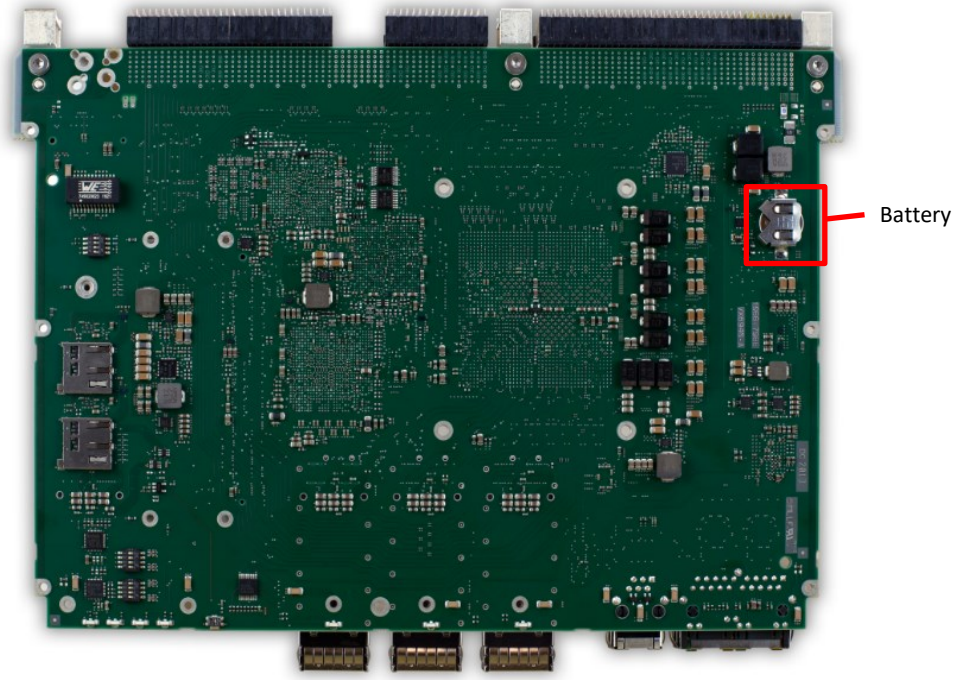


Figure 14: VX6940 Components Layout (Bottom side)



2.7 Technical Specification

Table 8: VX6940 Main Characteristics

Onboard Functions	Description
Unit Computer	NXP QorIQ T1042 quad-core processor : four integrated 64-bit e5500 cores, 1,2-1,4GHz.
	DDR3 SODIMM : 8GB, DDR3-1600, ECC, 204PIN, 800MHZ, 1.35V, -40/+85°C
	SPI Flash: NOR Flash Serial (SPI, Dual SPI, Quad SPI) 32M-bit 4M x 8 6ns SO8-200 -40/+85°C Note : Also accessible from ShMC
	Storage NAND Flash: 8GB eMMC 5.1.
	M.2 socket for SSD Flash modules: SATA II interface (3Gbps), 2242, D5 capable.
	Features not present in standard VX6940 version: MicroSDcard instead of eMMC, TPM 2.0, Approtect Secure Element
Ethernet Management	Ethernet switch : Broadcom BCM56760 featuring up to 72x 10GbE or 18x 40GbE integrated SerDes with support for 4x 100GbE.
	Ethernet PHY Broadcom BCM5482S: Dual-port 10BASE-T/100BASE-TX/1000BASE-T Gigabit Ethernet transceiver (RGMII, SGMII, and SerDes MAC interface options)
	LAN switch to route ETH0 MNGT port to front (1000BASE-T) or rear (100BASE-TX). (1) LAN switch to route ETH1 DATA port to front (1000BASE-T) or rear (1000BASE-T). (1)
Shelf Manager (ShMC)	Aspeed AST2520 service processor.
	DDR3 memory-down
	SPI Flash: 512Mbit NOR Flash, 104MHZ, -40/+85°C. A second spare device added for backup.
	Storage NAND Flash: 8GB eMMC 5.1.
	RTC & battery: External RTC with CR1220 battery.
	Temperature and voltage sensors.
	Feature not present in standard VX6940 version: MicroSDcard instead of eMMC,
Board Management	FPGA: Xilinx Spartan 6 XC6SLX45-CSG for boards management (reset, power supplies, LEDs, configuration etc.)
	FPGA SPI Flash: NOR Flash Serial (SPI, Dual SPI, Quad SPI) 32M-bit 4M x 8 6ns SO8-200 -40/+85°C Also accessible from ShMC
Backplane	Backplane connectors
	Ethernet 10G/40G/25G/100G ports: 2x VITA Fat Pipes / Data Planes supporting 2x quad 10G/25G SerDes links
	Ethernet 10G/40G ports: 10x VITA Fat Pipes / Data Planes supporting quad 10G SerDes links
	Ethernet 10G ports: 8x VITA Ultra Thin Pipes / Control Planes supporting 10G SerDes links
	Ethernet 100BASE-TX Port: Management Port ETH0 (dynamically redirected from front RJ45).
	Ethernet 1000BASE-T Port: Data Port ETH1 (dynamically redirected from front RJ45).
	Rear SMBus: SMB0 & SMB1.
	GPIOs: GDISCRETE1
	VPX Board Management: SYS_CON*, SYSRESET*, Maskable Reset*, NVMRO, GEOID (GAx, GAP#), JTAG.
	RTM Management: RTM I2C bus, RTM MDC/MDIO interface, RTM Reset*
	Power supplies: +12V VS1 power rail, VBAT
Front Panel (2)	Ethernet 1000BASE-T ports: Management port ETH0 and Data port ETH1 on dual RJ45 connector.
	RS-232 serial port: Management port COM on RJ11 connector.
	Uplink interfaces: 2x QSFP28 cages (each 1x 100G or 4x40G) and 1x QSFP+ cage (1x40G or 4x10G or 4x1G).
	Status LEDs: L1 to L4
	Reset push-button.
JTAG & Debug	JTAG and debug ports for development and production.
Battery	Coin cell battery in holder: CR1220.
Software	Description
Network Operating System (NOS)	Fastpath 8.6. Refer to VX6940 CLI Reference Manual.
IPMI	IPMI Version 2.0 compliant.
Mechanical Char.	Description
Form Factor	6U VPX, single slot, 1 inch pitch (4HP) ANSI/VITA 46.0
Weight	1290 g (SA, WA, RA classes)

(1) In RC Class variants, ETH0 and ETH1 ports are available on rear only.

(2) In RC Class variants, only Reset push-button and status LEDs are available. No management & data ports, no QSFP ports.

2.8 Environmental Specifications

Table 9: Environmental Specifications

Feature	SA Standard Commercial	WA Extended Temperature	RA Rugged air-cooled
Conformal coating	Optional	Standard	Standard
Air flow	6 CFM @52 W	12 CFM @52 W	16 CFM @52 W
Cooling method	Convection	Convection	Convection
Operating	0°C to +55°C	-20°C to +65°C	-40°C to +70°C
Storage (1)	-40°C to +85°C	-45°C to +100°C	-50°C to +100°C
Vibration Sine (Operating)	5 to 20 Hz : Displacement 1.25 mm 20 Hz to 500 Hz: 2 g Sweep rate : 1 octave / minute		5 to 19 Hz : Displacement 1.25 mm 19 Hz to 2000 Hz: 3 g Sweep rate : 1 octave / minute
Random (Operating)	5 Hz to 100 Hz: PSD = 0.04g²/Hz		5 Hz to 100 Hz: +3dB/octave 100 Hz to 1000 Hz: 0.04 g²/Hz 1000 Hz to 2000 Hz: -6dB/octave
Shock (Operating)	20 g, 11 ms, half-sine	20 g, 11 ms, half-sine	20 g, 11 ms, half-sine
Altitude (Operating)	-1 500 ft to 60 000 ft	-1 500 ft to 60 000 ft	-1 500 ft to 60 000 ft
Relative Humidity	90% without condensation (95% with coating option)	95% without condensation	95% without condensation

(1) The battery temperature range is -30°C to +70°C in SA and WA classes and -40°C to +85°C in RA class.

2.9 MTBF Data

The reliability predictions in Table 10 are based on standard MIL-HDBK-217F Notice 2 and were calculated for the following environments:

- Ground Benign (GB)
- Naval Sheltered (NS)
- Air Rotary Wing (ARW)
- Air Inhabited Cargo (AIC)

Table 10: VX6940 MTBF Data

MTBF	MILHDBK217F						
	GB (hours)		NS (hours)		ARW (hours)	AIC (hours)	
	25°C	40°C	25°C	40°C	55°C	40°C	55°C
VX6940-SA-00A00	139 155	113 819	33 256	25 375	5 554	19 416	12 536
VX6940-RC-00A00	144 202	117 810	35 077	26 652	5 970	20 468	13 111

3 Installation

The VX6940 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

3.1 Safety Requirements

The following safety precautions must be observed when installing or operating the VX6940. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Special care shall be taken while handling the board: the heat sink can get very hot during operation.

Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

This board contains electrostatic-sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector pins or traces.
- We strongly recommend our customers to work in an environment equipped with anti-static workbenches with professional discharging equipment.

3.2 Board Identification

The VX6940 boards are identified by labels fitted to the top side of the board.

The E.C. Level format is “xxxxxLy” where:

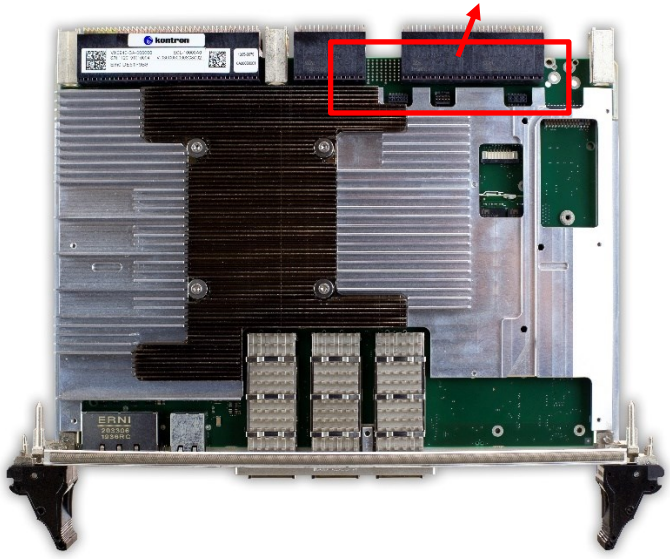
- The five digits “xxxxx” indicate the board E.C. Level (PCB revision included)
- “Ly” indicates the mechanical E.C. Level:
  - Letter “L” varies with the environment class (“A” for SA, “B” for WA, “C” for RA and “D” for RC)
  - Digit “y” gives the mechanical E.C. Level

See also section “Vital Product Data” in “VX6940 AMI-BIOS User Reference Manual”.

Top Side

Figure 15: VX6940 Identification (Top Side)

A "Identification" label: Order Code, Serial Number, Variant, E.C. Level, Ethernet first MAC address



3.3 Package Contents

The package contents include:

- The X6940 switch.
- A bag with the mechanical parts for the assembly of a M.2 module.

3.4 Board Configuration

3.4.1 Microswitches Identification

Figure 16: VX6940 Board Configuration - Microswitches (Top side)

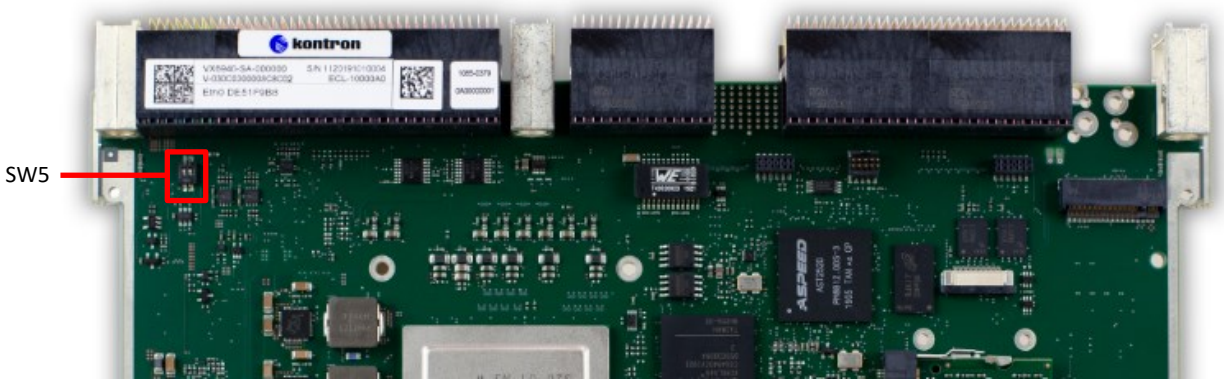
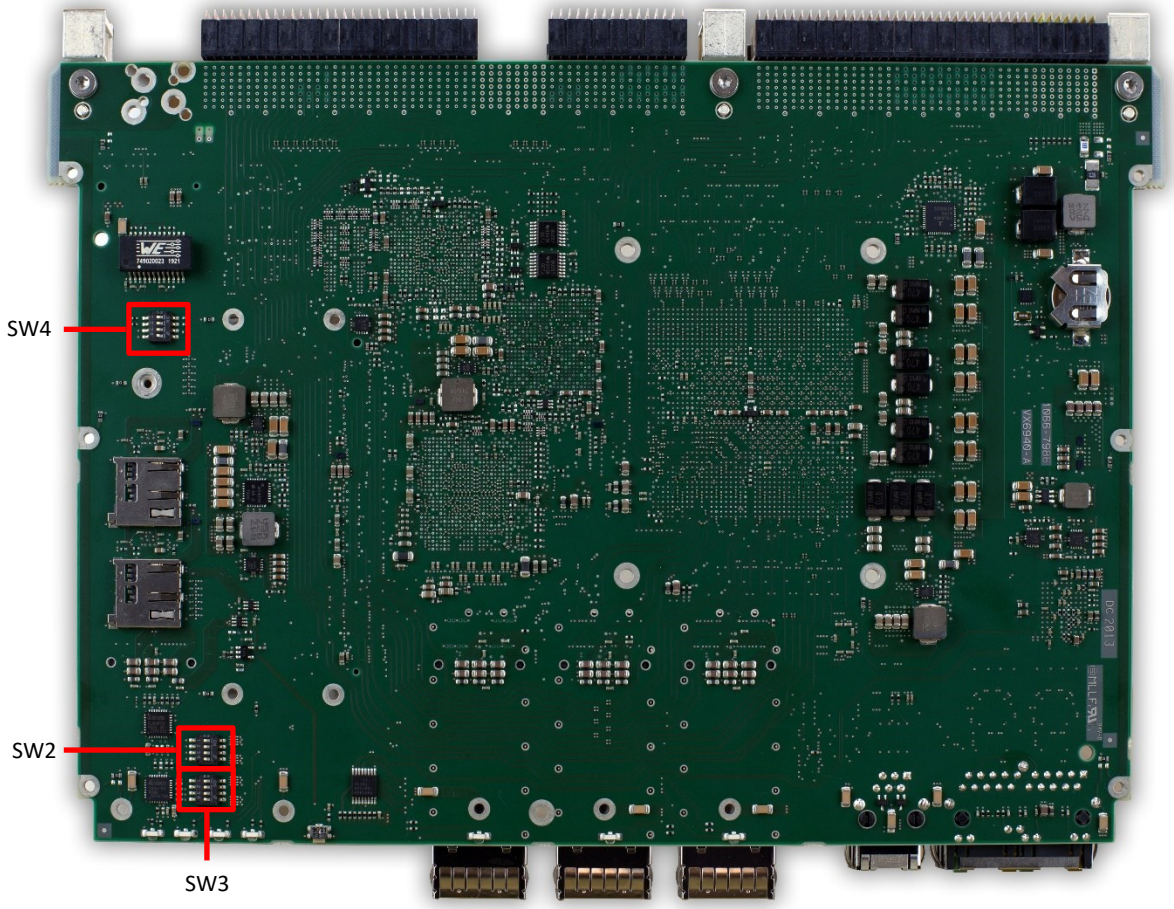


Figure 17: VX6940 Board Configuration - Microswitches (Bottom side)



3.4.2 Microswitches Definition

Table 11: Microswitch SW2

Function	Decription	Default
1- Watchdogs disable	OFF: ShMC and UC watchdogs enabled ON: ShMC and UC watchdogs disabled	OFF
2- ShMC override	OFF: ShMC NOT overriden ON: ShMC overriden (ShMC held in Reset; automatic power ON)	OFF
3- UC master	OFF: UC is the master of COM1, SPI, ETH1 ON: The master of COM1, UC SPI, ETH1 may be programmed independently.	OFF
4- Spare	Spare jumper	OFF

Table 12: Microswitch SW3

Function	Decription	Default
1- UC SPI write protect	OFF: UC SPI flash write protect enabled ON : UC SPI flash write protect disabled	OFF
2 - Spare	Spare jumper	OFF
3 - Spare	Spare jumper	OFF
4 - Spare	Spare jumper	OFF

Table 13: Microswitch SW4

Function	Decription	Default
1- JTAG Enable	OFF: JTAG_EN signal NOT activated. ON : JTAG_EN signal activated.	OFF
2- JTAG Reset	OFF: JTAG_RST# signal has a 75k pull-down. ON : JTAG_RST# signal has a 10k pull-up.	OFF
3- NVMRO Enable	OFF: NVMRO_EN signal activated. NVMRO taken into account ON : NVMRO_EN signal NOT activated. NVMRO has no impact on non-volatile memory write protection.	OFF
4- Spare	Spare jumper	OFF

Table 14: Microswitch SW5

Function	Description	Default
1- NMVRO	OFF: NVMRO is NOT forced to 0 by VX6940. ON : NVMRO is forced to 0 by VX6940. Potentially, all VPX Plug-in Modules may have their non-volatile memory devices updated.	OFF
2- Spare	Spare jumper	OFF

3.5 Initial Installation Procedures

To perform an initial installation of the VX6940 in a system proceed as follows:

1. Ensure that the safety requirements indicated in Section 3.1 are observed.

⚠CAUTION Failure to comply with the instructions below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the VX6940 refer to section 3.4. For the installation of Expansion cards and Mezzanines, refer to the appropriate sections in current chapter. For the installation of specific peripheral devices and Rear IO devices, refer to RTM in Chapter 8.

NOTICE Care must be taken when applying the procedures below to ensure that neither the VX6940 nor other system boards are physically damaged by the application of these procedures.

3. To install the VX6940:

3.1 Ensure that no power is applied to the system before proceeding.

NOTICE CAUTION: When performing the next step, DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

3.2 Carefully insert the board until it makes contact first with the backplane alignment keys, then with the backplane connectors.

3.3 Using the ejectors handles, engage the board with the backplane connectors. When the ejectors handles are locked, the board is fully installed.

3.4 Fasten the front panel retaining screws (SA, WA, RA classes) or the wedge locks (RC class).

3.5 Connect all external interfacing cables to the board as required.

3.6 Ensure that the board and all required interfacing cables are properly secured.

The VX6940 is now ready for operation.

3.6 Standard Removal Procedure

ESD Sensitive Device! Precautions are listed in chapter 3.1

To remove the board proceed as follows:

1. Turn off power.

2. Disconnect any interfacing cables that may be connected to the board (SA, WA, RA classes).

3. Loosen the front panel retaining screws (SA, WA, RA classes) or the wedge locks (RC class).

4. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.

5. After disengaging the board from the backplane, pull the board out of the slot.

HOT Surface!

Since the heat sink may be very hot, do not touch it when handling the board. Let the board cool to room temperature before further manipulation.

6. Dispose of the board as required.

3.7 Installation of Expansion Cards and Mezzanines

3.7.1 M.2 Module Insertion / Removal Instructions

Supported M.2 Module Types

The socket can host the following module types: 2242-XX-M and 2260-XX-M with XX = S1, S2, S3, D1, D2, D3, D4, D5.

Mechanical Parts

The mechanical parts are supplied in a bag.

Mechanical parts for the assembly of a M.2 module in its socket:

- Standoff socket S3 (H4.2): 1060-4972.
- Metallic washer: 1061-2434
- M2x6 Screw: 1058-7783

M.2 Module Insertion

ESD sensitive Device! Precautions are listed in chapter 3.1.

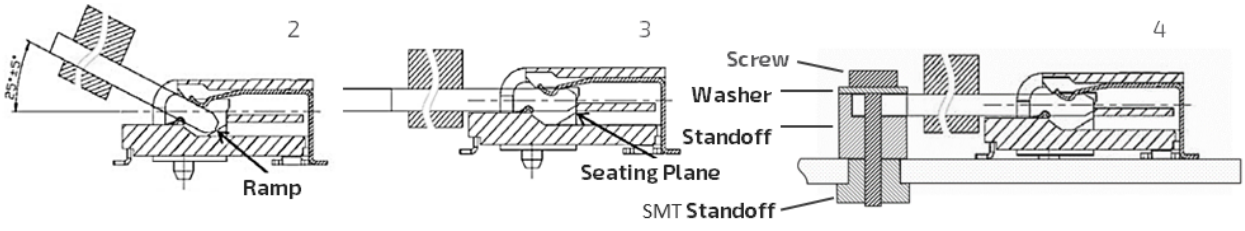
To install a M.2 module, proceed as follows:

1. Turn off power.
2. Insert the module with an angle of 25° until it touches the ramp.
3. Rotate the module to horizontal position and make sure the card edge touches the seating plane.
4. Attach module to PCB

   Place stand-off between module and VX6940 PCB.

   Add Washer and screw. Thread locker and torque as required by application.

Figure 18: M.2 Module Insertion



M.2 Module Removal

The removal of the M.2 Module is similar to the insertion : loosening the screw release the module

1. Turn off power.
2. Loosen the screw.
3. Remove screw, washer and stand-off.
4. Disengage the M.2 module.

3.7.2 Battery Location and Replacement

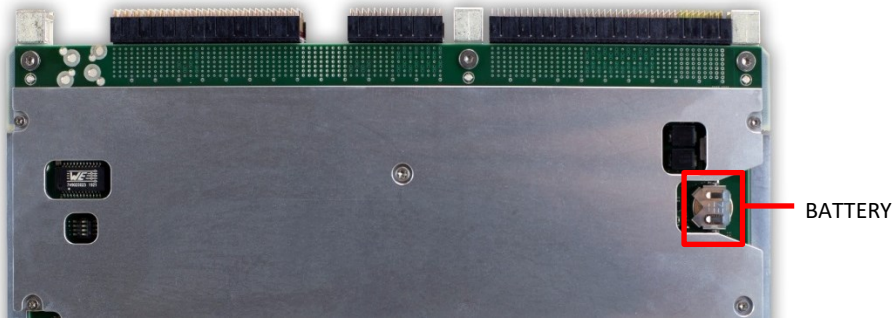
The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. The battery is used to run a time of day clock during the absence of power. Operation without the battery is possible but the date and time will not be retained in the absence of power. Alternatively the VPX VBAT signal from P1 can provide a 3.3V voltage from the backplane to retain the date and time

- **Battery Part Number**

Reference of the battery for VX6940-SA: RENATA CR1220 MFR (-30/+70°C)
Reference of the battery for VX6940-RA: RAYOVAC BR1225X-BA (-40/+85°C)

- **Battery Replacement**

Figure 19: Battery Holder Location on Bottom Side



To replace the battery, proceed as follows:

1. Turn off power.
2. Use a thin plastic tool to push the battery out of its holder.

NOTICE Do not subject the holder to mechanical stress when inserting the tool to eject battery.

3. Remove the battery.
4. Place the new battery into the socket with positive side (+) upwards and negative side (-) closest to printed circuit board

⚠CAUTION Danger of explosion when replacing with wrong type of battery. Replace only with the same part number or an UL recognised equivalent recommended by the manufacturer.

Do not dispose of lithium batteries in general trash collection. Dispose of the battery according to the local regulations dealing with the disposal of these special materials, (e.g. to the collecting points for dispose of batteries).

- **Battery Life**

Since the capacity of CR1220 MFR by Renata is 40 mAh, and the current drawn by RTC RV-8564-C2 is 450 nA max at 25°C, the expected battery life is 10 years in the absence of external power.

3.8 Software Installation

The VX6940 comes as a pre-installed system with all necessary OS, file system, drivers and applications factory-installed with default configurations.

Updating the Software with new operating system or applications or new versions is provided by a dedicated update mechanism, which is described in section 10.5.

3.9 Quick Start

This section gives instructions for (initially) accessing the CLI (Command Line Interface) of the VX3920 using either in-band access via the Ethernet fabric or the out-of-band management interfaces (serial port or Gigabit Ethernet) accessible from the front plate serial connector.

The CLI is required for configuring the GbE switch.

3.9.1 Out-of-Band CLI Access

The CLI can be accessed

- via the front plate serial port using the serial adapter cable
- or the Gigabit Ethernet port (MNGT)

3.9.1.1 Serial Port

The serial port is ready to use offhand without further configuration.

Port settings are:

- 115200 bps (serial speed might be different for customized system variants)
- 8 bit, no parity, 1 stop bit (8N1) no flow control

3.9.1.2 Ethernet Serviceport

The Gigabit Ethernet serviceport on the VX6940 has no IP address set by default, it is necessary to assign an IP address statically or enable dhcp on the serviceport. Because the required configuration steps are done in the CLI, an initial access using the serial port is required.

The procedure for assigning an IP address to the serviceport (MNGT) is described in the following. User input is printed in bold letters.

1. Connect to serial port on the front plate (using the Kontron DB9 adapter cable).

2. Ensure that the system is powered up.

3. Log in as admin and enter privileged mode by typing 'enable'. Note that a password is asked to be set after the first login.

```
User:admin
Password:<empty>
…
(Ethernet Fabric) >enable
Password:
(Ethernet Fabric) #
```

4. Set IP address and netmask. (see below for an example IP address setting)

```
(Ethernet Fabric) #serviceport ip 192.168.50.107 255.255.255.0
```

The GbE management interface is available from now on.

Alternatively, DHCP can be set for the serviceport

```
(Ethernet Fabric) #serviceport protocol dhcp
```

An IP address will be assigned to the serviceport by a DHCP server.

5. Save configuration using the 'write mem' command and confirm with 'y''

```
(Ethernet Fabric) #write memory
This operation may take a few minutes.
Management interfaces will not be available during this time.
Are you sure you want to save? (y/n) y
Config file 'current/startup-config' created successfully.
Configuration Saved!
```

```
(Ethernet Fabric) #
```

To access the CLI via Gigabit Ethernet serviceport, open a telnet connection to the configured IP address, port 23.

3.9.2 In-Band CLI Access

Since the GbE switch network port (in-band management access) on the VX6940 has no IP address set by default, it is necessary to assign an IP address to the network port either statically or through DHCP. Because the required configuration steps are done in the CLI, an initial access using the serial port is required.

The procedure for assigning an IP address to the network port is described hereafter with user input in bold print.

1. Connect to front serial port (using Kontron DB9 adapter cable).

2. Ensure that the system is powered up.

3. Log in as admin and enter privileged mode by typing 'enable' (no passwords required by default).

```
User:admin
Password:
(Ethernet Fabric) >enable
Password:
(Ethernet Fabric) #
```

4. Set IP address, netmask and default gateway. (see below for an example IP address setting)

(Ethernet Fabric) #network parms 192.168.50.107 255.255.255.0 192.168.50.254

The GbE management interface is available from now on.

Alternatively, DHCP can be set for the network port

```
(Ethernet Fabric) #network protocol dhcp
```

An IP address will be given to the network port by a DHCP server.

5. Save configuration by using the 'write mem' command and confirm 'y'

```
(Ethernet Fabric) #write memory
This operation may take a few minutes.
Management interfaces will not be available during this time.
Are you sure you want to save? (y/n) y
Config file 'current/startup-config' created successfully.
Configuration Saved!
(Ethernet Fabric) #
```

To access the CLI via the Gigabit Ethernet in-band network port, open a telnet connection to the configured IP address, port 23.

It might make sense to separate the management network from the data path by setting appropriate VLANs.

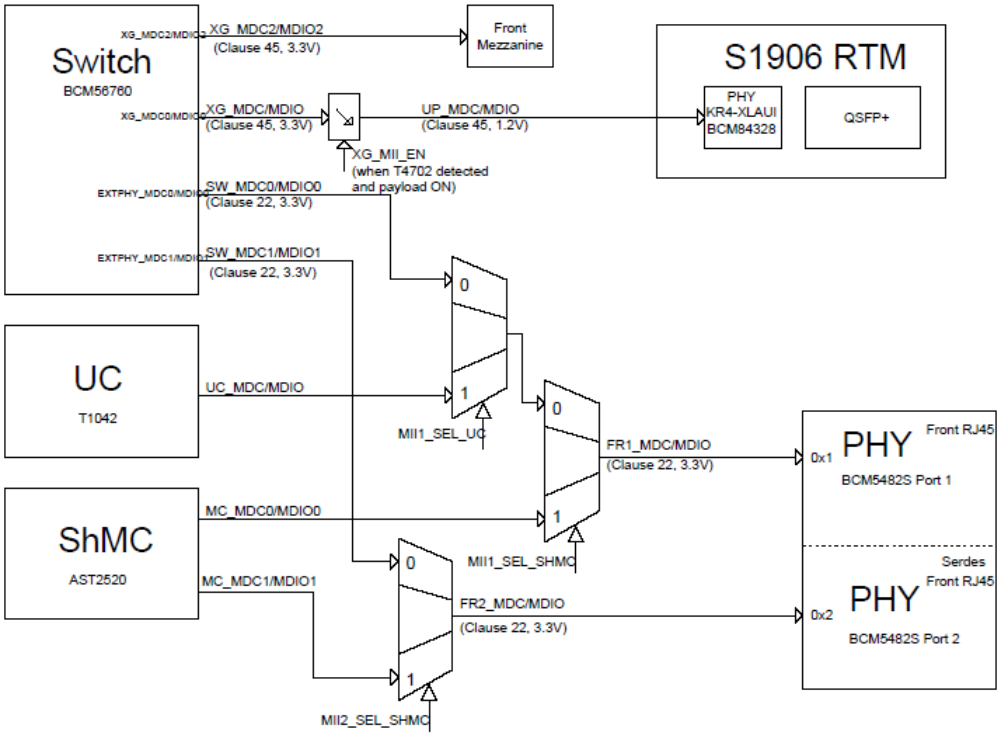
For additional information on the system configuration, refer to the VX6940 CLI Reference Manual.

4 Additional Board Features

4.1 MDC/MDIO Interface

The VX6940 benefits from the BCM5482S PHY flexibility by implementing multiple configuration schemes as shown in Figure 4, section 2.2.1. This implies that the MDC/MDIO interfaces of the BCM5482S be multiplexed for multi-master access as shown in the MDC/MDIO block diagram in Figure 20.

Figure 20: VX6940 MDC/MDIO Block Diagram

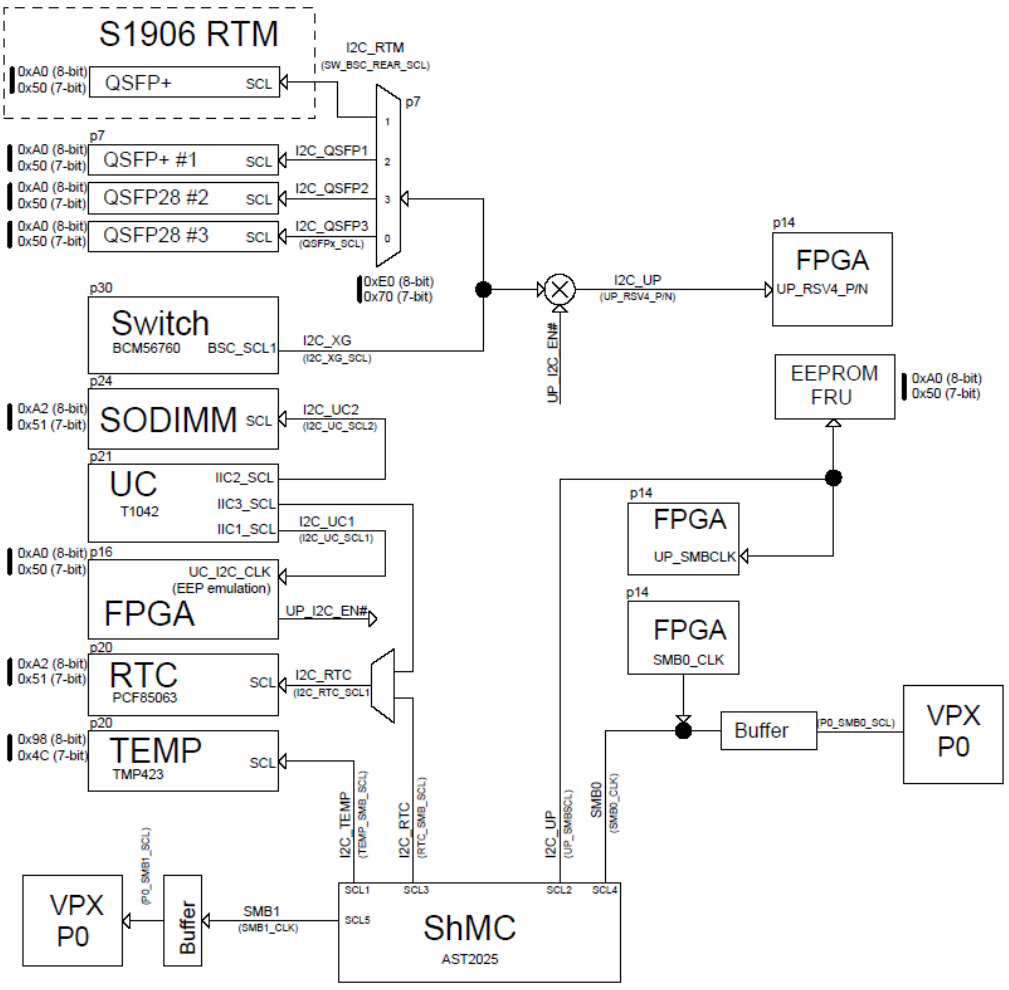


This diagram also show the connection of the XG_MDC/MDIO link to the RTM PHY.

4.2 I2C Structure

The VX6940 features not less than eight I2C busses handled by three I2C masters: the ShMC (4 busses), the Unit Computer T1042 (3 busses) and the BCM56760 (1 bus). These busses and the associated devices are illustrated in Figure 21.

Figure 21: VX6940 I2C Block Diagram



4.3 Real-Time Clock RTC

Standalone low-power RTC PCF85063A

The PCF85063A RTC by NXP features an internal oscillator, date and time keeping module with programmable alarm, timer and interrupt functions, a programmable offset register for frequency adjustment. The stability of its quartz crystal is +/- 20 ppm at 25°C (equivalent to a drift of 10 mn per year). Its 32.768 kHz clock output drives the FPGA.

Standby power supplied to the PCF85063A RTC

When the VX6940 is powered off, the RTC is powered through Schottky diodes either by the onboard 3.0 V battery or by the VPX 3.0V VBAT input (P1).

The RTC has an ultra low-power consumption in time keeping mode: 220 nA typical at 25°C and 600 nA maximum in -40°C/+85°C temperature range.

The RTC on the I2C_RTC bus

The RTC is located on the I2C bus I2C_RTC @0x51 (7-bit). This bus is by default connected to the T1042 I2C interface #3 but it can be connected through resistor equipment (production variant) to the ShMC I2C interface #3.

4.4 Battery

Battery location and replacement

Refer to section 3.7.2 Battery Replacement.

Battery life

Since the capacity of CR1220 MFR by Renata is 40 mAh, and the current drawn by RTC RV-8564-C2 is 450 nA max at 25°C, the expected battery life is 10 years in the absence of external power.

4.5 FPGA

The Xilinx Spartan6 XC6SLX45-CSG484 FPGA performs the following functions:

- Reset management.
- Onboard voltage regulators monitoring through PowerGood signals.
- Interrupts management for ShMC and UC.
- Interface to AST2520 ShMC: the FPGA is an SPI slave and a LPC master.
- Interface to T1042 UC: IFC interface.
- Interface to BCM56760 switch: LED interface (LED_CLK0/1 & LED_DATA0/1).

- Serial interfaces routing to/from ShMC, UC and COM port.
- Front LEDs for board status display.
- Board configuration through microswitches.
- Internal registers, and system management.
- JTAG management: The FPGA interconnects JTAG ports from/to the VPX, the onboard connector J01501, itself (programmation), and the onboard components T1042 UC, BCM56760 switch, AST2520 ShMC, BCM5482S PHY, COP debug header J11.

4.6 GPIOs

GDISCRETE1 is a VPX bussed bidir GPIO defined by VITA 65.0. On VX6940 it is:

- an open-drain output driven by the FPGA.
- an input connected to ShMC GPIOG7/SGPS2I1/SALT4 (SMB_ALERT4#)

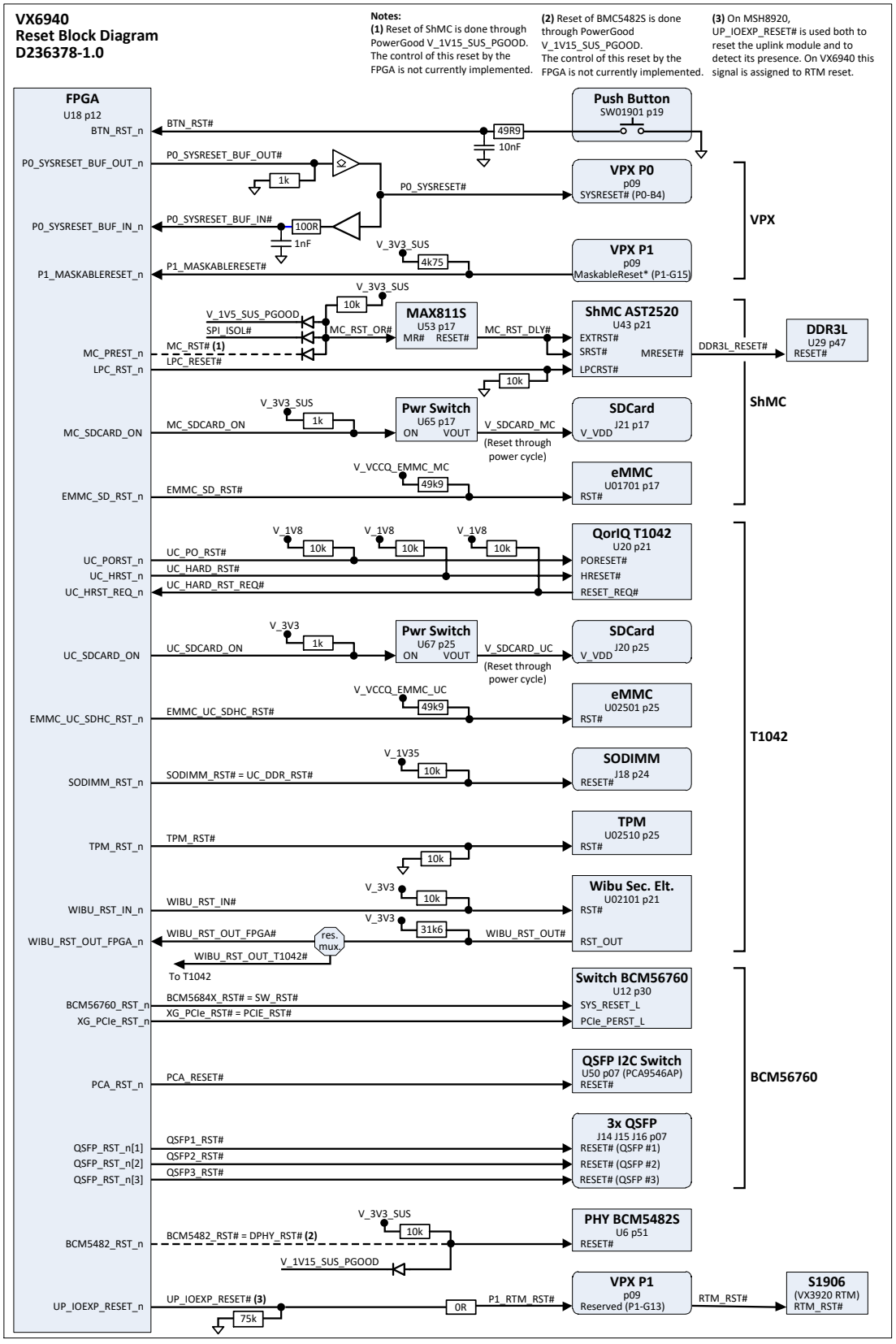
4.7 Reset

The reset sources of the VX6940 are:

- The VPX SYSRESET#.
- The VPX Maskable Reset#.
- The front reset push-button
- Addressed reset through the FPGA.

The FPGA handles the reset of all the VX6940 components as shown in the Reset Diagram, Figure 22.

Figure 22: Reset Diagram



4.8 EEPROMs and Flash Devices Write Protection

NVMRO

VITA 46.0 NVMRO (Non-Volatile Memory Read Only) is a system wide signal which, when asserted, prevents any non-volatile memories from being updated. On VX6940 it is routed to the FPGA which handles the Write-Enable controls.

To ease production tests on the VX6940, NVMRO will be ignored if microswitch SW4.3 is ON. Therefore, for normal operation, SW4.3 is always OFF.

Setting the microswitch SW5.1 ON will force NVMRO to 0, thus potentially enabling the update of the non-volatile memories of all the Plug-in Modules installed in the chassis.

Ensure that SW5.1 microswitch is never set ON unintentionally. Deasserting NVMRO by setting SW5.1 ON may impact the safety of the entire system since non-volatile memory updates will no longer be prevented.

4.9 Security Devices

4.9.1 Trusted Platform Module

The Infineon TPM 2.0 SLB9670 may be equipped. Please contact Kontron.

4.9.2 APPROTECT and the CodeMeter ASIC Technology by Wibu

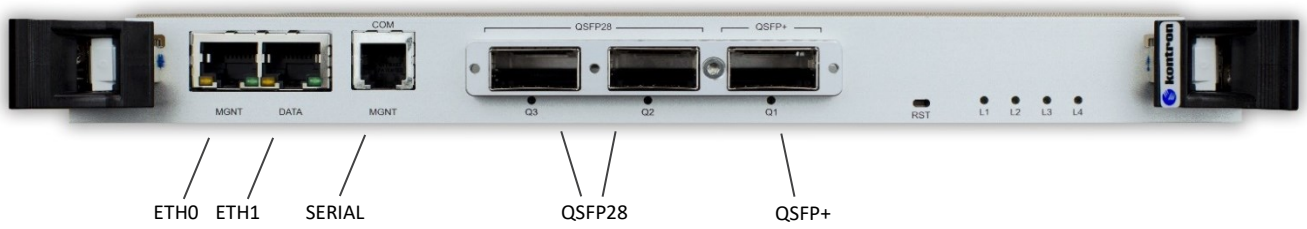
The Approtect Secure Element by Wibu with SPI interface may be equipped. Please contact Kontron

5 Physical IOs

5.1 Front Panel Connectors

Front connectors are available in SA, WA and RA variants. For RC variants, please refer to section 11.

Figure 23: Front Panel Connectors



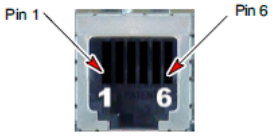
Manufacturer	MPN	Description	4-4 KGS	Function	Port ID	Refdes
STEWART	SS-6466S-A-PG4-BA	Conn RJ11 Modular Jack F 6 POS 2.54mm Solder RA Thru-Hole 6 Terminal 1 Port	1053-3454	Serial front management port	COM	J1902

COM Serial Port Pin Assignment

Table 15: Serial Connector Pin Assignment

Pin	Signal
1	COM1 RTS
2	NC
3	COM1 TXD
4	COM1 RXD
5	GND
6	COM1 CTS
CASE1 - CASE2	SHELL

Figure 24: Serial RJ11 Connector



COM Serial Port Signals Definition

Table 16: Serial Connector Signals Definition

Signal	Direction	Definition
COM1 TXD	Output	EIA-232 Transmit Data of port COM
COM1 RXD	Input	EIA-232 Receive Data of port COM
COM1 RTS	Output	EIA-232 Transmit Data of port COM
COM1 CTS	Input	EIA-232 Receive Data of port COM
GND	-	Power supply return and logic ground.
SHELL	-	Chassis ground

NOTICE

CAUTION: COM signals may be routed to both front panel connector and rear P1. Plugging a serial device to both connectors will lead to electrical contention. Be sure to use only one connector at a time.

5.1.2

5.1.3 Gigabit Ethernet Connector - Ports ETH0 & ETH1

Identification

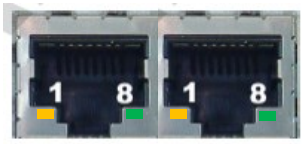
Manufacturer	MPN	Description	4-4 KGS	Function	Port ID	Refdes
ERNI	203306	Conn RJ45 Modular Jack F 20 POS 2.54mm Solder RA Thru-Hole 28 Terminal 2 Port, with magnetics	1062-1533	Ethernet 1000BASE-T front management port and data port	ETH0 ETH1	J1801

ETH0 & ETH1 R45 Pin Assignment

Table 17: Gigabit Ethernet Connector Pin Assignment

Pin	Signal
1	TX+ / BI_DA+
2	TX- / BI_DA-
3	RX+ / BI_DB+
4	BI_DC+
5	BI_DC-
6	RX- / BI_DB-
7	BI_DD+
8	BI_DD-
CASEn	SHELL

Figure 25: Gigabit Ethernet Connector



ETH0 ETH1

ETH0 & ETH1 R45 Signals Definition

Table 18: Signals Definition

Signal	Dir.	Definition
TX+/- / BI_DA+/-	O - I/O	10BASE-T & 100BASE-T: Transmit differential pair 1000BASE-T: BI_DA differential pair TRD1 corresponds to ETH0, TRD2 to ETH1.
RX+/- / BI_DB+/-	I - I/O	10BASE-T & 100BASE-T: Receive differential pair 1000BASE-T: BI_DB differential pair TRD1 corresponds to ETH0, TRD2 to ETH1.
BI_DC+/-	I/O	10BASE-T & 100BASE-T: NC 1000BASE-T: BI_DC differential pair TRD1 corresponds to ETH0, TRD2 to ETH1.
BI_DD+/-	I/O	10BASE-T & 100BASE-T: NC 1000BASE-T: BI_DD differential pair TRD1 corresponds to ETH0, TRD2 to ETH1.
SHELL	-	Chassis ground

5.1.4 Front QSFP Connectors

Identification

Manufacturer	MPN	Description	4-4 KGS	Function	Port ID	Refdes
YAMAICHI	CN120-038-0001	Conn RJ45 Modular Jack F 20 POS 2.54mm Solder RA Thru-Hole 28 Terminal 2 Port, with magnetics	1060-4094	Two QSFP28 and one QSFP+ interfaces.	QSFP#3 QSFP#2 QSFP#1	J16 J15 J14

QSFP Pin Assignment

Table 19: QSFP Connector Pin Assignment

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	13	GND	25	RX4_P	37	TX1_N
2	TX2_N	14	RX3_P	26	GND	38	GND
3	TX2_P	15	RX3_N	27	MODPRS#		
4	GND	16	GND	28	INT#		
5	TX4_N	17	RX1_P	29	V_VCC_TX		
6	TX6_P	18	RX1_N	30	V_VCC1		
7	GND	19	GND	31	LPMODE		
8	MODSEL#	20	GND	32	GND		
9	RESET#	21	RX2_N	33	TX3_P		
10	V_VCC_RX	22	RX2_P	34	TC3_N		
11	SCLn	23	GND	35	GND		
12	SDAn	24	RX4_N	36	TX1_P		

Figure 26: QSFP Connector

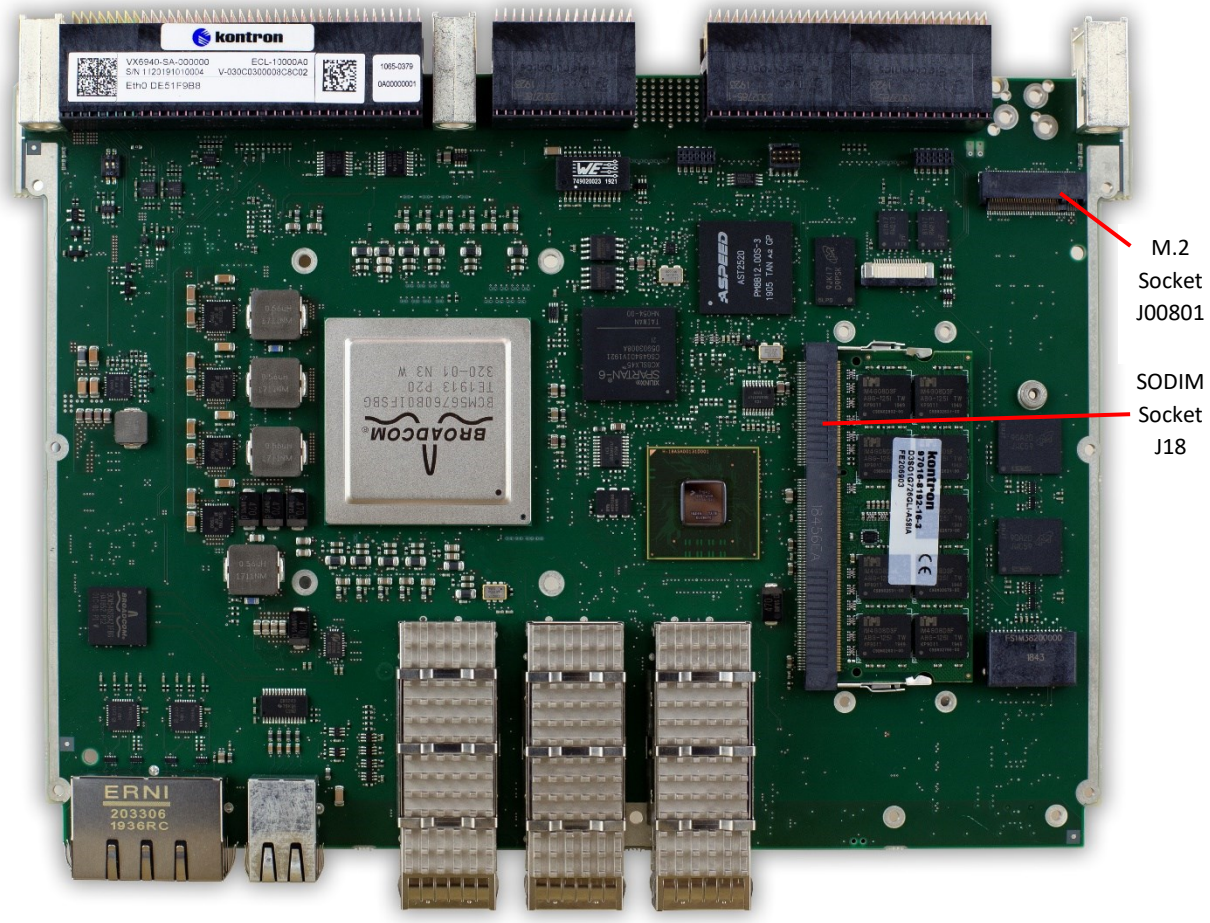
QSFP Signals Definition

Table 20: Signals Definition for QSFP

Signal	Dir	Description
GND	-	Power supply return and logic ground.
INT#	O	Open Drain. Module Interrupt.
LPMODE	I	Low Power Mode. Not managed on VX6940.
MODPRS#	O	Open Drain. Module Present.
MODSEL#	I	Mode Selection. Not managed on VX6940 (always active).
RESET#	I	Module Reset.
RXx_P/N	O	Receive Differential Pair number x with x = 1 to 4 On VX6940, connected to SerDes link TSCe9 (QSFP1) or TSCf2 (QSFP2) or TSCf1 (QSFP3).
TXx_P/N	I	Transmit Differential Pair number x with x = 1 to 4 On VX6940, connected to SerDes link TSCe9 (QSFP1) or TSCf2 (QSFP2) or TSCf1 (QSFP3).
SCLn	I	Serial clock of I2C bus I2C_QSFP1 to I2C_QSFP3.
SDAn	I/O	Serial data of I2C bus I2C_QSFP1 to I2C_QSFP3.
V_VCC_RX/TX	Power	Receive/Transmit +3.3V Power Supply
V_VCC1	Power	+3.3V Power Supply

5.2 Onboard Connectors

Figure 27: Onboard Connectors



5.2.1 M.2 Module Socket

- Identification

Manufacturer	MPN	Description	4-4 KGS	Function	Port ID	Refdes
TE Connectivity	1-2199230-6	SMT M.2 Minicard mounting connector, 0.5mm pitch, 67 pos, 4.2mm height, 0.5A, key M, ROHS -40/+80°C	1056-0723	M.2 SSD socket	M2_SATA: UC_SD_TX7+/- UC_SD_RX7+/-	J00801

According to PCIe M.2 specification, type M corresponds to socket type "Socket 3 SSD drive" (Table 1 - Optional Module Configurations).

- M.2 Socket Pin Assignment

Table 21: M.2 Sockets Pin Assignment

Pin	Signal
74	3.3V
72	3.3V
70	3.3V
68	NC (SUSCLK 32kHz)
	Connector Key
	Connector Key
	Connector Key
	Connector Key
58	NC (Reserved MFG_clock)
56	NC (Reserved MFG_data)
54	NC (PEWAKE#)
52	NC (CLKREQ#)
50	NC (PERST#)
48	NC
46	NC
44	NC
42	NC
40	NC
38	DEVSLP
36	NC
34	NC
32	NC
30	NC
28	NC
26	NC
24	NC
22	NC
20	NC
18	3.3V
16	3.3V
14	3.3V
12	3.3V
10	NC (LED1# / DAS_DSS#)
8	NC
6	NC
4	3.3V
2	3.3V

Signal	Pin
GND	75
GND	73
GND	71
PEDET	69
NC	67
Connector Key	
Connector Key	
Connector Key	
Connector Key	
GND	57
NC (REFCLKP)	55
NC (REFCLKN)	53
GND	51
SATA-A+ (PETp0 / SATA-A+)	49
SATA-A- (PETn0 / SATA-A-)	47
GND	45
SATA-B- (PERp0 / SATA-B-)	43
SATA-B+ (PERn0 / SATA-B+)	41
GND	39
NC (PETp1)	37
NC (PETn1)	35
GND	33
NC (PERp1)	31
NC (PERn1)	29
GND	27
NC (PETp2)	25
NC (PETn2)	23
GND	21
NC (PERp2)	19
NC (PERn2)	17
GND	15
NC (PETp3)	13
NC (PETn3)	11
GND	9
NC (PERp3)	7
NC (PERn3)	5
GND	3
GND	1

Note: When the name of a signal differs between VX6940 and standard pinout, the standard pinout name is shown in parentheses.

- M.2 Socket Signals Definition

Table 22: M.2 Socket Signals Definition

Signal PCIe / SATA	Direction	Definition
3.3V	Output	+3.3V power supply.
GND	-	Power supply return and logic ground.
SATA-B+/-	Input	SATA transmit differential pair connected to UC SATA receive pair #7.
SATA-A+/-	Output	SATA receive differential pair connected to UC SATA transmit pair #7.

5.2.2 SoDIMM Socket

- **Identification**

Manufacturer	MPN	Description	4-4 KGS	Function	Port ID	Refdes
Kontron	97016-8192-16-3	SODIMM 8GB, DDR3-1600, ECC, 204 pins, 800MHz, 1.35V	1055-7524	SO DIMM	UC DDR	J18

- **SODIMM Pin Assignment**

Table 23: SoDIMM Socket Pin Assignment

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VREFCA	43	DQS2#	85	VDD	127	C0#	169	GND
2	GND	44	DM2	86	VDD	128	ODT1	170	GND
3	GND	45	DQS2	87	CKE0	129	C1#	171	DQS6#
4	DQ4	46	GND	88	A15	130	A13	172	DM6
5	DQ0	47	GND	89	CKE1	131	VDD	173	DQS6
6	DQ5	48	DQ22	90	A14	132	VDD	174	DQ54
7	DQ1	49	DQ18	91	BA2	133	DQ32	175	GND
8	GND	50	DQ23	92	A9	134	DQ36	176	DQ55
9	GND	51	DQ19	93	VDD	135	DQ33	177	DQ50
10	DQS0#	52	GND	94	VDD	136	DQ37	178	GND
11	DMO	53	GND	95	A12/BC#	137	GND	179	DQ55
12	DQS0	54	DQ28	96	A11	138	GND	180	DQ60
13	DQ2	55	DQ24	97	A8	139	DQS4#	181	GND
14	GND	56	DQ29	98	A7	140	DM4	182	DQ61
15	DQ3	57	DQ25	99	A5	141	DQS4#	183	DQ56
16	DQ6	58	GND	100	A6	142	DQ38	184	GND
17	GND	59	DM3	101	VDD	143	GND	185	DQ57
18	DQ7	60	DQS3#	102	VDD	144	DQ39	186	DQS7#
19	DQ8	61	GND	103	A3	145	DQ34	187	GND
20	GND	62	DQS3	104	A4	146	GND	188	DQS7#
21	DQ9	63	DQ26	105	A1	147	DQ35	189	DM7
22	DQ12	64	GND	106	A2	148	DQ44	190	VSS
23	GND	65	DQ27	107	A0	149	GND	191	DQ58
24	DQ13	66	DQ30	108	BA1	150	DQ45	192	DQ62
25	DQS1#	67	GND	109	VDD	151	DQ40	193	DQ59
26	GND	68	DQ31	110	VDD	152	GND	194	DQ63
27	DQS1	69	CB0	111	CK0	153	DQ41	195	GND
28	DM1	70	GND	112	PAR_IN/NC/CK 1	154	DQS5#	196	GND
29	GND	71	CB1	113	CK0#	155	GND	197	SA0
30	RESET#	72	CB4	114	ERR_OUT#/NC/ CK1#	156	DQS6	198	NC (EVENT#)

31	DQ10	73	GND	115	VDD	157	DM5	199	VDDSPD
32	GND	74	CB5	116	VDD	158	GND	200	SDA
33	DQ11	75	DQS8#	117	DQS6#	159	DQ42	201	SA1
34	DQ14	76	DM8	118	NC (C3#)	160	DQ46	202	SCL
35	GND	77	DSQ8	119	BA0	161	DQ43	203	V_VTT
36	DQ15	78	GND	120	NC (C2#)	162	DQ47	204	V_VTT
37	DQ16	79	GND	121	WE#	163	GND	205	CASE
38	GND	80	CB6	122	RAS#	164	DQ48	206	CASE
39	DQ17	81	CB2	123	VDD123	165	DQ48		
40	DQ20	82	CB7	124	VDD124	166	DQ52		
41	GND	83	CB3	125	CAS#	167	DQ49		
42	DQ21	84	VREFCA	126	ODT0	168	DQ53		

SODIMM Signals Definition

Table 24: SoDIMM Socket Signal Definition

Signal	Direction	Definition
A[0-15]	Input	SDRAM address bus
BA[0-2]	Input	SDRAM bank select
C[0-1]#	Input	Rank Select Lines 0 & 1
CAS#	Input	SDRAM row address strobe
CB[0-7]	I/O	DIMM ECC check bits
CK0,CK0#	Input	SDRAM differential clock
CKE[0-1]	Input	SDRAM clock enable lines
DM[0-8]	Input	SDRAM data mask
DQ[0-63]	I/O	DIMM memory data bus
DQS[0-8]/#	I/O	SDRAM data strobe
ERR_OUT#	Output (open drain)	Parity error output
GND	-	Power supply return and logic ground.
ODT[0-1]	Input	Register on-die termination control lines
PAR_IN	Input	SDRAM parity onput
RAS#	Input	SDRAM row address strobe
RESET#	Input (LVCMOS)	Reset
SA[0-1]	Input	Address select for I2C device (temperature sensor & SPD EEPROM)
SCL	Input	Serial clock of I2C bus I2C_UC2 (temperature sensor & SPD EEPROM)
SDA	I/O	Serial data of I2C bus I2C_UC2 (temperature sensor & SPD EEPROM)
VDDSPD	Supply	Temperature sensor& SPD EEPROM power supply
VREFCA	Supply	SDRAM command/addres reference voltage
VREFDQ	Supply	SDRAM DQ bus reference voltage
VTT	Supply	Termination supply
WE#	Input	SDRAM write enable

5.3 Rear Connectors

Note about the Ethernet Lanes assignement

The lanes numbering and polarity used for the VPX connectors pin assignment described in this chapter follow the logical numbering that the BCM56760 actually uses.

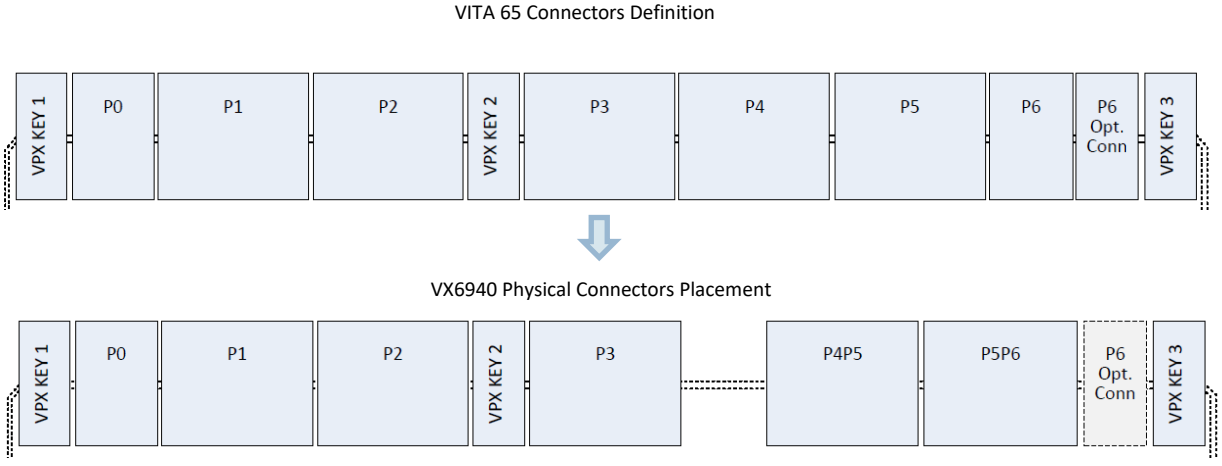
The physical lane swapping and reverse polarities cases which may be documented in other sections of this document or in the VX6940 schematics, are fully compensated by the built-in FastPath firmware portmap settings, so that only natural lane order and polarities presented in this chapter shall be used.

Note about the naming and location of physical VPX connectors on VX6940

The I/O interfaces distribution on the VPX connectors follows the VITA 65 profile MOD6-SWH-14F16U1U15U1J-10.8.1-n as described in section 2.2.4. In this profile, the upper half of P6 is dedicated to an optical connector and the lower half of P6 is a half-size VPX connector.

For clarity, it is worth noting that on VX6940, the lower half of P6 is not a half-size connector but the upper half of a full-size connector named P5P6. Similarly, P5 is made of two halves of P4P5 and P5P6. P4 is not used. This is illustrated in Figure 28. This difference has no impact whatsoever on the product and it is totally transparent to the user. Indeed, the VITA 65 designators are used throughout this document.

Figure 28: Rear Connectors Physical Naming and Location



5.3.1 VPX P0 Connector

Identification

Manufacturer	MPN	Description	4-4 KGS	Function	Port ID	Refdes
TE Connectivity	0-1410189-4	8-wafer, VPX P0, left end connector, RT 2	1053-3022	VPX P0 utility connector	SMBus : SMB0, SMB1	P0

P0 Pin Assignment

Table 25: P0 Pin Assignment

Wafer	Type	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Power	12V (VS1)	12V (VS1)	12V (VS1)	NC (No Pad)	NC (VS2)	NC (VS2)	NC (VS2)
2	Power	12V (VS1)	12V (VS1)	12V (VS1)	NC (No Pad)	NC (VS2)	NC (VS2)	NC (VS2)
3	Power	NC (VS3)	NC (VS3)	NC (VS3)	NC (No Pad)	NC (VS3)	NC (VS3)	NC (VS3)
4	Single-ended	SMB1_CLK (SM2)	SMB1_DAT (SM3)	GND	NC (-12V_AUX)	GND	SYSRESET*	NVMRO
5	Single-ended	GAP	GA4*	GND	NC (3.3V_AUX)	GND	SMB0_CLK (SM0)	SMB0_DAT (SM1)
6	Single-ended	GA3*	GA2*	GND	NC (+12V_AUX)	GND	GA1*	GA0*
7	Differential	TCK	GND	TDO	TDI	GND	TMS	TRST*
8	Differential	GND	NC (REF_CLK-)	NC (REF_CLK+)	GND	NC (AUX_CLK-)	NC (AUX_CLK+)	GND

Note: When the name of a signal differs between VX6940 and standard VITA pinout, the standard pinout name is shown in parentheses.

P0 Signals definition

Table 26: P0 Signals Definition

Signal	Direction	Definition
12V (VS1)	Input	- VITA 46.0 definition: +12V or +48V power rail. - On VX6940, a +12V incoming power rail as defined through 315° alignment key 1.
3.3V_AUX	Input	- VITA 46.0 definition: Mandatory auxiliary 3.3V power rail. - On VX6940, not connected.
SMB0_DAT (SM1)	Bidir	- VITA 46.0 definition: Optional System Management Connection (Data SM1). - On VX6940, data of SMBus SMB0 connected to ShMC.
SMB0_CLK (SM0)	Output	- VITA 46.0 definition: Optional System Management Connection (Clock SM0). - On VX6940, clock of SMBus SMB0 connected to ShMC.
SMB1_DAT (SM3)	Bidir	- VITA 46.0 definition: Optional System Management Connection (Data SM3). - On VX6940, data of SMBus SMB1 connected to ShMC.
SMB1_CLK (SM2)	Output	- VITA 46.0 definition: Optional System Management Connection (Clock SM2). - On VX6940, clock of SMBus SMB1 connected to ShMC.
GA[0..4]*	Input	- VITA 46.0 definition: Geographical address pins . - On VX6940, geographical address routed to ShMC and FPGA.
GAP	Input	- VITA 46.0 definition: Geographical address parity. - On VX6940, geographical address parity routed to ShMC and FPGA.

Signal	Direction	Definition
GND	-	Power supply return and logic ground.
NVMRO	Input	- VITA 46.0 definition: Non-Volatile Memory Read Only. When asserted (logical 1), prevents any non-volatile memory from being updated. Bussed to all slots. - On VX6940, connected to FPGA drives the non-volatile memory write enable controls.
TCK	Input	- VITA 46.0 definition: JTAG TCK. - On VX6940, connected to FPGA and JTAG connector J01501.
TDI	Bidir	- VITA 46.0 definition: JTAG TDI. - On VX6940, connected to FPGA and JTAG connector J01501.
TDO	Bidir	- VITA 46.0 definition: JTAG TDO. - On VX6940, connected to FPGA and JTAG connector J01501.
TMS	Bidir	- VITA 46.0 definition: JTAG TMS. - On VX6940, connected to FPGA and JTAG connector J01501..
TRST*	Bidir	- VITA 46.0 definition: JTAG TRST*. - On VX6940, connected to FPGA and JTAG connector J01501.
SYSRESET*	Bidir	- VITA 46.0 definition: VPX System Reset. Input and open collector output. - On VX6940, handled by FPGA.

Note: When the name of a signal differs between VX6940 and standard VITA pinout, the standard pinout name is shown in parentheses.

5.3.2 VPX P1 Connector

P1 Identification

Manufacturer	MPN	Description	4-4 KGS	Function	Port ID	Refdes
TE Connectivity	2302785-1	Right Angle Plug Assembly, 7 Row, Center, VPX, Multigig RT 3	1066-8074	VPX differential connector	TSCf0, TSCe3, TSCe4, TSCe5 I2C_RTM (def) or COM (opt)	P1

P1 Pin Assignment

Table 27: P1 Pin Assignment

Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	GDISCRETE1	GND	TSCF0_TD0- (DPfp01-T0-)	TSCF0_TD0+ (DPfp01-T0+)	GND	TSCF0_RD0- (DPfp01-R0-)	TSCF0_RD0+ (DPfp01-R0+)
2	GND	TSCF0_TD1- (DPfp01-T1-)	TSCF0_TD1+ (DPfp01-T1+)	GND	TSCF0_RD1- (DPfp01-R1-)	TSCF0_RD1+ (DPfp01-R1+)	GND
3	VBAT	GND	TSCF0_TD2- (DPfp01-T2-)	TSCF0_TD2+ (DPfp01-T2+)	GND	TSCF0_RD2- (DPfp01-R2-)	TSCF0_RD2+ (DPfp01-R2+)
4	GND	TSCF0_TD3- (DPfp01-T3-)	TSCF0_TD3+ (DPfp01-T3+)	GND	TSCF0_RD3- (DPfp01-R3-)	TSCF0_RD3+ (DPfp01-R3+)	GND
5	SYS_CON*	GND	TSCE5_TD0- (DPfp02-T0-)	TSCE5_TD0+ (DPfp02-T0+)	GND	TSCE5_RD0- (DPfp02-R0-)	TSCE5_RD0+ (DPfp02-R0+)
6	GND	TSCE5_TD1- (DPfp02-T1-)	TSCE5_TD1+ (DPfp02-T1+)	GND	TSCE5_RD1- (DPfp02-R1-)	TSCE5_RD1+ (DPfp02-R1+)	GND
7	NC	GND	TSCE5_TD2- (DPfp02-T2-)	TSCE5_TD2+ (DPfp02-T2+)	GND	TSCE5_RD2- (DPfp02-R2-)	TSCE5_RD2+ (DPfp02-R2+)
8	GND	TSCE5_TD3- (DPfp02-T3-)	TSCE5_TD3+ (DPfp02-T3+)	GND	TSCE5_RD3- (DPfp02-R3-)	TSCE5_RD3+ (DPfp02-R3+)	GND
9	def I2C_RTM_SCL opt COM TX	GND	TSCE4_TD0- (DPfp03-T0-)	TSCE4_TD0+ (DPfp03-T0+)	GND	TSCE4_RD0- (DPfp03-R0-)	TSCE4_RD0+ (DPfp03-R0+)
10	GND	TSCE4_TD1- (DPfp03-T1-)	TSCE4_TD1+ (DPfp03-T1+)	GND	TSCE4_RD1- (DPfp03-R1-)	TSCE4_RD1+ (DPfp03-R1+)	GND
11	def I2C_RTM_SDA opt COM RX	GND	TSCE4_TD2- (DPfp03-T2-)	TSCE4_TD2+ (DPfp03-T2+)	GND	TSCE4_RD2- (DPfp03-R2-)	TSCE4_RD2+ (DPfp03-R2+)
12	GND	TSCE4_TD3- (DPfp03-T3-)	TSCE4_TD3+ (DPfp03-T3+)	GND	TSCE4_RD3- (DPfp03-R3-)	TSCE4_RD3+ (DPfp03-R3+)	GND
13	RTM_RST# (Reserved)	GND	TSCE3_TD0- (DPfp04-T0-)	TSCE3_TD0+ (DPfp04-T0+)	GND	TSCE3_RD0- (DPfp04-R0-)	TSCE3_RD0+ (DPfp04-R0+)
14	GND	TSCE3_TD1- (DPfp04-T1-)	TSCE3_TD1+ (DPfp04-T1+)	GND	TSCE3_RD1- (DPfp04-R1-)	TSCE3_RD1+ (DPfp04-R1+)	GND
15	MRST# (Maskable Reset*)	GND	TSCE3_TD2- (DPfp04-T2-)	TSCE3_TD2+ (DPfp04-T2+)	GND	TSCE3_RD2- (DPfp04-R2-)	TSCE3_RD2+ (DPfp04-R2+)
16	GND	TSCE3_TD3- (DPfp04-T3-)	TSCE3_TD3+ (DPfp04-T3+)	GND	TSCE3_RD3- (DPfp04-R3-)	TSCE3_RD3+ (DPfp04-R3+)	GND

Note: When the name of a signal differs between VX6940 and standard VITA pinout, the standard pinout name is shown in parentheses.
Note: "def" and "opt" stand for Default and Option respectively.

P1 Signals Definition

Table 28: P1 Signals definition

Signal	Direction	Definition
GDISCRETE1	Bidir	- VITA 65 definition: General purpose, bussed, open drain signal. - On VX6940, GDISCRETE1 is an open drain output driven by the FPGA and an input to the ShMC (pin GPIOG7/SGPS2I1/SALT4) which can also be used as an SMB ALERT#.
GND	-	Power supply return and logic ground.
MRST# (Maskable Reset*)	Input	- VITA 65 definition: Maskable Reset*. - On VX6940, P1_MASKABLERESET# is handled by the FPGA.
RTM_RST# (Reserved)	Output	- VITA 65 definition: Reserved. - On VX6940: RESET# input for RTM driven by the FPGA.
def SW_BSC_REAR_SCL or opt COM1_RS232_TX# (MP01-TD)	Output	- VITA 65 definition: Serial TXD. - On VX6940, depending on configuration: . Default: clock of I2C bus I2C_RTM . Option: TXD signal of COM serial port (EIA-232).
def SW_BSC_REAR_SDA or opt COM1_RS232_RX# (MP01-RD)	Bidir/Input	- VITA 65 definition: Serial RXD. - On VX6940, depending on configuration: . Default: data of I2C bus I2C_RTM . Option: RXD signal of COM serial port (EIA-232).
SYS_CON*	Input	- VITA 65 definition: VPX system controller designator - On VX6940, routed to FPGA
TSCE/Fa_RDb+/- (DPfpx-Ry+/-)	Input	- VITA 65 definition: DPfpx: Fat Pipe Data Plane x with x = 01 to 12. Ry+/- : Receive pair y within this Fat Pipe with y = 0 to 3. - VX6940 definition (as per BCM56760 datasheet): TSCEa : SerDes Link TSCE number a with a = 0 to 13 TSCFa : SerDes Link TSCF number a with a = 0 to 3 RDb+/- : Receive pair b with b = 0 to 3.
TSCE/Fa_TDb+/- (DPfpx-Ty+/-)	Output	- VITA 65 definition: DPfpx: Fat Pipe Data Plane x with x = 01 to 12. Ty+/- : Transmit pair y within this Fat Pipe with y = 0 to 3. - VX6940 definition (as per BCM56760 datasheet): TSCEa : SerDes Link TSCE number a with a = 0 to 13 TSCFa : SerDes Link TSCF number a with a = 0 to 3 TDb+/- : Transmit pair b with b = 0 to 3.
VBAT	Input	- VITA 65 definition: Battery Voltage Input, 3V. Alternate source from VPX backplane for RTC backup voltage. - Same definition on VX6940

Note: When the name of a signal differs between VX6940 and standard VITA pinout, the standard pinout name is shown in parentheses.
Note: "def" and "opt" stand for Default and Option respectively.

5.3.3 VPX P2 Connector

P2 Identification

Manufacturer	MPN	Description	4-4 KGS	Function	Port ID	Refdes
TE Connectivity	2302785-1	Right Angle Plug Assembly, 7 Row, Center, VPX, Multigig RT 3	1066-8074	VPX differential connector	TSCe2, TSCe6, TSCe12, TSCe13 RTM MDC/MDIO, RTM LED bus	P2

P2 Pin Assigment

Table 29: P2 Pin Assignment

Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	NC	GND	TSCE6_TD0- (DPfp05-T0-)	TSCE6_TD0+ (DPfp05-T0+)	GND	TSCE6_RD0- (DPfp05-R0-)	TSCE6_RD0+ (DPfp05-R0+)
2	GND	TSCE6_TD1- (DPfp05-T1-)	TSCE6_TD1+ (DPfp05-T1+)	GND	TSCE6_RD1- (DPfp05-R1-)	TSCE6_RD1+ (DPfp05-R1+)	GND
3	NC	GND	TSCE6_TD2- (DPfp05-T2-)	TSCE6_TD2+ (DPfp05-T2+)	GND	TSCE6_RD2- (DPfp05-R2-)	TSCE6_RD2+ (DPfp05-R2+)
4	GND	TSCE6_TD3- (DPfp05-T3-)	TSCE6_TD3+ (DPfp05-T3+)	GND	TSCE6_RD3- (DPfp05-R3-)	TSCE6_RD3+ (DPfp05-R3+)	GND
5	NC	GND	TSCE2_TD0- (DPfp06-T0-)	TSCE2_TD0+ (DPfp06-T0+)	GND	TSCE2_RD0- (DPfp06-R0-)	TSCE2_RD0+ (DPfp06-R0+)
6	GND	TSCE2_TD1- (DPfp06-T1-)	TSCE2_TD1+ (DPfp06-T1+)	GND	TSCE2_RD1- (DPfp06-R1-)	TSCE2_RD1+ (DPfp06-R1+)	GND
7	NC	GND	TSCE2_TD2- (DPfp06-T2-)	TSCE2_TD2+ (DPfp06-T2+)	GND	TSCE2_RD2- (DPfp06-R2-)	TSCE2_RD2+ (DPfp06-R2+)
8	GND	TSCE2_TD3- (DPfp06-T3-)	TSCE2_TD3+ (DPfp06-T3+)	GND	TSCE2_RD3- (DPfp06-R3-)	TSCE2_RD3+ (DPfp06-R3+)	GND
9	SW_XG_MDC (Reserved)	GND	TSCE12_TD0- (DPfp07-T0-)	TSCE12_TD0+ (DPfp07-T0+)	GND	TSCE12_RD0- (DPfp07-R0-)	TSCE12_RD0+ (DPfp07-R0+)
10	GND	TSCE12_TD1- (DPfp07-T1-)	TSCE12_TD1+ (DPfp07-T1+)	GND	TSCE12_RD1- (DPfp07-R1-)	TSCE12_RD1+ (DPfp07-R1+)	GND
11	SW_XG_MDIO (Reserved)	GND	TSCE12_TD2- (DPfp07-T2-)	TSCE12_TD2+ (DPfp07-T2+)	GND	TSCE12_RD2- (DPfp07-R2-)	TSCE12_RD2+ (DPfp07-R2+)
12	GND	TSCE12_TD3- (DPfp07-T3-)	TSCE12_TD3+ (DPfp07-T3+)	GND	TSCE12_RD3- (DPfp07-R3-)	TSCE12_RD3+ (DPfp07-R3+)	GND
13	SW_LED_DATA (Reserved)	GND	TSCE13_TD0- (DPfp08-T0-)	TSCE13_TD0+ (DPfp08-T0+)	GND	TSCE13_RD0- (DPfp08-R0-)	TSCE13_RD0+ (DPfp08-R0+)
14	GND	TSCE13_TD1- (DPfp08-T1-)	TSCE13_TD1+ (DPfp08-T1+)	GND	TSCE13_RD1- (DPfp08-R1-)	TSCE13_RD1+ (DPfp08-R1+)	GND
15	SW_LED_CLK (Reserved)	GND	TSCE13_TD2- (DPfp08-T2-)	TSCE13_TD2+ (DPfp08-T2+)	GND	TSCE13_RD2- (DPfp08-R2-)	TSCE13_RD2+ (DPfp08-R2+)
16	GND	TSCE13_TD3- (DPfp08-T3-)	TSCE13_TD3+ (DPfp08-T3+)	GND	TSCE13_RD3- (DPfp08-R3-)	TSCE13_RD3+ (DPfp08-R3+)	GND

Note: When the name of a signal differs between VX6940 and standard VITA pinout, the standard pinout name is shown in parentheses.

P2: Signals Definition

Table 30: P2 Signals definition

Signal	Direction	Definition
GND	-	Power supply return and logic ground.
TSCEa_RDb+/- (DPfpx-Ry+/-)	Input	- VITA 65 definition: DPfpx: Fat Pipe Data Plane x with x = 01 to 12. Ry+/- : Receive pair y within this Fat Pipe with y = 0 to 3. - VX6940 definition (as per BCM56760 datasheet): TSCEa : SerDes Link TSCE number a with a = 0 to 13 RDb+/- : Receive pair b with b = 0 to 3.
TSCEa_TDb+/- (DPfpx-Ty+/-)	Output	- VITA 65 definition: DPfpx: Fat Pipe Data Plane x with x = 01 to 12. Ty+/- : Transmit pair y within this Fat Pipe with y = 0 to 3. - VX6940 definition (as per BCM56760 datasheet): TSCEa : SerDes Link TSCE number a with a = 0 to 13 TDb+/- : Transmit pair b with b = 0 to 3.
SW_XG_MDC/MDIO (Reserved)	Bidir / Output	- VITA 65 definition: Reserved - VX6940 definition: MDC/MDIO bus to the RTM.
SW_LED_DATA/CLK (MP01-RD)	Bidir / Input	- VITA 65 definition: Reserved - VX6940 definition: Data and clock of LED bus to RTM.

5.3.4 VPX P3 Connector

P3 Identification

Manufacturer	MPN	Description	4-4 KGS	Function	Port ID	Refdes
TE Connectivity	2302785-1	Right Angle Plug Assembly, 7 Row, Center, VPX, Multigig RT 3	1066-8074	VPX differential connector	TSCe0, TSCe1, TSCe11, TSCf3 Rear ETH1	P3

P3 Pin Assignment

Table 31: P3 Pin Assignment

Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	ETH1_P3_MDI0_- (DPtp01-DA-)	GND	TSCE1_TD0- (DPfp09-T0-)	TSCE1_TD0+ (DPfp09-T0+)	GND	TSCE1_RD0- (DPfp09-R0-)	TSCE1_RD0+ (DPfp09-R0+)
2	GND	TSCE1_TD1- (DPfp09-T1-)	TSCE1_TD1+ (DPfp09-T1+)	GND	TSCE1_RD1- (DPfp09-R1-)	TSCE1_RD1+ (DPfp09-R1+)	GND
3	ETH1_P3_MDI0_+ (DPtp01-DA+)	GND	TSCE1_TD2- (DPfp09-T2-)	TSCE1_TD2+ (DPfp09-T2+)	GND	TSCE1_RD2- (DPfp09-R2-)	TSCE1_RD2+ (DPfp09-R2+)
4	GND	TSCE1_TD3- (DPfp09-T3-)	TSCE1_TD3+ (DPfp09-T3+)	GND	TSCE1_RD3- (DPfp09-R3-)	TSCE1_RD3+ (DPfp09-R3+)	GND
5	ETH1_P3_MDI1_- (DPtp01-DB-)	GND	TSCE0_TD0- (DPfp10-T0-)	TSCE0_TD0+ (DPfp10-T0+)	GND	TSCE0_RD0- (DPfp10-R0-)	TSCE0_RD0+ (DPfp10-R0+)
6	GND	TSCE0_TD1- (DPfp10-T1-)	TSCE0_TD1+ (DPfp10-T1+)	GND	TSCE0_RD1- (DPfp10-R1-)	TSCE0_RD1+ (DPfp10-R1+)	GND
7	ETH1_P3_MDI1_+ (DPtp01-DB+)	GND	TSCE0_TD2- (DPfp10-T2-)	TSCE0_TD2+ (DPfp10-T2+)	GND	TSCE0_RD2- (DPfp10-R2-)	TSCE0_RD2+ (DPfp10-R2+)
8	GND	TSCE0_TD3- (DPfp10-T3-)	TSCE0_TD3+ (DPfp10-T3+)	GND	TSCE0_RD3- (DPfp10-R3-)	TSCE0_RD3+ (DPfp10-R3+)	GND
9	ETH1_P3_MDI2_- (DPtp01-DC-)	GND	TSCE11_TD0- (DPfp11-T0-)	TSCE11_TD0+ (DPfp11-T0+)	GND	TSCE11_RD0- (DPfp11-R0-)	TSCE11_RD0+ (DPfp11-R0+)
10	GND	TSCE11_TD1- (DPfp11-T1-)	TSCE11_TD1+ (DPfp11-T1+)	GND	TSCE11_RD1- (DPfp11-R1-)	TSCE11_RD1+ (DPfp11-R1+)	GND
11	ETH1_P3_MDI2_+ (DPtp01-DC+)	GND	TSCE11_TD2- (DPfp11-T2-)	TSCE11_TD2+ (DPfp11-T2+)	GND	TSCE11_RD2- (DPfp11-R2-)	TSCE11_RD2+ (DPfp11-R2+)
12	GND	TSCE11_TD3- (DPfp11-T3-)	TSCE11_TD3+ (DPfp11-T3+)	GND	TSCE11_RD3- (DPfp11-R3-)	TSCE11_RD3+ (DPfp11-R3+)	GND
13	ETH1_P3_MDI3_- (DPtp01-DD-)	GND	TSCF3_TD0- (DPfp12-T0-)	TSCF3_TD0+ (DPfp12-T0+)	GND	TSCF3_RD0- (DPfp12-R0-)	TSCF3_RD0+ (DPfp12-R0+)
14	GND	TSCF3_TD1- (DPfp12-T1-)	TSCF3_TD1+ (DPfp12-T1+)	GND	TSCF3_RD1- (DPfp12-R1-)	TSCF3_RD1+ (DPfp12-R1+)	GND
15	ETH1_P3_MDI3_+ (DPtp01-DD+)	GND	TSCF3_TD2- (DPfp12-T2-)	TSCF3_TD2+ (DPfp12-T2+)	GND	TSCF3_RD2- (DPfp12-R2-)	TSCF3_RD2+ (DPfp12-R2+)
16	GND	TSCF3_TD3- (DPfp12-T3-)	TSCF3_TD3+ (DPfp12-T3+)	GND	TSCF3_RD3- (DPfp12-R3-)	TSCF3_RD3+ (DPfp12-R3+)	GND

Note: When the name of a signal differs between VX6940 and standard VITA pinout, the standard pinout name is shown in parentheses.

P3 Signals Definition

Table 32: P3 Signals Definition

Signal	Direction	Definition
GND	-	Power supply return and logic ground.
TSCE/Fa_RDb+/- (DPfpx-Ry+/-)	Input	- VITA 65 definition: DPfpx: Fat Pipe Data Plane x with x = 01 to 12. Ry+/- : Receive pair y within this Fat Pipe with y = 0 to 3. - VX6940 definition (as per BCM56760 datasheet): TSCEa : SerDes Link TSCE number a with a = 0 to 13 TSCFa : SerDes Link TSCF number a with a = 0 to 3 RDb+/- : Receive pair b with b = 0 to 3.
TSCE/Fa_TDb+/- (DPfpx-Ty+/-)	Output	- VITA 65 definition: DPfpx: Fat Pipe Data Plane x with x = 01 to 12. Ty+/- : Transmit pair y within this Fat Pipe with y = 0 to 3. - VX6940 definition (as per BCM56760 datasheet): TSCEa : SerDes Link TSCE number a with a = 0 to 13 TSCFa : SerDes Link TSCF number a with a = 0 to 3 TDb+/- : Transmit pair b with b = 0 to 3.
ETH1_P3_MDIx_+/- (DPtp01-Dy+/-)	Bidir	- VITA 65 definition: DPtp01: Data Plane Thin Pipe #01 Dx+/- : Pair Dx with x = A, B, C, D - VX6940 definition : ETH1_P3_MDIx_+/- : 1000BASE-T ETH1 data port, differential pair TMDIx with x = 0 to 3 SA, RA, WA Classes: Port routed through LAN switch to either front RJ45 (default) or to rear P3. RC Class: Port routed to rear P3 only.

5.3.5 VPX P4 Connector

P4 is not used on VX6940.

5.3.6 VPX P5 Connector

P5 Identification

Manufacturer	MPN	Description	4-4 KGS	Function	Port ID	Refdes
TE Connectivity	2302785-1	Right Angle Plug Assembly, 7 Row, Center, VPX, Multigig RT 3	1066-8074	VPX differential connector	TSCe7.0, TSCe7.1 TSCe8.0, TSCE8.3 TSCe10.0, TSCe10.1, TSCe10.2	P4P5 (1)

(1) P5 is physically made of the upper half of P4P5 and the lower half of P5P6. Refer to note at the beginning of chapter 5.3.

P5 Pin Assignment

Table 33: P5 Pin Assignment

Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	NC	GND	NC	NC	GND	NC	NC
2	GND	NC	NC	GND	NC	NC	GND
3	NC	GND	NC	NC	GND	NC	NC
4	GND	NC	NC	GND	NC	NC	GND
5	NC	GND	NC	NC	GND	NC	NC
6	GND	NC	NC	GND	NC	NC	GND
7	NC	GND	NC	NC	GND	NC	NC
8	GND	NC	NC	GND	NC	NC	GND
9	GND	GND	GND	GND	GND	GND	GND
10	GND	TSCE8_TD0- (CPutp01-T-)	TSCE8_TD0+ (CPutp01-T+)	GND	TSCE8_RD0- (CPutp01-R-)	TSCE8_RD0+ (CPutp01-R+)	GND
11	COM1 TXD	GND	TSCE8_TD3- (CPutp02-T-)	TSCE8_TD3+ (CPutp02-T+)	GND	TSCE8_RD3- (CPutp02-R-)	TSCE8_RD3+ (CPutp02-R+)
12	GND	TSCE7_TD0- (CPutp03-T-)	TSCE7_TD0+ (CPutp03-T+)	GND	TSCE7_RD0- (CPutp03-R-)	TSCE7_RD0+ (CPutp03-R+)	GND
13	COM1 RXD	GND	TSCE7_TD1- (CPutp04-T-)	TSCE7_TD1+ (CPutp04-T+)	GND	TSCE7_RD1- (CPutp04-R-)	TSCE7_RD1+ (CPutp04-R+)
14	GND	TSCE10_TD0- (CPutp05-T-)	TSCE10_TD0+ (CPutp05-T+)	GND	TSCE10_RD0- (CPutp05-R-)	TSCE10_RD0+ (CPutp05-R+)	GND
15	NC	GND	TSCE10_TD1- (CPutp06-T-)	TSCE10_TD1+ (CPutp06-T+)	GND	TSCE10_RD1- (CPutp06-R-)	TSCE10_RD1+ (CPutp06-R+)
16	GND	TSCE10_TD2- (CPutp07-T-)	TSCE10_TD2+ (CPutp07-T+)	GND	TSCE10_RD2- (CPutp07-R-)	TSCE10_RD2+ (CPutp07-R+)	GND

Note: When the name of a signal differs between VX6940 and standard VITA pinout, the standard pinout name is shown in parentheses.

P5 Signals Definition

Table 34: P5 Signals definition

Signal	Direction	Definition
GND	-	Power supply return and logic ground.
COM1 TXD	Output	EIA-232 Transmit Data of port COM
COM1 RXD	Input	EIA-232 Receive Data of port COM
TSCEa_RDb+/- (CPutpx-R+/-)	Input	- VITA 65 definition: CPutpx: Ultra Thin Pipe Control Plane x with x = 01 to 07. R+/- : Receive pair y within this Ultra Thin Pipe. - VX6940 definition (as per BCM56760 datasheet): TSCEa : SerDes Link TSCE number a with a = 0 to 13 RDb+/- : Receive pair b with b = 0 to 3.
TSCEa_TDb+/- (CPutpx-T+/-)	Output	- VITA 65 definition: CPutpx: Ultra Thin Pipe Control Plane x with x = 01 to 07. T+/- : Receive pair y within this Ultra Thin Pipe. - VX6940 definition (as per BCM56760 datasheet): TSCEa : SerDes Link TSCE number a with a = 0 to 13 TDb+/- : Transmit pair b with b = 0 to 3.

5.3.7 VPX P6 Connector

P6 Identification

Manufacturer	MPN	Description	4-4 KGS	Function	Port ID	Refdes
TE Connectivity	2302785-1	Right Angle Plug Assembly, 7 Row, Center, VPX, Multigig RT 3	1066-8074	VPX differential connector	TSCe10.3 Rear ETH0	P5P6 (1)

(1) VITA P6 is physically made of the upper half of P5P6. Refer to note at the beginning of chapter 5.3.

P6 Pin Assignment

Table 35: P6 Pin Assignment

Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	ETH0_P6_MDI0_- (CPext01-T-)	GND	TSCE10_TD3- (CPutp08-T-)	TSCE10_TD3+ (CPutp08-T+)	GND	TSCE10_RDC3- (CPutp08-R-)	TSCE10_RDC3+ (CPutp08-R+)
2	GND	NC	NC	GND	NC	NC	GND
3	ETH0_P6_MDI0_+ (CPext01-T+)	GND	NC	NC	GND	NC	NC
4	GND	NC	NC	GND	NC	NC	GND
5	ETH0_P6_MDI1_- (CPext01-R-)	GND	NC	NC	GND	NC	NC
6	GND	NC	NC	GND	NC	NC	GND
7	ETH0_P6_MDI1_+ (CPext01-R+)	GND	NC	NC	GND	NC	NC
8	GND	NC	NC	GND	NC	NC	GND

Note: When the name of a signal differs between VX6940 and standard VITA pinout, the standard pinout name is shown in parentheses.

P6 Signals Definition

Table 36: P6 Signals Definition

Signal	Direction	Definition
GND	-	Power supply return and logic ground.
TSCE10_RD3+/- (CPutp08-R+/-)	Input	- VITA 65 definition: CPutp08: Ultra Thin Pipe Control Plane 08, R+/- : Receive pair. - VX6940 definition (as per BCM56760 datasheet): TSCE10 : SerDes link TSCe10, RD3+/- : Receive pair of lane 3.
TSCE10_TD3+/- (CPutp08-T+/-)	Output	- VITA 65 definition: CPutp08: Ultra Thin Pipe Control Plane 08, R+/- : Transmit pair. - VX6940 definition (as per BCM56760 datasheet): TSCE10 : SerDes link TSCe10, TD3+/- : Transmit pair of lane 3.
ETH0_P6_MDI0_+/- (CPext01-T+/-)	Output	- VITA 65 definition: CPext01: Control Plane Ext Thin Pipe #01, T+/- : Transmit pair. - VX6940 definition : ETH0_P6_MDI0_+/- : 100BASE-TX management port ETH0 transmit pair. SA, RA, WA Classes: Port routed through LAN switch to either front RJ45 (default) or to rear P6. RC Class: Port routed to rear P6 only
ETH0_P6_MDI1_+/- (CPext01-R+/-)	Input	- VITA 65 definition: CPext01: Control Plane Ext Thin Pipe #01, R+/- : Receive Pair. - VX6940 definition : ETH0_P6_MDI1_+/- : 100BASE-TX management port ETH0 receive pair. SA, RA, WA Classes: Port routed through LAN switch to either front RJ45 (default) or to rear P6. RC Class: Port routed to rear P6 only.

5.4 LEDs

Status LEDs on front panel

There are four LEDs on the front panel numbered L1 to L4 from left to right.

Figure 29: Front Panel Status LEDs

Status LEDs States

Table 37: LEDs states

Symbol	State Description
X	LED OFF
R / B	Steady / Blinking Red
G / B	Steady / Blinking Green
A / B	Steady / Blinking Amber (both Red and Green)
Y / B	Steady / Blinking Yellow

Status LEDs Meaning

Table 38: LEDs meaning

LED1	LED2	LED3	LED4	Control	Meaning
X	X	X	X		Permanent system error. Board not functional
X				ShMC	Status: Board functional.
A				ShMC	Status: Warning.
R				ShMC	Status: Critical.
G				ShMC	Reserved.
	G			FPGA	Power is ON.
	Bs			FPGA	Blinking slow : Board in SUSPEND state : PAYLOAD domain supplies are OFF. Blink: 100ms every 2s.
	Bf			FPGA	Blinking fast : Power Error. The number of flashes codes the failing power supply. Sequence: n flashes 200 ms ON / 200 ms OFF followed by 1 s OFF.
		G		FPGA	Board held in reset. PAYLOAD domain supplies are ON.
		X		FPGA	Board is NOT in reset state.
			Y	ShMC	TBD
			G	ShMC	TBD
			X	ShMC	TBD

- **QSFP LEDs**

Table 39: QSFP LEDs

LED QSFP 1/2/3	Control	Meaning
X	FPGA	No Link
B	FPGA	Activity. Speed 10G/40G/100G.
G	FPGA	Link established. No activity.

5.5 Reset Push-Button

- **Identification**

Manufacturer	MPN	Description	4-4 KGS	Function	Port ID	Refdes
C&K	KMS231GPLFS	Switch Tactile N.O. SPST Rectangular Button Gull Wing 0.05A 32VDC 1VA 100000Cycles 3N SMD -40°C to 85°C	1065-0577	Local Reset (when pressed for less than 4 sec.) Power On/Off (when pressed for more than 4 sec.)	BTN_RST#	SW1

The front Push-button SW1 has two functions:

- Reset: when pressed for less than 4 sec, the FPGA will issue a local reset.
- Power on/off: when pressed for more than 4 sec. the FPGA will start or shut odwn the board. Please not that shutdown is immediate and brutal.

6 Electrical Specifications

6.1. Input Power Rail VS1

VS1 Specification

The VX6940 is powered by the VPX +12V rail VS1. This supply should comply to the following:

- Voltage: 12V +/- 5% (11.4V to 12.6V) inclusive of ripple (VITA 46.0).
- Power on: monotonic rise time, 20 to 125 ms.
- Power off: no undershoot below 0V (VITA 46.0) and a level of 0V maintained at least one second before the next power on.

VS1 Protection

The VS1 input power rails is protected by fuse as described in Table 40.

To prevent safety hazards, the chassis power supply must not exceed the Voltage Rating and Interrupt Rating of the fuse.

Table 40: VS1 Protection

Power rail	VS1
Location	P0
Voltage	+12 V
Protection	Non resettable fuse
Rated current	12 A
Typical melt I^2T	20.341 A^2s
Voltage rating	32 V
Interrupting rating	150 A @ 32VDC
Manufacturer / PN	Littelfuse / 0501012.WR or equivalent

6.2. Input Power Rail +3.3V_AUX

The VPX +3.3V_AUX rail is not used on VX6940.

6.3. VBAT

VBAT Specification

Voltage: 3.0 V typical, 2.55 V minimum, 3.5 V maximum (VITA 46.0).

The VPX VBAT rail takes over onboard battery to power the PCF85063A RTC when the battery is not available.

6.4. Voltage Monitoring

The incoming +12V VS1 rail and the internal power rails are multiplexed and monitored through the ShMC A/D converter.

Table 41: Voltage Monitoring

Voltage Sensor ID	Domain	Voltage	Monitoring Controller	Default IMPI Thresholds	Line Commands
VS1	Incoming VPX	+12 V	ShMC, ADC0, 1		ShMC> sensor
VSDXC	PAYLOAD	+3.3 V	ShMC, ADC0, 0		ShMC> sensor
5V SUS	SUSPEND	+5 V	ShMC, ADC1, 1		ShMC> sensor
VTT DDR	PAYLOAD	+0.675 V	ShMC, ADC1, 0		ShMC> sensor
3V3 SUS	SUSPEND	+3.3 V	ShMC, ADC2, 1		ShMC> sensor
3V3	PAYLOAD	+3.3 V	ShMC, ADC2, 0		ShMC> sensor
2V5 SUS	SUSPEND	+2.5 V	ShMC, ADC3, 1		ShMC> sensor
1V8 SUS	SUSPEND	+1.8 V	ShMC, ADC4, 1		ShMC> sensor
1V8	PAYLOAD	+1.8 V	ShMC, ADC4, 0		ShMC> sensor
1V35 SUS	SUSPEND	+1.35 V	ShMC, ADC5, 1		ShMC> sensor
1V35	PAYLOAD	+1.35 V	ShMC, ADC5, 0		ShMC> sensor
1V2 SUS	SUSPEND	+1.2 V	ShMC, ADC6, 1		ShMC> sensor
3V3 MDIO	PAYLOAD	+3.3 V	ShMC, ADC6, 0		ShMC> sensor
12V SUS	SUSPEND	+12 V	ShMC, ADC7, 1		ShMC> sensor
1V15 SUS	SUSPEND	+1.25 V	ShMC, ADC7, 0		ShMC> sensor
1V25 ANA	SUSPEND	+1.25 V	ShMC, ADC9		ShMC> sensor
1V0 UC	PAYLOAD	+1.0 V	ShMC, ADC10		ShMC> sensor
1V0 IMON	PAYLOAD	+1.0 V	ShMC, ADC11		ShMC> sensor
1V0 ANA IMON	PAYLOAD	+1.0 V	ShMC, ADC12		ShMC> sensor
1V0 Core	PAYLOAD	+1.0 V	ShMC, ADC13		ShMC> sensor
1V0 ANA	PAYLOAD	+1.0 V	ShMC, ADC14		ShMC> sensor
VBAT	Incoming VPX SUSPEND	+12V	ShMC, ADC15		ShMC> sensor

7 Power and Thermal Management

7.1 Power Consumption Specification

Table 42: VX6940 Power Consumption

VX6940-SA-00A00	Continuous Current	Continuous Power	Test Conditions
Typical	4.3 A @ 12V	52 W	Full load.
Maximum	5.8A @ 12V	70 W (1)	Full load. Worst case.

(1) This figure is intended to help the user design the power supplies for his chassis. Kontron thermal qualification was based on typical full-load power consumption (52 W).

7.2 Temperature Monitoring

Overview of the temperature sensors

The VX6940 temperature sensors are listed in Table 45.

Table 43: VX6940 Temperature Sensors

Temperature Sensor ID	Target or Location	Monitoring Device	Monitoring Controller	Default IMPI Thresholds	Line Commands
Temp Board	Board	TMP423 (U13) Accuracy +/- 1.5°C	ShMC, I2C #2 (I2C_TEMP)	lcr: -41°C unc: 71°C ucr: 86°C unr: not set	ShMC> sensor Fastpath: show sensors all UC: ipmitool
Temp UC	T1042 Unit Computer die	TMP423 (U13) Accuracy +/- 1°C	ShMC, I2C #2 (I2C_TEMP)	lcr: -1°C unc: 71°C ucr: 86°C unr: 106°C	ShMC> sensor Fastpath: show sensors all UC: ipmitool
Temp ShMC PCB	Thermal diode under ShMC	TMP423 (U13) Accuracy +/- 1°C	ShMC, I2C #2 (I2C_TEMP)	lcr: -1°C unc: 71°C ucr: 86°C unr: not set	ShMC> sensor Fastpath: show sensors all UC: ipmitool
Temp Switch PCB	Thermal diode under BCM56760 switch	TMP423 (U13) Accuracy +/- 1°C	ShMC, I2C #2 (I2C_TEMP)	lcr: -1°C unc: 76°C ucr: 91°C unr: 101°C	ShMC> sensor Fastpath: show sensors all UC: ipmitool
Temp Switch	BCM56760 switch die	BCM56760 switch	BCM56760 switch	lcr: -1°C unc: 93°C ucr: 111°C unr: 124°C	ShMC> sensor Fastpath: show sensors all UC: ipmitool BCM.0> show Temp
Temp QSFP 1 Temp QSFP 2 Temp QSFP 3	QSFP cage #1 or #2 or #3	QSFP Transceiver sensor	BCM56760 switch (I2C_XG multiplexed into I2C_QSFP1/2/3)	lcr: -1°C unc: 59°C ucr: 71°C unr: not set	ShMC> sensor Fastpath: show fiber-ports optical-transceiver all UC: ipmitool
Temp SODIMM	SODIMM	SODIMM Sensor	UC ShMC	lcr: -1°C unc: 80°C ucr: 96°C unr: not set	ShMC> sensor Fastpath: show fiber-ports optical-transceiver all UC: ipmitool

Figure 30: VX6940 Thermal Sensors (Top Side)

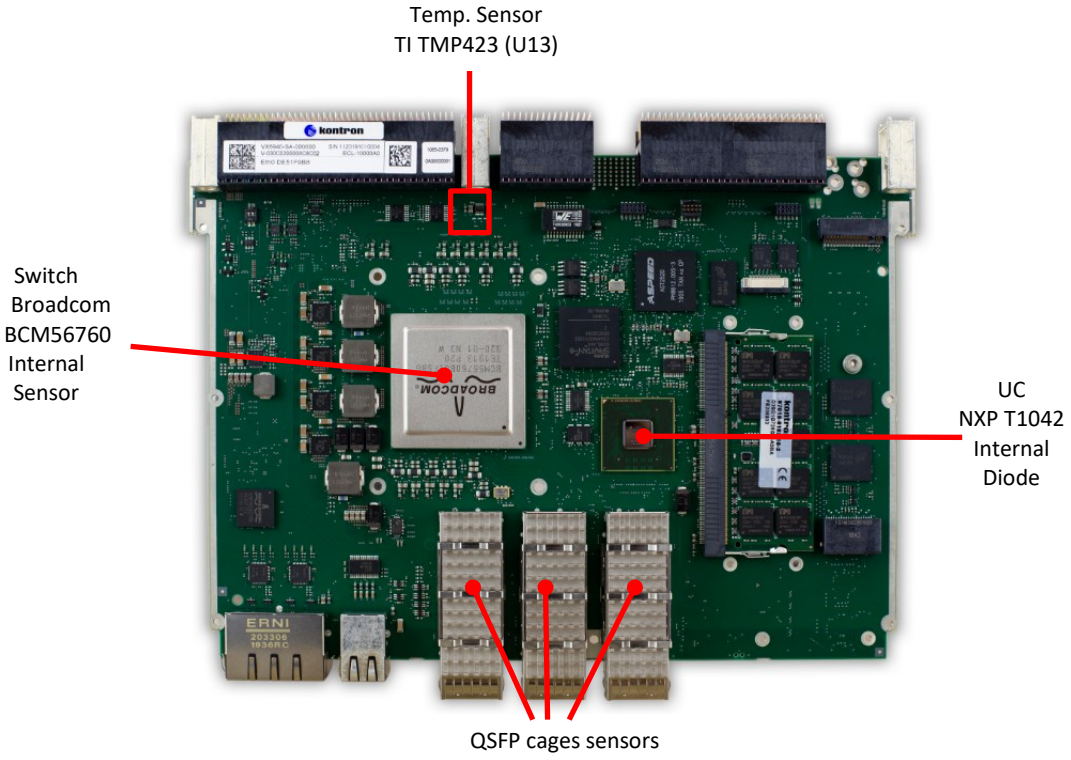
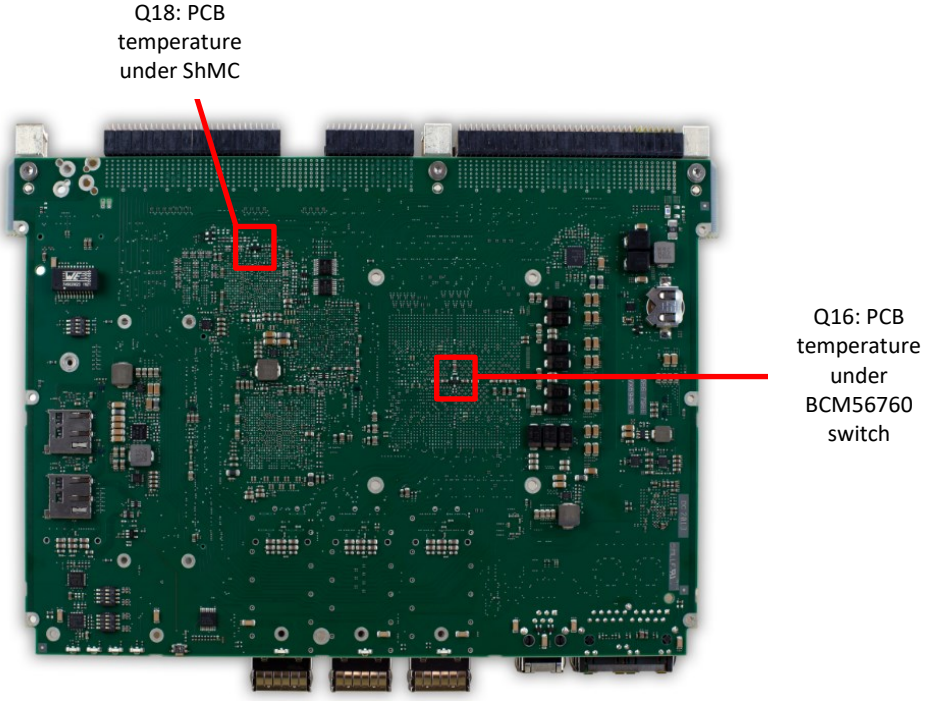


Figure 31: VX6940 Thermal Sensors (Bottom Side)



TMP423 sensor: board temperature, internal UC temperature, PCB temperatures under the switch & ShMC

The Texas Instruments TMP423s feature one internal temperature sensor with a +/-1.5°C accuracy and three remote temperature monitors with a +/-1°C accuracy. The three remote temperature monitors are connected to the UC internal temperature diode, a transistor located under the BCM56760 switch for PCB temperature measurement and a transistor located under the ShMC for PCB temperature measurement.

The TMP423 can be accessed through ShMC I2C #1 (bus I2C_TEMP) at address 0x4C (7-bit).

T1042 Unit Computer Temperature Diode

The T1042 UC features an internal temperature diode which is connected to the TMP423 sensor.

Temperature range: 80°C - 105°C.

BCM56760 Switch Temperature Monitor

The BCM56760 features an internal temperature monitor.

QSFP Cages

The transceivers of the QSFP cages can be accessed through the BCM56760 I2C bus # 1 (named I2C_GX). Refer to the transceiver documentation for the sensor characteristics.

Temperature Thresholds Modification

Six thresholds are defined in the ShMC:

- lnr = lower non-recoverable
- lcr = lower critical
- lnc =lower non-critical
- unc = upper non critical
- ucr = upper critical
- unr = upper non recoverable

The sensors may be listed through command

```
# ipmitool sensor list
```

or

```
# ipmitool -m 0xSN sensor list
```

with slot number SN = (0xB0 + 2*Slot_num). For example : slot 0=0xB0, slot 1 = 0xB2,...

The sensor value may be changed through command such as

```
# ipmitool -m 0xB4 sensor thresh "S02:Temp Board" ucr 105
# ipmitool -m 0xB4 sensor thresh "S02:Temp Board" unr 115
```

with unr > ucr.

Note: The change is not stored in non-volatile memory.

The new value may be checked through command

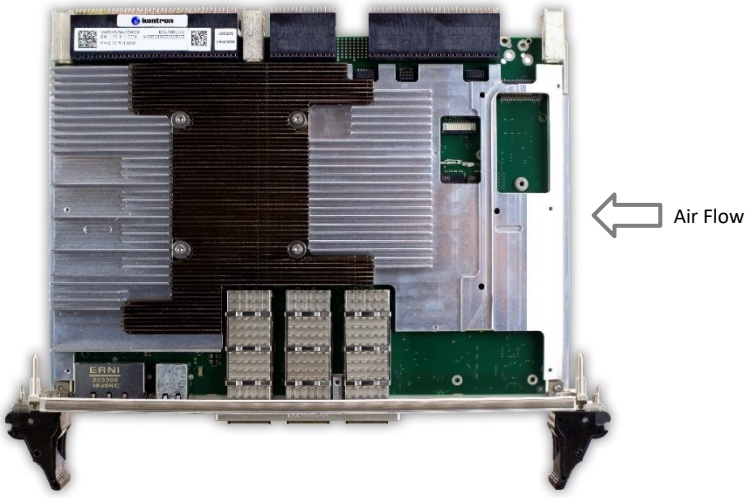
```
# ipmitool -m 0xB4 get "S02:Temp Board" -vvvvv
```

7.3 Air Flow Specification

Air Flow Direction

The VPX standard defines air flow direction from right to left (or bottom to top) as shown on Figure 31.

Figure 32: Air Flow Direction



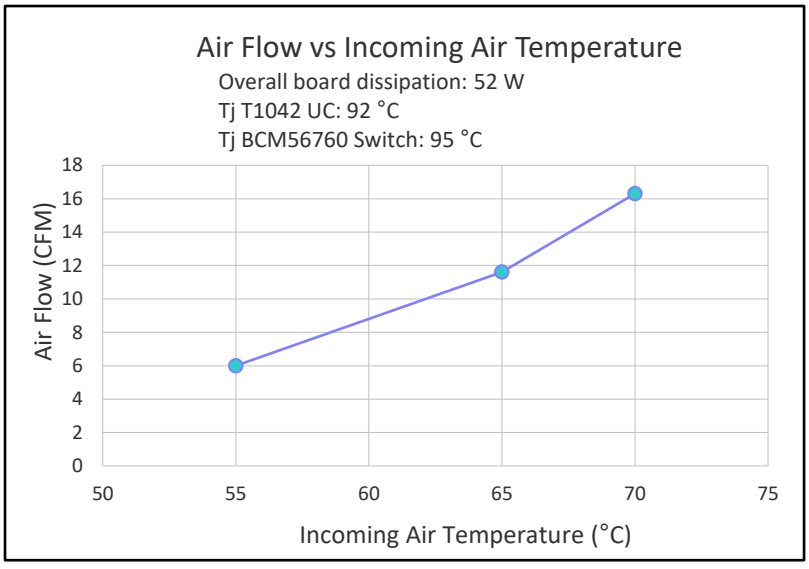
Thermal Operating Points

Figure 33 shows three thermal operating points defined as air flow vs incoming air temperature for the three environment classes: SA class (55°C), WA class (65°C) and RA class (70°C).

In this 52 W scenario, the air flow has been set to grant the two main components, the UC and the Ethernet switch, a margin of 13 °C and 15 °C with respect to their specified maximum junction temperature :

- T1042 UC: Tj = 92°C (max specified: 105°C)
- BC56760 switch: Tj = 95°C (max specified: 110°C).

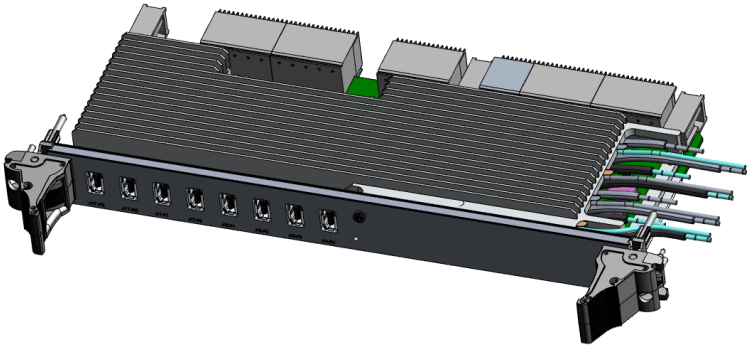
Figure 33: Thermal Operating Points at 52W for SA, WA and RA Classes



8 MPO Rear Transition Module

The Rear Transition Module (RTM) RTM-EZVX6940-MPO is not the only one which has been designed for VX6940. For the sake of brevity this RTM is referred to as MPO RTM in this section.

Figure 34: MPO Rear Transition Module



8.1 MPO RTM Features

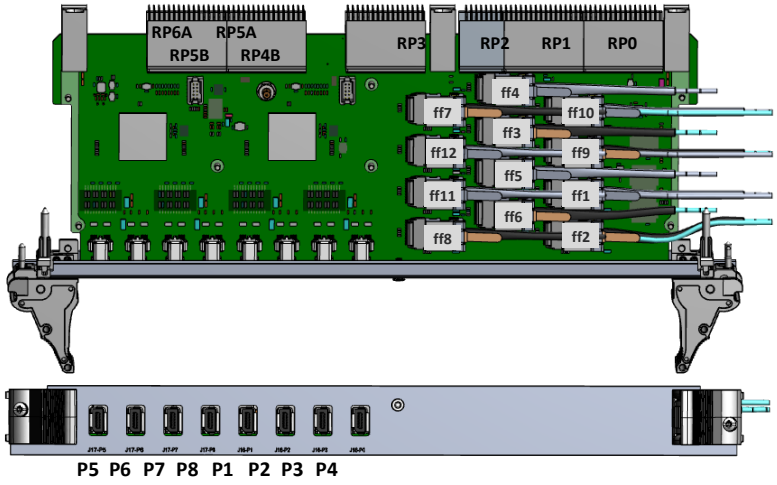
Main Features

The MPO RTM has been designed to offer maximum IOs connectivity and throughput on a single board:

- Ethernet 1000BASE-T ports: Up to 8x 1000BASE-T ports on rear panel, derived from VPX P5/P6 control planes.
- Optical links: Up to 12x Samtec Firefly sockets from VPX P1/P2/P3 data planes, to equip with Samtec 40G/4x10G Firefly optical transceivers.
- Required power supplies (RP0):
  - VS1: +12V, 0.25A.
  - VS2: +3.3V, 6A.
  - VS3: not used.
- Form factor: 6U RTM. Dimensions : 81.5 x 233.35. Height : 4HP (0.8 inch).

Connectors identification

Figure 35: Connectors identification on MPO RTM



Ethernet ports

The two quad BCM54140 PHYs convert the SGMII links from VPX RP5 & RP6 into the eight 1000BASE-T ports on rear panel. The connectors from Harting ix Industrial series (A coding) have been selected for their compactness and performance. They are well suited for high data rates (from Cat. 5e / 1Gbps to Cat. 6A / 10Gbps) and include a lock mechanism.

Optical ports

Twelve optical transceivers Firefly by Samtec convert the Ethernet 10GBASE-KR lanes.

The chassis must be designed to allow the escape of the fibers on the right side of the RTM. Please contact Kontron for other configurations.

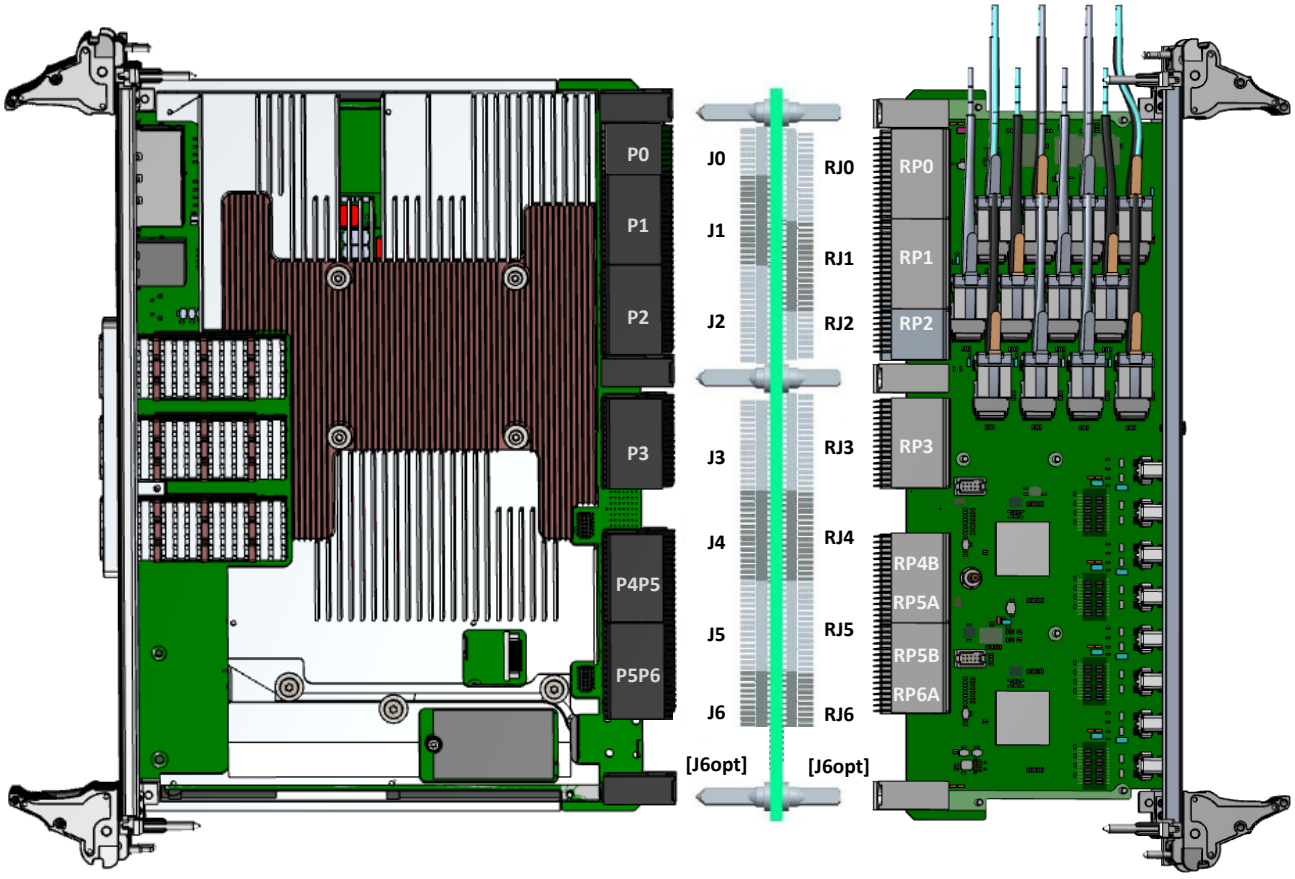
Backplane Connectors

On VPX backplanes, the daughter card and RTM connectors are staggered on the P0/P1/P2 portion: P0/J0 have only 8 wafers whereas RJ0/RP0 have 16 (and vice-versa for P2/J2 and RJ2/RP2). See Figure 36 below.

The VX6940 and the RTM do not use P4 and implement only a half P6 (P6A). To ease design and production, 16-wafer connectors have been placed across VITA P5 location (see P4P5 and P5P6 in Figure 36). Functionally, this is equivalent to no P4, a full P5 and a half P6 (ie P6A).

The VX6940 also include the possibility of a P6 optical connector. This link is not managed by the MPO RTM.

Figure 36: Backplane Connectors Correspondence with RPO RTM



Thermal Management

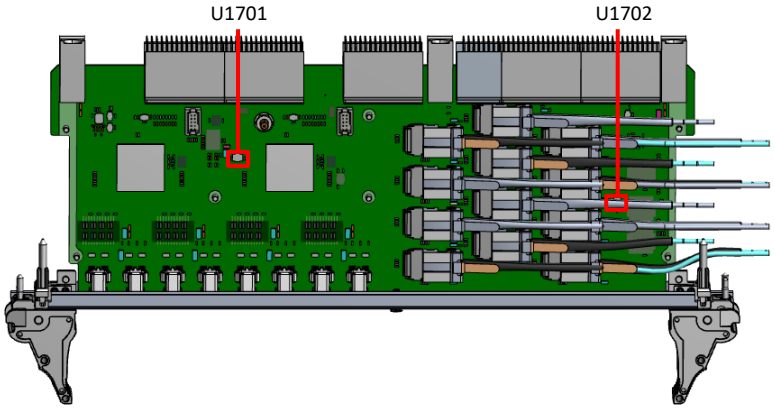
The power dissipation is (23W max) comes mainly from the Firefly transceivers and to a lesser extent from the Ethernet PHYs. A heatsink is attached to these components through appropriate thermal interface.

An air flow of 1.2 m/s is recommended.

The monitoring of the temperature on the MPO RTM is possible through the LM73 thermal sensors:

- U1701: between the two PHYs; I2C address 0x4C (7-bit).
- U1702: close to the Fireflies connectors; I2C address 0x49 (7-bit).

Figure 37: Temperature Sensors Location on MPO RTM



8.2 RTM Installation

To perform an initial installation of the RTM in a system proceed as follows:

1. Ensure that the safety requirements indicated in Section 3.1 are observed.

⚠CAUTION Failure to comply with the instructions below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the VX6940 refer to section 3.4. For the installation of Expansion cards and Mezzanines, refer to the appropriate sections in current chapter.

NOTICE Care must be taken when applying the procedures below to ensure that neither the VX6940 nor other system boards are physically damaged by the application of these procedures.

3. To install the RTM:

3.1 Ensure that no power is applied to the system before proceeding.

NOTICE CAUTION: When performing the next step, DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

3.2 Carefully insert the board until it makes contact first with the backplane alignment keys, then with the backplane connectors.

3.3 Using the ejectors handles, engage the board with the backplane connectors. When the ejectors handles are locked, the board is fully installed.

3.4 Fasten the front panel retaining screws.

3.5 Connect all external interfacing cables to the board as required.

3.6 Ensure that the RTM and all required interfacing cables are properly secured.

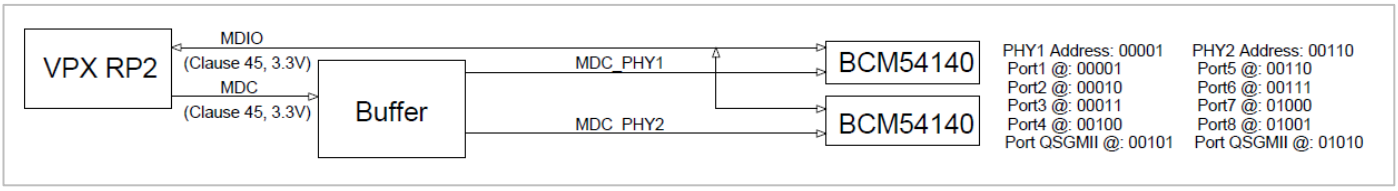
The RTM is now ready for operation.

8.3 Configuration busses: I2C & MDIO

- MDIO bus

  A two-wire MDC/MDIO bus (Clause 45, 3.3V) is implemented between the VX6940 and the MPO RTM to configure the BCM54140 PHYs.

Figure 38: MDIO Topology Diagram of MPO RTM

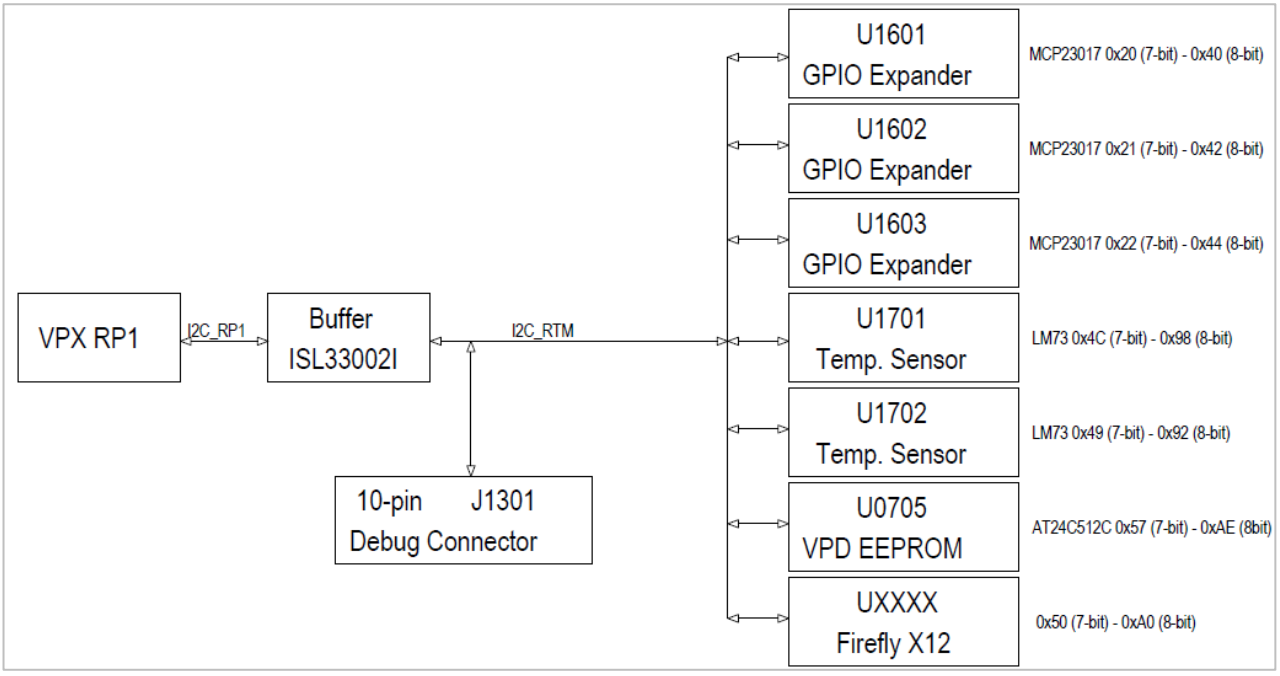


- I2C bus

  A two-wire I2C bus is used to configure the GPIO expanders, the temperature sensors, a VPD EEPROM and the Samtec Firefly transceivers.

  The Samtec Firefly transceivers do not have individual I2C addresses. Each Firefly transceiver's I2C interface must be enabled (MODSEL#). This is done through the GPIOs expanders and decoders.

Figure 39: I2C Topology Diagram of MPO RTM



8.4 Physical IOs of MPO RTM

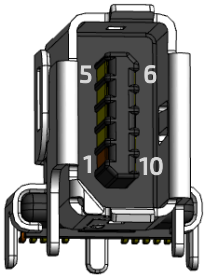
8.4.1 Rear Ethernet Connectors

Ethernet 1000BASE-T Connectors

Table 44: MPO RTM, Ethernet Ports Pin Assignment

Pin	Signal
1	BI_DA+
2	BI_DA-
3	GND
4	BI_DC+
5	BI_DC-
6	BI_DB+
7	BI_DB-
8	GND
9	BI_DD+
10	BI_DD-
Sn	SHIELD

Figure 40: MPO RTM, Ethernet Ports ix Connector



Harting 09452812560

Table 45: MPO RTM, Ethernet Ports Signals Definition

Signal	Dir.	Definition
BI_DA+/-	I/O	BI_DA differential pair
BI_DB+/-	I/O	BI_DB differential pair
BI_DC+/-	I/O	BI_DC differential pair
BI_DD+/-	I/O	BI_DD differential pair
SHIELD	-	Chassis ground

Ethernet 1000BASE-T Cables

Adaptation cable from ix Industrial to RJ45 can be found in any length at Harting's (for instance **09 48 261 2749 010 for a 1m-cable).**

Figure 41: MPO RTM, Ethernet Cable

Harting 09 48 261 2749 010

8.4.2 Onboard Optical Ports & Firefly Connectors

This section describes the optical ports ff1 to ff12. The Samtec Optical Firefly Solution includes two connectors :

- The UCC8 connector is a low speed connector which carries utility and sideband signals such as Presence Detect, Reset, I2C, supply etc.
- The UEC5 connector is the high speed data connector.

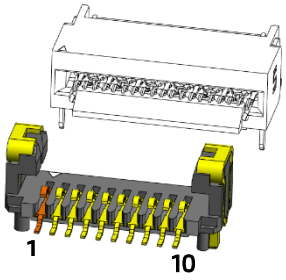
Optical Firefly Assembly is referred to as ECUO in Samtec documentation.

Firefly UCC8 Utility Connector Description

Table 46: MPO RTM, Firefly UCC8 Pin Assignment

Pin	Copper Signal	Optical Signal
1	NC	+3.3V
2	NC	GND
3	GND	PRESENT#
4	NC	SELECT#
5	NC	INT#
6	NC	RESET#
7	NC	SDA
8	NC	SCL
9	NC	NC
10	NC	+3.3V

Figure 42: MPO RTM, Firefly UCC8 Utility Connector



SAMTEC UCC8-010-1-H-S-1-A

Table 47: MPO RTM, UCC8 Signal Definition

Signal	Dir.	Definition
INT#	O	Interrupt signal. Indicates a possible module operational fault or status critical to the host system. On MPO RTM, managed through GPIO expander.
RESET#	I	Reset signal. A low state on this pin indicates a complete module reset, returning all user settings to their default value. On MPO RTM, managed through GPIO expander.
GND	-	Ground
NC	-	Not connected. Reserved.
PRESENT#	O	Module Presence Detect. On MPO RTM, managed through GPIO expander.
SCL	I/O	I2C Interface Clock. On MPO RTM, connected to P1.SE4.
SDA	I/O	I2C Interface Data. On MPO RTM, connected to P1.SE5.
SELECT#	I	Active low I2C Enable Pin. On MPO RTM, managed through GPIO expander.
+3.3V	Power	+3.3V Power Supply.

Firefly UEC5 Data Connector Description

Table 48: MPO RTM, Firefly UEC5 Pin Assignment

Pin	Signal	Pin	Signal
A1	GND	B1	GND
A2	TX1-	B2	TX2-
A3	TX1+	B3	TX2+
A4	GND	B4	GND
A5	TX3-	B5	TX4-
A6	TX3+	B6	TX4+
A7	GND	B7	GND
A8	50 Ohm to GND	B8	50 Ohm to GND
A9	50 Ohm to GND	B9	50 Ohm to GND
A10	50 Ohm to GND	B10	50 Ohm to GND
A11	50 Ohm to GND	B11	50 Ohm to GND
A12	50 Ohm to GND	B12	50 Ohm to GND
A13	GND	B13	GND
A14	RX4+	B14	RX3+
A15	RX4-	B15	RX3-
A16	GND	B16	GND
A17	RX2+	B17	RX1+
A18	RX2-	B18	RX1-
A19	GND	B19	GND

Figure 43: MPO RTM, Firefly UEC5 Data Connector

SAMTEC UEC5-019-2-H-D-RA-1

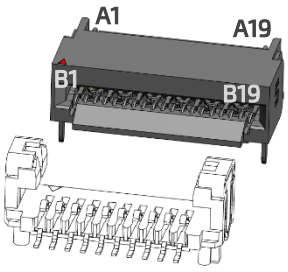


Table 49: MPO RTM, UEC5 Signal Definition

Signal	Dir.	Definition
RXn+/-	I	Ethernet receive differential pair n (n=1 to 4).
TXn+/-	O	Ethernet transmit differential pair n (n=1 to 4).
GND	-	Ground

8.4.3 VPX Connectors

For a detailed pin assignment, please refer to the VX6940 description in section "Rear Connectors".

Table 50: MPO RTM, Optical Ports Assignment

RP0 (TE 2302794-2, Multigig RT3)			RP1 (TE 2302795-2, Multigig RT3)			RP2 (TE 2302796-2, Multigig RT3)			RP3 (TE 2302795-2, Multigig RT3)		
Wafer	**Lane on VX6940 BCM56760**	**Firefly Conn.**	**Wafer**	**Lane on VX6940 BCM56760**	**Firefly Conn.**	**Wafer**	**Lane on VX6940 BCM56760**	**Firefly Conn.**	**Wafer**	**Lane on VX6940 BCM56760**	Firefly Conn.
w1	-	-	w1	TSCe4 L0	ff9	w1	TSCe12 L0	ff3	w1	TSCe1 L0	ff7
w2	-		w2	TSCe4 L1		w2	TSCe12 L1		w2	TSCe1 L1	
w3	-		w3	TSCe4 L2		w3	TSCe12 L2		w3	TSCe1 L2	
w4	-		w4	TSCe4 L3		w4	TSCe12 L3		w4	TSCe1 L3	
w5	-	-	w5	TSCe3 L0	ff10	w5	TSCe13 L0	**ff4**	w5	TSCe0 L0	ff12
w6	-		w6	TSCe3 L1		w6	TSCe13 L1		w6	TSCe0 L1	
w7	-		w7	TSCe3 L2		w7	TSCe13 L2		w7	TSCe0 L2	
w8	-		w8	TSCe3 L3		w8	TSCe13 L3		w8	TSCe0 L3	
w9	TSCf0 L0	ff2	w9	TSCe6 L0	ff6				w9	TSCe11 L0	ff11
w10	TSCf0 L1		w10	TSCe6 L1					w10	TSCe11 L1	
w11	TSCf0 L2		w11	TSCe6 L2					w11	TSCe11 L2	
w12	TSCf0 L3		w12	TSCe6 L3					w12	TSCe11 L3	
w13	TSCe5 L0	ff1	w13	TSCe2 L0	ff5				w13	TSCf3 L0	ff8
w14	TSCe5 L1		w14	TSCe2 L1					w14	TSCf3 L1	
w15	TSCe5 L2		w15	TSCe2 L2					w15	TSCf3 L2	
w16	TSCe5 L3		w16	TSCe2 L3					w16	TSCf3 L3	

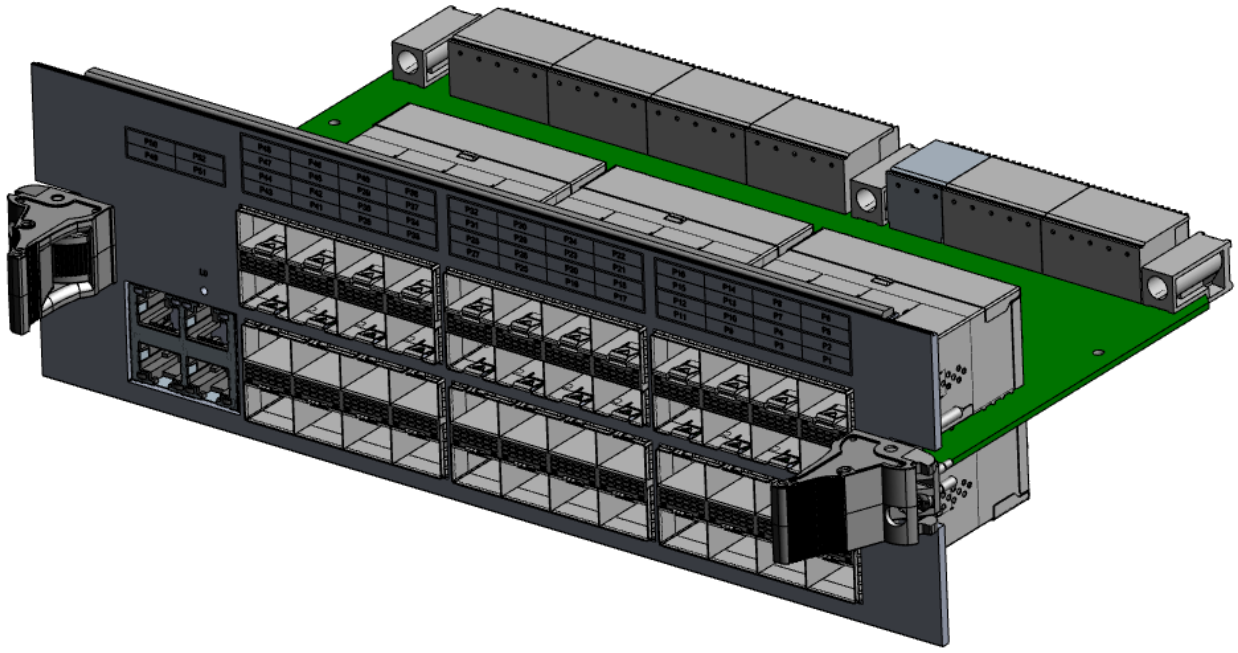
Table 51: MPO RTM, 1000BASE-T Ethernet Ports Assignment

RP5 (VITA denomination) (TE 2302795-2, Multigig RT3)			RP6A (VITA denomination) (TE 2302795-2, Multigig RT3)		
Wafer	**Lane on VX6940 BCM56760**	**1000BASE-T Ethernet Port**	**Wafer**	**Lane on VX6940 BCM56760**	**1000BASE-T Ethernet Port**
-	-	-	w1	TSCe10 L3	P8
w10	TSCe8 L0	P1	-	-	-
w11	TSCe8 L3	P2	-	-	-
w12	TSCe7 L0	P3	-	-	-
w13	TSCe7 L1	P4	-	-	-
w14	TSCe10 L0	P5	-	-	-
w15	TSCe10 L1	P6	-	-	-
w16	TSCe10 L2	P7	-	-	-

9 SFP Rear Transition Module

The Rear Transition Module (RTM) RTM-EZVX6940-SFP is not the only one which has been designed for VX6940. For the sake of brevity this RTM is referred to as SFP RTM in this section.

Figure 44: SFP Rear Transition Module



9.1 SFP RTM Features

Main Features

The SFP RTM has been designed to offer maximum IOs connectivity and throughput on a single card:

- Modular SFP+ ports

Up to 48x SFP+ sockets from VPX P1/P2/P3 data planes, to equip with 1000BASE-T, 1000BASE-SX, 10GBASE-T or 10GBASE-SR SFP+ transceivers.

- Ethernet 1000BASE-T ports

Up to 4x 1000BASE-T ports on rear panel, derived from VPX P5/P6 control planes.

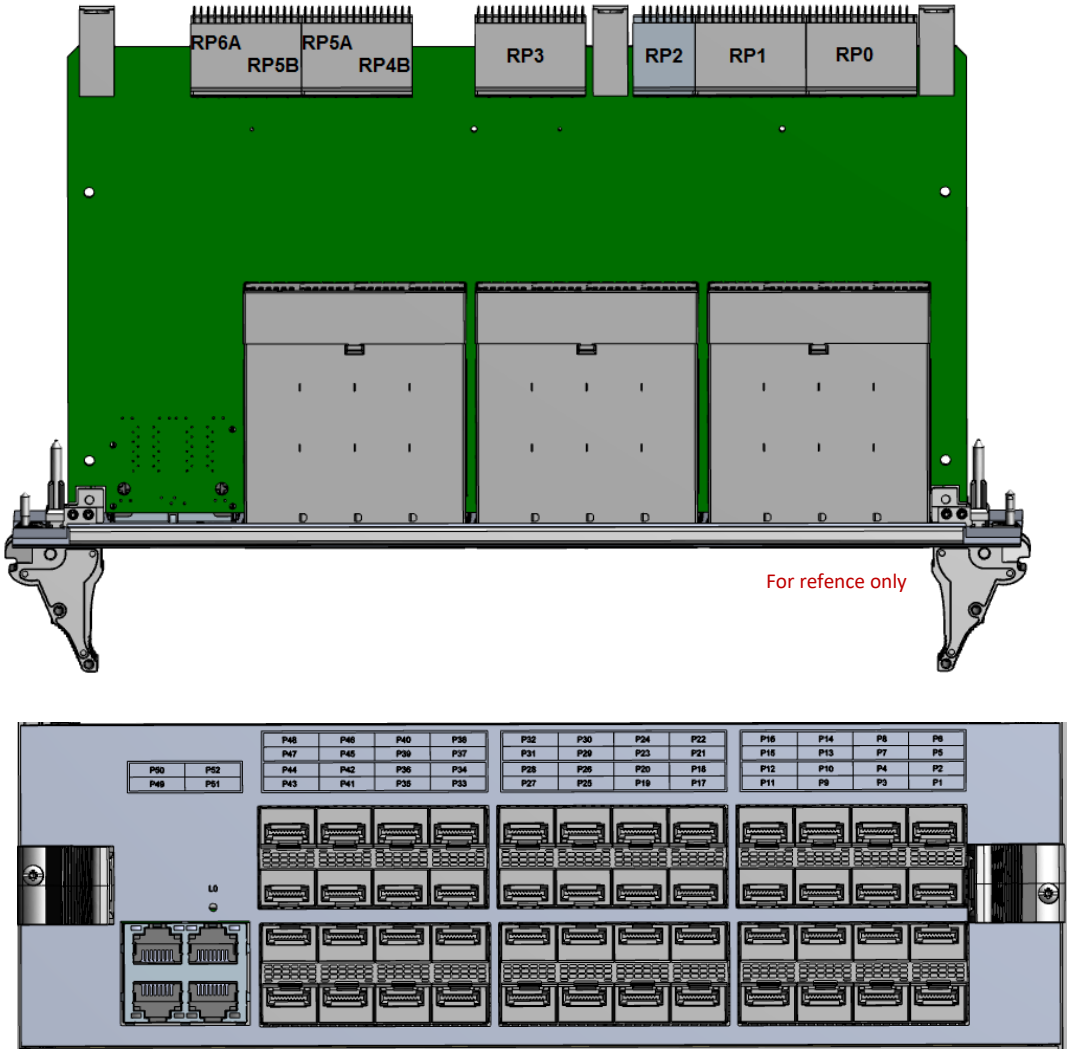
- Required power supplies (RP0)
  - VS1: +12V, 2.7A (fully equipped with 48 SFP+ transceiver 10GBASE-T 80m #87588).
  - VS2: +3.3V, 13.3A (fully equipped with 48 SFP+ transceiver 10GBASE-T 80m #87588).
  - VS3: +3.3V, 12.2A (fully equipped with 48 SFP+ transceiver 10GBASE-T 80m #87588).
- Specific form factor

6U width. Dimensions : 120 x 233.35. Height : 8HP (1.6 inch).

The SFP RTM does not comply to VITA 46.10 RTM standard regarding power supplies and mechanical dimensions. Please contact Kontron for specific backplane and chassis implementation.

Connectors identification

Figure 45: Connectors identification on SFP RTM



The front silk screen shown in Figure 46 corresponds to logical Fastpath ports.

Figure 46: SFP RTM Front Silk Screen

		P48	P46	P40	P38	P32	P30	P24	P22	P16	P14	P8	P6
		P47	P45	P39	P37	P31	P29	P23	P21	P15	P13	P7	P5
P50	P52	P44	P42	P36	P34	P28	P26	P20	P18	P12	P10	P4	P2
P49	P51	P43	P41	P35	P33	P27	P25	P19	P17	P11	P9	P3	P1

1000BASE-T Ethernet Ports

The quad BCM54140 PHY converts the SGMII links from VPX RP5 into the four 1000BASE-T ports on front panel. The connectors are standard RJ45 connectors.

SFP+ Ethernet Ports

The forty eight SFP+ transceivers are connected to BCM56760 Ethernet Switch SerDes through retimer to ensure proper signal integrity across backplane up to 10Gb Ethernet.

The following SFP+transceivers have been qualified at Kontron:

- 10GBASE-T 80m #87588 from FS.com
- 1000BASE-T FCLF8520P2BTL from Finisar.
- 1GBASE-SR/10GBASE-SR dual rate 850nm FTLX8574D3BCV from Finisar

NOTICE

For other SFP+ transceiver compatibility please contact Kontron.

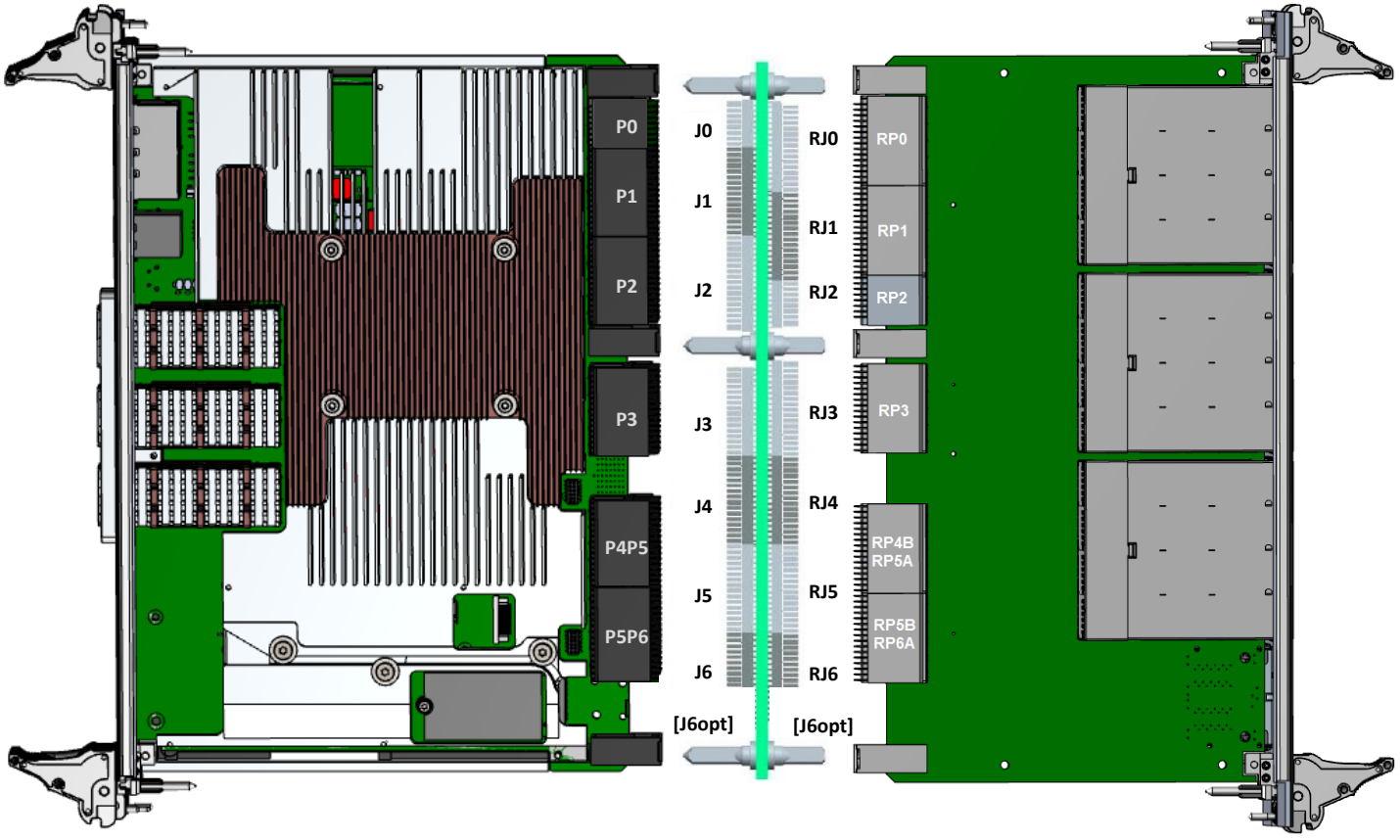
Backplane Connectors

On VPX backplanes, the daughter card and RTM connectors are staggered on the P0/P1/P2 portion: P0/J0 have only 8 wafers whereas RJ0/RP0 have 16 (and vice-versa for P2/J2 and RJ2/RP2). See Figure 47 below.

The VX6940 and the RTM do not use P4 and implement only a half P6 (P6A). To ease design and production, 16-wafer connectors have been placed across VITA P5 location (see P4P5 and P5P6 in Figure 47). Functionally, this is equivalent to no P4, a full P5 and a half P6 (ie P6A).

The VX6940 also include the possibility of a P6 optical connector. This link is not managed by the RTM-EZVX6940-SFP.

Figure 47: Backplane Connectors Correspondence with SFP RTM



Thermal Management

The power dissipation of 115W (130W max) comes mainly from the retimers, SFP+ transceiver and to a lesser extent from the Ethernet PHY. A heatsink is attached to the retimers.

An air flow of 1. 2 m/s is recommended.

The monitoring of the temperature on the RTM is possible through the LM73 thermal sensors:

- U1201: located at air flow exit on TOP side; I2C address 0x4C (7-bit).
- U1202: located at air flow entry on TOP side; I2C address 0x4D (7-bit).
- U1203: located at air flow exit on BOTTOM side; I2C address 0x4E (7-bit).

Figure 48: Temperature Sensors Location on SFP RTM (Top Side)

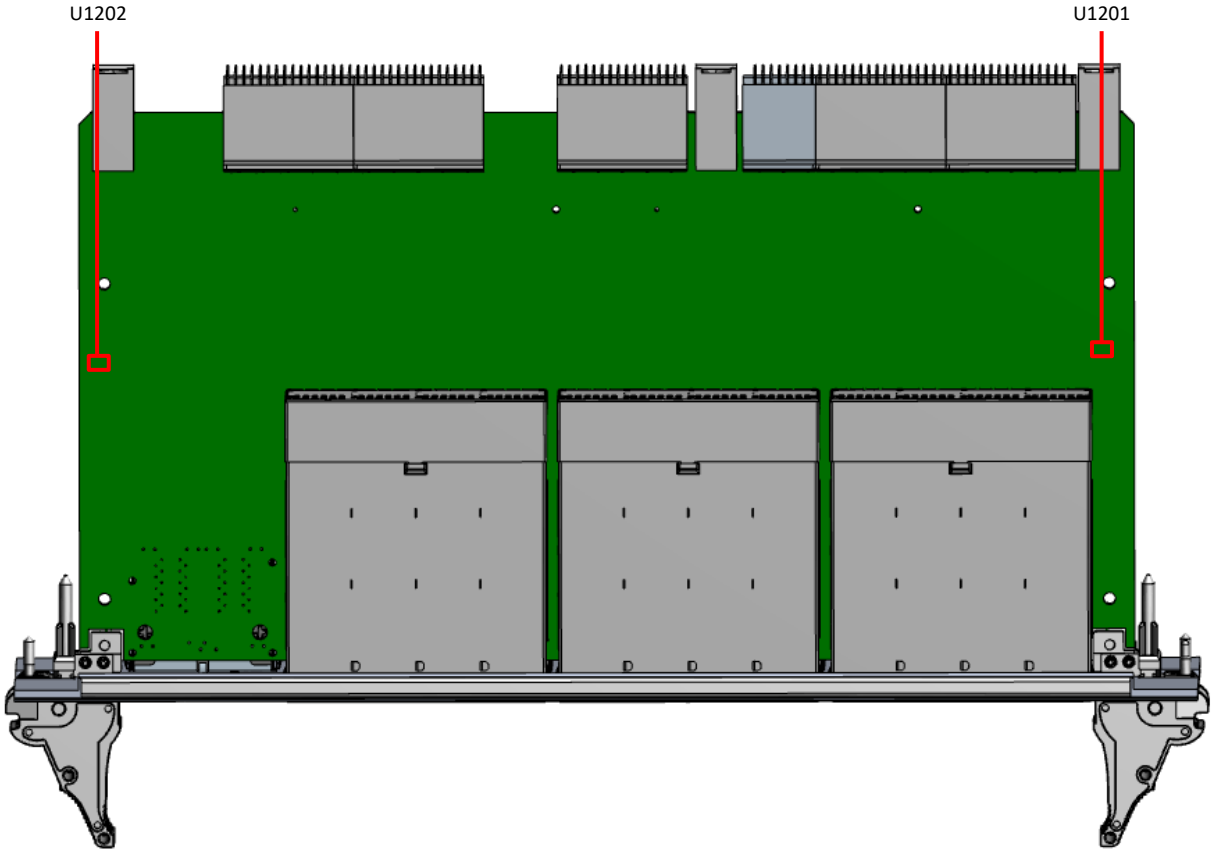
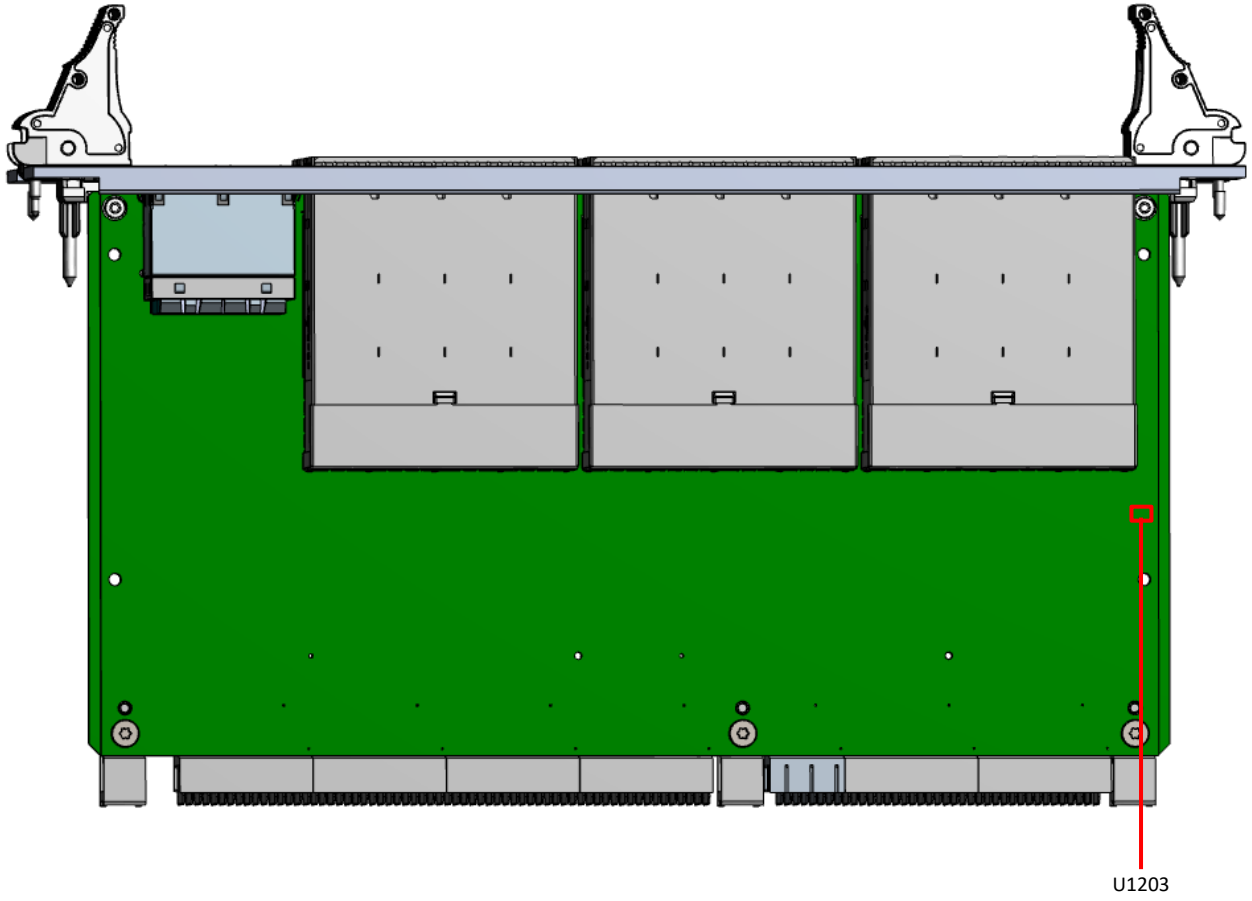


Figure 49: Temperature Sensors Location on SFP RTM (Bottom Side)



9.2 RTM Installation

To perform an initial installation of the RTM in a system proceed as follows:

1. Ensure that the safety requirements indicated in Section 3.1 are observed.

⚠CAUTION Failure to comply with the instructions below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the VX6940 refer to section 3.4. For the installation of Expansion cards and Mezzanines, refer to the appropriate sections in current chapter. For the installation of specific peripheral devices and Rear IO devices, refer to RTM in Chapter 8.

NOTICE Care must be taken when applying the procedures below to ensure that neither the VX6940 nor other system boards are physically damaged by the application of these procedures.

3. To install the RTM:

3.1 Ensure that no power is applied to the system before proceeding.

NOTICE CAUTION: When performing the next step, DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

3.2 Carefully insert the board until it makes contact first with the backplane alignment keys, then with the backplane connectors.

3.3 Using the ejectors handles, engage the board with the backplane connectors. When the ejectors handles are locked, the board is fully installed.

3.4 Fasten the front panel retaining screws.

3.5 Connect all external interfacing cables to the board as required.

3.6 Ensure that the RTM and all required interfacing cables are properly secured.

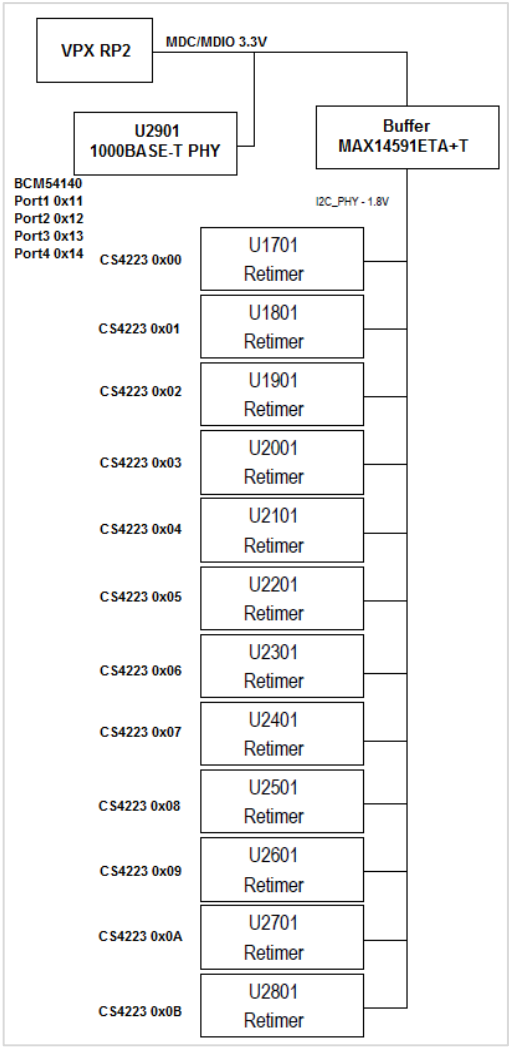
The RTM is now ready for operation.

9.3 Configuration busses: I2C & MDIO

MDIO bus

A two-wire MDC/MDIO bus is implemented between the VX6940 and the RTM to configure the BCM54140 Ethernet PHY and the CS4223 retimers.

Figure 50: MDIO Topology Diagram of SFP RTM

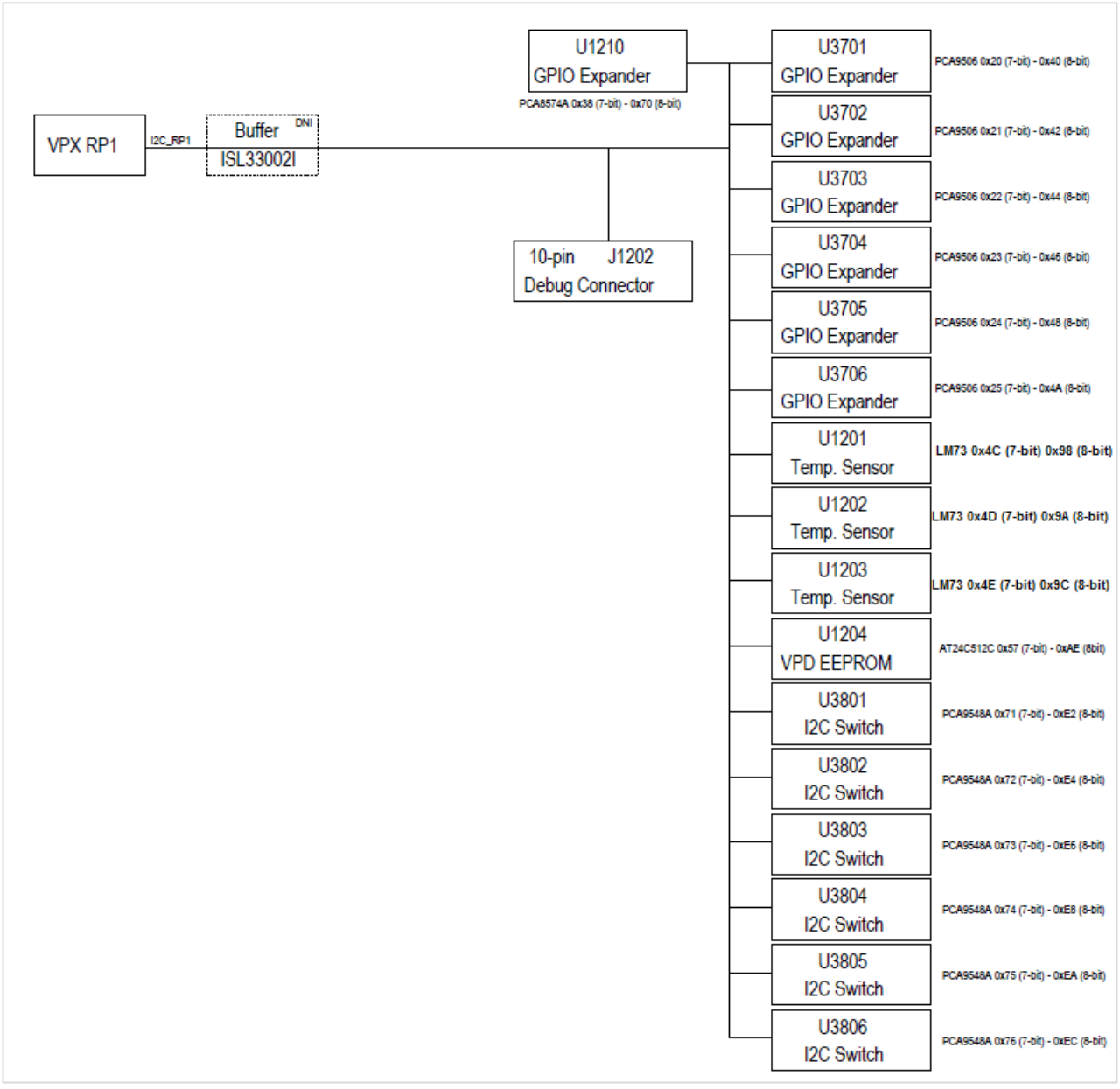


I2C bus

A two-wire I2C bus is used to configure the I2C multiplexor, the GPIO expanders, the temperature sensors, a VPD EEPROM and the SFP+ transceivers.

The SFP+ transceivers do not have individual I2C addresses. Each SFP+ transceiver's I2C interface must be reached through I2C multiplexor. SFP+ transceivers control signals (TX_FAULT, TX_DIS, RX_LOS, MOD_ABS and RS0) are handled through GPIO expanders connected on I2C bus.

Figure 51: I2C Topology Diagram of SFP RTM



9.4 Physical IOs of SFP RTM

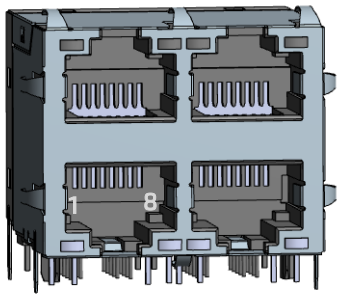
9.4.1 Rear Ethernet Connectors

- **Ethernet 1000BASE-T Connectors**

Table 52: SFP RTM, Ethernet Ports Pin Assignment

Pin	Signal
1	BI_DA+
2	BI_DA-
3	BI_DB+
4	BI_DC+
5	BI_DC-
6	BI_DB-
7	BI_DD+
8	BI_DD-
CASEn	SHELL

Figure 52: SFP RTM, Ethernet Ports Connector



Pulse Electronics JXC0-0351NL

Table 53: SFP RTM, Ethernet Ports Signals Definition

Signal	Dir.	Definition
BI_DA+/-	I/O	BI_DA differential pair
BI_DB+/-	I/O	BI_DB differential pair
BI_DC+/-	I/O	BI_DC differential pair
BI_DD+/-	I/O	BI_DD differential pair
SHELL	-	Chassis ground

9.4.2 SFP+ Connectors

This section describes the SFP+ ports. These ports are SFF-8431 and SFF-8432 MSA compliant.

Figure 53: SFP RTM, SFP+ Connector Pin Assignment (Top View)

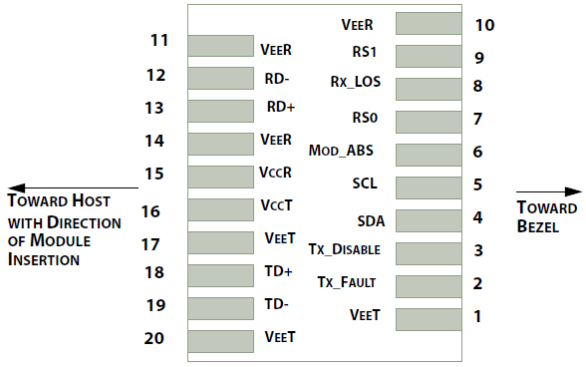


Figure 54: SFP RTM, SFP+ Cage and Connectors

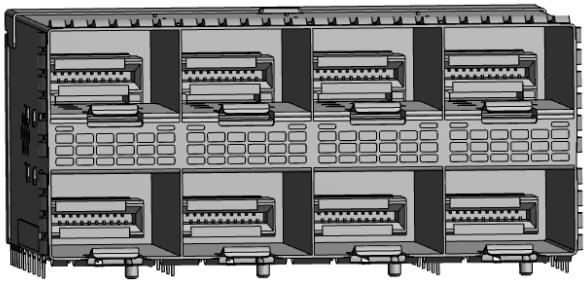


Figure 55: SFP+ Module Contact Pins Assignment

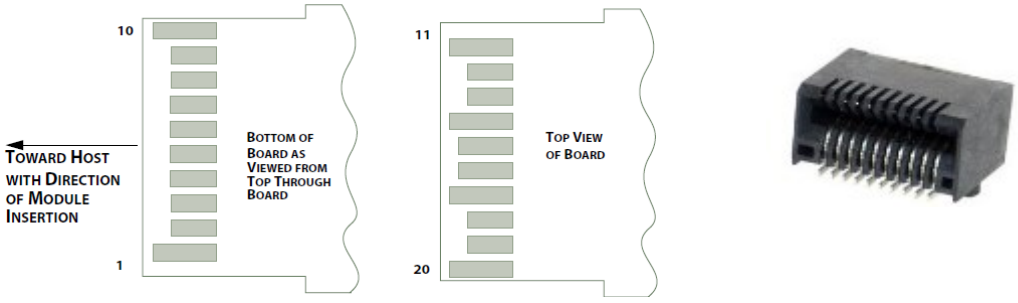


Table 54: SFP RTM, SFP+ connector pins assignment

Signal	Dir.	Definition
TX_FAULT	I	When high, indicates that the module transmitter has detected a fault condition. On RTM-EZVX6940-SFP, managed through GPIO expander.
TX_DISABLE	O	When high or left open, the SFP+ module transmitter output is turned off. On RTM-EZVX6940-SFP, managed through GPIO expander.
RS0	O	Module Rate Select 0. On RTM-EZVX6940-SFP, managed through GPIO expander.
RS1	O	Module Rate Select 1. Not Connected on RTM-EZVX6940-SFP.
MOD_ABS	I	Module Presence Detect. On RTM-EZVX6940-SFP, managed through GPIO expander.
RX_LOS	I	Only for optical SFP+ transceiver. When high indicates an optical signal level below that specified in the relevant standard. On RTM-EZVX6940-SFP, managed through GPIO expander.
SCL	O	I2C Interface Clock. On RTM-EZVX6940-SFP, connected to P1.SE4 and switched by I2C multiplexor.
SDA	I/O	I2C Interface Data. On RTM-EZVX6940-SFP, connected to P1.SE5 and switched by I2C multiplexor.
+3.3V	Power	+3.3V Power Supply.
GND	-	Ground

9.4.3 VPX Connectors

For a detailed pin assignment, please refer to the VX6940 description in section "Rear Connectors".

Table 55: SFP RTM, SFP+ Ports Assignment

RP0 (TE 2302794-2, Multigig RT3)			RP1 (TE 2302795-2, Multigig RT3)			RP2 (TE 2302796-2, Multigig RT3)			RP3 (TE 2302795-2, Multigig RT3)		
Wafer	**Lane on VX6940 BCM56760**	**Firefly Conn.**	**Wafer**	**Lane on VX6940 BCM56760**	**Firefly Conn.**	**Wafer**	**Lane on VX6940 BCM56760**	**Firefly Conn.**	**Wafer**	**Lane on VX6940 BCM56760**	**Firefly Conn.**
w1	-	-	w1	TSCe4 L0	9	w1	TSCe12 L0	25	w1	TSCe1 L0	33
w2	-		w2	TSCe4 L1	10	w2	TSCe12 L1	26	w2	TSCe1 L1	34
w3	-		w3	TSCe4 L2	11	w3	TSCe12 L2	27	w3	TSCe1 L2	35
w4	-		w4	TSCe4 L3	12	w4	TSCe12 L3	28	w4	TSCe1 L3	36
w5	-	-	w5	TSCe3 L0	13	w5	TSCe13 L0	**29**	w5	TSCe0 L0	37
w6	-		w6	TSCe3 L1	14	w6	TSCe13 L1	30	w6	TSCe0 L1	38
w7	-		w7	TSCe3 L2	15	w7	TSCe13 L2	31	w7	TSCe0 L2	39
w8	-		w8	TSCe3 L3	16	w8	TSCe13 L3	32	w8	TSCe0 L3	40
w9	TSCf0 L0	1	w9	TSCe6 L0	17				w9	TSCe11 L0	41
w10	TSCf0 L1	2	w10	TSCe6 L1	18				w10	TSCe11 L1	42
w11	TSCf0 L2	3	w11	TSCe6 L2	19				w11	TSCe11 L2	43
w12	TSCf0 L3	4	w12	TSCe6 L3	20				w12	TSCe11 L3	44
w13	TSCe5 L0	5	w13	TSCe2 L0	21				w13	TSCf3 L0	45
w14	TSCe5 L1	6	w14	TSCe2 L1	22				w14	TSCf3 L1	46
w15	TSCe5 L2	7	w15	TSCe2 L2	23				w15	TSCf3 L2	47
w16	TSCe5 L3	8	w16	TSCe2 L3	24				w16	TSCf3 L3	48

Table 56: SFP RTM, 1000BASEèT Ethernet Ports Assignment

RP5 (TE 2302795-2, Multigig RT3)			RP6A (TE 2302795-2, Multigig RT3)		
Wafer	**Lane on VX6940 BCM56760**	**1000BASE-T Ethernet Port**	**Wafer**	**Lane on VX6940 BCM56760**	**1000BASE-T Ethernet Port**
-	-	-	w1	TSCe10 L3	NC
w10	TSCe8 L0	49	-	-	-
w11	TSCe8 L3	50	-	-	-
w12	TSCe7 L0	51	-	-	-
w13	TSCe7 L1	52	-	-	-
w14	TSCe10 L0	NC	-	-	-
w15	TSCe10 L1	NC	-	-	-
w16	TSCe10 L2	NC	-	-	-

10 Software

Software on the VX6940 includes :

- The bootloader
- initrd (including rootfs, kernel)
- The application software (FASTPATH switching SW)

The Software operates the switching hardware and is therefore referred to as firmware. It is pre-installed on the system and its update requires a specific procedure.

This section describes the bootloader and Linux rootfs/kernel, and introduces the update procedure. For additional information about system configuration using CLI commands, please refer to the “VX6940 CLI Reference Manual”.

10.1 Supported Standards & RFCs

10.1.1 Management

- **Core Features**

Table 57: Management Core Features RFCs (Miscellaneous)

ID	Purpose	ID	Purpose
RFC 854	Telnet	RFC 855	Telnet option specifications
RFC 1155	SMI v1	RFC 1157	SNMP
RFC 1212	Concise MIB definitions	RFC 1867	HTML/2.0 forms with file upload extensions
RFC 1901	Community-based SNMP v2	RFC 1908	Coexistence between SNMP v1 and SNMP v2
RFC 2068	HTTP/1.1 protocol as updated by draft-ietf-http-v11-spec-rev-03	RFC 2271	SNMP framework MIB
RFC 2295	Transparent content negotiation	RFC 2296	Remote variant selection; RSVA/1.0 state management cookies- draft-ietf-http-state-mgmt-05
RFC 2576	Coexistence between SNMP v1, v2, and v3	RFC 2578	SMI v2
RFC 2579	Textual conventions for SMI v2	RFC 2580	Conformance statements for SMI v2
RFC 2616	HTTP/1.1	RFC 3410	Introduction and Applicability Statements for Internet Standard Management Framework
RFC 3411	An Architecture for Describing SNMP Management Frameworks	RFC 3412	Message Processing and Dispatching
RFC 3413	SNMP v3 Applications	RFC 3414	User-Based Security Model for SNMP v3
RFC 3415	View-based Access Control Model for SNMP	RFC 3416	Version 2 of SNMP Protocol Operations for SNMP
RFC 3417	Transport Mappings for SNMP	RFC 3418	Management Information Base (MIB) for the Simple Network Management Protocol (SNMP)
RFC 6020	A Data Modeling Language for NETCONF	RFC 6022	YANG Module for NETCONF Monitoring
RFC 6241	Network Configuration Protocol (NETCONF)	RFC 6242	Using the NETCONF Protocol over Secure Shell (SSH)
RFC 6415	Web Host Metadata	RFC 6536	NETCONF Access Control Model
RFC 7223	YANG Data Model for Interface Management	RFC 7277	YANG Data Model for IP Management
RFC 7317	YANG Data Model for System Management		

Table 58: Management Core Features RFCs (SSL 3.0, TLS 1.0, TLS 1.1, TLS 1.2)

ID	Purpose	ID	Purpose
RFC 2246	The TLS protocol, version 1.0	RFC 2818	HTTP over TLS
RFC 3268	AES cipher suites for Transport layer security	RFC 4346	The Transport Layer Security (TLS) Protocol Version 1.1
RFC 5246	The Transport Layer Security (TLS) Protocol Version 1.2 SSH 2.0		

Table 59: Management Core Features RFCs (SSH 2.0)

ID	Purpose	ID	Purpose
RFC 4251	SSH protocol architecture	RFC 4252	SSH authentication protocol
RFC 4253	SSH transport layer protocol	RFC 4254	SSH connection protocol
RFC 4716	SECSH public key file format	RFC 4419	Diffie-Hellman group exchange for the SSH transport layer protocol
RFC 6668	SHA-2 Data Integrity Verification for the Secure Shell (SSH) Transport Layer Protocol		

Other core features include:

- Configurable management VLAN
- HTML 4.0 specification, December 1997
- Java Plug-in 1.6.0_01 and Java Script 1.3
- RESTCONF: https://tools.ietf.org/html/draft-ietf-netconf-restconf-04
- draft-ietf-netmod-syslog-model-03
- draft-ietf-netconf-yang-library-00
- draft-ietf-httpauth-basicauth-update-03
- draft-ietf-netmod-yang-json-05
- draft-jxl-tictoc-1588v2-yang-03
- Bonjour service
- Dual software images
- Management port access control
- Password management (history)
- Strong passwords
- RESTful APIs
- Management vis NetSNMP

- **Advanced Management Features**
  - Industry-standard CLI with the following features:
    - Scripting capability
    - Command completion
    - Context-sensitive help
  - Optional user password encryption
  - Multisession Telnet server
  - Secure copy server
  - Command authorization
  - Port locator
  - Dynamic/prescriptive topology map
  - Management Access Control and Administration List

10.1.2 Switching

- **Core Features**

Table 60: Switching Core Features

ID	Purpose	ID	Purpose
IEEE 801.1Qbb	Priority-based Flow Control	IEEE 802.1AB	Link Layer Discovery Protocol (LLDP)
IEEE 802.1ak	Virtual Bridged Local Area Networks - Amendment 07: Multiple Registration Protocol	IEEE 802.1p	Ethernet priority with user provisioning and mapping
IEEE 802.1D	Spanning tree compatibility	IEEE 802.1s	Multiple spanning tree compatibility
IEEE 802.1Q	Virtual LANs with port-based VLANs	IEEE 802.1v	Protocol-based VLANs
IEEE 802.1X-2010	Port-based authentication and supplicant support	IEEE 802.1w	Rapid spanning tree compatibility
IEEE 802.3	10Base-T	IEEE 802.3u	100Base-T
IEEE 802.3ab	1000Base-T	IEEE 802.3ac	VLAN tagging
IEEE 802.3ad	Link aggregation	IEEE 802.3ae	10GbE
IEEE 802.3bj-CL91	Forward Error Correction (FEC)	IEEE 802.3x	Flow control
ANSI/TIA-1057	LLDP-Media Endpoint Discovery (MED)	GARP	Generic Attribute Registration Protocol
GMRP	Dynamic L2 multicast registration	GVRP	Dynamic VLAN registration
PVSTP	Per VLAN Spanning Tree Protocol	PVRSTP	Per VLAN Rapid Spanning Tree Protocol
VPC	Virtual Port Channel (MLAG)	RFC 4541	Considerations for Internet Group Management Protocol (IGMP) and Multicast Listener Discovery (MLD) Snooping Switches
RFC 5171	UniDirectional Link Detection (UDLD) Protocol		

- Additional Layer 2 Functionalities

Table 61: Additional Layer 2 Functionalities

Functionality	Functionality
ARP Guard	Authentication, Authorization, and Accounting (AAA)
Broadcast/Multicast/Unicast storm recovery	Cut-through switching support
DHCP Snooping (IPv4 and IPv6)	Double VLAN/VMAN tagging
Flow-based port mirroring	IGMP and MLD Snooping Querier
Independent VLAN Learning (IVL) support	IPv6 classification APIs
ISDP (CDP-interoperability)	Jumbo Ethernet frames
Multicast VLAN Registration (MVR)	Port MAC locking
VLAN MAC locking	Port mirroring
Protected ports	RSPAN
ERSPAN	IP subnet-based VLANs
MAC-based VLANs	Static MAC filtering
Voice VLANs	Selectable LAG hashing algorithm
IP source guard (IPv4 and IPv6)	Dynamic ARP inspection
MAC Authentication Bypass	MGMD snooping SSM
Switchport mode configuration	Link Dependency
IPv6 RA Guard (Stateless)	MLAG - RPVST+
STP features: Root guard, BPDU guard, TCN guard, Loop guard, BPDU filter, BPDU flood	L2 Loop Protection
Link Debounce Feature	Private VLANs: Isolated private VLAN trunk port, Promiscuous private VLAN trunk port

- System Facilities

Table 62: System Facilites RFCs

ID	Purpose	ID	Purpose
	Autoinstall		Cable test
	CPU rate limiting		Dynamic link detection
	DNS client		Event and error logging facility
	Runtime and configuration download capability		Events-based interface shutdown and recovery
	Friendly port naming		Network and host DOS protection
	IP address conflict notification		Email alerts
	PING utility		Traceroute utility
	Authentication Tiering		FTP transfers using IPv4/IPv6
	Malicious code detection	RFC 768	UDP
RFC 783	TFTP	RFC 791	IP
RFC 792	ICMP	RFC 793	TCP
RFC 826	Ethernet ARP	RFC 894	Transmission of IP Datagrams over Ethernet Networks
RFC 896	Congestion Control in IP/TCP Networks	RFC 951	BootP
RFC 1034	Domain names (concepts and facilities)	RFC 1035	Domain names (implementation and specification)
RFC 1321	Message digest algorithm	RFC 1534	Interoperability between BootP and DHCP
RFC 2021	Remote Network Monitoring Management Information base v2	RFC 2030	Simple Network Time Protocol (SNTP) v4 for IPv4, IPv6, and OSI
RFC 2131	DHCP Client/Server	RFC 2132	DHCP options and BootP vendor extensions
RFC 2347	TFTP Option Extension	RFC 2348	TFTP Blocksize Option
RFC 2819	Remote Network Monitoring Management Information Base	RFC 2830	TLS support for LDAP
RFC 2865	RADIUS client	RFC 2866	RADIUS accounting
RFC 2868	RADIUS attributes for tunnel protocol support	RFC 2869	RADIUS Extensions—Support for Extensible Authentication Protocol (EAP)
RFC 3162	RADIUS and IPv6	RFC 3164	BSD syslog protocol
RFC 3580	802.1X RADIUS usage guidelines	RFC 4511	LDAP protocol
RFC 4515	Lightweight Directory Access Protocol (LDAP): String Representation of Search Filters	RFC 5176	Dynamic Authorization Server (Disconnect-Request processing only)
RFC 5424	Syslog protocol	TACACS+	Client with support for IPv4 and IPv6 functionality
sFlow Version 5	Industry standard for sFlow implementation	sFlow LAG Counters Structure	Standard to export LACP counters in the sFlow counter sample for a port that is a member of a LAG
	Tracking of LAG flaps		

- **Switching MIBs**

Table 63: Switching MIBs

ID	Purpose	ID	Purpose
RFC 1213	MIB-II	RFC 1493	Bridge MIB
RFC 1612	DNS Resolver MIB Extensions	RFC 1643	Ethernet-like MIB
RFC 2011	IP-MIB	RFC 2233	Interfaces Group MIB using SMI v2
RFC 2613	SMON MIB	RFC 2618	RADIUS Authentication Client MIB
RFC 2620	RADIUS Accounting MIB	RFC 2674	Q-BRIDGE-MIB
RFC 2737	Entity MIB version 2	RFC 2819	RMON Groups 1,2,3, and 9

ID	Purpose
RFC 2863	IF-MIB
RFC 3273	RMON Groups 1,2 and 3
RFC 3434	RMON Groups 1,2, and 3
RFC 4113	UDP-MIB
IEEE 802.1AB	LLDP MIB
	FASTPATH Enterprise MIBs supporting Switching features

ID	Purpose
RFC 2925	Definitions of Managed Objects for Remote Ping, Traceroute, and Lookup Operations
RFC 3291	INET-ADDRESS-MIB
RFC 4022	TCP-MIB
IEEE 802.1X	MIB (IEEE 802.1-PAE-MIB 2004 Revision)
ANSI/TIA-1057	LLDP-MED MIB

10.1.3 Routing

Table 64: Routing Functionalities

ID	Purpose
	ECMP
	Loopback interfaces
	OSPF
	RIP
	Static routing
	VRRP
	Policy-Based Routing
	VRF-lite
	Configurable routing limits
	Static routes on management interface
	IP unnumbered interface
	IP SLA
RFC 1256	ICMP router discovery messages
RFC 1765	OSPF database overflow
RFC 2082	RIP-2 MD5 authentication
RFC 2328	OSPFv2
RFC 2453	RIP v2
RFC 3046	DHCP/BootP relay
RFC 3137	OSPF Stub Router Advertisement
RFC 3704	Ingress Filtering for Multihomed Networks
RFC 5798	Virtual Router Redundancy Protocol (VRRP) Version 3 for IPv4 & IPv6
RFC 5881	Bidirectional Forwarding Detection (BFD) for IPv4 & IPv6

ID	Purpose
	ICMP Throttling
	Multinetting
	ARP and Proxy ARP
	Route redistribution across RIP, BGP, and OSPF
	VLAN and port-based routing
	UDP Relay/IP Helper
	Virtual Route Forwarding
	Algorithmic longest prefix match (ALPM)
	OSPF interface flap dampening/31 subnets
	OSPF LSA flooding reduction
	Microsoft Network Load Balance (MS NLB)
RFC 1027	Using ARP to implement transparent subnet gateways (Proxy ARP)
RFC 1519	CIDR
RFC 1812	Requirements for IPv4 routers
RFC 2131	DHCP relay
RFC 2370	The OSPF Opaque LSA Option
RFC 3021	Using 31-Bit Prefixes on Point-to-Point Links
RFC 3101	The OSPF “Not So Stubby Area” (NSSA) option
RFC 3623	Graceful OSPF Restart
RFC 3768	Virtual Router Redundancy Protocol (VRRP)
RFC 5880	Bidirectional Forwarding Detection (BFD)
RFC 6860	Hiding Transit-Only networks in OSPF

Table 65: Routing MIBs (Available Through Management Module)

ID	Purpose
RFC 1724	RIP v2 MIB Extension
RFC 2096	IP Forwarding Table MIB
RFC 3636	MAU MIB

ID	Purpose
RFC 1850	OSPF MIB
RFC 2787	VRRP MIB
RFC 6527	Definitions of Managed Objects for the Virtual Router Redundancy Protocol Version 3 (VRRPv3)

ID	Purpose
	FASTPATH Enterprise MIB supporting Routing features

ID	Purpose

10.1.4 IPv6 Routing

- **Core Features**

Table 66: IPV6 Routing Core Features RFCs

ID	Purpose
RFC 1981	Path MTU for IPv6
RFC 2464	IPv6 over Ethernet
RFC 3056	Connection of IPv6 Domains through IPv4 Clouds
RFC 3315	Dynamic Host Configuration Protocol for IPv6 (DHCPv6)
RFC 3493	Basic socket interface for IPv6
RFC 3542	Advanced sockets API for IPv6
RFC 3633	IPv6 Prefix Options for Dynamic Host Configuration Protocol (DHCP) version 6
RFC 4213	Basic Transition Mechanisms for IPv6
RFC 4443	ICMPv6
RFC 4862	IPv6 stateless address autoconfiguration
RFC 5340	OSPF for IPv6
RFC 5798	Virtual Router Redundancy Protocol (VRRP) version 3
RFC 6164	Using 127-Bit IPv6 Prefixes on Inter-Router Links
	Dual IPv4/IPv6 TCP/IP Stack Operation
	6to4 automatic tunnels
	IPv6 negative ARPs
	Stateful DHCPv6 server
	OSPFv3 stub router
	OSPFv3 timers throttle

ID	Purpose
RFC 2460	IPv6 protocol specification
RFC 2711	IPv6 router alert
RFC 3306	Unicast prefix-based IPv6 multicast addresses
RFC 3484	Default address selection for IPv6
RFC 3513	Addressing architecture for IPv6
RFC 3587	IPv6 Global Unicast Address Format
RFC 3736	Stateless DHCPv6
RFC 4291	Addressing Architecture for IPv6
RFC 4861	Neighbor discovery for IPv6
RFC 5187	OSPFv3 Graceful Restart
RFC 5549	Advertising IPv4 Network Layer Reachability Information with an IPv6 Next Hop
RFC 5881	BFD for IPv4 and IPv6 (Single Hop)
RFC 6583	Operational Neighbor Discovery Problems
	ICMPv6 Throttling
	DNSv6
	IPv6/127 support
	IPv6 server lists
	OSPFv3 LSA group pacing
	OSPFv3 bundle direct ACKs

- **IPv6 Routing MIBs**

Table 67: IPV6 Routing MIBs

ID	Purpose
RFC 2465	IPv6 MIB
RFC 5643	OSPFv3 MIB

ID	Purpose
RFC 2466	ICMPv6 MIB

10.1.5 QoS

- **DiffServ**

Table 68: DiffServ RFCs

ID	Purpose
RFC 1858	Security Considerations for IP Fragment Filtering
RFC 2475	An architecture for differentiated services
RFC 2697	Single-rate policing
RFC 3246	An expedited forwarding PHB (Per-Hop Behavior)

ID	Purpose
RFC 2474	Definition of the differentiated services field (DS Field) in the IPv4 and IPv6 headers
RFC 2597	Assured forwarding PHB group
RFC 2698	A Two Rate Three Color Marker
RFC 3260	New terminology and clarifications for DiffServ

- **Access Control Lists (ACL)**

Permit/deny actions for inbound or outbound IP (IPv4 and IPv6) traffic classification based on:

- Type of service (ToS) or differentiated services (DS) DSCP field
- Source IP address
- Destination IP address
- TCP/UDP source port
- TCP/UDP destination port
- IP protocol number
- IPv6 flow label

Permit/deny actions for inbound or outbound Layer-2 traffic classification based on:

- Source MAC address
- Destination MAC address
- EtherType
- VLAN identifier value or range (outer and/or inner VLAN tag)
- IEEE 802.1p user priority (outer and/or inner VLAN tag)

DiffServ and ACL actions:

- Assign matching traffic flow to a specific queue
- Specific port redirect or mirror (flow-based mirroring) matching traffic flow
- Generate trap log entries containing rule hit counts

Class of Service (CoS):

- Auto VoIP: Automatic VoIP Class of Service (CoS) settings
- Direct user configuration of the following:
- IP DSCP to traffic class mapping
- IP precedence to traffic class mapping
- Interface trust mode: IEEE 802.1p, IP Precedence, IP DSCP, or untrusted
- Interface traffic shaping rate
- Minimum and maximum bandwidth per queue
- Strict priority versus weighted (WRR/WFQ) scheduling per queue
- Tail drop versus Weighted Random Early Detection (WRED) queue depth management

Quality of Service MIBs (Available Through Management Module)

- RFC 3289: Management Information Base for the Differentiated Services Architecture (read-only)
- Private MIBs supporting DiffServ, ACL, and CoS functionality

10.1.6 Multicast

- **Core Features**

Table 69: Multicast Core Features RFCs

ID	Purpose	ID	Purpose
RFC 1112	Host extensions for IP multicasting	RFC 2236	Internet Group Management Protocol (IGMP) version 2
RFC 2365	Administratively scoped IP multicast	RFC 2710	Multicast Listener Discovery (MLD) for IPv6
RFC 3376	Internet Group Management Protocol (IGMP), version 3	RFC 3810	Multicast Listener Discovery Version 2 (MLDv2) for IPv6
RFC 3973	Protocol Independent Multicast - Dense Mode (PIM-DM)	RFC 4601	Protocol Independent Multicast - Sparse Mode (PIM-SM)
Draft-ietf-idmr-dvmrp-v3-10	Distance Vector Multicast Routing Protocol (DVMRP)	Draft-ietf-magma-igmp-proxy-06	IGMP/MLD-based
	multicast forwarding (IGMP/MLD proxying)	Draft-ietf-magma-igmpv3-and-routing-05	IGMPv3/MLDv2 and multicast routing protocol interaction
draft-ietf-pim-sm-bsr-05	Bootstrap Router (BSR) Mechanism for PIM		draft-ietf-ssm-arch-05.txt - Source-Specific Multicast (SSM) for IP
	Static RP configuration		MLD proxy
	IGMPv3 proxy		IP multicast Traceroute
	Multihop RP		

- **Multicast MIBs**

Table 70: Multicast MIB RFCs

ID	Purpose	ID	Purpose
RFC 2932	IPv4 Multicast Routing MIB	RFC 2933	Internet Group Management Protocol MIB
RFC 5060	Protocol Independent Multicast MIB	RFC 5519	Multicast Group Membership Discovery MIB
draft-ietf-idmr-dvmrp-mib-11	Distance-Vector Multicast Routing Protocol (DVMRP) standard MIB	draft-ietf-magma-mgmd-mib-05	Multicast Group Membership Discovery MIB
draft-ietf-pim-bsr-mib-06	PIM Bootstrap Router MIB		FASTPATH Enterprise MIB supporting Multicast features

10.1.7 Data Center

- **Core Features**
  - IEEE 802.1Qau: Virtual Bridged Local Area Networks Amendment 13: Congestion Notification (Draft 2.4)
  - IEEE 802.1Qaz: Enhanced Transmission Selection (ETS) for Bandwidth Sharing Between Traffic Classes (Draft 2.4)
  - ANSI/INCITS Fibre Channel Backbone-5 (FC-BB-5) REV 2.0.0: FIP Snooping Bridge
  - OpenFlow Switch Specification, Version 1.0.0 (Wire Protocol 0x01) and Version 1.3.4

- **Data Center MIBs**
  - IEEE 802.1: Congestion Management MIB (IEEE8021-CN-MIB)
  - IEEE 802.1: Textual Conventions MIB (IEEE8021-TC-MIB)
  - IEEE 802.1: LLDP V2 TC MIB

10.2 Supported MIBS

Table 71: Supported MIBs

MIB	Purpose
Broadcom-REF-MIB	Broadcom Reference
DIFFSERV-DSCP-TC	The Textual Conventions defined in this module should be used whenever a Differentiated Services Code Point is used in a MIB.
DISMAN-PING-MIB	The Ping MIB (DISMAN-PING-MIB) provides the capability of controlling the use of the ping function at a remote host.
DISMAN-TRACEROUTE-MIB	The Traceroute MIB (DISMAN-TRACEROUTE-MIB) provides access to the traceroute capability at a remote host.
DNS-RESOLVER-MIB	The MIB module for entities implementing the client (resolver) side of the Domain Name System (DNS) protocol.
DNS-SERVER-MIB	The MIB module for entities implementing the server side of the Domain Name System (DNS) protocol.
DVMRP-STD-MIB	Distance-Vector Multicast Routing Protocol MIB
FASTPATH-AUTHENTICATION-MANAGER-MIB	The Broadcom Private MIB for FASTPATH authentication manager feature.
FASTPATH-BONJOUR-MIB	The Broadcom Private MIB for FASTPATH Bonjour
FASTPATH-BOXSERVICES-PRIVATE-MIB	The Broadcom Private MIB for FASTPATH Box Services Feature.
FASTPATH-DCBX-MIB	The MIB module defines objects to configure DCBX
FASTPATH-DENIALOFSERVICE-PRIVATE-MIB	The Broadcom Private MIB for FASTPATH Denialof Service.
FASTPATH-DHCP6SERVER-PRIVATE-MIB	The Broadcom Private MIB for FASTPATH DHCPv6 Server/Relay
FASTPATH-DHCPCLIENT-PRIVATE-MIB	The Broadcom Private MIB for FASTPATH DHCP Client
FASTPATH-DHCPSERVER-PRIVATE-MIB	The Broadcom Private MIB for FASTPATH DHCP Server
FASTPATH-DNS-RESOLVER-CONTROL-MIB	Defines a portion of the SNMP MIB under the Broadcom Corporation enterprise OID pertaining to DNS Client control configuration
FASTPATH-DOT1X-ADVANCED-FEATURES-VER-MIB	The Broadcom Private MIB for FASTPATH Dot1xAdvanced Features
FASTPATH-DOT1X-AUTHENTICATION-SERVER-MIB	The Broadcom Private MIB for FASTPATH Dot1xAuthentication Server
FASTPATH-FIPSNOOPING-MIB	The MIB module defines objects to configure FIP snooping and monitor the status of FCoE sessions.
FASTPATH-INTERFACE-APP-MIB	The Broadcom Private MIB for FASTPATH Interface Application
FASTPATH-INVENTORY-MIB	Unit and Slot configuration.
FASTPATH-IPV6-LOOPBACK-MIB	The Broadcom Private MIB for FASTPATH Loopback IPV6 address configuration.
FASTPATH-IPV6-OSPFV3-MIB	The Broadcom FASTPATH OSPFV3 MIB.
FASTPATH-IPV6-TUNNEL-MIB	The Broadcom Private MIB for FASTPATH IPV6 Tunnel.
FASTPATH-ISDP-MIB	Industry Standard Discovery Protocol MIB
FASTPATH-KEYING-PRIVATE-MIB	The Broadcom Private MIB for FASTPATH Keying Utility
FASTPATH-LDAP-CLIENT-MIB	Defines a portion of the SNMP MIB under the Broadcom Corporation enterprise OID pertaining to LDAP client configuration.
FASTPATH-LLPF-PRIVATE-MIB	The Broadcom Private MIB for FASTPATH Link Local Protocol Filtering.
FASTPATH-LOGGING-MIB	This MIB provides objects to configure and display events logged on this system.
FASTPATH-LOOPBACK-MIB	The Broadcom Private MIB for FASTPATH Loopback
FASTPATH-MAB-MIB	FASTPATH MIB for MAB specific objects
FASTPATH-MANAGEMENT-ACAL-MIB	The Broadcom Private MIB for FASTPATH management acal feature.
FASTPATH-MGMT-SECURITY-MIB	The Broadcom Private MIB for FASTPATH Mgmt Security
FASTPATH-MULTICAST-MIB	The MIB definitions for Multicast Routing Flex package.
FASTPATH-MVR-PRIVATE-MIB	The Broadcom Private MIB for MVR Configuration
FASTPATH-OUTBOUNDTELNET-PRIVATE-MIB	The Broadcom Private MIB for FASTPATH Outbound Telnet
FASTPATH-PFC-MIB	The MIB definitions Priority based Flow Control Feature.
FASTPATH-PORTSECURITY-PRIVATE-MIB	Port Security MIB.
FASTPATH-QOS-ACL-MIB	FASTPATH Flex QOS ACL
FASTPATH-QOS-AUTOVOIP-MIB	FASTPATH Flex QOS VOIP
FASTPATH-QOS-COS-MIB	FASTPATH Flex QOS COS
FASTPATH-QOS-DIFFSERV-EXTENSIONS-MIB	FASTPATH Flex QOS DiffServ ExtensionsPrivate MIBs' definitions
FASTPATH-QOS-DIFFSERV-PRIVATE-MIB	FASTPATH Flex QOS DiffServ Private MIBs' definitions
FASTPATH-QOS-ISCSI-MIB	FASTPATH Flex QOS iSCSI Flow Acceleration MIBs' definitions
FASTPATH-QOS-MIB	FASTPATH Flex QOS Support
FASTPATH-RADIUS-AUTH-CLIENT-MIB	The Broadcom Private MIB for FASTPATH Radius Authentication Client.
FASTPATH-ROUTE-POLICY-MIB	The MIB definitions for Route Policy system.
FASTPATH-ROUTING-MIB	FASTPATH Routing - Layer 3
FASTPATH-ROUTING6-MIB	The Broadcom Private MIB for FASTPATH IPv6 Routing.
FASTPATH-SFLOW-MIB	The Broadcom Private MIB for FASTPATH SFLOW

MIB	Purpose
FASTPATH-SNTP-CLIENT-MIB	Defines Broadcom Corporation enterprise OID pertaining to SNTP client configuration and statistical collection.
FASTPATH-SWITCHING-MIB	FASTPATH Switching - Layer 2
FASTPATH-TIMERANGE-MIB	The Broadcom Private MIB for FASTPATH Time Ranges
FASTPATH-UDLD-MIB	UDLD MIB
FASTPATH-VPC-MIB	The MIB definitions for VPC.
HC-ALARM-MIB	Initial version of the High Capacity Alarm MIB module. This version published as RFC 3434.
HC-RMON-MIB	The original version of this MIB, published as RFC3273.
HCNUM-TC	A MIB module containing textual conventions for high capacity data types.
IANA-ADDRESS-FAMILY-NUMBERS-MIB	The MIB module defines the AddressFamilyNumbers textual convention.
IANA-MAU-MIB	This MIB module defines dot3MauType OBJECT-IDENTITIES and IANAifMauListBits, IANAifMauMediaAvailable, IANAifMauAutoNegCapBits,
IANA-RTPROTO-MIB	IANA IP Route Protocol and IP MRoute Protocol Textual Conventions
IANAifType-MIB	This MIB module defines the IANAifType Textual Convention
IEEE 802.1X (Revision of	The MIB module for IEEE 802.1X configuration 802.1X-2004).
IEEE8021-CN-MIB	Congestion notification module for managing IEEE 802.1Qau
IEEE8021-PFC-MIB	Priority-based Flow Control module for managing IEEE 802.1Qbb
IEEE8021-TC-MIB	Textual conventions used throughout the various IEEE 802.1 MIB modules.
INET-ADDRESS-MIB	This MIB module defines textual conventions for representing Internet addresses.
IP-FORWARD-MIB	The MIB module for the management of CIDR multipath IP Routes.
IP-MIB	The MIB module for managing IP and ICMP implementations, but excluding their management of IP routes.
IPMROUTE-STD-MIB	The MIB module for management of IP Multicast routing, but independent of the specific multicast routing protocol in use.
KEX-CONFIG-MIB	The KEX Private MIB for configuration features.
KEX-DEBUG-MIB	The KEX Private MIB for debug features.
KEX-FILE-INTEGRITY-MIB	The KEX Private MIB for file integrity feature.
KEX-IPMI-MIB	The KEX Private MIB for IPMI features.
KEX-MGMT-MIB	The KEX Private MIB for board related features.
KEX-MODULE_IDENTITY	The KEX Private MIB containing the Kontron Module Identity.
KEX-NTP-MIB	The KEX Private MIB for NTP configuration.
KEX-OEM-MIB	The KEX Private MIB for OEM features.
KEX-PHY-MIB	The KEX Private MIB for PHY/SFP features.
KEX-SENSOR-MIB	The KEX Private MIB for sensor information.
KEX-VERSION-MIB	The KEX Private MIB for version information.
LAG-MIB	The Link Aggregation module for managing IEEE 802.3ad
LLDP-EXT-DOT3-MIB	The LLDP Management Information Base extension module for IEEE 802.3 organizationally defined discovery information.
LLDP-EXT-MED-MIB	The LLDP Management Information Base extension module for TIA-TR41.4 Media Endpoint Discovery information.
LLDP-MIB	Management Information Base module for LLDP configuration, statistics, local system data and remote systems data components.
LLDP-V2-TC-MIB	Textual conventions used throughout the IEEE Std 802.1AB version 2 and later MIB modules.
MGMD-STD-MIB	The MIB module for MGMD Management.
NOTIFICATION-LOG-MIB	The MIB module for logging SNMP Notifications, that is, Traps and Informs.
RADIUS-ACC-CLIENT-MIB	RADIUS Accounting Client MIB
RADIUS-AUTH-CLIENT-MIB	RADIUS Authentication Client MIB
RFC 1213 - RFC1213-MIB	Management Information Base for Network Management of TCP/IP-based internets: MIB-II
RFC 1493 - BRIDGE-MIB	Definitions of Managed Objects for Bridges (dot1d)
RFC 1724 - RIPv2-MIB	RIP Version 2 MIB Extension
RFC 1850 - OSPF-MIB	OSPF Version 2 Management Information Base
RFC 1850 - OSPF-TRAP-MIB	The MIB module to describe traps for the OSPF Version 2 Protocol.
RFC 1907 - SNMPv2-MIB	The MIB module for SNMPv2 entities
RFC 2465 - IPV6-MIB	Management Information Base for IP Version 6: Textual Conventions and General Group
RFC 2466 - IPV6-ICMP-MIB	Management Information Base for IP Version 6: ICMPv6 Group
RFC 2674 - P-BRIDGE-MIB	The Bridge MIB Extension module for managing Priority and Multicast Filtering, defined by IEEE 802.1D-1998.
RFC 2674 - Q-BRIDGE-MIB	The VLAN Bridge MIB module for managing Virtual Bridged Local Area Networks
RFC 2737 - ENTITY-MIB	Entity MIB (Version 2)
RFC 2787 - VRRP-MIB	Definitions of Managed Objects for the Virtual Router Redundancy Protocol
RFC 2819 - RMON-MIB	Remote Network Monitoring Management Information Base
RFC 2863 - IF-MIB	The Interfaces Group MIB using SMIv2
RFC 3289 - DIFFSERV-MIB	Management Information Base for the Differentiated Services Architecture
RFC 3419 - TRANSPORT-ADDRESS-MIB	Textual Conventions for Transport Addresses

MIB	Purpose
RFC 3635 - Etherlike-MIB	Definitions of Managed Objects for the Ethernet-like Interface Types
RFC 5060 - PIM-STD-MIB	Protocol Independent Multicast MIB
RFC 5240 - PIM-BSR-MIB	Bootstrap Router mechanism for PIM routers
RFC 6527 - VRRPV3-MIB	Definitions of Managed Objects for the Virtual Router Redundancy Protocol version 3
SFLOW-MIB	sFlow MIB
SMON-MIB	The MIB module for managing remote monitoring device implementations for Switched Networks
SNMP-FRAMEWORK-MIB	The SNMP Management Architecture MIB
SNMP-MPD-MIB	The MIB for Message Processing and Dispatching
SNMP-NOTIFICATION-MIB	The Notification MIB Module
SNMP-TARGET-MIB	The Target MIB Module
SNMP-USER-BASED-SM-MIB	The management information definitions for the SNMP User-based Security Model.
SNMP-VIEW-BASED-ACM-MIB	The management information definitions for the View-based Access Control Model for SNMP.
TACACS-CLIENT-MIB	Defines a portion of the SNMP MIB under the Broadcom Corporation enterprise OID pertaining to TACACS+ client configuration.
The MAC security entity (SecY)	The MIB module for IEEE 802.1X MAC SecYmodule for IEEE 802.1AE configuration.

10.3 Bootloader

On the VX6940 Ethernet Switch, the bootloader 'u-boot' (universal bootloader) is used. The bootloader initializes the main components of the system like Unit Computer, RAM, serial lines etc. for operation and performs a power on self test (POST). After these steps have been finished, kernel and application are started from flash.

10.3.1 Power On Self Tests

The bootloader of the VX6940 performs a build in self-test during the startup of the switch.

Table 72: Power On Self Tests (POST)

POST	Description	Procedure	Error Code
UART0	Serial port controller loopback	Configure the serial controller in loopback mode. Send a data pattern and re-read the looped data. The test is pass if the sent and received data are equal.	1
I2C	Check onboard I2C devices	Checks if the expected I2C peripherals respond on the I2C bus.	2
PCIe	Check PCIe device presence	Checks if the switch silicon responds on the PCIe bus. Both PCI functional instances are tested.	3
ENV	Check bootloader environment consistency	Check if the bootloader environment area in the SPI flash contains valid data. Valid data is detected either if the entire partition is empty, i.e. filled with the value FFh, or if the data checksum is correct.	5
VPD (vital product data)	Check VPD data consistency	Check if the bootloader VPD area in the SPI flash contains valid data. Valid data is detected if the data checksum is correct and VPD data MAC entry can be read.	6
DDR	Check DDR memory	Performs a memory data line and address line test. Test fails if shorts ore opens on data lines result in testpattern changes read back or if 2 different addresses in the address map will access one physical memory storage location.	8
SPI write protection	Check SPI write protection status	Check if the block protection is enabled on the lower half of the SPI flash.	13
Reset Source	Check for valid reset source	Checks if the previous board reset has been issued by a valid reset source. The test fails if an unsolicited reset is detected.	15

The status of the tests can be monitored during the board boot on serial console.

Example:

```
POST i2c PASSED
POST memory PASSED
POST uart PASSED
```

```
POST pci PASSED
POST env PASSED
POST vpd PASSED
POST spiwp PASSED
POST reset PASSED
```

The CLI provides a command to show the last POST result:

```
(Ethernet Fabric)#show board post-status system
System POST Code       : 0x00 (o.k.)
```

10.3.2 Bootloader Shell Options

The boot process can be interrupted by entering the bootstopkey phrase “stop”. This will open a bootloader shell session.

Entering “?” provides a list of possible built-in commands, “printenv” provides a list of current environment settings.

The bootloader shell can be used to customize boot options and system startup by changing some of its environment variables. There are some important environment settings influencing behavior of the board. Different settings are defined for boot monitor and failsafe bootloader. The boot monitor supports storing of environment variables in the associated 'env' volume whereas changes in failsafe bootloader environment cannot be stored permanently to avoid un-bootable boards due to environment misconfiguration.

A list of available environment variables and its description can be seen in the table below:

Table 73: Bootloader Shell Options

Name	Default Value	Description
autoload	No	Do not automatically load bootfile on bootp request.
baudrate	115200	Serial console baud rate
bootcmd	run check_integrity && run bootcmd_${bootsource}	Boot command to execute after boot delay time has been elapsed
bootcmd_mmc	run setbootargs && load mmc 0:1 ${loadaddr} /bootorder/${bootnumber} /system.itb && load mmc 0:1 ${ramdiskaddr} /bootorder/${bootnumber}/ramdisk && w dt dev kexpld_wdt && wdt ${watchdogoscmd} && bootm ${loadaddr} ${ramdiskaddr} ; run next_bootimage	Boot command to boot from emmc flash
bootcmd_net	run setbootargs && bootp && tftp ${loadaddr} ${bootfile} && wdt dev kexpld_wdt && wdt ${watchdogoscmd} && bootm ${loadaddr}	Boot command to boot from net via TFTP
bootdelay	3	Boot delay before booting from bootsource
bootnumber	1	Select the boot image
bootsource	mmc	Intended boot source.
check_integrity	wdt dev kexpld_wdt && wdt ${watchdogbootcmd} && if run check_pos terr ; then echo POST error detected - exit to CLI ; wdt stop ; false ; else true ; fi && test -n ${bootsource}	Start watchdog and check POST before booting.
check_posterr	test ${postresult} != 0 && test ${stop_posterr} != 0	Check POST result.

Name	Default Value	Description
clear_config	setenv bootargs quiet clearconfig config=${configdev} && load mmc 0:1 ${loadaddr} /bootorder/${bootnumber}/system.itb && load mmc 0:1 ${ramdiskaddr} /bootorder/${bootnumber}/ramdisk && wdt dev kexpld_wdt && wdt ${watchdogoscmd} && bootm ${loadaddr} ${ramdiskaddr}	Clean up the current configuration.
clear_env	sf probe 0 && sf erase 0x3F0000 10000	Clear bootloader environment variables in SPI flash
configdev	/dev/mmcblk0p2	Current emmc partition for the configuration.
eth1addr	00:00:de:51:fa:d0	Ethernet MAC address
eth2addr	00:00:de:51:fa:d2	Ethernet MAC address
Ethact	FM1@DTSEC2	Current network interface
Ethaddr	00:00:de:51:fa:d1	Ethernet MAC address
ethprime	FM1@DTSEC2	Primary network interface
next_bootimage	test ${is_failsafe} != 1 && pld.q write 1 1 ; reset	Select the next bootimage
postresult	0	Result of the POST
serial#	1120311030017	Board serial number.
setbootargs	setenv bootargs quiet root=/dev/mmcblk0p1:/bootorder/${bootnumber} config=${configdev}	The kernel bootargs
watchdogbootcmd	start 30000	Watchdog timeout for boot monitor initialization sequence
watchdogoscmd	start 45000	Watchdog timeout for kernel startup sequence

10.4 FASTPATH Port Mappings

10.4.1 Port Map Selection

Table 74: Port Paps

Name	Description
10g_40g-a	10G/40G Backplane, 3x 40G QSFP+
100g_uplinks-a	10G/40G Backplane, 40G QSFP+ + 2x QSFP28

```
(Ethernet Fabric)#show board port-map all
Active ID                    Description
------ --------------------  ---------------------------------------------
   *   10g_40g-a             10G/40G Backplane, 3x 40G QSFP+
       100g_uplinks-a        10G/40G Backplane, 40G QSFP+ + 2x QSFP28
```

To select a port-map:

```
(Ethernet Fabric)# set board port-map 100g_uplinks-a
```

10.4.2 Standard Port Map – 10g_40g-a

Table 75: Port Map 10g_40g-a

Fastpath Interface #	Connector / Wafer		Default Port Speed	Auto-negociate (default)	Capabilities
0/1	VPX P1 DPfp01	w1	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/2		w2	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/3		w3	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/4		w4	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/5	VPX P1 DPfp02	w5	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/6		w6	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/7		w7	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/8		w8	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/9	VPX P1 DPfp03	w9	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/10		w10	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/11		w11	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/12		w12	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/13	VPX P1 DPfp04	w13	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/14		w14	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/15		w15	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/16		w16	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/17	VPX P2 DPfp05	w1	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/18		w2	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/19		w3	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/20		w4	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/21	VPX P1 DPfp06	w5	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/22		w6	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/23		w7	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/24		w8	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/25	VPX P2 DPfp07	w9	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/26		w10	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/27		w11	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/28		w12	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/29		w13	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s

Fastpath Interface #	Connector / Wafer		Default Port Speed	Auto-negociate (default)	Capabilities
0/30	VPX P2 DPfp08	w14	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/31		w15	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/32		w16	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/33	VPX P3 DPfp09	w1	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/34		w2	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/35		w3	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/36		w4	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/37	VPX P3 DPfp10	w5	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/38		w6	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/39		w7	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/40		w8	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/41	VPX P3 DPfp11	w9	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/42		w10	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/43		w11	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/44		w12	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/45	VPX P3 DPfp12	w13	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/46		w14	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/47		w15	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/48		w16	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/49	P5 CPutp01	w2	10Gb/s	Yes (KR)	10Gb/s (KR), 1Gb/s
0/50	P5 CPutp02	w3	10Gb/s	Yes (KR)	10Gb/s (KR), 1Gb/s
0/51	P5 CPutp05	w4	10Gb/s	Yes (KR)	10Gb/s (KR), 1Gb/s
0/52	P5 CPutp06	w5	10Gb/s	Yes (KR)	10Gb/s (KR), 1Gb/s
0/53	P5 CPutp05	w6	10Gb/s	Yes (KR)	10Gb/s (KR), 1Gb/s
0/54	P5 CPutp06	w7	10Gb/s	Yes (KR)	10Gb/s (KR), 1Gb/s
0/55	P5 CPutp07	w8	10Gb/s	Yes (KR)	10Gb/s (KR), 1Gb/s
0/56	P6 CPutp08	w1	10Gb/s	Yes (KR)	10Gb/s (KR), 1Gb/s
0/57	Front QSFP1		40Gb/s	No	40Gb/s (KR4, SR4), 10Gb/s (KR, SR), 1Gb/s
0/58			Detached	No	10Gb/s (KR, SR), 1Gb/s
0/59			Detached	No	10Gb/s (KR, SR), 1Gb/s
0/60			Detached	No	10Gb/s (KR, SR), 1Gb/s

Fastpath Interface #	Connector / Wafer	Default Port Speed	Auto-negociate (default)	Capabilities
0/61	Front QSFP2	40Gb/s	No	40Gb/s (KR4, SR4), 10Gb/s (KR, SR), 1Gb/s
0/62		Detached	No	10Gb/s (KR, SR), 1Gb/s
0/63		Detached	No	10Gb/s (KR, SR), 1Gb/s
0/64		Detached	No	10Gb/s (KR, SR), 1Gb/s
0/65	Front QSFP3	40Gb/s	No	40Gb/s (KR4, SR4), 10Gb/s (KR, SR), 1Gb/s
0/66		Detached	No	10Gb/s (KR, SR), 1Gb/s
0/67		Detached	No	10Gb/s (KR, SR), 1Gb/s
0/68		Detached	No	10Gb/s (KR, SR), 1Gb/s
0/69	NC (1)	1G/s	Yes	1Gb/s
0/70	ShMC (2)	1G/s	Yes	1Gb/s
0/71	T1042 eth1 (3)	1G/s	Yes	1Gb/s
0/72	T1042 eth2 (3)	1G/s	Yes	1Gb/s

(1) The 0/69 can be redirected to be linked to the MNGT port (front) in place of the Service Port (FastPath management port). Refer to chapter 10.5.7.

(2) The 0/70 interface is by default routed to the ShMC. It can be routed to the front panel DATA port. Refer to chapter 10.5.6

(3) 0/71 and 0/72 interfaces are reserved.

10.4.3 100Gb Port Map - 100g_uplinks-a

Table 76: Port Map 100g_uplinks-a

Fastpath Interface #	Connector / Wafer		Default Port Speed	Auto-negociate (default)	Capabilities
0/1	VPX P1 DPfp01	w1	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/2		w2	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/3		w3	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/4		w4	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/5	VPX P1 DPfp02	w5	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/6		w6	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/7		w7	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/8		w8	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/9	VPX P1 DPfp03	w9	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/10		w10	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/11		w11	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/12		w12	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/13	VPX P1 DPfp04	w13	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/14		w14	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/15		w15	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/16		w16	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/17	VPX P2 DPfp05	w1	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/18		w2	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/19		w3	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/20		w4	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/21	VPX P1 DPfp06	w5	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/22		w6	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/23		w7	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/24		w8	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/25	VPX P2 DPfp07	w9	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/26		w10	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/27		w11	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/28		w12	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/29		w13	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s

Fastpath Interface #	Connector / Wafer		Default Port Speed	Auto-negociate (default)	Capabilities
0/30	VPX P2 DPfp08	w14	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/31		w15	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/32		w16	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/33	VPX P3 DPfp09	w1	40Gb/s	Yes (KR4)	40Gb/s (KR4), 10Gb/s (KR), 1Gb/s
0/34		w2	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/35		w3	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/36		w4	Detached	Yes (KR)	10Gb/s (KR), 1Gb/s
0/37	VPX P3 DPfp10	w5	Detached	-	-
0/38		w6	Detached	-	-
0/39		w7	Detached	-	-
0/40		w8	Detached	-	-
0/41	VPX P3 DPfp11	w9	Detached	-	-
0/42		w10	Detached	-	-
0/43		w11	Detached	-	-
0/44		w12	Detached	-	-
0/45	VPX P3 DPfp12	w13	Detached	-	-
0/46		w14	Detached	-	-
0/47		w15	Detached	-	-
0/48		w16	Detached	-	-
0/49	P5 CPutp01	w2	10Gb/s	Yes (KR)	10Gb/s (KR,), 1Gb/s
0/50	P5 CPutp02	w3	10Gb/s	Yes (KR)	10Gb/s (KR,), 1Gb/s
0/51	P5 CPutp05	w4	10Gb/s	Yes (KR)	10Gb/s (KR,), 1Gb/s
0/52	P5 CPutp06	w5	10Gb/s	Yes (KR)	10Gb/s (KR,), 1Gb/s
0/53	P5 CPutp05	w6	10Gb/s	Yes (KR)	10Gb/s (KR,), 1Gb/s
0/54	P5 CPutp06	w7	10Gb/s	Yes (KR)	10Gb/s (KR,), 1Gb/s
0/55	P5 CPutp07	w8	10Gb/s	Yes (KR)	10Gb/s (KR,), 1Gb/s
0/56	P6 CPutp08	w1	10Gb/s	Yes (KR)	10Gb/s (KR,), 1Gb/s
0/57	Front QSFP1		40Gb/s	No	40Gb/s (KR4, SR4), 10Gb/s (KR, SR), 1Gb/s
0/58			Detached	No	10Gb/s (KR, SR), 1Gb/s
0/59			Detached	No	10Gb/s (KR, SR), 1Gb/s
0/60			Detached	No	10Gb/s (KR, SR), 1Gb/s

Fastpath Interface #	Connector / Wafer	Default Port Speed	Auto-negociate (default)	Capabilities
0/61	Front QSFP2	100Gb/s	No	100Gb/s (SR4), 50Gb/s (SR2), 40Gb/s (CR4), 25Gb/s (SR), 10Gb/s (CR), 1Gb/s
0/62		Detached	No	25Gb/s (SR), 10Gb/s (CR), 1Gb/s
0/63		Detached	No	50Gb/s (SR2) 25Gb/s (SR), 10Gb/s (CR), 1Gb/s
0/64		Detached	No	25Gb/s (SR), 10Gb/s (CR), 1Gb/s
0/65	Front QSFP3	100Gb/s	No	100Gb/s (SR4), 50Gb/s (SR2), 40Gb/s (CR4), 25Gb/s (SR), 10Gb/s (CR), 1Gb/s
0/66		Detached	No	25Gb/s (SR), 10Gb/s (CR), 1Gb/s
0/67		Detached	No	50Gb/s (SR2) 25Gb/s (SR), 10Gb/s (CR), 1Gb/s
0/68		Detached	No	25Gb/s (SR), 10Gb/s (CR), 1Gb/s
0/69	NC **(1)**	1G/s	Yes	1Gb/s
0/70	ShMC **(2)**	1G/s	Yes	1Gb/s
0/71	T1042 eth1 **(3)**	1G/s	Yes	1Gb/s
0/72	T1042 eth2 **(3)**	1G/s	Yes	1Gb/s

(1) The 0/69 can be redirected to be linked to the MNGT port (front) in place of the Service Port (FastPath management port). Refer to chapter 10.5.7.

(2) The 0/70 interface is by default routed to the ShMC. It can be routed to the front panel DATA port. Refer to chapter 10.5.6.

(3) 0/71 and 0/72 interfaces are reserved.

10.5 Firmware Administration

A running VX6940 system requires – once the bootloader has passed control to the kernel: the kernel itself, the root file system (initrd) and the FASTPATH switching application. These software components make up the VX6940 firmware.

The board implements two system storage devices:

- A SPI Flash device used as the primary boot source. As its size is not sufficient to hold all system software, only the startup SPL code is loaded during normal boot.
- An eMMC Flash device which holds the system software loaded by the SPL code. The eMMC device uses volumes to store the different system images needed.

10.5.1 SPI Flash Layout

Table 77: SPI Flash Layout

Partition	Offset	Size (bytes)	Name	Write Protection in Field	Description
mtd0	0	1C0000	failsafe boot code (rcw, pbl, spl, bootloader)	yes	
mtd1	1C0000	30000	reserved0	yes	Currently this board does not require a firmware blob for usual operation. Reserved for future use.
mtd2	1F0000	10000	vpd	yes	
mtd3	200000	1F0000	reserved1		Currently this board does not require a firmware blob for usual operation. Reserved for future use.
mtd4	3F0000	10000	environment		

10.5.2 EMMC Layout

Table 78: eMMC Layout

Partition	Size (bytes)	Description
mmcblk0p1	1.369.559.040	boot
mmcblk0p2	510.496.768	volatile

10.5.3 Updating Firmware

A complete software release for the VX6940 consists of one file: vx6940-system-GA-X.00-YYYYMMDDHH.pkg

The system update package contains an image of bootloader, kernel, root filesystem and config partition as well as a

MD5 checksum file for consistency check.

The firmware - including bootloader - image is updated using the CLI. The following precautions are met to ensure a reliable and failsafe update procedure:

Two independent system partitions, containing image1 system and image2 system firmware. Image1 system is

stored in flash mtd partitions mtd1, image2 system is a verbatim copy of primary system and is stored in flash partition mtd2 as a whole. This allows flash recovery from the redundant system in case that update fails due to power loss or similar errors.

The CLI commands described below are executed in the privileged mode of the CLI hierarchy, which is entered by executing the ‘enable’ command. Please refer to the “VX6940 CLI Reference Manual“ for more information regarding the CLI commands and the way to use them.

When performing a firmware update, the software package is loaded from a remote server (TFTP, HTTP, SSH). A software update of the VX6940 is done by performing the following steps (example):

1. Prepare network access of the system.

2. Log in to the privileged exec mode of the CLI of the system.

3. Check which image is in use:

```
(Ethernet Fabric)#show bootvar
 image1 : System Firmware
 image2 : System Firmware
 -------------------------  -------------------------  --------------  -----------
 image1                     image2                     current-active  next-active
 -------------------------  -------------------------  --------------  -----------
 HEAD-0.00-20200612140219   HEAD-0.00-20200701081214    image2          image2
```

4. Copy new system image into the alternate image, not the current-active one, of the flash memory. Note that the URL may be based on http, scp or tftp:

```
(Ethernet Fabric)#copy tftp://update-server/system.pkg image1

Mode........................................... TFTP
Set Server IP.................................. update-server
Path..........................................
Filename....................................... system.pkg
Data Type...................................... Code
Destination Filename........................... image1

Management access will be blocked for the duration of the transfer
Are you sure you want to start? (y/n) y

File transfer in progress. Management access will be blocked for the duration of the
transfer. Please wait...
TFTP Code transfer starting...
Write image to flash starting...

File transfer operation completed successfully.
```

5. Then, activate the new image :

```
(Ethernet Fabric)#boot system image1
(Ethernet Fabric)#show bootvar
 image1 : System Firmware
 image2 : System Firmware
 -------------------------  -------------------------  --------------  -----------
 image1                     image2                     current-active  next-active
 -------------------------  -------------------------  --------------  -----------
 HEAD-0.00-20200722220202   HEAD-0.00-20200701081214    image2          image1
```

6. Restart the board using the reload command:

```
(Ethernet Fabric)#reload
…
```

7. At the next reboot:

```
(Ethernet Fabric)#show bootvar
 image1 : System Firmware
```

```
image2 : System Firmware
-------------------------  -------------------------  -------------  -----------
image1                     image2                     current-active  next-active
-------------------------  -------------------------  -------------  -----------
HEAD-0.00-20200722220202   HEAD-0.00-20200701081214   image1          image1
```

10.5.4 Vital Product Data

The identification data of the switch are available with the CLI command:

```
(Ethernet Fabric)#show board version
Product Information
  System description        : kontron VX6940-SA-B19208, GA-6.00-20210607152557, Linux
5.4.23
  Product name              : VX6940-SA-B19208
  Product serial number     : 1120311030017
  Product part number       : 1066-6707
  Product manufacturer      : kontron
  Board name                : VX6940-SA-B19208
  Board serial number       : 1120311030017
  Board part number         : 1066-6707
  Board manufacturer        : kontron
  Board eclevel             : 10002A0
  Board variant             : 000C0300001C9C02
  Fastpath version          : 8.6.0.3-FastPath-Ent-esw-xgs5-kex-R-CLNT-D6AIQH
```

10.5.5 Expand Interfaces (40G to 4x10G or 100G to 4x25G)

With the following Fastpath CLI command, it is possible to expand a 40G or 100G interface into 4 10G, respectively 25G, interfaces:

```
(Ethernet Fabric) #configure
(Ethernet Fabric)(Config)#interface 0/65,0/61
(Ethernet Fabric)(Interface 0/65,0/61)# hardware profile portmode expand
```

To go back to one interface instead of 4:

```
(Ethernet Fabric) #configure
(Ethernet Fabric)(Config)#interface 0/9-0/12
(Ethernet Fabric)(Interface 0/9-0/12)#no hardware profile portmode expand
```

10.5.6 Configure DATA port ETH1

By default, the DATA port is not configured. The related switch interface 0/70 is connected to the ShMC.

It is possible to connect the DATA port to the switch at the interface 0/70 by editing the file /etc/default/fastpath:

```
(Ethernet Fabric)#linuxsh
/ # vi /etc/default/fastpath
## start Fastpath in diag mode
# FP_OPTS="-diag"

## un-comment the following line to connect the first 1G Phy
## to the switch port 69. It is connected to the unit computer eth0 by default.
#export FP_SERVICE_PORT_MODE=switch

## Use the FP_SERVICE_PORT_MUX variable to connect the first 1G Phy with
```

```
## the line side to the front panel or backplane (VPX P6, CPext01). Set
## therefore the value **backplane** or `front`. It is connected to the front
## panel by default except for rugged variant where it is set to backplane
## by default.
#export FP_SERVICE_PORT_MUX=backplane

## un-comment the following line to connect the second 1G Phy with the host side
## to the switch port 70. By default the host side connects to the BMC.
# export FP_LAN_PORT_MODE=switch

## Use the FP_LAN_PORT_MUX variable to connect the second 1G Phy with
## the line side to the front panel or backplane. On SA boards, this interface connects
## to the front panel by default. On RC boards, the default connection goes
## to the backplane. Valid parameters are "backplane" or "front".
#export FP_LAN_PORT_MUX=backplane
```

Uncomment the line '# export FP_LAN_PORT_MODE=switch'

```
/ # exit
Connection closed by foreign host.
(Ethernet Fabric)# reload
```

Note that it is also possible to route this interface to the front or to the backplane using the FP_LAN_PORT_MUX variable.

10.5.7 Configure MNGT port ETH0

By default, the management port ETH0 is link to the CPU and is used as the Service Port of Fastpath.

It is possible to connect the MNGT port ETH0 to the switch at the interface 0/69 by editing the file /etc/default/fastpath. Take care of the fact that the Service port will not be available to manage Fast, so it is advised to setup the network port to get access to a management interface of Fastpath instead of the Service port:

```
(Ethernet Fabric)#linuxsh
/ # vi /etc/default/fastpath
## start Fastpath in diag mode
# FP_OPTS="-diag"

## un-comment the following line to connect the first 1G Phy
## to the switch port 69. It is connected to the unit computer eth0 by default.
#export FP_SERVICE_PORT_MODE=switch

## Use the FP_SERVICE_PORT_MUX variable to connect the first 1G Phy with
## the line side to the front panel or backplane (VPX P6, CPext01). Set
## therefore the value **backplane** or `front`. It is connected to the front
## panel by default except for rugged variant where it is set to backplane
## by default.
#export FP_SERVICE_PORT_MUX=backplane

## un-comment the following line to connect the second 1G Phy with the host side
## to the switch port 70. By default the host side connects to the BMC.
# export FP_LAN_PORT_MODE=switch

## Use the FP_LAN_PORT_MUX variable to connect the second 1G Phy with
## the line side to the front panel or backplane. On SA boards, this interface connects
```

```
## to the front panel by default. On RC boards, the default connection goes
## to the backplane. Valid parameters are "backplane" or "front".
#export FP_LAN_PORT_MUX=backplane
```

Uncomment the line '#export FP_SERVICE_PORT_MODE=switch'

```
/ # exit
Connection closed by foreign host.
(Ethernet Fabric)# reload
```

Note that it is also possible to route this interface to the front or to the backplane using the FP_SERVICE_PORT_MUX variable.

10.5.8 IBIT (User/Operator-initiated Built-in Self-test)

A set of CLI Fastpath commands can be used to perform diagnostics and tests of the interfaces and functionnalities of the switch.

- **Port Link State**

The user can monitor the state of the port link by the management interface.

Example:

```
(Ethernet Fabric)#show port 0/57

                 Admin     Physical   Physical   Link   Link    LACP   Actor
Intf      Type   Mode      Mode       Status     Status Trap    Mode   Timeout
--------- ------ --------- ---------- ---------- ------ ------- ------ --------
0/57             Enable    10G Full   10G Full   Up     Enable  Enable long
```

- **Interface Counters**

The user can monitor various port related counters as packet receive and transmit error and link flaps counters.

Example:

```
(Ethernet Fabric)#show interface 0/57

Packets Received Without Error..................... 20775153
Packets Received With Error........................ 0
Broadcast Packets Received......................... 0
Receive Packets Discarded.......................... 0
Packets Transmitted Without Errors................. 19923636
Transmit Packets Discarded......................... 0
Transmit Packet Errors............................. 0
Collision Frames................................... 0
Number of link down events......................... 0
Load Interval...................................... 300
Bits Per Second Received........................... 236678704
Bits Per Second Transmitted........................ 225462488
Packets Per Second Received........................ 57784
Packets Per Second Transmitted..................... 55479
Percent Utilization Received....................... 2%
Percent Utilization Transmitted.................... 2%
Link Flaps......................................... 0
Time Since Counters Last Cleared................... 0 day 0 hr 1 min 24 sec
```

Detailed RMON compliant statistics are available.

Example:

```
(Ethernet Fabric)#show interface ethernet 0/57

Total Packets Received (Octets)................ 38195560960
Packets Received 64 Octets..................... 0
Packets Received 65-127 Octets................. 0
Packets Received 128-255 Octets................ 0
Packets Received 256-511 Octets................ 0
Packets Received 512-1023 Octets............... 74600704
Packets Received 1024-1518 Octets.............. 0
Packets Received 1519-2047 Octets.............. 0
Packets Received 2048-4095 Octets.............. 0
Packets Received 4096-9216 Octets.............. 0
Good Packets Received > 1518 Octets............ 0
Packets RX and TX 64 Octets.................... 0
Packets RX and TX 65-127 Octets................ 0
Packets RX and TX 128-255 Octets............... 0
Packets RX and TX 256-511 Octets............... 61327872
Packets RX and TX 512-1023 Octets.............. 74600704
Packets RX and TX 1024-1518 Octets............. 0
Packets RX and TX 1519-2047 Octets............. 0
Packets RX and TX 2048-4095 Octets............. 0
Packets RX and TX 4096-9216 Octets............. 0

Total Packets Received Without Errors.......... 74600660
Unicast Packets Received....................... 74600660
Multicast Packets Received..................... 0
Broadcast Packets Received..................... 0

Receive Packets Discarded...................... 0

Total Packets Received with MAC Errors......... 0
Jabbers Received............................... 0
Fragments Received............................. 0
Undersize Received............................. 0
Alignment Errors Received...................... 0
FCS Errors Received............................ 0
Overruns Received.............................. 0
URPF Discards.................................. 0

Total Received Packets Not Forwarded........... 0
802.3x Pause Frames Received................... 0
Unacceptable Frame Type........................ 0

Total Packets Transmitted (Octets)............. 31154558468
Packets Transmitted 64 Octets.................. 0
Packets Transmitted 65-127 Octets.............. 0
Packets Transmitted 128-255 Octets............. 0
Packets Transmitted 256-511 Octets............. 61327872
Packets Transmitted 512-1023 Octets............ 0
Packets Transmitted 1024-1518 Octets........... 0
```

```
Packets Transmitted > 1518 Octets.............. 0
Max Frame Size................................. 1518
Maximum Transmit Unit.......................... 1500

Total Packets Transmitted Successfully......... 61327871
Unicast Packets Transmitted.................... 61327871
Multicast Packets Transmitted.................. 0
Broadcast Packets Transmitted.................. 0

Transmit Packets Discarded..................... 0

Total Transmit Errors.......................... 0
FCS Errors Transmitted......................... 0
Transmit errors................................ 0
Jabbers Transmitted............................ 0

Total Transmit Packets Discarded............... 0
Single Collision Frames........................ 0
Multiple Collision Frames...................... 0
Excessive Collision Frames..................... 0

802.3x Pause Frames Transmitted................ 0
GVRP PDUs received............................. 0
GVRP PDUs transmitted.......................... 0
GVRP failed registrations...................... 0
GMRP PDUs received............................. 0
GMRP PDUs transmitted.......................... 0
GMRP failed registrations...................... 0

STP BPDUs Transmitted.......................... 0
STP BPDUs Received............................. 0
RSTP BPDUs Transmitted......................... 0
RSTP BPDUs Received............................ 0
MSTP BPDUs Transmitted......................... 0
MSTP BPDUs Received............................ 0
SSTP BPDUs Transmitted......................... 0
SSTP BPDUs Received............................ 0

EAPOL Frames Transmitted....................... 0
EAPOL Start Frames Received.................... 0

Load Interval.................................. 300
Bits Per Second Received....................... 689026144
Bits Per Second Transmitted.................... 550479008
Packets Per Second Received.................... 168222
Packets Per Second Transmitted................. 135456
Percent Utilization Received................... 6%
Percent Utilization Transmitted................ 5%

Time Since Counters Last Cleared............... 0 day 0 hr 4 min 22 sec
```

Optical Modules Monitoring

The switch management application provides DDM/DOM information of optical modules (if implemented by it).

Example:

```
(Ethernet Fabric)#show sfp 0/57 detail

SFP 0/57:
  eeprom
        (checksum correct)
    Identifier               : 0x0d (QSFP+)
    Extended Identifier      : 0x10 (Power Class 1 (1.5W max),CLEI)
    Connector                : 0x0c (MPO 1x12)
    Compliance               : 0x04 0x00 0x00 0x00 0x00 0x00 0x00 0x00
                               - 10G/40G Ethernet Compl.  : 40G BASE-SR4
    Encoding                 : 0x05 (64B66B)
    Nominal bit rate         : 10300 MBit/sec
    Ext. rateselect compl.   : 0x00
    Length SMF               : 0 km
    Length OM3 50 um         : 150 meter
    Length OM2 50 um         : 0 meter
    Length OM1 62.5 um       : 0 meter
    Length copper            : 0 meter
    Device technology        : 0x00
    Vendor name              : FS
    Extended module          : 0x00
    Vendor IEEE ID           : 0x9065
    Vendor part number       : QSFP-SR4-40G
    Vendor revision          : B
    Laser wavelength         : 17000 (x 0.05 nm)
    Wavelength tolerance     : 2000 (x 0.005 nm)
    Max case temperature     : 70 degrees C
    Extended Compliance      : 0x00
    Options                  : 0x01 0x04 0xd8
    Vendor serial number     : G1906332052
    Vendor date              : 2020.19.08 06
    Diagnostic monitoring    : 0x0e (txPower/rxPower)
    Enhanced options         : 0x00
    Nominal bit rate         : 0 MBit/sec

  eeprom - diagnostic
    Identifier               : 0x0d (QSFP+)
    Status: memory-Map Vers  : 0xd2
    Status Indicators        : 0x02 (paging)
    Interrupt Flags
      LOS (Rx/Tx1-4)         : 0x00
      TX-Fault (Tx1-4)       : 0x00
      Temperature Alarm      : 0x00
      VCC-Alarm              : 0x00
      Vendor specific        : 0xd2
      Rx Power Alarm         : 0x00 0x00
      Tx Bias Alarm          : 0x00 0x00
```

```
    Tx Power Alarm          : 0x00 0x00
    reserved                : 0xd2 0xd2 0xd2 0xd2
    Vendor specific         : 0xd2 0xd2 0xd2
  Module Monitors
    Temperature             : 39.00 degrees C
    reserved                : 0xd2 0xd2
    Supply Voltage          : 3.33 Volt
    Vendor specific         : 0xd2 0xd2 0xd2 0x00
  Channel monitors
    (Channel)               :   (chnl 1)  (chnl 2)  (chnl 3)  (chnl 4)
    Rx Power                :      0.53      0.51      0.40      0.40  mWatt
    Tx Bias                 :      6.20      6.08      6.14      6.10  mAmpere
    Tx Power                :      1.08      1.06      1.07      1.06  mWatt
  Control Bytes
    Disable (Tx1-4)         : 0x00
    Rate Select (Rx1-4)     : 0x00
    Rate Select (Tx1-4)     : 0x00
    Power status bits       : 0x00
    CDR_control (Rx/Tx1-4)  : 0x00
    In/Out signal control   : 0x00
  Module and Channel Masks
    LOS Mask (Rx/Tx1-4)     : 0x00
    Fault Mask (Tx1-4)      : 0x00
    CDR LOL Mask (Rx/Tx1-4): 0x00
    Temperature Alarm Mask  : 0x00
    VCC Alarm Mask          : 0x00
    Vendor specific         : 0x00 0x1f
  Password Change Area      : 0x00 0x00 0x00 0x00
  Password Entry Area       : 0x00 0x00 0x00 0x00
  Page Select Byte          : 0x00

eeprom - page 3
  Thresholds
    (threshold)             :   (HiAlrm) (LowAlrm)  (hiWarn) (lowWarn)
    Temperature             :     85.00    -10.00     70.00      0.00  degrees C
    Supply Voltage          :      3.60      2.90      3.50      3.10  Volt
    Rx Power Alarm          :      2.51      0.01      1.73      0.03  mWatt
    Tx Bias Alarm           :     15.00      0.00     12.00      2.00  mAmpere
    Tx Power Alarm          :      2.51      0.08      1.73      0.17  mWatt
  Tx Equalizer/Rx Emphasis : 0x00
  Rx Output Amplitude       : 0x00
  Control options advertise: 0x00 0x00 0x00 0x00
  Optional Channel Controls: 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x00 0xff 0xff 0xff 0xff
  Channel Monitor Masks     : 0x00 0x00 0x00 0x00 0xff 0xff 0xff 0xff 0xff 0xff
```

Selected DDM/DOM parameters of a module, like temperature and supply voltage, are also available as a dedicated sensor.

Example:

```
(Ethernet Fabric)#show board sensor slot sfp

Number   Sensor Name                          Value    Unit       Status
-------- ------------------------------------ -------- ---------- -----------
```

```
4/1      QSFP 57 Temperature                  39.000 degrees C  ok
4/2      QSFP 57 Supply Voltage                3.340 Volts      ok
4/3      QSFP 61 Temperature                  36.480 degrees C  ok
4/4      QSFP 61 Supply Voltage                3.340 Volts      ok
4/5      QSFP 65 Temperature                   0.000 degrees C  not-present
4/6      QSFP 65 Supply Voltage                0.000 Volts      not-present
```

Board Operational Parameters

The switch management application exports various board level parameters, like temperature, voltage, power, current strength as a sensor. Various measure points are implemented.

Example: Reading of all voltage sensors

```
(Ethernet Fabric)#show board sensor all | include Volts
Reading sensors, this may take some seconds ...

1/21     Vcc +12V IN                         11.780 Volts      ok
1/22     Vcc +5V SUS                          4.963 Volts      ok
1/23     Vcc +3.3V SUS                        3.356 Volts      ok
1/24     Vcc +2.5V SUS                        2.486 Volts      ok
1/25     Vcc +1.8V SUS                        1.795 Volts      ok
1/26     Vcc +1.35V SUS                       1.337 Volts      ok
1/27     Vcc +1.2V_SUS                        1.176 Volts      ok
1/28     Vcc SDXC                             3.342 Volts      ok
1/29     Vcc VTT DDR                          0.672 Volts      ok
1/30     Vcc +3.3V                            3.342 Volts      ok
1/31     Vcc +1.8V                            1.795 Volts      ok
1/32     Vcc +1.35V                           1.323 Volts      ok
1/33     Vcc +3.3V MDIO                       0.000 Volts      ok
1/34     Vcc +1.15V_SUS                       1.134 Volts      ok
1/35     Vcc +1.25V                           1.253 Volts      ok
1/36     Vcc +1.0V UC                         0.994 Volts      ok
1/37     Vcc +1.0V Core                       0.994 Volts      ok
1/38     Vcc +1.0V Analog                     0.987 Volts      ok
1/39     VBAT +3V                             3.215 Volts      ok
1/49     PSU1:Volt In                         0.000 Volts      ok
1/51     PSU1:Volt Out                        0.000 Volts      ok
1/60     PSU2:Volt In                         0.000 Volts      ok
1/62     PSU2:Volt Out                        0.000 Volts      ok
4/2      QSFP 57 Supply Voltage               3.340 Volts      ok
4/4      QSFP 61 Supply Voltage               3.340 Volts      ok
4/6      QSFP 65 Supply Voltage               0.000 Volts      not-present
```

Chassis Fan

The fan rotation speed in supported chassis types are exported as a sensor.

Example:

```
(Ethernet Fabric)#show board sensor slot rtm | include RPM

5/3      RTM Fan 1                         3960.000 RPM        n/a
5/4      RTM Fan 2                         4050.000 RPM        n/a
5/5      RTM Fan 3                         3960.000 RPM        n/a
```

Rear Transmission Module

The fan rotation speed in a supported chassis types are exported as a sensor.

Example:

```
(Ethernet Fabric)#show board sensor slot rtm | include Temp

        5/1      RTM Temperature 1                    26.250 degrees C  ok
        5/2      RTM Temperature 2                    30.750 degrees C  ok
```

10.5.9 CBIT (Continuous Built-in Self-test)

Continuous built-in Tests (CBIT) are used to get a status of the interfaces and functions during the up-time of the switch in a automatic way and with a minimum of intrusion and use of resources.

Unit Computer Memory

The CPU's memory controller detects single and double bit errors during a read operation. The Linux EDAC subsystem monitors the occurrence of such an error and reports it to the switch management application. The switch management application logs this event and generates an SNMP trap towards a management application.

Example:

```
(Ethernet Fabric)#show logging buffered | include EDAC

<189> Jun  2 16:43:28 10.0.114.166-1 TRAPMGR[emWeb]: traputil.c(772) 14084 %% NOTE EDAC
counter found: mc0, csrow1: ce-count=20, ue-count=999
```

Interface Link State

The link state of the switch ports are periodically monitored. Link state change events are logged and forwarded as SNMP trap.

Example:

```
(Ethernet Fabric)#show logging buffered | include "Link Up"

<189> Jun  2 16:14:37 10.0.114.166-1 TRAPMGR[trapTask]: traputil.c(721) 13735 %% NOTE Link
Up: 0/8
<189> Jun  2 16:14:37 10.0.114.166-1 TRAPMGR[trapTask]: traputil.c(721) 13734 %% NOTE Link
Up: 0/7
<189> Jun  2 16:14:37 10.0.114.166-1 TRAPMGR[trapTask]: traputil.c(721) 13733 %% NOTE Link
Up: 0/6
<189> Jun  2 16:14:37 10.0.114.166-1 TRAPMGR[trapTask]: traputil.c(721) 13732 %% NOTE Link
Up: 0/5
<189> Jun  2 16:14:34 10.0.114.166-1 TRAPMGR[trapTask]: traputil.c(721) 13543 %% NOTE Link
Up: 0/72
<189> Jun  2 16:14:34 10.0.114.166-1 TRAPMGR[trapTask]: traputil.c(721) 13541 %% NOTE Link
Up: 0/71
<189> Jun  2 16:14:34 10.0.114.166-1 TRAPMGR[trapTask]: traputil.c(721) 13537 %% NOTE Link
Up: 0/70
```

Optical Modules State

The change of the presence state of optical modules is reported in the syslog and forwarded as SNMP trap.

Example

```
(Ethernet Fabric)#show logging buffered | include "SFP"

<189> Jun  2 16:14:37 10.0.114.166-1 TRAPMGR[KEX-SFP-PRESENT]: traputil.c(772) 13726 %%
NOTE SFP Inserted: 0/65
```

Sensor Monitoring

Sensors which are exported from the switch management application can periodically monitored by setting an RMON alarm.

Example: Script to setup RMON Alarm Events on a linux server

```
#!/bin/bash
HOST=192.168.0.1

OID_RMON=SNMPv2-SMI:mib-2.16
OID_EVENT_ENTRY=${OID_RMON}.9.1.1
OID_ALARM_ENTRY=${OID_RMON}.3.1.1

# As an example for monitoring I use the RTM FAN speed because I can
# change the speed by setting a fixed speed.
# The OID is kexSensorCurrentValue (.1.3.6.1.4.1.15000.13.2.1.5)
# see KEX-SENSOR-MIB. The index is unit=0, slot=RTM (5), and slot-number
# one of the FAN speeds (e.g.4).
OID_FAN_SPEED=.1.3.6.1.4.1.15000.13.2.1.5.0.5.4

# First create the Event
# eventIndex is a unique Number.
# Used fields in RMON Event Table:
#    eventStatus(7) with values: valid(1),
#                                createRequest(2),
#                                underCreation(3),
#                                invalid(4)
#    eventType(3) with values: snmp-trap(3)

# Create 2 Event (eventStatus)
snmpset -m SNMPv2-MIB -c private -v 2c $HOST ${OID_EVENT_ENTRY}.7.1 i 2
snmpset -m SNMPv2-MIB -c private -v 2c $HOST ${OID_EVENT_ENTRY}.7.2 i 2
# Set event type trap (eventType)
snmpset -m SNMPv2-MIB -c private -v 2c $HOST ${OID_EVENT_ENTRY}.3.1 i 3
snmpset -m SNMPv2-MIB -c private -v 2c $HOST ${OID_EVENT_ENTRY}.3.2 i 3
# Set Event Valid (eventStatus)
snmpset -m SNMPv2-MIB -c private -v 2c $HOST ${OID_EVENT_ENTRY}.7.1 i 1
snmpset -m SNMPv2-MIB -c private -v 2c $HOST ${OID_EVENT_ENTRY}.7.2 i 1

# Create an alarm
# Fields in RMON alarm table:
#   [alarmIndex (1)]
#   alarmInterval(2)            value in seconds
#   alarmVariable(3)            value = selected OID, e.g. FAN speed
#   alarmSampleType(4)          value = deltaValue(2)
#   [alarmValue(5)]
#   alarmStartupAlarm(6)        value = risingOrFallingAlarm(3)
#   alarmRisingThreshold(7)     value = maximal speed
#   alarmFallingThreshold(8)    value = minimal speed
#   alarmRisingEventIndex(9)    value = event 1
#   alarmFallingEventIndex(10)  value = event 2
#   [alarmOwner(11)]
```

```
#   alarmStatus(12)              values see above as for eventStatus

# Create an alarm (alarmStatus)
snmpset -m SNMPv2-MIB -c private -v 2c $HOST ${OID_ALARM_ENTRY}.12.1 i 2

# Configure the alarm (field description above)
snmpset -m SNMPv2-MIB -c private -v 2c $HOST \
        ${OID_ALARM_ENTRY}.2.1  i 5    \
        ${OID_ALARM_ENTRY}.3.1  o ${OID_FAN_SPEED} \
        ${OID_ALARM_ENTRY}.4.1  i 2    \
        ${OID_ALARM_ENTRY}.6.1  i 3    \
        ${OID_ALARM_ENTRY}.7.1  i 4300 \
        ${OID_ALARM_ENTRY}.8.1  i 3900 \
        ${OID_ALARM_ENTRY}.9.1  i 1    \
        ${OID_ALARM_ENTRY}.10.1 i 2

# Set alarm status valid
snmpset -m SNMPv2-MIB -c private -v 2c $HOST ${OID_ALARM_ENTRY}.12.1 i 1
```

10.5.10 Reset User Data on the Unit Computer

Method 1: Reset the running configuration to defaults Monitoring

The running configuration can be reset to factory defaults by the “clear config” CLI command. A reboot of the UC is not required, but the Fastpath application ends in the login prompt. A user may also note that all access to the switch by IP protocols, e.g. telnet, ssh, Web, may be interrupted, if the corresponding interfaces are reset to default values – most probably not configured.

```
(Ethernet Fabric)#clear config
Warning: Exercising this function will cause all system configuration parameters to be
reset to their default values. It is possible that the ip address of the switch will
change. If this occurs you will need to determine the new ip address to access the device
using the IP based services.
Are you sure you want to clear the configuration? (y/n) y

Clearing configuration. Please wait for login prompt.
(Unit 1)>

User:
```

It is required to login to the CLI and save the “new” running configuration as new startup configuration. If not done, the switch will start with the old configuration after the next reboot.

Also this procedure does not delete any additional (user) data from the data partition, e.g. persistent log files, crash logs, hardware profiles, etc.

Method 2: Wipe the data partition

The data partition which includes all non-volatile configuration changes can be reset to factory defaults by a sequence initiated from the bootloader shell.

The script "clear_config" boots the Linux kernel with an initramfs which then wipes out and then recreates the data partition. After the following reboot the application image starts with empty data partition and the application falls back to defaults.

```
=> run clear_config
WARNING: adjusting available memory to 30000000
5972396 bytes read in 1009 ms (5.6 MiB/s)
```

```
WARNING: adjusting available memory to 30000000
1678696 bytes read in 309 ms (5.2 MiB/s)
WARNING: adjusting available memory to 30000000
## Loading kernel from FIT Image at 02000000 ...
   Using 'config-1' configuration
   Trying 'kernel-1' kernel subimage
     Description:  Linux Kernel
     Type:         Kernel Image
     Compression:  gzip compressed
     Data Start:   0x020000d8
     Data Size:    5944541 Bytes = 5.7 MiB
     Architecture: PowerPC
     OS:           Linux
     Load Address: 0x00000000
     Entry Point:  0x00000000
     Hash algo:    md5
     Hash value:   d11f2ae18f955f12b1eb3aef7de549ad
   Verifying Hash Integrity ... md5+ OK
## Loading init Ramdisk from Legacy Image at 10000000 ...
   Image Name:
   Image Type:   PowerPC Linux RAMDisk Image (uncompressed)
   Data Size:    1678632 Bytes = 1.6 MiB
   Load Address: 00000000
   Entry Point:  00000000
   Verifying Checksum ... OK
## Loading fdt from FIT Image at 02000000 ...
   Using 'config-1' configuration
   Trying 'fdt-1' fdt subimage
     Description:  Flattened device tree
     Type:         Flat Device Tree
     Compression:  uncompressed
     Data Start:   0x025ab6a0
     Data Size:    26069 Bytes = 25.5 KiB
     Architecture: PowerPC
     Hash algo:    md5
     Hash value:   69b55d69672fc0e8ed267b8cb92177c8
   Verifying Hash Integrity ... md5+ OK
   Booting using the fdt blob at 0x25ab6a0
   Uncompressing Kernel Image
   Using Device Tree in place at 025ab6a0, end 025c4c74
rtc-pcf85063 2-0051: hctosys: unable to read the hardware clock
Formatting config partition..
mke2fs 1.45.5 (07-Jan-2020)
/dev/mmcblk0p2 contains a ext4 file system
        last mounted on /etc on Thu Jan  1 00:00:01 1970
Discarding device blocks: done
Creating filesystem with 524268 1k blocks and 131072 inodes
Filesystem UUID: c30caef3-1690-4266-b943-b6a2f579cca9
Superblock backups stored on blocks:
        8193, 24577, 40961, 57345, 73729, 204801, 221185, 401409

Allocating group tables: done
```

```
Writing inode tables: done
Creating journal (8192 blocks): done
Writing superblocks and filesystem accounting information: done

reboot: Restarting system
```

10.5.11 Fan Control

The Fastpath application can control and monitor the fans only on specific chassis providing this function with specific RTM. Three modes are available:

- Automatic closed loop mode: fan speed settable, fan voltage readable.
- Automatic open loop mode: fan speed readable, fan voltage settable.
- Fixed speed mode: fixed fan speed settable

In automatic modes (open and closed loop) the fan control depends on five temperature ranges.

The four user settable Temperature Threshold parameters Tt1, Tt2, Tt3, Tt4 (integers) define the five possible temperature ranges Tr0, Tr1, Tr2, Tr3, Tr4. The minimum allowed difference between two consecutive Tt is 5°C. The temperature hysteresisTh has the fixed value of 3°C.

Table 79: Fan Control and Temperature Ranges

Temperature Range	Previous range below (increasing temperature)	Previous range above (decreasing temperature)
Tr0	Tai < Tt1	Tai + Th < Tt1
Tr1	Tt1 <= Tai < Tt2	Tt1 <= Tai + Th < Tt2
Tr2	Tt2 <= Tai < Tt3	Tt2 <= Tai + Th < Tt3
Tr3	Tt3 <= Tai < Tt4	Tt3 <= Tai + Th < Tt4
Tr4	Tt4 < Tai	Tt4 < Tai + Th

For the automatic modes, the Fastpath application implements a control task, which schedules every 30s. The task reads the current input temperature parameter (Tai) from the hardware and computes the corresponding temperature range. If the temperature range changes, depending on the actual mode, the fan speed parameter or the fan voltage parameter, are reprogrammed into the fan controller IC.

Dedicated CLI commands and SNMP OID are available to setup the feature and its parameters.

CLI Commands:

- **set board fan control mode**

This command selects the fan control mode. Three modes are available. In fixed mode the fan runs at fixed speed. In Open Loop mode and Closed Loop mode the fan speed is controlled by five user settable temperature ranges.

Format

```
set board fan control mode <fix|open|closed>
```

Default

```
open
```

set board fan speed

This command selects the fan speed in fixed mode.

Format

```
set board fan speed <speed>|max
```

Default

```
max
```

set board fan control threshold

This command sets the temperature thresholds for automatic FAN control. The 'no' variant of this command reverts to default values.

Five temperature ranges (Tr0 to Tr4) are defined which expect 4 threshold values (Tt1, Tt2, Tt3, Tt4) in ascending order. The threshold values are in degrees C. The minimum allowed difference between two consecutive thresholds is 5 degrees C. The hysteresis (Th) is fixed to 3 degrees C. The temperature ranges are defined in Table 79 above.

Format

```
set board fan control threshold <Tt1> <Tt2> <Tt3> <Tt4> no set board fan control threshold
```

Mode

```
Privileged Exec
```

Default

```
25 35 45 55
```

set board fan control speed

This command sets the speed related to the temperature thresholds in closed loop mode. The 'no' variant of this command returns to factory default values. The fan speed is in RPM.

Format

```
set board fan control speed <Fs0>|max <Fs1>|max <Fs2>|max <Fs3>|max <Fs4>|max no set board fan
control speed
```

Mode

```
Privileged Exec
```

Default

```
max max max max max
```

set board fan control voltage

This command sets the voltage related to the temperature thresholds in open loop mode. The 'no' version of this command returns to factory default values.

Format

```
set board fan control voltage <Fv0> <Fv1> <Fv2> <Fv3> <Fs4> no set board fan control voltage
```

Mode

```
Privileged Exec
```

Default

```
1200 1200 1200 1200 1200
```

set board fan monitor voltage

This command sets monitoring of the fan voltage DAC in closed loop mode. If no thresholds ('none') is defined the monitoring is disabled. The "no" version of this commands resets the values to 'none'.

Format

```
set board fan monitor voltage <range> <lower threshold>|none <upper threshold>|none no set board fan monitor voltage <range>
```

Mode

```
Privileged Exec
```

Default

```
Disabled by default
```

set board fan monitor speed

This command sets monitoring of the fan speed in closed and open loop mode. If no thresholds ('none') is defined the monitoring is disabled. The "no" version of this commands resets the values to 'none'.

Format

```
set board fan monitor speed <range> <lower threshold>|none <upper threshold>|none no set board fan monitor speed <range>
```

Mode

```
Privileged Exec
```

Default

```
Disabled by default
```

show board fan

This command shows the following fields:

Table 80: show board fan command

Control Mode	Configured fan control mode, either fix, open, closed
Temperature Threshold	Configured temperature threshold values in degrees C
Fan Speed	Configured fan speed for each temperature range (valid in closed loop mode)
Fan Voltage	Configured fan voltage for each temperature range (valid in open loop mode)
Monitoring Thresholds	Configured thresholds for monitoring fan speed and/or voltage for each temperature range
Current Range	Current temperature range Tr0 through Tr4
Current Temperature	Temperature reading in degrees C used for the control algorithm
Alarm Status	Status for monitoring thresholds for the current temperature range
Fixed Fan Speed	RPM value in fixed mode

The current fan speed/voltage reading for each fan is available by the show board sensors command.

Format

```
show board fan
```

Mode

```
All
```

clear board fan

This command resets all FAN configuration to default values.

Format

```
clear board fan
```

Mode

```
Privileged Exec
```

11/ Conduction-Cooled VX6940-RC

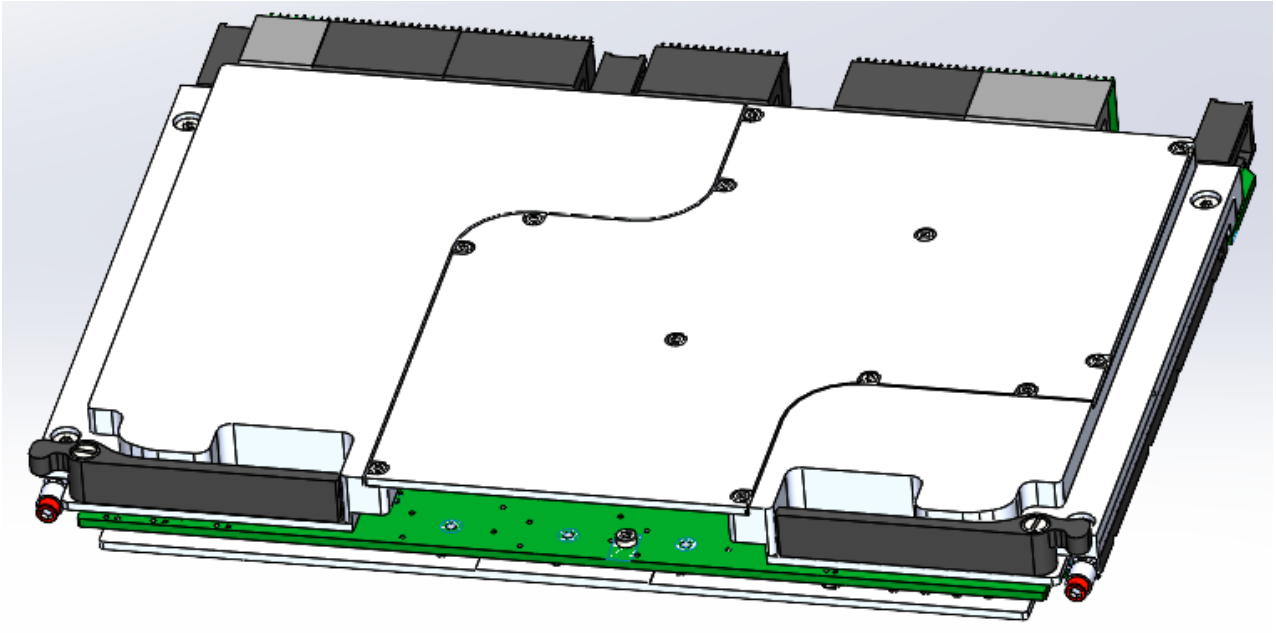
The VX6940 is also available in a conduction-cooled configuration referred to as VX6940-RC. This section covers its key features.

11.1. VX6940-RC Overview

The Kontron-designed thermal frame or "ruggedizer" combines thermal efficiency and mechanical robustness to offer:

- Two different ranges of operating temperature depending on user's application:
  - RC3: from -40°C to +70°C (qualified with a power dissipation of 52 W)
  - RC4: from -40°C to +85°C (qualified with a power dissipation of 52 W)
- VITA 47 / MIL-STD-810-G high levels of shocks and vibrations specification.
- Enhanced reliability and MTBF : Refer to Table 10 in section 2.9.

Figure 56: VX6940-RC Overview



11.2. VX6940-RC Order Codes

Table 81: VX6940-RC Order Codes

Order Code	Description
VX6940-RC-00A00	6U Open VPX 10/40/100 GbE Managed Ethernet Switch. Based on the Broadcom switch BCM56760, the NXP QorIQ T1042 and the Aspeed AST2520. eMMC, M.2 2242 Socket. Switched Ethernet Lanes: - 12 rear VPX Fat Pipe Data Planes (12 quad Ethernet SerDes). - 8 rear VPX Ultra Thin Pipe Control Planes (8 Ethernet SerDes). Rear data port: 1000BASE-T ETH1. Rear management ports: 100BASE-TX ETH0 & RS-232 COM link. Battery not equipped. Rugged Conduction-cooled RC3 (-40°C to +70°C). Conformal coating.

Other SKU and other temperature ranges, including RC4 (-40°C to +85°C), are available on demand. Please contact Kontron.

11.3. VX6940-RC Board Identification

Same identification scheme as VX6940-SA. Please refer to section 3.2.

11.4. VX6940-RC Specifications

Table 82: Mechanical Specifications

Mechanical Specifications	RC - Rugged Conduction-cooled
Plug-in unit type (VITA 48.2)	Type 2, secondary side retainers
Dimensions	6U form factor: 233.35 x 160.0 mm
Height	Single slot
Weight	RC3: 1550g +/-1.5%. RC4: 1485g +/-1.5%.

Table 83: Environmental Specifications

Environmental Specifications	RC - Rugged Conduction-cooled
Conformal coating	Standard
Cooling method	Conduction
Operating Temperature	RC3: -40°C to +70°C **(1)** RC4: -40°C to +85°C **(2)**
Storage Temperature	-50°C to +100°C

Environmental Specifications	RC - Rugged Conduction-cooled
Sine Wave Vibration (Operating)	5 to 22 Hz : Displacement 2.5 mm 22 Hz to 2000 Hz: 5 g Sweep rate : 1 octave / minute
Random Vibration (Operating)	5 Hz to 100 Hz: +3dB/octave 100 Hz to 1000 Hz: 0.1 g^2/Hz 1000 Hz to 2000 Hz: -6dB/octave
Shock (Operating)	40 g, 11 ms, half-sine
Altitude (Operating)	-1 500 ft to 60 000 ft
Relative Humidity	95% without condensation

(1) The RC3 temperature range of -40°C/+70°C has been qualified with a power dissipation of 52 W. Temperature should be measured on the left card edge as described in section "VX6940-RC Thermal ".

(2) The RC4 temperature range of -40°C/+85°C has been qualified with a power dissipation of 52 W. Temperature should be measured on the left card edge as described in section "VX6940-RC Thermal ".

11.5. VX6940-RC Peripheral Connectivity and Daughter Cards

On the front side, the VX6940-RC does not support the QSFP cages, the Ethernet ports ETH0 & ETH1 and the serial port COM. Only the LED indicators and the reset push-button are available.

The equipment of the rear connectors is unchanged.

The VX6940-RC includes all the daughter cards and mezzanines defined on the standard VX6940-SA.

11.6. VX6940-RC Board Installation and Removal

NOTICE

Running the VX6940-RC at high temperature without tightening the wedgelocks to the cold plate may result in permanent damage to the board.

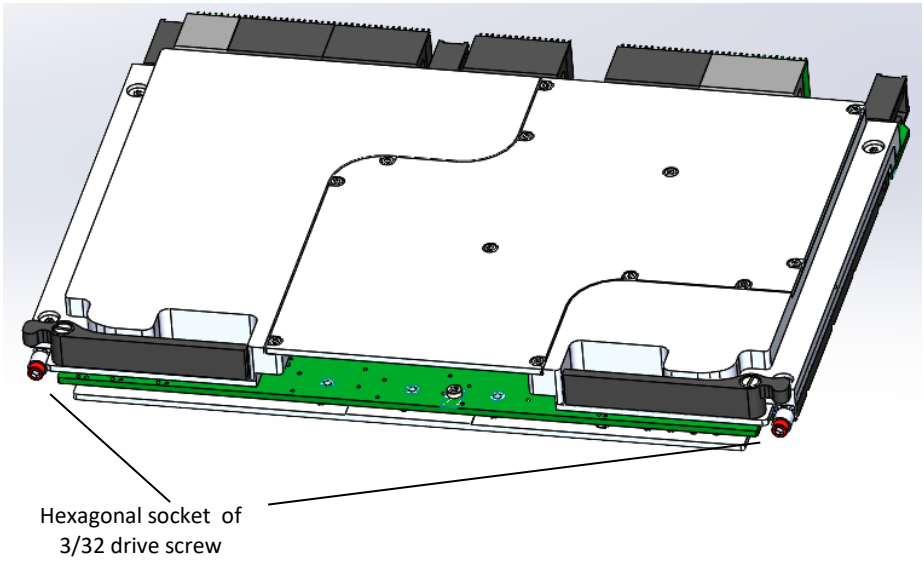
Board Insertion and Removal

The insertion and removal instructions are identical to those applying to the standard VX6940 except for the tightening of the wedgelocks described hereafter. Refer to sections "Initial Installation Procedures" and "Standard Removal Procedure".

Wedgelocks Tightening

After inserting the board into the chassis, tighten the wedgelock drive screws (Calmark serie 265) using a 3/32 Allen wrench with a torque value set to 0.9 N.m.

Figure 57: Wedgelocks Tightening



11.7. VX6940-RC VBAT Input for RTC

On VX6940-RC, the battery holder is not equipped. When the board is off, the onboard RTC may be supplied through rear P1 VBAT pin.

11.8. VX6940-RC Thermal Management

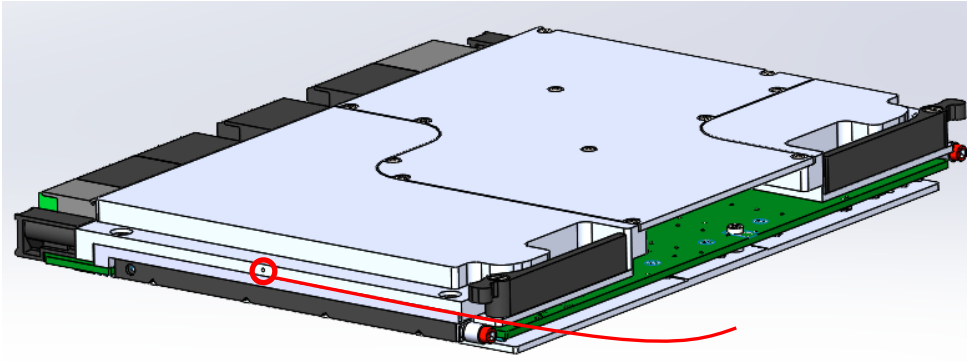
Secondary Side Attachment

To enhance thermal efficiency, the heatsink implements the secondary side attachment defined by VITA 48.2. This type of attachment increases the edge surface area available for thermal exchanges with the cold plate.

Temperature Monitoring - Thermocouple Location

The thermocouple used for monitoring the card edge temperature must be installed at a precise location for the temperature being measured to be consistent with the thermal design. As shown on Figure 58, the thermocouple must be positionned along the left side of the heatsink (when board is horizontal) and halfway between the rear connector and the front of the board.

Figure 58: Thermocouple Location for Board Temperature Monitoring



Thermal Management

The user must monitor temperatures to optimize thermal management:

- **Processor Load**: Kontron advises to keep some margin for real time behavior and stay within 80% of processor load.
- **Card Edge Temperature**: It is the card edge temperature which has been used for the thermal design and the definition of the specified temperature ranges (RC3 up to 70°C or RC4 up to 85°C). Therefore it should be measured as described above and monitored during system qualification to ensure that the board operates in its specified range.
- **Processor and Switch Temperatures**: The T1042 Unit Computer maximum junction temperature is 105°C and the one of the BCM56760 switch is 110°C. Both these temperatures must be carefuly monitored and a good margin (5 to 10°C at least) should be secured during system design.

Thermal Operating Points

Table 84 below provides some practical thermal operating points in conduction-cooled configurations.
Case 1 is an example of a RC3 configuration (-40°C/+70°C) with the Unit Computer running full load. Case 2 is in RC4 configuration (-40°C/+85°C), still with the Unit Computer running full load. In both cases, the Ethernet switch - which is not heavily loaded - shows a large margin in terms of junction temperature.

Table 84: VX6940-RC Thermal Operating Points in Conduction-Cooled Configuration

Case	Temp. Range Specification	Chamber Temp.	Card Edge Temp. (1)		BCM56760 Switch Tj	T1042 UC Tj	Board Temp.	Board Power	Test conditions
			Left	Right					
Case 1	RC3: -40/+70°C	64 °C	73 °C	-	84 °C	92 °C	75 °C	47 W	Command "stress" on UC. No heat pipe.
Case 2	RC4: -40/+85°C	74 °C	82 °C	-	92 °C	102 °C	83 °C	49 W	Command "stress" on UC. No heat pipe.
Case 3	RC4: -40/+85°C	80 °C	86 °C	85 °C	98 °C	102 °C	88 °C	47 W	Command "stress" on UC. Heat pipe.

(1) Test conditions according to Kontron procedure. In cases 1 & 2 only the highest edge temperature is mentionned (left side).

Appendix A: Detailed Ethernet Ports Mapping

Table 85: Detailed VX6940 Ethernet Ports Mapping (1 of 2)

Fastpath interface #	Port #	BCM56760			VX6940				Connector or Component	Default Port Map			
		TSC			RX Pair		TX Pair			Possible Modes		Default	
		Lane (1)	ID	Lane (1)	Lane (2)	Swap	Lane (2)	Swap		Port Modes (3)	Gbps rate	Port Mode	Gbps rate
1	53	29	TSCf0	0	0		0		VPX P1 DPfp01	KR4, KR	40G, 10G,1G	KR4	40G
2	54	30		1	1		1			detached, KR	-----,10G,1G	detached	-
3	55	31		2	2		2			detached, KR	-----,10G,1G	detached	-
4	56	32		3	3		3			detached, KR	-----,10G,1G	detached	-
5	33	21	TSCe5	0	3	x	3	x	VPX P1 DPfp02	KR4, KR	40G, 10G,1G	KR4	40G
6	34	22		1	2	x	2	x		detached, KR	-----,10G,1G	detached	-
7	35	23		2	1	x	1	x		detached, KR	-----,10G,1G	detached	-
8	36	24		3	0	x	0	x		detached, KR	-----,10G,1G	detached	-
9	29	17	TSCe4	0	0		0		VPX P1 DPfp03	KR4, KR	40G, 10G,1G	KR4	40G
10	30	18		1	1		1			detached, KR	-----,10G,1G	detached	-
11	31	19		2	2		2			detached, KR	-----,10G,1G	detached	-
12	32	20		3	3		3			detached, KR	-----,10G,1G	detached	-
13	25	13	TSCe3	0	0		0		VPX P1 DPfp04	KR4, KR	40G, 10G,1G	KR4	40G
14	26	14		1	1		1			detached, KR	-----,10G,1G	detached	-
15	27	15		2	2		2			detached, KR	-----,10G,1G	detached	-
16	28	16		3	3		3			detached, KR	-----,10G,1G	detached	-
17	37	25	TSCe6	0	0		0		VPX P2 DPfp05	KR4, KR	40G, 10G,1G	KR4	40G
18	38	26		1	1		1			detached, KR	-----,10G,1G	detached	-
19	39	27		2	2		2			detached, KR	-----,10G,1G	detached	-
20	40	28		3	3		3			detached, KR	-----,10G,1G	detached	-
21	21	9	TSCe2	0	0		0		VPX P1 DPfp06	KR4, KR	40G, 10G,1G	KR4	40G
22	22	10		1	1		1			detached, KR	-----,10G,1G	detached	-
23	23	11		2	2		2			detached, KR	-----,10G,1G	detached	-
24	24	12		3	3		3			detached, KR	-----,10G,1G	detached	-
25	45	57	TSCe12	0	0		0		VPX P2 DPfp07	KR4, KR	40G, 10G,1G	KR4	40G
26	46	58		1	1		1			detached, KR	-----,10G,1G	detached	-
27	47	59		2	2		2			detached, KR	-----,10G,1G	detached	-
28	48	60		3	3		3			detached, KR	-----,10G,1G	detached	-
29	49	61	TSCe13	0	3 rp	x	1	x	VPX P2 DPfp08	KR4, KR	40G, 10G,1G	KR4	40G
30	50	62		1	2 rp	x	0	x		detached, KR	-----,10G,1G	detached	-
31	51	63		2	1 rp	x	2 rp	x		detached, KR	-----,10G,1G	detached	-
32	52	64		3	0 rp	x	3 rp	x		detached, KR	-----,10G,1G	detached	-
33	17	5	TSCe1	0	0		0		VPX P3 DPfp09	KR4, KR	40G, 10G,1G	KR4	40G
34	18	6		1	1		1			detached, KR	-----,10G,1G	detached	-
35	19	7		2	2		2			detached, KR	-----,10G,1G	detached	-
36	20	8		3	3		3			detached, KR	-----,10G,1G	detached	-

(1) BCM56760 lane numbering: The four lanes within each TSC of the BCM56760 are numbered from 0 to 3. The lanes are also numbered from 1 to 72 within the BCM56760 : from 1 to 36 in half pipe 0 and from 37 to 72 in half pipe 1. This numbering defines logical lanes, 'independent of the routing and the connections made outside of the BCM56760.

(2) Lanes connection on VX6940: To facilitate VX6940 routing to the QSFP cages or VPX connectors, some lanes have been swapped. Swapping is done on a differential-pair basis (TX or RX). For proper BCM56760 configuration, it is important to clearly identify the original number of a lane (its logical number) and the actual lane number it is connected to (its physical number). For example, the receive differential pair 0 (RX0+/-) of a given TSC inside the BCM56760 may be routed to the receive differential pair 3 (RX3+/-) of a given QSFP. In this case RX3+/- is called the physical pair inside the physical lane 3 as opposed to the logical pair RX0+/- in logical lane 0.
In addition, the polarity of a differential pair may also be swapped, the "+" trace being connected to "-" pin and vice versa. This is noted as "rp" for "reversed polarity" in the table. Reversed polarity - when used - applies to physical lanes, not logical lanes.

(3) Port Setting: Each 40G KR4 Fat Pipe (4 lanes totaling 8 differential pairs) may be reconfigured as four 10G KR UltraThin Pipes (four times 1 lane = 2 pairs)

Table 86: Detailed VX6940 Ethernet Ports Mapping (2 of 2)

Fastpath interface #	Port #	BCM56760			VX6940				Connector or Component	Default Port Map			
			TSC		RX Pair		TX Pair			Possible Modes		Default	
		Lane (1)	ID	Lane (1)	Lane (2)	Swap	Lane (2)	Swap		Port Modes (3)	Gbps rate	Port Mode	Gbps rate
37	13	1	TSCe0	0	0		0		VPX P3 DPfp10	KR4, KR	40G, 10G,1G	KR4	40G
38	14	2		1	1		1			detached, KR	-----,10G,1G	detached	-
39	15	3		2	2		2			detached, KR	-----,10G,1G	detached	-
40	16	4		3	3		3			detached, KR	-----,10G,1G	detached	-
41	41	53	TSCe11	0	0		0		VPX P3 DPfp11	KR4, KR	40G, 10G,1G	KR4	40G
42	42	54		1	1		1			detached, KR	-----,10G,1G	detached	-
43	43	55		2	2		2			detached, KR	-----,10G,1G	detached	-
44	44	56		3	3		3			detached, KR	-----,10G,1G	detached	-
45	69	69	TSCf3	0	2	x	3 rp	x	VPX P3 DPfp12	KR4, KR	40G, 10G,1G	KR4	40G
46	70	70		1	3 rp	x	0 rp	x		detached, KR	-----,10G,1G	detached	-
47	71	71		2	0	x	1 rp	x		detached, KR	-----,10G,1G	detached	-
48	72	72		3	1	x	2	x		detached, KR	-----,10G,1G	detached	-
49	5	41	TSCe8	0	0		0		P5 CPutp01	KR, KX, BX	10G,1G	KR	10G
50	8	44		3	3		3		P5 CPutp02	KR, KX, BX	10G,1G	KR	10G
51	1	37	TSCe7	0	0		0		P5 CPutp05	KR, KX, BX	10G,1G	KR	10G
52	2	38		1	1		1		P5 CPutp06	KR, KX, BX	10G,1G	KR	10G
53	9	49	TSCe10	0	0		0		P5 CPutp05	KR, KX, BX	10G,1G	KR	10G
54	10	50		1	1		1		P5 CPutp06	KR, KX, BX	10G,1G	KR	10G
55	11	51		2	2		2		P5 CPutp07	KR, KX, BX	10G,1G	KR	10G
56	12	52		3	3		3		P6 CPutp08	KR, KX, BX	10G,1G	KR	10G
57	61	45	TSCe9	0	0		0		Front QSFP1	SR4, CR4, SR, CR	40G,10G,1G	SR4	40G
58	62	46		1	1		1			det, det, SR, CR	-----,10G,1G	detached	-
59	63	47		2	2		2			det, det, SR, CR	-----,10G,1G	detached	-
60	64	48		3	3		3			det, det, SR, CR	-----,10G,1G	detached	-
61	65	65	TSCf2	0	1 rp	x	2 rp	x	Front QSFP2	SR4, CR4, SR, CR	40G,10G,1G	SR4	40G
62	66	66		1	3 rp	x	0 rp	x		det, det, SR, CR	-----,10G,1G	detached	-
63	67	67		2	0 rp	x	1	x		det, det, SR, CR	-----,10G,1G	detached	-
64	68	68		3	2 rp	x	3			det, det, SR, CR	-----,10G,1G	detached	-
65	57	33	TSCf1	0	3	x	0 rp	x	Front QSFP3	SR4, CR4, SR, CR	40G,10G,1G	SR4	40G
66	58	34		1	0	x	3	x		det, det, SR, CR	-----,10G,1G	detached	-
67	59	35		2	1	x	2 rp	x		det, det, SR, CR	-----,10G,1G	detached	-
68	60	36		3	2	x	1	x		det, det, SR, CR	-----,10G,1G	detached	-
69	7	43	TSCe8	2	2		2		BCM5482 (5)	1000BASE-T	1G	1000BASE-T	1G
70	6	42	TSCe8	1	1		1		BCM5482 (4)	1000BASE-X	1G	1000BASE-X	1G
71	3	39	TSCe7	2	2		2		T1042 eth1	1000BASE-X	1G	1000BASE-X	1G
72	4	40	TSCe7	3	3		3		T1042 eth2	1000BASE-X	1G	1000BASE-X	1G

(1) BCM56760 lane numbering: The four lanes within each TSC of the BCM56760 are numbered from 0 to 3. The lanes are also numbered from 1 to 72 within the BCM56760 : from 1 to 36 in half pipe 0 and from 37 to 72 in half pipe 1. This numbering defines logical lanes, 'independent of the routing and the connections made outside of the BCM56760.

(2) Lanes connection on VX6940: To facilitate VX6940 routing to the QSFP cages or VPX connectors, some lanes have been swapped. Swapping is done on a differential-pair basis (TX or RX). For proper BCM56760 configuration, it is important to clearly identify the original number of a lane (its logical number) and the actual lane number it is connected to (its physical number). For example, the receive differential pair 0 (RX0+/-) of a given TSC inside the BCM56760 may be routed to the receive differential pair 3 (RX3+/-) of a given QSFP. In this case RX3+/- is called the physical pair inside the physical lane 3 as opposed to the logical pair RX0+/- in logical lane 0.
In addition, the polarity of a differential pair may also be swapped, the "+" trace being connected to "-" pin and vice versa. This is noted as "rp" for "reversed polarity" in the table. Reversed polarity - when used - apply to physical lanes, not logical lanes.

(3) Port Setting: Each 40G KR4 Fat Pipe (4 lanes totaling 8 differential pairs) may be reconfigured as four 10G KR Ultra Thin Pipes (four times 1 lane = 2 pairs)

(4) The BCM5482S PHY converts the 1000BASE-X link TSCE_8.1 from the BCM56760 into 1000BASE-T ETH1 or into RGMII2 of ShMC. Refer to block diagram.

(5) The BCM5482S PHY converts the 1000BASE-X link TSCE_8.2 from the BCM56760 into 1000BASE-T Management Port ETH0. Refer to block diagram.

About Kontron – An S&T Company

Kontron is a global leader in IoT/Embedded computing technology (ECT). As a part of technology group S&T, Kontron offers a combined portfolio of secure hardware, middleware and services for Internet of Things (IoT) and Industry 4.0 applications. With its standard products and tailor-made solutions based on highly reliable state-of-the-art embedded technologies, Kontron provides secure and innovative applications for a variety of industries. As a result, customers benefit from accelerated time-to-market, reduced total cost of ownership, product longevity and the best fully integrated applications overall.

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