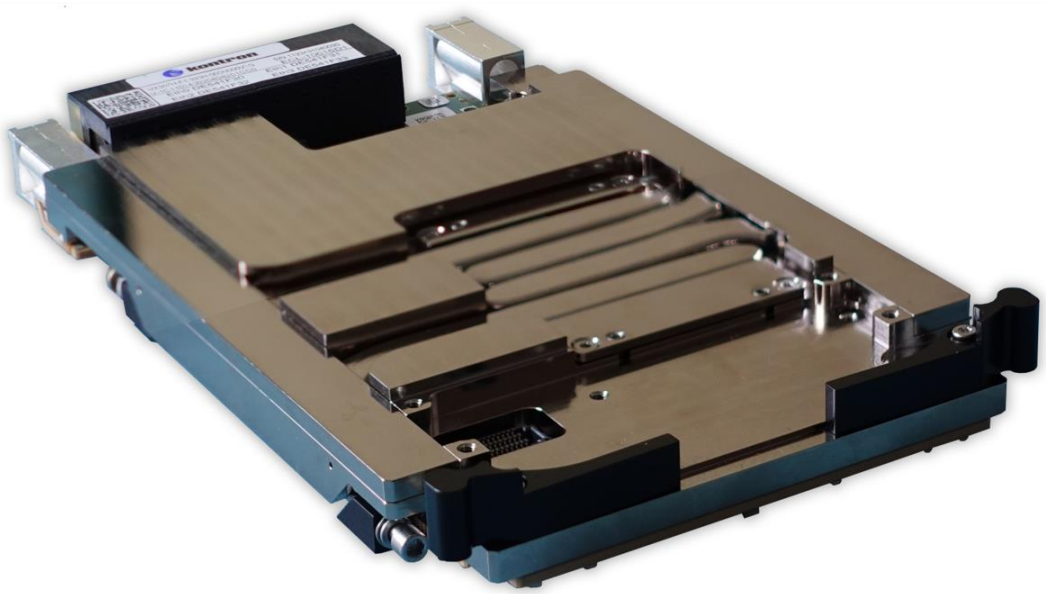
VX307H - User Guide

3U VPX Computing Node



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⚠CAUTION	Handling and operation of the product is permitted only for trained personnel within a work place that is access controlled. Please follow the “General Safety Instructions” supplied with the system.
NOTICE	You find the most recent version of the “General Safety Instructions“ online in the download area of this product.
NOTICE	This product is not suited for storage or operation in corrosive environments, in particular under exposure to sulfur and chlorine and their compounds. For information on how to harden electronics and mechanics against these stress conditions, contact Kontron Support.

Revision History

Revision	Brief Description of Changes	Date of Issue
0.1	Preliminary - Initial Issue	2022-Sept-6
0.2	Preliminary - version updated	2023-May-09
0.3	Preliminary - version updated	2023-May-16
0.4	Section 1.3.2: figure 3 updated Section 1.5: weight/mass table updated Section 1.6: MTBF updated Section 1.7 : document list updated Section 4.4 updated with Power States and error codes	2023-Aug-29
0.5	Refer to the change bars in the left margin	2024-Mar-13
0.6	Refer to the change bars in the left margin	2024-August-02
0.7	Figure 4, 7, 18, 19, 22, 30, 34 updated with the latest information Table 4, 44, 45, 47 updated with the latest information Refer also to the change bars in the left margin related to other corrections	2025-Mar-19
1.0	Reference to VX307H-SA16G-EVAL and VX307H-SA16H-EVAL variants removed References to the Rugged Air-Cooled variant added Table 1, 2, 3, 4, 9, 13, 14, 15, 16, 17, 18, 19, 38, and 51 updated Figure 4, 5, 7, 8, 13, 15, 21, 29, 35, and 36 updated or added Other minor updates marked by change bars in the left margin	2025-July-08

Terms and Conditions

Kontron warrants products in accordance with defined regional warranty periods. For more information about warranty compliance and conformity, and the warranty period in your region, visit https://www.kontron.com/terms-and-conditions.

Kontron sells products worldwide and declares regional General Terms & Conditions of Sale, and Purchase Order Terms & Conditions. Visit https://www.kontron.com/terms-and-conditions.

For contact information, refer to the corporate offices contact information on the last page of this user guide or visit our website CONTACT US.

Customer Support

Please contact our support team at support.KFR@kontron.com .

Customer Service

As a trusted technology innovator and global solutions provider, Kontron extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly experienced support enables Kontron to provide exceptional peace of mind to build and maintain successful products.

For more details on Kontron's service offerings such as: enhanced repair services, extended warranty, Kontron training academy, and more visit https://www.kontron.com/support-and-services.

Customer Comments

If you have any difficulties using this user guide, discover an error, or just want to provide some feedback, contact Kontron support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user guide on our website.

Symbols

The following symbols may be used in this user guide

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
NOTICE	NOTICE indicates a property damage message.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
	**Electric Shock!** This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	**ESD Sensitive Device!** This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	**HOT Surface!** Do NOT touch! Allow to cool before servicing.
	**Laser!** This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol indicates important information which must be read carefully.
	This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning
All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!
Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.
Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

⚠CAUTION

Danger of explosion if the battery is replaced incorrectly.
Replace only with same or equivalent battery type recommended by the manufacturer.
Dispose of used batteries according to the manufacturer's instructions.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Quality and Environmental Management

Kontron aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding Kontron's quality and environmental responsibilities, visit https://www.kontron.com/about-kontron/corporate-responsibility/quality-management.

Disposal and Recycling

Kontron's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Environmental protection is a high priority with Kontron.
Kontron follows the WEEE directive
You are encouraged to return our products for proper disposal.

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1. Introduction

The Kontron VX307H is a 3U VPX computing blade for data and signal processing application focusing on application domains such as Military & Aerospace, Transportation and Energy/Industry.
The Kontron VPX blade VX307H is the ideal building block for intensive parallel computing workloads where a cluster of Kontron VX307H can be used in switched OpenVPX environments.

VX307H variants are fully compatible with system architectures developed in alignment with the SOSA™ technical standard.

In this document:
VX307H is the product/board without any option or variant considerations.
VX307H stands for variant compatible with the SOSA Compute Intensive profile.
RA variant stands for the Rugged Air-cooled variants
AFT stands for the Rugged Air Flow Through variants
RC3 or RC4 variant stands for the Ruggedized Conduction cooled variants

Figure 1: Air-cooled variant overview

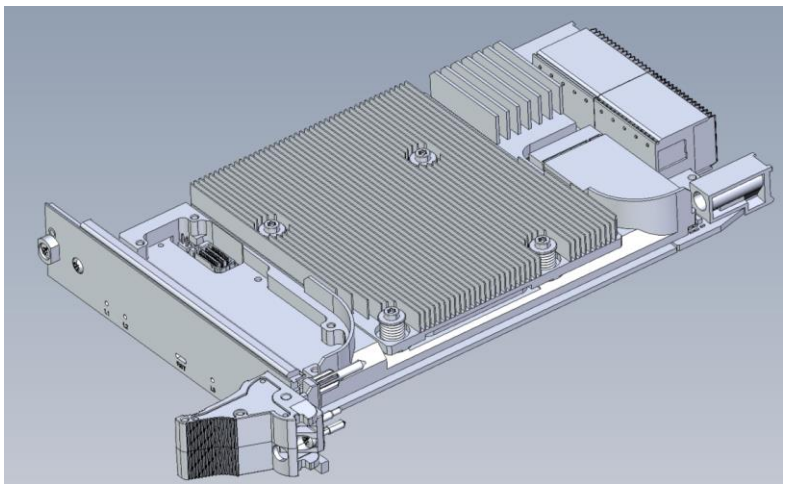
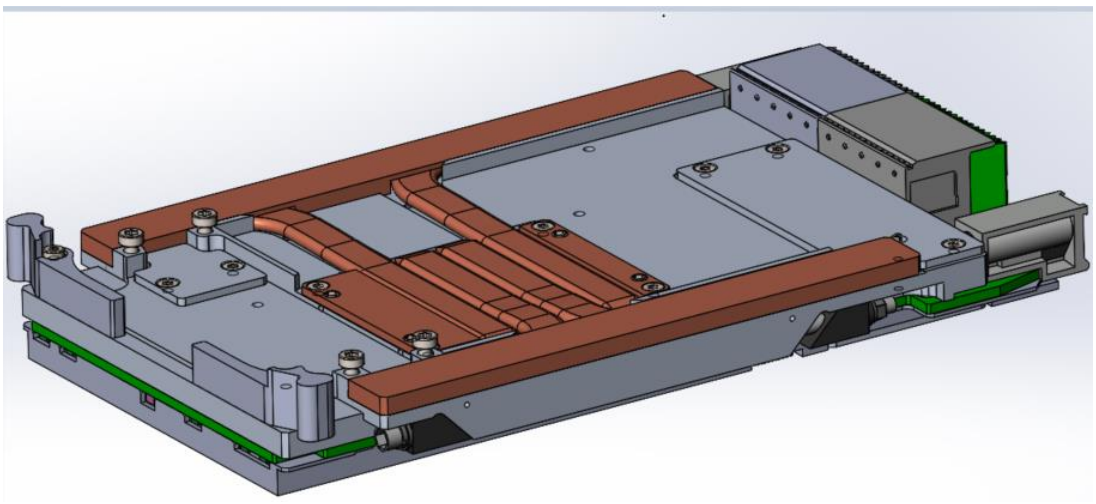


Figure 2: Conduction cooled variant overview



1.1. Manual Overview

1.1.1. Objective

This guide provides general information, instructions, operating instructions and functional description of the VX307H board. The onboard programming, onboard firmware and other software (e.g. drivers and BSPs) are described in detail in separate guides (see section "Related Publications").

This hardware technical documentation reflects the most recent version of the product. The “Release Notes" (see section "Related Publications") might help to keep track of potential evolutions

1.1.2. Audience

The scope of this guide is intended to cover, as far as possible, the range of people who will be handling or using the VX307H, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, system, cabling, grounding and communications.

1.1.3. Scope

This guide describes the VX307H product, without any optional mezzanines equipped.
The VX307H variants described in this guide are fully compatible with system architectures developed in alignment with the SOSA™ technical standard.

1.1.4. Terminology, Definitions and Abbreviations

In this document:
In this document, VX307H refers to the product/board without any options or variants considerations
SA/WA/RA/AFT are air-cooled variants whereas RC variant is conduction-cooled

- VX307H board
  This User Guide describes the VX307H board.
  The VX307H is fully compatible with system architectures developed in alignment with the SOSA™ technical standard.

- Environment class terminology:
  VX307H RC will be associated to the rugged conduction-cooled version of the board.

- Terms and acronyms:

Table 1: Terms and acronyms

Term or Acronym	Definition
BIOS	BIOS (Basic Input/Output System) firmware
BSP	A BSP (Board Support Package) from Kontron is a collection of software and configuration files that support the operation of a specific hardware platform
Compute Intensive	VPX compute intensive refers to VPX systems designed to handle high-performance computing tasks that require significant processing power and data throughput
Core	A processing unit including instruction cache, data cache, and often L2 cache.
COTS	Commercial Off The Shelf.
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
ECC	ECC (Error-Correcting Code) memory is a type of computer data storage that can detect and correct the most common kinds of internal data corruption
E.C.Level or ECL	Engineering Change Level refers to the exact technical definitions and revisions of a produc
EEPROM	Electrically Erasable Programmable Read-Only Memory
EU Directive	EU directives are legislative acts that set out goals that all EU countries must achieve
F-RAM	Ferroelectric Random Access Memory
I2C or I^2C	I2C (Inter-Integrated Circuit), also known as I^2C or IIC, is a synchronous, multi-master/multi-slave, single-ended, serial communication bus
IPMC	Intelligent Platform Management Controller
IPMI	Intelligent Platform Management Interface
DDR4	DDR4 (Double Data Rate 4) is the fourth generation of DDR SDRAM (Synchronous Dynamic Random-Access Memory) technology
Gdiscrete1	GDiscrete1 is a signal used in embedded computing systems, particularly in VPX (VITA 46) and SOSA (Sensor Open Systems Architecture) standards
GPIO	General-Purpose Input/Output
KCS	KCS (Keyboard Controller Style) interface is a communication interface between the host CPU and the IPMI (Intelligent Platform Management Interface) controller
LED	Light-Emitting Diode
LPC	Low Pin Count bus interface

Term or Acronym	Definition
LVCMOS	Low Voltage Complementary Metal-Oxide-Semiconductor
M.2	M.2, formerly known as the Next Generation Form Factor (NGFF), is a specification for internally mounted computer expansion cards and associated connectors. M.2 replaces the Mini SATA (mSATA) and Mini PCIe (mPCIe) standards
MTBF	Mean Time Between Failure
NVME	NVMe (Non-Volatile Memory Express) is a protocol used for accessing high-speed storage media that utilizes the PCI Express (PCIe) interface
NVMRO	NVMRO (Non-Volatile Memory Read Only) is a signal used in embedded computing systems to control the write protection of non-volatile memory
OD	Open Drain Output
Option	A feature which requires a specific order code.
PBIT	Power-on Built-In Test is a diagnostic test performed during the power-on sequence of a system to verify the functionality and integrity of its hardware components.
PCB	Printed Circuit Board.
PCH	Platform Controller Hub. The PCH architecture replaced the older northbridge and southbridge chipset design. The PCH is integrated in the D-2700/D-2800 SoC.
PCIe	Synonym of PCI Express.
PECI	PECI (Platform Environment Control Interface) is a communication protocol developed by Intel for monitoring and controlling the temperature and power consumption of Intel processors
Processor	According to Intel® terminology, the processor - synonymous with SoC Refers to the Intel® Core™ XEON-D-27xx or D-28xx processor.
PROCHOT	PROCHOT (Processor Hot) is a signal used by Intel processors to indicate that the CPU has reached a critical temperature threshold
Provision	A feature not yet available.
PTU (Intel®)	Intel® Performance Test Utility.
RTC	Real-Time Clock
RS-232 or EIA-232	RS-232, also known as EIA-232, is a standard for serial communication transmission of data
RS-422 or EIA-422	RS-422, also known as EIA-422, is a standard for serial communication transmission of data
RS-485 or EIA-485	RS-485, also known as EIA-485, is a standard for serial communication transmission of data
SATA	SATA (Serial AT Attachment) is a computer bus interface that connects host bus adapters to mass storage devices
SBC	Single Board Computer (the term defaults to VM606x).
SoC (Intel®)	System on chip. According to Intel® terminology, the SoC - synonymous with processor
SDRAM	Synchronous Dynamic Random-Access Memory
SKU	Stock Keeping Unit: A catalog's product and service identification code.
SOSA	Sensor Open Systems Architecture
SMBus or SMB	System Management Bus.
SSD	Solid State Drive
SWaP, SWaP-C	Seize, Weight and Power - Cost: an acronym to summarize the capabilities of an embedded system in Military or Aerospace.
TBD	To Be Defined. Information not available at the time this document was released
TDP	Thermal Design Power: the target power level of the processor. It represents the maximum sustained power expected from realistic applications. It is an input to the thermal design of the board.

Term or Acronym	Definition
TPM	Trusted Platform Module: An international standard for a secure crypto processor based on a dedicated hardware device and integrating cryptographic keys. Promoted by consortium TCG (Trusted Computing Group).
Turbo Boost Technology (Intel®)	A feature that opportunistically enables the processor to run a faster frequency. This results in increased performance of both single and multi-threaded applications.
uEFI or UEFI	UEFI (Unified Extensible Firmware Interface) is a specification for the firmware architecture of a computing platform
Uncore	In Intel® architecture, a unit of the SoC which includes the Ring, the Caching Agent Cbo, the Last Level Cache (LLC), the Home Agent (HA), the Integrated Memory Controller (IMC), the Integrated IO Module (IIO), the Power Control Unit (PCU).
USB	Universal Serial Bus
USER Domain	The USER domain is a specific area within the non-volatile memory that stores user-specific data
VPD	Vital Product Data
VPD Domain	The VPD domain is a specific area within the non-volatile memory that stores VPD data
VR	Voltage Regulator
XMC	XMC (Switched Mezzanine Card) is a standard for mezzanine cards used in embedded computing systems
XMCIO or XMCIOs	XMC mezzanine rear I/Os
1 GbE	Abbreviation for 1-Gbit Ethernet interface (1000BASE-T).
2LM	Top/bottom covers for the 2 Maintenance level as defined per VITA 48 REDI standards

1.2. VPX Overview

VPX (VITA 46) specifications establish a new direction for the next revolution in bus boards. VPX is an ANSI standard which breaks out from the traditional connector scheme of VMEbus to merge the latest in connector and packaging technology with the latest in bus and serial fabric technology. VPX combines best-in-class technologies to assure a very long technology cycle similar to that of the original VMEbus solutions. Traditional parallel VMEbus will continue to be supported by VPX through bridging schemes that assure a solid migration pathway.
For further information regarding this standards and its use, visit the home page of the VITA - Open Standards, Open Markets (http://www.vita.com)

1.3. Board Overview

1.3.1. Manual Overview

› Intel® Core™ XEON D-2700 and D-2800 processors

The VX307H computing node is a VPX computing blade for parallel data and signal processing applications. The VX307H is the ideal building block for intensive parallel computing workloads where a cluster of VX307H is used in full mesh or switched OpenVPX environments. Target applications include radar, sonar, imaging systems, airborne fighters, and unmanned aerial vehicle (UAV) radar, as well as rugged multi-display consoles. It is also well suited for transport applications.

The processing node of the VX307H implements Intel® Xeon® D-2700/D-2800 SoC integrating high count performance Cores and a highly flexible Ethernet controller, coupled with dual channel DDR4 memory. The highly integrated Xeon® D-2700/D-2800 SoC offers numerous PCIe channels, USB and SATA channels.

Table 2: Features overview

Features overview	
Processor	Intel® Xeon® D-2700 or D-2800 processor
Platform Controller Hub	Integrated Intel® 500 Series Chipset Family On-Package Platform Controller Hub.
Network Accelerator Complex	Integrates a Ethernet Multi-rate PHY that provides up to eight high-speed Ethernet interfaces
Onboard Controllers	
Gigabit Ethernet controllers	I225 or i226 and i210 controllers equipped depending on the product options Note: when equipped, the I210 does not support IEEE802.3 clause 73 backplane auto-negotiation
Watchdog	CPLD-based, timeout ranging from 4 ms to 510s, IRQ, Reset, dual-stages
Real Time Clock (RTC)	Separate low power RTC RV8803
System CPLD	Power - on/ off control, Reset control, Local environmental control/monitoring, I2C, LEDs control, Serial lines multiplexer, Serial VPD and user memories, User and system GPIOs, Internal registers that allow system management Watchdog : CPLD-based, timeout ranging from 4 ms to 510s, IRQ, Reset, dual-stages
IPMC	FRU subsystem management: Local environmental control/monitoring, IPMB A/B interfaces, FRU memory, system event log.
Memory	
System Memory	Up to 64 GB dual channel DDR4 SDRAM, with ECC, soldered
Flash (uEFI BIOS)	Two 32MB boot FLASH, with recovery image and uEFI BIOS settings
EEPROM	Refer to section 3.2 and 3.3 for detailed information.
F-RAM	One serial 1M-Bit dedicated to system data
Front Interfaces	
LEDs	Five LEDs reporting the board CPU health status and activity
Reset	Reset push button
Optional front panel	Refer to section 4.1
Onboard Interfaces	
Top M.2 option (M2S1) Bottom M.2 option (M2S2)	Top/bottom M.2 module option (named M2S1 and M2S2 slots): Type M, 22 mm x 42 mm form factor Default Slot interface: x2 PCIe
VPX Interface	
VPX Slot Profiles	VX307H is ompatible with the following as per Vita 65: SLT3-PAY-1F1U1S1S1U1U4F1J-14.6.13-n and SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-0 Refer to the available product options for MOD3p-PAY-1F1U1S1S1U1U2F1H-16.6.11-11 or MOD3p-PAY-1F1U1S1S1U1U4F1J-16.6.13-1 comaptibilities.
Rear I/O via P1&P2	Refer to the pin assignment tables in this document.
Supervisory Functions	Non Maskable RESET NVMRO, Master SMBus and Master/Slave SMBus interfaces for system management. Compatible with Kontron CMB (Monitoring Board), temperature and voltage sensors on the board
Power Supplies	On P0: VS1=12V; VS2&VS3 not used; +12V_AUX is optional in VITA 46 and not connected -12V_AUX is optional in VITA 46. It is not used internally on VX307H 3.3V_AUX is mandatory in VITA 46. However, if absent, it will be generated internally.
OS Support	Linux, ask for: Windows, VxWorks
Mechanical size	Rugged Air-Cooled (RA class):3U 160 mm, Slot pitch: 1.00 inch Air Fow Through (AFT class): 3U 160 mm, Slot pitch: 1.50 inches Conduction cooled (RC class): 3U 160 mm, Slot pitch: 1.00 inch according to VITA 48.2

All the Flash and non-volatile memories onboard have a write protect mechanism taking into account the NVMRO (Non Volatile Memory read Only) VPX signal. For further details, see “NVMRO” section

- Software

  Kontron is one of the few compact PCI, VME and VPX vendors to offer in-house support for most of the industry-proven real-time operating systems available today.
  its close relationship with software editors, allows Kontron to locally produce and support BIOS, BSPs and drivers for the latest operating system revisions thereby taking advantage of technology changes that follow silicon evolution.
  Kontron also offers hotline software support and regular software updates to customers with a maintenance contract.
  A dedicated website is available for online updates and release downloads.
  The VX307H is shipped with the AMI's BIOS which supports Secure Boot and TPM. This BIOS supports the PBIT Expert Mode option from Kontron CMON-Line (https://kfrlabs.kontron.com/monitoring.php)
  The VX307H also supports a live Linux distribution (a Fedora Core remix distribution) for instant evaluation and benchmarking. Based on Fedora Linux, it offers many turn-key features, such as Continuous BIT service (CBIT). Refer to our Kontron VME/VPX Fedora Remix Release Notes for details.
  By loading this software image onto a USB stick, you can instantly access to all the board's features. The CBIT dashboard is available at http://board-ip-address:8000/kehm-RESULTS.xml .

Contact Kontron for further information regarding other operating systems and software support

- Tooling - I/O module

  The VX307H is compatible with the I/O module option "FB-VX3-0010".
  Refer to the "Front Board Tooling Option" for more information.

- Tooling Rear Transition Module

  The VX307H is compatible with the « PB-VX3-40G-H-601 rear transition module.
  Refer to the "RTM Characteristics" section for more information.

1.3.2. Block Diagram

Figure 3: VX307H- High-Level Block Diagram

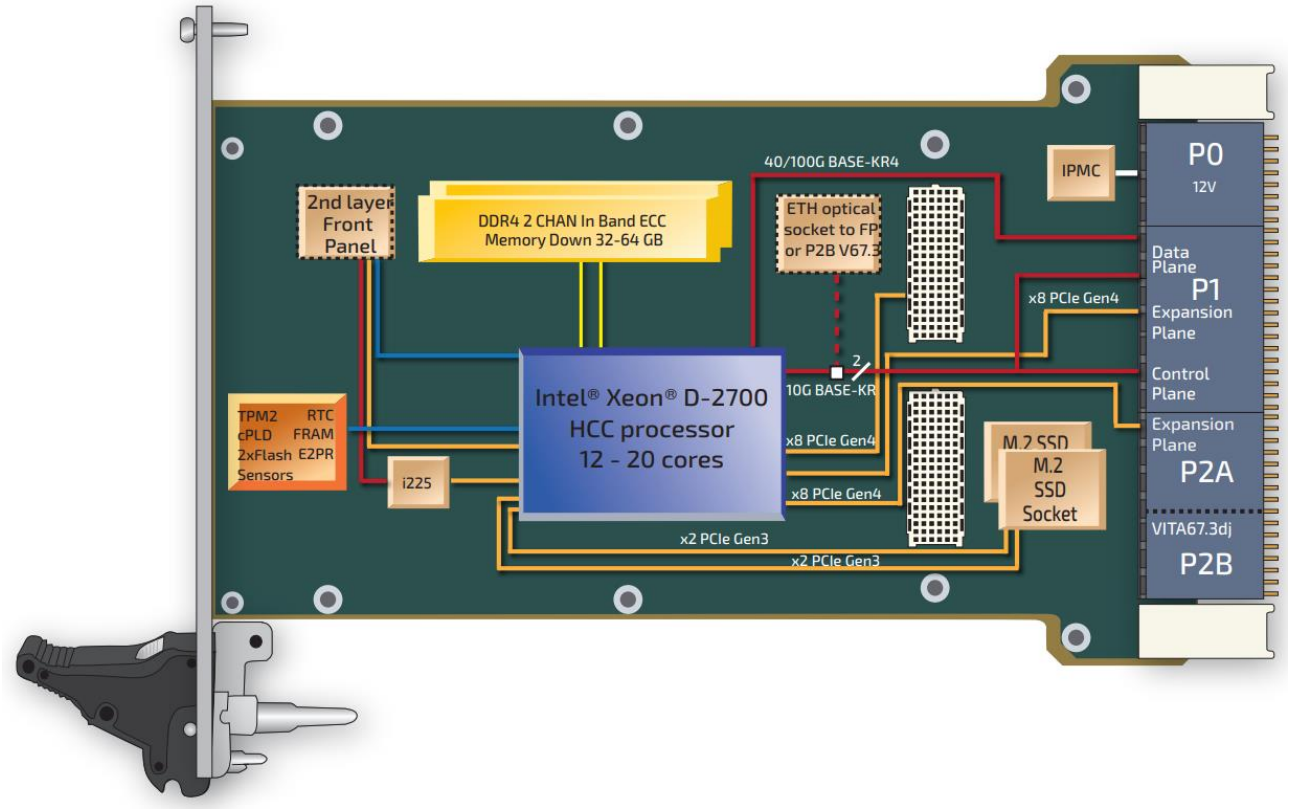
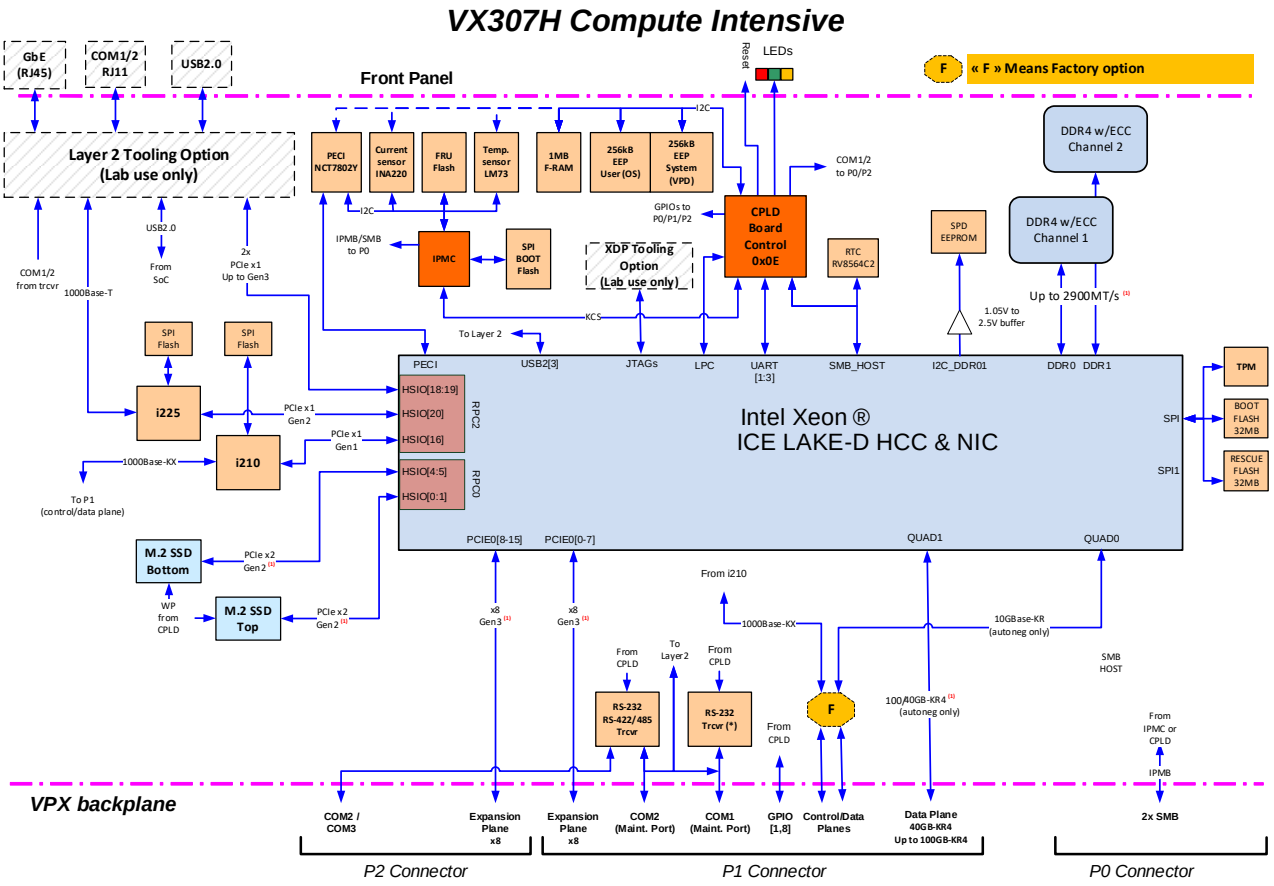


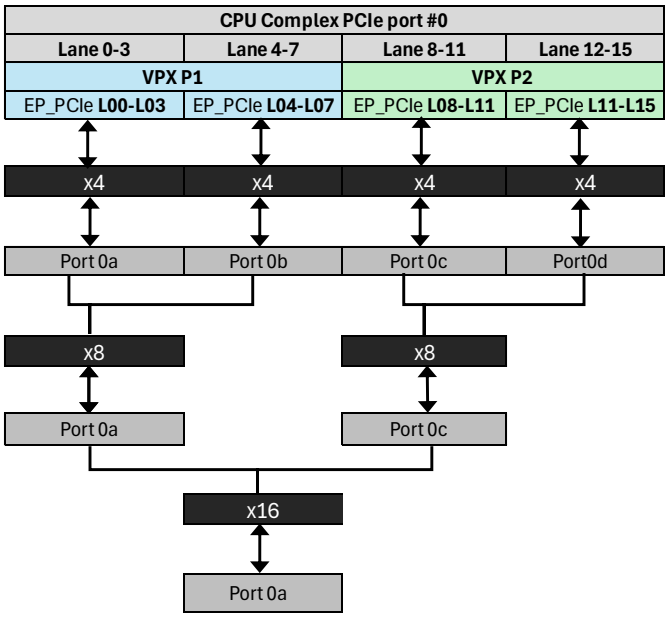
Figure 4: VX307H- Detailed block diagram of the Compute Intensive Variant



Note (1): Ask Kontron for the available COTS product configurations

CPU complex PCIe signal partitioning capability of the PCIE#0 port of the HCC Ice Lake D processor:

x16 CPU PCIe port#0 is routed to the x16 Expansion plane on VPX P1 and P2 connectors (see section 4.3.2 and 4.3.3)
CPU PCIe port#0 can be bifurcated as two x8 ports, four x4 ports, or any combination thereof.



CPU complex PCIe Port #0A is defined as Port #1A in BIOS
Default COTS width configuration on the VPX expansion plane is x16.
Refer to the BIOS manual (D283956) for more information about possible PCIe configurations.

1.3.3. Ordering information

Table 3: Available RC class Order Codes (Conduction Cooled)

Environmental Class	Ordering Code	Commercial Code	Description
RC3 (1)	Generic	**VX307H-RC3xxy**-00rN000V1z (1) (3)	Conduction-Cooled '**RC3**' class (-40°C to 70°C) (1) Processor option (xx): xx=16: Intel(r) Xeon D-2775TE Processor, 100W TDP @Base Freq. 2GHz, 16 cores xx=20: Intel(r) Xeon D-2796TE Processor, 118W TDP @Base Freq. 2GHz, 20 cores xx=21: Intel(r) Xeon D-2896TER Processor, 110W TDP @Base Freq. 2GHz, 20 cores
	1070-5147	VX307H-RC316G-000N000V1P	Memory DDR4 option (y): y= G: 32 GB soldered SDRAM with ECC y= H: 64 GB soldered SDRAM with ECC
	1073-4433	VX307H-RC316G-000N000V1Q	
	1074-8592	VX307H-RC316G-001N000V1P	
	1074-8593	VX307H-RC316G-001N000V1Q	
	1073-4667	VX307H-RC316G-002N000V1P	Rear I/O Profile option (r): r=0: Rear module profile is aligned with MOD3p-PAY-1F1U1S1S1U1U4F1J-16.6.13-1 with 100/40GBase-KR4 (Auto-negotiation mode only), 10GBase-KR Data Plane (Auto-negotiation mode only), 1000Base-KX Control Plane (does not support IEEE802.3 clause 73 backplane auto-negotiation), x16 PCIe Gen3 Expansion Plane
	1073-4668	VX307H-RC316G-002N000V1Q	
	1070-5302	VX307H-RC316H-000N000V1P	
	1074-0901	VX307H-RC320G-000N000V1P	r=1: Rear module profile is aligned with MOD3p-PAY-1F1U1S1S1U1U4F1J-16.6.13-1 with 100/40GBase-KR4 (Auto-negotiation mode only), 1000Base-KX Data Plane (does not support IEEE802.3 clause 73 backplane auto-negotiation), 10GBase-KR Control Plane (Auto-negotiation mode only), x16 PCIe Gen3 Expansion Plane
	1074-0902	VX307H-RC320G-000N000V1Q	
	1070-5304	VX307H-RC320H-000N000V1P	r=2: Rear module profile is aligned with MOD3p-PAY-1F1U1S1S1U1U2F1H-16.6.11-11 with 100/40GBase-KR4 (Auto-negotiation mode only), 10GBase-KR Data Plane (Auto-negotiation mode only), 10000Base-KX Control Plane (does not support IEEE802.3 clause 73 backplane auto-negotiation), x8 PCIe Gen3 Expansion Plane, No P2 connector.
	1073-1002	VX307H-RC320H-000N000V1Q	
	1073-4664	VX307H-RC320H-002N000V1P	r=3: Rear module profile is aligned with MOD3p-PAY-1F1U1S1S1U1U2F1H-16.6.11-11 with 100/40GBase-KR4 (Auto-negotiation mode only), 1000Base-KX Data Plane (does not support IEEE802.3 clause 73 backplane auto-negotiation), 10GBase-KR Control Plane (Auto-negotiation mode only), x8 PCIe Gen3 Expansion Plane, No P2 connector.
	1073-4665	VX307H-RC320H-002N000V1Q	
	1074-1353	VX307H-RC321G-000N000V1P	Software option (z): z=0: No PBIT z=P: Power on Built in Test Run Time z=Q: PBIT RT & NVMe SSD on the Top or Bottom M.2 slot with preloaded Linux
	1074-1354	VX307H-RC321G-000N000V1Q	
	1073-4970	VX307H-RC321H-000N000V1P	
	1073-4971	VX307H-RC321H-000N000V1Q	
	1073-4973	VX307H-RC321H-002N000V1P	**Other product options** No VITA 48 2LM covers Top/Bottom 2242 M.2 slot : up to D5 and M Key with x2 PCIe RTC Power sourced from system VPX VBAT, VITA 46.11 Support, TPM 2.0 Secure element Conformal Coating (2)
	1073-4974	VX307H-RC321H-002N000V1Q	
	1075-2125	VX307H-RC321G-002N000V1Q	

Note (1): Default BIOS configuration on COTS sets the maximum processor temperature range during operation to ±145°C, starting from boot time temperature, with CPU PCIe Gen3 and PCH PCIe/SATA Gen2 speed limitations. See also Section “Environmental Specifications”.

Note (2): Conformal coating is present on qualified products. Early prototypes or unqualified products may be delivered without conformal coating.

Note (3): product limitations may apply. Refer to the product Release Note for more information.

Table 4: Available EFT Order Codes – Rugged Air cooled

Environmental Class	Ordering Code	Commercial Code	Description
EFT/EVAL (Lab-grade)	1074-2683 1074-2685	VX307H-RA21H-000N000V1P [(1) (3)] VX307H-RA21H-000N000V1Q [(1) (3)]	Rugged Air-Cooled 'RA' (-40°C to +70°C) [(1) (3)] Intel(r) Xeon-D2896TER Processor (30M Cache, up to 3.20 GHz) 110W TDP, 20 cores 64 GB soldered SDRAM with ECC No VITA 48 2LM covers Rear module profile is aligned with MOD3p-PAY-1F1U1S1S1U1U4F1J-16.6.13-1 *with 40GBase-KR4 (Auto-negotiation mode only), 10GBase-KR Data Plane (Auto-negotiation mode only), 1000Base-KX Control Plane (does not support IEEE802.3 clause 73 backplane auto-negotiation), x16 PCIe Gen3 Expansion Plane* No Front I/O connectors Top 2242 M.2 slot : up to D5 and M Key with x2 PCIe up to Gen3 Bottom 2242 M.2 slot : up to D5 and M Key with x2 PCIe up to Gen3 RTC Power sourced from system VPX VBAT VITA 46.11 Support TPM 2.0 Secure element PBIT RT & NVMe SSD on the Top or Bottom M.2 slot with preloaded Linux Conformal Coating [(2)]

Note (1): EFT Order codes restricted to an EVAL/ Lab-grade use case. EVAL/EFT boards are not qualified. See also Section “Environmental Specifications”

Note (2): Conformal coating is present on qualified products. Early prototypes or unqualified products may be delivered without conformal coating.

Note (3): Refer to the product Release Note for more information about the EFT or product limitations.

Table 5: Available Tooling equipment

Use Case	Ordering Code	Commercial Code	Description
EVAL Lab-grade	1070-5679	FB-VX3-0010	Tooling equipment for lab use. Tooling kit providing one serial line, one USB2.0 port and one RJ45 1000Base-T Ethernet. Serial, USB2.0 and Ethernet interfaces definition presented in section 4.1 is applicable to the FB-VX3-0010 kit
EVAL Lab-grade	1065-0152	PB-VX3-40G-H-601	3U single slot 5 HP (1.0") VPX Rear Transition Module providing serial lines for standard VX307H boards. Tooling equipment for lab use.

1.3.4. I/O Interfaces

› Front Interfaces

Figure 5: Front view of the RA variant

Figure 6: RC3 variant - Front Panel Interfaces - FB-VX3-0010 tooling option not equipped

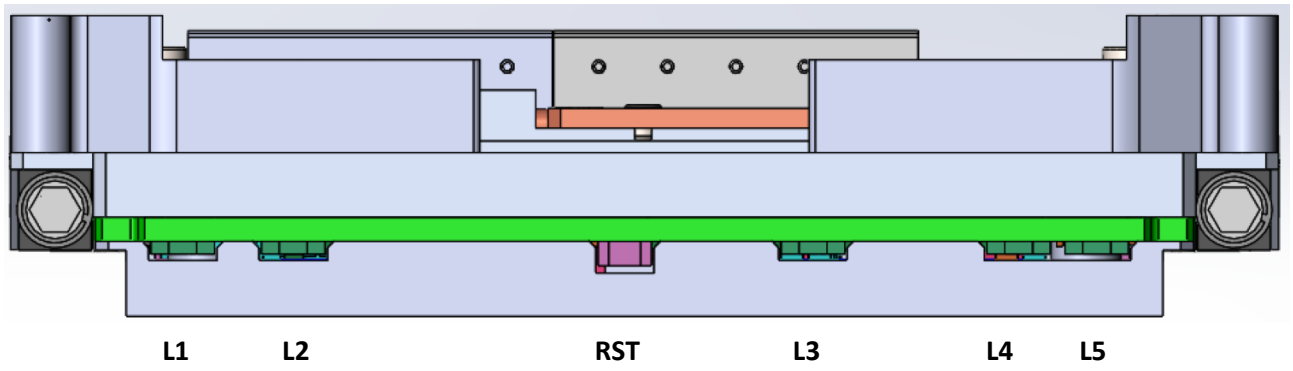


Figure 7: RC3 variant - Front Panel Interfaces - FB-VX3-0010 tooling option equipped

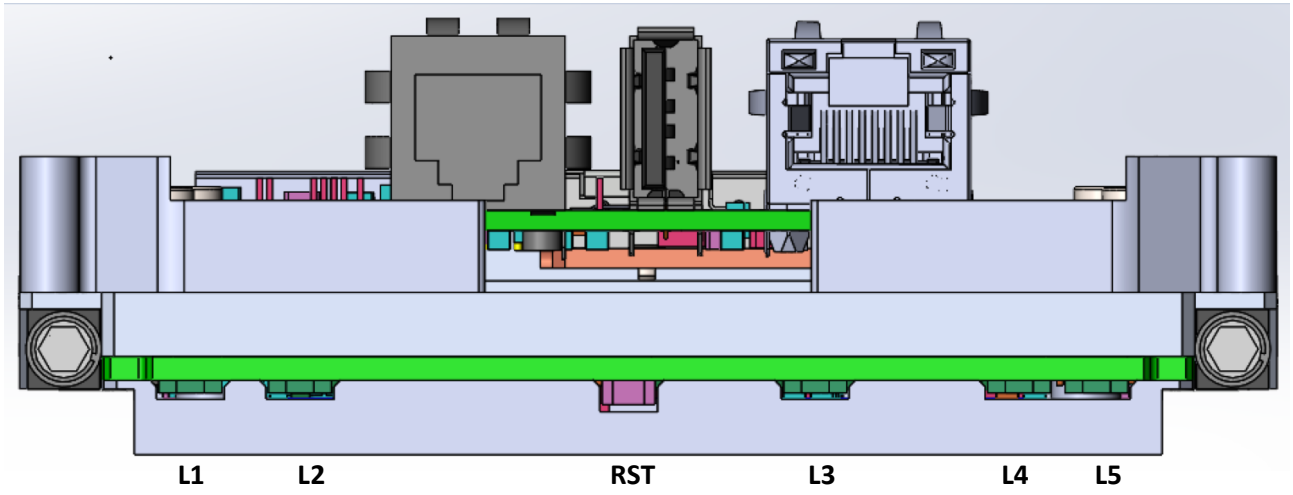


Table 6: Front Panel - Interfaces

FUNCTION	DESCRIPTION	SEE ALSO
RST	Reset push button	Front Interfaces
Lx	LED indicators reporting the board CPU health status and activity	Section 4.4 for LEDs Description
SERIAL	RJ12 serial port	
USB	USB2.0 port	
ETH	RJ45 Ethernet port	

The front panel push button must be handled with care. Use a non-metallic and blunt tool with a rounded tip (tip diameter must be roughly equal to the front panel button surface)

- Rear Interfaces

  VX307H SOSA variant with the Compute Intensive manufacturing options:
  - Compatible with SLT3-PAY-1F1U1S1S1U1U4F1J-14.6.13-n and SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-0
  - if P2A not loaded: Compatible with MOD3p-PAY-1F1U1S1S1U1U2F1H-16.6.11-4
  - if P2A loaded: Compatible with MOD3p-PAY-1F1U1S1S1U1U4F1J-16.6.13-1

1.3.5. Components Layout

Figure 8: Components Layout (Top view)

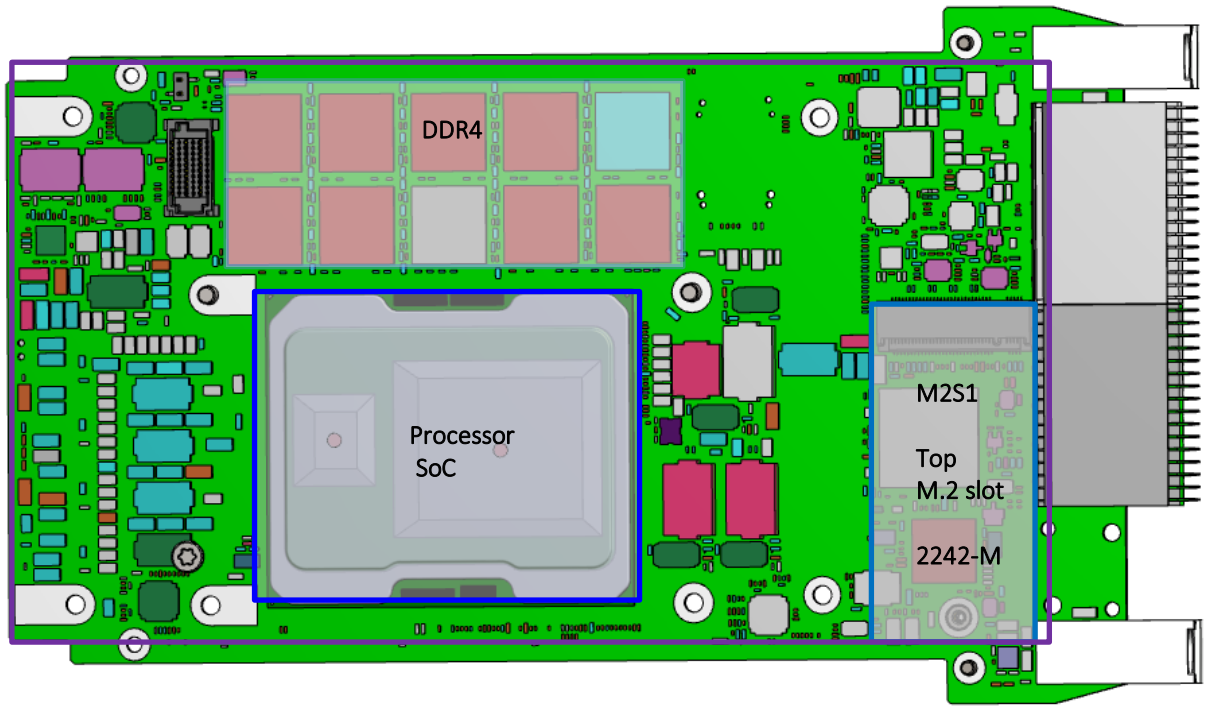
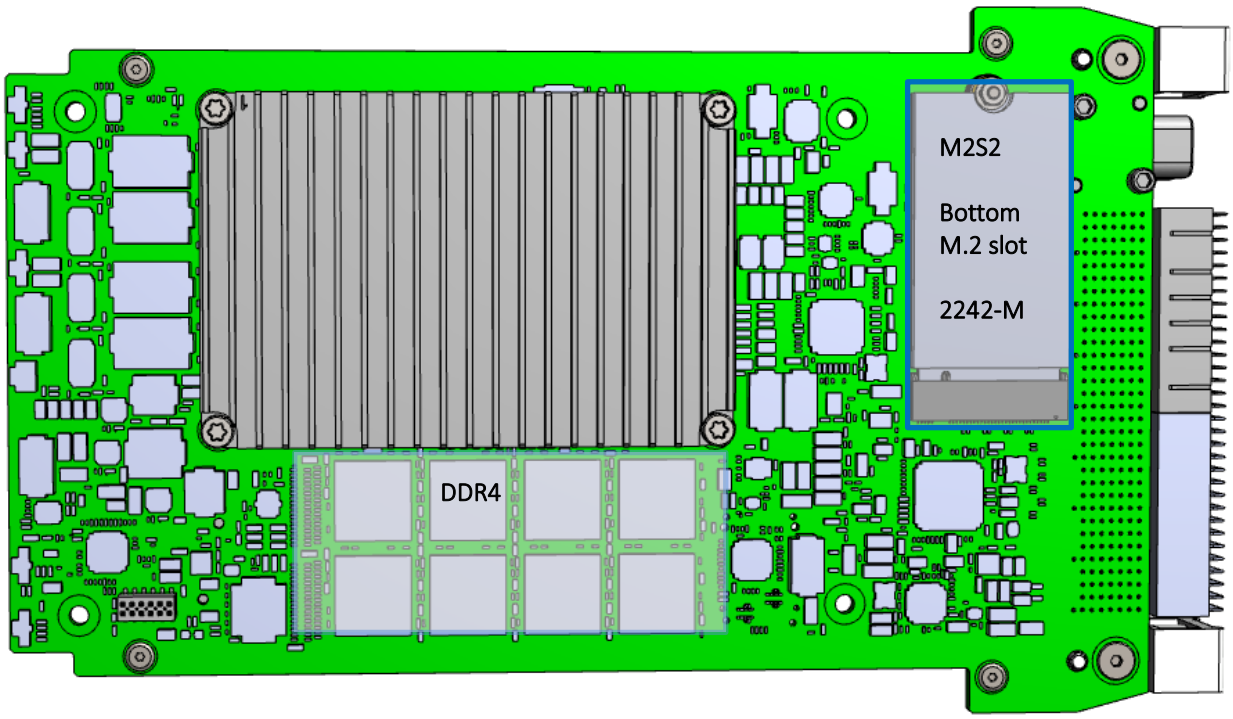


Figure 9: Components Layout (Bottom view)



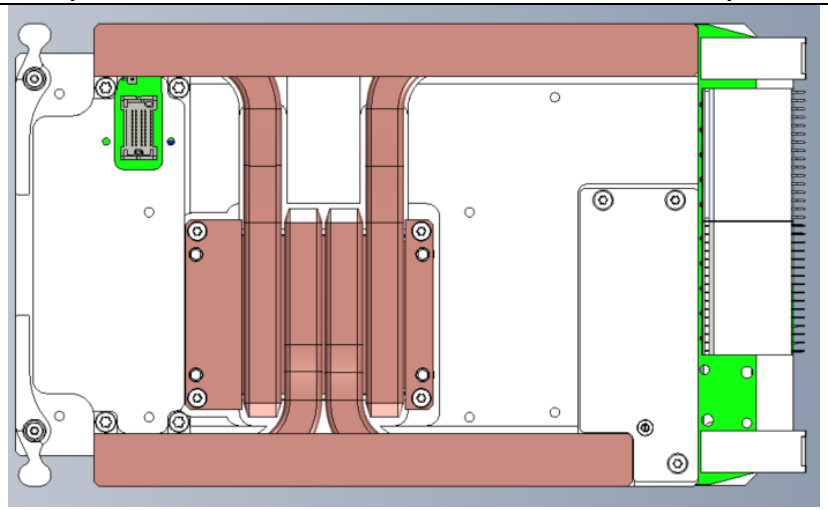
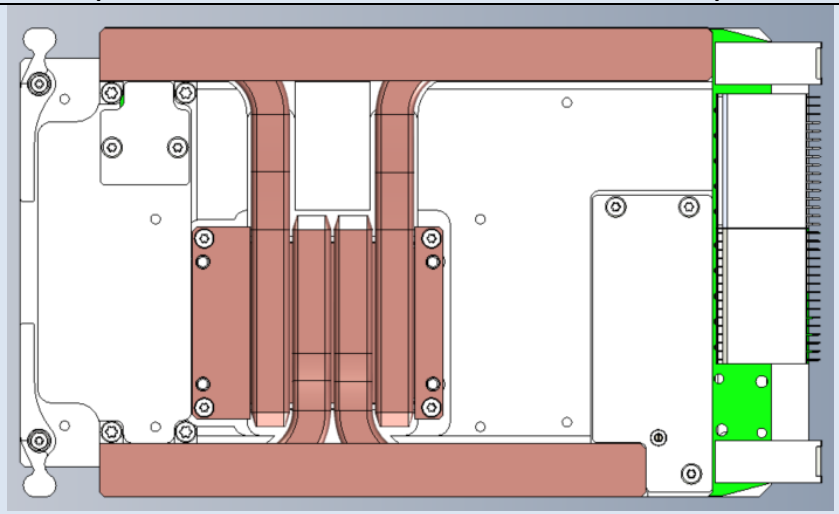
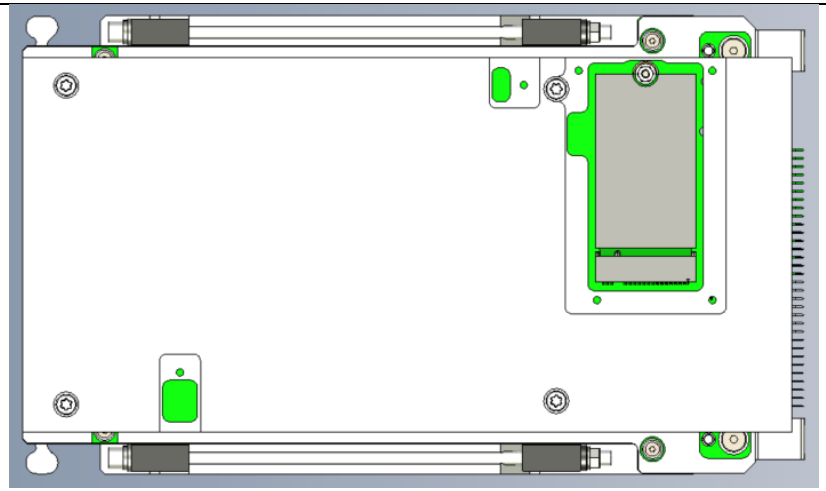
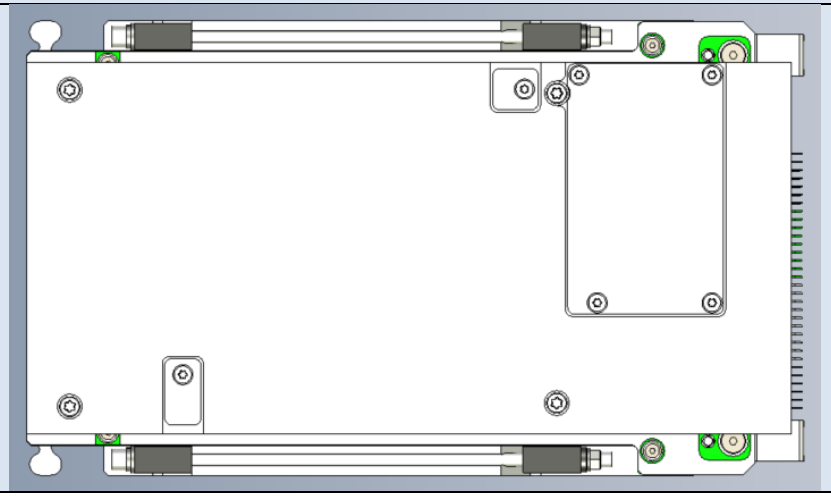
1.3.6. Tested M.2 Module List

Table 7: Non-exhaustive M.2 module list, tested on the product

Module Type	Tested slot	Upstream interface option selected on the M.2 socket	Capacity	Manufacturer	Part Number
SSD SATA, Type 2242 M	M2S1 M2S2	SATA	256 GB	Innodisk	DEM24-B56DK1GW1DL(-P62)
SSD NVME, Type 2242 M	M2S1 M2S2	PCIe	1 TB	Innodisk	DEM24-01TDD1GWAQF
SSD NVME, Type 2242 M	M2S1 M2S2	PCIe	960 GB	Innodisk	DEM24-01TDH1KWAQF-JT56
SSD NVME, Type 2242 M	M2S1 M2S2	PCIe	320 GB	Virtium	VTPM24CEXI320-BK110C

1.3.7. Conduction Cooled Product - Mechanical cover equipment without and with the “2LM” product option

Table 8: Views of the VX307H-RC COTS without and with the 2LM option

Top/bottom views of the VX307H-RC COTS without the 2LM option	Top/bottom views of the VX307H-RC COTS with the 2LM option
	
	

1.4. Environmental Specifications

The applicable environment class depends on the ordered VX307H variant

Table 9: Environmental Specifications – Standard and extended classes

Environmental class	RA Rugged Air-Cooled
Plugin unit type	3U VPX Module Vita 46.0 specification, Type2, corrected by REDI VITA 48.1 July 2010
Conformal Coating	Optional
Airflow	Refer to section 5.5
Cooling Method	Convection
Operating	Inlet air temperature from -40 °C to +70 °C (1)
Storage	-50 °C to +100 °C
Vibration Sine (Operating)	1 hour per axis: 5-20Hz : 2mm, 20-2000Hz : 3g
Random (Operating)	1 hour per axis: 5-100Hz : PSD = +3dB/octave 100-1000Hz : PSD = 0.04g2/Hz 1000-2000Hz : PSD = -6dB.octave
Shock (Operating)	½ sinus 20g 11ms
Relative Humidity	90 % without condensation (95 % without condensation and with coating option)

Table 10: Environmental Specifications - Rugged classes

Environmental class	AFT2 Rugged Air-cooled	AFT3 Rugged Air-cooled	RC Rugged Conduction cooled
Plugin unit type	3U VPX Module Vita 46.0 specification, corrected by REDI VITA 48.8 December 2022 (7.5HP)	3U VPX Module Vita 46.0 specification, corrected by REDI VITA 48.8 December 2022 (7.5HP)	5HP, Type 2, secondary side retainers, REDI VITA 48.2-2022 (7.5HP)
Conformal Coating	Standard	Standard	Standard
Airflow	Refer to section 5.6	Refer to section 5.6	NA
Cooling Method	Air Flow Through	Air Flow Through	Conduction – Refer to section 5.7
Operating	Inlet air temperature from -40 °C to +55 °C (1) (3)	Inlet air temperature from -40 °C to +70 °C (1) (3)	Card edge temperature from -40 °C to +70 °C (2) (3)
Storage	-50 °C to +100 °C	-50 °C to +100 °C	-50 °C to +100 °C
Vibration Sine (Operating)	1 hour per axis: 5-20 Hz, displacement 2.5 mm 20-2000 Hz, 5 g	1 hour per axis: 5-20 Hz, displacement 2.5 mm 20-2000 Hz, 5 g	1 hour per axis: 5-20 Hz, displacement 2.5 mm 20-2000 Hz, 5 g
Random (Operating)	1 hour per axis: 5 Hz to 100 Hz PSD increasing at +3 dB/octave 100 Hz to 1000 Hz PSD = 0.1 g^2/Hz 1000 Hz to 2000 Hz PSD decreasing at -6 dB/octave	1 hour per axis: 5 Hz to 100 Hz PSD increasing at +3 dB/octave 100 Hz to 1000 Hz PSD = 0.1 g^2/Hz 1000 Hz to 2000 Hz PSD decreasing at -6 dB/octave	1 hour per axis: 5 Hz to 100 Hz PSD increasing at +3 dB/octave 100 Hz to 1000 Hz PSD = 0.1 g^2/Hz 1000 Hz to 2000 Hz PSD decreasing at -6 dB/octave
Shock (Operating)	40 g / 11 ms, half sine	40 g / 11 ms, half sine	40 g / 11 ms, half sine
Altitude (Operating)	-1,500 to 60,000 ft	-1,500 to 60,000 ft	-1,500 to 60,000 ft
Relative Humidity	95 % without condensation	95 % without condensation	95 % without condensation

(1) According to Thermal characterization performed in laminar flow bench following Kontron procedure.

(2) Maximum temperature measured at card edge in the following conditions: processor performance rate @80% all cores, maximum processor TDP without CPU throttling.

(3) Refer to the Intel EDS documents for detailed information about DTR = Dynamic Temperature Range limitations. The default maximum processor temperature range during operation is ±145°C, starting from boot time temperature, with CPU PCIe Gen3 and PCH PCIe/SATA Gen2 speed limitations. For more information, contact Kontron Support.

Table 11: Lab-grade Environmental Specifications for Prototypes or EVAL Variants

Lab-grade air-cooled version	
Conformal Coating	optional
Inlet Airflow	3 m/s
Cooling Method	Convection or conduction
Operating	10 °C to +30 °C
Known product limitations	Refer to the active release note for detailed information. Ask Kontron.
Other specifications	According to standard lab conditions The use case as per EU directive is applicable: custom built evaluation kits destined for professionals to be used solely at research and development facilities for such purposes

Lab-grade conduction cooled version	
Conformal Coating	Optional
Cooling Method	Conduction
Max card edge Operating Temperature	0 °C to +30 °C
Known product limitations	Refer to the active release note for detailed information. Ask Kontron.
Other specifications	According to standard lab conditions The use case as per EU directive is applicable: custom built evaluation kits destined for professionals to be used solely at research and development facilities for such purposes

1.5. Board Weight/Mass

Table 12: Board Weight / Mass

Mass	
VX307H-RC316G-000N000V1P Without any M.2 module	~650 g

1.6. MTBF

Table 13: MTBF

MTBF at sea level Standard KFR method Model based on the methods andguidelines outlined in MIL-HDBK217 Revision F2	GB (Hours)	
	25 °C	40 °C
VX307H-RC321H-000N000V1P Without any M.2 module	356 449 hrs	300 000 hrs

Ask to Kontron for MTBF values related to other or custom mission profiles.

1.7. Related Publications

The following publications contain information relating to this product:.

Table 14: VX6096 COTS - Related publications

Product	Document ID	Publication
VX307H	D309280	Hardware Release Notes
VX307H	D283956	AMI-BIOS User Reference Manual
VX307H	D234669	PBIT User Guide
VX30xx product family	D298811	VITA 46.11 Firmware Release Note
VX30xx product family	D275280	Kontron VME/VPX Fedora Remix Release Notes

Table 15: VITA - Related publications

Designation	Title	Abstract	VITA Status – April 2025
ANSI/VITA 42.0-2021	XMC: Switched Mezzanine Card (XMC) Auxiliary Standard	This document defines an open standard for supporting high-speed, switched interconnect protocols on an existing, widely deployed mezzanine card form factor.	ANSI/VITA Approved
ANSI/VITA 46.0-2023 +Errata	VPX Baseline Standard	This standard describes VITA 46.0 VPX Baseline Standard; an evolutionary step forward for the provision of high-speed interconnects in harsh environment applications.	ANSI/VITA Approved
ANSI/VITA 46.9-2018 (R2024)	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard	This document describes an open standard for PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	ANSI/VITA Reaffirmed
ANSI/VITA 46.10-2009 (S2024)	Rear Transition Module for VPX	This standard defines signal mapping for VPX Rear Transition Modules (RTMs).	ANSI/VITA Stabilized Maintenance
ANSI/VITA 46.11-2022	System Management on VPX	This document defines a framework for System Management in VPX systems. It enables interoperability within the VPX ecosystem at the Field Replaceable Unit (FRU), chassis and system levels.	ANSI/VITA Approved
ANSI/VITA 47.0-2019	Construction, Safety, and Quality for Plug-In Modules Standard	The VITA 47 group of standards defines environmental, design and construction, safety, and quality requirements for commercial-off-the-shelf (COTS) Plug-In Modules intended for ground and aerospace applications.	ANSI/VITA Approved
ANSI/VITA 48.0-2022	Mechanical Standard for Microcomputers using Ruggedized	This standard defines a mechanical implementation for Plug-In Modules.	ANSI/VITA Approved

Designation	Title	Abstract	VITA Status – April 2025
	Enhanced Design Implementation (REDI)		
ANSI/VITA 48.2-2022	Mechanical Standard for VPX REDI Conduction Cooling	This standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	ANSI/VITA Approved
ANSI/VITA 48.8-2022	Mechanical Standard for VPX REDI Air Flow Through Cooling, 1.0 "to 1.5 "Pitches	This document describes an open standard for the design requirements for an air-flow-through cooled plug-in module having 3U and 6U form factors while retaining the VITA 46.0 connector layout.	ANSI/VITA Approved
ANSI/VITA 51.0-2012 (S2024)	Reliability Prediction	This document provides a framework for electronics equipment reliability standards, and establishes a reliability Community of Practice.	ANSI/VITA Stabilized Maintenance
ANSI/VITA 61.0-2022	XMC 2.0	This standard is based upon VITA 42.0 XMC. It defines an open standard for supporting high-speed, switched interconnect protocols on the existing, widely deployed XMC form factor.	ANSI/VITA Approved
ANSI/VITA 65.0-2023	OpenVPX System Standard	The OpenVPX System Standard was created to bring versatile system architectural solutions to the VPX market.	ANSI/VITA Approved
ANSI/VITA 65.1-2023	OpenVPX System Standard –Profile Tables	This standard documents variations of Slot, Backplane, and Modules Profiles.	ANSI/VITA Approved
ANSI/VITA 88.0-2021	Switched Mezzanine Card Plus (XMC+) Standard	This document defines a standard for improved electrical/mechanical mezzanine connectors for XMC applications.	ANSI/VITA Approved

Table 16: SOSA - Related publications

Title / Version	Comment
SOSA Reference Architecture (C119)	SOA Reference Architecture. Technical Standard (2011)
SOSA Technical Standard Reference Architecture (S221)	The Open Group Snapshot (2022)
Technical Standard for SOSA™ Reference Architecture (S241)	The Open Group Snapshot (2024)

2. Installation

The VX307H has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

2.1. Safety Requirements

The following safety precautions must be observed when installing or operating the VX307H. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

This board contains electrostatically sensitive devices. Observe the necessary precautions to avoid damage to your board:
Discharge your clothing before touching the assembly. Tools must be discharged before use.
Do not touch components, connector pins or traces.
We strongly recommend our customers to work in an environment equipped with antistatic workbenches with professional discharging equipments.

HOT Surface!
Special care shall be taken while handling the board: the heat sink or heat frame can get very hot during operation. Do not touch the heat sink when installing or removing the board.
In addition, the board should not be placed on any surface or in any form of storage container before the board and heat sink have cooled down to room temperature.

2.2. Board Identification

The VX307H boards are identified by labels fitted to the top side of the board.
The E.C. Level format is "xxxxxLy" where

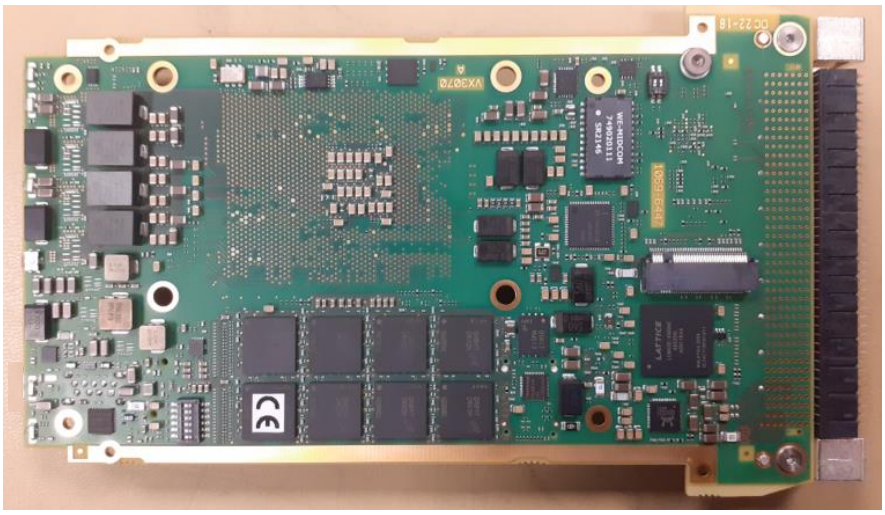
- The five digits "xxxxx" indicate the board E.C. Level (PCB revision included)
- "Ly" indicates the mechanical E.C. Level:
  - letter "L" varies with the environment class ("A" for SA, "B" for WA, "C" for RA and "D" for RC)
  - digit "y" gives the mechanical E.C. Level.

› Top Side

A "Identification" label: Order Code, Serial Number, Variant, E.C. Level, Ethernet MAC addresses

Figure 10: Product Identification (Top Side)

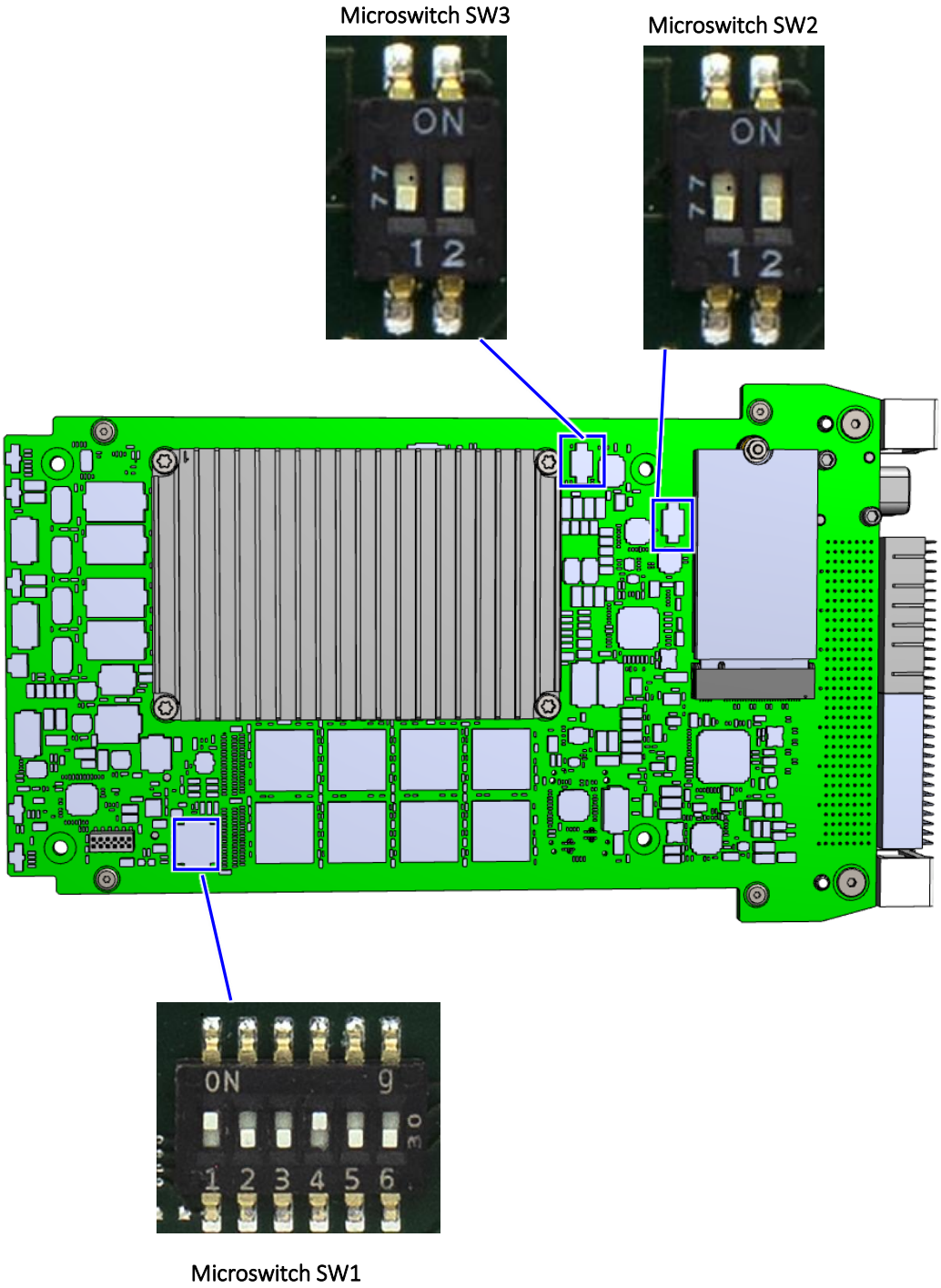
Figure 11: Product identification (Bottom Side, without 2LM option)



2.3. Board Configuration

2.3.1. Microswitches location

Figure 12: Board Configuration (Bottom view)



2.3.2. SW1 Microswitch description

Table 17: SW1 Microswitch Description

SW1		
#	Function	Description
1	FACTORY_MODE	OFF: Normal operation ON : Enable special config for factory tests (NVMRO masked, …)
2	VPD_WP	OFF: Normal operation ON : force **unprotection** of devices in “VPD” domain (see "Write protection")
3	USER_WP	OFF: Normal operation ON : force protection of devices in “USER” domain (see "Write protection")
4	DBG_MODE	OFF: Normal operation ON : Debug mode enabled
5	BIOS_FAILSAFE	OFF: Normal operation ON : start software in failsafe mode for recovery purpose
6	CS_SWAP	OFF: Normal operation ON : boot on rescue BIOS (swap of CS0/CS1 SPI boot flash chip select)

2.3.3. SW2 Microswitch description

Table 18: SW2 Microswitch Description

SW2		
#	Function	Description
1	FORCE_SINGLE_CHANNEL	OFF: Normal operation ON : Reserved
2	NVMRO_OFF	OFF: Normal operation ON : force NVMRO off on backplane and on local board

2.3.4. SW3 Microswitch description

Table 19: SW3 Microswitch Description

SW3 only for VX307H with IPMI		
#	Function	Description
1	BMC_PROG	OFF: Normal operation ON : Reserved
2	SW3_SPARE	OFF: Normal operation ON: Reserved

2.4. Package Contents

The package contents vary with the VX307H variant.

- VX307H variant - see section “Ordering Information”. Board equipment differs depending on the ordered Order Code.
- Bolt accessories for mezzanine/module mounting

2.5. Initial Installation Procedures

The following procedures are applicable only for the initial installation of the VX307H in a system.
Procedures for standard removal operations are found in their respective chapters.

To perform an initial installation of the VX307H in a system, proceed as follows:

1. Ensure that the safety requirements indicated in section “Safety Requirements” are observed.

CAUTION: Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For the configuration and installation of VX307H, specific peripheral devices and Rear I/O devices refer to the appropriate sections in current Chapter.

CAUTION: Care must be taken when applying the procedures below to ensure that neither the VX307H nor other system boards are physically damaged by the application of these procedures.

3. To install the VX307H, perform the following:

a. Ensure that no power is applied to the system before proceeding.

b. Select the slot where the board should be inserted as per application requirements. Then carefully insert the board until it makes contact with the backplane connectors.

Conduction Cooled variants: when performing the next step and when the chassis accommodating the board is compliant with VITA48.2, it is recommended to use the ejector handles to seat the board into the backplane connectors. For the other chassis, simply push the board into the backplane connectors.

c. Engage the board with the backplane using the ejector handle until the handle is locked. In RC configurations (no handle or handle not locked), push the board until it is fully seated in the backplane.

d. RA class board type: Tight the front panel screws to lock the board.

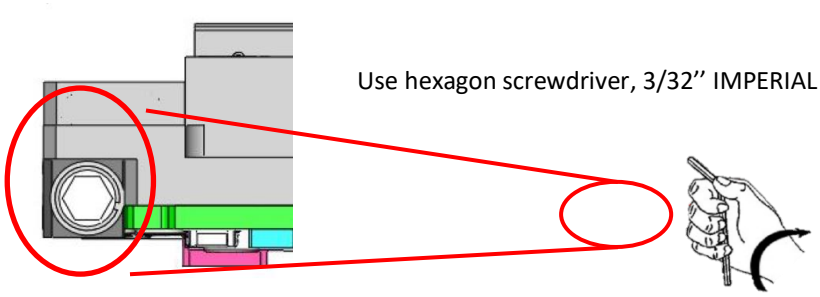
RC class board type: Tight the wedgelocks to the cold plate. A torque of 0.68 N.m must be applied to the wedgelock screw

e. Ensure that the board is properly secured.

The VX307H is now ready for operation. Refer to appropriate VX307H specific software, application, and system documentation.

Figure 13: RA variant - Screws Location on the front panel

Figure 14: RC variant - Wedgelock Screw Location



⚠CAUTION Running the board at high temperature without tightening the wedgelocks to the cold plate may result in permanent damage to the board.

2.6. Standard Removal Procedure

ESD sensitive Device! Precautions are listed in Section "Safety Requirements"

To remove the board from the chassis, proceed as follows:

1. Ensure that the safety requirements indicated in Section "Safety Requirements" are observed. Particular attention must be paid to the warning regarding the heat frame!

CAUTION: Care must be taken when applying the procedures below to ensure that neither the VX307H nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. RC class type board: loosen the wedgelocks
4. Disengage the board from the backplane using the board ejection handle, press the handle until the board is disengaged.
5. After disengaging the board from the backplane, pull the board out of the slot.

HOT Surface!
Due care should be exercised when handling the board due to the fact that the heat frame can get very hot. Do not touch the heat frame when changing the board.

6. Dispose of the board as required.

2.7. XMC Installation

Not available on VX307H variants.

2.8. M.2 Module Insertion / Removal Instructions

› Supported M.2 Module Type

The M.2 socket (M2S1 & M2S2) is compliant with NVME PCIe interfaces.

The socket can host the 2242-B-M modules

› M.2 Module Insertion Process

› M.2 Module Insertion Process

ESD sensitive Device! Precautions are listed in Section “Safety Requirements”

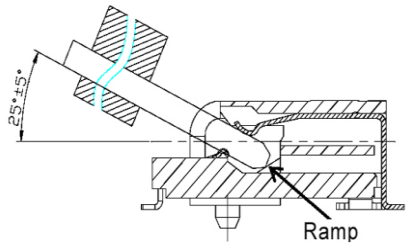
Apply "Loctite 222" threadlock or equivalent on each screw during reassembly of the M.2 module

1. If 2LM cover option is present, Disassemble the top or bottom M.2 cover according the the 2LM cover procedure. Remove flat washer and hexagon thin nut. See figures below.

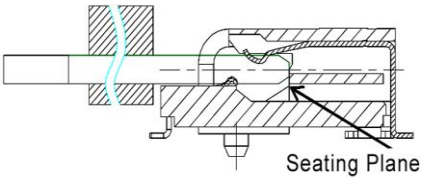
2. For VX307H variants requiring a standoff (in a separate bag included in packaging), place the standoff above the mounting hole.

M.2 Module Insertion

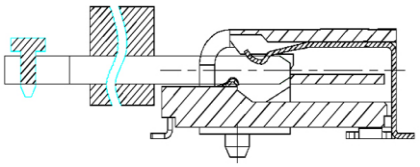
3. Insert the module at an angle of 25°±5° until the module makes contact with the ramp



4. Rotate the module to horizontal position and make sure the card’s edge makes contact with the seating plane.



6. Attach the module using appropriate mechanical parts (washer, nut or screw) as described in figures below.



6. For Rugged variants, adhesive is required as shown in pictures below.

Figure 15: RA variant – M.2 module mounting, without 2LM cover option.

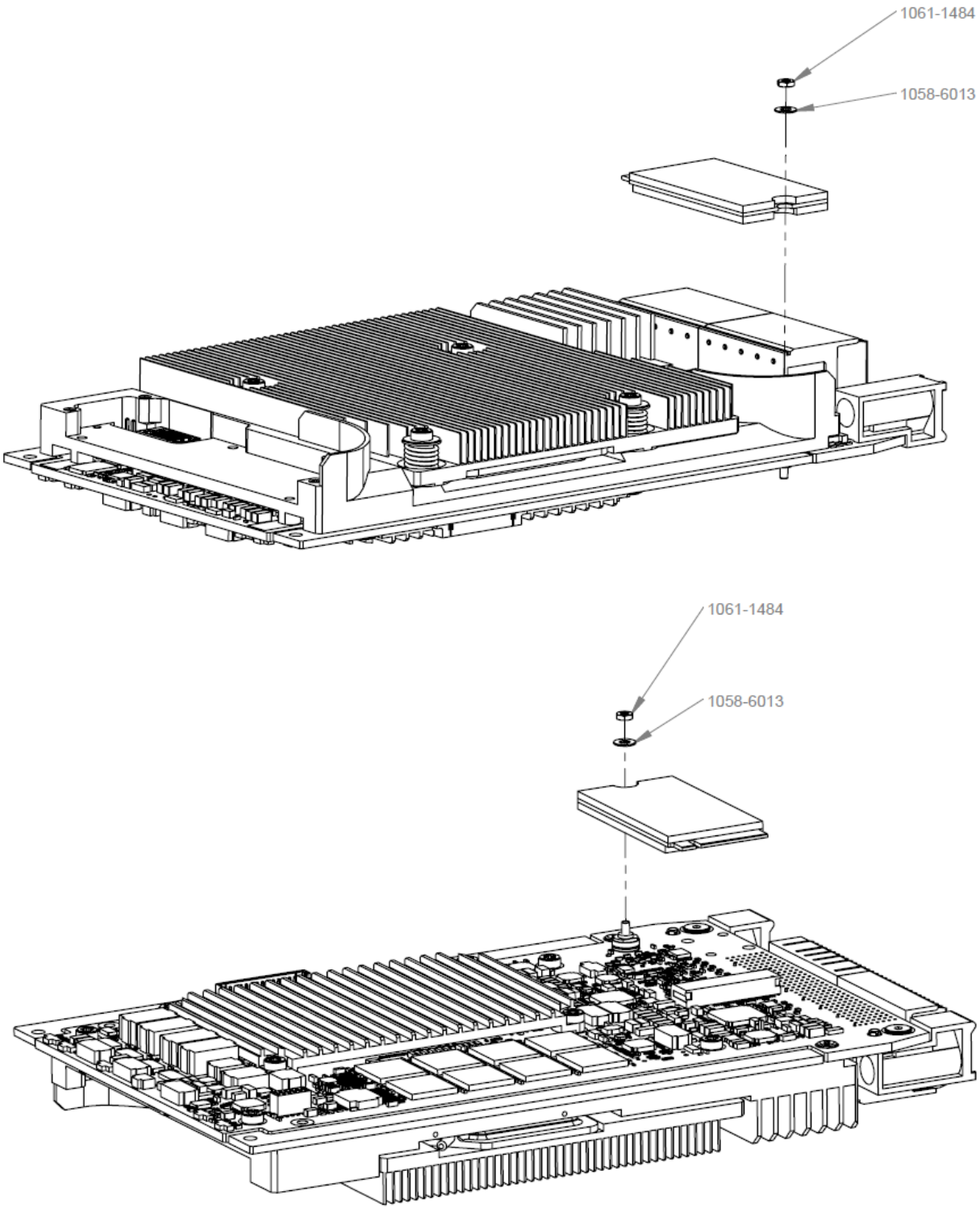


Table 20: RA variant M.2 module mounting – nut and washer defintion

Article	DESCRIPTION	Qty	Torque	Thread lock
1058-6013	WASHER ISO 7092-2-200HV-A4	1	-	-
1061-1484	HEXAGON THIN NUT ISO 4035-M1.6-A4-70	1	0.09 N.m	Loctite 222 Or equivalent

Figure 16: RC variant – Top/bottom M.2 module mounting, without 2LM cover option

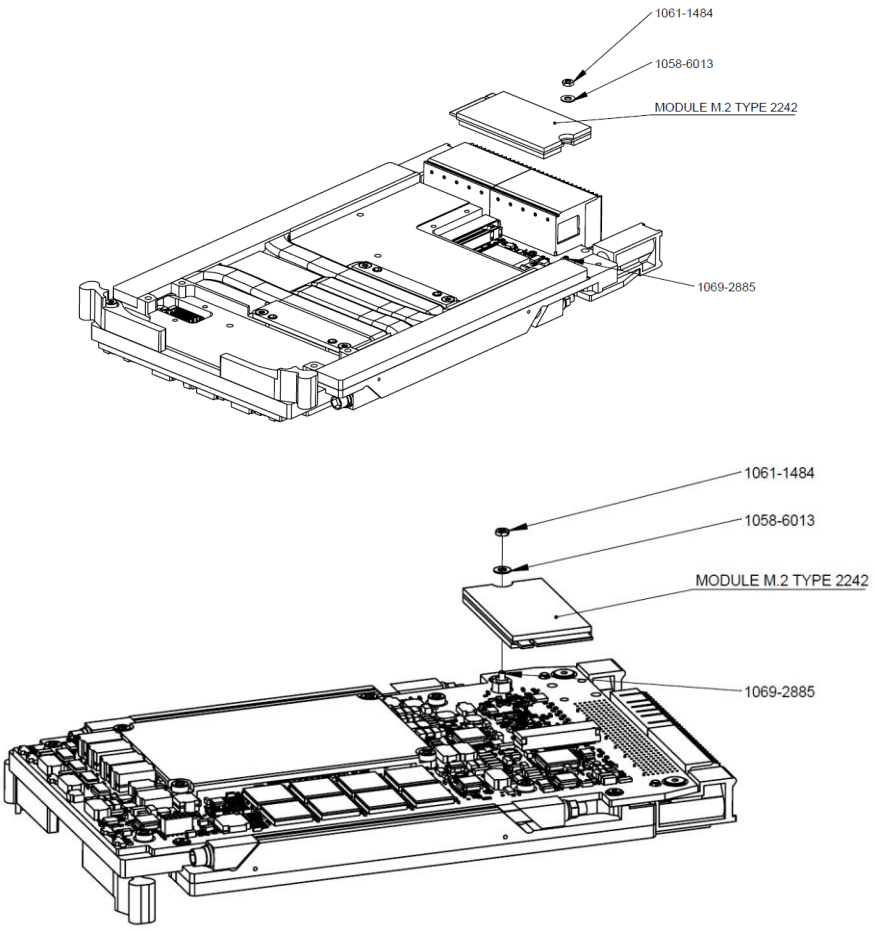
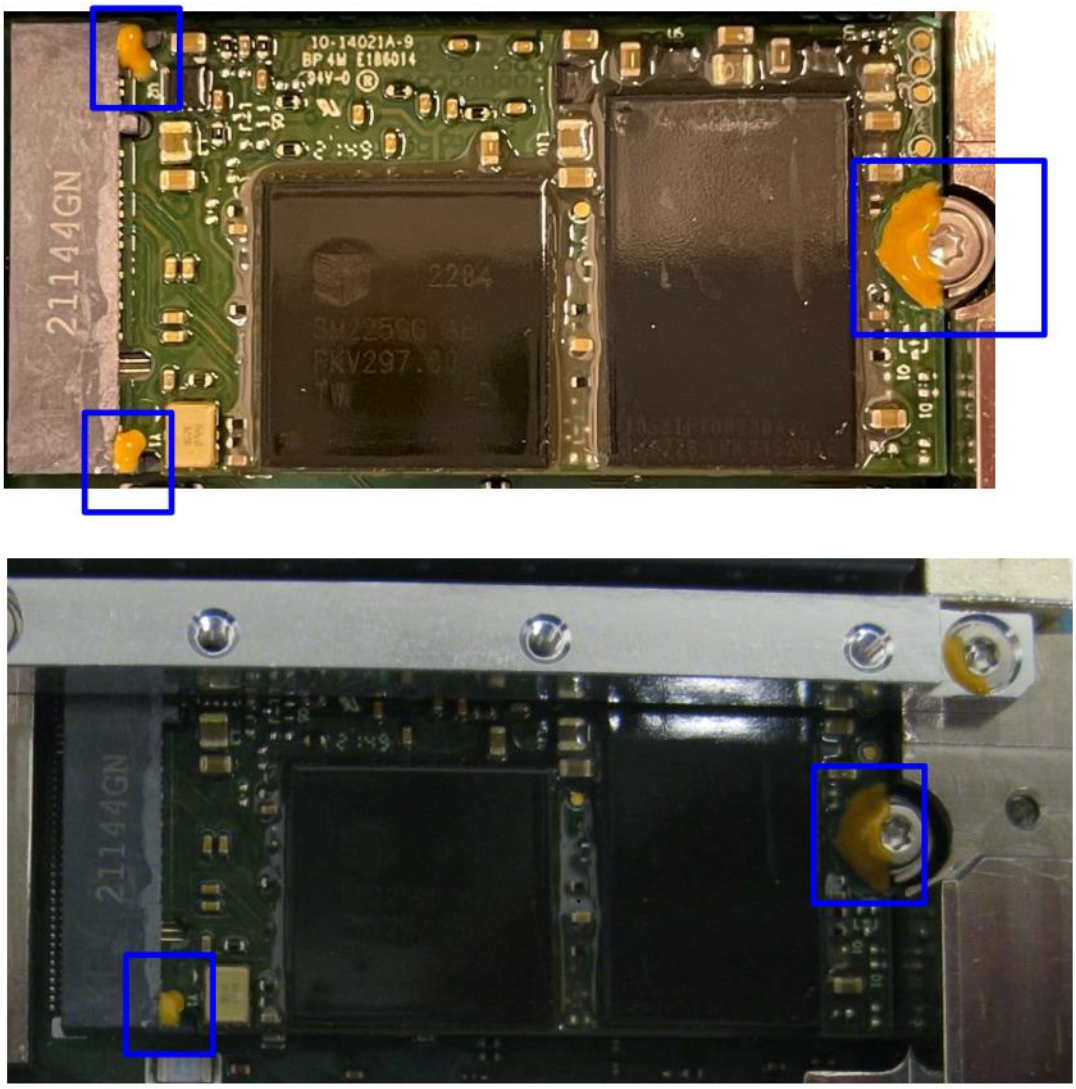


Table 21: RC variant - M.2 module mounting – nut and washer defintion

Article	DESCRIPTION	Qty	Torque	Thread lock
1058-6013	WASHER ISO 7092-2-200HV-A4	1	-	-
1061-1484	HEXAGON THIN NUT ISO 4035-M1.6-A4-70	1	0.09 N.m	Loctite 222 Or equivalent

Figure 17: Adhesive application example to lock M.2 Module on RA and RC class rugged boards



⚠CAUTION

For harsh environment applications (RA or RC classes), Kontron recommends to apply adhesives to lock the M.2 module. Such as 3M Scotch-Weld™ 7838, or equivalent: at the junction between the module and the M.2 connector/screw (Blue rectangles on the pictures above)
All screws must be locked with Loctite 222 or equivalent thread lockers

Figure 18: Top M.2 module cover and Thermal interface Material mounting

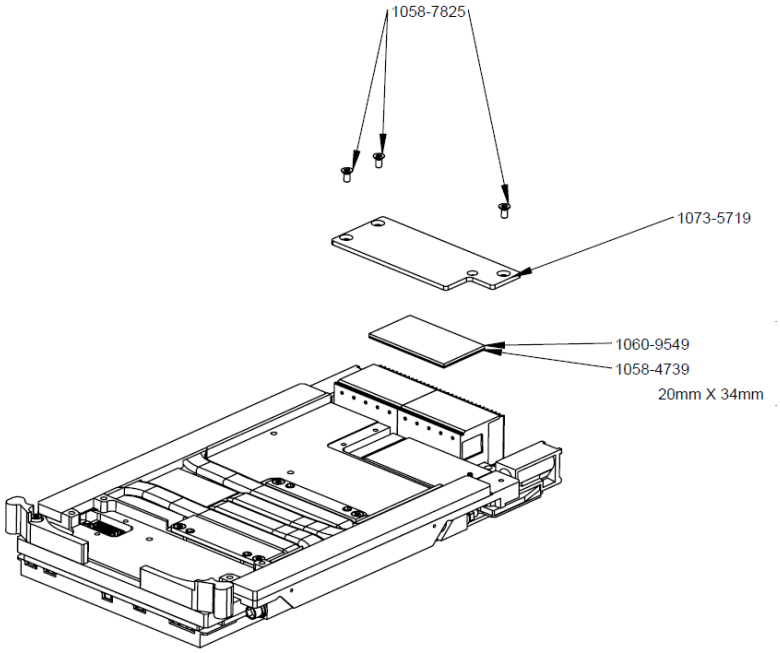
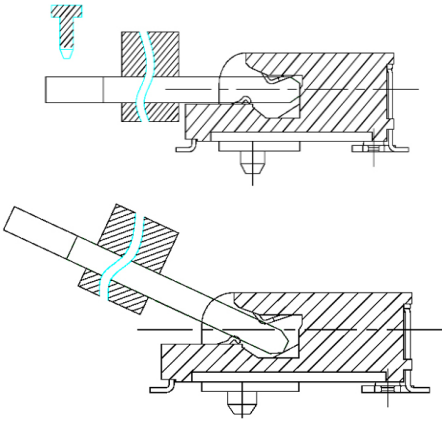


Table 22: Top M.2 module cover and Thermal interface Material mounting

Article	DESCRIPTION	Qty	Torque	Thread lock
1058-7825	COUNTERSUNK FLAT HEAD SCREW ISO 14581-M2X4-A4-70	3	0.2 N.m	Loctite 222 Or equivalent
1060-9549 or 1058-4739	FUJIPOLY PG 80A-00-150BL If the 2242 module is D1 type (20mm x 34mm) or FUJIPOLY PG 80A-00-100BL if the 2242 module is not D1 type (20mm x 34mm)	1	-	-

M.2 Module Removal Process

1. Loosen the screw by hand and the module will be rotated automatically due to connector contact's counterforce at the same time.



2. Take away the module by hand.

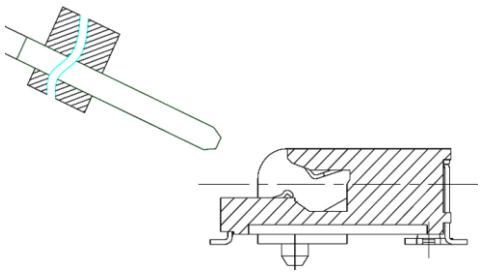


Figure 19: Bottom M.2 module and microswitch covers

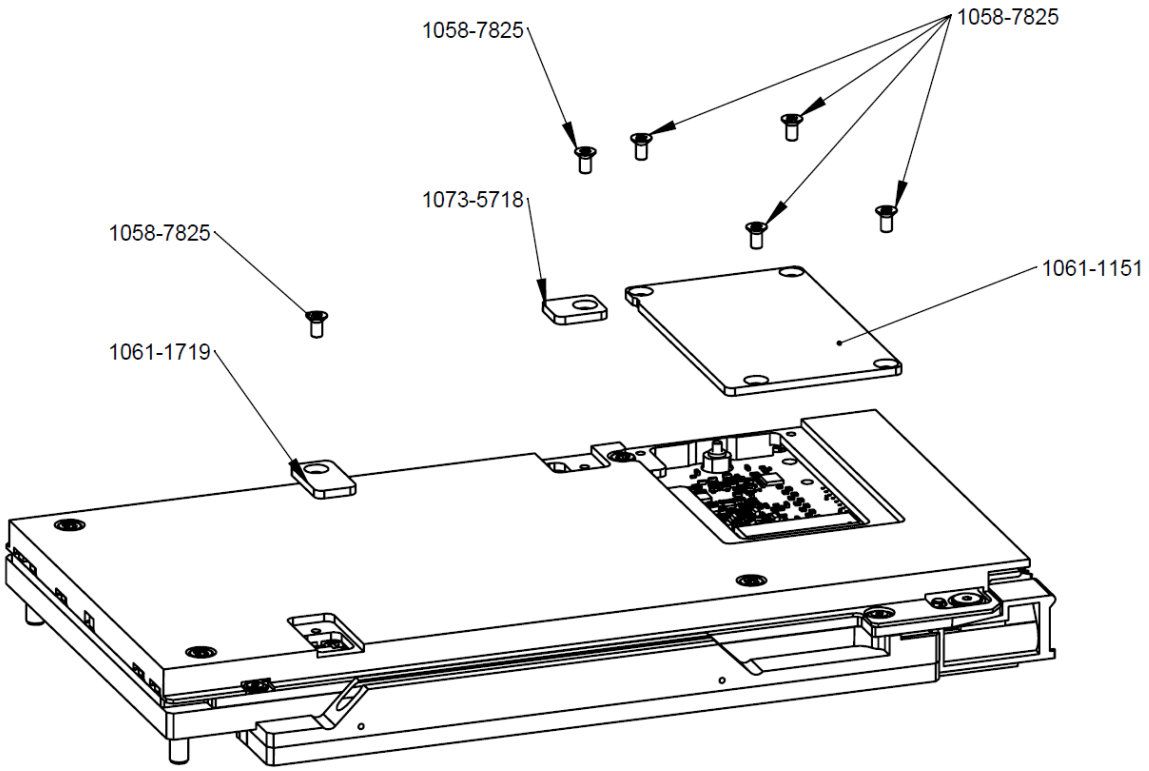


Table 23: Bottom M.2 module cover and Thermal interface Material mounting

Article	DESCRIPTION	Qty	Torque	Thread lock
1058-7825	COUNTERSUNK FLAT HEAD SCREW ISO 14581-M2X4-A4-70	6	0.2 N.m	Loctite 222 Or equivalent

2.9. Software Installation

The installation of all on-board peripheral drivers is described in detail in the relevant Driver Kit files or Board Support Packages (BSP).
The installation of an operating system is dependent of the OS software and is not addressed in this manual.
Refer to appropriate OS software documentation for software installation.

3. Additional Board Feature

3.1. RTC, Watchdog, Timers

3.1.1. Real-Time Clock (RTC)

Two Real Time Clocks (RTC) are available on the VX307H: one is embedded in the CPU while the other is a standalone, high-precision, low-power component (RV-8803) accessed through the PCH SMBus.

- **Standby power supplied to the RV-8803 RTC**
  When the VX307H is powered off, the RTC power supply comes either from the VPX 3.3V_AUX rail or from the VPX VBAT rail. To ensure data retention in the RV-8803 RTC, the VPX VBAT must be set in the range [2.5V - 5.5V]. The maximum current drawn over the -40 °C/+85 °C temperature range is 500 nA (VBAT= 3 V, no I2C activity) or 550 nA (VBAT=5 V, no I2C activity).

- **Internal Integrated PCH RTC**
  The integrated PCH RTC module provides a date and time keeping device with two banks of static RAM with 128 bytes each although the first bank has 114 bytes for general-purpose usage. The BIOS programs the RTC interrupt on Legacy IRQ8 that is never shared with other interrupts. It is clocked by an external 32.768 KHz oscillator with a parabolic coefficient of 0.4 ppm/°C² and a stability of +/-20 ppm at 25 °C. A 20 ppm stability is equivalent to a 10 mn/year drift.

- **Standalone low-power RTC RV-8803**
  The RV-8803 RTC by Micro Crystal includes an internal oscillator and a date and time keeping module with programmable alarm, timer and interrupt functions. It features an ultra low-power consumption in time keeping mode: 240 nA typical and 800 nA maximum in worst case conditions.
  RV-8803 offers a very high Time Accuracy (best in class): ±1.5 ppm 0 to +50°C, ±3.0 ppm -40 to +85°C, ±7.0 ppm +85 to +105°C.

- **RTC management by BIOS and OS**
  At each startup, the BIOS retrieves the date and time information from the high-precision RV-8803 RTC and copies it into the integrated PCH RTC.
  Any update of date and time in the BIOS settings will be done both in integrated PCH RTC and RV-8803 RTC.
  Regarding the RTC management by the OS, the OS should use the high-precision RV-8803 RTC driver. Failing to do so, the updates will be done only in integrated PCH RTC and will not be saved.
  If no power is applied on the RV-8803 RTC, the BIOS displays the BIOS build date and time instead of the current date and time.

- **Century flag**
  For compatibility reasons, the BIOS implements the century flag for the high-precision RTC as follows:
    - Century Flag C = 0 for 1900-1999 years
    - Century Flag C = 1 for 2000-2099 years.

  The user should check that the OS driver implements the same convention.

3.1.2. CPLD Watchdog

In addition to the standard watchdog timer included in the integrated PCH, the cPLD implements a hardware watchdog timer that can be used by the operating software to monitor the normal operation of the system.
It is enabled by software, and once enabled must be restarted at regular intervals. If not, its expiration sets off an interrupt (IRQ) to the local processor, a board reset or a board power-cycle.
The watchdog has the following features:

- timeout programmable from 1 to 511 clock periods, by steps of 2 periods
- clock periods of 1s or 1ms
- lock bit: when set, can only refresh (restart) the watchdog, but not change its settings
- 4 modes: timer, reset, interrupt or power-cycle
- restart counter: can manage the remaining number of resets or power-cycles done by the watchdog before giving-up.

3.2. I2C Structure

The VX307H features several I2C busses.

- Two are attached to the integrated Platform Hub Controller and control the DDR4 SPD EEPROM and the low-power RTC.
- The other two are handled by the CPLD device and by the IPMC device

Figure 20: I2C Block Diagram for information

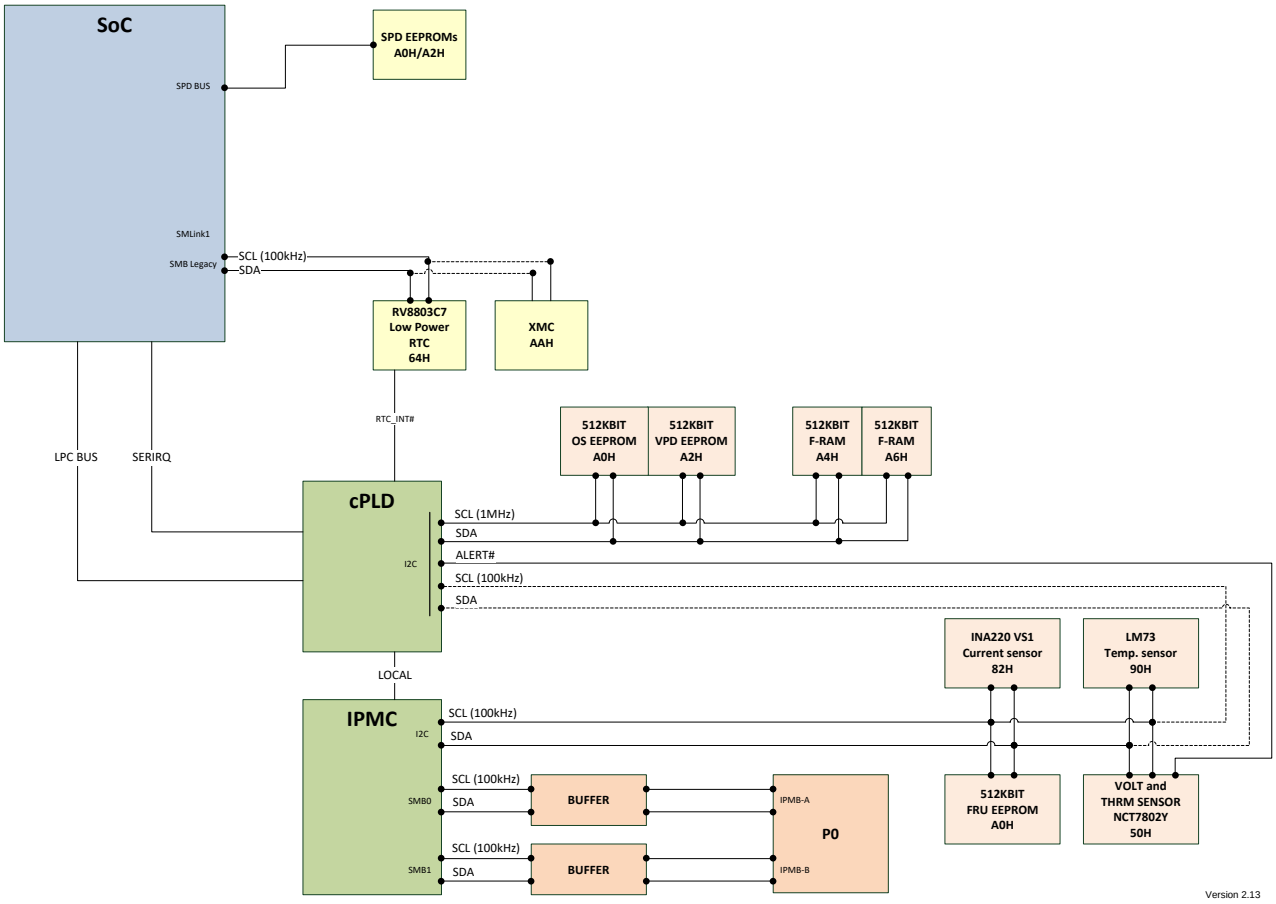


Table 24: I2C device list

Device	Size	Bus	SMBUS BASE ADDRESS (7bit)	FEATURES
M24C04	4-Kbit	SPD Bus	A0H	DDR SPD eeprom – Bank0
M24C04	4-Kbit	SPD Bus	A2H	DDR SPD eeprom – Bank1
RV-8803-C7	-	SMB Legacy	64H	External RTC Device
XMC eeprom	-	SMB Legacy	AAH	XMC slot SMBus **– Not applicable to VX307H**
INA220	-	I2C IPMC (cPLD)	82H	VS1 Current Monitoring
LM73	-	I2C IPMC (cPLD)	90H	Temperature sensor
NCT7802Y	-	I2C IPMC (cPLD)	50H	Voltage and Temperature sensor
AT24C512C	512-Kbit	I2C IPMC (cPLD)	A0H	IPMI – FRU data
AT24CM01	512-Kbit	cPLD	A2H	Vital Product Data
AT24CM01	512-Kbit	cPLD	A0H	User eeprom
FM24V10	1-Mbit	cPLD	A4H/A6H	User data

3.3. EEPROM Mapping

On-board EEPROM mapping are in the following tables

Table 25: VPD and OS EEPROM mapping

VPD EEPROM I2c @ (A0H) Global Mapping

EEPROM addresses	Description
0x0000 – 0x100	Board Vital Product Data
0x100 - 0x300	Reserved (Optional VPD - MAC address …)
0x300 - 0x7FFF	Free Area
0x8000 - 0xFFFF	Free Area (64kB eeprom size)

OS EEPROM I2c @ (A2H) Global Mapping

EEPROM addresses	Description
0x0000 – 0x1400	Free for OS (used by Linux BSP)
0x1400-0x2000	PBIT Reserved (Factory Test Information)
0x2000- 0x3000	PBIT Test List/Test/Rescue list …
0x3000-0x4000	Reserved PBIT
0x4000- 0x5000	PBIT System Test Config and Recorded Information
0x5000-0x6000	Reserved PBIT
0x60F0 -0x612F	CPLD Power ON Config Data
0x6130-0x7FFF	Free area
0x8000-0xFFFF	Free area (64kB eeprom size)

3.4. Main CPLD Features

The CPLD manages the following features:

- Power-on/off control
- Reset control
- LPC interface to processor
- KCS interface to IPMC
- LEDs control
- Serial lines multiplexer
- Serial VPD and user memories
- User and system GPIOs
- Internal registers dedicated to system management

› cPLD Register

- cPLD registers are accessible from the CPU.
- On non-IPMI boards, some of these registers are also accessible from the backplane I2C buses for board control and monitoring.
- Under OS, these registers are managed by some cPLD drivers and tools, so to use the cPLD features under OS, please see the related BSP documentation.
- The BSP sources are also a good start to port the drivers and tools to some other OS.
- In some cases, a full description of the cPLD registers may be needed. Please contact Kontron.

3.5. Serial Lines Additional Modes

› Serial ports Location
Refer to section 4.1.1 and 7 for serial interfaces available on the front panel.
Refer to section 4.3 for serial interfaces available on the rear panel (VPX P1 connector).

› Protocol selection
MP01 port on VPX P1: default mode is EIA-232 protocol. Mode can be set to LVCMOS through BIOS settings
MP02 port on VPX P1: default mode is EIA-232 protocol.

› Additional feature
When EIA-422/485 is selected, the transmit can be enabled/disabled through a bit in a CPLD register (legacy method), or by the RTS signal of the UART, or also automatically using the CPLD "auto-TX" feature (when the UART sends some data)

3.6. User GPIOs and GDISCRETE1

3.6.1. GPIOs

The VX307H variants offers up to 2 GPIOs managed by the CPLD depending on the product variant. Refer to section related to VPX pin assignments for the exact location and availability. Refer also to the Software Release Notes for further details about the GPIO driver.

- Up to one GPIO is available on VPX P1 connector
- One GPIO with dual purpose GPIO/Maskable_Reset is available on VPX P1 connector

The CPLD features LVCMOS33 cells (0-3V3) with 8mA drive strength (sink or source), a clamp diode which is not 5V tolerant and a 250 mV hysteresis. The CPLD does not implement any internal pull-up or pull-down resistor.

On the VX307H board, a pull-up of 47 kOhms is connected to GPIOs.

The GPIOs share the same interrupt in the CPLD.

3.6.2. GDISCRETE1

GDISCRETE1 is a bussed open-collector GPIO defined by OpenVPX VITA 65 and available on P1. See section “VPX P1 Connector” for detailed pinout.

It is handled by the CPLD and buffered by a SN74LVC1G125 buffer wired as an Open Collector to meet the electrical characteristics defined in VITA 65.

It has a dedicated interrupt in the CPLD.

3.7. Reset

Table 26: Reset Management Table

RESET SOURCE	RESET ACTION	RESET CONTROL	RESET STATUS	NOTE
Front panel push button	Platform reset	Front panel push button	I2C_BOARD_STATUS @0x72	Reset propagation options and masks available in cPLD registers
VPX Sysreset	Platform reset	VPX P0 / Row B/ Wafer 4	I2C_BOARD_STATUS @0x72	See VPX Vita46.0 standard Reset propagation and mask options available in cPLD registers
VPX maskable reset	Platform reset	VPX P1 / Row G/ Wafer 15	I2C_BOARD_STATUS @0x72	See VPX Vita46.0 standard
cPLD watchdog reset	Platform reset	Refer to the Fedora Remix Release note	I2C_BOARD_STATUS @0x72	Refer to the Fedora Remix Release note
Processor watchdog reset	Platform reset	Refer to the Intel SoC watchdog feature and control registers	Refer to the Intel SoC watchdog feature and control registers	Refer to the Intel SoC watchdog feature and control registers
cPLD software reset	Platform reset	I2C_BOARD_CONTROL @0x73	I2C_BOARD_STATUS @0x72	Refer to the cPLD control/status registers

3.8. NVMRO

NVMRO is defined by the VITA 46.0 standard.
VX307H is compliant with Standard for SOSA™ Reference Architecture, Edition 1 / Rule 6.4.2-4.

Please contact Kontron support for more information.

Memory	Part Ref	Size	Fully Write protected when NVMRO is asserted	Write protection Level	Possible HW Write Protections	Writable During Operation With HW Write protection disabled	Function	Existing Writing tool If HW Write protection is disabled	Proposed sanitization procedure
MP2978, MP2976 Power Supplies	MP2978GU-6903-Z MP2976GU-6903-Z Monolithic Power Systems	Proprietary	No	NA	None. No User access.	No	VR configuration	None	No user access. Sanitization not required.
SDRAM EEPROM	M24C04-RMC6TG ST MICROELECTRONICS	4 Kbit	Yes	VPD	NVMRO MicroSwitch SW1[2] MEM_PROTECT Register (see product manuals)	Yes	SDRAM size and timing information storage	Kontron BIOS/kspd	Turn off WP and erase data. **The product will no longer work after sanitization.**
VPD EEPROM	AT24CM01-SSHM-T MICROCHIP	512Kbit	Yes	VPD		Yes	Region1: Storage of board configuration data Region2: user data	Kontron BIOS/BSP commands	Turn off WP and erase data **The product will no longer work after sanitization**
i225 Flash Memory	W25Q16JVUXIM Winbond	16 Mbit	Yes	VPD		Yes	Config and Ethernet controller address	**Intel Lanconf/Eeupdate**	Turn off WP and erase data The product will behave badly after sanitization.
i210 Flash Memory	W25Q16JVUXIM Winbond	16 Mbit	Yes	VPD		Yes	Config and Ethernet controller address	**Intel Lanconf/Eeupdate**	Turn off WP and erase data The product will behave badly after sanitization.
FLASH in cPLD	LCMXO2-4000HC-4BG256ITR LATTICE	256Kbit	Yes	USER	NVMRO MicroSwitch SW1[3] MEM_PROTECT Register (see product manuals)	Yes	Storage for cPLD configuration data	Kontron BIOS/kpld	Turn off WP and erase data **The product will no longer work after sanitization**.
FRAM	FM24V10-GTR CYPRESS	1 Mbit	Yes	USER		Yes	Storage of user data	Kontron PBIT/BSP commands	Turn off the WP and erase data using the API and driver provided in the Linux BSP.
IPMC BOOT FLASH	W25Q16JVUXIM Winbond	16 Mbit	Yes	USER		Yes	IPMC boot flash device	Kontron BIOS/BSP commands	Turn off WP and overwrite data with the BIOS/kflash command. **The product will no longer work after sanitization**.
BOOT FLASH	MT25QL512ABB1EW9-0SIT Micron	2x 512 Mbit	**No**	USER	**Full HW protection is not possible because Intel proprietary due to ME writes. No direct user access allowed when operating.** NVMRO MicroSwitch SW1[3] MEM_PROTECT Register (see product manuals)	Yes	Boot and Rescue Boot Flash devices	Kontron BIOS/BSP commands	Turn off WP and overwrite data with the BIOS/BSP command. **The product will no longer work after sanitization**.
SYS EEPROM	AT24CM01-SSHM-T MICROCHIP	512Kbit	Yes	SYSTEM	NVMRO MEM_PROTECT Register (see product manuals)	Yes	Region1: Storage of board configuration data Region2: user data	Kontron BIOS/BSP commands	Turn off WP and erase data
FRU EEPROM	AT24C512C-MAHM-T MICROCHIP	512Kbit	Yes	SYSTEM		Yes	Region1: Storage of board configuration data Region2: user data	Kontron BIOS/BSP commands	Turn off WP and erase data **The product will no longer work after sanitization**
TPM	ST33KTPM2X32CKE3 STMicroelectronics	-	No	NA	No.	Yes	Storage of Key	-	-
IPMC	LPC2368FET100,518	128kB	No	NA	No.	Yes	Storage of IPMC execution source code	Kontron BIOS/BSP commands	Erase data **The product will no longer work after sanitization**

Memory	Part Ref	Size	Fully Write protected when NVMRO is asserted	Write protection Level	Possible HW Write Protections	Writable During Operation With HW Write protection disabled	Function	Existing Writing tool If HW Write protection is disabled	Proposed sanitization procedure
M.2 module (1)	VSFBN4CI240G-V11-H or equivalent (M2S1 slot) VIRTIUM	240 GBytes	**No**	USER	No WP feature for this Innodisk module.	Yes	Storage of user data	Kontron BIOS/PBIT/BSP commands	**According to the sanitization procedure defined by the Virtium manufacturer.** The product may behave badly after sanitization.

(1) Only related to VX307H part with letter Q at the end of part number, example : VX307H-RC316H-000N000V1Q

3.9. IPMI Option

The VX307H embeds an IPMI controller so much so that the VX307H is considered as a FRU as per VITA 46.11. The IPMI controller is accessible through an IPMB bus or through a host Keyboard Controller Style (KCS) interface.

The IPMC manages the following features:

- Local environmental control/monitoring
- I2C interfaces to I2C bus IPMB A/B (rear P0)
- KCS interface to CPLD
- Serial FRU memory
- IPMI watchdog
- System Event Log (SEL)
- Sensor Device functionality

For further detail about IPMI firmware, refer to VX307H IPMI Firmware Release Note.

› VPX IPMB I2C interfaces

VX307H implements two I2C buses connected to P0 VPX connector. See section 4.3 for the detailed P0 pin assignments:

- IPMB A (I2C0) CLK on pin P0-B5, DATA on pin P0-A5
- IPMB B (I2C1): CLK on pin P0-G4, DATA on pin P0- F4

› IPMI commands available

The VX307H IPMI firmware supports all the Mandatory IPMC Tier-1 and Tier-2 commands. See the exhaustive list of IPMI supported commands in the VX307H IPMI Firmware Release Note.

3.10. Graphic Option

Not available on the VX307H variant.

3.11. Security Solution

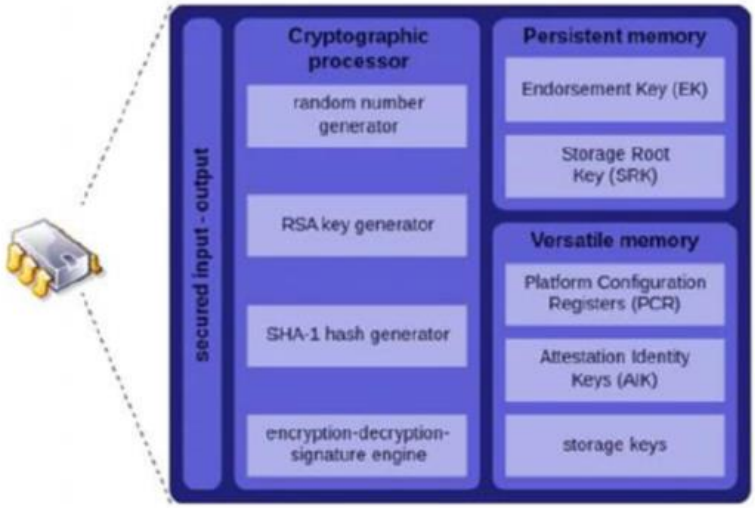
The VX307H answers digital security requirements with hardware enforced root of trust (secure elements). The VX307H supports SEC-Line computer security offering:

- **AUTHENTICATION WITH TPM**: Secure network protocols
- **Secure Boot**：Hardware and Software Secure Boot solutions
- **Secure SSD**：Natively AES-256 encrypted SSD

If needed customers can customize the solution to meet specific needs. For more information, contact Kontron Support.

3.12. Trusted Platform Module (TPM 2.0)

The VX307H is compliant with TPM 2.0 standard. A Trusted Platform Module (TPM) stores encryption keys specific to the host system for hardware authentication. The term TPM refers to the set of specifications applicable to TPM chips.



4. Physical IO

4.1. Front Panel

Figure 21: RA variant - Front Panel Interfaces

Figure 22: RC3 variant - Front Panel Interfaces – FB-VX3-0010 tooling option not equipped

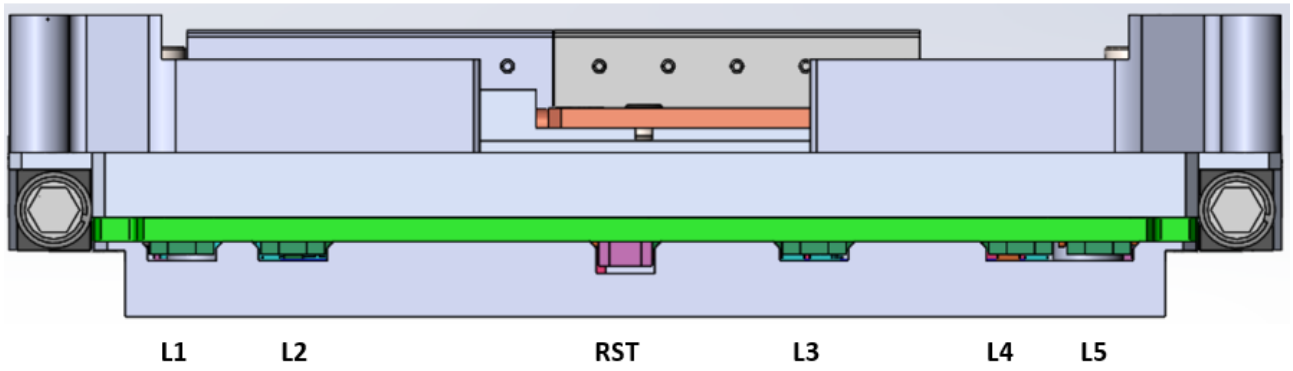


Table 27: Front Panel – I/Os interfaces

FUNCTION	DESCRIPTION	SEE ALSO
RST	Reset push button	Front Interfaces
Lx	LED indicators reporting the board CPU health status and activity	Section 4.4 for LEDs Description
SERIAL	RJ12 serial port	Only Available if FB-VX3-0010 option is equipped. Refer to section 7 for detailed information
USB	USB2.0 port	
ETH	RJ45 Ethernet port	

The front panel push button must be handled with care. Use a non-metallic and blunt tool with a rounded tip (tip diameter must be roughly equal to the front panel button surface)

4.1.1. SERIAL Interface when FB-VX3-0010 tooling is equipped

When equipped, the FB-VX3-0010 tooling option provides one serial maintenance, one USB2.0 and one Ethernet RJ45 / 1000Base-T ports on the front panel.

Defaults setting Serial maintenance port configuration: EIA-232 port connected to the processor COM1 Port, simplified serial line mode Rx/Tx only, 115200 bauds.

› Pin Assignment

Table 28: Serial Connector Pin Assignment

PIN	SIGNAL
1	COM2 TXD
2	Shell
3	COM1 TXD
4	COM1 RXD
5	GND
6	COM2 RXD

Figure 23: Serial Connector

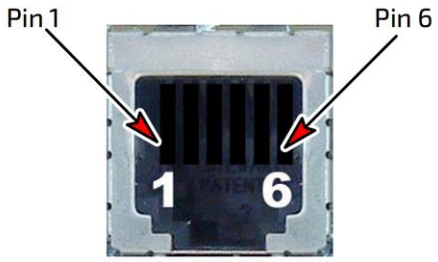


Table 29: Serial Connector Signal Description

MNEMONIC	DESCRIPTION
COM1 TXD/RXD	COM1 serial line
COM2 TXD/RXD	COM2 serial line
GND	Ground
Shell	Chassis Ground

› Serial Cable Designation

The Serial cable shall be shielded and shall provide a good shielding continuity between each end. The Serial cable length should not exceed 10 m.

Serial cable is a RJ-12 (6 pin, 6 conductors). A RJ-12 to DB9 male or DB9 female adapter is available from multiple sources, such as:

- Kontron Order Code KIT-RJ12DB9
- Triangle Cable http://www.trianglecables.com/db9m-rj12.html

Table 30: Serial Cable Pin Assignment

DB9 A Pin Connector	Signal	RJ-12 Pin Connector
-	-	1
2	TXD	3
3	RXD	4
-	-	6
5	GND	5

Figure 24: Serial Cable

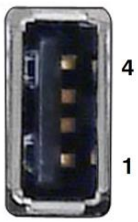
4.1.2. USB 2.0 Interface when FB-VX3-0010 tooling is equipped

USB cable shall be compliant to Universal Serial Bus Specification, Revision 2.0.
This USB cable shall have double shielding.
The USB cable length should not exceed 3 m.

Table 31: USB 2.0 Connector Pin Assignment

PIN	SIGNAL	function	I/O
1	VCC (+5V Protected)	VCC	O
2	USB_D-	Differential USB-	I/O
3	USB_D+	Differential USB+	I/O
4	GND	GND	--

Figure 25: USB 2.0 Connector



USB

4.1.3. Gigabit Ethernet Connector when FB-VX3-0010 tooling is equipped

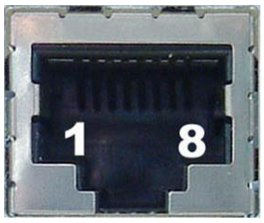
The Ethernet cable shall be CAT6 compliant.
This Ethernet cable shall be S/FTP type at least (Shielded Foiled Twisted Pair), providing shielding continuity between each end.
The Ethernet transmission should operate using a CAT6 cable with a maximum length of 100 m.

The Ethernet connector is available as RJ-45 connectors with tab down. The interface provides automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

Table 32: Gigabit Ethernet Connector Pin Assignment

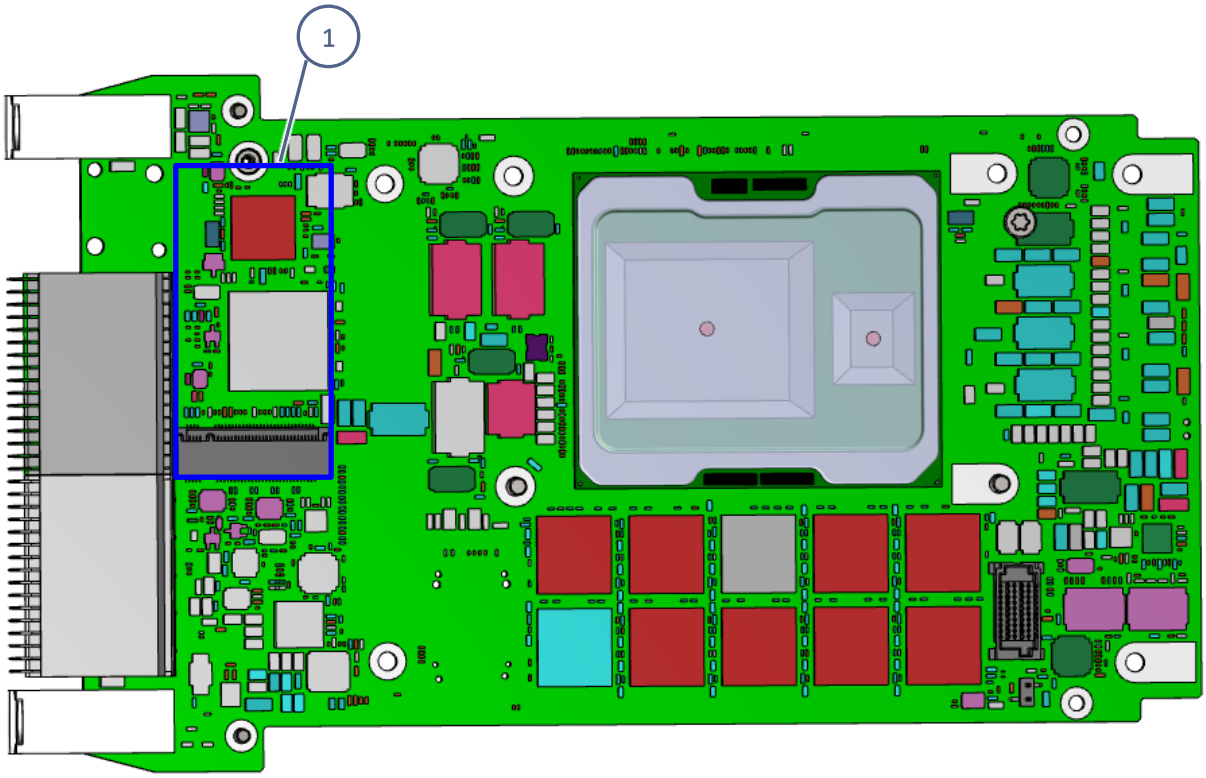
pin	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-		I/O	BI_DC+
5	-	-	-		I/O	BI_DC-
6	I	RX-	I	RX-	I/O	BI_DB-
7	-	-	-		I/O	BI_DD+
8	-	-	-		I/O	BI_DD-
Shell	Chassis Ground					

Figure 26: RJ45 Ethernet Connector



4.2. User/On-Board connectors

Figure 27: User/Onboard Connectors



1. M2S1 slot (M.2 2242-M)
2. M2S2 slot (M.2 2242-M)

4.2.1. Optional - XMC J15 Connector Pin Assignments

Not available on VX307H variants.

4.2.2. Optional - XMC J16 Connector Pin Assignments

Not available on VX307H variants.

4.2.3. Optional – Top/Bottom M.2 Connector Pin Assignments

The M.2 sockets are used to connect M.2 modules, key M for storage.

PCIe mode is the default product mode.

The M.2 sockets support only 2242 form factor.

SATA interface can be used depending on the product options.
Refer to VX307H Software release notes. Ask Kontron.

The top M.2 lot is named M2S1. The bottom M.2 lot is named M2S2.

Table 33: M.2 socket connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	3V3
3	GND	4	3V3
5	NC	6	NC
7	NC	8	NC
9	GND	10	DAS/DSS#LED1#
11	NC	12	3V3
13	NC	14	3V3
15	GND	16	3V3
17	NC	18	3V3
19	NC	20	NC
21	GND	22	NC
23	NC	24	NC
25	NC	26	NC
27	GND	28	NC
29	PER1-	30	NC
31	PER1+	32	NC
33	GND	34	NC
35	PET1-	36	NC
37	PET1+	38	DEVSLP
39	GND	40	NC
41	PER0- (SATA-B+)	42	NC
43	PER0+ (SATA-B-)	44	NC
45	GND_45	46	NC
47	PET0- (SATA-A-)	48	NC
49	PET0+ (SATA-A+)	50	PERST#
51	GND_51	52	CLKREQ#
53	REFCLK_N	54	PEWAKE#
55	REFCLK_P	56	NC
57	GND	58	**WP#**
59	CONNECTOR_KEY	60	CONNECTOR_KEY
61	CONNECTOR_KEY	62	CONNECTOR_KEY
63	CONNECTOR_KEY	64	CONNECTOR_KEY
65	CONNECTOR_KEY	66	CONNECTOR_KEY
67	NC	68	SUSCLK
69	PEDET	70	3V3_70
71	GND_71	72	3V3_72
73	GND_73	74	3V3_74
75	GND_75		

Table 34: M.2 Module Socket Signal Description

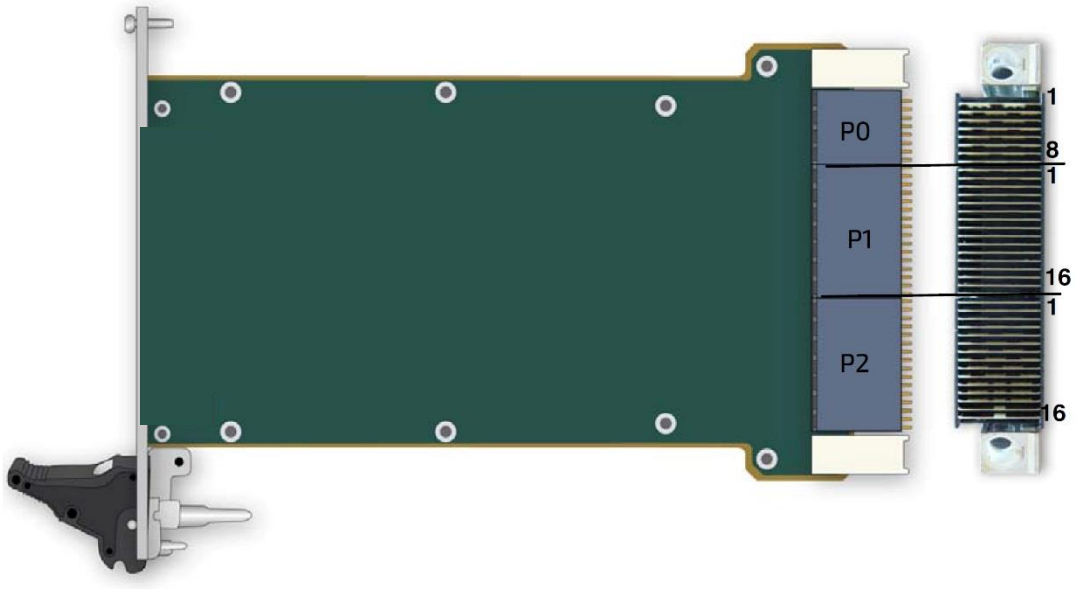
MNEMONIC	DIRECTIO	SIGNAL DEFINITION
3.3V	O	I
GND	-	Logic ground.
LED1# / DAS_DSS#	I	- PCI Express: LED_1# indicator as per PCI Express M.2 specification. - SATA: Device Activity Signal /Disable Staggered Spinup as per SATA 3.2. DAS is not connected to a LED (which is the main purpose of this signal) and DSS is not used since the devices are SSD and not hard drives (no spinup). Signal connected to dedicated CPLD
PEDET	I	PEDET (PCI Express Detect) as per PCI Express M.2 specification is driven low by SATA modules and high-Z by PCI Express modules (seen as a logic 1 due to on-board pull-up resistor). This signal is connected to a dedicated CPLD pin.
PERn+/- (SATA-B+/-)	I	- PCI Express: Receive differential pair as per PCI Express M.2 & PCI Express 3.0 specifications. - SATA: Receive differential pair as per SATA 3.2.
PERST#	O	- PCI Express: PCI Express PERST# as per PCI Express M.2 specification, handled by CPLD.
PETn+/- (SATA-A+/-)	O	- PCI Express: Transmit differential pair as per PCI Express M.2 & PCI Express 3.0 specifications. - SATA: Transmit differential pair as per SATA 3.2.
PEWAKE#	I/O	- PCI Express: Open drain WAKE# signal as per PCI Express M.2.
REFCLKP/N	O	- PCI Express: PCIe 100MHz clock as per PCI Express M.2.
SUSCLK	O	Suspend Clock for low power mode handling as per PCI Express M.2 specification (32.768 kHz, duty cycle between 30% and 70%, 200ppm). Connected to SoC SUSCLK_GPIO62.
CLKREQ#	I/O	- PCI Express: Open drain reference clock request signal as per PCI Express M.2.
WP#	I (open drain)	SSD write protect input. Expected SSD behavior when Write-Protect (WP) signal is used: When WP is low, any writes by the host will be aborted by the SSD (any write command not acknowledged by the SSD will be aborted). When WP# is high or if unused by the SSD module: no write protection.

4.3. VPX Rear Connectors

The complete 3U VPX connectors configuration comprises three connectors named P0 to P2:

- P0: 8-wafer 7-row connector.
- P1 - P2: 16-wafer 7-row differential connectors.

Figure 28: VPX Connectors



4.3.1. VX307H - VPX P0 Connector

Table 35: VX307H - VPX Connector P0 Wafer Assignment

P0	G	F	E	D	C	B	A
1	VS1 (12V)	VS1 (12V)	VS1 (12V)	N.C.	NC	NC	NC
2	VS1 (12V)	VS1 (12V)	VS1 (12V)	N.C.	NC	NC	NC
3	NC	NC	NC	N.C.	NC	NC	NC
4	IPMB_B CLK	IPMB_B DAT	GND	-12V_AUX	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3V3_AUX (optional)	GND	IPMB_A CLK	IPMB_A DAT
6	GA3*	GA2*	GND	NC	GND	GA1*	GA0*
7	TCK	GND	TDO	TDI	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND
CASE	GND						

* signal active when low

REF_CLK-/+: 25MHz and 100MHz clock manufacturing options are available. Contact Kontron. Default is the 25MHz standard option.

Table 36: VX307H - VPX Connector P0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
+12V	+12 Volts DC power (VS1 VPX supply). NC (+12V) pins are not connected (VS2 VPX supply)
-12V_AUX	-12 Volts auxiliary power. Only used to supply XMC. **Not applicable to VX307H**
3V3_AUX	+3.3 Volts auxiliary power. Not required because it generate internally is 3V3_AUX power rail is not present on the backplane.
NVMRO	Non-Volatile Memory Read Only signal as per SOSA standards.
GAi	Geographical address pins
GAP	Geographical address parity
GND	Ground
IPMB A	I2C Bus 0
IPMB B	I2C Bus 1
REF_CLK+/-	The Reference Clock is a bussed differential pair. Output if the VX307H is plugged in the system controller slot, input otherwise. It enables the entire system to synchronize to a common time reference if desired. Counter/timer in the CPLD can use this clock
AUX_CLK+/-	1 PPS (one pulse per second) clock input. Can be programmed as an output on system controller slot. Can be used to phase the CPLD timer/counter clocked by REF_CLK+/-.
SYSRESET*	System Reset. Input and open collector output.
TCK, TMS, TDO, TDI, TRST*	VPX JTAG interface connected

4.3.2. VX307H - VPX P1 Connector

Table 37: VX307H - VPX Connector P1 Wafer Assignment

P1	G	F	E	D	C	B	A
1	Gdiscrete 1	GND	DP_ETH L00 TX-	DP_ETH L00 TX+	GND	DP_ETH L00 RX-	DP_ETH L00 RX+
2	GND	DP_ETH L01 TX-	DP_ETH L01 TX+	GND	DP_ETH L1 RX-	DP_ETH L01 RX+	GND
3	VBAT	GND	DP_ETH L2 TX-	DP_ETH L02 TX+	GND	DP_ETH L02 RX-	DP_ETH L02 RX+
4	GND	DP_ETH L3 TX-	DP_ETH L3 TX+	GND	DP-ETH L3-RX-	DP_ETH L03 RX+	GND
5	SYS_CON*	GND	ETH1 TX-	ETH1 TX+	GND	ETH1 RX-	ETH1 RX+
6	GND	CLK1-	CLK1+	GND	MP01 TXD	MP01 RXD	GND
7	GND	GND	GND	GND	GND	GND	GND
8	GND	ETH0 TX-	ETH0 TX+	GND	ETH0 RX-	ETH0 RX+	GND
9	MP02 TXD	GND	EP_PCIe L00 TX-	EP_PCIe L00 TX+	GND	EP_PCIe L00 RX-	EP_PCIe L00 RX+
10	GND	EP_PCIe L01 TX-	EP_PCIe L01 TX+	GND	EP_PCIe L01 RX-	EP_PCIe L01 RX+	GND
11	MP02 RXD	GND	EP_PCIe L02 TX-	EP_PCIe L02 TX+	GND	EP_PCIe L02 RX-	EP_PCIe L02 RX+
12	GND	EP_PCIe L03 TX-	EP_PCIe L03 TX+	GND	EP_PCIe L03 RX-	EP_PCIe L03 RX+	GND
13	GPIO1	GND	EP_PCIe L04 TX-	EP_PCIe L04 TX+	GND	EP_PCIe L04 RX-	EP_PCIe L04 RX+
14	GND	EP_PCIe L05 TX-	EP_PCIe L05 TX+	GND	EP_PCIe L05 RX-	EP_PCIe L05 RX+	GND
15	Msk RST	GND	EP_PCIe L06 TX-	EP_PCIe L06 TX+	GND	EP_PCIe L06 RX-	EP_PCIe L06 RX+
16	GND	EP_PCIe L07 TX-	EP_PCIe L07 TX+	GND	EP_PCIe L07 RX-	EP_PCIe L07 RX+	GND
CASE	GND						

* signal active when low

The ordered product manufacturing options may alter the VPX P1 pin assignment. Contact Kontron.
MP01 Manufacturing options: product can be ordered with MP01 compatible with LVCMOS or TIA-232 interfaces (exclusive)

Table 38: VX307H - VPX Connector P1 Signal Definition

MNEMONIC	SIGNAL DEFINITION
DP_ETH	100/40GBase-KR4 Ethernet link (Auto negotiation mode only)
EP_PCIe	Expansion plane PCIe from Lane 0 to Lane 7
ETH0/ETH1	SerDes Ethernet links. Refer to the ordering information for more information about the available Ethernet factory options
GDISCRETE1	Open VPX GDISCRETE1 signal
GPIO1*	General Purpose I/O 1 (handled by the CPLD)
Maskable Reset* or GPIO2	Reset input or Optional general purpose I/O (handled by CPLD) (may be left unconnected if not used).
GND	Ground
SYS_CON	System Controller Slot Indication
VBAT	Source for RTC backup voltage, from the VPX 3.3V_AUX rail or from the VPX P1 / G3 VBAT rail
MP01	Maintenance port : serial Lines EIA-232 or 3V3 signal leveling
MP02	Maintenance port : serial Lines EIA-232

4.3.3. VX307H - VPX P2 Connector

Table 39: VX307H - VPX Connector P2 Wafer Assignment

P2	G	F	E	D	C	B	A
1	NC	GND	EP_PCIe L08 TX-	EP_PCIe L08 TX+	GND	EP_PCIe L08 RX-	EP_PCIe L08 RX+
2	GND	EP_PCIe L09 TX-	EP_PCIe L09 TX+	GND	EP_PCIe L09 RX-	EP_PCIe L09 RX+	GND
3	NC	GND	EP_PCIe L10 TX-	EP_PCIe L10 TX+	GND	EP_PCIe L10 RX-	EP_PCIe L10 RX+
4	GND	EP_PCIe L11 TX-	EP_PCIe L11 TX+	GND	EP_PCIe L11 RX-	EP_PCIe L11 RX+	GND
5	NC	GND	EP_PCIe L12 TX-	EP_PCIe L12 TX+	GND	EP_PCIe L12 RX-	EP_PCIe L12 RX+
6	GND	EP_PCIe L13 TX-	EP_PCIe L13 TX+	GND	EP_PCIe L13 RX-	EP_PCIe L13 RX+	GND
7	NC	GND	EP_PCIe L14 TX-	EP_PCIe L14 TX+	GND	EP_PCIe L14 RX-	EP_PCIe L14 RX+
8	GND	EP_PCIe L15 TX-	EP_PCIe L15 TX+	GND	EP_PCIe L15 RX-	EP_PCIe L15 RX+	GND
9	VITA66 option	GND	VITA66 option	VITA66 option	GND	VITA66 option	VITA66 option
10	GND	VITA66 option	VITA66 option	GND	VITA66 option	VITA66 option	GND
11	VITA66 option	GND	VITA66 option	VITA66 option	GND	VITA66 option	VITA66 option
12	GND	VITA66 option	VITA66 option	GND	VITA66 option	VITA66 option	GND
13	VITA66 option	GND	VITA66 option	VITA66 option	GND	VITA66 option	VITA66 option
14	GND	VITA66 option	VITA66 option	GND	VITA66 option	VITA66 option	GND
15	VITA66 option	GND	VITA66 option	VITA66 option	GND	VITA66 option	VITA66 option
16	GND	VITA66 option	VITA66 option	GND	VITA66 option	VITA66 option	GND
CASE	GND						

* signal active when low

The ordered product manufacturing options may alter the VPX P2 pin assignment. Contact Kontron.

Table 40: VX307H - VPX Connector P2 Signal Definition

MNEMONIC	SIGNAL DEFINITION
EP_PCIe	Expansion plane PCIe from Lane 8 to Lane 15
VITA66 option	Reserved for VITA 66 manufacturing options – Contact Kontron
GND	Ground

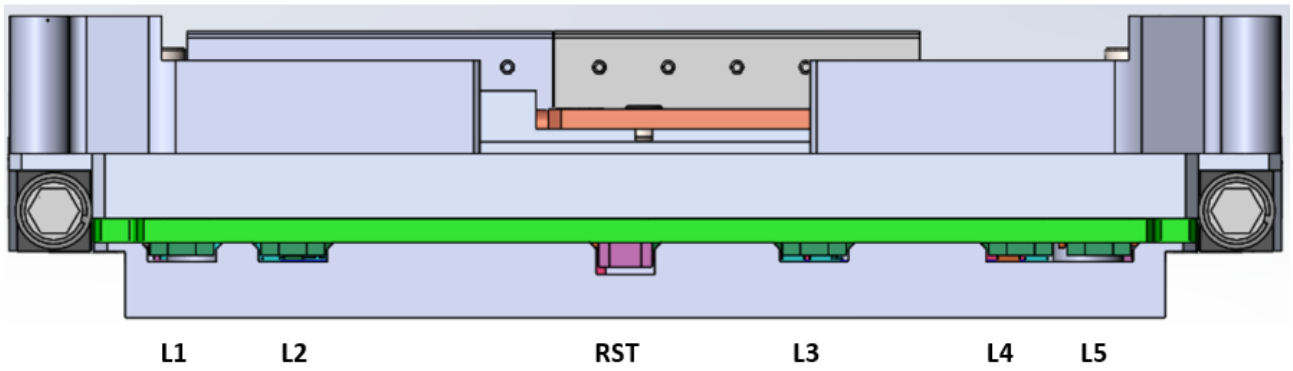
4.4. LEDs

4.4.1. LEDs Location

There are five bicolor LEDs (Red/Green) on the front panel of the VX307H.

Figure 29: RA variant - Front Panel Interfaces

Figure 30: RC variant - Front panel LEDs



4.4.2. LEDs Activity – Normal Mode

When LED1 is red, the meaning of the other LEDs is changed. See Section "Power Sequencer"/"Error codes".
If “debug mode” is active, please refer to Section "Power Sequencer/Power states"
For "user mode" on LED3,LED4 and LED5, see Section "CPLD Registers"

During normal operation (not configured in "user mode", no fatal error, not in “debug mode”), their state is as follows:

Table 41: LEDs Description – Normal Mode

LED1	
OFF	Board fully off
GREEN	Board running. Blinking slow (@0.5Hz) when off/sleeping and no reset source is active.
ORANGE	Board reset asserted. Blinking slow (@0.5Hz) when off/sleeping and a reset source is active
RED	Fatal error. See chapter "Power Sequencer"/"Error codes"

LED2	
OFF	Board off or sleeping
GREEN	Normal operation. Blinking on CPLD activity (LPC or I2C0/1 slave)
ORANGE	Same than green, but when FACTORY_MODE switch is ON
RED	Watchdog timeout

LED3	
OFF	
GREEN	M2S1/M2S2 activity (off when no activity)
ORANGE	-
RED	Solid “on” when temperature alert (see reg @0x74 bit 7); Otherwise blinking slow (@0.5Hz) if SOC CATERR# is asserted

LED4	
OFF	
GREEN	i225 interface with link up, blinking on activity
ORANGE	-
RED	PBIT error (through register POST_STATUS @ 0x02)

LED5	
OFF	
GREEN	-
ORANGE	-
RED	-

4.4.3. LEDs - Power States

When in "debug mode", the LEDs no more have their operational meaning, but LED1 is blinking green fast (@2Hz), and LED2, LED3, LED4, LED5 are displaying the current power state as follows :

Table 24: LEDs Description – Debug Mode / Error codes

LEDs In "DEBUG MODE"					
Power state number	**Name**	**LED2**	**LED3**	**LED4**	**LED5**
0	POR_ST	OFF	OFF	OFF	OFF
1	V3V3_S5_ST	GREEN	OFF	OFF	OFF
2	V1V8_S5_ST	OFF	GREEN	OFF	OFF
3	VNN_S5_ST	GREEN	GREEN	OFF	OFF
4	V1V05_S5_ST	OFF	OFF	GREEN	OFF
5	V1V8_NACDLY_ST	GREEN	OFF	GREEN	OFF
6	RSMRST	OFF	GREEN	GREEN	OFF
7	WAITBPPWR_ST	GREEN	GREEN	GREEN	OFF
8	PWRBTN_ST	OFF	OFF	OFF	GREEN
9	WAITS4_ST	GREEN	OFF	OFF	GREEN
10	WAITS3_ST	OFF	GREEN	OFF	GREEN
11	V3V3_ST	GREEN	GREEN	OFF	GREEN
12	V2V5DDR_ST	OFF	OFF	GREEN	GREEN
13	V1V2DDR_ST	GREEN	OFF	GREEN	GREEN
14	V1V8PCIE_ST	OFF	GREEN	GREEN	GREEN
15	VCCIN_ST	GREEN	GREEN	GREEN	GREEN
16	FORCEOFF_ST	OFF	OFF	OFF	RED
23	RUNNING_ST	GREEN	GREEN	GREEN	RED
31	ERROR_ST	According to error code (see below)	According to error code (see below)	According to error code (see below)	According to error code (see below)

4.4.4. LEDs – Error Codes

In case of error, the error code is also reported on front LEDs as follows :

ERROR CODES ON LEDs						
Error code number	**Name**	**LED1**	**LED2**	**LED3**	**LED4**	**LED5**
0	ERR_NO_ERROR	-	-	-	-	-
1	ERR_3V3_S5	RED	RED	OFF	OFF	OFF
2	ERR_1V8_S5	RED	OFF	RED	OFF	OFF
3	ERR_VNN_PCH	RED	RED	RED	OFF	OFF
4	ERR_VNN_NAC	RED	OFF	OFF	RED	OFF
5	ERR_1V05_S5	RED	RED	OFF	RED	OFF
6	ERR_1V8_NACDLY	RED	OFF	RED	RED	OFF
7	ERR_3V3	RED	RED	RED	RED	OFF
8	ERR_5V0	RED	OFF	OFF	OFF	RED
9	ERR_2V5DDR	RED	RED	OFF	OFF	RED
10	ERR_1V2DDR	RED	OFF	RED	OFF	RED
11	ERR_VTTDDR	RED	RED	RED	OFF	RED
12	ERR_PECI_CRIT	RED	OFF	OFF	RED	RED
13	ERR_THERM_PROT	RED	RED	OFF	RED	RED
14	ERR_THERMTRIP	RED	OFF	RED	RED	RED
15	ERR_CATERR	RED	RED	RED	RED	RED
16	ERR_BP_UV_PWRGD	RED	OFF	OFF	OFF	GREEN
17	ERR_BP_OV_PWRGD	RED	RED	OFF	OFF	GREEN
18	ERR_VCCIN	RED	OFF	RED	OFF	GREEN
19	ERR_1V8PCIE	RED	RED	RED	OFF	GREEN
20	ERR_PWR_INALRT	RED	OFF	OFF	RED	GREEN
21	ERR_PWR_CATFLT	RED	RED	OFF	RED	GREEN
22		RED	OFF	RED	RED	GREEN
23		RED	RED	RED	RED	GREEN

5. Power and Thermal Specifications

5.1. Power considerations

The considerations presented in the ensuing sections must be taken into account by system integrators when specifying the VX307H system environment.

5.1.1. Backplane

Backplanes to be used with the VX307H must be adequately specified and comply with VITA 65.0. The backplane must provide optimal power distribution for the VPX VS1 and 3V3 AUX power inputs.
Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided

5.1.2. Power Supplies

Power supplies for the VX307H must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires. Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for die resistance variations.

› Tolerance

The following table provides information regarding the required characteristics for each board input voltage.

Table 42: VPX Input Voltage Tolerance

POWER RAIL	NOMINAL VALUE	TOLERANCE*	MAX RIPPLE (p-p)	REMARKS
+12V VPX VS1	+12VDC	+/-5%	50mV over a range of 0-20MHz	Main voltage
+3.3V VPX VS2	*+3.3VDC*	*3.25V min 3.45V max*	*50mV over a range of 0-20MHz*	*Not used*
+5V VPX VS3	*+5VDC*	*+5%/-2.5%*	*50mV over a range of 0-20MHz*	*Not used*
VPX 3.3V AUX	+3.3VDC	+/-5%	50mV over a range of 0-20MHz	Optional
GND	Ground, not directly connected to potential earth (PE)			

(*)Tolerance values include ripple.

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

› Rise Time

As per VITA 46.0, section 5.1 the system power supply ramp-up phase should be between 20 and 150 msec. However, Kontron recommend a ramp-up phase below 25ms.

› Regulation

The system power supplies should be monotonic as they ramp to their specified final values during power up conditions as per VITA 46.0, section 5.1.

The system power supplies shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it went below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

5.1.3. Power Supplies Monitoring

The VX307H embeds three voltage sensors monitoring power rails and internal power supply voltage.

- NCT7802Y by Nuvoton
- LTC2913 by Linear Technology
- INA220 by Texas Instruments

The voltage sensor NCT7802Y is programmed by the IPMC to monitor VS1 and internal voltages, it asserts an alert signal whenever either voltages get out of its specified range. This alert is routed to a maskable interrupt in the cPLD. For detailed specification of NCT7802Y.

The voltage sensor LTC2913 monitors VS1 voltage with a 10 % tolerance. The thresholds are set by hardware on the board. Undervoltage and overvoltage conditions on VS1 are reported to the cPLD which in turn shuts down all VX307H internal power supplies. There is no mechanism for masking these alerts.

The current sensor INA220 monitors VS1 input current.

5.1.4. Output Power Supplies Protections

On the VX307H, all the output power supplies provided on connectors are protected by fuse or current-limiting devices as described in the following table.

Table 43: Output Powers Supplies Protection

Port	Function	Location	Voltage	Protection	Rated Current*	Trip current	Characteristics
Top M2 Slot	M2. Slot power supply	On-Board	+3.3V	Non resettable fuse	4.5 A	-	-
Bottom M2 Slot	M2. Slot power supply	On-Board	+3.3V	Non resettable fuse	4.5 A	-	-

* Worst Case Hold Rated Current* for maximum operation temperature

- VPX Input Power Rails Specification
  The VX307H board has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.
- Absolute Maximum Input Voltage
  The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the VX307H should be carefully tested to ensure compliance with these ratings.

Table 44: Absolute maximum input voltage

POWER RAIL	ABSOLUTE MAXIMUM INPUT VOLTAGE
VPX 3.3V AUX	3.5V
+12V VPX VS1	13V

⚠WARNING

The maximum permitted voltage indicated in the table above must not be exceeded.
Failure to comply with these figures may result in damage to your board.

- Recommended Operating Input voltage
  The following table specifies the recommended operating conditions of the different input power voltages within the board as per VITA46.0. The VX307H is not guaranteed to function if the board is not operating within the prescribed limits.

Table 45: Recommended Operating Input Voltage

POWER RAIL	RECOMMENDED OPERATING INPUT VOLTAGE
VPX 3.3V AUX	3.3V +/-5%
+12V VPX VS1	+12V +/-5% inclusive of ripple

VPX 3.3V AUX shall be used on VX307H boards as per VITA 46.0 and VITA 65.0.
However, this power rail input could be optional on VX307H boards because it is internally generated from the +12V VS1 power input when it is not present on the backplane.
If both, VBAT and 3.3V AUX are not present on the backplane, the date and time retention is not ensured.

- Input Power Supply Protection
  The input power rails are protected on the VX307H by fuse as described in the following table.
  To prevent safety hazards, the chassis power supply must not exceed the Voltage Rating and Interrupt Rating of the fuse.

Table 46: Input Powers Supplies Protection

POWER RAIL	VPX VS1	VPX 3.3 V AUX	VPX -12V AUX
LOCATION	Near P0 power input pins	Near P0 power input pins	Near P0 power input pins
VOLTAGE	+12 V	+3.3 V	-12 V
PROTECTION	Non resettable fuse	Non resettable fuse	Non resettable fuse
RATED CURRENT	20 A	1.5 A	1.5 A
VOLTAGE RATING	32VDC	32VDC	32VDC
MANUFACTURER / PN	EATON / 3216FF20-R	LITTELFUSE / 043501.5KR	LITTELFUSE / 043501.5KR

5.2. Power Consumption Specification

5.2.1. Thermal Power

The following data show total board consumption for different processor configuration and Thermal Design Power. These data help for thermal power dissipation analysis.

Table 47: Thermal Power: board power based on current measurements

Order code	Power Mode	Measured CPU package power (SoC TDP)	Average VPX VS1 Thermal Power (W)	Max VPX VS1 Thermal Power 100ms sampling (W)	Test Condition
VX307H / D-2775TE 16-Core/32-Thread Base freq. @2Ghz TDP 100W	Intel PTU tool 100 % all cores	100 W	130 W (1)	135 W	VPX VS1= 12V, CPU Turbo Off Intel® Xeon® D-2725TE @2Ghz, 32GB DDR4 M.2 bottom module is equipped (OS boot device) No USB module, and no top M.2 module equipped.. Intel PTU benchmarks
	Intel PTU tool 80 % all cores	95 W	120 W (1)	125 W	
	Linux Idle	-	32 W (1)	-	VPX VS1= 12V Intel® Xeon® D-2725TE @2Ghz M.2 bottom module is equipped (OS boot device). No USB module, no top M.2 module equipped. Kontron Board Support Packages in its default configuration.
	BIOS uEFI prompt	-	60 W (1)	-	No USB, and no M.2 module equipped.

Note (1): Typical consumption measured on a few D-27xx parts.

Order code	Power Mode	Measured CPU package power (SoC TDP)	Average VPX VS1 Thermal Power (W)	Max VPX VS1 Thermal Power 100ms sampling (W)	Test Condition
VX307H / D-2796TE 20-Core/40-Thread Base freq. @2Ghz TDP 118W **VX307H / D-2896TER** 20-Core/40-Thread Base freq. @2Ghz TDP 110W	Intel PTU tool 100 % all cores	118 W 110 W	150 W (1) 140 W (2)	155 W 145 W (2)	VPX VS1= 12V, CPU Turbo Off Intel® Xeon® D-2796TE @2Ghz, 64GB DDR4 M.2 bottom module is equipped (OS boot device) No USB module, and no top M.2 module equipped. Intel PTU benchmarks
	Intel PTU tool 80 % all cores	105 W 98 W (2)	140 W (1) 135 W (2)	145 W 140 W (2)	
	Linux Idle	-	48 W	-	VPX VS1= 12V Intel® Xeon® D-2796TE @2Ghz M.2 bottom module is equipped (OS boot device). No USB module, and no top M.2 module equipped. Kontron Board Support Packages in its default configuration.
	BIOS uEFI prompt	-	70 W	-	No USB, and no M.2 module equipped.

Note (1): Typical consumption measured on a few D-27xx parts.
Note (2): Estimated values for D-2896TER

	Voltage Rail Name	Max Current	Max Continuous Power Consumption (W)	Test condition
Board without VPX VS1 power supply Board in stand-by mode	VPX +3V3_AUX	< 500mA	< 1.5 W	VPX +3V3_AUX power rail is present and VPX VS1 power rail not present. VPX +3V3_AUX power rail must support peak current condition at power-on.

5.2.2. Maximum Peak Current

The following data provide maximum continuous and worst case current values on VPX VS1 (12V) power supply. These maximum includes margin to guarantee worst-case part behavior.

Table 48: Maximum VS1 Current

Order code	Measured VPX VS1 Inrush current	Test Condition
VX307H / D-2775TE	16.5 Amps (< 1ms) (1)	Intel® Xeon® D-2725TE @2Ghz Without any USB, M.2 module equipped

Note (1): Typical consumption measured on a few D-27xx parts.

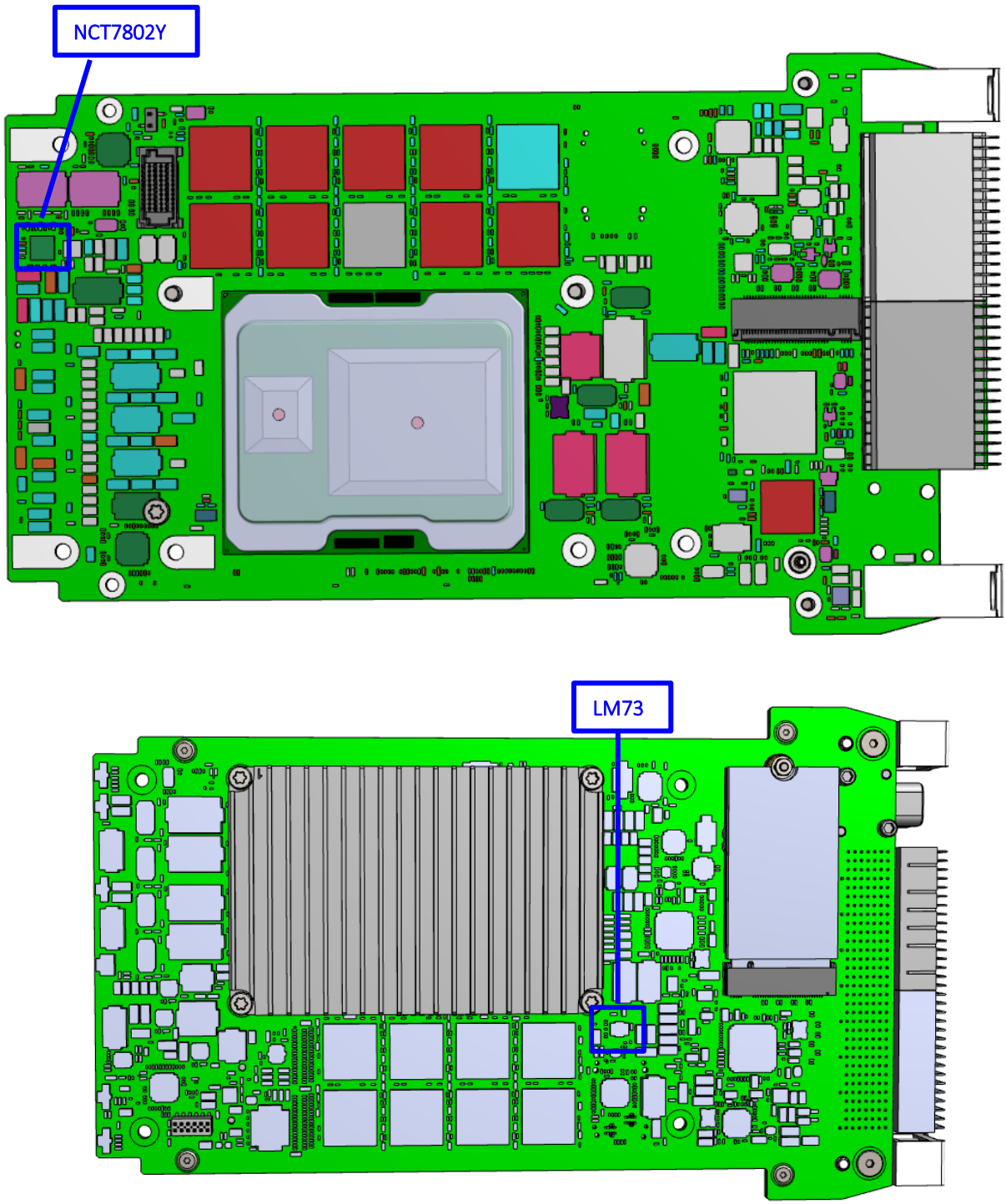
Maximum and peak current draw are intended as without enabled Turbo mode and without M.2 device plugged on board.

5.3. Board - Thermal Monitoring

To ensure long-term reliability of the VX307H, onboard components must not operate beyond their specified maximum temperature. The most critical component on the VX307H is the processor. Operating the VX307H above the maximum operating limits will result in permanent damage to the board.

The VX307H includes a temperature sensor (NCT7802Y by Nuvoton) managed by the IPMC through I2C, and a LM73CIMK managed through the cPLD.

Figure 31: Temperature Sensor Location



In addition to monitoring several internal power supplies, the NCT7802Y supports one on-die temperature sensor and can also get the processor temperature directly via the Intel® PECI interface. The NCT7802Y temperature and voltages monitoring data may be viewed with the Linux "ipmitool" command.

The NCT7802Y has 2 alarm outputs connected to the CPLD:

- ALERT#: logged in CPLD to generate a maskable interrupt.
  The low threshold may also be used as the lower threshold for high temperature hysteresis.
- T_CRIT#: logged in CPLD reg @0x74, leads to fatal error with all internal PSUs power supplies being switched off and the error status is being displayed on the front panel LEDs.

ALERT and T_CRIT thresholds may be modified by the Shelf Manager using the IPMI command or locally by using Linux “ipmitool” command. To know default value and further details about these thresholds, refer to VX307H VITA 46.11 Firmware Release Note document (see section “Related Publications”)

› NCT7802Y Key specifications:
  - Voltage monitoring accuracy +-10 mV
  - Temperature Sensor Accuracy
    - On-chip Temperature Sensor Accuracy (25~70 °C) +- 2 °C typ.
    - On-chip Temperature Sensor Resolution 1 °C
  - Operating Temperature Range -40 °C ~ 85 °C

› LM73CIMK Key specifications: https://www.ti.com/product/LM73/part-details/LM73CIMK-0/NOPB

5.4. SoC - Thermal Monitoring

To allow optimal operation and long-term reliability of the VX307H, the processor must remain within the maximum junction temperature specifications. The maximum operating temperature for the processor die (Tj max) depends on Intel SKUs. The Tj max temperature is the temperature not to exceed, to avoid entering the throttling mode with reduced performance.
The THERMTRIP# temperature threshold is the temperature not to exceed to protect processor from catastrophic overheating. The processor will stop all executions when THERMTRIP# is reached. This threshold is 130°C.
The processor uses the Adaptive Thermal Monitor feature to protect the processor from overheating and includes the following on-die temperature sensors:

- One Digital Thermal Sensor (DTS) for monitoring each processor core
- Catastrophic Cooling Failure Sensor (THERMTRIP#)

These sensors are integrated in the processor and work without any interoperability of the uEFI BIOS or the software application. Thermal Control Circuit allows the processor to maintain a safe operating temperature without the need for special software drivers or interrupt handling routines.

› Digital Thermal Sensor (DTS)

The processor includes on-die Digital Thermal Sensors (DTS), one per processor cores. They can be read via an internal register of the processor.

The temperature returned by the Digital Thermal Sensor will always be at or below the maximum operating junction temperature. Via the Digital Thermal Sensors, the uEFI BIOS or the application software can measure the processor die temperature.

The Max DTS temperature is 100°C.

› Catastrophic Cooling Failure Sensor

The Catastrophic Cooling Failure Sensor protects the processor from catastrophic overheating.
The Catastrophic Cooling Failure Sensor threshold is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds this threshold. Once activated, the event remains latched until the VX307H undergoes a power-on restart (all power off and then on again).
This function cannot be enabled or disabled in the uEFI BIOS. It is always enabled to ensure that the processor is protected in any event.

5.5. Rugged Air-Cooled (RA) - Thermal Performance

› Board Level Thermal Performance
The CPU core maximum DTS temperature is the maximum temperature allowed before entering into throttling mode. The maximum operating temperature for the processor die is 100°C.
This core temperature is accessible through the Linux sensors driver. Refer to the Kontron VME/VPX Fedora Remix Release Notes for information about the "sensors" command, RC class specific features, and power management.

The user can modify several parameters to optimize board thermal performance:

- Processor load: Kontron advises to keep some margin for real time behavior and stay within 80% of processor load.
- Turbo boost mode: for a better control of thermal performance, it is advised to disable this mode for real-time applications.

› Turbo Boost
When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency will dynamically increase until the upper limit of frequency is reached. Intel Turbo Boost Technology has multiple algorithms operating in parallel to manage current, power, and temperature to maximize performance and energy efficiency.

Intel Turbo Boost Technology allows the processor to operate at a power level that is higher than its rated upper power limit (TDP) for short durations to maximize performance.

Learn more about Intel Turbo Boost Technology: http://www.intel.com/technology/turboboost/

Refer to the AMI BIOS for VX307H - User Reference Manual.

⚠CAUTION

Exceeding the limits will lock the board: Enabling the turbo mode is tempting, but the board behavior cannot be guaranteed. Even if the CPU chip may adapt quickly to the situation with frequency reduction, this shall not be recommended.

Table 49: RA variant - Typical Functional Points

TBD- Not available yet

Figure 32: RA Variant – Flow rate vs Ambient Temperature

TBD- Not available yet

5.6. Air-Flow Through (AFT) - Thermal Performance

Figure 33: AFT variant – Example of Air flow direction

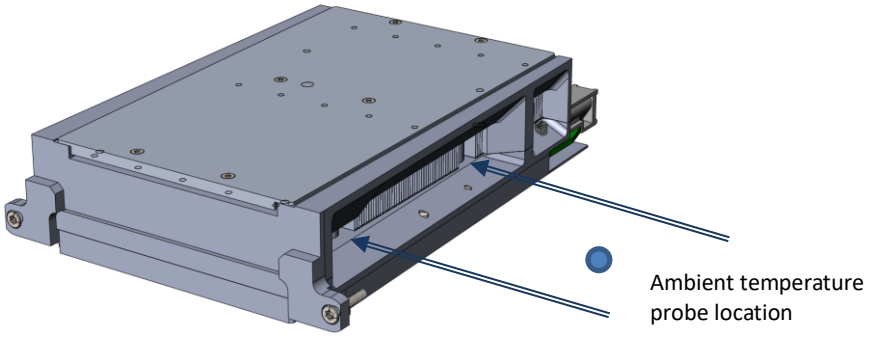


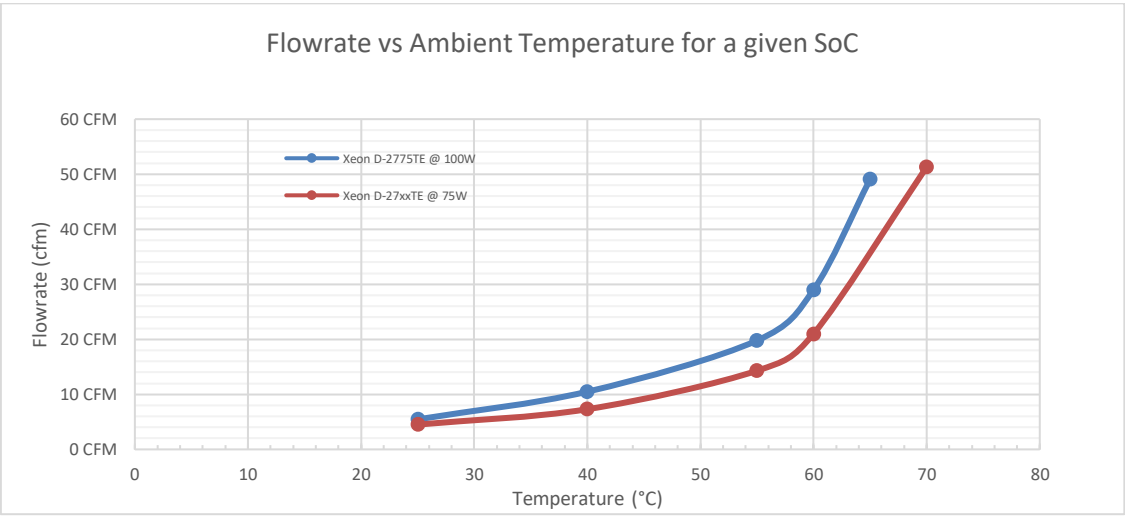
Table 50: AFT variant - Typical Functional Points

VX307H RC class Order Codes	Xeon D-2775TE Xeon D-2896TER Total TDP SoC **@ 100W** (1)	Xeon D-27xxTE Xeon D-2896TER Total TDP SoC **@ 75 W** (1)	Test conditions
CPU Core Base Frequency	2 GHz	2 GHz	Standard Kontron test bench., running Intel PTU with cpu TDP as specified on the processor cores. Processor turbo Off No M.2 module module equipped.
CPU Core Junction Temperature	**100 °C** (2)	**100 °C** (2)	
VX307H-AFT2xxx-xxxxxxxxxx variants **Minimum Flow rate vs temperature**	**20 CFM @55 °C** (2)	**16 CFM @55 °C** (2)	
VX307H-AFT3xxx-xxxxxxxxxx variants **Minimum Flow rate vs temperature**	**N/A**	**52 CFM @70 °C** (2)	

Note (1): Typical processor dissipation measured on a few D-27xx parts using the Intel PTU monitoring tool. Intel PTU stress mode adjusted to force the total SoC power dissipation to the value specified in the table.

Note (2): no CPU throttling if processor junction temperature is strictly below 100°C. End customer applications should target a maximum junction temperature of 97°C (or below) to ensure at least 3°C of margin.

Figure 34: AFT Variant – Flow rate vs Ambient Temperature

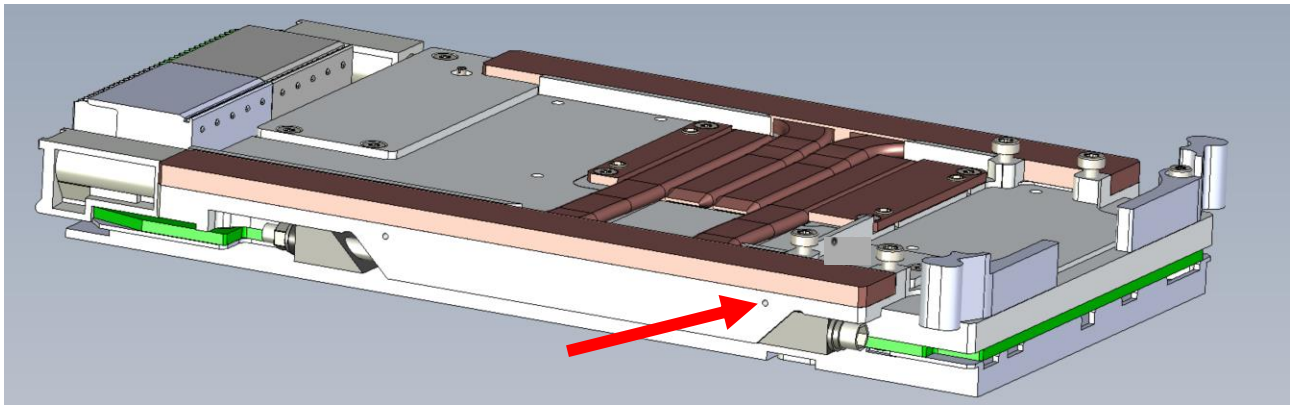


The processor junction temperature shall never exceed 100°C at any time.
Contact Kontron support for additional thermal design data.
Refer to the Intel EDS documents for detailed information about DTR = Dynamic Temperature Range limitations. The default maximum processor temperature range during operation is ±145°C, starting from boot time temperature, with CPU PCIe Gen3 and PCH PCIe/SATA Gen2 speed limitations.
For more information, contact Kontron Support.

5.7. Conduction Cooled - Thermal Performance

› Card Edge Temperature Measurement
The card edge temperature is measured as follows: refer to the red arrow, applicable to the left and rear sides. The wedgelock channel is the channel between the edge of the heat frame and the cold wall of the rack. Refer to probe locations in the following views.

Figure 35: Conduction cooled variant - Holes location for thermal probes



According to ANSI/VITA 47 standard, the plug-in unit edge surface temperature is measured on the plug-in unit.
Card edge shall never exceed +70°C and processor junction temperature shall never exceed 100°C at any time

Table 51: Conduction cooled variant - Typical Functional Points

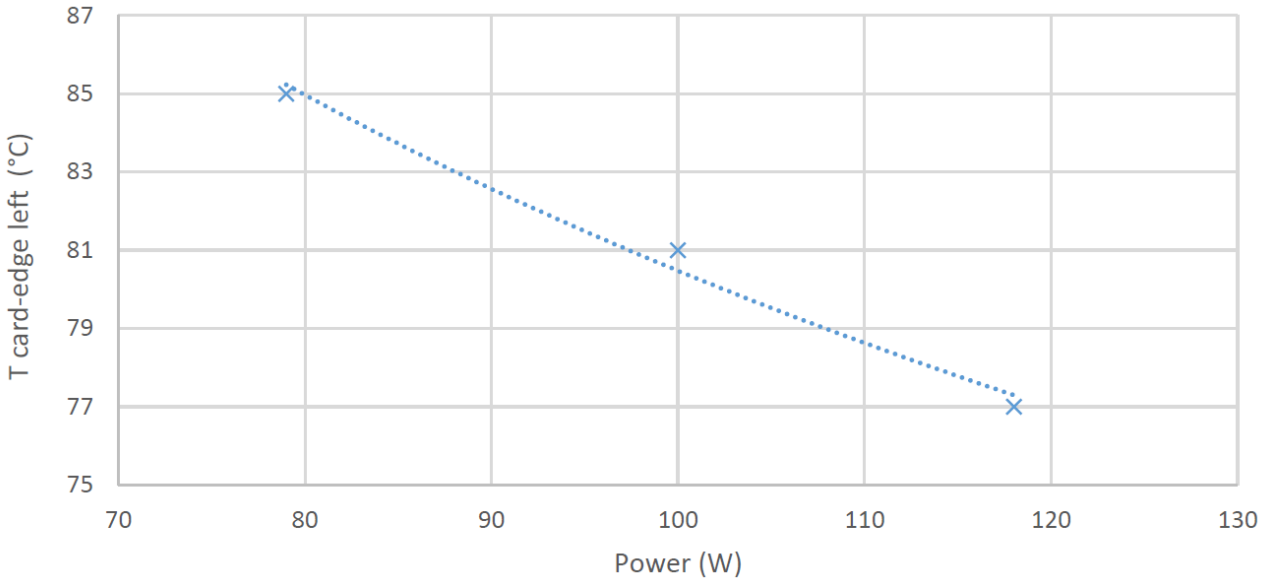
VX307H RC class Order Codes	Xeon D-2775TE Total TDP SoC **@ 100W** (1)	Xeon D-2896TER Total TDP SoC **@ 110 W** (1)	Xeon D-2796TE Total TDP SoC **@ 118 W** (1)	Test conditions
CPU Core Base Frequency	2 GHz	2 GHz	2 GHz	Temperature measured at card edge. Standard RC Kontron test bench., running Intel PTU with cpu TDP as specified on the processor cores. Processor turbo Off No M.2 module module equipped. Maximum temperature measured at card edge. Important note: processor junction temperature shall never exceed 100°C at any time
CPU Core Junction Temperature	**100 °C** (2)	**100 °C** (2)	**100 °C** (2)	
VX307H-RC3xxx-xxxxxxxxxx variants **Max card edge temperature allowed**	**70 °C**	**70°C**	**70°C**	
VX307H-RC4xxx-xxxxxxxxxx variants **Max card edge temperature allowed**	**81 °C** (2)	**78 °C** (2)	**77 °C** (2)	

Note (1): Typical processor dissipation measured on a few D-27xx parts using the Intel PTU monitoring tool. Intel PTU stress mode adjusted to force the total SoC power dissipation to the value specified in the table.

Note (2): no CPU throttling if processor junction temperature is strictly below 100°C. End customer applications a maximum junction temperature of 97°C (or below) instead of 100°C to ensure at least 3°C of margin.

The processor junction temperature shall never exceed 100°C at any time.
Contact Kontron support for additional thermal design data.
Refer to the Intel EDS documents for detailed information about DTR = Dynamic Temperature Range limitations. The default maximum processor temperature range during operation is ±145°C, starting from boot time temperature, with CPU PCIe Gen3 and PCH PCIe/SATA Gen2 speed limitations.
For more information, contact Kontron Support.

Figure 36: CPU Heatsink performance applicable to RC Variant – CPU power vs Card Edge Temperature



6. RTM compatible with the VX307H Compute Intensive profile

6.1. Overview

The Kontron PB-VX3-40G-H-601 is a 3U VPX Rear Transition Module compliant with the definition of the Rear Transition Module on VPX Standard –VITA 46.10.
It provides rear I/O peripherals connectivity for Kontron VX307H Compute Intensive variants featuring P2 VPX connector.

Figure 48: PB-VX3-40G-H-601 3U VPX Overview

6.2. Ordering Information

Table 52: RTM tooling - Order Codes

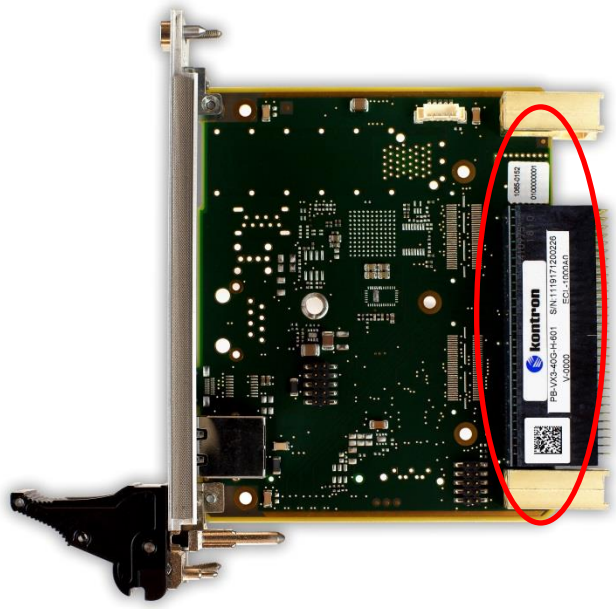
Standard Order Codes	Description
PB-VX3-40G-H-601 (1065-0152)	3U single slot 5 HP (1.0") VPX Rear Transition Module providing serial lines for standard VX307H boards. Tooling equipment for lab use.

PB-VX3-40G-H-601 is compatible with VX307H Compute Intensive Variants only.
Do not use with I/O Intensive boards and ecosystems.
When plugged in an existing VPX ecosystem, the available and usable interfaces of the PB-VX3-40G-H-601 will depend on the VX307H variant and the backplane used.

6.3. Identification and labels

The PB-VX3-40G-H-601 RTMs are identified by labels fitted to the VPX connector on the top side of the board. Example on the picture below.

Table 53: RTM tooling - Identification



6.4. Technical specification

Table 54: PB-VX3-40G-H-601 Technical Specifications

TECHNICAL SPECIFICATIONS	
Power Specification	
Supply Voltage	5V VS3 VPX, 12V VS1 VPX
Mechanical Specification	
Front Panel size	1 slot (5HP)
Dimension (mm)	100 x 81.5
Weight (g)	120
Environmental Specification	
Conformal coating	Not available
Operating temperature	10°C/35°C (lab use)

5V VS3 VPX power supply must be provided to PB-VX3-40G-H-601 for full operating.

6.5. Front Panel Interfaces

Figure 37: PB-VX3-40G-H-601 Front Panel I/O Interfaces

Table 55: PB-VX3-40G-H-601 Front Panel Technical Specification

Front Panel Name	Description	Comment
MAINT	COM1/2: maintenance port , EIA-232 or 3.3V LVCMOS level signaling - RJ-12 connector	

6.6. Safety Requirements

The following safety precautions must be observed when installing or operating the PB-VX3-40G-H-6xx. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

NOTICE

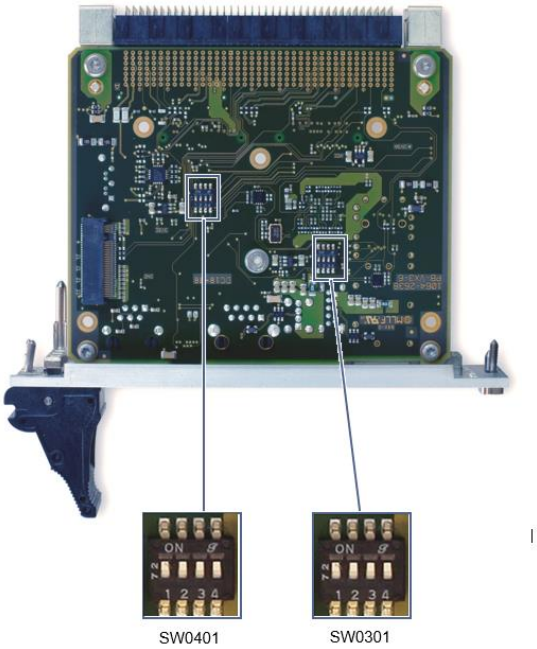
ESD Sensitive Device!
This RTM contains electrostatically sensitive devices. Observe the necessary precautions to avoid damage to your board:
Discharge your clothing before touching the assembly. Tools must be discharged before use.
Do not touch components, connector pins or traces.
We strongly recommend our customers to work in an environment equipped with anti-static workbenches with professional discharging equipment

6.7. Installation

The standard precautions, installation procedures, and general information detailed in section 6 for PB-VX3-40G-H-601 RTMs must also be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

- Microswitches
  If equipped, micro switches on the PB-VX3-40G-601 are unused. Default setting is OFF for all switches.

Figure 38: PB-VX3-40G-H-601 - Micro switches location



6.8. Physical I/Os

The following section lists the physical I/Os that are different from PB-VX3-40G-601 RTMs variant.

6.8.1. Maintenance Port Connector

The PB-VX3-40G-H-601 provides two serial maintenance ports, COM1 and COM2 on front panel RJ12 connector. COM1 and COM2 can operate simultaneously in EIA-232 mode only (simplified RX/TX) or in 3.3V LVCMOS level signaling.
Defaults setting are:

- Processor console is redirected on COM1
- Serial mode is simplified serial line mode Rx/Tx only, 115200 bauds

Each serial port is configurable via the BIOS setup menu as EIA-232 or 3.3V LVCMOS level signaling.
Each port operates in full duplex mode.

› Pin Assignment

Table 56: Serial Connector Pin Assignment

PIN	SIGNAL
1	COM2 TXD
2	Shell
3	COM1 TXD
4	COM1 RXD
5	GND
6	COM2 RXD

Figure 39: Serial Connector

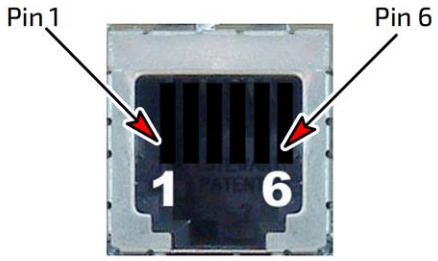


Table 57: Serial Connector Signal Description

MNEMONIC	DESCRIPTION
COM2 RXD	COM2 Receive Data
COM2 TXD	COM2 Transmit data
COM1 RXD	COM1 Receive Data
COM1 TXD	COM1 Transmit Data
GND	Ground
Shell	Chassis Ground

› Serial Cable Designation

The Serial cable shall be shielded and shall provide a good shielding continuity between each end. The Serial cable length should not exceed 10 m.

Serial cable is a RJ-12 (6 pin, 6 conductors). A RJ-12 to DB9 male or DB9 female adapter is available from multiple sources, such as:

- Kontron Order Code KIT-RJ12DB9
- Triangle Cable http://www.trianglecables.com/db9m-rj12.html

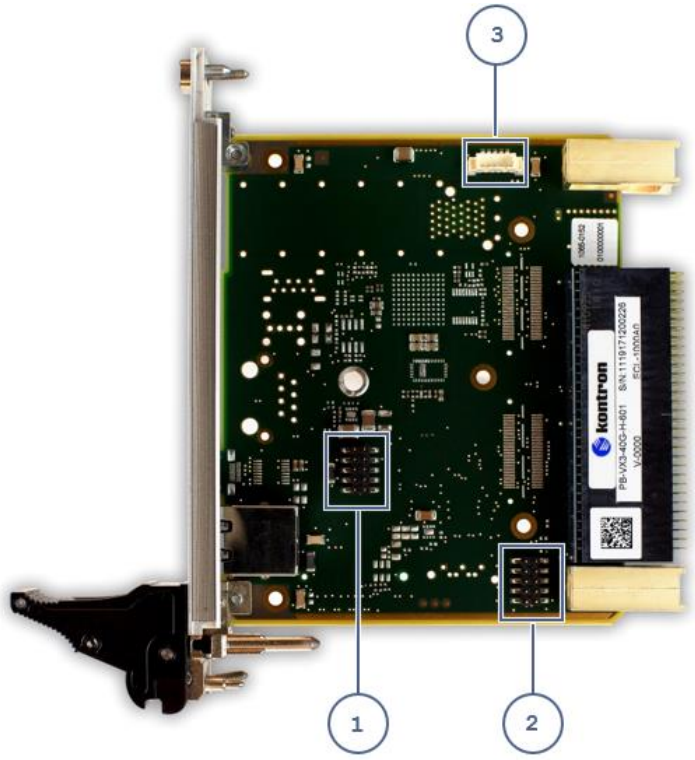
Table 58: Serial Cable Pin Assignment

DB9 A Pin Connector	Signal	RJ-12 Pin Connector
-	-	1
2	TXD	3
3	RXD	4
-	-	6
5	GND	5

Figure 40: Serial Cable

6.8.2. On-board Connectors

Figure 41: PB-VX3-40G-H-601 – On-board Connectors



1. J0401
2. J0402
3. J0403

Table 59: PB-VX3-40G-H-601 – On-board Connectors

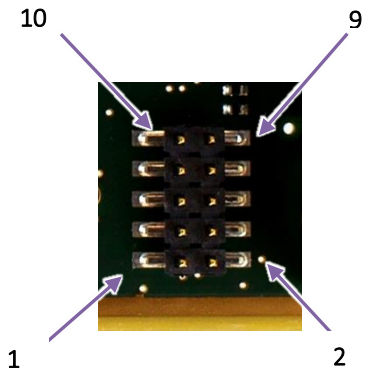
CONNECTOR	DESCRIPTION	VX307H usage
J0401	Serial lines on-board connector	Not used with VX307H
J0402	GPIOs connector	Refer to the next sections
J0403	SMBus connector. IPMB B is default SMBus	Not used with VX307H

6.8.3. GPIOs on-board Connector

Table 60: GPIOs Connector Pin Assignment

PIN	SIGNAL
1	Reserved, do not use
2	Reserved, do not use
3	Reserved, do not use
4	VPX Maskable Reset
5	GND
6	GND
7	Reserved, do not use
8	GPIO1
9	Reserved, do not use
10	Reserved, do not use

Figure 42: GPIOs Connector



GPIOs availability depends on the SBC variants.
Contact Kontron support for detailed information.

6.8.4. Rear I/O Connectors

The PB-VX3-40G-H-6xx Rear Transition Module conducts a wide range of I/O signals through the rear I/O connectors RP0, RP1 and RP2.

- RP0: 15-wafer 7-row mixed connector.
- RP1: 16-wafer 7-row differential connector.
- RP2: Not equipped.
-

Figure 43: PB-VX3-40G-H-601 – Rear I/O Connectors

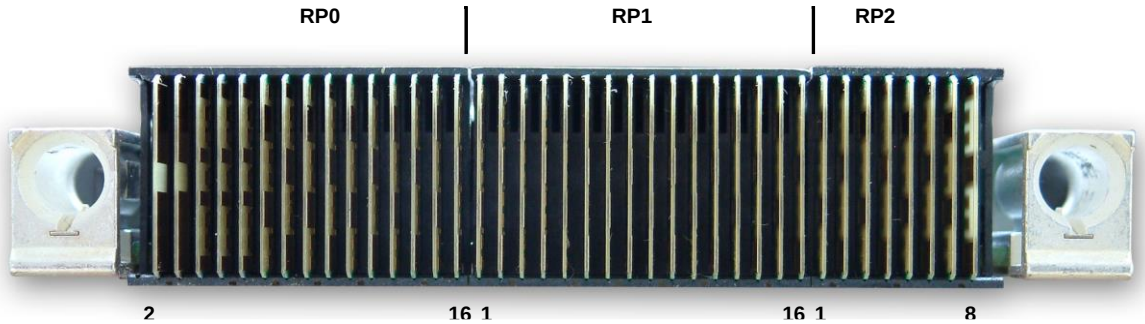
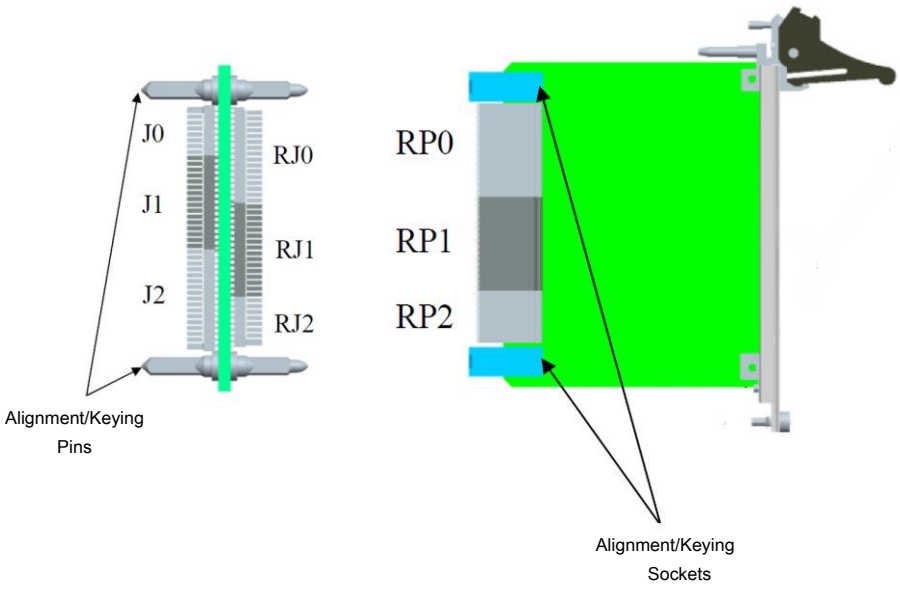


Figure 44: PB-VX3-40G-H-601 – Connectors Identification



6.8.5. RP0 Connector

Table 61: Rear I/O VPX Connector RP0 Wafer Assignment

- Legend

IPMB_B/A	IPMB I2C bus
COM1/COM2	Maintenance Ports

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	No wafer						
2	+12V	+12V	+12V	NC	NC	NC	NC
3	+5V	+5V	+5V	NC	+5V	+5V	+5V
4	IPMB_B CLK	IPMB_B DAT	GND	NC	GND	SYSRESET*	NC
5	NC	NC	GND	NC	GND	NC	NC
6	NC	NC	GND	NC	GND	NC	NC
7	NC	GND	NC	NC	GND	NC	NC
8	GND	NC	NC	GND	NC	NC	GND
9	NC	GND	NC	NC	GND	NC	NC
10	GND	NC	NC	GND	NC	NC	GND
11	NC	GND	NC	NC	GND	NC	NC
12	GND	NC	NC	GND	NC	NC	GND
13	NC	GND	NC	NC	GND	NC	NC
14	GND	NC	NC	GND	COM1 TXD	COM1 RXD	GND
15	GND	GND	GND	GND	GND	GND	GND
16	GND	NC	NC	GND	NC	NC	GND
CASE	GND						

* signal active when low

Table 62: Rear I/O VPX Connector RP0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
+12V	+12 Volts DC power (VS1 VPX supply). NC (+12V) pins are not connected (VS2 VPX supply)
+5V	+5 Volts DC power (VS3 VPX supply).
GND	Ground
IPMB B	I2C Bus 1
COM1	Maintenance port : serial Lines EIA-232 or 3V3 LVCMOS level signaling
NC	Not connected

6.8.6. RP1 Connector

Table 63: Rear I/O VPX Connector RP1 Wafer Assignment

- Legend

COM2	Maintenance Port	Maskable Reset	Maskable reset

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	COM2 TXD	GND	NC	GND	GND	NC	GND
2	GND	NC	NC	NC	NC	NC	NC
3	COM2 RXD	GND	NC	GND	GND	NC	GND
4	GND	NC	NC	NC	NC	NC	NC
5	NC	GND	NC	GND	GND	NC	GND
6	GND	NC	NC	NC	NC	NC	NC
7	Maskable Reset*	GND	NC	GND	GND	NC	GND
8	GND	NC	NC	NC	NC	NC	NC
9	NC	GND	NC	NC	GND	NC	NC
10	GND	NC	NC	GND	NC	NC	GND
11	NC	GND	NC	NC	GND	NC	NC
12	GND	NC	NC	GND	NC	NC	GND
13	NC	GND	NC	NC	GND	NC	NC
14	GND	NC	NC	GND	NC	NC	GND
15	NC	GND	NC	NC	GND	NC	NC
16	GND	NC	NC	GND	NC	NC	GND
CASE	GND						

* signal active when low

Table 64: Rear I/O VPX Connector RP1 Signal Definition

MNEMONIC	SIGNAL DEFINITION
Maskable Reset* or GPIO8	Reset input or Optional general purpose I/O 8 (handled by CPLD) (may be left unconnected if not used).
COM2	COM2 Maintenance port : serial Lines EIA-232 or 3V3 LVCMOS level signaling
NC	Not connected
GND	Ground

7. Front Board – EVAL Tooling

The conduction cooled variant of the VX307H does not offer front I/O interfaces.
To ease product assessments and developments in lab conditions, the FB-VX3-0010 tooling kit can be ordered to offer Serial, Ethernet and USB2.0 interfaces on the front panel of conduction cooled variants.

The FB-VX3-0010 tooling kit is not equipped by default on conduction-cooled boards
If FB-VX3-0010 is required on conduction-cooled boards for assessments or developments, this tooling option must be ordered separately.
When FB-VX3-0010 tooling kit is installed on the products, the product specifications will be restricted to lab use conditions.

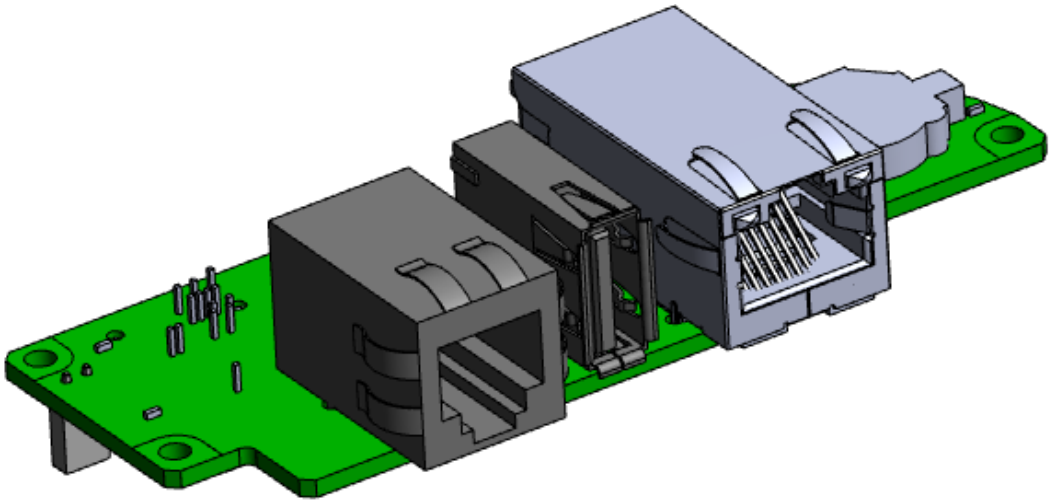
Table 65: FB-VX3-0010 tooling - Order Code

Standard Order Codes	Description
FB-VX3-0010	Tooling kit providing one serial line, one USB2.0 port and one RJ45 1000Base-T Ethernet. Tooling equipment for lab use. Serial, USB2.0 and Ethernet interfaces definition presented in section 4.1 is applicable to the FB-VX3-0010 kit

When FB-VX3-0010 is mounted on a conduction cooled board:

- The product usage is restricted to a lab use, in lab conditions.
- The product form factor is affected
- The RC class specifications are not applicable

Figure 45: FB-VX3-0010 tooling



The mounting of the FB-VX3-0010 kit is described in the following sections.

7.1. Installation on Conduction Cooled variant

Figure 46: FB-VX3-0010 mounting - Conduction Cooled variant

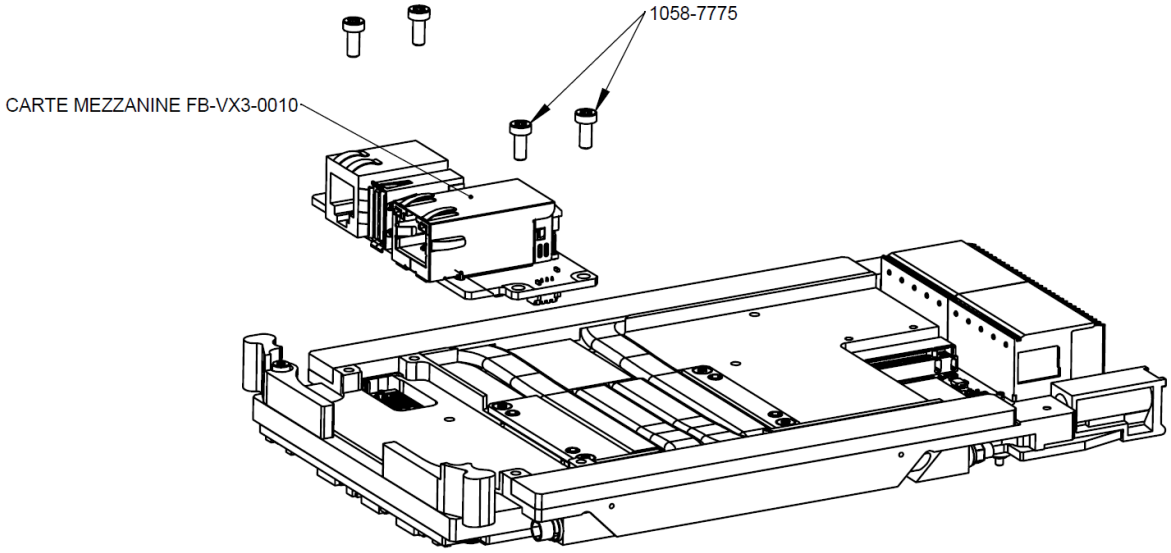


Table 66: FB-VX3-0010 mounting – nut and washer defintion

Article	DESCRIPTION	Qty	Torque	Thread lock
1058-7775	HEXALOBULAR SOCKET CHEESE HEAD SCREW ISO 14580-M2.5X6-A4-70	4	0.28 N.m	Loctite 222 Or equivalent

8. Technical Support

For technical support, contact our Support Department:
E-Mail: support.KFR@kontron.com
Phone: +33-498-163-400

Make sure you have the following information available when you call:
Product ID Number (PN),
Serial Number (SN)

The serial number can be found on the Type Label, located on the product's rear side.

Be ready to explain the nature of your problem to the service technician.

9. Warranty

Due to their limited service life, parts that by their nature are subject to a particularly high degree of wear (wearing parts) are excluded from the warranty beyond that provided by law. This applies to the CMOS battery, for example.

If there is a protection label on your product, then the warranty is lost if the product is opened.

10. Returning Defective Merchandise

All equipment returned to Kontron must have a Return of Material Authorization (RMA) number assigned exclusively by Kontron. Kontron cannot be held responsible for any loss or damage caused to the equipment received without an RMA number. The buyer accepts responsibility for all freight charges for the return of goods to Kontron's designated facility. Kontron will pay the return freight charges back to the buyer's location in the event that the equipment is repaired or replaced within the stipulated warranty period. Follow these steps before returning any product to Kontron.
Visit the RMA Information website: https://www.kontron.com/en/support/rma-information

TO REQUEST A RETURN MATERIAL AUTHORIZATION (RMA) NUMBER

1. E-mail to repair.KFR@kontron.com with the following information:
2. Part number, serial number of the material to be returned,
3. Failure description or reason for return
4. Once everything is completed, an RMA form will be sent to you if your equipment is under warranty. If your equipment is not under warranty, a quote will be sent and the RMA will be sent when we receive your PO.
5. Print the RMA form and put it with the material to be returned
6. Ship the goods to the address indicated on the RMA form

The goods for repair must be packed properly for shipping, considering shock and ESD protection.

Goods returned to Kontron Modular Computers S.A.S in non-proper packaging will be considered as customer caused faults and cannot be accepted as warranty repairs.

About Kontron

Kontron is a global leader in IoT/Embedded Computing Technology (ECT) and offers individual solutions in the areas of Internet of Things (IoT) and Industry 4.0 through a combined portfolio of hardware, software and services. With its standard and customized products based on highly reliable state-of-the-art technologies, Kontron provides secure and innovative applications for a wide variety of industries. As a result, customers benefit from accelerated time-to-market, lower total cost of ownership, extended product lifecycles and the best fully integrated applications.

For more information, please visit: **www.kontron.com**

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