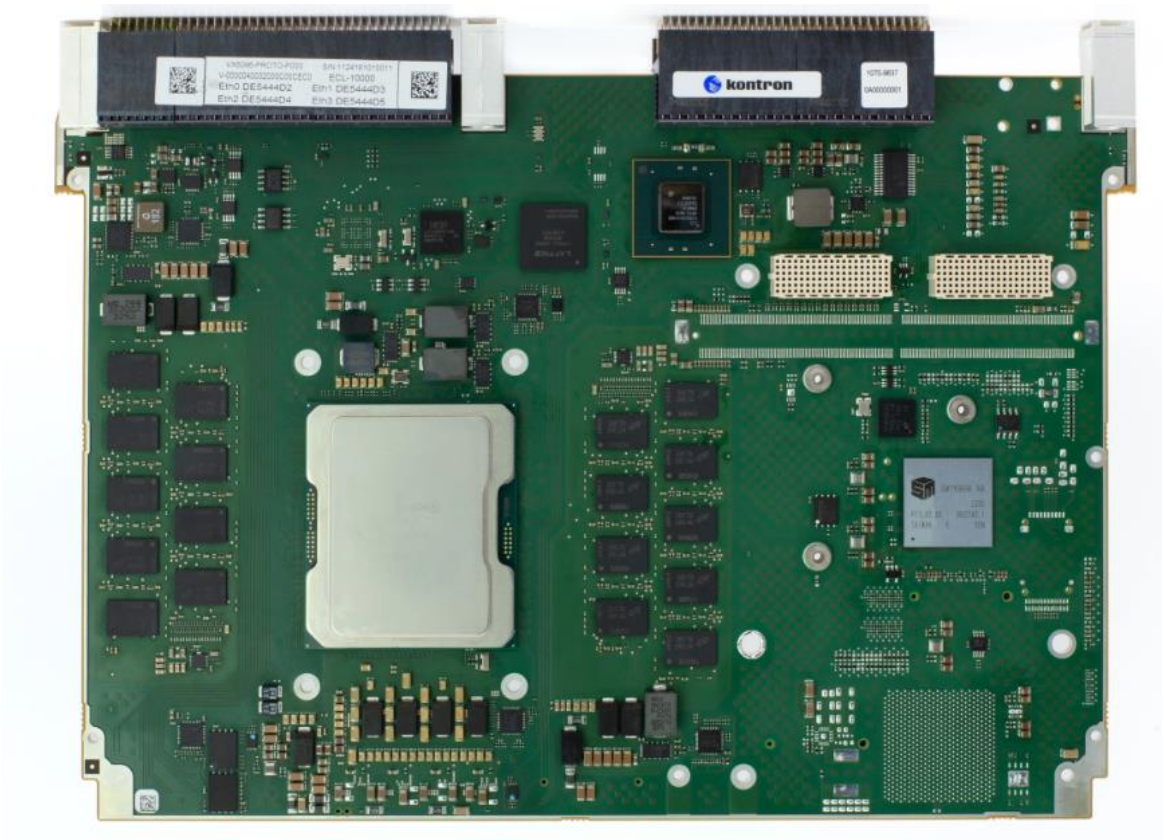
VX6096 - User Guide

6U VPX Computing Node



D287691-V0.4 - May 2025

kontron

Disclaimer

Kontron would like to point out that the information contained in this user guide may be subject to alteration, particularly as a result of the constant upgrading of Kontron products. This document does not entail any guarantee on the part of Kontron with respect to technical processes described in the user guide or any product characteristics set out in the user guide. Kontron assumes no responsibility or liability for the use of the described product(s), conveys no license or title under any patent, copyright or mask work rights to these products and makes no representations or warranties that these products are free from patent, copyright or mask work right infringement unless otherwise specified. Applications that are described in this user guide are for illustration purposes only. Kontron makes no representation or warranty that such application will be suitable for the specified use without further testing or modification. Kontron expressly informs the user that this user guide only contains a general description of processes and instructions which may not be applicable in every individual case. In cases of doubt, please contact Kontron.

 Kontron points out that the information contained in this user guide is constantly being updated in line with the technical alterations and improvements made by Kontron to the products and thus this user guide only reflects the technical status of the products by Kontron at the time of publishing.

Kontron Europe GmbH
Gutenbergstraße 2
85737 Ismaning
Germany
www.kontron.com

Intended Use

You understand and agree that your use of Kontron devices as a component in High Risk Applications is entirely at your risk. To minimize the risks associated with your products and applications, you should provide adequate design and operating safeguards. You are solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning your products. You are responsible to ensure that your systems (and any Kontron hardware or software components incorporated in your systems) meet all applicable requirements. Unless otherwise stated in the product documentation, the Kontron device is not provided with error-tolerance capabilities and cannot therefore be deemed as being engineered, manufactured or setup to be compliant for implementation or for resale as device in High Risk Applications. All application and safety related information in this document (including application descriptions, suggested safety measures, suggested Kontron products, and other materials) is provided for reference only.

⚠CAUTION	Handling and operation of the product is permitted only for trained personnel within a work place that is access controlled. Please follow the “General Safety Instructions” supplied with the system.
NOTICE	You find the most recent version of the “General Safety Instructions“ online in the download area of this product.
NOTICE	This product is not suited for storage or operation in corrosive environments, in particular under exposure to sulfur and chlorine and their compounds. For information on how to harden electronics and mechanics against these stress conditions, contact Kontron Support.

Revision History

Revision	Brief Description of Changes	Date of Issue
0.1	Preliminary - Initial Issue	17-Nov-2023
0.2	Preliminary issue. Modifications tracked by change bars in the left margin	24-May-2024
0.3	Preliminary issue: Figure 4 updated	05-June-2024
0.4	Preliminary issue Sections significantly moved and renumbered Refer to the change bars in the left margin	07-May-2025

Terms and Conditions

Kontron warrants products in accordance with defined regional warranty periods. For more information about warranty compliance and conformity, and the warranty period in your region, visit https://www.kontron.com/terms-and-conditions.
Kontron sells products worldwide and declares regional General Terms & Conditions of Sale, and Purchase Order Terms & Conditions. Visit https://www.kontron.com/terms-and-conditions.
For contact information, refer to the corporate offices contact information on the last page of this user guide or visit our website CONTACT US.

Customer Support

Please contact our support team at support.KFR@kontron.com .

Customer Service

As a trusted technology innovator and global solutions provider, Kontron extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly experienced support enables Kontron to provide exceptional peace of mind to build and maintain successful products.
For more details on Kontron's service offerings such as: enhanced repair services, extended warranty, Kontron training academy, and more visit https://www.kontron.com/support-and-services.

Customer Comments

If you have any difficulties using this user guide, discover an error, or just want to provide some feedback, contact Kontron support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user guide on our website.

1. Symbols

The following symbols may be used in this user guide

DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
NOTICE	NOTICE indicates a property damage message.
CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
	**Electric Shock!** This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	**ESD Sensitive Device!** This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	**HOT Surface!** Do NOT touch! Allow to cool before servicing.
	**Laser!** This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol indicates important information which must be read carefully.
	This symbol precedes helpful hints and tips for daily use.

2. For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning
All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!
Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.
Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

⚠CAUTION

Danger of explosion if the battery is replaced incorrectly.
Replace only with same or equivalent battery type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

3. General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

4. Quality and Environmental Management

Kontron aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding Kontron's quality and environmental responsibilities, visit https://www.kontron.com/about-kontron/corporate-responsibility/quality-management.

Disposal and Recycling

Kontron's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Environmental protection is a high priority with Kontron.
Kontron follows the WEEE directive
You are encouraged to return our products for proper disposal.

5. Table of Contents

6. List of Figures

7. List of Tables

8. Introduction

The Kontron VX6096 is a 6U VPX computing blade for data and signal processing application focusing on application domains such as Defense, Transportation and Energy/Industry.
The Kontron VPX blade VX6096 is the ideal building block for intensive parallel computing workloads where a cluster of Kontron VX6096 can be used in switched OpenVPX environments.

VX6096 variants are fully compatible with system architectures developed in alignment with the SOSA™ technical standard.

In this document:
VX6096 is the product/board without any option or variant considerations.
VX6096 stands for variant compatible with the SOSA Compute Intensive profile.
AFT stands for the Standard Air Flow Through variants
RC variant stands for the Ruggedized Conduction cooled variants

A list of Terminology, Definitions and Abbreviations applicable to this document are presented in the “Terminology, Definitions and Abbreviations” section at the end of this document.

Figure 1: AFT variant overview

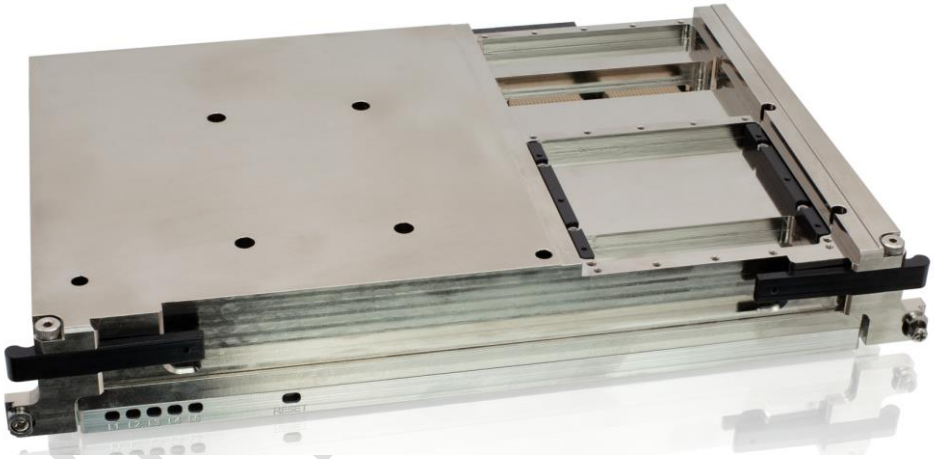
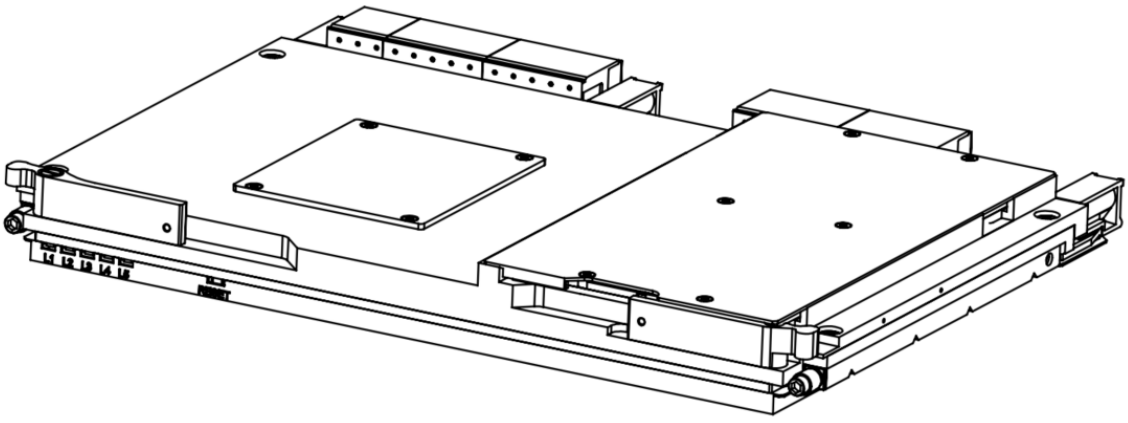


Figure 2: Conduction cooled variant view (with 2LM option)



8.1. Manual Overview

8.1.1. Objective

This guide provides general information, hardware instructions, operating instructions and functional description of the VX6096 board. The onboard programming, onboard firmware and other software (e.g. drivers and BSPs), and product limitations are described in detail in separate product guides and Release Notes (see section "Related Publications").

This hardware technical documentation reflects the most recent version of the product. The “Release Notes" (see section "Related Publications") might help to keep track of potential evolutions

In this document
AFT stands for AFT2 and AFT3 variants
RC stands for RC3 variants
Refer to the “Environmental Specifications” Section for details about the the AFT and RC class definitions.

8.1.2. Audience

The scope of this guide is to cover, as much as possible the range of people who will handle or use the VX6096, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, system, cabling, grounding and communications.

8.1.3. Scope

This guide describes the VX6096 product, without any optional mezzanines equipped.
The VX6096 variants described in this guide are fully compatible with system architectures developed in alignment with the SOSA™ technical standard.

8.1.4. Terminology, Definitions and Abbreviations

Table 1: Terms and acronyms

Term or Acronym	Definition
BIOS	BIOS (Basic Input/Output System) firmware
BSP	A BSP (Board Support Package) from Kontron is a collection of software and configuration files that support the operation of a specific hardware platform
Compute Intensive	VPX compute intensive refers to VPX systems designed to handle high-performance computing tasks that require significant processing power and data throughput
Core	A processing unit including instruction cache, data cache, and often L2 cache.
COTS	Commercial Off The Shelf.
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
ECC	ECC (Error-Correcting Code) memory is a type of computer data storage that can detect and correct the most common kinds of internal data corruption
E.C.Level or ECL	Engineering Change Level refers to the exact technical definitions and revisions of a produc
EEPROM	Electrically Erasable Programmable Read-Only Memory
EU Directive	EU directives are legislative acts that set out goals that all EU countries must achieve
F-RAM	Ferroelectric Random Access Memory
I2C or I²C	I2C (Inter-Integrated Circuit), also known as I²C or IIC, is a synchronous, multi-master/multi-slave, single-ended, serial communication bus
IPMC	Intelligent Platform Management Controller
IPMI	Intelligent Platform Management Interface
DDR4	DDR4 (Double Data Rate 4) is the fourth generation of DDR SDRAM (Synchronous Dynamic Random-Access Memory) technology
Gdiscrete1	GDiscrete1 is a signal used in embedded computing systems, particularly in VPX (VITA 46) and SOSA (Sensor Open Systems Architecture) standards
GPIO	General-Purpose Input/Output
KCS	KCS (Keyboard Controller Style) interface is a communication interface between the host CPU and the IPMI (Intelligent Platform Management Interface) controller
LED	Light-Emitting Diode
LPC	Low Pin Count bus interface
LVCMOS	Low Voltage Complementary Metal-Oxide-Semiconductor
M.2	M.2, formerly known as the Next Generation Form Factor (NGFF), is a specification for internally mounted computer expansion cards and associated connectors. M.2 replaces the Mini SATA (mSATA) and Mini PCIe (mPCIe) standards
MTBF	Mean Time Between Failure
NVME	NVMe (Non-Volatile Memory Express) is a protocol used for accessing high-speed storage media that utilizes the PCI Express (PCIe) interface
NVMRO	NVMRO (Non-Volatile Memory Read Only) is a signal used in embedded computing systems to control the write protection of non-volatile memory
OD	Open Drain Output
Option	A feature which requires a specific order code.
PBIT	Power-on Built-In Test is a diagnostic test performed during the power-on sequence of a system to verify the functionality and integrity of its hardware components.
PCB	Printed Circuit Board.

Term or Acronym	Definition
PCH	Platform Controller Hub. The PCH architecture replaced the older northbridge and southbridge chipset design. The PCH is integrated in the D-2700/D-2800 SoC.
PCIe	Synonym of PCI Express.
PECI	PECI (Platform Environment Control Interface) is a communication protocol developed by Intel for monitoring and controlling the temperature and power consumption of Intel processors
Processor	According to Intel® terminology, the processor - synonymous with SoC Refers to the Intel® Core™ XEON-D-27xx or D-28xx processor.
PROCHOT	PROCHOT (Processor Hot) is a signal used by Intel processors to indicate that the CPU has reached a critical temperature threshold
Provision	A feature not yet available.
PTU (Intel®)	Intel® Performance Test Utility.
RTC	Real-Time Clock
RS-232 or EIA-232	RS-232, also known as EIA-232, is a standard for serial communication transmission of data
RS-422 or EIA-422	RS-422, also known as EIA-422, is a standard for serial communication transmission of data
RS-485 or EIA-485	RS-485, also known as EIA-485, is a standard for serial communication transmission of data
SATA	SATA (Serial AT Attachment) is a computer bus interface that connects host bus adapters to mass storage devices
SBC	Single Board Computer (the term defaults to VM606x).
SoC (Intel®)	System on chip. According to Intel® terminology, the SoC - synonymous with processor
SDRAM	Synchronous Dynamic Random-Access Memory
SKU	Stock Keeping Unit: A catalog's product and service identification code.
SOSA	Sensor Open Systems Architecture
SMBus or SMB	System Management Bus.
SSD	Solid State Drive
SWaP, SWaP-C	Seize, Weight and Power - Cost: an acronym to summarize the capabilities of an embedded system in Military or Aerospace.
TBD	To Be Defined. Information not available at the time this document was released
TDP	Thermal Design Power: the target power level of the processor. It represents the maximum sustained power expected from realistic applications. It is an input to the thermal design of the board.
TPM	Trusted Platform Module: An international standard for a secure crypto processor based on a dedicated hardware device and integrating cryptographic keys. Promoted by consortium TCG (Trusted Computing Group).
Turbo Boost Technology (Intel®)	A feature that opportunistically enables the processor to run a faster frequency. This results in increased performance of both single and multi-threaded applications.
uEFI or UEFI	UEFI (Unified Extensible Firmware Interface) is a specification for the firmware architecture of a computing platform
Uncore	In Intel® architecture, a unit of the SoC which includes the Ring, the Caching Agent Cbo, the Last Level Cache (LLC), the Home Agent (HA), the Integrated Memory Controller (IMC), the Integrated IO Module (IIO), the Power Control Unit (PCU).
USB	Universal Serial Bus
USER Domain	The USER domain is a specific area within the non-volatile memory that stores user-specific data
VPD	Vital Product Data
VPD Domain	The VPD domain is a specific area within the non-volatile memory that stores VPD data
VR	Voltage Regulator
XMC	XMC (Switched Mezzanine Card) is a standard for mezzanine cards used in embedded computing systems

Term or Acronym	Definition
XMCIO or XMCIOs	XMC mezzanine rear I/Os
1 GbE	Abbreviation for 1-Gbit Ethernet interface (1000BASE-T).
2LM	Top/bottom covers for the 2 Maintenance level as defined per VITA 48 REDI standards

8.2. Related Publications

The following publications contain information relating to this product.

Table 2: VITA - Related publications

Designation	Title	Abstract	VITA Status – April 2025
ANSI/VITA 42.0-2021	XMC: Switched Mezzanine Card (XMC) Auxiliary Standard	This document defines an open standard for supporting high-speed, switched interconnect protocols on an existing, widely deployed mezzanine card form factor.	ANSI/VITA Approved
ANSI/VITA 46.0-2023 +Errata	VPX Baseline Standard	This standard describes VITA 46.0 VPX Baseline Standard; an evolutionary step forward for the provision of high-speed interconnects in harsh environment applications.	ANSI/VITA Approved
ANSI/VITA 46.9-2018 (R2024)	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard	This document describes an open standard for PMC or XMC mezzanine rear I/O pin mappings to VITA 46.0 plug-in module backplane connectors.	ANSI/VITA Reaffirmed
ANSI/VITA 46.10-2009 (S2024)	Rear Transition Module for VPX	This standard defines signal mapping for VPX Rear Transition Modules (RTMs).	ANSI/VITA Stabilized Maintenance
ANSI/VITA 46.11-2022	System Management on VPX	This document defines a framework for System Management in VPX systems. It enables interoperability within the VPX ecosystem at the Field Replaceable Unit (FRU), chassis and system levels.	ANSI/VITA Approved
ANSI/VITA 47.0-2019	Construction, Safety, and Quality for Plug-In Modules Standard	The VITA 47 group of standards defines environmental, design and construction, safety, and quality requirements for commercial-off-the-shelf (COTS) Plug-In Modules intended for ground and aerospace applications.	ANSI/VITA Approved
ANSI/VITA 48.0-2022	Mechanical Standard for Microcomputers using Ruggedized Enhanced Design Implementation (REDI)	This standard defines a mechanical implementation for Plug-In Modules.	ANSI/VITA Approved
ANSI/VITA 48.2-2022	Mechanical Standard for VPX REDI Conduction Cooling	This standard defines the mechanical requirements that are needed to ensure the mechanical interchangeability of conduction cooled 3U and 6U Plug-In Modules and defines the features required to achieve Two Level Maintenance compatibility.	ANSI/VITA Approved
ANSI/VITA 48.8-2022	Mechanical Standard for VPX REDI Air Flow Through Cooling, 1.0 "to 1.5 "Pitches	This document describes an open standard for the design requirements for an air-flow-through cooled plug-in module having 3U and 6U form factors while retaining the VITA 46.0 connector layout.	ANSI/VITA Approved
ANSI/VITA 51.0-2012 (S2024)	Reliability Prediction	This document provides a framework for electronics equipment reliability standards, and establishes a reliability Community of Practice.	ANSI/VITA Stabilized Maintenance
ANSI/VITA 61.0-2022	XMC 2.0	This standard is based upon VITA 42.0 XMC. It defines an open standard for supporting high-speed, switched interconnect protocols on the existing, widely deployed XMC form factor.	ANSI/VITA Approved

Designation	Title	Abstract	VITA Status – April 2025
ANSI/VITA 65.0-2023	OpenVPX System Standard	The OpenVPX System Standard was created to bring versatile system architectural solutions to the VPX market.	ANSI/VITA Approved
ANSI/VITA 65.1-2023	OpenVPX System Standard –Profile Tables	This standard documents variations of Slot, Backplane, and Modules Profiles.	ANSI/VITA Approved
ANSI/VITA 88.0-2021	Switched Mezzanine Card Plus (XMC+) Standard	This document defines a standard for improved electrical/mechanical mezzanine connectors for XMC applications.	ANSI/VITA Approved

Table 3: SOSA - Related publications

Title / Version	Comment
SOSA Reference Architecture (C119)	SOA Reference Architecture. Technical Standard (2011)
SOSA Technical Standard Reference Architecture (S221)	The Open Group Snapshot (2022)
Technical Standard for SOSA™ Reference Architecture (S241)	The Open Group Snapshot (2024)

Table 4: VX6096 COTS - Related publications

Product	Document ID	Publication
VX6096	D304203	EFT Release Notes
VX6096	D295426	AMI-BIOS User Reference Manual
VX6096	D234669	PBIT User Guide
VPX product family	D303485	VITA 46.11 Firmware Release Note
VPX product family	D305293	Kontron VME/VPX Fedora Remix Release Notes

8.3. VPX Overview

VPX (VITA 46) specifications establish a new direction for the next revolution in bus boards. VPX is an ANSI standard which breaks out from the traditional connector scheme of VMEbus to merge the latest in connector and packaging technology with the latest in bus and serial fabric technology. VPX combines best-in-class technologies to assure a very long technology cycle similar to that of the original VMEbus solutions. Traditional parallel VMEbus will continue to be supported by VPX through bridging schemes that assure a solid migration pathway.
For further information regarding this standards and its use, visit the home page of the VITA - Open Standards, Open Markets (http://www.vita.com)

8.4. Product Overview

8.4.1. VX6096 Overview

› Intel® Core™ XEON-D-2700 or D-2800 processor series

The VX6096 computing node is a VPX computing blade for parallel data and signal processing applications. The VX6096 is the ideal building block for intensive parallel computing workloads where a cluster of VX6096is used in full mesh or switched OpenVPX environments. Target applications include radar, sonar, imaging systems, airborne fighters, and unmanned aerial vehicle (UAV) radar, as well as rugged multi-display consoles. It is also well suited for transport applications.

The processing node of the VX6096 implements Intel® Xeon® D-2700 SoC integrating high count performance Cores and a highly flexible Ethernet controller, coupled with 4 channels DDR4 memory. The highly integrated Xeon® D-2700 SoC offers numerous PCIe channels, USB and SATA channels.

Table 5: Features overview

Features overview	
SoC	
Processor	Intel® Xeon® D-27xx/D-28xx processor series
Platform Controller Hub	Integrated Intel® 500 Series Chipset Family On-Package Platform Controller Hub.
Network Accelerator Complex	Two 100/40GbE interfaces
Onboard Controllers	
Gigabit Ethernet controllers	Two Intel® i226 1GbE controllers
10GbE Ethernet controllers	One Intel® EYE810XXVAM2 dual 1G/10GbE controller
Graphics	One Silicon Motion SM768 Graphics Media Processor
RTC	Separate low power RTC RV8803
System CPLD	Power - on/ off control, Reset control, Local environmental control/monitoring, I2C, LEDs control, Serial lines multiplexer, Serial VPD and user memories, User and system GPIOs, Internal registers that allow system management Watchdog : CPLD-based, timeout ranging from 4 ms to 510s, IRQ, Reset, dual-stages
LVCMOS/EIA-232 Serial port	One LVCMOS/EIA-232 port (MP01)
Flexible serial port	One RS-422/485 port (SER01) or two RS-232 Rx/Tx ports (MP02 and SER01)
IPMC	FRU subsystem management: Local environmental control/monitoring, IPMB A/B interfaces, FRU memory, system event log.
Memory	
System Memory	Up to 128 GB quad channel DDR4 SDRAM, with ECC, soldered
Flash (uEFI BIOS)	Two 64MB boot FLASH devices, with recovery image and uEFI BIOS settings
EEPROM	Refer to section “Other Board Features” for detailed information.
F-RAM	One serial 1-Mbit dedicated to user defined data
Front Interfaces	
LEDs	Five bicolor LEDs reporting the board CPU health status and activity
Reset	Reset push button
Sensors	
Multi-sensor	NCT7802Y device offering voltage/temperature monitoring, and PECI interface
Temperature sensors	Two LM73CIM
Current sensor	One INA220 current sensor
Voltage sensor	One ADS7930 voltage sensor
Secure elements	
TPM 2.0	TPM 2.0 ST33KTPM2X32CKE3 device equipped
Onboard mezzanine slot	
XMC slot	One XMC VITA61 12mm slot offering Upstream x8 PCIe Interface up to Gen4 speed XMC IOs with XMC/VPX mapping as per the slot and module profiles defined in this document (Ask for VITA88 option)
Bottom M.2 slot option (M2B)	Bottom M.2 module option (named M2B): Type M, 22 mm x 42 mm form factor 2242 type M single or double sided module type supported

Features overview	
	Slot interface: x2 PCIe up to Gen3 (8Gb/s) or SATA link up to 6 Gb/s. The M.2 slot can optionally be used to equip a 2-D graphic module, based on the Silicon Motion SM750 graphic controller. 2242 type M single or double sided module type supported depending on the ordered variant
Top M.2 slot option (M2A)	Bottom M.2 module option (named M2A): Type M, 22 mm x 42/80 mm form factor Slot interface: x4 PCIe up to Gen3 (8Gb/s) or SATA link up to 6 Gb/s. 2242 type M single or double sided module type supported depending on the ordered variant
VPX Interface	
VPX Slot Profiles	SOSA -2 profile Compatible with the following as per Vita 65: Slot profile SLT6-PAY-4F1Q1H4U1T1S1S1TU2U2T1H-10.6.3-0 Module profile MOD6-PAY-4F1Q1H4U1T1S1S1TU2U2T1H-12.6.3-2
Rear I/O via P1&P2	Refer to the pin assignment tables in this document.
Supervisory Functions	Non Maskable RESET NVMRO, Master SMBus and Master/Slave SMBus interfaces for system management. Compatible with Kontron CMB (Monitoring Board), temperature and voltage sensors on the board
Power Supplies	On P0: VS1=VS2=12V; VS3 not used; +12V_AUX is optional in VITA 46 and not connected -12V_AUX is optional in VITA 46. It is not used internally on VX6096 3.3V_AUX is mandatory in VITA 46. However, if absent, it will be generated internally.
OS Support	Linux, ask for: Windows, VxWorks
Mechanical size	Air Flow Through : 6U x 160mm, Slot pitch 1.50 inches according to VITA 48.8 Conduction cooled: 6U x 160mm, Slot pitch 1.00 inch according to VITA 48.2

All the Flash and non-volatile memories onboard have a write protect mechanism taking into account the NVMRO (Non Volatile Memory read Only) VPX signal. For further details, see “NVMRO” section

› Software

Kontron is one of the few compact PCI, VME and VPX vendors providing in-house support for most of the industry-proven real-time operating systems that are currently available.
Thanks to its close relationship with the software editors, Kontron is able to locally produce and support BIOS, BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology which follow silicon evolution.
Finally, Kontron offers to its customers owners of a maintenance agreement a hotline software support and regular software updates.
A dedicated web site is also available for online updates and release downloads.
The VX6096 is delivered with the UEFI BIOS from AMI which supports Secure Boot and TPM. This BIOS supports PBIT Expert mode option from Kontron CMON-Line (https://kfrlabs.kontron.com/monitoring.php)
The VX6096 supports a live Linux distribution (a Fedora Core remix distribution) for instant evaluation and benchmarking. Based on Fedora Linux, it offers many turn-key features, such as Continuous BIT service (CBIT). Refer to our Kontron VME/VPX Fedora Remix Release Notes for details.
With this software image loaded on a USB stick, you get instant access to all the features of the board. The CBIT dashboard can be accessed at http://board-ip-address:8000/kehm-RESULTS.xml .

Contact Kontron for further information regarding other operating systems and software support

› Tooling Rear Transition Module

The VX6096 is compatible with the PB-VX6-0000 rear transition module.
Refer to the “RTM Characteristics” section for more information.

8.4.2. VX6096 Block Diagram

Figure 3: VX6096 - High-Level Block Diagram

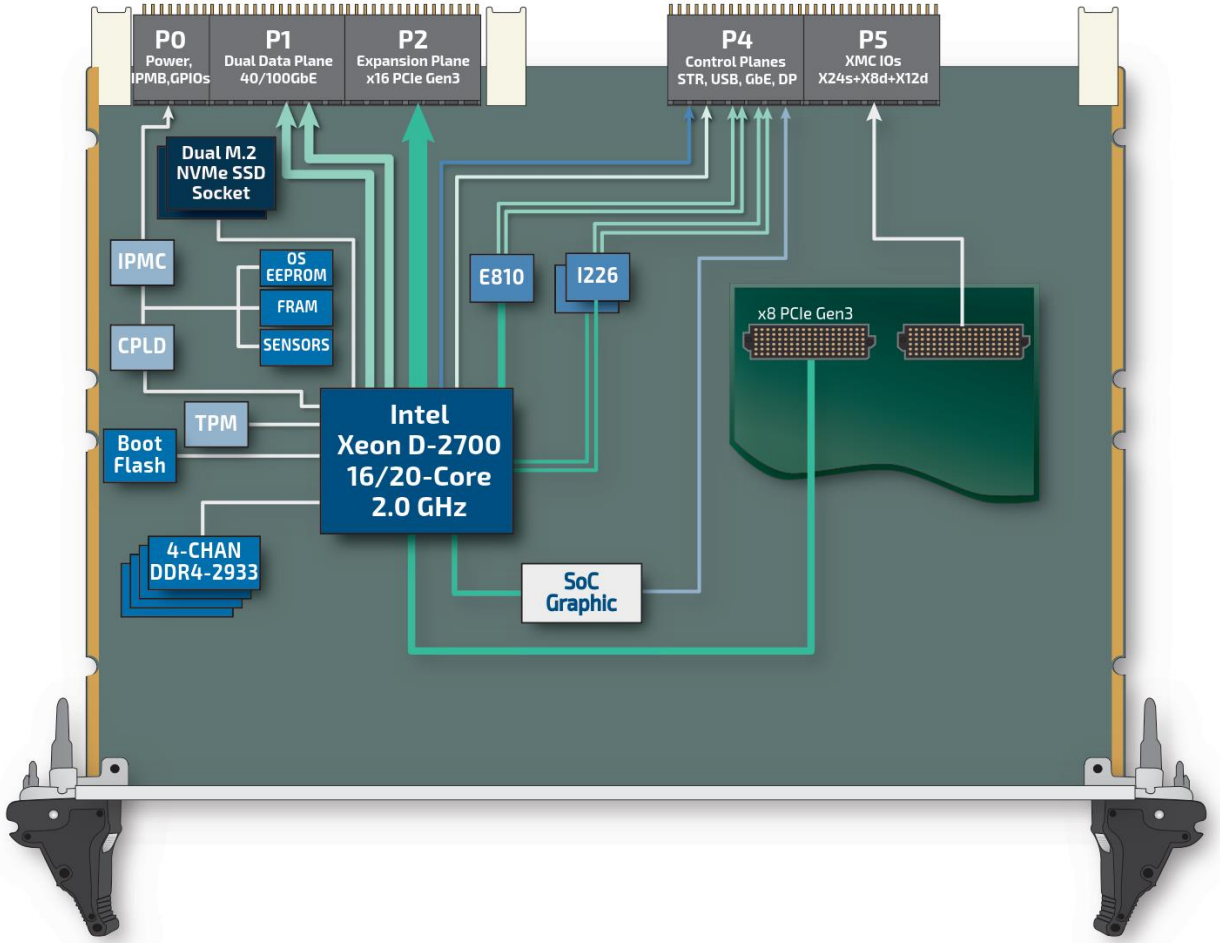
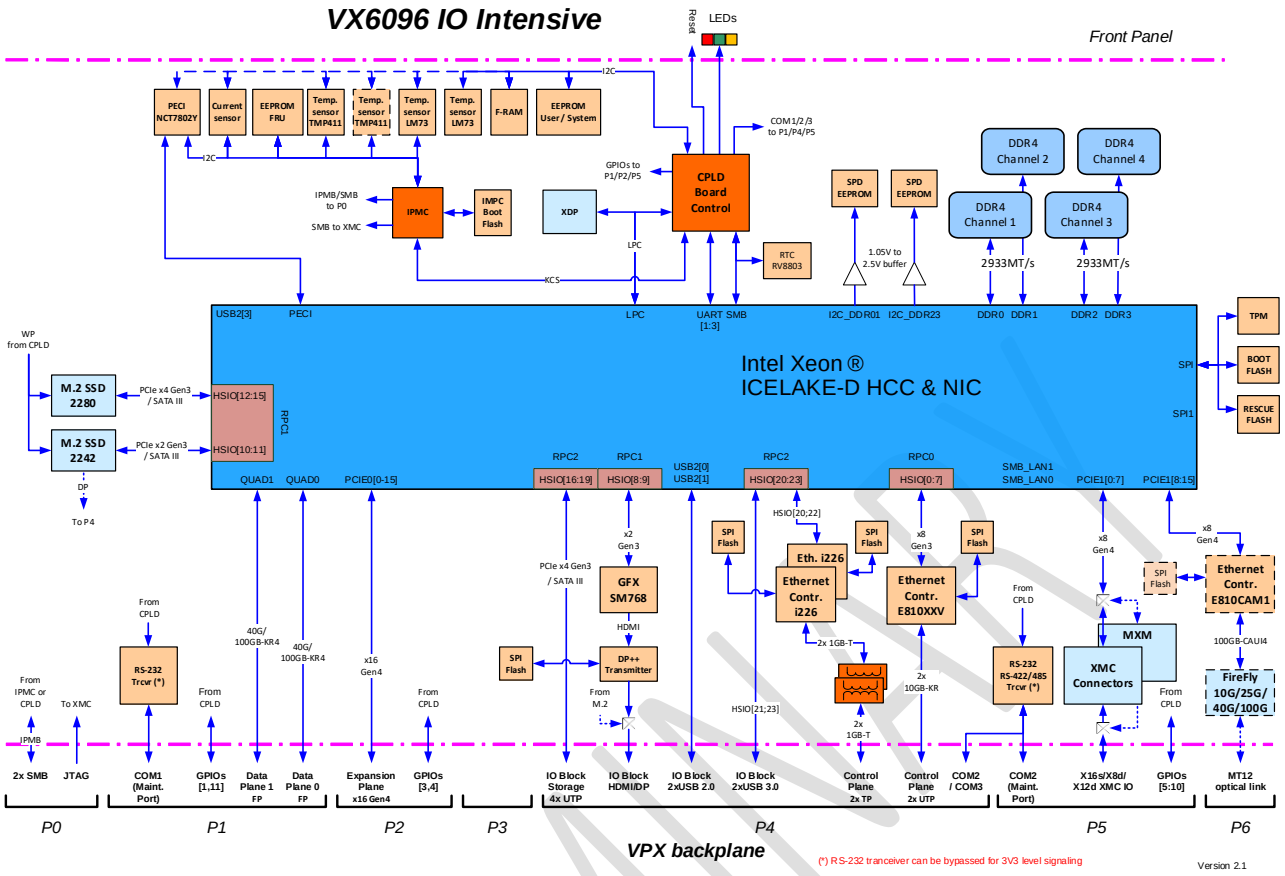


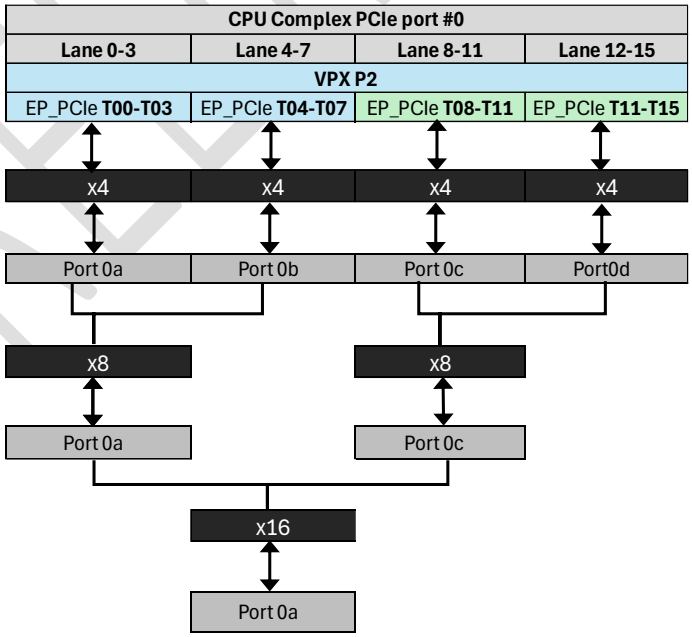
Figure 4: VX6096 - Detailed block diagram of the Compute Intensive Variant



Complex PCIe signal partitioning capability of the PCIE#0 port of the HCC Ice Lake D processor:

x16 CPU PCIe port#0 is routed to the x16 Expansion plane on the VPX P2 connector.

CPU PCIe port#0 on VPX P2 can be bifurcated as two x8 ports, four x4 ports, or any combination thereof.



CPU complex PCIe Port #0A is defined as Port #1A in BIOS
Default COTS width configuration on the VPX expansion plane is x16.

8.4.3. Components Layout

Figure 5: Components Layout (Top view)

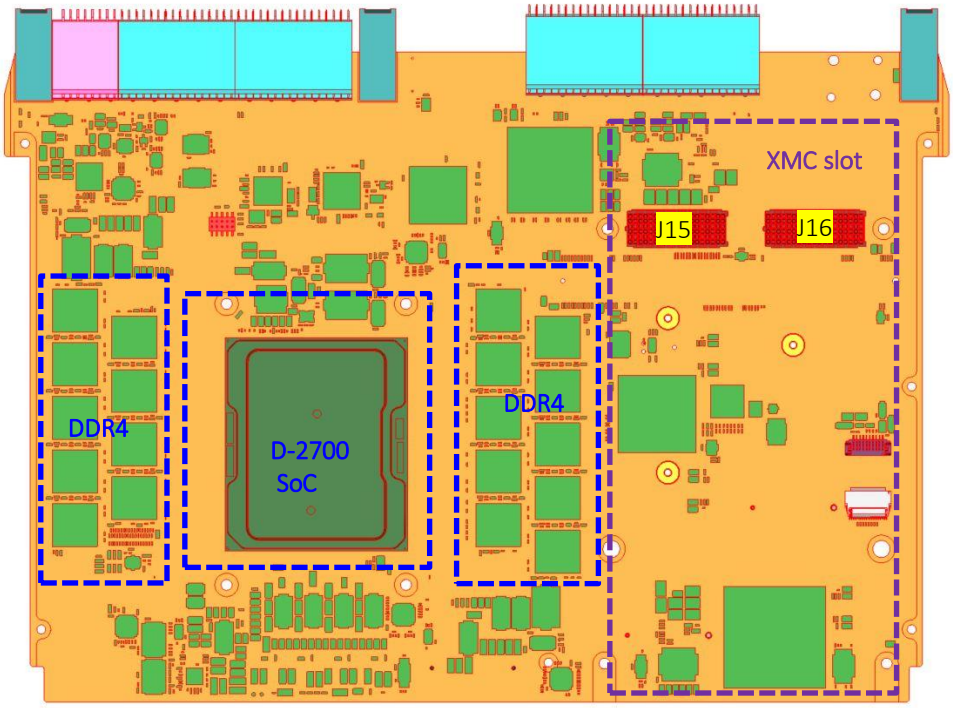
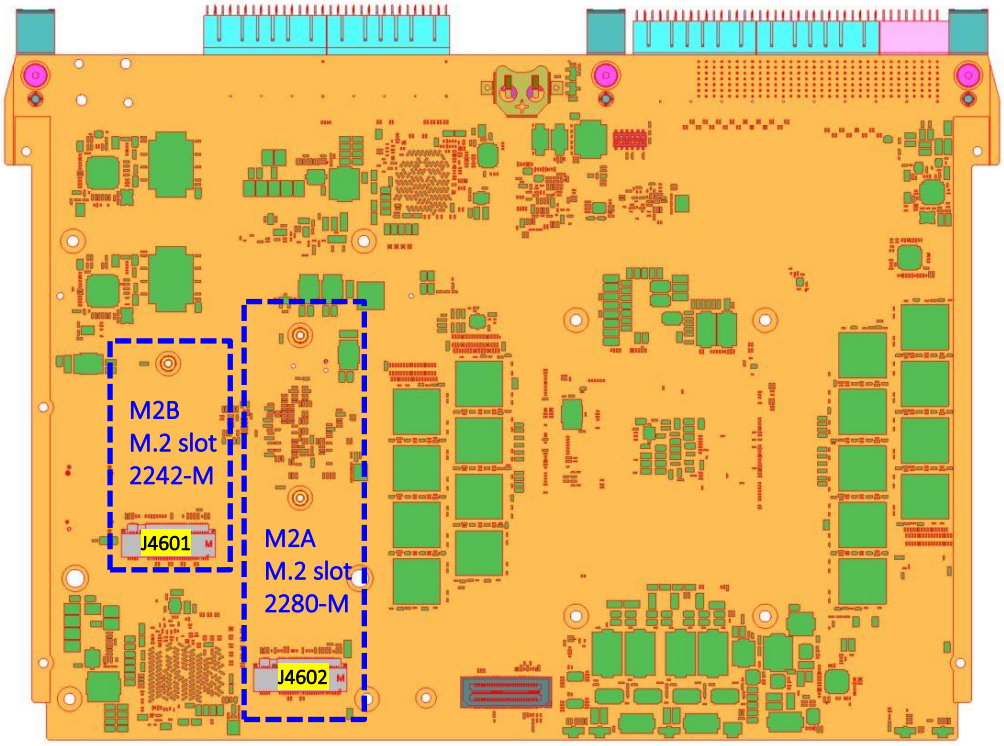


Figure 6: Components Layout (Bottom view)



9. Ordering information

9.1. VX6096 - Ordering information

Table 6: VX6096 - Order Codes

Environmental Class	Ordering Code	Commercial Code	Description
	Generic	**VX6096-vvvxxd-mcr**N000V1z [(1) (3)]	Environmental Class option (vvv): **vvv= AFT2**: 1.5" Rugged Air-Cooled 'AFT2' (-40°C to +55°C) conformal coating [(1) (3)] **vvv= AFT3:** 1.5" Rugged Air-Cooled 'AFT3' (-40°C to +70°C) conformal coating [(1) (3)] **vvv= RC3:** 1" Rugged Conduction-Cooled 'RC3' (-40°C to +70°C) conformal coating [(1) (3)]
AFT2 [(1)]	1073-3189	VX6096-AFT216H-110N000V1P	
AFT2 [(1)]	1073-5096	VX6096-AFT216H-110N000V1Q	Processor option (xx): **xx=16**: Intel(r) Xeon D-2775TE Processor, 100W TDP @Base Freq. 2GHz, 16 cores **xx=20**: Intel(r) Xeon D-2796TE Processor, 118W TDP @Base Freq. 2GHz, 20 cores **xx=21**: Intel(r) Xeon D-2896TER Processor, 110W TDP @Base Freq. 2GHz, 20 cores
RC3 [(1)]	1073-3190	VX6096-RC316H-110N000V1P	Memory DDR4 option (d): **d= H**: 64 GB soldered SDRAM with ECC **d= I**: 128 GB soldered SDRAM with ECC Mezzanine Slot option (m): **m= 0**: No mezzanine slot **m= 1**: XMC Mezzanine on x8 PCIe (VITA61, up to Gen4) **m= 2**: XMC Mezzanine on x8 PCIe (VITA42, up to Gen4)
RC3 [(1)]	1073-5097	VX6096-RC316H-110N000V1Q	
RC3 [(1)]	1073-5098	VX6096-RC320I-110N000V1P	Covers Option (c): **c= 0:** no VITA 48 2LM covers **c=1**: VITA 48 2LM covers
RC3 [(1)]	1073-5099	VX6096-RC320I-110N000V1Q	Rear I/O Profile option (r): **r=0:** Slot profile : SLT6-PAY-4F1Q1H4U1T1S1S1TU2U2T1H-10.6.3-0, Module profile : MOD6-PAY-4F1Q1H4U1T1S1S1TU2U2T1H-12.6.3-2 Software option (z): **z=0**: No PBIT **z=P**: Power on Built in Test Run Time **z=Q**: PBIT RT & Preloaded Linux on Eval M.2 320GB SSD **Other options** No Front I/O connectors, First 2242/2280 M.2 slot (bottom) : x4 PCIe Gen3, up to D3 and M Key Second 2242 M.2 slot (bottom) : x2 PCIe Gen3, up to D3 and M Key, RTC Power sourced from system VPX VBAT, VITA 46.11 Support, TPM 2.0 Secure element Conformal Coating [(2)]

Note (1): Order codes restricted to an EVAL/ Lab-grade use case. EVAL products are not qualified against the AFT2 class.
Note (2): Conformal coating is present on qualified products. Early prototypes or unqualified products may be delivered without conformal coating.
Note (3): The maximum temperature allowed is processor TDP dependent.

9.2. RTM - Ordering information

Table 7: RTM - Order Codes

Standard Order Codes	Description
PB-VX6-0000	6U single slot 5 HP (1.0") VPX Rear Transition Module (RTM) providing serial lines for standard VX6096 boards. Tooling equipment for lab use.

Detailed information about the RTM module can be found in the “RTM compatible with the VX6096” section

10. Environmental Specifications

The applicable environment class depends on the ordered VX6096 variant

Table 8: Environmental Specifications - Rugged classes

Environmental class	AFT2/AFT3 Class (4) Rugged Air-cooled	RC3 Class (4) Rugged Conduction cooled
Plugin unit type	6U VPX Module Vita 46.0 specification, corrected by REDI VITA 48.8 December 2022 (7.5HP)	5HP, Type 2, secondary side retainers, REDI VITA 48.2-2022 (7.5HP)
Conformal Coating	Standard	Standard
Airflow	Refer to "Thermal Performance "section	NA
Cooling Method	Air Flow Through	Conduction - Refer to "Thermal Performance "section
Operating	AFT2: Inlet air temperature from -40 °C to +55 °C (1) (2) (3) AFT3: Inlet air temperature from -40 °C to +70 °C (1) (2) (3)	Card edge temperature from -40 °C to +70 °C (2) (3)
Storage (1)	-50 °C to +100 °C	-50 °C to +100 °C
Vibration Sine (Operating)	1 hour per axis: 5-20 Hz, displacement 2.5 mm 20-2000 Hz, 5 g	1 hour per axis: 5-20 Hz, displacement 2.5 mm 20-2000 Hz, 5 g
Random (Operating)	Product withstand vibration as defined below, 1 hour per axis: 5 Hz to 100 Hz PSD increasing at +3 dB/octave 100 Hz to 1000 Hz PSD = 0.1 g^2/Hz 1000 Hz to 2000 Hz PSD decreasing at -6 dB/octave	Product withstand vibration as defined below, 1 hour per axis: 5 Hz to 100 Hz PSD increasing at +3 dB/octave 100 Hz to 1000 Hz PSD = 0.1 g^2/Hz 1000 Hz to 2000 Hz PSD decreasing at -6 dB/octave
Shock (Operating)	40 g / 11 ms, half sine	40 g / 11 ms, half sine
Altitude (Operating)	-1,500 to 60,000 ft	-1,500 to 60,000 ft
Relative Humidity	95 % without condensation	95 % without condensation

(1) According to Thermal characterization performed in laminar flow bench following Kontron procedure.

(2) The maximum allowed temperature depends on the processor TDP.

(3) Refer to the Intel EDS documents for detailed information about DTR = Dynamic Temperature Range limitations. The default maximum processor temperature range during operation is ±145°C, starting from boot time temperature, with CPU PCIe Gen3 and PCH PCIe/SATA Gen2 speed limitations. For more information, contact Kontron Support.

(4) Severity levels applicable to the baseboard without any M.2 or any XMC module equipped on the board. Ask Kontron for product variants with M.2 or XMC module options equipped.

Table 9: Lab-grade Environmental Specifications for Prototypes, EFT or EVAL Variants

Lab-grade air-cooled version (1.5" single height passive module heat sink, forced air)	
Conformal Coating	optional
Inlet Airflow	3 m/s
Cooling Method	Convection or conduction
Operating	10 °C to +30 °C
Known product limitations	Refer to the active release note for detailed information. Ask Kontron.
Other specifications	According to standard lab conditions The use case as per EU directive is applicable: custom built evaluation kits destined for professionals to be used solely at research and development facilities for such purposes

Lab-grade conduction cooled version	
Conformal Coating	Optional
Cooling Method	Conduction
Max card edge Operating Temperature	0 °C to +30 °C
Known product limitations	Refer to the active release note for detailed information. Ask Kontron.
Other specifications	According to standard lab conditions The use case as per EU directive is applicable: custom built evaluation kits destined for professionals to be used solely at research and development facilities for such purposes

11. Board Weight/Mass

Table 10: Board Weight / Mass

Mass	
VX6096-AFT216H-110N000V1P Without XMC or M.2 module installed	~ 1.7 kg
VX6096-RC16H-110N000V1P Without XMC or M.2 module installed	~ 1.3 kg

12. MTBF

Table 11: MTBF

MTBF at sea level Calculations according to MIL-HDBK-217F Notice 2 and ANSI/VITA 51.1-2008, corrected by Kontron field data	GB (Hours)	
	25 °C	40 °C
VX6096-AFT216H-110N000V1P Without XMC or M.2 module installed	423 425	364 561
VX6096-RC16H-110N000V1P Without XMC or M.2 module installed	422 996	363 901

Ask Kontron for MTBF values related to other or custom mission profiles.

13. Mechanical Specifications

Figure 7: AFT board outlines

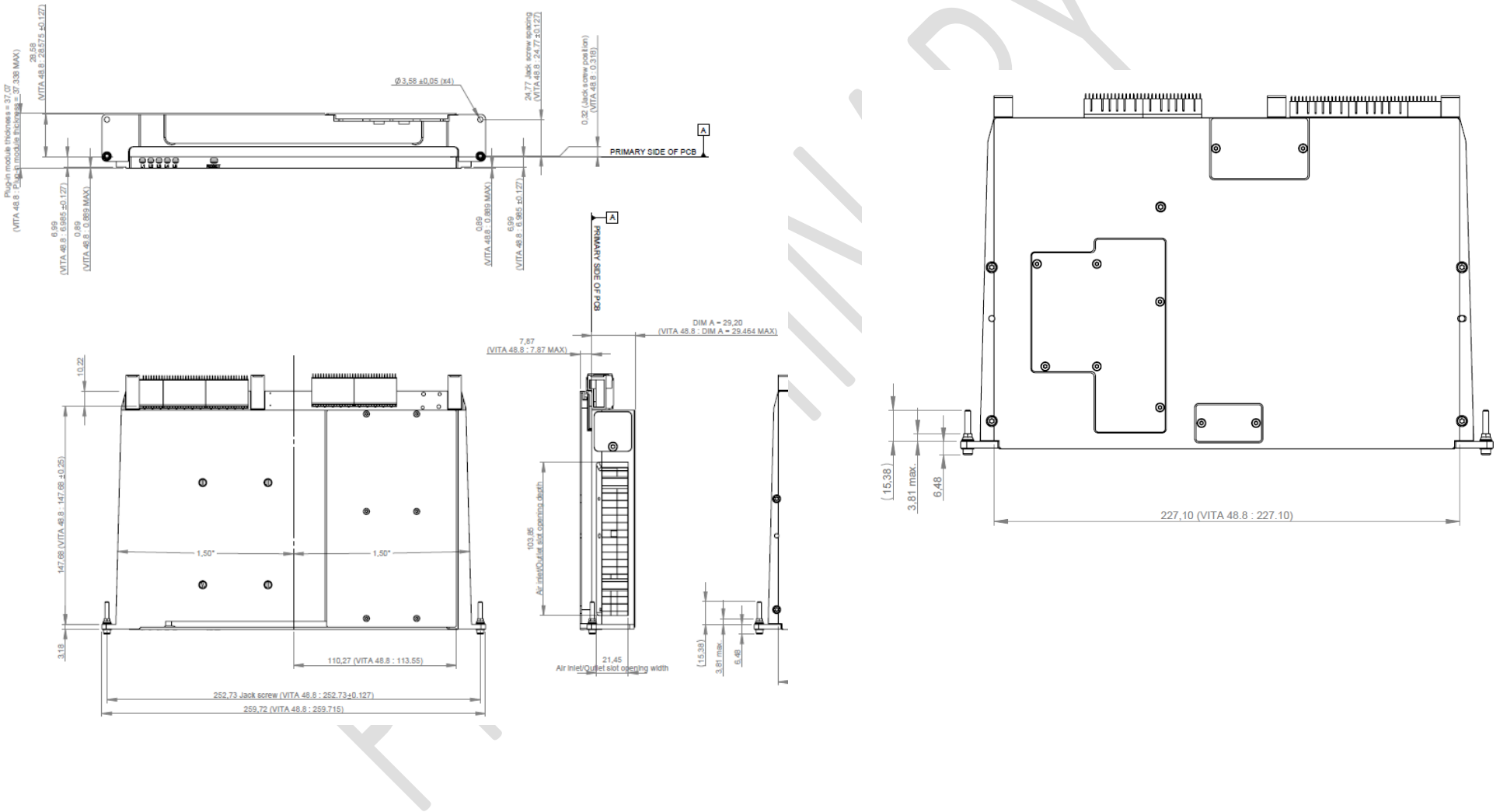
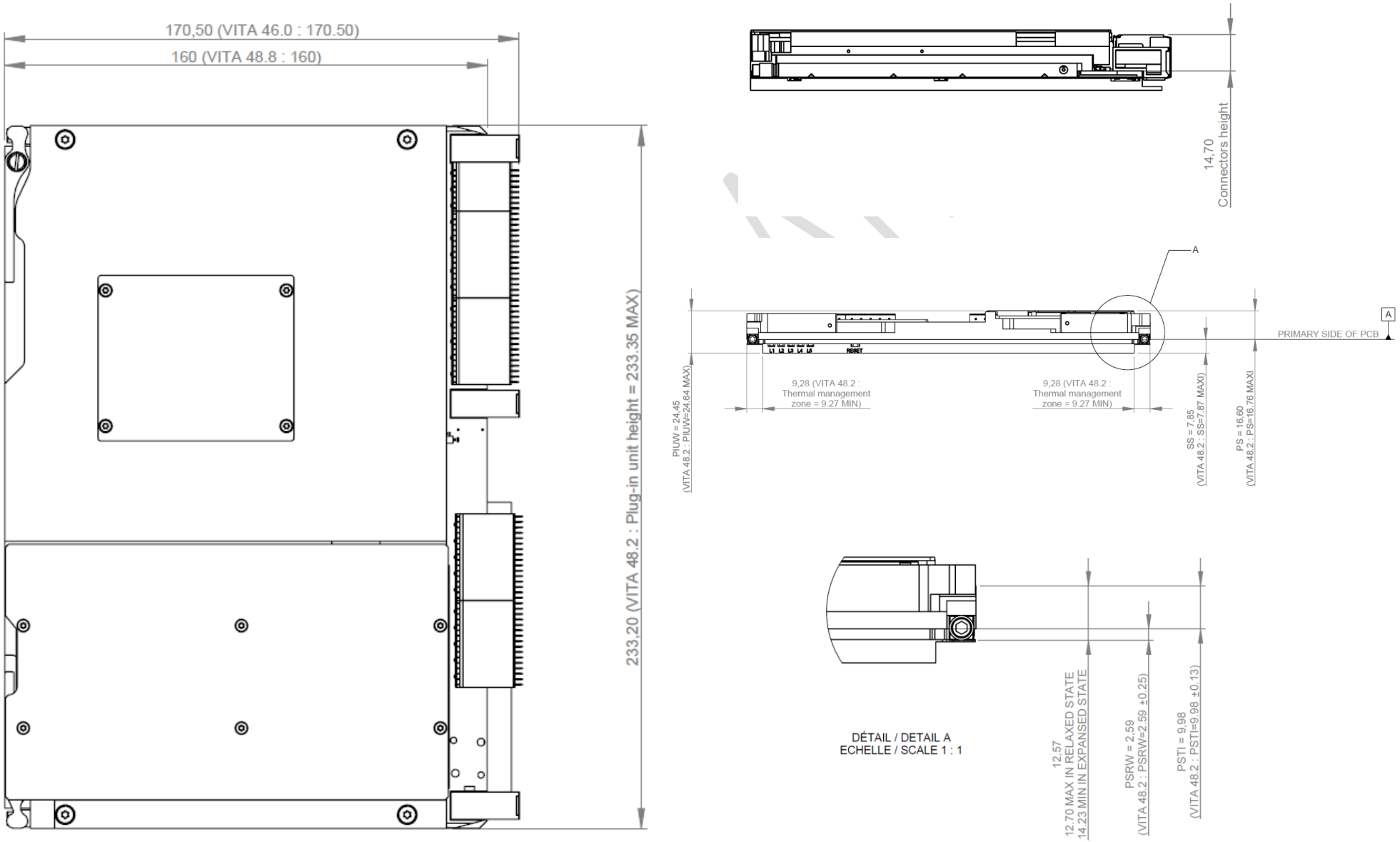


Figure 8: RC Board outlines



14. Physical IO

14.1. Front panel overview

Figure 9: AFT variant - Front Panel with LED indicators and reset button

Figure 10: RC variant - Front Panel with LED indicators and reset button

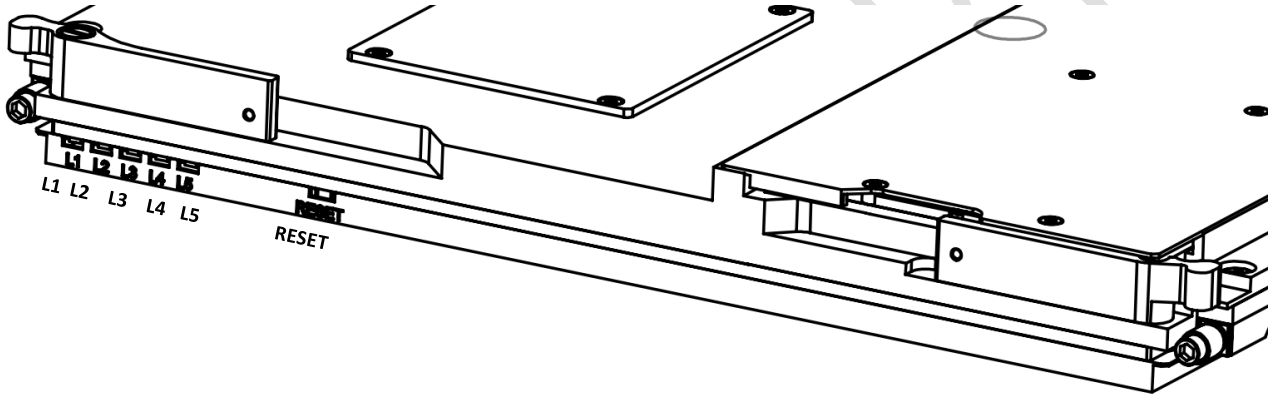


Table 12: Front Panel - Interfaces

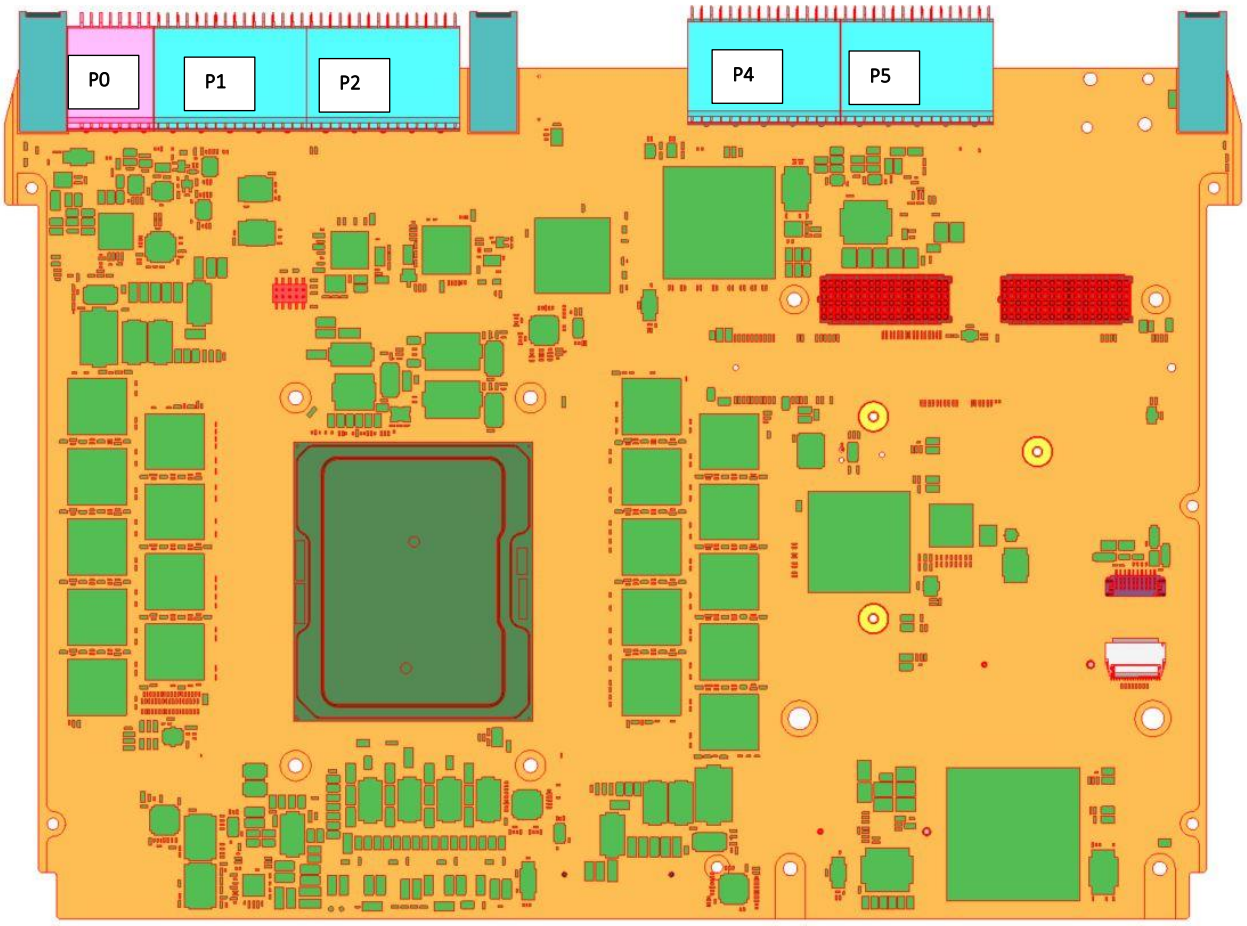
FUNCTION	DESCRIPTION	SEE ALSO
RST	Reset push button	Front Interfaces
L 1 to L5	LED indicators reporting the board CPU health status and activity	Refer to the “LEDs” Section

The front panel push button must be handled with care. Use a non-metallic and blunt tool with a rounded tip (tip diameter must be roughly equal to the front panel button surface)

14.2. VPX Connectors

The complete 6U VPX connectors configuration comprises three connectors named P0 to P5

Figure 11: VPX Connectors



14.2.1. VPX P0 Connector

Table 13: VPX Connector P0 Wafer Assignment

P0	G	F	E	D	C	B	A
1	VS1 (+12V)	VS1 (+12V)	VS1 (+12V)	NC	NC (VS2)	NC (VS2)	NC (VS2)
2	VS1 (+12V)	VS1 (+12V)	VS1 (+12V)	NC	NC (VS2)	NC (VS2)	NC (VS2)
3	NC (VS3)	NC (VS3)	NC (VS3)	NC	NC (VS3)	NC (VS3)	NC (VS3)
4	IMPB B _CLK	IMPB B _DAT	GND	-12V_AUX	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3V3_AUX	GND	IMPB A_CLK	IMPB A _DAT
6	GA3*	GA2*	GND	NC (+12V_AUX)	GND	GA1*	GA0*
7	TCK	GND	TDO	TDI	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND

* signal active when low

REF_CLK-/+: 25MHz and 100MHz clock manufacturing options are available. Contact Kontron. Default is the 25MHz standard option.

Table 14: VPX Connector P0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
VS1 and VS2 (+12V)	+12 Volts DC power (VPX supply).
-12V_AUX	-12 Volts auxiliary power. Only used to supply XMC if needed.
3V3_AUX	+3.3 Volts auxiliary power. Not required because it generate internally is 3V3_AUX power rail is not present on the backplane.
NVMRO	Non-Volatile Memory Read Only. When asserted (logical 1), prevents any non-volatile memory from being updated.
GAi	Geographical address pins
GAP	Geographical address parity
GND	Ground
IPMB A	I2C Bus 0
IPMB B	I2C Bus 1
REF_CLK+/-	The Reference Clock is a bussed differential pair. Output if the VX6096 is plugged in the system controller slot, input otherwise. It enables the entire system to synchronize to a common time reference if desired. Counter/timer in the CPLD can use this clock
AUX_CLK+/-	1 PPS (one pulse per second) clock input. Can be programmed as an output on system controller slot. Can be used to phase the CPLD timer/counter clocked by REF_CLK+/-.
SYSRESET*	System Reset. Input and open collector output.
NC	“Not connected”

14.2.2. VPX P1 Connector

Table 15: VPX Connector P1 Wafer Assignment

P1	G	F	E	D	C	B	A
1	Gdiscrete 1	GND	DP01 T0-	DP01 T0+	GND	DP01 R0-	DP01 R0+
2	GND	DP01 T1-	DP01 T1+	GND	DP01 R1-	DP01 R1+	GND
3	P1-VBAT	GND	DP01 T2-	DP01 T2+	GND	DP01 R2-	DP01 R2+
4	GND	DP01 T3-	DP01 T3+	GND	DP01 R3-	DP01 R3+	GND
5	SYS_CON*	GND	DP02 T0-	DP02 T0+	GND	DP02 R0-	DP02 R0+
6	GND	DP02 T1-	DP02 T1+	GND	DP02 R1-	DP02 R1+	GND
7	GPIO01	GND	DP01 T2-	DP01 T2+	GND	DP01 R2-	DP02 R2+
8	GND	DP02 T3-	DP02 T3+	GND	DP02 R3-	DP02 R3+	GND
9	MP01-TD	GND	NC	NC	GND	NC	NC
10	GND	NC	NC	GND	NC	NC	GND
11	MP01-RD	GND	NC	NC	GND	NC	NC
12	GND	NC	NC	GND	NC	NC	GND
13	GPIO02	GND	NC	NC	GND	NC	NC
14	GND	NC	NC	GND	NC	NC	GND
15	Msk RST (GPIO 11)	GND	NC	NC	GND	NC	NC
16	GND	NC	NC	GND	NC	NC	GND

* signal active when low

The ordered product manufacturing options may alter the VPX P1 pin assignment. Contact Kontron.

Table 16: VPX Connector P1 Signal Definition

MNEMONIC	SIGNAL DEFINITION
DPxx	100/40GBASE-KR4 Ethernet links
Gdiscrete1	Open VPX Gdiscrete1 signal
GPIO01	General Purpose I/O 1 (handled by the CPLD)
Msk RST (GPIO 11)	Reset input or Optional general purpose I/O (handled by CPLD) (may be left unconnected if not used).
GND	Ground
SYS_CON	System Controller Slot Indication
P1-VBAT	Source for RTC backup voltage, from the VPX 3.3V_AUX rail or from the VPX P1-G3 VBAT rail
MP01-xx	Maintenance Port 1: serial Lines EIA-232 or 3V3 signal leveling

14.2.3. VPX P2 Connector

Table 17: VPX Connector P2 Wafer Assignment

P2	G	F	E	D	C	B	A
1	AXreset1*	GND	EP T00-	EP T00+	GND	EP R00-	EP R00+
2	GND	EP T01-	EP T01+	GND	EP R01-	EP R01+	GND
3	AXreset3*	GND	EP T02-	EP T02+	GND	EP R02-	EP R02+
4	GND	EP T03-	EP T03+	GND	EP R03-	EP R03+	GND
5	GPlvds01-	GND	EP T04-	EP T04+	GND	EP R04-	EP R04+
6	GND	EP T05-	EP T05+	GND	EP R05-	EP R05+	GND
7	GPlvds01+	GND	EP T06-	EP T06+	GND	EP R06-	EP R06+
8	GND	EP T07-	EP T07+	GND	EP R07-	EP R07+	GND
9	GPlvds02-	GND	EP T08-	EP T08+	GND	EP R08-	EP R08+
10	GND	EP T09-	EP T09+	GND	EP R09-	EP R09+	GND
11	GPlvds02+	GND	EP T10-	EP T10+	GND	EP R10-	EP R10+
12	GND	EP T11-	EP T11+	GND	EP R11-	EP R11+	GND
13	GPIO03	GND	EP T12-	EP T12+	GND	EP R12-	EP R12+
14	GND	EP T13-	EP T13+	GND	EP R13-	EP R13+	GND
15	GPIO04	GND	EP T14-	EP T14+	GND	EP R14-	EP R14+
16	GND	EP T15-	EP T15+	GND	EP R15-	EP R15+	GND

* signal active when low

The ordered product manufacturing options may alter the VPX P2 pin assignment. Contact Kontron.

Table 18: VPX Connector P2 Signal Definition

MNEMONIC	SIGNAL DEFINITION
EP Txx/Rxx	Expansion plane PCIe interface, up to Gen4
AXresetxx	Reserved for VITA 66 manufacturing options – Contact Kontron
GPlvdsxx	LVDS General purpose IO according to the VITA standards
GPIOxx	General purpose input/output according to the VITA standards
GND	Ground

14.2.4. VPX P4 Connector

Table 19: VPX Connector P4 Wafer Assignment

P4	G	F	E	D	C	B	A
1	**SER01-TX-**	GND	STR01 T-	STR01 T+	GND	STR01 R-	STR01 R+
2	GND	STR02 T-	STR02 T+	GND	STR02 R-	STR02 R+	GND
3	**SER01-TX+**	GND	STR03 T-	STR03 T+	GND	STR03 R-	STR03 R+
4	GND	STR04 T-	STR04 T+	GND	STR04 R-	STR04 R+	GND
5	**VID01-PWR**	GND	VID D1-	VID D1+	GND	VID D0-	VID D0+
6	GND	VID D3-	VID D3+	GND	VID D2-	VID D2+	GND
7	**VID01-HPD**	GND	VID AUX-	VID AUX+	GND	GPlvds03-	GPlvds03+
8	GND	USB02 SST-	USB02 SST+	GND	USB02 SSR-	USB02 SSR+	GND
9	**USB01 VBUS**	GND	USB02 D-	USB02 D+	GND	USB01 D-	USB01 D+
10	GND	USB01 SST-	USB01 SST+	GND	USB01 SSR-	USB01 SSR+	GND
11	**USB02-VBUS**	GND	CPutp02 T-	CPutp02 T+	GND	CPutp02 R-	CPutp02 R+
12	GND	CPutp01 T-	CPutp01 T+	GND	CPutp01 R-	CPutp01 R+	GND
13	**SER01-RX-**	GND	CPtp02 DB-	CPtp02 DB+	GND	CPtp02 DA-	CPtp02 DA+
14	GND	CPtp02 DD-	CPtp02 DD+	GND	CPtp02 DC-	CPtp02 DC+	GND
15	**SER01-RX+**	GND	CPtp01 DB-	CPtp01 DB+	GND	CPtp01 DA-	CPtp01 DA+
16	GND	CPtp01 DD-	CPtp01 DD+	GND	CPtp01 DC-	CPtp01 DC+	GND

* signal active when low

The ordered product manufacturing options may alter the VPX P4 pin assignment.
Contact Kontron.

Table 20: VPX Connector P4 Signal Definition

MNEMONIC	SIGNAL DEFINITION
STRxx	SATA / Storage ports
VIDxx	Display Port 1.2 video link
USB02_SSxx	USB3.0 Gen1 Super Speed port
USBxx D	USB2 ports with VBUS
CPutpxx	UTP Ethernet ports (1GBase-KX/10GBase-KR)
CPtpxx	TP Ethernet ports 1000Base-T
SER01	Multi-protocol Rx/Tx Serial port (RS-232, RS-422/485)
GPlvdsxx	LVDS General Purpose I/O (handled by the CPLD)
GND	Ground

14.2.5. VPX P5 Connector

Table 21: VPX Connector P5 Wafer Assignment

P5	G	F	E	D	C	B	A
1	**MP02 TD-**	GND	XMC-J16-C8	XMC-J16-C9	GND	XMC-J16-F8	XMC-J16-F9
2	GND	XMC-J16-C10	XMC-J16-C11	GND	XMC-J16-F10	XMC-J16-F11	GND
3	**MP02 RD**	GND	XMC-J16-C12	XMC-J16-C13	GND	XMC-J16-F12	XMC-J16-F13
4	GND	XMC-J16-C14	XMC-J16-C15	GND	XMC-J16-F14	XMC-J16-F15	GND
5	**GPIO05**	GND	XMC-J16-C16	XMC-J16-C17	GND	XMC-J16-F16	XMC-J16-F17
6	GND	XMC-J16-C18	XMC-J16-C19	GND	XMC-J16-F18	XMC-J16-F19	GND
7	**GPIO6**	GND	XMC-J16-A1	XMC-J16-B1	GND	XMC-J16-D1	XMC-J16-E1
8	GND	XMC-J16-A3	XMC-J16-B3	GND	XMC-J16-D3	XMC-J16-E3	GND
9	**GPIO7**	GND	XMC-J16-A11	XMC-J16-B11	GND	XMC-J16-D11	XMC-J16-E11
10	GND	XMC-J16-A13	XMC-J16-B13	GND	XMC-J16-D13	XMC-J16-E13	GND
11	**GPIO8**	GND	XMC-J16-A5	XMC-J16-B5	GND	XMC-J16-D5	XMC-J16-E5
12	GND	XMC-J16-A7	XMC-J16-B7	GND	XMC-J16-D7	XMC-J16-E7	GND
13	**GPIO9**	GND	XMC-J16-A9	XMC-J16-B9	GND	XMC-J16-D9	XMC-J16-E9
14	GND	XMC-J16-A15	XMC-J16-B15	GND	XMC-J16-D15	XMC-J16-E15	GND
15	**GPIO10**	GND	XMC-J16-A17	XMC-J16-B17	GND	XMC-J16-D17	XMC-J16-E17
16	GND	XMC-J16-A19	XMC-J16-B19	GND	XMC-J16-D19	XMC-J16-E19	GND

* signal active when low

The ordered product manufacturing options may alter the VPX P2 pin assignment.
Contact Kontron.

Table 22: VPX Connector P5 Signal Definition

MNEMONIC	SIGNAL DEFINITION
MP02	Maintenance Port 2: serial Lines EIA-232 or 3V3 signal leveling
GPIOx	General Purpose I/O (handled by the CPLD)
XMC-xx	XMC IOs connected to the XMC-J16 connector
GND	Ground

14.3. Optional - XMC J15/J16 Connector Pin Assignments

The XMC J15 and J16 connector location can be found in the “Components Layout” Section

Table 23: Pin Assignmeent - XMC J15

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR (1)
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR (1)
4	GND	GND	TCK	GND	GND	N.C.
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR (1)
6	GND	GND	TMS	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR (1)
8	GND	GND	TDI	GND	GND	-12V
9	Reserved	Reserved	NC	Reserved	Reserved	VPWR (1)
10	GND	GND	TDO	GND	GND	GA0
11	PER0p0	PER0n0	MBIST	PER0p1	PER0n1	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PER0p2	PER0n2	3.3V AUX	PER0p3	PER0n3	VPWR (1)
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	NC	PER0p5	PER0n5	VPWR (1)
16	GND	GND	NVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	NC	PER0p7	PER0n7	NC
18	GND	GND	NC	GND	GND	NC
19	REFCLK+0	REFCLK-0	NC	WAKE#	N.C.	NC

(1) VPWR is connected to +12V via a fuse.

Signals active when low.

Table 24: XMC J15 Signal Description

MNEMONIC	DIRECTION	SIGNAL DEFINITION
VPWR	O	+12 Volts DC power pin.
+12V	O	+12 Volts DC power pin.
-12V	O	-12 Volts DC power pin.
3.3V	O	+3.3 Volts DC power pin.
3.3V AUX	O	Auxiliary +3.3 Volts.
GA[0..2]	O	I2C channel select as per VITA42.0.
GND	-	Ground
MRSTI#*	O	XMC Reset In as per VITA42.0 (10 ms pulse min.) and PCIe PERST# as per VITA42.3.
MSDA	I/O	I2C serial data as per VITA42.0.
MSCL	O	I2C serial clock as per VITA42.0.
MPRESENT#	O	Module present as per VITA42.0.
NC	-	Not Connected
RFU	-	Reserved
NVMRO	O	XMC Write Prohibit as per VITA42.0.
TCK	O	JTAG Clock as per VITA42.0.
TDI	O	JTAG Data In as per VITA42.0.
TD0	I	JTAG Data Out as per VITA42.0.
TMS	O	JTAG Mode Select as per VITA42.0.
TRST#	O	JTAG Reset as per VITA42.0.
PETxx	I/O	PCIe x8 differential transmit/receive pairs (as per VITA42.3)
REFCLK+/-0	O	100MHz PCIe differential reference clock as per VITA42.3.
WAKE#	I	Open drain WAKE# signal.

Table 25: Pin Assignmeent - XMC J16

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	XMCIO-DP0+	XMCIO-DP0-	NC	XMCIO-DP01+	XMCIO-DP01-	NC
2	GND	GND	NC	GND	GND	NC
3	XMCIO-DP02+	XMCIO-DP02-	NC	XMCIO-DP03+	XMCIO-DP03-	NC
4	GND	GND	NC	GND	GND	NC
5	XMCIO-DP04+	XMCIO-DP04-	NC	XMCIO-DP05+	XMCIO-DP05-	NC
6	GND	GND	NC	GND	GND	NC
7	XMCIO-DP06+	XMCIO-DP06-	NC	XMCIO-DP07+	XMCIO-DP07-	NC
8	GND	GND	XMCIO-SE23	GND	GND	XMCIO-SE24
9	XMCIO-DP08+	XMCIO-DP08-	XMCIO-SE21	XMCIO-DP09+	XMCIO-DP09-	XMCIO-SE22
10	GND	GND	XMCIO-SE19	GND	GND	XMCIO-SE20
11	XMCIO-DP10+	XMCIO-DP10-	XMCIO-SE17	XMCIO-DP11+	XMCIO-DP11-	XMCIO-SE18
12	GND	GND	XMCIO-SE15	GND	GND	XMCIO-SE16
13	XMCIO-DP12+	XMCIO-DP12-	XMCIO-SE13	XMCIO-DP13+	XMCIO-DP13-	XMCIO-SE14
14	GND	GND	XMCIO-SE11	GND	GND	XMCIO-SE12
15	XMCIO-DP14+	XMCIO-DP14-	XMCIO-SE09	XMCIO-DP15+	XMCIO-DP15-	XMCIO-SE10
16	GND	GND	XMCIO-SE07	GND	GND	XMCIO-SE08
17	XMCIO-DP16+	XMCIO-DP16-	XMCIO-SE05	XMCIO-DP17+	XMCIO-DP17-	XMCIO-SE06
18	GND	GND	XMCIO-SE03	GND	GND	XMCIO-SE04
19	XMCIO-DP18+	XMCIO-DP18-	XMCIO-SE01	XMCIO-DP19+	XMCIO-DP19-	XMCIO-SE02

Table 26: XMC J16 Signal Description

MNEMONIC	DIRECTIO	SIGNAL DEFINITION
XMCIO DPn+/-	I/O	XMCIO differential pair n.
XMCIO SEn	I/O	XMCIO single-ended signal n.
NC	-	Not Connected

14.4. M.2 Connector Pin Assignments

VX6096 offers two M.2 sockets named M2A and M2B. The M.2 sockets are used to connect M.2 modules, key M for storage. PCIe or SATA mode can be selected using BIOS settings, and according to the product options.

Refer to VX6096 Software release notes. The M2B socket support up to 2280 form factor.

The XMC J15 and J16 connector location can be found in the “Components Layout” Section

Table 27: M.2 socket connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	3V3
3	GND	4	3V3
5	PER3- (M2A slot only)	6	NC
7	PER3+ (M2A slot only)	8	NC
9	GND	10	DAS/DSS#LED1#
11	PET3- (M2A slot only)	12	3V3
13	PET3+ (M2A only)	14	3V3
15	GND	16	3V3
17	PER2- (M2A slot only)	18	3V3
19	PER2+ (M2A slot only)	20	NC
21	GND	22	NC
23	PET2- (M2A slot only)	24	NC
25	PET2+ (M2A slot only)	26	NC
27	GND	28	NC
29	PER1-	30	**Optional WP# (manufacturing option)**
31	PER1+	32	NC
33	GND	34	NC
35	PET1-	36	NC
37	PET1+	38	DEVSLP
39	GND	40	NC
41	PER0-/SATA-B+	42	NC
43	PER0+/SATA-B-	44	NC
45	GND_45	46	NC
47	PET0-/SATA-A-	48	NC
49	PET0+/SATA-A+	50	PERST#
51	GND_51	52	CLKREQ#
53	REFCLK_N	54	PEWAKE#
55	REFCLK_P	56	NC
57	GND	58	**Optional WP# (manufacturing option)**
59	CONNECTOR_KEY	60	CONNECTOR_KEY
61	CONNECTOR_KEY	62	CONNECTOR_KEY
63	CONNECTOR_KEY	64	CONNECTOR_KEY
65	CONNECTOR_KEY	66	CONNECTOR_KEY
67	NC	68	SUSCLK
69	PEDET	70	3V3_70
71	GND_71	72	3V3_72
73	GND_73	74	3V3_74
75	GND_75		

Table 28: M.2 Module Socket Signal Description

MNEMONIC	DIRECTIO	SIGNAL DEFINITION
3.3V	O	I
GND	-	Logic ground.
LED1# / DAS_DSS#	I	- PCI Express: LED_1# indicator as per PCI Express M.2 specification. - SATA: Device Activity Signal /Disable Staggered Spinup as per SATA 3.2. DAS is not connected to a LED (which is the main purpose of this signal) and DSS is not used since the devices are SSD and not hard drives (no spinup). Signal connected to dedicated CPLD
PEDET	I	PEDET (PCI Express Detect) as per PCI Express M.2 specification is driven low by SATA modules and high-Z by PCI Express modules (seen as a logic 1 due to on-board pull-up resistor). This signal is connected to a dedicated CPLD pin.
PERn+/- SATA-B+/-	I	- PCI Express: Receive differential pair as per PCI Express M.2 & PCI Express 3.0 specifications. - SATA: Receive differential pair as per SATA 3.2.
PERST#	O	- PCI Express: PCI Express PERST# as per PCI Express M.2 specification, handled by CPLD. - SATA: NC.
PETn+/- SATA-A+/-	O	- PCI Express: Transmit differential pair as per PCI Express M.2 & PCI Express 3.0 specifications. - SATA: Transmit differential pair as per SATA 3.2.
PEWAKE#	I/O	- PCI Express: Open drain WAKE# signal as per PCI Express M.2. - SATA: NC..
REFCLKP/N	O	- PCI Express: PCIe 100MHz clock as per PCI Express M.2. - SATA: NC..
SUSCLK	O	Suspend Clock for low power mode handling as per PCI Express M.2 specification (32.768 kHz, duty cycle between 30% and 70%, 200ppm). Connected to SoC SUSCLK_GPIO62.
CLKREQ#	I/O	- PCI Express: Open drain reference clock request signal as per PCI Express M.2. - SATA: NC.
WP#	I (open drain)	SSD write protect input. Expected SSD behavior when Write-Protect (WP) signal is used: When WP is low, any writes by the host will be aborted by the SSD (any write command not acknowledged by the SSD will be aborted). When WP# is high or if unused by the SSD module: no write protection.

When PCI Express and SATA functions coexist, the following convention applies PCI Express function / SATA function.

signal active when low

15. LEDs

15.1.1. LEDs Location

There are five bicolor LEDs (Red/Green) on the front panel of the VX6096.

Figure 12: Front LED indicators

15.1.2. LEDs Activity – Normal Mode

When LED1 is red, the meaning of the other LEDs is changed.
Refer to the "Power Sequencer"/"Error codes" section
If “debug mode” is active, please refer to Section "Power Sequencer/Power states"
For "user mode" on LED3,LED4 and LED5, see "CPLD Registers" Section

During normal operation (not configured in "user mode", no fatal error, not in “debug mode”), their state is as follows:

Table 29: LEDs Description – Normal Mode

LED1	
OFF	Board fully off
GREEN	Board running. Blinking slow (@0.5Hz) when off/sleeping and no reset source is active.
ORANGE	Board reset asserted. Blinking slow (@0.5Hz) when off/sleeping and a reset source is active.
RED	Fatal error. See chapter "Power Sequencer"/"Error codes"

LED2	
OFF	Board off or sleeping
GREEN	Normal operation. Blinking on CPLD activity (LPC or I2C0/1 slave)
ORANGE	Same than green, but when FACTORY_MODE switch is ON
RED	Watchdog timeout

LED3	
OFF	
GREEN	M2S1/M2S2 activity (off when no activity)
ORANGE	
RED	Solid “on” when temperature alert (see reg @0x74 bit 7); otherwise blinking slow (@0.5Hz) if SoC CATERR# is asserted and this signal is treated as an alert

LED4	
OFF	
GREEN	At least one i226 interface with link up, blinking on activity
ORANGE	Reserved
RED	PBIT error

LED5	
OFF	
GREEN	At least one E810 link up at full speed, blinking on link activity
ORANGE	At least one E810 link up but none at full speed, blinking on link activity
RED	

15.1.3. LEDs - Power States

When in "debug mode", the LEDs no more have their operational meaning, but LED1 is blinking green fast (@2Hz), and LED2, LED3, LED4, LED5 are displaying the current power state as follows :

Table 24: LEDs Description – Debug Mode

LEDs In "DEBUG MODE"					
Power state number	Name	LED2	LED3	LED4	LED5
0	POR_ST	OFF	OFF	OFF	OFF
1	V3V3_S5_ST	GREEN	OFF	OFF	OFF
2	V1V8_S5_ST	OFF	GREEN	OFF	OFF
3	VNN_S5_ST	GREEN	GREEN	OFF	OFF
4	V1V05_S5_ST	OFF	OFF	GREEN	OFF
5	V1V8_NACDLY_ST	GREEN	OFF	GREEN	OFF
6	RSMRST	OFF	GREEN	GREEN	OFF
7	WAITBPPWR_ST	GREEN	GREEN	GREEN	OFF
8	PWRBTN_ST	OFF	OFF	OFF	GREEN
9	WAITS4_ST	GREEN	OFF	OFF	GREEN
10	WAITS3_ST	OFF	GREEN	OFF	GREEN
11	V3V3_ST	GREEN	GREEN	OFF	GREEN
12	E810_1_ST	OFF	OFF	GREEN	GREEN
13	E810_2_ST	GREEN	OFF	GREEN	GREEN
14	DDR_ST	OFF	GREEN	GREEN	GREEN
15	V2V5DDR_ST	GREEN	GREEN	GREEN	GREEN
16	V1V2DDR_ST	OFF	OFF	OFF	RED
17	V1V8PCIE_ST	GREEN	OFF	OFF	RED
18	VCCIN_ST	OFF	GREEN	OFF	RED
19	FORCEOFF_ST	GREEN	GREEN	OFF	RED
23	RUNNING_ST	GREEN	GREEN	GREEN	RED
31	ERROR_ST	According to error code (see below)	According to error code (see below)	According to error code (see below)	According to error code (see below)

15.1.4. LEDs – Error Codes

Table 24: LEDs Description – Error codes

ERROR CODES ON LEDs						
Error code number	Name	LED1	LED2	LED3	LED4	LED5
0	ERR_NO_ERROR	-	-	-	-	-
1	ERR_3V3_S5	RED	RED	OFF	OFF	OFF
2	ERR_1V8_S5	RED	OFF	RED	OFF	OFF
3	ERR_VNN_PCH	RED	RED	RED	OFF	OFF
4	ERR_VNN_NAC	RED	OFF	OFF	RED	OFF
5	ERR_1V05_S5	RED	RED	OFF	RED	OFF
6	ERR_1V8_NACDLY	RED	OFF	RED	RED	OFF
7	ERR_3V3	RED	RED	RED	RED	OFF
8	ERR_5V0	RED	OFF	OFF	OFF	RED
9	ERR_2V5ABDDR	RED	RED	OFF	OFF	RED
10	ERR_1V2ABDDR	RED	OFF	RED	OFF	RED
11	ERR_VTTABDDR	RED	RED	RED	OFF	RED
12	ERR_PECI_CRIT	RED	OFF	OFF	RED	RED
13	ERR_THERM_PROT	RED	RED	OFF	RED	RED
14	ERR_THERMTRIP	RED	OFF	RED	RED	RED
15	ERR_CATERR	RED	RED	RED	RED	RED
16	ERR_BP_UV_PWRGD	RED	OFF	OFF	OFF	GREEN
17	ERR_BP_OV_PWRGD	RED	RED	OFF	OFF	GREEN
18	ERR_VCCIN	RED	OFF	RED	OFF	GREEN
19	ERR_1V8PCIE	RED	RED	RED	OFF	GREEN
20	ERR_PWR_INALRT	RED	OFF	OFF	RED	GREEN
21	ERR_PWR_CATFLT	RED	RED	OFF	RED	GREEN
22	ERR_3V3SB_SRC	RED	OFF	RED	RED	GREEN
23	ERR_5V0MXM	RED	RED	RED	RED	GREEN
24	ERR_E810A0V8	RED	OFF	OFF	OFF	ORANGE
25	ERR_E810A0V9	RED	RED	OFF	OFF	ORANGE
26	ERR_E810B1V8	RED	OFF	RED	OFF	ORANGE
27	ERR_E810B1V1	RED	RED	RED	OFF	ORANGE
28	ERR_1V5GFX	RED	OFF	OFF	RED	ORANGE
29	ERR_1V2GFX	RED	RED	OFF	RED	ORANGE
30		RED	OFF	RED	RED	ORANGE
31		RED	RED	RED	RED	ORANGE
32	ERR_MXM_OVERT	RED	OFF	OFF	GREEN	OFF
33	ERR_E810ATEMP	RED	RED	OFF	GREEN	OFF
34	ERR_E810BTEMP	RED	OFF	RED	GREEN	OFF
35	ERR_E810B0V8	RED	RED	RED	GREEN	OFF
36	ERR_E810B0V9	RED	OFF	OFF	ORANGE	OFF
37	ERR_2V5EFDDR	RED	RED	OFF	ORANGE	OFF
38	ERR_1V2EFDDR	RED	OFF	RED	ORANGE	OFF
39	ERR_VTTEFDDR	RED	RED	RED	ORANGE	OFF

16. VX6096 - Power specification

16.1. Power considerations

The considerations presented in the ensuing sections must be taken into account by system integrators when specifying the VX6096 system environment.

16.1.1. Backplane

Backplanes to be used with the VX6096 must be adequately specified and comply with VITA 65.0. The backplane must provide optimal power distribution for the VPX VS1 and 3V3 AUX power inputs.
Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided

16.1.2. Power Supplies

Power supplies for the VX6096 must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires.
An industrial power supply unit should be able to provide at least twice as much power as the entire system requires.
An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.
Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for die resistance variations.

- Tolerance

The following table provides information regarding the required characteristics for each board input voltage.

Table 30: VPX Input Voltage Tolerance

POWER RAIL	NOMINAL VALUE	TOLERANCE*	MAX RIPPLE (p-p)	REMARKS
+12V VPX VS1 & VS2	+12VDC	+/-5%	50mV over a range of 0-20MHz	Main voltage
VPX 3.3V AUX	+3.3VDC	+/-5%	50mV over a range of 0-20MHz	Optional
GND	Ground, not directly connected to potential earth (PE)			

(*)Tolerance values include ripple.

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

- Rise Time

As per VITA 46.0, the system power supply ramp-up phase should be between 20 and 150 msec. However, Kontron recommend a ramp-up phase below 25ms.

› Regulation

The system power supplies should be monotonic as they ramp to their specified final values during power up conditions as per VITA 46.0.

The system power supplies shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it went below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

16.1.3. Power Supplies Monitoring

The VX6096 embeds three voltage sensors monitoring power rails and internal power supply voltage.

- NCT7802Y by Nuvoton
- LTC2913 by Linear Technology
- INA220 by Texas Instruments

The voltage sensor NCT7802Y is programmed by the IPMC to monitor internal voltages. It asserts an alert signal whenever monitored voltages get out of its specified range. This alert is routed to a maskable interrupt in the cPLD.

Refer to the datasheet of the NCT7802Y for detailed specifications.

The voltage sensor LTC2913 monitors VS1 voltage with a 10 % tolerance. The thresholds are set by hardware on the board. Undervoltage and overvoltage conditions on VS1 are reported to the cPLD which in turn shuts down all VX6096 internal power supplies. There is no mechanism for masking these alerts.

The current sensor INA220 monitors VS1 input current.

› INA220 Current Sensor: Key specifications: https://www.ti.com/product/INA220

The voltage sensor ADS7830 is programmed by the IPMC to monitor VS1 and internal voltages,

16.1.4. Output Power Supplies Protections

On the VX6096, all the output power supplies provided on connectors are protected by fuse or current-limiting devices as described in the following table.

Table 31: Output Powers Supplies Protection

Port	Function	Location	Voltage	Protection	Rated Current*	Trip current	Characteristics
M2A/M2B Slots	M2. Slot power supply	On-Board	+3.3V	Non resettable fuse	4.5 A	-	-

** Worst Case Hold Rated Current* for maximum operation temperature*

- VPX Input Power Rails Specification
  The VX6096 board has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.
- Absolute Maximum Input Voltage
  The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the VX6096 should be carefully tested to ensure compliance with these ratings.

Table 32: Absolute maximum input voltage

POWER RAIL	ABSOLUTE MAXIMUM INPUT VOLTAGE
VPX 3.3V AUX	3.5V
+12V VPX VS1	13V

⚠WARNING

The maximum permitted voltage indicated in the table above must not be exceeded.
Failure to comply with these figures may result in damage to your board.

- Recommended Operating Input voltage
  The following table specifies the recommended operating conditions of the different input power voltages within the board as per VITA46.0. The VX6096 is not guaranteed to function if the board is not operating within the prescribed limits.

Table 33: Recommended Operating Input Voltage

POWER RAIL	RECOMMENDED OPERATING INPUT VOLTAGE
VPX 3.3V AUX	3.3V +/-5%
+12V VPX VS1	+12V +/-5% (inclusive of ripple)

VPX 3.3V AUX shall be used on VX6096 boards as per VITA 46.0 and VITA 65.0.
However, this power rail input could be optional on VX6096 boards because it is internally generated from the +12V VS1 power input when it is not present on the backplane.
If both, VBAT and 3.3V AUX are not present on the backplane, the date and time retention is not ensured.

- Input Power Supply Protection
  The input power rails are protected on the VX6096 by fuse as described in the following table.

  To prevent safety hazards, the chassis power supply must not exceed the Voltage Rating and Interrupt Rating of the fuse.

Table 34: Input Powers Supplies Protection

POWER RAIL	VPX VS1	VPX 3.3 V AUX	VPX -12V AUX
LOCATION	Near P0 power input pins	Near P0 power input pins	Near P0 power input pins
VOLTAGE	+12 V	+3.3 V	-12 V
PROTECTION	Non resettable fuse	Non resettable fuse	Non resettable fuse
RATED CURRENT	20 A	1.5 A	1.5 A
VOLTAGE RATING	32VDC	32VDC	32VDC
MANUFACTURER / PN	EATON / 3216FF20-R	LITTELFUSE / 043501.5KR	LITTELFUSE / 043501.5KR

16.2. Power Consumption Specification

16.2.1. Thermal Power

The following data show total board consumption for different processor configuration and Thermal Design Power. These data help for thermal power dissipation analysis.

Table 35: Thermal Power when VX6096 is equipped with D-2775TE processors

Order code	Power Mode	Measured CPU package power	Average VPX VS1 Thermal Power (W)	Max VPX VS1 Thermal Power 100ms sampling (W)	Test Condition
VX6096 / D-2775TE 16-Cores/32-Threads Base freq. @2Ghz TDP 100W	100 % all cores	100 W	138 W (1)	155 W (1)	VPX VS1= 12V, CPU Turbo Off Intel® Xeon® D-2725TE @2Ghz No USB, M.2, or XMC devices equipped Intel PTU benchmarks Kontron Board Support Packages in its default configuration.
	80 % all cores	95 W (1)	130 W (1)	147 W (1)	
	Linux Idle	-	62 W (1)	-	VPX VS1= 12V, CPU Turbo Off Intel® Xeon® D-2725TE @2Ghz No USB, M.2, or XMC devices equipped No traffic on rear VPX high speed links Kontron Board Support Packages in its default configuration.
	BIOS uEFI prompt	-	97 W (1)	-	VPX VS1= 12V, CPU Turbo Off No USB, M.2, and XMC modules equipped.

Note (1): Typical consumption measured on a few D-27xx parts.

Table 36: Thermal Power when board is equipped with D-2796TE/D-2896TER processors

Order code	Power Mode	Measured CPU package power (SoC TDP)	Average VPX VS1 Thermal Power (W)	Max VPX VS1 Thermal Power 100ms sampling (W)	Test Condition
VX6096 / D-2796TE 20-Core/40-Thread Base freq. @2Ghz TDP 118W	Intel PTU tool 100 % all cores	118 W 110 W	166 W (1) 155 W (2)	181 W 170 W (2)	VPX VS1= 12V, CPU Turbo Off. Intel® Xeon® D-2796TE @2Ghz, 128GB DDR4. No USB device and no XMC equipped. Intel PTU benchmarks Kontron Board Support Packages in its default configuration.
	Intel PTU tool 80 % all cores	109 W (1) 102 W (2)	155 W (1) 150 W (2)	169 W 164 W (2)	
VX6096 / D-2896TER 20-Core/40-Thread Base freq. @2Ghz TDP 110W	Linux Idle	-	62 W (1)	-	VPX VS1= 12V, CPU Turbo Off. Intel® Xeon® D-2796TE @2Ghz. No USB device and no XMC equipped. Kontron Board Support Packages in its default configuration.
	BIOS uEFI prompt	-	103 W (1)	-	VPX VS1= 12V, CPU Turbo Off. No USB, M.2, and XMC modules equipped.

Note (1): Typical consumption measured on a few D-27xx parts.
Note (2): Estimated values for D-2896TER

Table 37: 3V3_AUX power consomption

	Voltage Rail Name	Max Current	Max Continuous Power Consumption (W)	Test condition
Board without VPX VS1 power supply Board in stand-by mode	VPX +3V3_AUX	< 500mA	< 1.5W	VPX +3V3_AUX power rail is present and VPX VS1 power rail not present.

16.2.2. Maximum Peak Current

The following data provide maximum continuous and worst case current values on VPX VS1 (12V) power supply. These maximum includes margin to guarantee worst-case part behavior.

Table 38: Maximum VS1 Current

Order code	Measured VPX VS1 Inrush current	Test Condition
VX6096 / D-2775TE	26 Amps (< 1ms) (1)	Intel® Xeon® D-2725TE @2Ghz No USB, M.2, or XMC devices equipped

Note (1): Typical consumption measured on a few D-27xx parts.

Maximum and peak current draw are intended as with Turbo mode disabled

17. VX6096 - Thermal Performance

17.1. Board - Thermal Monitoring

To ensure long-term reliability of the VX6096, onboard components must not operate beyond their specified maximum temperature. The most critical component on the VX6096 is the processor. Operating the VX6096 above the maximum operating limits will result in permanent damage to the board.

The VX6096 includes a temperature sensor (NCT7802Y by Nuvoton) managed by the IPMC through I2C, and a LM73CIMK managed through the cPLD.

Figure 13: Temperature Sensor Location – Top side

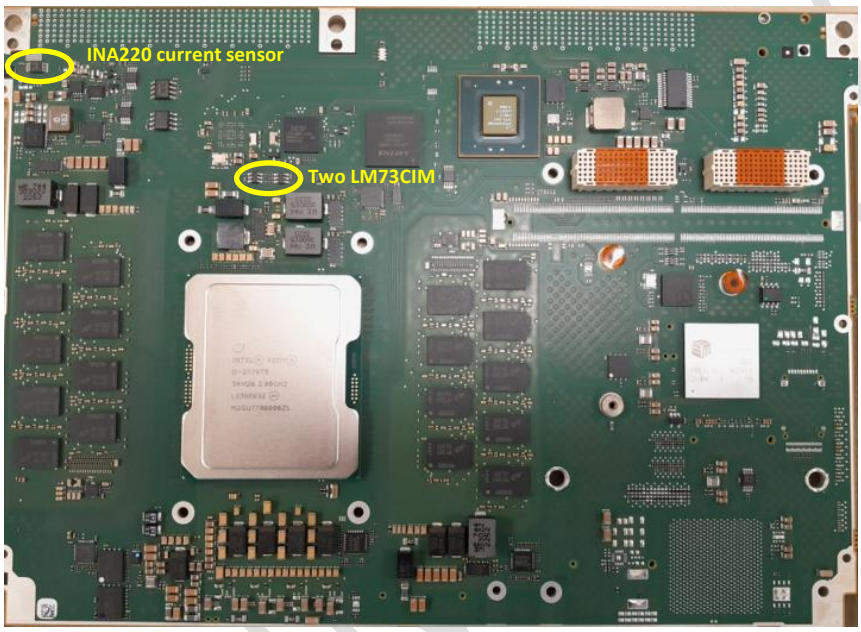
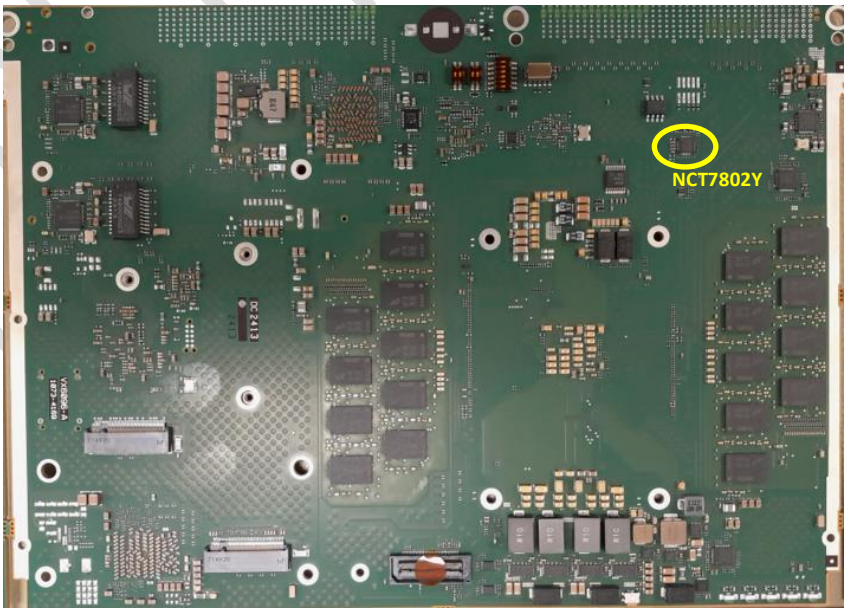


Figure 14: Temperature Sensor Location – Bottom side



In addition to monitoring several internal power supplies, the NCT7802Y supports one on-die temperature sensor and can also get the processor temperature directly via the Intel® PECI interface. The NCT7802Y temperature and voltages monitoring data may be viewed with the Linux "ipmitool" command.

The NCT7802Y has 2 alarm outputs connected to the CPLD:

- ALERT#: logged in CPLD to generate a maskable interrupt.
  The low threshold may also be used as the lower threshold for high temperature hysteresis.
- T_CRIT#: logged in CPLD reg @0x74, leads to fatal error with all internal PSUs power supplies being switched off and the error status is being displayed on the front panel LEDs.

ALERT and T_CRIT thresholds may be modified by the Shelf Manager using the IPMI command or locally by using Linux “ipmitool” command. To know default value and further details about these thresholds, refer to VITA 46.11 Firmware Release Note document (see section “Related Publications”)

› NCT7802Y Key specification:
  - Voltage monitoring accuracy +-10 mV
  - Temperature Sensor Accuracy
    - On-chip Temperature Sensor Accuracy (25~70 °C) +- 2 °C typ.
    - On-chip Temperature Sensor Resolution 1 °C
  - Operating Temperature Range -40 °C ~ 85 °C

› LM73CIMK-0/NOPB Key specifications: https://www.ti.com/product/LM73/part-details/LM73CIMK-0/NOPB

17.2. SoC - Thermal Monitoring

To allow optimal operation and long-term reliability of the VX6096, the processor must remain within the maximum junction temperature specifications. The maximum operating temperature for the processor die (Tj max) depends on Intel SKUs. The Tj max temperature is the temperature not to exceed, to avoid entering the throttling mode with reduced performance.
The THERMTRIP# temperature threshold is the temperature not to exceed to protect processor from catastrophic overheating. The processor will stop all executions when THERMTRIP# is reached. This threshold is 130°C.
The processor uses the Adaptive Thermal Monitor feature to protect the processor from overheating and includes the following on-die temperature sensors:

- One Digital Thermal Sensor (DTS) for monitoring each processor core
- Catastrophic Cooling Failure Sensor (THERMTRIP#)

These sensors are integrated in the processor and work without any interoperability of the uEFI BIOS or the software application. Thermal Control Circuit allows the processor to maintain a safe operating temperature without the need for special software drivers or interrupt handling routines.

› Digital Thermal Sensor (DTS)
The processor includes on-die Digital Thermal Sensors (DTS), one per processor cores. They can be read via an internal register of the processor.
The temperature returned by the Digital Thermal Sensor will always be at or below the maximum operating junction temperature. Via the Digital Thermal Sensors, the uEFI BIOS or the application software can measure the processor die temperature.
The Max DTS temperature is 100°C.

› Catastrophic Cooling Failure Sensor
The Catastrophic Cooling Failure Sensor protects the processor from catastrophic overheating.
The Catastrophic Cooling Failure Sensor threshold is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds this threshold. Once activated, the event remains latched until the VX6096 undergoes a power-on restart (all power off and then on again).
This function cannot be enabled or disabled in the uEFI BIOS. It is always enabled to ensure that the processor is protected in any event.

17.3. Air-Flow Through (AFT) - Thermal Performance

Figure 15: AFT variant – Example of Air flow direction

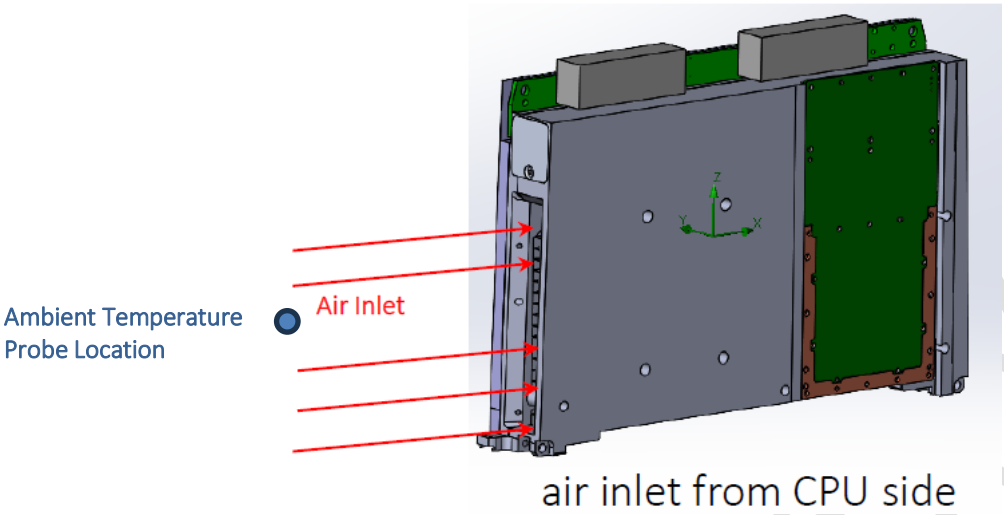


Table 39: AFT variant - Typical Functional Points

VX6096 AFT Variants	Processor Xeon D-2775TE	Processor Xeon D-2896TER	Test conditions
CPU Core Frequency	2 GHz	2 GHz	Standard AFT2 Kontron test bench., running Intel PTU with cpu workload as specified. No XMC module equipped. No M.2 module equipped. Processor turbo Off. No CPU throttling Processor junction temperature shall never exceed 100°C at any time
CPU workload Typical processor dissipation	100% all cores 100W TDP (1)	100% all cores 110W TDP (1)	
CPU Core Junction Temperature	**100 °C** (2)	**100 °C** (2)	
Min Inlet airflow (CFM)	TBD- Not available yet	TBD- Not available yet	
Max Inlet Air Temperature	55°C	55°C	

Note (1): Typical processor dissipation measured on a few D-27xx or D-28xx parts using the Intel PTU monitoring tool. Intel PTU stress mode adjusted to force the total SoC power dissipation to the value specified in the table.

Note (2): no CPU throttling if processor junction temperature is strictly below 100°C. End customer applications should not exceed a maximum CPU junction temperature of 97°C (or below) instead of 100°C to ensure at least 3°C of margin.

The processor junction temperature shall never exceed 100°C at any time.
Contact Kontron support for additional thermal design data.
Refer to the Intel EDS documents for detailed information about DTR = Dynamic Temperature Range limitations. The default maximum processor temperature range during operation is ±145°C, starting from boot time temperature, with CPU PCIe Gen3 and PCH PCIe/SATA Gen2 speed limitations.
For more information, contact Kontron Support.

Figure 16: AFT Variant – Flow rate vs Ambient Temperature

TBD- Not available yet

17.4. Conduction Cooled - Thermal Performance

› Card Edge Temperature Measurement
The card edge temperature is measured with a thermal probe located on the card edge as follows

Figure 17: Conduction cooled variant - Holes location for thermal probes

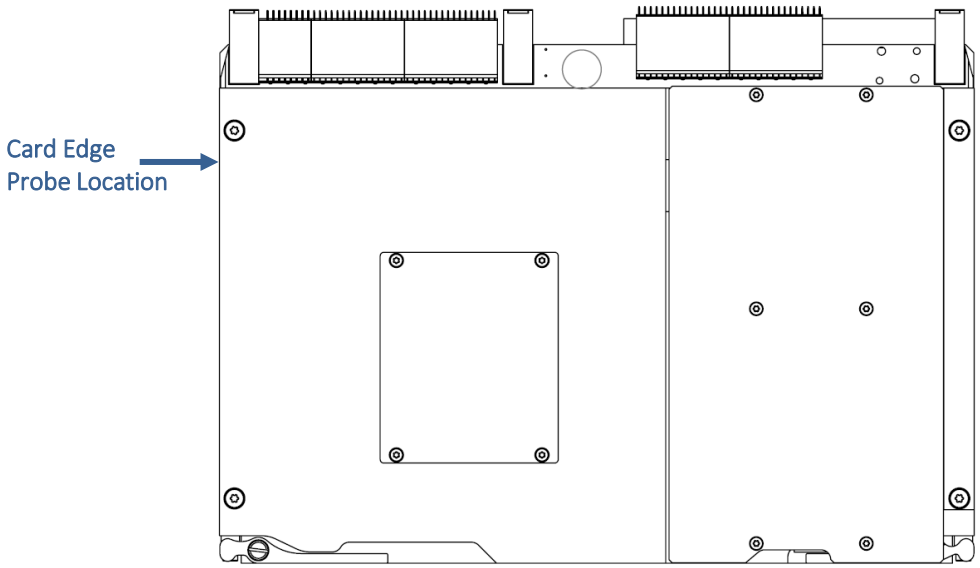


Table 40: Conduction cooled variant - Typical Functional Points

VX6096 RC Variants	Processor Xeon D-2775TE	Processor Xeon D-2896TER	Test conditions
CPU Core Frequency	2 GHz	2 GHz	Standard RC Kontron test bench., running Intel PTU with cpu workload as specified. No XMC module equipped. No M.2 module equipped. Maximum temperature measured at card edge. Processor turbo Off. No CPU throttling
CPU workload	100% all cores 100 W TDP (1)	100% all cores 110 W TDP (1)	
CPU Core Junction Temperature	**100 °C** (2)	**100 °C** (2)	
Max Card Edge temperature	TBD- Not available yet	TBD- Not available yet	

Note (1): Typical processor dissipation measured on a few D-27xx parts using the Intel PTU monitoring tool. Intel PTU stress mode adjusted to force the total SoC power dissipation to the value specified in the table.

Note (2): no CPU throttling if the processor junction temperature is strictly below 100°C. End customer applications should not exceed a maximum junction temperature of 97°C (or below) instead of 100°C to ensure at least 3°C of margin.

The processor junction temperature shall never exceed 100°C at any time.
Contact Kontron support for additional thermal design data.
Refer to the Intel EDS documents for detailed information about DTR = Dynamic Temperature Range limitations. The default maximum processor temperature range during operation is ±145°C, starting from boot time temperature, with CPU PCIe Gen3 and PCH PCIe/SATA Gen2 speed limitations.
For more information, contact Kontron Support.

Figure 18: RC Variant – Card edge vs Processor TDP

TBD- Not available yet

18. VX6096 - Installation

The VX6096 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

18.1. Safety Requirements

The following safety precautions must be observed when installing or operating the VX6096. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

This board contains electrostatically sensitive devices. Observe the necessary precautions to avoid damage to your board:
Discharge your clothing before touching the assembly. Tools must be discharged before use.
Do not touch components, connector pins or traces.
We strongly recommend our customers to work in an environment equipped with antistatic workbenches with professional discharging equipment.

HOT Surface!
Special care shall be taken while handling the board: the heat sink or heat frame can get very hot during operation. Do not touch the heat sink when installing or removing the board.
In addition, the board should not be placed on any surface or in any form of storage container before the board and heat sink have cooled down to room temperature.

18.2. Package Contents

The package contents vary with the VX6096 variant.

- VX6096 variant - see section “Ordering Information”. Board equipment differs depending on the ordered Order Code.
- Bolt accessories for mezzanine/module mounting

18.2.18.3. Board Identification

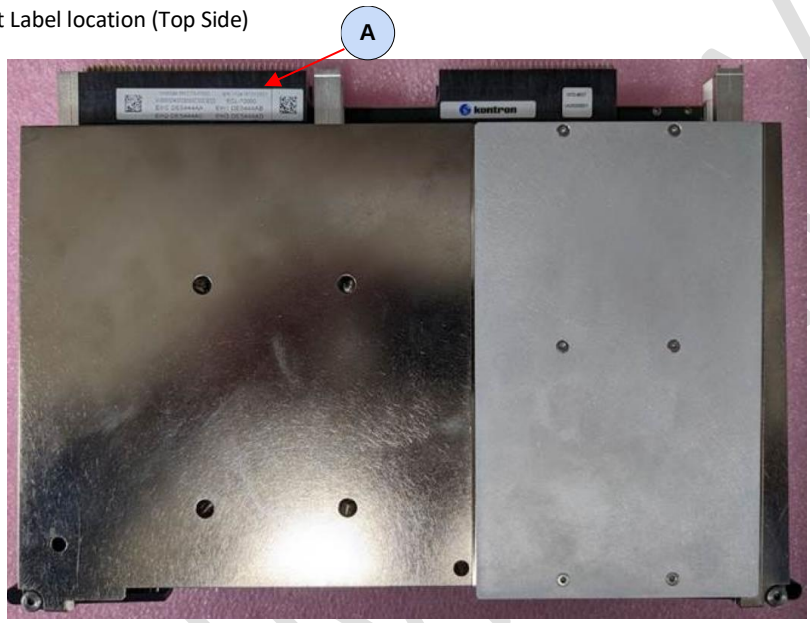
The VX6096 boards are identified by labels fitted to the top side of the board.
The E.C. Level format is "xxxxxLy" where

- The five digits "xxxxx" indicate the board E.C. Level (PCB revision included)
- "Ly" indicates the mechanical E.C. Level:
  - letter "L" varies with the environment class
  - digit "y" gives the mechanical E.C. Level.

› Top Side

A "Identification" label: Order Code, Serial Number, Variant, E.C. Level, Ethernet MAC addresses

Figure 19: Main Product Label location (Top Side)

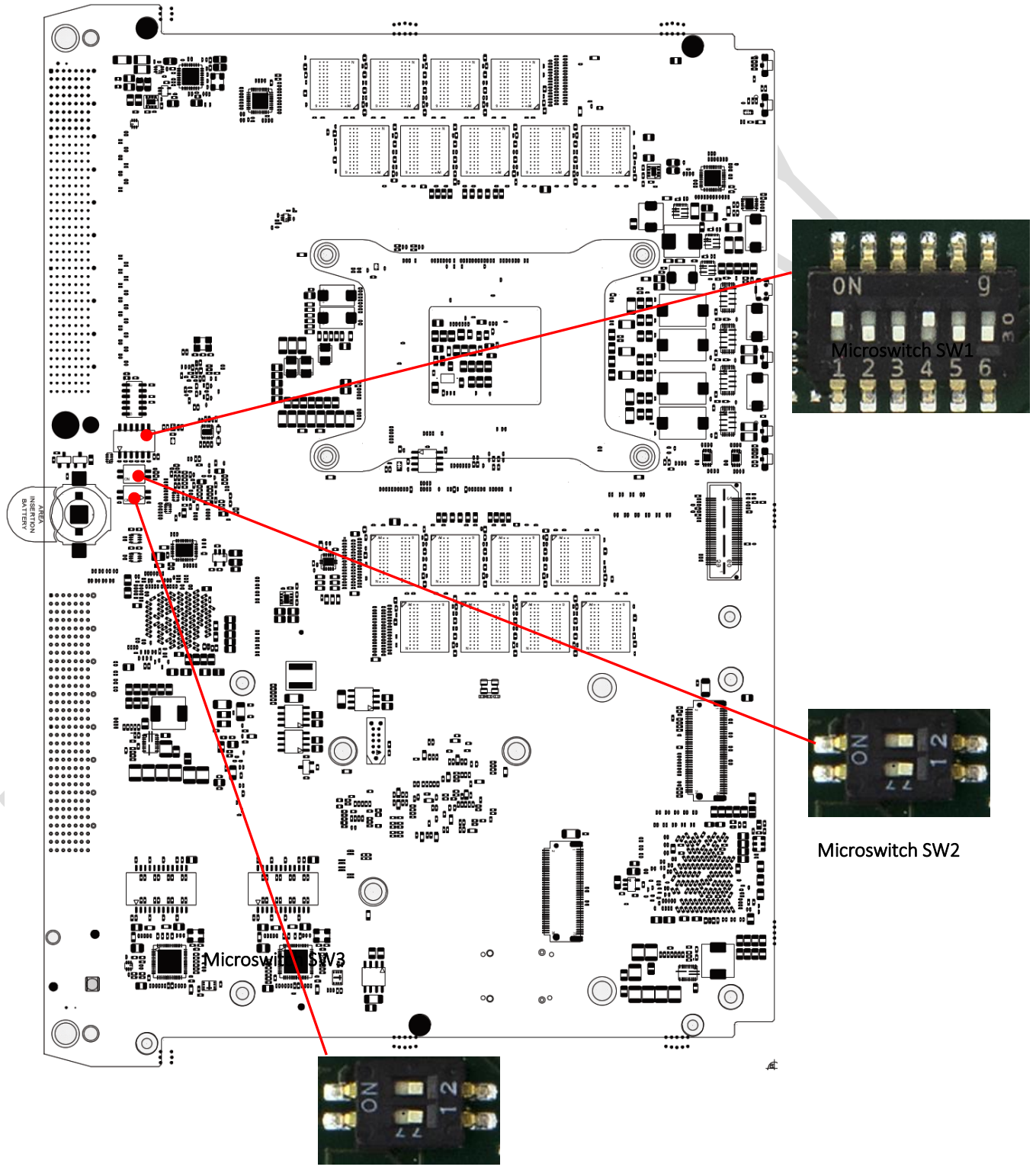


18.3.18.4. Board Configuration

18.3.1.18.4.1. Microswitches location

All switches' positions can be read back from software through CPLD registers

Figure 20: Board Configuration – Micro switches location (Bottom view)



18.3.2.18.4.2. SW1 Microswitch description

Table 41: SW1 Microswitch Description

SW1		
#	Function	Description
1	FACTORY_MODE	OFF: Normal operation (default) ON : Reserved
2	VPD_WP	OFF: Normal operation (default) ON : force **unprotection** of devices in “VPD” domain (see "NVMRO" section)
3	USER_WP	OFF: Normal operation (default) ON : force protection of devices in “USER” domain (see "NVMRO" section)
4	DBG_MODE	OFF: Normal operation (default) ON : Debug mode enabled
5	BIOS_FAILSAFE	OFF: Normal operation (default) ON : start software in failsafe mode for recovery purpose
6	CS_SWAP	OFF: Normal operation (default) ON : boot on rescue BIOS flash device

18.3.3.18.4.3. SW2 Microswitch description

Table 42: SW2 Microswitch Description

SW2		
#	Function	Description
1	FORCE_PROCHOT	OFF: Normal operation (default) ON : Reserved
2	NVMRO_OFF	OFF: Normal operation (default) ON : force NVMRO off on backplane and on local board (see "NVMRO" section)

18.3.4.18.4.4. SW3 Microswitch description

Table 43: SW3 Microswitch Description

SW3 only for VX6096 with IPMI option		
#	Function	Description
1	BMC_CONSOLE_ENABLE	OFF: Normal operation (default) ON : serial ports forced to RS232 mode with TX enabled for debug/recovery using an RS232 console
2	FORCED_RS232	OFF: Normal operation (default) ON: Reserved

18.4.18.5. Initial Installation Procedures

The following procedures are applicable only for the initial installation of the VX6096 in a system. Procedures for standard removal operations are found in their respective chapters.

To perform an initial installation of the VX6096 in a system, proceed as follows:

1. Ensure that the safety requirements indicated in the “For Your Safety” section are observed.

CAUTION: Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For the configuration and installation of VX6096, specific peripheral devices and Rear I/O devices refer to the appropriate sections in current Chapter.

CAUTION: Care must be taken when applying the procedures below to ensure that neither the VX6096 nor other system boards are physically damaged by the application of these procedures.

3. To install the VX6096, perform the following:

a. Ensure that no power is applied to the system before proceeding.

b. Select the slot where the board should be inserted as per application requirements. Then carefully insert the board until it makes contact with the backplane connectors.

Conduction Cooled variants: when performing the next step and when the chassis accommodating the board is compliant with VITA48.2, it is recommended to use the ejector handles to seat the board into the backplane connectors. For the other chassis, simply push the board into the backplane connectors.

c. Engage the board with the backplane using the ejector handle until the handle is locked. In RC configurations (no handle or handle not locked), push the board until it is fully seated in the backplane.

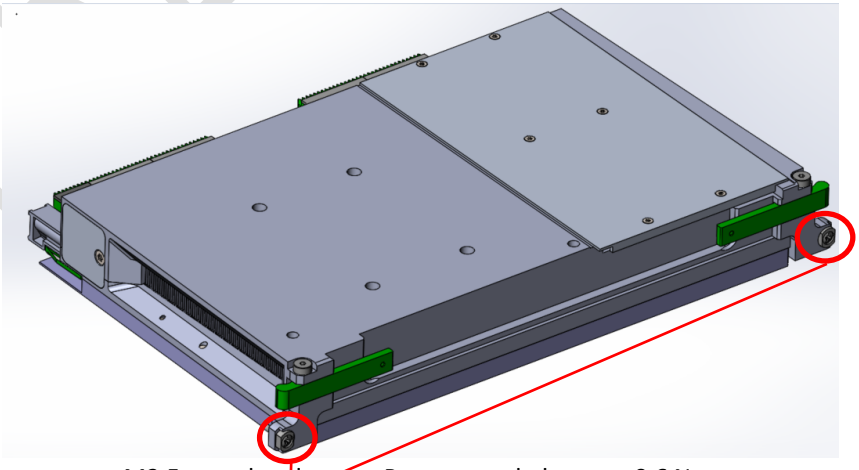
d. AFT class board type: Tight the front panel screws to lock the board.

RC class board type: Tight the wedgelocks to the cold plate. A torque of 0.68 N.m must be applied to the wedgelock screw

e. Ensure that the board is properly secured.

The VX6096 is now ready for operation. Refer to appropriate VX6096 specific software, application, and system documentation.

Figure 21: AFT variant Locking Screws Location on the front panel

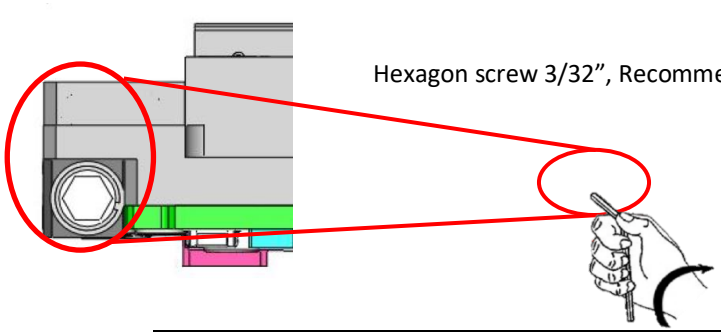


M2.5 cross head screw. Recommended torque 0.6 N.m

⚠CAUTION

Running the AFT board without tightening the locking screws may result in permanent damage to the board.

Figure 22: RC variant - Wedgelock Screw Location



⚠CAUTION

Running the board at high temperature without tightening the wedgelocks to the cold plate may result in permanent damage to the board.

18.5.18.6. Standard Removal Procedure

ESD sensitive Device! Precautions are listed in “For Your Safety” Section

To remove the board from the chassis, proceed as follows:

1. Ensure that the safety requirements indicated in “For Your Safety” Section are observed. Particular attention must be paid to the warning regarding the heat frame!

CAUTION: Care must be taken when applying the procedures below to ensure that neither the VX6096 nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. RC class type board: loosen the wedgelocks
4. Disengage the board from the backplane using the board ejection handle, press the handle until the board is disengaged.
5. After disengaging the board from the backplane, pull the board out of the slot.

HOT Surface!
Due care should be exercised when handling the board due to the fact that the heat frame can get very hot. Do not touch the heat frame when changing the board.

6. Dispose of the board as required.

18.6.18.7. XMC Removal Procedure

	ESD sensitive Device! Precautions are listed in “For Your Safety” Section
	Apply "Loctite 222e" threadlock on each screw during reassembly of the XMC

Supported XMC type

The default XMC connectors are VITA 61 XMC 2.0 compliant and support PCI-Express interface.

XMC IOs connector (J16) is equipped by default.

The XMC stack is 12 mm.

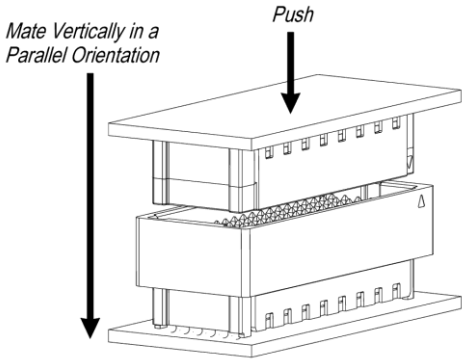
XMC installation

To install an XMC on a RC variant, proceed as follows:

1. If the VX6096 board is plugged in the chassis, follow the procedure described in the “Installation” section
2. For RC variants, remove the XMC cover mounted on the heat frame if any. Discard nylon washers.
3. Align the XMC connectors. Press to fully engage the XMC.

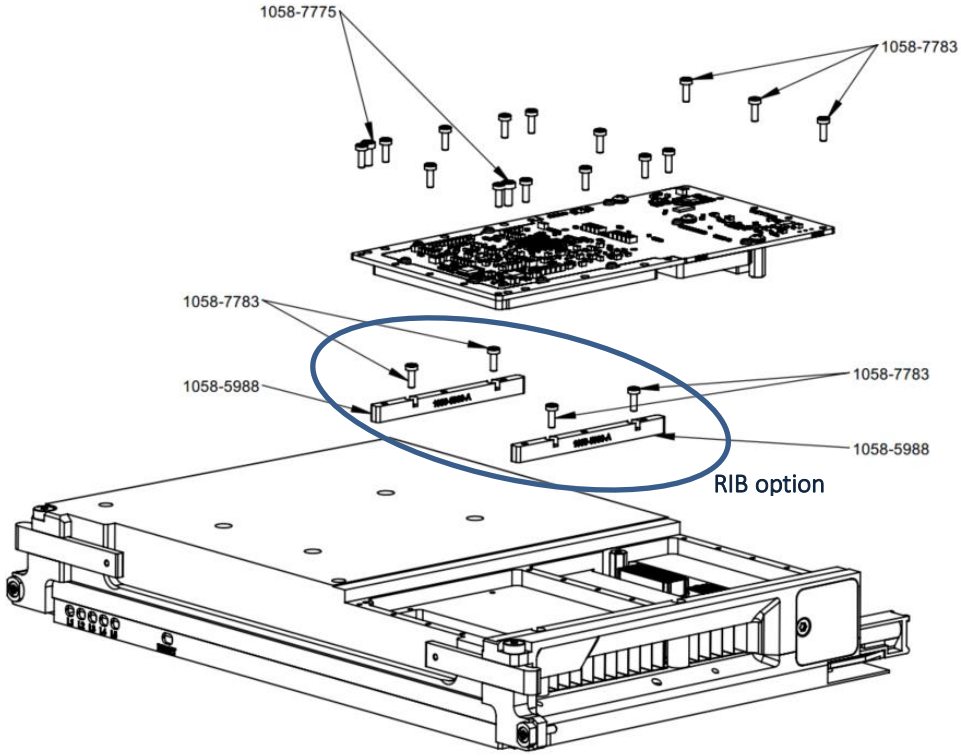
⚠CAUTION	The XMC connectors should be mated straight: Align the connectors and when the keys start to enter the keyways, push at the approximate center of the connector into the mating connector until the face of the receptacle cover bottoms on the face of the plug. Because of the asymmetric keying, reverse mating is impossible (the key end of the receptacle cannot be inserted into the non-keyway end of the plug). Both connectors have a lead-in around the perimeter that will allow blind mating.

Figure 23: XMC Module Insertion



4. Screw the XMC in place using the appropriate mounting points as depicted in Figures 14 and 15. Screw the XMC cover if any using nine mounting points.

Figure 24: XMC module Installation on a AFT board type

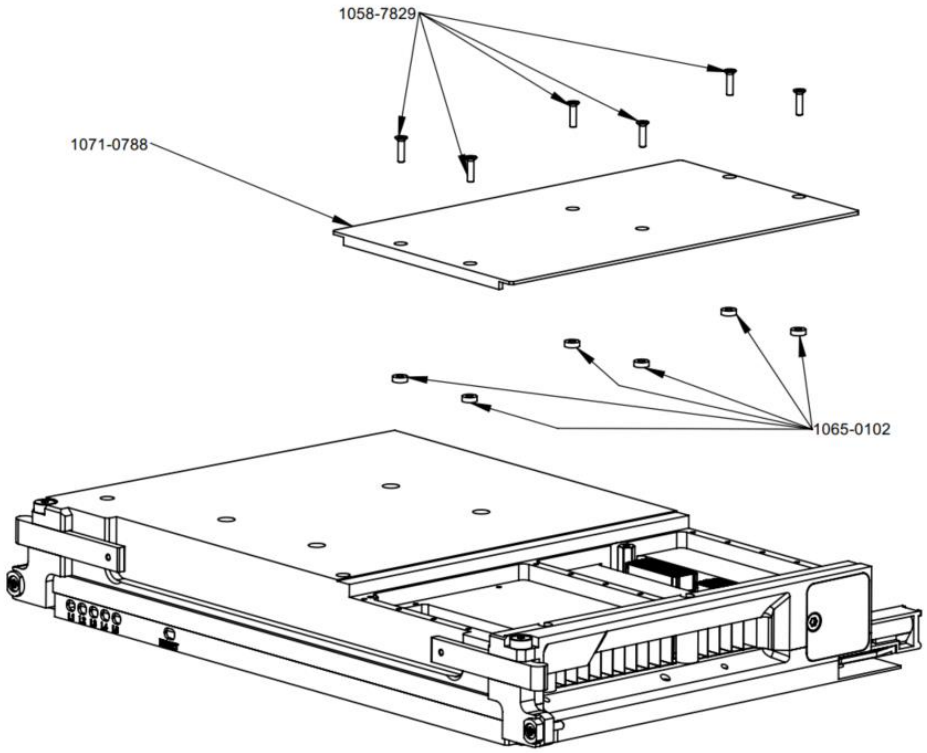


	Description	Qty	Torque	Thred lock
1058-7775	HEXALOBULAR SOCKET CHEESE HEAD SCREW ISO 14580-M2.5X6-A4-70	2	0.28 N.m	Loctite 222 Or equivalent
1058-7783	HEXALOBULAR SOCKET CHEESE HEAD SCREW ISO 14580-M2X6-A4-70	15	0.14 N.m	

Additional parts to install the XMC RIB option

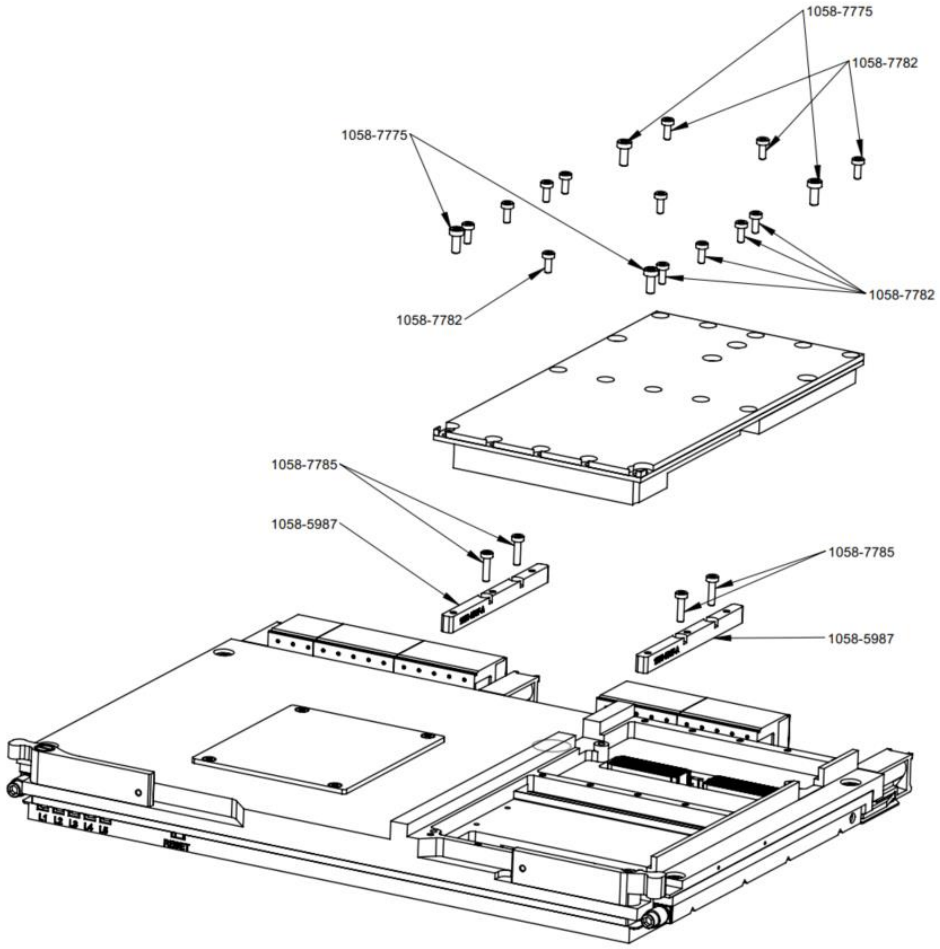
Article	Description	Qty	Torque	Thred lock
1058-7783	HEXALOBULAR SOCKET CHEESE HEAD SCREW ISO 14580-M2X6-A4-70	4	0.2 N.m	Loctite 222 Or equivalent
1058-5988	XMC RIB	2	-	

Figure 25: XMC cover Installation on a AFT board type



Article	Description	Qty	Torque	Thred lock
1058-7829	COUNTERSUNK FLAT HEAD SCREW ISO 14581-M2X8-A4-70	6	0.2 N.m	Loctite 222 Or equivalent
1071-0788	TOP COVER XMC 3U VITA48.8	1	-	
1065-0102	RICHCO R913-1 NYLON SPACERS 2.3X4.8X1.6	6	-	

Figure 26: XMC module Installation on a RC board type

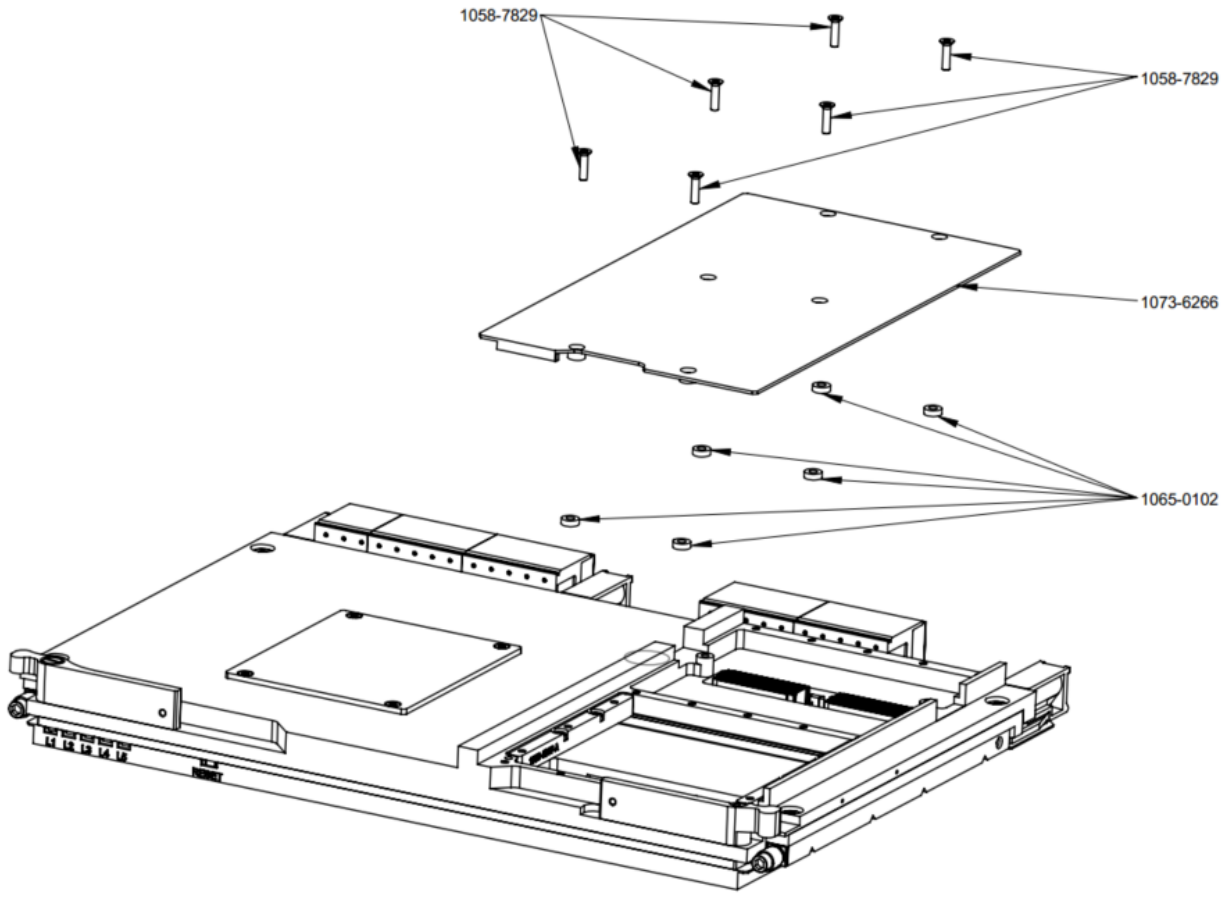


	Description	Qty	Torque	Thred lock
1058-7775	HEXALOBULAR SOCKET CHEESE HEAD SCREW ISO 14580-M2.5X6-A4-70	4	0.28 N.m	Loctite 222 Or equivalent
1058-7782	HEXALOBULAR SOCKET CHEESE HEAD SCREW ISO 14580-M2X5-A4-70	14	0.14 N.m	

Additional parts to install the XMC RIB option

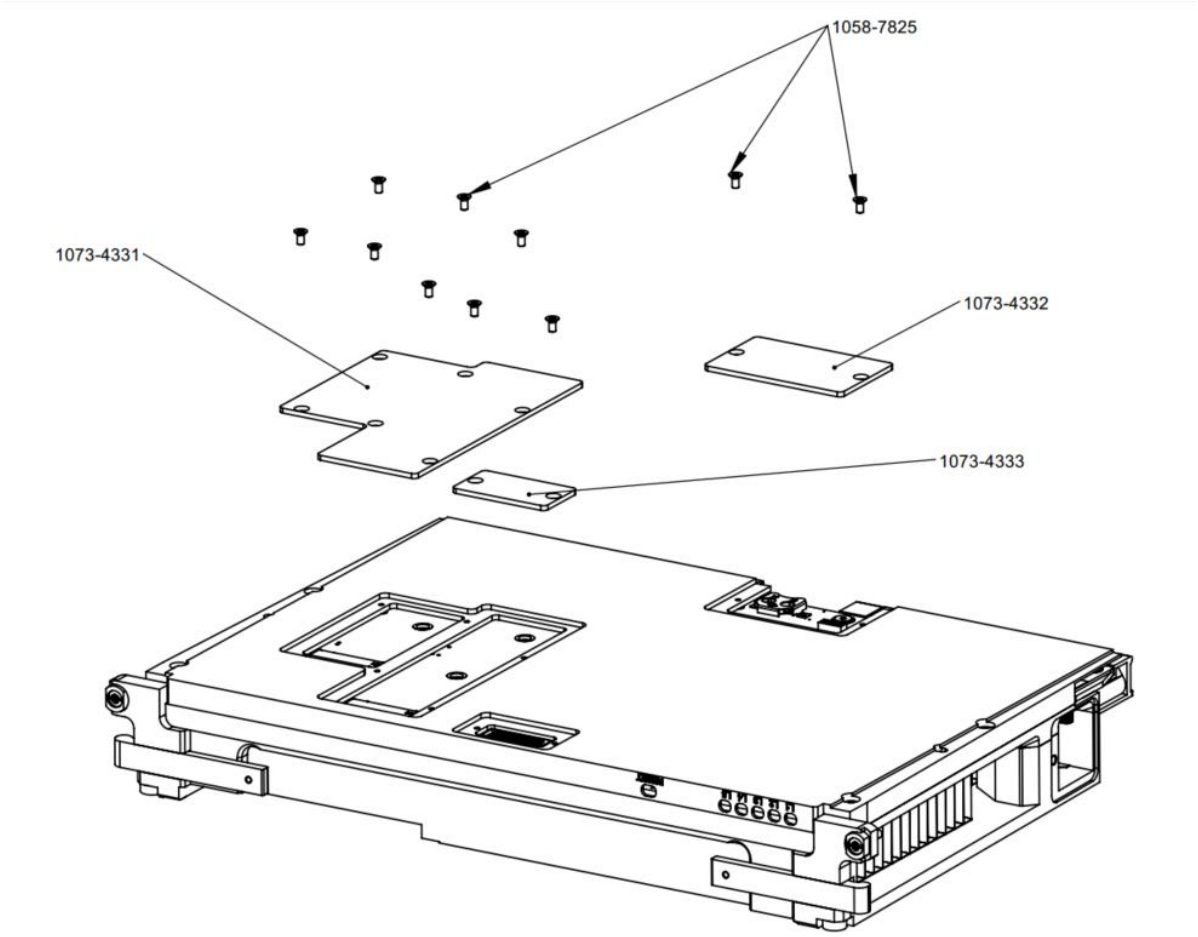
Article	Description	Qty	Torque	Thred lock
1058-7783	HEXALOBULAR SOCKET CHEESE HEAD SCREW ISO 14580-M2X6-A4-70	4	0.2 N.m	Loctite 222 Or equivalent
1058-5988	XMC RIB	2	-	

Figure 27: XMC cover Installation on a RC board type



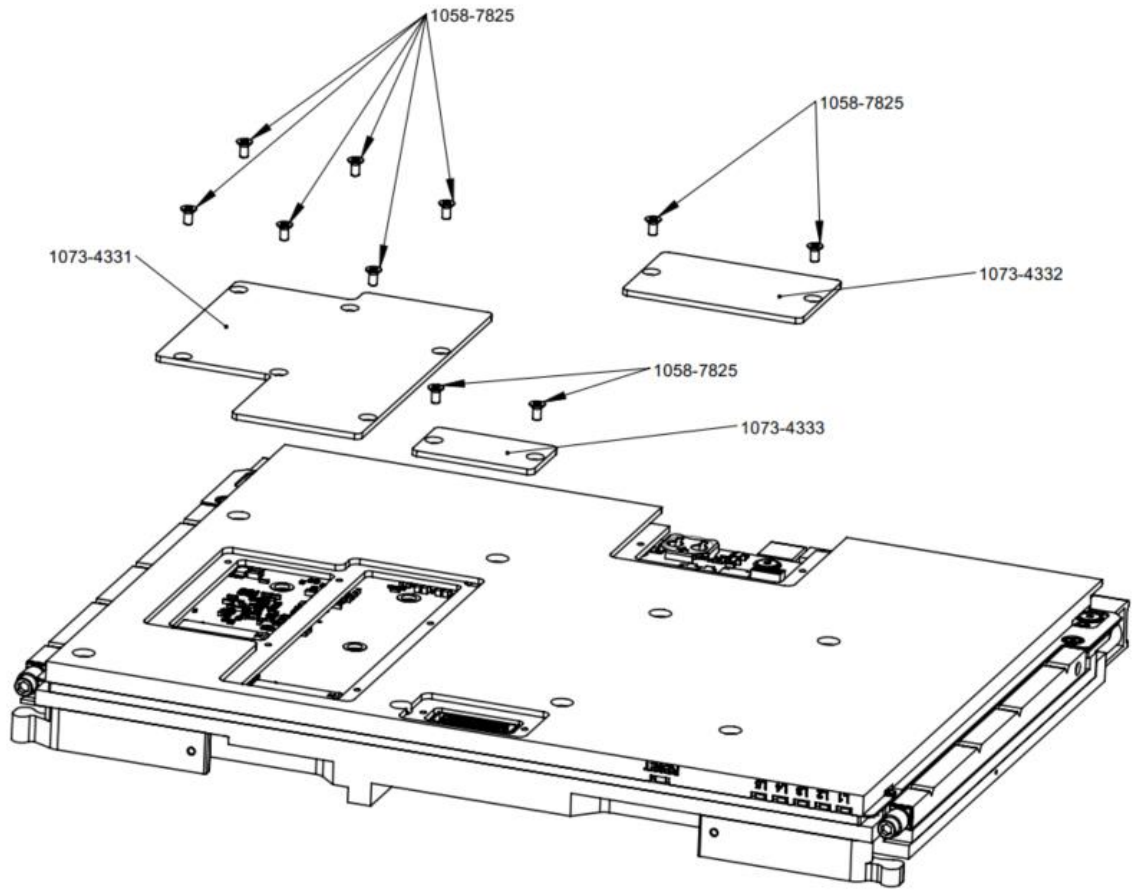
Article	Description	Qty	Torque	Thred lock
1058-7829	COUNTERSUNK FLAT HEAD SCREW ISO 14581-M2X8-A4-70	6	0.2 N.m	Loctite 222 Or equivalent
1073-6266	VX6096 RC TOP COVER XMC	1	-	
1065-0102	RICHCO R913-1 NYLON SPACERS 2.3X4.8X1.6	6	-	

Figure 28: Bottom covers Installation on a AFT board type



Article	Description	Qty	Torque	Thred lock
1058-7825	COUNTERSUNK FLAT HEAD SCREW ISO 14581-M2X4-A4-70	10	0.2 N.m	Loctite 222 Or equivalent
1073-4331	VX6096 AFT M.2 BOTTOM COVER	1	-	
1073-4332	VX6096 AFT BATTERY AND SWITCH BOTTOM COVER	1	-	
1073-4333	VX6096 AFT CONNECTOR BOTTOM COVER	1	-	

Figure 29: Bottom covers Installation on a RC board type



Article	Description	Qty	Torque	Thred lock
1058-7825	COUNTERSUNK FLAT HEAD SCREW ISO 14581-M2X4-A4-70	10	0.2 N.m	Loctite 222 Or equivalent
1073-4331	VX6096 AFT M.2 BOTTOM COVER	1	-	
1073-4332	VX6096 AFT BATTERY AND SWITCH BOTTOM COVER	1	-	
1073-4333	VX6096 AFT CONNECTOR BOTTOM COVER	1	-	

18.7.18.8. M.2 Module Insertion / Removal Instructions

› M.2 Module Insertion Process

ESD sensitive Device! Precautions are listed in “For Your Safety” Section

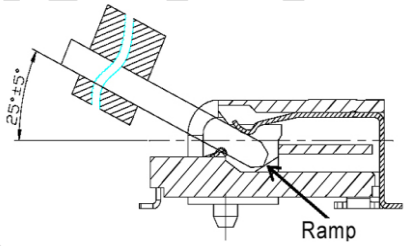
Apply "Loctite 222" threadlock or equivalent on each screw during reassembly of the M.2 module

1. If 2LM cover option is present, Disassemble the bottom M.2 cover according to the bottom cover procedure. Remove flat washer and hexagon thin nut. See figures below.

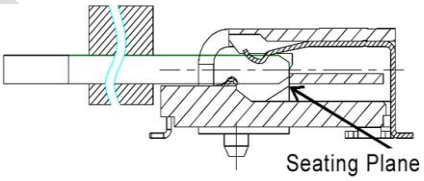
2. For VX6096 variants requiring a standoff (in a separate bag included in packaging), place the standoff above the mounting hole.

M.2 Module Insertion

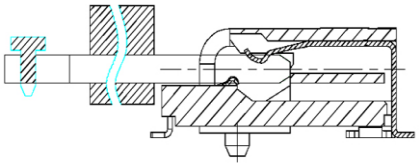
3. Insert the module at an angle of 25°±5° until the module makes contact with the ramp



4. Rotate the module to horizontal position and make sure the card’s edge makes contact with the seating plane.

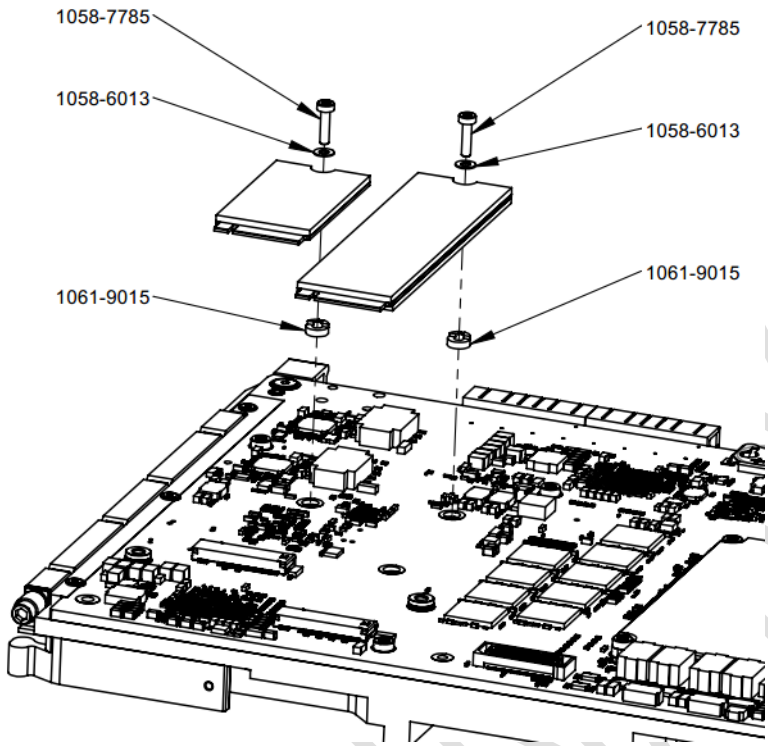


6. Attach the module using appropriate mechanical parts (washer, nut or screw) as described in figures below.



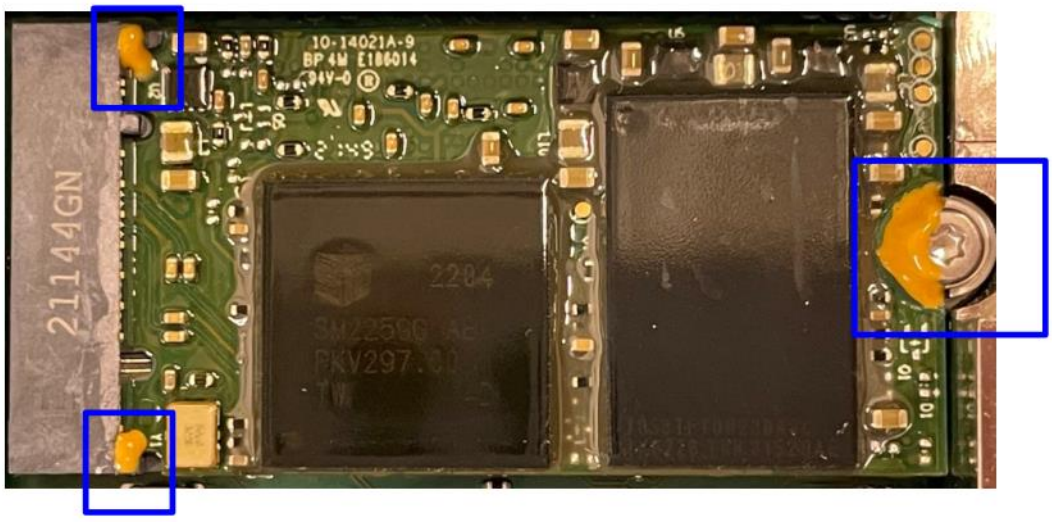
6. For Rugged variants, adhesive is required as shown in pictures below.

Figure 30: AFT and RC variant – M.2 module mounting



Article	DESCRIPTION	Qty	Torque	Thread lock
1058-7785	HEXALOBULAR SOCKET CHEESE HEAD SCREW ISO 14580-M2X8-A4-70	2	0.14 N.m	Loctite 222e Or equivalent
1058-6013	WASHER FLAT M2 ISO7092 SS	2	-	-
1061-9015	ENTRETOISE POUR M.2 SSD H3.2	2	-	

Figure 31: Adhesive application example to lock M.2 Module on AFT or RC class rugged boards

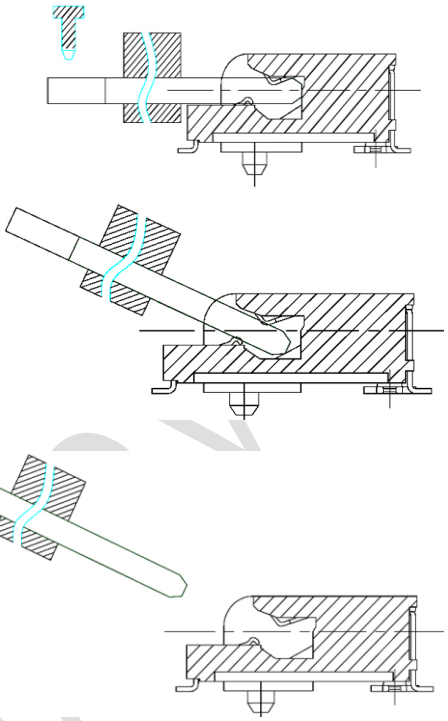


⚠CAUTION

For harsh environment applications, Kontron recommends to apply adhesives to lock the M.2 module. Such as 3M Scotch-Weld™ 7838, or equivalent: at the junction between the module and the M.2 connector/screw (Blue rectangles on the pictures above)
All screws must be locked with Loctite 222 or equivalent thread lockers

M.2 Module Removal Process

1. Loosen the screw by hand and the module will be rotated automatically due to connector contact's counterforce at the same time.



2. Take away the module by hand.

18.8.18.9. OS Software Installation

The installation of all on-board peripheral drivers is described in detail in the relevant Driver Kit files or Board Support Packages (BSP).
The installation of an operating system is dependent of the OS software and is not addressed in this manual.
Refer to appropriate OS software documentation for software installation.

19. VX6096 - Detailed On-Board Features

19.1. Real-Time Clock (RTC)

Two Real Time Clocks (RTC) are available on the VX6096: one is embedded in the CPU while the other is a standalone, high-precision, low-power component (RV-8803) accessed through the PCH SMBus.

- **Standby power supplied to the RV-8803 RTC**
  When the VX6096 is powered off, the RTC power supply comes either from the VPX 3.3V_AUX rail or from the VPX VBAT rail. To ensure data retention in the RV-8803 RTC, the VPX VBAT must be set in the range [2.5V - 5.5V]. The maximum current drawn over the -40 °C/+85 °C temperature range is 500 nA (VBAT= 3 V, no I2C activity) or 550 nA (VBAT=5 V, no I2C activity).

- **Internal Integrated PCH RTC**
  The integrated PCH RTC module provides a date and time keeping device with two banks of static RAM with 128 bytes each although the first bank has 114 bytes for general-purpose usage. The BIOS programs the RTC interrupt on Legacy IRQ8 that is never shared with other interrupts. It is clocked by an external 32.768 KHz oscillator with a parabolic coefficient of 0.4 ppm/°C² and a stability of +/-20 ppm at 25 °C. A 20 ppm stability is equivalent to a 10 mn/year drift.

- **Standalone low-power RTC RV-8803**
  The RV-8803 RTC by Micro Crystal includes an internal oscillator and a date and time keeping module with programmable alarm, timer and interrupt functions. It features an ultra low-power consumption in time keeping mode: 240 nA typical and 800 nA maximum in worst case conditions.
  RV-8803 offers a very high Time Accuracy (best in class): ±1.5 ppm 0 to +50°C, ±3.0 ppm -40 to +85°C, ±7.0 ppm +85 to +105°C.

- **RTC management by BIOS and OS**
  At each startup, the BIOS retrieves the date and time information from the high-precision RV-8803 RTC and copies it into the integrated PCH RTC.
  Any update of date and time in the BIOS settings will be done both in integrated PCH RTC and RV-8803 RTC.
  Regarding the RTC management by the OS, the OS should use the high-precision RV-8803 RTC driver. Failing to do so, the updates will be done only in integrated PCH RTC and will not be saved.
  If no power is applied on the RV-8803 RTC, the BIOS displays the BIOS build date and time instead of the current date and time.

- **Century flag**
  For compatibility reasons, the BIOS implements the century flag for the high-precision RTC as follows:
  - Century Flag C = 0 for 1900-1999 years
  - Century Flag C = 1 for 2000-2099 years.

  The user should check that the OS driver implements the same convention.

19.2. CPLD Watchdog

In addition to the standard watchdog timer included in the integrated PCH, the cPLD implements a hardware watchdog timer that can be used by the operating software to monitor the normal operation of the system.
It is enabled by software, and once enabled must be restarted at regular intervals. If not, its expiration sets off an interrupt (IRQ) to the local processor, a board reset or a board power-cycle.
The watchdog has an option to be automatically enabled at power-on or reset to protect from an hanging BIOS.
The watchdog has the following features:

- timeout programmable from 1 to 511 clock periods, by steps of 2 periods
- clock periods of 1s or 1ms
- lock bit: when set, can only refresh (restart) the watchdog, but not change its settings
- 4 modes: timer, reset, interrupt or power-cycle
- restart counter: can manage the remaining number of resets or power-cycles done by the watchdog before giving-up.
- pre-timeout interrupt (dual stage)

19.3. I2C Structure

The VX6096 features several I2C busses.

- Two are attached to the integrated Platform Hub Controller and control the DDR4 SPD EEPROM and the low-power RTC.
- The other two are handled by the CPLD device and by the IPMC device

Figure 32: I2C Block Diagram for information

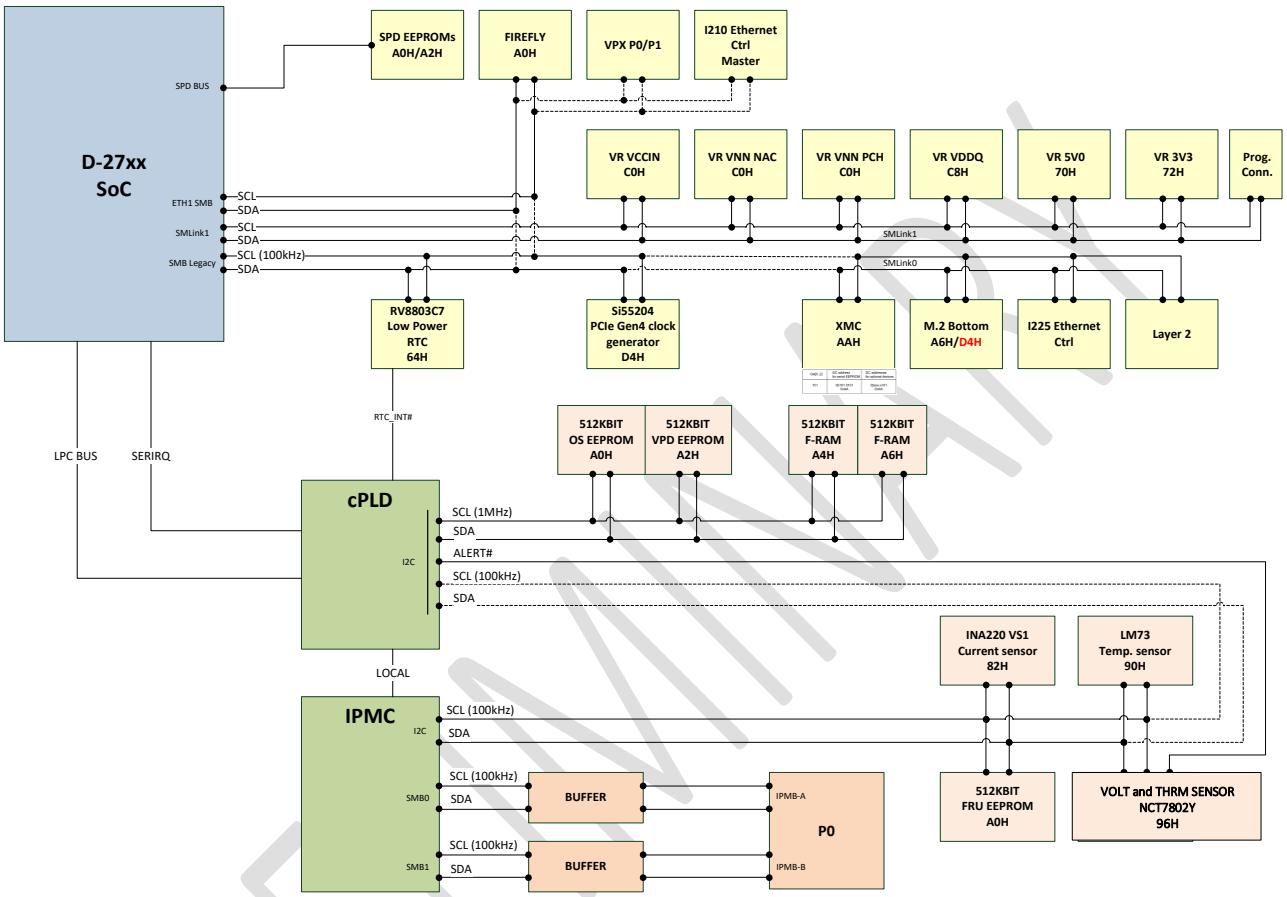


Table 44: End user I2C device list

End User Device	Size	Default Bus	SMBUS BASE ADDRESS (8-bit address)	FEATURES
RV-8803-C7	-	SMB HOST	64H	External RTC Device
XMC eeprom	-	SML PCH	AAH	XMC slot SMBus
INA220	-	I2C IPMC (cPLD)	82H	VS1 Current Monitoring
LM73	-	I2C IPMC (cPLD)	90H	Temperature sensor
TMP411A	-	I2C IPMC (cPLD)	98H	E810 dual 10GbE temperature sensor
TMP411B	-	I2C IPMC (cPLD)	9AH	E810 100GbE temperature sensor
NCT7802Y	-	I2C IPMC (cPLD)	96H	Voltage and Temperature sensor
AT24C512C	512-Kbit	I2C IPMC (cPLD)	A0H	IPMI – FRU data
LM73	-	cPLD	90H	Temperature sensor
AT24CM01	512-Kbit	cPLD	A0H	VPD EEPROM (Vital Product Data)
AT24CM01	512-Kbit	cPLD	A2H	OS EEPROM
FM24V10	1-Mbit	cPLD	A4H/A6H	User data

19.4. EEPROM Mapping

On-board EEPROM mapping are in the following tables

Table 45: VPD and OS EEPROM mapping

VPD EEPROM I2c @ (A0H) Global Mapping

EEPROM addresses	Description
0x0000 – 0x0200	Board Vital Product Data
0x0200 - 0x0300	Reserved (Optional VPD - MAC address …)
0x0300 - 0x07FFF	Free Area
0x8000 - 0xFFFF	Free Area

OS EEPROM I2c @ (A2H) Global Mapping

EEPROM addresses	Description
0x0000 – 0x1400	Free for OS (used by Linux BSP)
0x1400-0x2000	PBIT Reserved (Factory Test Information)
0x2000- 0x3000	PBIT Test List/Test/Rescue list …
0x3000-0x4000	Reserved PBIT
0x4000- 0x52FF	PBIT System Test Config and Recorded Information
0x5300-0x6000	Reserved PBIT
0x60F0 -0x612F	CPLD Power ON Config Data
0x6130-0x7FFF	Free area
0x8000-0xFFFF	Free area

19.5. Main CPLD Features

The CPLD manages the following features:

- Power-on/off control
- Reset control
- LPC interface to processor
- KCS interface to IPMC
- LEDs control
- Serial lines multiplexer
- Serial VPD and user memories
- User and system GPIOs
- Internal registers dedicated to system management

› cPLD Register

cPLD registers are accessible from CPU through LPC bus. Most of them are managed by the BIOS or by OS drivers, and the others can be managed by a dedicated tool such as cpldtool. See Linux Kontron VME/VPX Fedora Remix – Release Note.

19.6. Serial Lines Modes

› Serial Ports Location

MP01 (i.e. COM1): Serial interface available on the VPX P1 connector
MP02 (i.e. COM2): Serial interface available on the VPX P5 connector
SER01 (i.e. COM2 or COM2 and COM3): Serial interfaces available on the VPX P4 connector

› Protocol Selection

MP01 port on VPX P1: default mode is LVCMOS protocol. Mode can be set to EIA-232 through BIOS settings.
MP02 port on VPX P5: default mode is EIA-232 protocol. Mode can be set to LVCMOS through BIOS settings.
SER01 port on VPX P4: default mode is EIA-422/485 protocol. Mode can be set to dual EIA-232 interfaces through BIOS settings.

Table 46: SER01 Mapping Table

Pin Name	Dual EIA-232	EIA-232	LVCMOS	EIA-422/485 full duplex	EIA-485 half duplex
SER01-TX- (VPX P4-G1)	COM2 TXD	COM2 TXD	COM2 TXD	COM2 TXD-	COM2 TXD-
SER01-TX+ (VPX P4-G3)	COM3 TXD	COM2 RTS#	-	COM2 TXD+	COM2 TXD+
SER01-RX- (VPX P4-G13)	COM2 RXD	COM2 RXD	COM2 RXD	COM2 RXD-	-
SER01-RX+ (VPX P4-G15)	COM3 RXD	COM2 CTS#	-	COM2 RXD+	-

› Additional feature

When EIA-422/485 is selected, the transmit can be enabled/disabled through a bit in a CPLD register (legacy method), or by the RTS signal of the UART, or also automatically using the CPLD "auto-TX" feature (when the UART sends some data)

19.7. LVCMOS GPIOs

The VX6096 provides up to eleven GPIOs managed by the CPLD:

- Two GPIOs (GPIO01 and GPIO02) are available on the VPX P1 connector
- Two GPIOs (GPIO03 and GPIO04) are available on the VPX P2 connector
- Six GPIOs (GPIO05 to GPIO10) are available on the VPX P5 connector
- One GPIO (GPIO11) with dual purpose GPIO/Maskable Reset is available on the VPX P1 connector

Refer to the Software Release Notes for further details about the GPIO driver.

The default GPIO mode on COTS after boot is the input mode.

These GPIOs are 3.3V logic and are NOT 5V tolerant (maximum voltage is 3.6V).

When set as output, the drive strength is 8mA (sink or source).

When set as input, there's a hysteresis of ~250mV.

A weak pull-up of 47KOhms is present on all GPIOs.

The GPIOs share the same interrupt in the CPLD.

The GPIOs share the same interrupt in the CPLD.

19.8. LVDS GPIOs

The VX6096 provides up to three LVDS GPIOs managed by the CPLD:

- Two LVDS GPIOs (GPlvds01 and GPlvds02) are available on the VPX P2 connector
- One LVDS GPIO (GPlvds03) is available on the VPX P4 connector

Refer to the Software Release Notes for further details about the GPIO driver.

19.9. Gdiscrete1

GDISCRETE1 is a bussed open-collector GPIO defined by OpenVPX VITA 65 and available on the VPX P1 connector.

It is handled by the CPLD and buffered by a SN74LVC1G125 buffer wired as an Open Collector to meet the electrical characteristics defined in VITA 65.

It has a dedicated interruption in the CPLD.

19.10. Reset

Table 47: Reset Management Table

RESET SOURCE	RESET ACTION	RESET CONTROL	RESET SOURCE INFORMATION	NOTE
Front panel push button	Platform reset	Front panel push button	I2C_BOARD_STATUS @0x72	Reset propagation options and masks available in cPLD registers
VPX Sysreset	Platform reset	VPX P0 / Row B/ Wafer 4	I2C_BOARD_STATUS @0x72	See VPX Vita46.0 standard Reset propagation and mask options available in cPLD registers
VPX maskable reset	Platform reset	VPX P1 / Row G/ Wafer 15	I2C_BOARD_STATUS @0x72	See VPX Vita46.0 standard
cPLD watchdog reset	Platform reset	Refer to the Fedora Remix Release note	I2C_BOARD_STATUS @0x72	Refer to the Fedora Remix Release note
Processor watchdog reset	Platform reset	Refer to the Intel Tiger Lake watchdog feature and control registers	Refer to the Intel Tiger Lake watchdog feature and control registers	Refer to the Intel Tiger Lake watchdog feature and control registers
cPLD software reset	Platform reset	I2C_BOARD_CONTROL @0x73	I2C_BOARD_STATUS @0x72	Refer to the cPLD control/status registers

19.11. NVMRO

NVMRO is defined by the VITA 46.0 standard.
VX6096 is designed to meet Standard for SOSA™ Reference Architecture, Edition 1 / Rule 6.4.2-4.

Table 48: NVMRO - Write Protections

Memory	Part Ref	Size	Fully Write protected when NVMRO is asserted	Write protection Level	Possible HW Write Protections	Writable During Operation With HW Write protection disabled	Function	Existing Writing tool If HW Write protection is disabled	Proposed sanitization procedure
MP2978	MP2978GU-6903-Z (U6601) Monolithic Power Systems	Proprietary	No	NA	None. No User access.	No	VR configuration	None	No user access. Sanitization not required.
MP2978	MP2978GU-6906-Z (U7001) Monolithic Power Systems	Proprietary	No	NA	None. No User access.	No	VR configuration	None	No user access. Sanitization not required.
MP2976	MP2976GU-6903-Z (U7301) Monolithic Power Systems	Proprietary	No	NA	None. No User access.	No	VR configuration	None	No user access. Sanitization not required.
MP2978	MP2978GU-6905-Z (U7701, U8101) Monolithic Power Systems	Proprietary	No	NA	None. No User access.	No	VR configuration	None	No user access. Sanitization not required.
SDRAM EEPROM	M24C04-RMC6TG (U0301, U0501) ST MICROELECTRONICS	4 Kbit	Yes	VPD	NVMRO MicroSwitch SW1[2] MEM_PROTECT Register (see product manuals)	Yes	SDRAM size and timing information storage	Kontron BIOS/kspd	Turn off WP and erase data. **The product will no longer work after sanitization.**
VPD EEPROM	AT24CM01-SSHM-T (U4908/1) MICROCHIP	512Kbit	Yes	VPD		Yes	Region1: Storage of board configuration data Region2: user data	Kontron BIOS/BSP commands	Turn off WP and erase data **The product will no longer work after sanitization**
i226 Flash Memory	W25Q16JVUXIM (U3302, U3455) Winbond	16 Mbit	Yes	VPD		Yes	Config and Ethernet controller address	**Intel Lanconf/Eeupdate**	Turn off WP and erase data The product will behave badly after sanitization.
E810XXVAM2 Flash Memory	W25Q128JVSIQ (U3503) Winbond	128 Mbit	Yes	VPD		Yes	Config and Ethernet controller address	**Intel Lanconf/Eeupdate**	Turn off WP and erase data The product will behave badly after sanitization.
FLASH in cPLD	LCMXO2-4000HC-4BG256ITR (U5501) LATTICE	256Kbit	Yes	USER	NVMRO MicroSwitch SW1[3] MEM_PROTECT Register (see product manuals)	Yes	Storage for cPLD configuration data	Kontron BIOS/kpld	Turn off WP and erase data **The product will no longer work after sanitization**.
FRAM	FM24V10-GTR (U4904) CYPRESS	1 Mbit	Yes	USER		Yes	Storage of user data	Kontron PBIT/BSP commands	Turn off the WP and erase data using the API and driver provided in the Linux BSP.
IPMC BOOT FLASH	W25Q16JVUXIM (U5302) Winbond	16 Mbit	Yes	USER		Yes	IPMC boot flash device	Kontron BIOS/BSP commands	Turn off WP and overwrite data with the BIOS/kflash command. **The product will no longer work after sanitization**.
BOOT FLASH	MT25QL512ABB1EW9-0SIT (U4702 & U4703) Micron	2x 512 Mbit	**No**	USER	**Full HW protection is not possible because Intel proprietary due to ME writes. No direct user access allowed when operating.** NVMRO MicroSwitch SW1[3]	Yes	Boot and Rescue Boot Flash devices	Kontron BIOS/BSP commands	Turn off WP and overwrite data with the BIOS/BSP command. **The product will no longer work after sanitization**.

Memory	Part Ref	Size	Fully Write protected when NVMRO is asserted	Write protection Level	Possible HW Write Protections	Writable During Operation With HW Write protection disabled	Function	Existing Writing tool If HW Write protection is disabled	Proposed sanitization procedure
					MEM_PROTECT Register (see product manuals)				
SYS EEPROM	AT24CM01-SSHM-T (U4908/2) MICROCHIP	512Kbit	Yes	SYSTEM	NVMRO MEM_PROTECT Register (see product manuals)	Yes	Region1: Storage of board configuration data Region2: user data	Kontron BIOS/BSP commands	Turn off WP and erase data
FRU EEPROM	AT24C512C-MAHM-T (U5304) MICROCHIP	512Kbit	Yes	SYSTEM		Yes	Region1: Storage of board configuration data Region2: user data	Kontron BIOS/BSP commands	Turn off WP and erase data **The product will no longer work after sanitization**
TPM	ST33KTPM2X32CKE3 (U4701)	Up to 2MB	No	NA	No.	Yes	Storage of user data such as keys, TPM firmware	Kontron BIOS	Dedicated tool to perform sanity checks is provided by ST (under UEFI/Linux)
IPMC	LPC2368FET100,518 (U5301)	128kB	No	NA	No.	Yes	Storage of IPMC execution source code	Kontron BIOS/BSP commands	Erase data **The product will no longer work after sanitization**
M.2 module Option	If option DEM24-B56DH1KWAQFH INNODISK	256 GBytes	Yes	USER	NVMRO MicroSwitch SW1[3] MEM_PROTECT Register (see product manuals)	Yes	Storage of user data	Kontron BIOS/PBIT/BSP commands	**According to the sanitization procedure defined by the Innodisk manufacturer.** The product may behave badly after sanitization.
XMC module	Customer part	NA	Yes **(if supported by XMC modules)**	SYSTEM	NVMRO MEM_PROTECT Register	Yes	Customer use case	Standard LinuxOS API	Turn off WP and overwrite data with the Standard LinuxOS API or customer API. The product may behave badly after sanitization.

Please contact Kontron support for more information.

19.12. IPMI Option

The VX6096 embeds an IPMI controller so much so that the VX6096 is considered as a FRU as per VITA 46.11. The IPMI controller is accessible through an IPMB bus or through a host Keyboard Controller Style (KCS) interface.

The IPMC manages the following features:

- Local environmental control/monitoring
- I2C interfaces to I2C bus IPMB A/B (rear P0)
- KCS interface to CPLD
- Serial FRU memory
- IPMI watchdog
- System Event Log (SEL)
- Sensor Device functionality

For further detail about IPMI firmware, refer to VX6096 IPMI Firmware Release Note.

› VPX IPMB I2C interfaces

VX6096 implements two I2C buses connected to P0 VPX connector:

- IPMB A (I2C0) CLK on pin P0-B5, DATA on pin P0-A5
- IPMB B (I2C1): CLK on pin P0-G4, DATA on pin P0- F4

› IPMI commands available

The VX6096 IPMI firmware supports all the Mandatory IPMC Tier-1 and Tier-2 commands. See the exhaustive list of IPMI supported commands in the VX6096 IPMI Firmware Release Note.

19.13. Graphic Option

The VX6096 embeds a Silicon Motion SM768 graphics media processor which provides a 1.2 DisplayPort interface available on the VPX P4 connector. The VX6096 also has an optional feature to route a proprietary M.2 graphics module instead.

Please contact Kontron for M.2 DisplayPort graphics module option and availability.

19.14. Security Solution

The VX6096 answers digital security requirements with hardware enforced root of trust (secure elements).
The VX6096 supports SEC-Line computer security offering:

- **AUTHENTICATION WITH TPM**: Secure network protocols

If needed customers can customize the solution to meet specific needs.

Please contact Kontron support for more information.

19.15. Trusted Platform Module (TPM 2.0)

The VX6096 is compliant with TPM 2.0 standard. A Trusted Platform Module (TPM) stores RSA encryption keys specific to the host system for hardware authentication.

19.16. Tested M.2 Module List

Table 49: Tested M.2 modules (Non-exhaustive List)

Tested configuration	Slot used for the Functional test	Upstream interface option selected on the M.2 socket	Capacity	Memory Technology	Manufacturer	Part Number
1	M2A M2B	M2A: Not equipped M2B: SATA 3.0	- 30GB	- MLC	- Virtium	- VSFBM4XI030G-150
2	M2A M2B	M2A: SATA 3.0 M2B: Not equipped	60GB -	MLC -	Virtium -	VSFBM4XI060G -
3	M2A M2B	M2A: NVME Gen 1 and 2 speed M2B: NVME Gen 1 and 2 speed	320GB 320GB	pSLC pSLC	Virtium Virtium	VSFBN4CI240G-V11 VSFBN4CI240G-V11
4	M2A M2B	M2A: NVME Gen 1 and 2 speed M2B: NVME Gen 1 speed	320GB 320GB	pSLC pSLC	Virtium Virtium	VTPM24CEXI320-0011 VTPM24CEXI320-0011

20. RTM – Detailed Features

20.1. RTM Overview

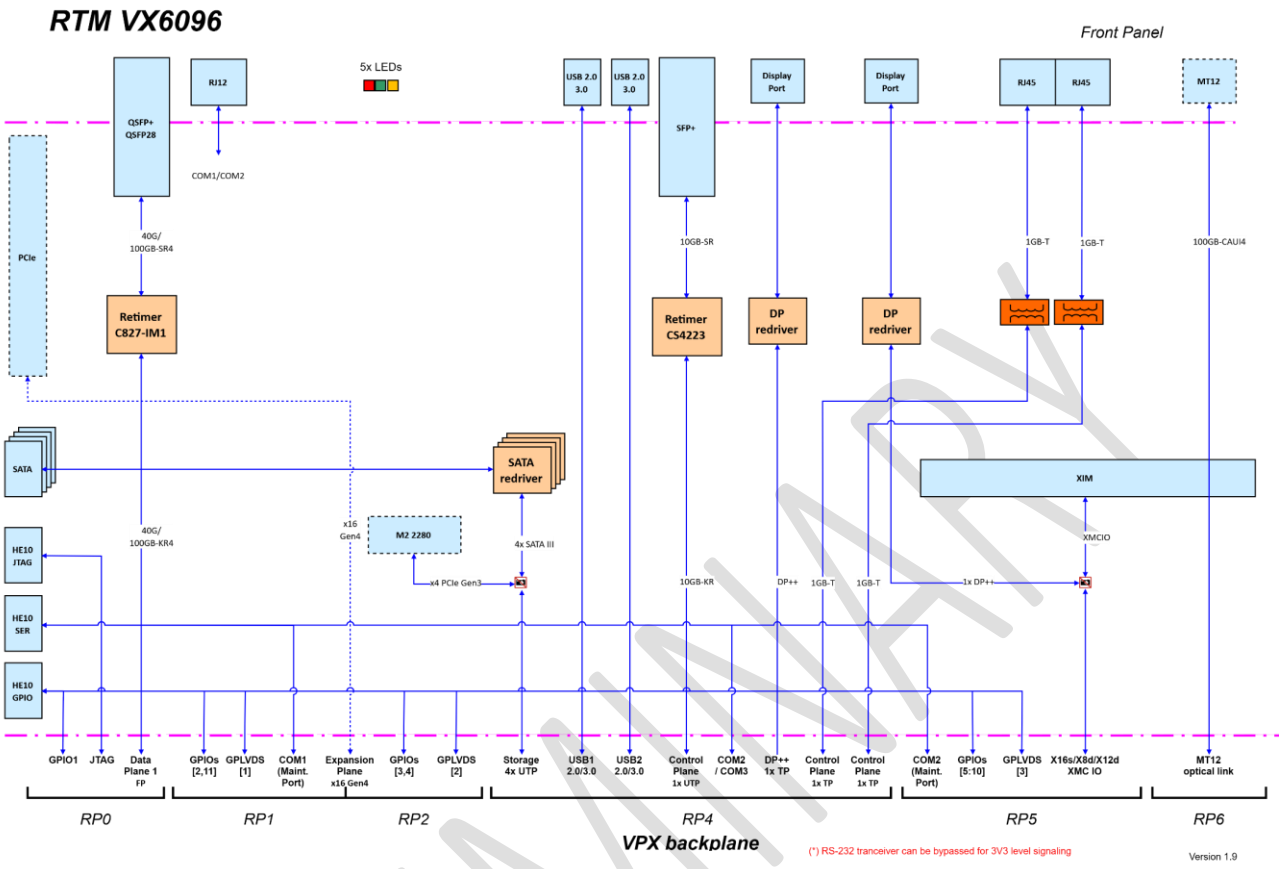
The Kontron PB-VX6-0000 is a 6U VPX Rear Transition Module (RTM) compliant with the definition of the Rear Transition Module on VPX Standard –VITA 46.10.
It provides rear I/O peripherals connectivity for Kontron VX6096 Compute Intensive variants featuring VPX connectors.

Figure 48: RTM Overview

In this document, RTM means PB-VX6-0000.
This RTM is compatible with VX6096 Compute Intensive Variants.
Do not use with I/O Intensive boards and ecosystems.
When plugged in an existing VPX ecosystem, the available and usable interfaces of the RTM will depend on the VX6096 variant and the backplane used.

20.2. RTM PB-VX6-0000 - Block diagram

Figure 48: RTM - PB-VX6-0000 Block Diagram



20.3. RTM Safety Requirements

The following safety precautions must be observed when installing or operating the RTM. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

NOTICE

ESD Sensitive Device!

This RTM contains electrostatically sensitive devices. Observe the necessary precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

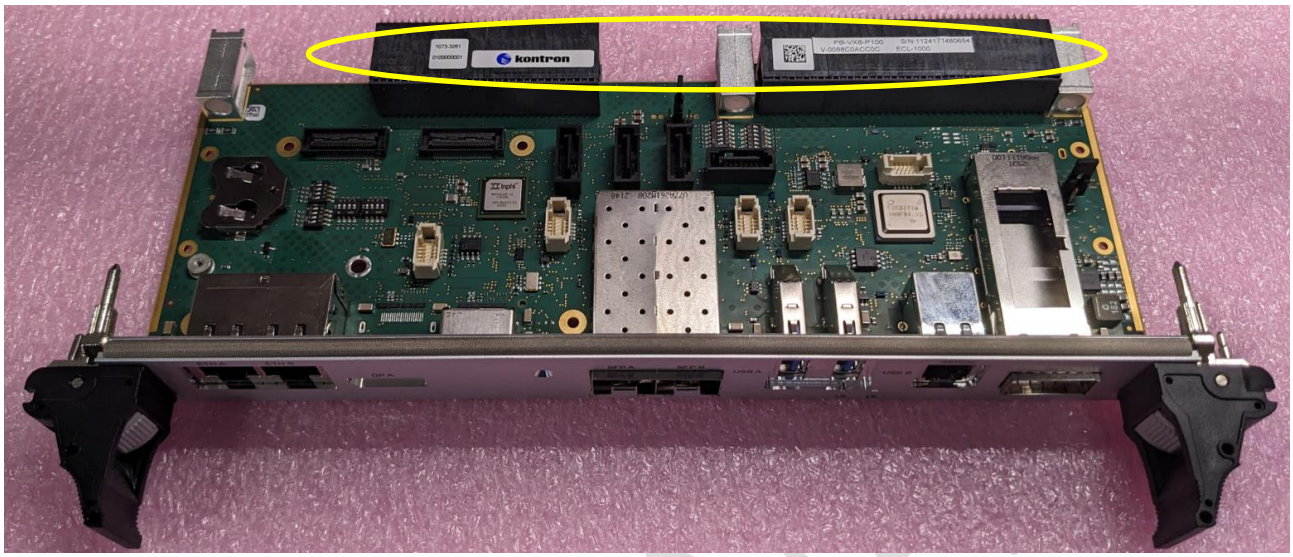
Do not touch components, connector pins or traces.

We strongly recommend our customers to work in an environment equipped with anti-static workbenches with professional discharging equipment

20.4. RTM Identification and labels

The RTM is identified by labels fitted to the VPX connector on the top side of the board.
Example on the picture below.

Figure 48: RTM PB-VX6-0000 RTM tooling - Labels location on the VPX connectors



20.5. RTM Technical specification

Table 50: RTM - Technical Specifications

TECHNICAL SPECIFICATIONS	
Power Specification	
Supply Voltage	12V VS1 VPX
Mechanical Specification	
Front Panel size	1 slot (5HP)
Dimension	VPX 6U standard form factor
Weight (g)	~ 300 g
Environmental Specification	
Conformal coating	Not available
Operating temperature	10°C/35°C (lab use)

12V VS1 VPX power supply must be provided to RTM for full operating

20.6. RTM Front Panel Interfaces

Figure 33: RTM Front Panel I/O Interfaces

Table 51: RTM Front Panel Technical Specification

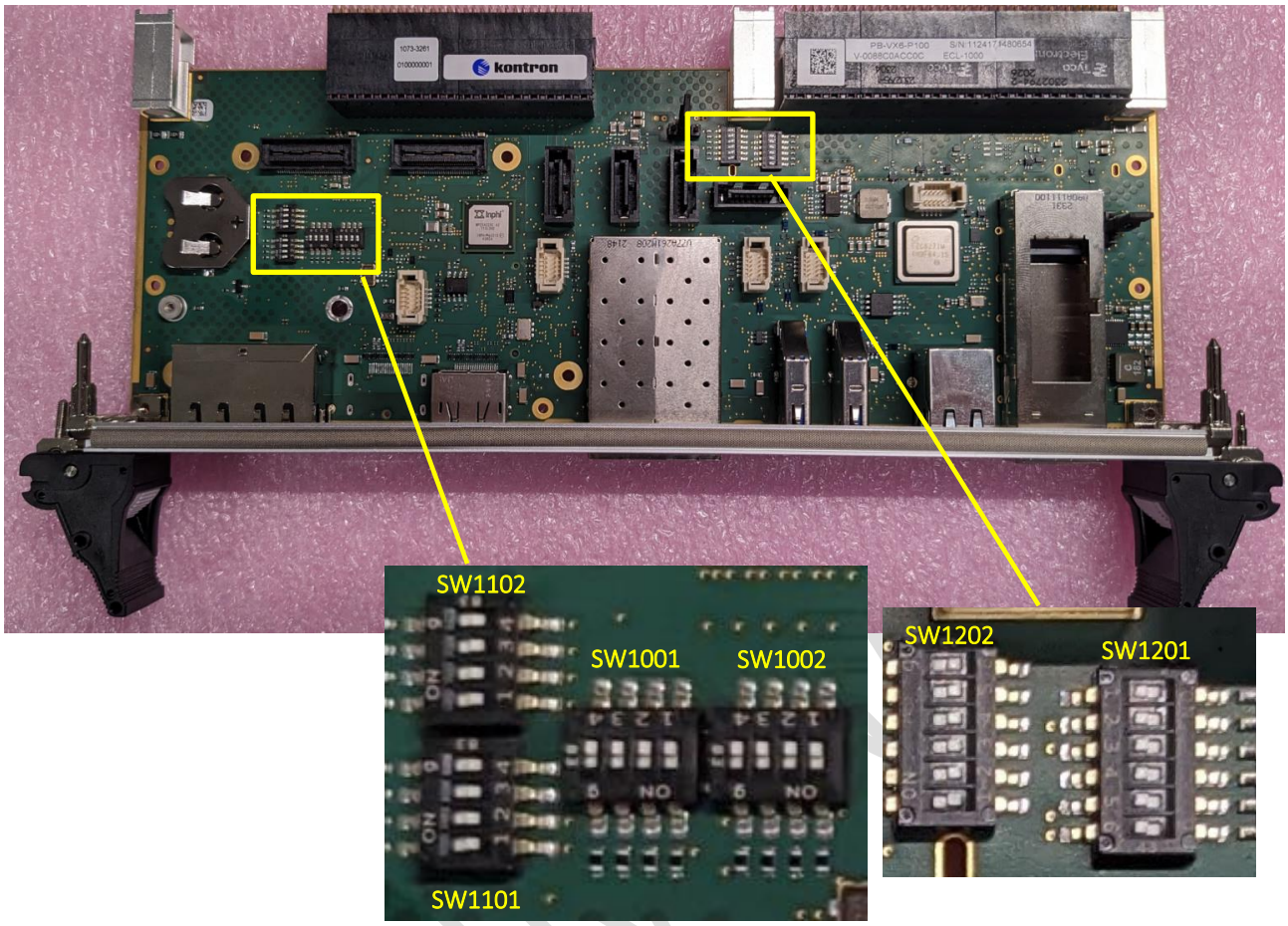
Front Panel Name	Description	Comment
ETHA / ETHB	RJ45 1000-BaseT Ethernet ports	
DPA	Display Port output	
SFP A /SFP B	Dual SFP Links	
USB-A / USB-B	two USB front connectors carrying USB 2.0 port and USB 3.0 port USBSS (USB-A and USB-B)	
SERIAL	RJ12 serial port	
QSFP	QSFP Ethernet port	
L1 to L6	Led indicators	

USB cable shall be compliant to Universal Serial Bus Specification, Revision 3.0.
This USB cable shall have double shielding. The USB cable length should not exceed 3 m.

ETH A port on the RTM font panel refers to the CPtp01 Ethernet interface on the VX6096/VPX P4 Connector
ETH B port on the RTM font panel refers to the CPtp02 Ethernet interface on the VX6096/VPX P4 Connector
DP port on the RTM font panel refers to display interface on the VX6096/VPX P4 Connector
SFP A port on the RTM font panel refers to the CPutp01 Ethernet interface on the VX6096/VPX P4 Connector
SFP B port on the RTM font panel refers to the CPutp02 Ethernet interface on the VX6096/VPX P4 Connector
USB A port on the RTM font panel refers to the USB01 USB interface on the VX6096/VPX P4 Connector
USB B port on the RTM font panel refers to the USB02 USB interface on the VX6096/VPX P4 Connector
QSFP+/QSFP28 port on the RTM font panel refers to the DP02 Ethernet interface on the VX6096/VPX P4 Connector
SERIAL port on the RTM font panel refers to the MP01 Serial interface on the VX6096/VPX P1 Connector

20.7. RTM Microswitches

Figure 34: RTM – TOP Micro switches location



Default setting is OFF for all switches.
OFF for all switches is the normal operation mode

Figure 35: RTM – BOTTOM Micro switches location

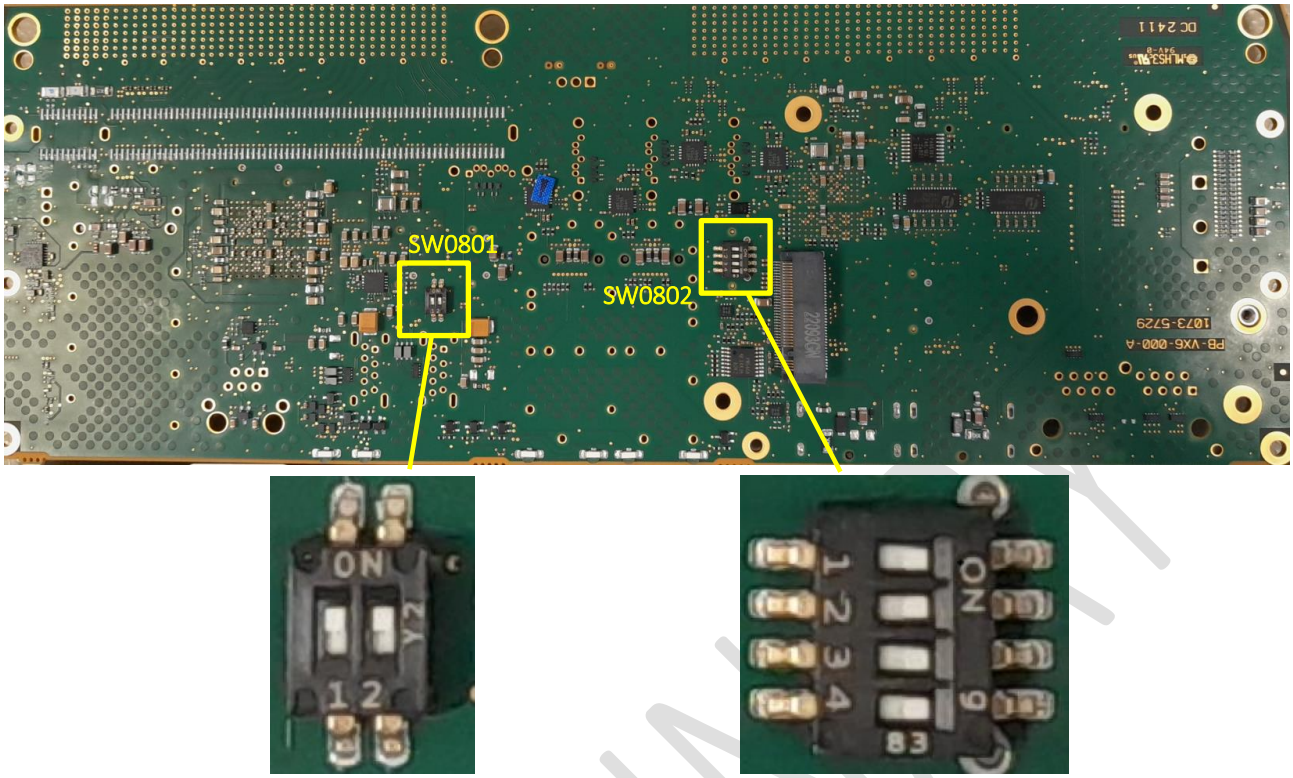


Table 52: RTM - Microswitches

Top Micro Switch / Position	Function	Description
SW0801 / Position 1	NVM write protection mode	OFF: NVM Write protection forced (default) ON: NVM Write protection not forced
SW1201 / Position 2	RTM Master Reset Mode	OFF: Normal Operation default) ON: Reserved
SW0802/ Position 1	RP0 Voltage Translator mode	OFF: Normal Operation default) ON: Reserved
SW0802/ Position 2	RP0 Voltage Translator mode	OFF: Normal Operation default) ON: Reserved
SW0802/ Position 3	SMB	OFF: Normal Operation default) ON: Reserved
SW0802/ Position 4	SFI2PHY Voltage Translator mode	OFF: Normal Operation default) ON: Reserved

Default setting is OFF for all switches.
OFF for all switches is the normal operation mode

20.8. RTM Installation

The standard precautions and installation procedures must also be observed to ensure proper installation and to prevent damage to the board, other system components, or injury to personnel.

20.9. RTM Physical I/Os

20.9.1. RTM Connectors overview

Figure 36: RTM – RTM Connectors – Top Side

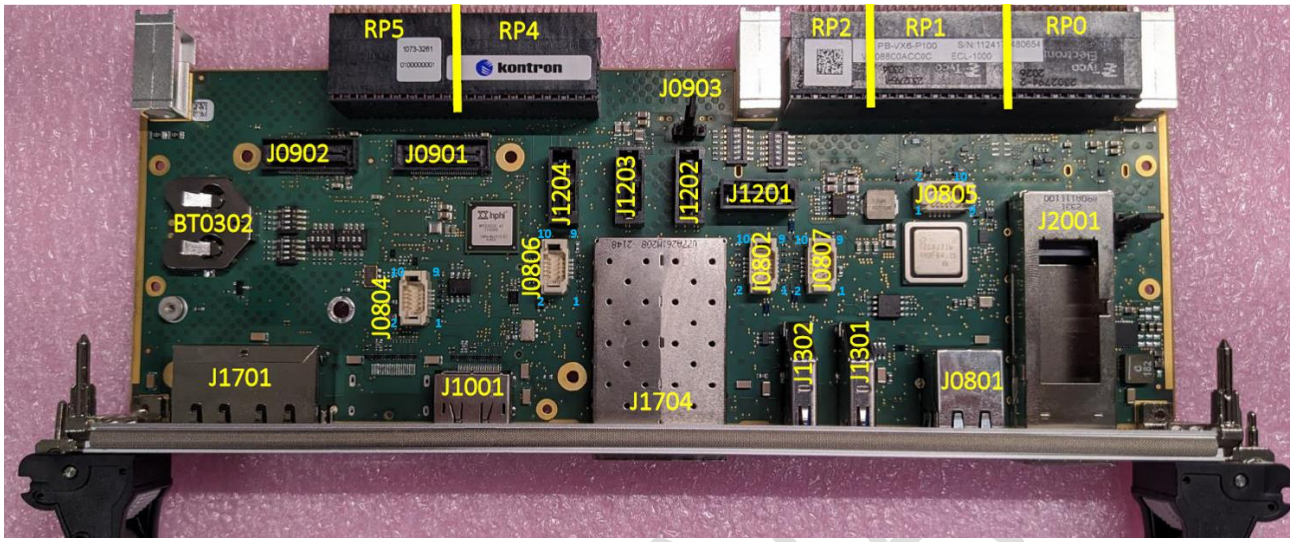
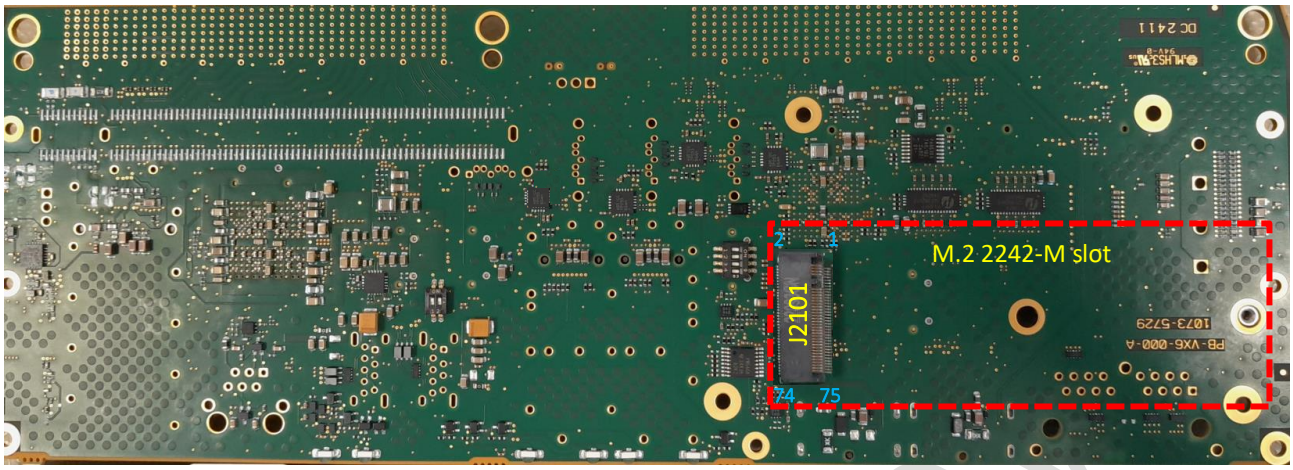


Table 53: RTM - Connectors

Top Side	Description	Connector type
J1701	Dual RJ45 Ethernet ports (1000-BaseT)	
J1001	DP1.2 Display Port interface	
J1704	Dual SFP+ Ethernet Interfaces	
J1301, J1302	USB3.0 Type A Receptacle	
J0801	Serial line interfaces	RJ12
J2001	QSFP+/QSFP28 Ethernet Interface	
BT0302	2032 Coin Cell Battery socket	CR2032 socket
J0802, J0807	GPIO interface	SAMTEC T1M-05-GF-DV-K
J0804	JTAG interface	SAMTEC T1M-05-GF-DV-K
J0805	Serial ports	SAMTEC T1M-05-GF-DV-K
J0806	I2C interfaces	SAMTEC T1M-05-GF-DV-K
J0901 / J0902	XMCIO interface	QSH-030-01-L-D-A
J0903	5V power selection P1-P2 ON: Normal operation – Default (internal 5V power rail selected) P2-P3 ON: Reserved	
J1201	SATA0 Interface	
J1202	SATA1 Interface	
J1203	SATA2 Interface	
J1204	SATA3 Interface	
RP0 to RP5	VPX rear connectors	

Table 54: RTM – On-board Connectors – Bottom Side



Bottom Side	Description	Comment
J2101	M.2 socket type M socket SATA port or NVME port (up to x4) depending on STR01~STR04 upstream link mode coming from the VX6096 LRU (VPX P4 wafers 1 to 4)	for the M.2 2242-M slot

20.9.2. RTM Front Panel - Maintenance Port Connector (J0801)

The RTM provides two serial maintenance ports, COM1 and COM2 on front panel RJ12 connector. COM1 and COM2 can operate simultaneously in EIA-232 mode only (simplified RX/TX) or in 3.3V LVCMOS level signaling.
Defaults setting are :

- Processor console is redirected on COM1
- Serial mode is simplified serial line mode Rx/Tx only, 115200 bauds

Each serial port is configurable via the BIOS setup menu as EIA-232 or 3.3V LVCMOS level signaling.

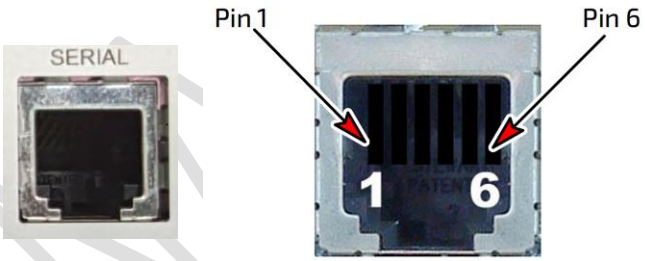
COM1 refers to the MP01 Serial interface on the VPX P1 Connector.

› Pin Assignment

Table 55: RTM – Serial RJ12 Connector Pin Assignment (J0801)

PIN	SIGNAL	DESCRIPTION
1	Reserved	
2	Shell	Chassis Ground
3	COM1 TXD	EIA-232 COM1 Transmit Data
4	COM1 RXD	EIA-232 COM1 Receive Data
5	GND	Ground
6	Reserved	

Figure 37: RTM - Serial RJ12 Connector (J0801)



› Serial Cable Designation

The Serial cable shall be shielded and shall provide a good shielding continuity between each end. The Serial cable length should not exceed 10 m.

Serial cable is a RJ-12 (6 pin, 6 conductors). A RJ-12 to DB9 male or DB9 female adapter is available from multiple sources, such as: Kontron Order Code KIT-RJ12DB9

Table 56: Serial Cable Pin Assignment

DB9 Pin Connector	Signal	RJ-12 Pin Connector
-	-	1
2	TXD	3
3	RXD	4
-	-	6
5	GND	5

Figure 38: Serial Cable

20.9.3. RTM VPX RP0 Connector

Table 57: RTM - Rear I/O VPX Connector RP0 Wafer Assignment

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	NO WAFER						
2	+12V	+12V	+12V	NC	NC (+12V)	NC (+12V)	NC (+12V)
3	NC	NC	NC	NC	NC	NC	NC
4	IPMB_B CLK	IPMB_B DAT	GND	-12V_AUX	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3V3_AUX	GND	IPMB_A CLK	IPMB_A DAT
6	GA3*	GA2*	GND	NC	GND	GA1*	GA0*
7	TCK	GND	TDO	TDI	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND
9	Gdiscrete1	GND	NC	NC	GND	NC	NC
10	GND	NC	NC	GND	NC	NC	GND
11	VBAT	GND	NC	NC	GND	NC	NC
12	GND	NC	NC	GND	NC	NC	GND
13	SYS_CON*	GND	DP1-ETH L0-TX-	DP1-ETH L0-TX+	GND	DP1-ETH L0-RX-	DP1-ETH L0-RX+
14	GND	DP1-ETH L1-TX-	DP1-ETH L1-TX+	GND	DP1-ETH L1-RX-	DP1-ETH L1-RX+	GND
15	GPIO1	GND	DP1-ETH L2-TX-	DP1-ETH L2-TX+	GND	DP1-ETH L2-RX-	DP1-ETH L2-RX+
16	GND	DP1-ETH L3-TX-	DP1-ETH L3-TX+	GND	DP1-ETH L3-RX-	DP1-ETH L3-RX+	GND
CASE	GND						

* signal active when low

Table 58: RTM - Rear I/O VPX Connector RP0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
+12V	+12 Volts DC power (VPX supply).
-12V_AUX	-12 Volts auxiliary power
3V3_AUX	+3.3 Volts auxiliary power. Not required because it generate internally is 3V3_AUX power rail is not present on the backplane.
NVMRO	Non-Volatile Memory Read Only. When asserted (logical 1), prevents any non-volatile memory from being updated.
GAi	Geographical address pins
GAP	Geographical address parity
GND	Ground
IPMB_A	VPX IPMB/I2C Bus A
IPMB_B	VPX IPMB/I2C Bus B
REF_CLK+/-	The Reference Clock is a bussed differential pair.
AUX_CLK+/-	1 PPS (one pulse per second) clock input.
SYSRESET*	System Reset. Input and open collector output.
NC	“Not connected”
DPxx	Ethernet links
Gdiscrete1	Open VPX Gdiscrete1 signal
GPIO01	General Purpose I/O 1
GND	Ground
SYS_CON	System Controller Slot Indication
VBAT	Source for RTC backup voltage
TCK, TDI, TDO, TMS, TRST	JTAG interface

20.9.4. RTM VPX RP1 Connector

Table 59: RTM - Rear I/O VPX Connector RP1 Wafer Assignment

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	COM1 TXD	GND	NC	NC	GND	NC	NC
2	GND	NC	NC	GND	NC	NC	GND
3	COM1 RXD	GND	NC	NC	GND	NC	NC
4	GND	NC	NC	GND	NC	NC	GND
5	GPIO2	GND	NC	NC	GND	NC	NC
6	GND	NC	NC	GND	NC	NC	GND
7	Maskable Reset*	GND	NC	NC	GND	NC	NC
8	GND	NC	NC	GND	NC	NC	GND
9	AXreset1*	GND	EP-PCI L0-TX-	EP-PCI L0-TX+	GND	EP-PCI L0-RX-	EP-PCI L0-RX+
10	GND	EP-PCI L1-TX-	EP-PCI L1-TX+	GND	EP-PCI L1-RX-	EP-PCI L1-RX+	GND
11	AXreset2*	GND	EP-PCI L2-TX-	EP-PCI L2-TX+	GND	EP-PCI L2-RX-	EP-PCI L2-RX+
12	GND	EP-PCI L3-TX-	EP-PCI L3-TX+	GND	EP-PCI L3-RX-	EP-PCI L3-RX+	GND
13	GPLVDS1-	GND	EP-PCI L4-TX-	EP-PCI L4-TX+	GND	EP-PCI L4-RX-	EP-PCI L4-RX+
14	GND	EP-PCI L5-TX-	EP-PCI L5-TX+	GND	EP-PCI L5-RX-	EP-PCI L5-RX+	GND
15	GPLVDS1+	GND	EP-PCI L6-TX-	EP-PCI L6-TX+	GND	EP-PCI L6-RX-	EP-PCI L6-RX+
16	GND	EP-PCI L7-TX-	EP-PCI L7-TX+	GND	EP-PCI L7-RX-	EP-PCI L7-RX+	GND
CASE	GND						

* signal active when low

Table 60: RTM - Rear I/O VPX Connector RP1 Signal Definition

MNEMONIC	SIGNAL DEFINITION
EP-PCI xx	Expansion plane PCIe interface/lanes
AXresetxx	Reserved for VITA 66 manufacturing options – Contact Kontron
GPlvdsxx	LVDS General purpose IO
GPIOx	General purpose input/output
GND	Ground
NC	“Not connected”
COM1	Simplified EIE-232 port (Tx/Rx only)
Maskable Reset*	Maskable Reset signal as per VITA

20.9.5. RTM VPX RP2 Connector

Table 61: RTM - Rear I/O VPX Connector RP2 Wafer Assignment

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	GPLVDS2-	GND	EP-PCI L8-TX-	EP-PCI L8-TX+	GND	EP-PCI L8-RX-	EP-PCI L8-RX+
2	GND	EP-PCI L9-TX-	EP-PCI L9-TX+	GND	EP-PCI L9-RX-	EP-PCI L9-RX+	GND
3	GPLVDS2+	GND	EP-PCI L10-TX-	EP-PCI L10-TX+	GND	EP-PCI L10-RX-	EP-PCI L10-RX+
4	GND	EP-PCI L11-TX-	EP-PCI L11-TX+	GND	EP-PCI L11-RX-	EP-PCI L11-RX+	GND
5	GPIO3	GND	EP-PCI L12-TX-	EP-PCI L12-TX+	GND	EP-PCI L12-RX-	EP-PCI L12-RX+
6	GND	EP-PCI L13-TX-	EP-PCI L13-TX+	GND	EP-PCI L13-RX-	EP-PCI L13-RX+	GND
7	GPIO4	GND	EP-PCI L14-TX-	EP-PCI L14-TX+	GND	EP-PCI L14-RX-	EP-PCI L14-RX+
8	GND	EP-PCI L13-TX-	EP-PCI L15-TX+	GND	EP-PCI L15-RX-	EP-PCI L15-RX+	GND
CASE	GND						

* signal active when low

Table 62: RTM - Rear I/O VPX Connector RP2 Signal Definition

MNEMONIC	SIGNAL DEFINITION
EP-PCI xx	Expansion plane PCIe interface/lanes
GPlvdsxx	LVDS General purpose IO
GPIOx	General purpose input/output
GND	Ground

20.9.6. RTM VPX RP4 Connector

Table 63: RTM - Rear I/O VPX Connector RP4 Wafer Assignment

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	COM2 TXD-	GND	STR L0-TX+	STR L0-TX-	GND	STR L0-RX+	STR L0-RX-
2	GND	STR L1-TX+	STR L1-TX-	GND	STR L1-RX+	STR L1-RX-	GND
3	COM2 TXD+	GND	STR L2-TX+	STR L0-TX-	GND	STR L2-RX+	STR L2-RX-
4	GND	STR L3-TX+	STR L3-TX-	GND	STR L3-RX+	STR L3-RX-	GND
5	VID1-PWR	GND	VID-D1-	VID-D1+	GND	VID-D0-	VID-D0+
6	GND	VID-D3-	VID-D3+	GND	VID-D2-	VID-D2+	GND
7	VID-HPD	GND	VID-AUX-	VID-AUX+	GND	GPLVDS3-	GPLVDS3+
8	GND	USB2-SST-	USB2-SST+	GND	USB2-SSR-	USB2-SSR+	GND
9	USB1-VBUS	GND	USB2-D-	USB2-D+	GND	USB1-D-	USB1-D+
10	GND	USB1-SST-	USB1-SST+	GND	USB1-SSR-	USB1-SSR+	GND
11	USB2-VBUS	GND	ETH1-TX-	ETH1-TX+-	GND	ETH1-RX-	ETH1-RX+
12	GND	ETH0-TX-	ETH0-TX+	GND	ETH0-RX-	ETH0-RX+	GND
13	COM2 RXD-	GND	ETH6-DB-	ETH6-DB+	GND	ETH6-DA-	ETH6-DA+
14	GND	ETH6-DD-	ETH6-DD+	GND	ETH6-DC-	ETH6-DC+	GND
15	COM2 RXD+	GND	ETH5-DB-	ETH5-DB+	GND	ETH5-DA-	ETH5-DA+
16	GND	ETH5-DD-	ETH5-DD+	GND	ETH5-DC-	ETH5-DC+	GND
CASE	GND						

* signal active when low

Table 64: RTM - Rear I/O VPX Connector RP4 Signal Definition

MNEMONIC	SIGNAL DEFINITION
STR_xx	Storage port/interface
VIDxx	Display Port 1.2 video link
USBx_SSxx	USB3.0 Gen1 Super Speed port
USBx_Dx USBx_VBUS	USB2 ports USB2 VBUS
ETH0-xx ETH1-xx	Serdes Ethernet ports
ETH5-xx ETH6-xx	1000Base-T Ethernet ports
COM2_xx	Multi-protocol Rx/Tx Serial port (RS-232, RS-422/485)
GND	Ground

20.9.7. RTM VPX RP5 Connector

Table 65: RTM - Rear I/O VPX Connector RP5 Wafer Assignment

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	COM3 TXD	GND	XMCIO_S23	XMCIO_S21	GND	XMCIO_S24	XMCIO_S22
2	GND	XMCIO_S19	XMCIO_S17	GND	XMCIO_S20	XMCIO_S18	GND
3	COM3 RXD	GND	XMCIO_S15	XMCIO_S13	GND	XMCIO_S16	XMCIO_S14
4	GND	XMCIO_S11	XMCIO_S09	GND	XMCIO_S12	XMCIO_S10	GND
5	GPIO5	GND	XMCIO_S07	XMCIO_S05	GND	XMCIO_S08	XMCIO_S06
6	GND	XMCIO_S03	XMCIO_S01	GND	XMCIO_S04	XMCIO_S02	GND
7	GPIO6	GND	XMCIO_DP01+	XMCIO_DP01-	GND	XMCIO_DP01+	XMCIO_DP01-
8	GND	XMCIO_DP02+	XMCIO_DP02-	GND	XMCIO_DP03+	XMCIO_DP03-	GND
9	GPIO7	GND	XMCIO_DP10+	XMCIO_DP10-	GND	XMCIO_DP11+	XMCIO_DP11-
10	GND	XMCIO_DP12+	XMCIO_DP12-	GND	XMCIO_DP13+	XMCIO_DP13-	GND
11	GPIO8	GND	XMCIO_DP04+	XMCIO_DP04-	GND	XMCIO_DP05+	XMCIO_DP05-
12	GND	XMCIO_DP06+	XMCIO_DP06-	GND	XMCIO_DP07+	XMCIO_DP07-	GND
13	GPIO9	GND	XMCIO_DP08+	XMCIO_DP08-	GND	XMCIO_DP09+	XMCIO_DP09-
14	GND	XMCIO_DP14+	XMCIO_DP14-	GND	XMCIO_DP15+	XMCIO_DP15-	GND
15	GPIO10	GND	XMCIO_DP16+	XMCIO_DP16-	GND	XMCIO_DP17+	XMCIO_DP17-
16	GND	XMCIO_DP18+	XMCIO_DP18-	GND	XMCIO_DP19+	XMCIO_DP19-	GND
CASE	GND						

* signal active when low

Table 66: RTM - Rear I/O VPX Connector RP5 Signal Definition

MNEMONIC	SIGNAL DEFINITION
XMCIO_Sxx	XMCIOs (Single Ended) routed to J0901 and J0902 – Contact Kontron
XMCIO_DPxx	XMCIOs (Differential pairs) routed to J0901 and J0902 – Contact Kontron
COM3_xx	Rx/Tx Serial port (EIA-232)
GND	Ground
GPIOx	General purpose input/output

20.9.8. RTM – On-board Connectors

Figure 39: RTM – On-board Connectors – Top Side

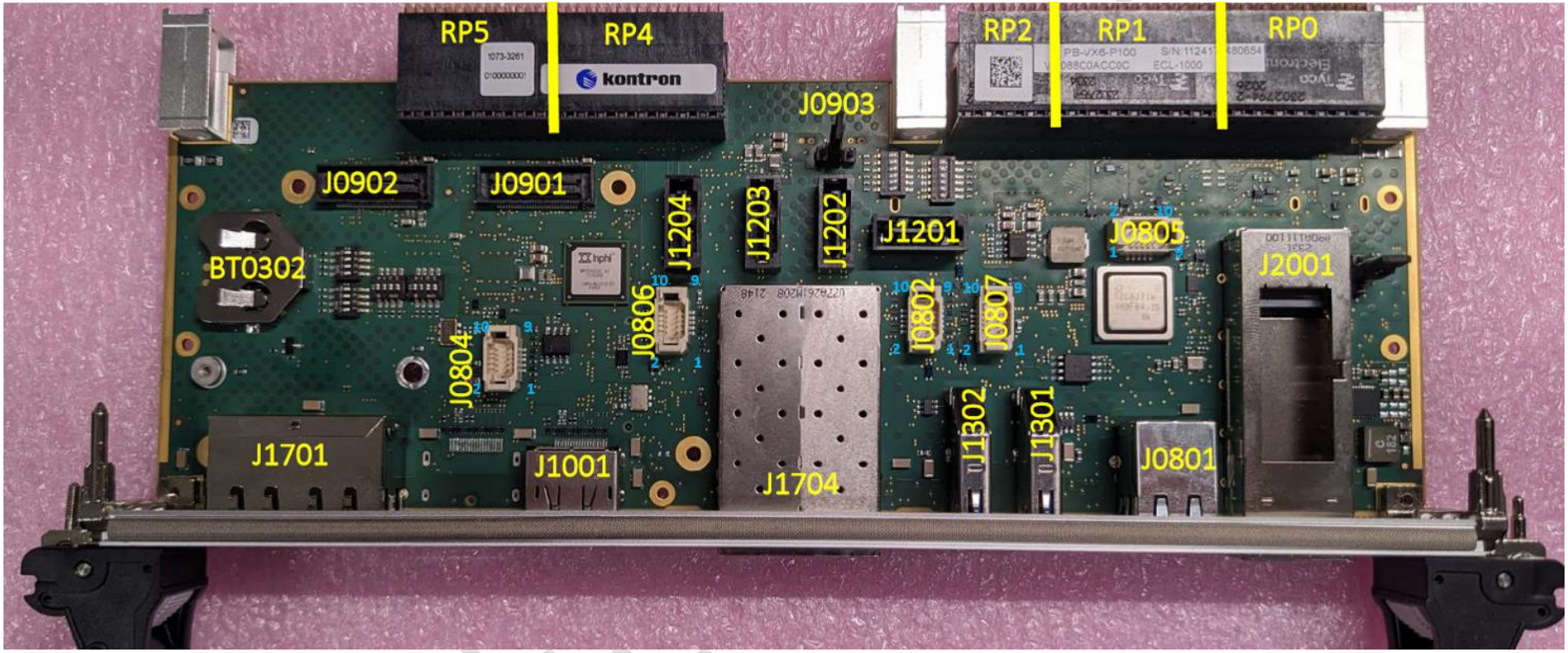


Table 67: On-board Connectors pin assignments when the RTM is used with a VX6096 board

Active low signal			RTM means PB-VX6-0000				
VX6096 Interface	**VX6096 VPX output signal name**	**VX6096 VPX Pin**	**RTM VPX input pin**	**RTM VPX input signal name**	**RTM Header/pin**	**RTM Header P/N**	**RTM Note**
NVMRO	NVMRO	VPX P0-A4	RP0-A4	RP0_NVMRO	-		Tied to SW0801/Position 1
RESET	SYSRESET*	VPX P0-B4	RP0-B4	RP0_SYSRESET*			Tied to SW0801/Position 2
				3V3	J0806/pin2	SAMTEC T1M-05-GF-DV-K	
				GND	J0806/pin9	SAMTEC T1M-05-GF-DV-K	
SMB	SMB0_DAT	VPX P0-A5	RP0-A5	RP0_IPMB_A_DAT	J0806/pin3	SAMTEC T1M-05-GF-DV-K	
SMB	SMB0_CLK	VPX P0-B5	RP0-B5	RP0_IPMB_A_CLK	J0806/pin1	SAMTEC T1M-05-GF-DV-K	
SMB	SMB1_DAT	VPX P0-F4	RP0-F4	RP0_IPMB_B_DAT	J0806/pin7	SAMTEC T1M-05-GF-DV-K	
SMB	SMB1_CLK	VPX P0-G4	RP0-G4	RP0_IPMB_B_CLK	J0806/pin5	SAMTEC T1M-05-GF-DV-K	
				3V3	J0804/pin2	SAMTEC T1M-05-GF-DV-K	
				GND	J0804/pin4	SAMTEC T1M-05-GF-DV-K	
JTAG	TCK	VPX P0-G7	RP0-G7	JTAG_VPX_TCK	J0804/pin1	SAMTEC T1M-05-GF-DV-K	
JTAG	TDO	VPX P0-E7	RP0-E7	JTAG_VPX_TDO	J0804/pin3	SAMTEC T1M-05-GF-DV-K	
JTAG	TDI	VPX P0-D7	RP0-D7	JTAG_VPX_TDI	J0804/pin7	SAMTEC T1M-05-GF-DV-K	
JTAG	TMS	VPX P0-B7	RP0-B7	JVPX_TMS	J0804/pin5	SAMTEC T1M-05-GF-DV-K	
JTAG	TRST*	VPX P0-A7	RP0-A7	JVPX_TRST*	J0804/pin9	SAMTEC T1M-05-GF-DV-K	
				GND	J0807/pin5	SAMTEC T1M-05-GF-DV-K	
GPIO	Gdiscrete1	VPX P1-G1	RP0-G9	Gdiscrete1 OUT (RTM drives to VPX)	J0807/pin6	SAMTEC T1M-05-GF-DV-K	
GPIO	Gdiscrete1	VPX P1-G1	RP0-G9	Gdiscrete1IN (RTM receives from VPX)	J0807/pin10	SAMTEC T1M-05-GF-DV-K	
PWR	P1-VBAT	VPX P1-G3	RP0-G11	V_BAT_RP0	-		Tied to the BT0301 socket
GPIO	GPIO1	VPX P1-G7	RP0-G15	GPIO1	J0802/pin1	SAMTEC T1M-05-GF-DV-K	
				GND	J0805/pin5	SAMTEC T1M-05-GF-DV-K	
Serial	MP01-TD	VPX P1-G9	RP1-G1	COM1_TXD	J0805/pin1	SAMTEC T1M-05-GF-DV-K	
Serial	MP01-RD	VPX P1-G11	RP1-G3	COM1_RXD	J0805/pin3	SAMTEC T1M-05-GF-DV-K	
GPIO	GPIO2	VPX P1-G13	RP1-G5	GPIO2	J0802/pin2	SAMTEC T1M-05-GF-DV-K	
GPIO/RESET	Msk RST (GPIO 11)	VPX P1-G15	RP1-G7	Msk RST (GPIO 11)	J0807/pin8	SAMTEC T1M-05-GF-DV-K	
RESET	AVXReset1*	VPX P2-G1	RP1-G9	AX_RESET1*	-		Tied to SW0801/Position 1
RESET	AVXReset3*	VPX P2-G3	RP1-G11	AX_RESET2*	J0902/pin15 (PIM slot) J1401/pinA11 (PCIE slot) J2101/pin50 (M.2 slot)		
GPI	GPlvds01-	VPX P2-G5	RP1-G13	GP1_LVDS-	J0807pin3	SAMTEC T1M-05-GF-DV-K	
GPI	GPlvds01+	VPX P2-G7	RP1-G15	GP1_LVDS+	J0807/pin10	SAMTEC T1M-05-GF-DV-K	
GPI	GPlvds02-	VPX P2-G9	RP2-G1	GP2_LVDS-	J0807/pin9	SAMTEC T1M-05-GF-DV-K	
GPI	GPlvds02+	VPX P2-G11	RP2-G3	GP2_LVDS+	J0807/pin7	SAMTEC T1M-05-GF-DV-K	
GPIO	GPIO3	VPX P2-G13	RP2-G5	GPIO3	J0802/pin3	SAMTEC T1M-05-GF-DV-K	
GPIO	GPIO4	VPX P2-G15	RP2-G7	GPIO4	J0802/pin4	SAMTEC T1M-05-GF-DV-K	
Serial	SER01-TX-	VPX P4-G1	RP4-G1	COM2_TXD-	J0805/pin4	SAMTEC T1M-05-GF-DV-K	
Serial	SER01-TX+	VPX P4-G3	RP4-G3	COM2_TXD+	J0805/pin2	SAMTEC T1M-05-GF-DV-K	
Serial	SER01-RX-	VPX P4-G13	RP4-G13	COM2_RXD-	J0805/pin10	SAMTEC T1M-05-GF-DV-K	
Serial	SER01-RX+	VPX P4-G15	RP4-G15	COM2_RXD+	J0805/pin8	SAMTEC T1M-05-GF-DV-K	
Serial	MP02-TD	VPX P5-G1	RP5-G1	COM3_TXD	J0805/pin7	SAMTEC T1M-05-GF-DV-K	
Serial	MP02-RD	VPX P5-G3	RP5-G3	COM3_RXD	J0805/pin9	SAMTEC T1M-05-GF-DV-K	
GPIO	GPIO5	VPX P5-G5	RP5-G5	GPIO5	J0802/pin5	SAMTEC T1M-05-GF-DV-K	
GPIO	GPIO6	VPX P5-G7	RP5-G7	GPIO6	J0802/pin6	SAMTEC T1M-05-GF-DV-K	
GPIO	GPIO7	VPX P5-G9	RP5-G9	GPIO7	J0802/pin7	SAMTEC T1M-05-GF-DV-K	
GPIO	GPIO8	VPX P5-G11	RP5-G11	GPIO8	J0802/pin8	SAMTEC T1M-05-GF-DV-K	
GPIO	GPIO9	VPX P5-G13	RP5-G13	GPIO9	J0802/pin9	SAMTEC T1M-05-GF-DV-K	
GPIO	GPIO10	VPX P5-G15	RP5-G15	GPIO10	J0802/pin10	SAMTEC T1M-05-GF-DV-K	

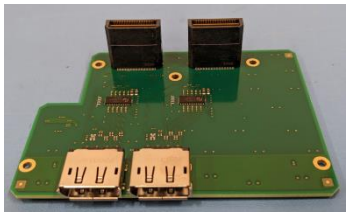
20.9.9. PIM-VX-2DP-WOLF option

Ask to Kontron for more information

Thanks to J0901 and J0902, an optional module can be plugged on the RTM to route the XMCIO of the VX6096 (J15/J16) to the front panel connectors of the RTM.

A PIM-VX-2DP-WOLF is available to route two Display port of the Wolf 3476 XMC module to the RTM front panel.

Figure 40: PIM-VX-2DP-WOLF module



When plugged, the total height of the RTM is increased from 5 HP to 7.5 HP.
The total mass is also increased.
When 347632-F000-000XMCv30 is installed on a VX6096, and the PIM-VX-2DP-WOLF installed on the RTM, the two display ports on the PIM-VX-2DP-WOLF will be functional for lab use.

Figure 41: RTM with the optional PIM-VX-2DP-WOLF module installed

The PIM-VX-2DP-WOLF provides two standard DP front connector offering two additional DP graphics interface on front panel of the RTM (named DP B and DP C)

Figure 42: PIM-VX-2DP-WOLF module – DP A and DP B ports

21. Technical Support

For technical support, contact our Support Department:
E-Mail: support.KFR@kontron.com
Phone: +33-498-163-400

Make sure you have the following information available when you call:
Product ID Number (PN),
Serial Number (SN)

The serial number can be found on the Type Label, located on the product's rear side.

Be ready to explain the nature of your problem to the service technician.

22. Warranty

Due to their limited service life, parts that by their nature are subject to a particularly high degree of wear (wearing parts) are excluded from the warranty beyond that provided by law. This applies to the CMOS battery, for example.

If there is a protection label on your product, then the warranty is lost if the product is opened.

23. Returning Defective Merchandise

All equipment returned to Kontron must have a Return of Material Authorization (RMA) number assigned exclusively by Kontron. Kontron cannot be held responsible for any loss or damage caused to the equipment received without an RMA number. The buyer accepts responsibility for all freight charges for the return of goods to Kontron's designated facility. Kontron will pay the return freight charges back to the buyer's location in the event that the equipment is repaired or replaced within the stipulated warranty period. Follow these steps before returning any product to Kontron.
Visit the RMA Information website: https://www.kontron.com/en/support/rma-information

TO REQUEST A RETURN MATERIAL AUTHORIZATION (RMA) NUMBER

1. E-mail to repair.KFR@kontron.com with the following information:
2. Part number, serial number of the material to be returned,
3. Failure description or reason for return
4. Once everything is completed, an RMA form will be sent to you if your equipment is under warranty. If your equipment is not under warranty, a quote will be sent and the RMA will be sent when we receive your PO.
5. Print the RMA form and put it with the material to be returned
6. Ship the goods to the address indicated on the RMA form

The goods for repair must be packed properly for shipping, considering shock and ESD protection.

Goods returned to Kontron Modular Computers S.A.S in non-proper packaging will be considered as customer caused faults and cannot be accepted as warranty repairs.

About Kontron

Kontron is a global leader in IoT/Embedded Computing Technology (ECT) and offers individual solutions in the areas of Internet of Things (IoT) and Industry 4.0 through a combined portfolio of hardware, software and services. With its standard and customized products based on highly reliable state-of-the-art technologies, Kontron provides secure and innovative applications for a wide variety of industries. As a result, customers benefit from accelerated time-to-market, lower total cost of ownership, extended product lifecycles and the best fully integrated applications.

For more information, please visit: **www.kontron.com**

Your Contact

Kontron Modular Computers S.A.S

150 rue Marcelin Berthelot
ZI de Toulon-Est – BP 244
83078 Toulon Cedex 9, France
Tel.: + 33 4 98 16 34-00
sales.KFR@kontron.com

Global Headquarters

Kontron Europe GmbH

Gutenbergstraße 2
85737 Ismaning, Germany
Tel.: + 49 821 4086-0
info@kontron.com

www.kontron.com