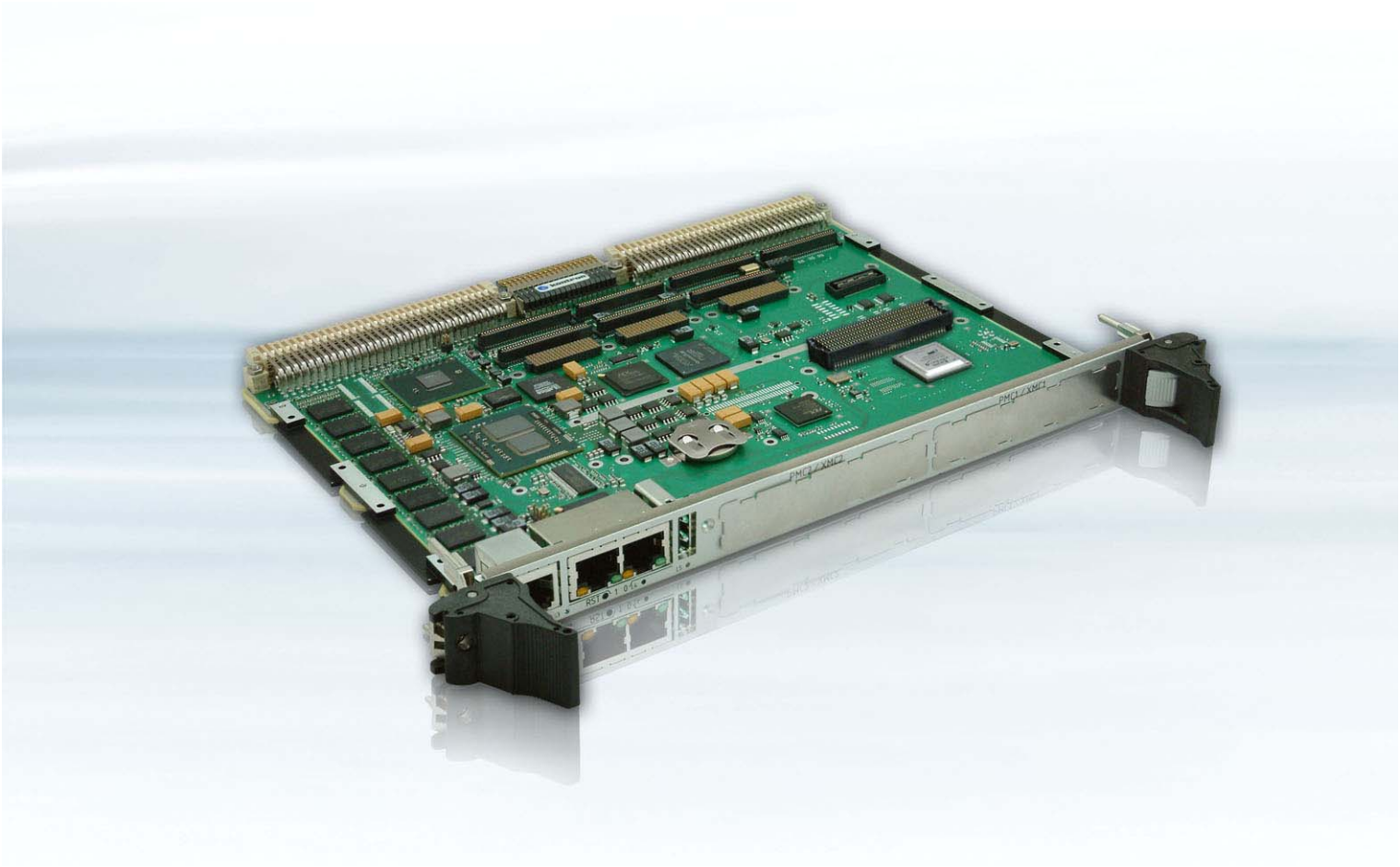
HARDWARE
RELEASE NOTES



VM6050

CA.DT.A94.4e - March 2016

POSSIBILITIES START HERE kontron

VM6050 Hardware Release Notes

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REVISION HISTORY

PUBLICATION TITLE:	VM6050 Hardware Release Notes	
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Revision	Brief Description of Changes	Date of Issue
4e	E.C. Levels 02029 and 02039 added	03-2016
3e	E.C. Levels 02009 and 02019 added	09-2014
2e	Add of E.C. Levels 02006, 02016, 02007, 02017, 02008, 02018 and of RA/RC Mechanical E.C. Levels Update of Revision Guide for MOD-GX	07-2013
1e	Add of E.C. Level 02005	06-2012
0e	Initial Version	04-2012

SYMBOLS

The following symbols may be used in this manual:

DANGER DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.

WARNING WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.

CAUTION CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.

NOTICE NOTICE indicates a property damage message.

Electric Shock!
This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material. Please refer also to the "High-Voltage Safety Instructions" portion below in this section.

ESD Sensitive Device!
This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.

This symbol indicates general information about the product and the user manual.
This symbol also indicates detail information about the specific product configuration.

This symbol precedes helpful hints and tips for daily use.

FOR YOUR SAFETY

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution, in case of danger, the power connector is the product's main disconnect device and must be easily accessible.

⚠CAUTION

Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.

Caution, Electric Shock!
Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.
Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last disconnected or the first connected during operations of cabling.

Special Handling and Unpacking Instructions

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

GENERAL INSTRUCTIONS ON USAGE

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction.

ENVIRONMENTAL PROTECTION STATEMENT

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Environmental protection is a high priority with Kontron. Kontron follows the DEEE/WEEE directive. You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- reduce waste arising from electrical and electronic equipment (EEE)
- make producers of EEE responsible for the environmental impact of their products, especially when they become waste
- encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- improve the environmental performance of all those involved during the lifecycle of EEE

TRADEMARKS

This document may include names, company logos and trademarks, which are registered trademarks and, therefore, proprietary to their respective owners.

Table Of Contents

1 / Introduction

This document describes the engineering evolution of the referenced products to the up-to-date ones which are detailed in the Kontron hardware documentation.

NOTICE

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

You will find in the following pages:

This document applies to all available VM6050 Environment Classes: Standard (SA), Extended Temperature Air-Cooled (WA), Rugged Air-Cooled (RA) and Rugged Conduction-Cooled (RC) versions.

If a specific information applies only to a specific environment class, it is clearly specified in the information description. For example, the reference VM6050/RC applies only to VM6050 Rugged Conduction-Cooled environment class.

This document refers to the up-to-date release of the following hardware documentation:

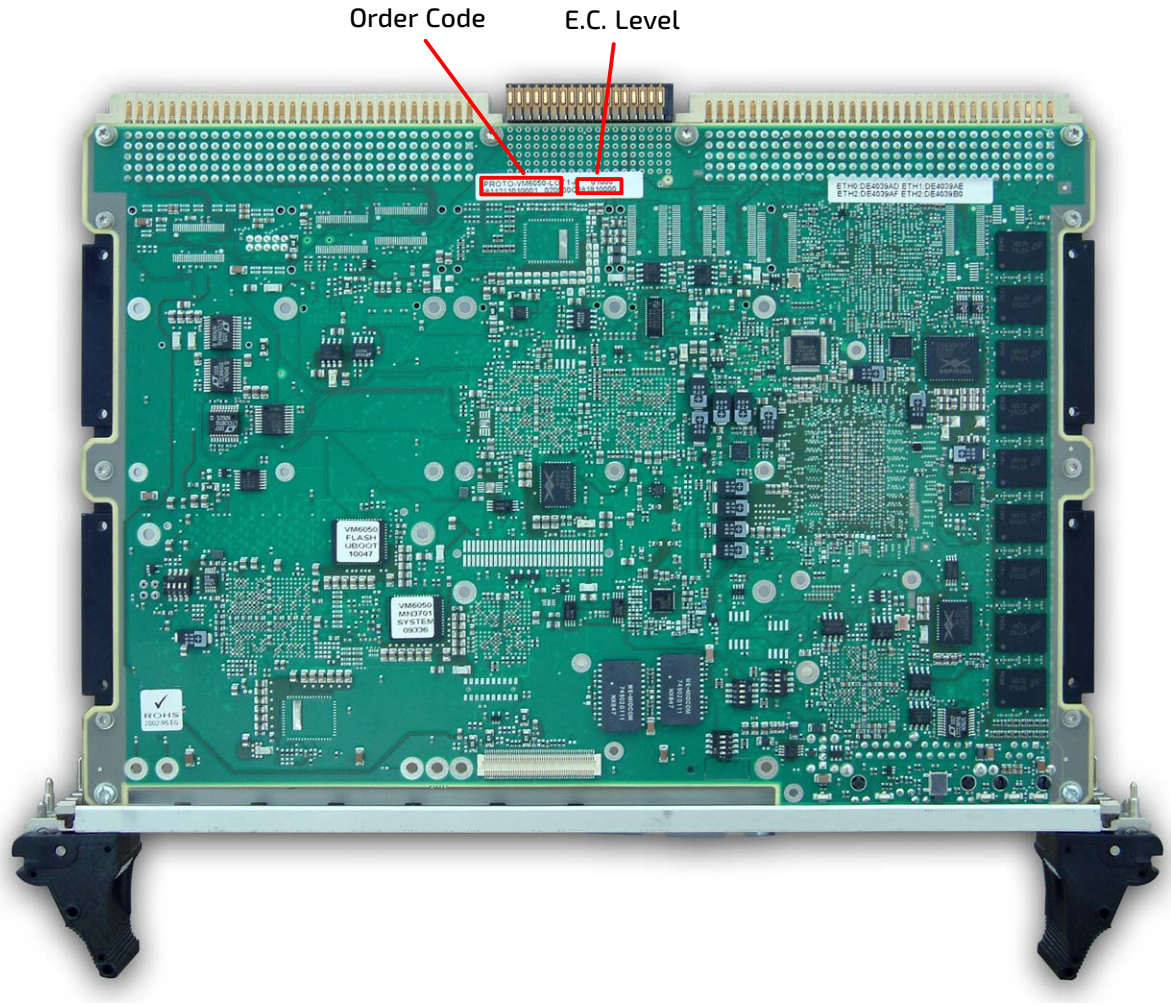
- VM6050 User's Guide CA.DT.A93

2 / Board Identification

2.1 VM6050

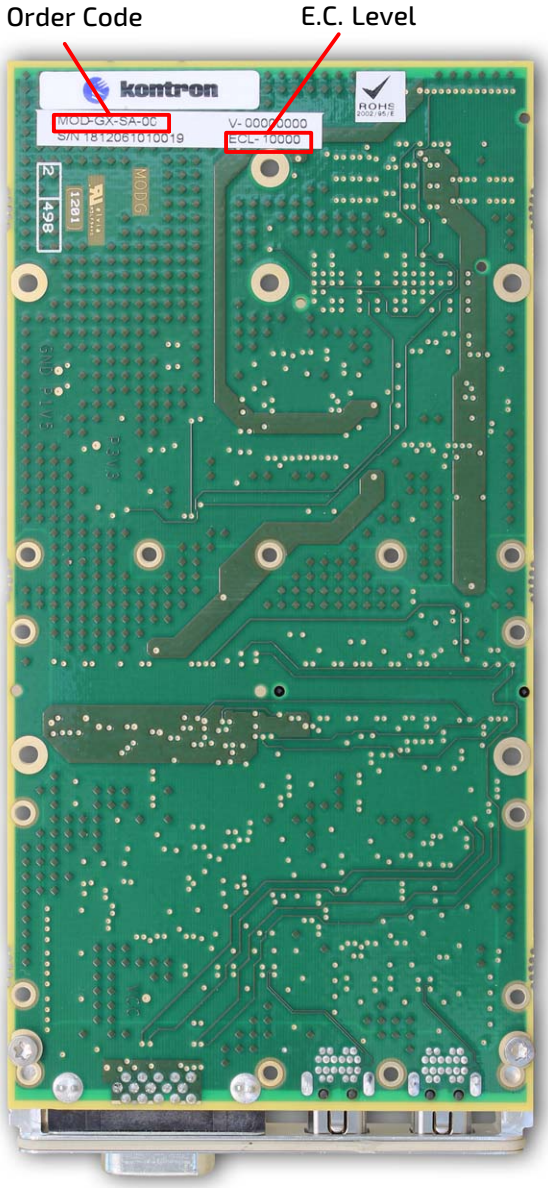
Engineering Change Level and Order Code

The Engineering Change Level (E.C. Level) and the Order Code informations are available on the “Board Identification" label, located on the bottom side of the board.



2.2 MOD-GX

The Engineering Change Level (E.C. Level) and the Order Code informations are available on the “Board Identification" label, located on the bottom side of the board.



3 / General Information

Personal Injuries

VM6050/SA/WA

⚠CAUTION

- Do not touch the CPU heatsink while removing the board from a rack because it can get very hot.
- Be careful while handling the board, because of the cutting edges of the heatsink.
- Do not place the board on any surface or in any form of storage container until the board and its heatsink have cooled down to room temperature.

VM6050/RC/RA

⚠CAUTION

- Do not touch the ruggedizer while removing the board from a rack because it can get very hot.
- Do not place the board on any surface or in any form of storage container until the board and its ruggedizer have cooled down to room temperature.

PMCs Signaling Level

The PCI PMC V(I/O) voltage level is +3.3V only. It is not +5V tolerant. The user must check that its PMC type is compatible with this signaling voltage (refer to the Chapter "PMC Sites" in the VM6050 User's Guide).

EMC Gasket

In order to protect the EMC gasket located in the front panel, be careful during the insertion of the boards in the rack. It is recommended to insert the boards in a rack starting from the higher slot number and extract them starting from the lowest slot number.

Power Supplies

On +5V power supply, monotonic rise time no longer than 25 ms is required at Power on.

On +3.3V power supply, monotonic rise time no longer than 25 ms is required at Power on.

For a power off condition to be valid, the +5V and +3.3V power supply input should remain at 0V for at least one second.

Components Height on Top Side of the Board – CRP3980

The front panel connectors are slightly higher than the maximum height specified by the VME standard.

List of the components of the VM6050 that do not comply with the VME standard (13.7 mm top height):

- Front panel Ethernet connectors: 13.80 mm
- Front panel USB connector: 13.83 mm
- Front panel Console (RJ11) connector: 13.84 mm

No impact since the exceeding height is located very close to the front panel.

Height of the Board fitted with the Hard Disk Storage Kit - CRP3979

The height of the VM6050 board fitted with the hard disk storage kit (KIT-DISK25-SATA) is slightly higher than the maximum height as specified by the VME standard.

14.5 mm instead of the required standard of 13.7 mm

Mounting plate	5.9	mm away from the PCB
2.5" disk	9.5	mm thick
Total	15.4	mm

Mounting Ribs conflict with Front IO connector on RC Class board - CRP 3981

Ribs used to improve the PMC conduction cooling are in conflict with Front IO connector when it is fitted. Ribs cannot be used on VM6050 RA/RC classes board when graphic module is plugged.

No impact since graphic module does not required Ribs to be cooled.

PMC Excursion VITA20 requirement not satisfied with RC Class Ruggedizer

PMC location does not satisfy the PMC excursion requirement in VITA 20 standard (see appendix) The distance from PMC edge to VM6050 edge size must be higher than 19.7 mm as specified by the VME standard. The actual size is 10.5 mm instead of the 19.7 mm, minimum that standard required.

VM6050/SA Handling

⚠CAUTION Do not lie the board on the CPU heatsink to avoid damages on the processors.

Unavailable Functionalities

- LynxOS BSP not available.

VITA 31.1 Compliance

The P0 ethernet routing allows to support VITA 31.1 backplane networking but the P0 pinout is not compliant with the VITA 31.1 standard because:

The pins in P0 connector position 1 and 6 are used for PMC I/O, misc signal and rear USB power supplies, whereas VITA 31.1 specifies to keep them Not Connected (NC) to avoid the possibility of interfering with the Ethernet signals.

- **VM6050 P0 Pin Assigment**

PIN	P0 CONNECTOR					
	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	PMC2 IO 39	PMC2 IO 38	PMC2 IO 37	PMC2 IO 36	PMC2 IO 35	GND
2	ETH2 BI_DA+	ETH2 BI_DA-	GND	ETH2 BI_DC+	ETH2 BI_DC-	GND
3	ETH2 BI_DB+	ETH2 BI_DB-	GND	ETH2 BI_DD+	ETH2 BI_DD-	GND
4	ETH3 BI_DA+	ETH3 BI_DA-	GND	ETH3 BI_DC+	ETH3 BI_DC-	GND
5	ETH3 BI_DB+	ETH3 BI_DB-	GND	ETH3 BI_DD+	ETH3 BI_DD-	GND
6	RESET#	USB2 PWR	NVMRO	RTC-BAT	USB3 PWR	GND

- VITA 31.1 Standard - P0 Pin Assigment

PIN	P0 CONNECTOR					
	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	N.C.	N.C.	N.C.	N.C.	N.C.	GND
2	+Txa LPa_DA+	-Txa LPa_DA-	GND	LPa_DC+	LPa_DC-	GND
3	+Rxa LPa_DB+	-Rxa LPa_DB-	GND	LPa_DD+	LPa_DD-	GND
4	+Txb LPb_DA+	-Txb LPb_DA-	GND	LPb_DC+	LPb_DC-	GND
5	+Rxb LPb_DB+	-RXb LPb_DB-	GND	LPb_DD+	LPb_DD-	GND
6	N.C.	N.C.	GND	N.C.	N.C.	GND

To support more efficiently the VITA 31.1 backplane:

- The VM6050 board family uses shielded HSHM P0 connector which suppresses the interference between adjacent pin positions in P0 connector.
- The pins in P0 connector position 1 may be NC by removing 0 ohm network resistor.

4 / Board Revision Guide

4.1 How to Use the Board Revision Guide Table

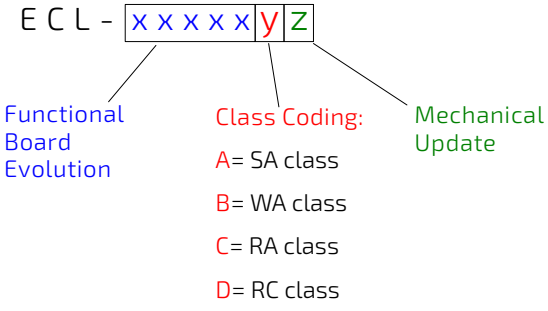
1. Find the E.C. Level associated to your board as described in the Chapter 2 "Board Identification" page 2.
2. Find the column associated to the E.C. Level of your board in this table.
3. Check for a specific item in the table lines:
   - 3.1. A x (cross) in the E.C. Level column indicates that this item applies to this E.C. Level.
   - 3.2. No x (cross) in the E.C. Level column indicates that this item does not apply to this E.C. Level.
   - 3.3. If the functionality described by the item is not available on your board don't take into account this item. To know the functionalities available or not on your board, read the User's Guide associated with your board version.

NOTICE

Each item is fully described in section 4.6 "Item Detailed Description" page 10.

4.2 E.C. Level Coding

The E.C. Level of VM6050 board is composed of a functional part coding and a mechanical part coding. The five first digits are used to code the functional board evolution and the two last digits are used to code the mechanical board evolution, as described as follows:



4.3 Revision Guide Table - Functional E.C. Levels

Item	CRP	DESCRIPTION	E.C. LEVELS															
			02000	02001	02002	02003	02004	02005	02006	02016	02007	02017	02008	02018	02009	02019	02029	02039
1	3984	Missing implementation in CPLD: LED function	X															
2	3985	Missing implementation in CPLD: ALMA2f reset	X															
3	3986	CPLD fix: erroneous character displayed on COM1	X															
4	3987	CPLD fix: reset holding during 5sec at Power On	X															
5	3976	CPLD fix: reset deadlock	X															
6	3989	DP and HDMI cable detection do not work	X															
7	3990	No BIOS prompt available when XMC is plugged in slot 1	X	X														
8	3991	Ibex-Peak watchdog does not work	X	X														
9	3992	Missing implementation in CPLD: PCI 32-bit register function (PMC slot 1)	X	X	X													
10	3993	PCI 64-bit of PMC slot 2 may hang	X	X	X	X												
11	3995	Missing implementation in CPLD: serial line configuration	X	X	X	X												
12	4003	PMC slot 1 clock skew not compliant with PCI 66 Mhz Standard	X	X	X	X												
13	4004	PMC slot 2 clock skew not compliant with PCI 133 MHz	X	X	X	X												
14	3996	Power failure after +3.3 VDC power rail backplane loss	X	X	X	X	X	X	X		X		X					
15	3997	ALMA2f may be not detected at Power On	X	X	X	X	X											
16	3998	VM6050 does not boot up to the BIOS/EFI prompt	X	X	X	X	X											
17	3987	5 sec. reset holding for some boards	X	X	X	X	X											
18	3999	Inconsistent character send on console after shut-down/halt Linux command	X	X	X	X	X	X										
19	4000	PMC Kontron PMC-ETH2 not detected on PMC 32-bit slot 1	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
20	4001	No link or Tx/Rx error on giga ethernet port with 100m cable	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
21	4002	No GND connection with SA heatsink	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
22	3859	DisplayPort display not detected when +5VDC power rail from backplane is lower than 5.0V	X	X	X	X	X											
23	4040	I2C backplane input levels are not respected	X	X	X	X	X	X										
24	4073	No reset propagation to VME in system controller mode	X	X	X	X	X	X										
25	4075	VME SYSRESET propagation to local reset may cause board dysfunction	X	X	X	X	X	X										
26	4064	Reset holding during 4~5sec after hard reset	X	X	X	X	X	X										

Item	CRP	DESCRIPTION	E.C. LEVELS														
			02000	02001	02002	02003	02004	02005	02006	02016	02007	02017	02008	02018	02009	02019	02029	02039
27	4131	VME SYSRESET is not maskable and reset all component of the board	X	X	X	X	X	X	X	X								
28	4132	Image flicker on HDMI/DVI display	X	X	X	X	X	X	X	X								
29	4144	No picture displayed on monitor when using DisplayPort interface	X	X	X	X	X	X	X	X	X	X						
30	4201	GA (geo_id) value in reg 0x6A of CPLD sometimes wrong	X	X	X	X	X	X	X	X	X	X	X	X				
31	4202	Potential reboot due to noise on reset signal	X	X	X	X	X	X	X	X	X	X	X	X				
32	4205	CPLD watchdog issue	X	X	X	X	X	X	X	X	X	X	X	X				
33	4206	Glitches on serial lines at power-on and reset_	X	X	X	X	X	X	X	X	X	X	X	X				
34	4207	OS halt/shutdown and SYSRESET issues	X	X	X	X	X	X	X	X	X	X	X	X				
35	4072	Wrong cPLD boot status after reset	X	X	X	X	X	X										
36	4312	Obsolescence management on SPI BIOS flash															X	X

4.4 Revision Guide Table - RA Mechanical E.C. Levels

Item	CRP	DESCRIPTION	E.C. LEVEL						
			C0	C1	C2	C3			
RA-1	-	Ruggedizer dimension adjustment with regard to processor height tolerance	X						
RA-2	-	PCB bow (warpage)close to rear connector	X						
RA-3	-	Mechanical tolerance and gap isolation adjustment	X						
RA-4	-	No conductive area to Earth on the ruggedizer	X	X					
RA-5	-	Mechanical tolerance adjustment on plot (integrated ring spacer) of ruggedizer	X	X	X				

4.5 Revision Guide Table - RC Mechanical E.C. Levels

Item	CRP	DESCRIPTION	E.C. LEVEL						
			D0	D1	D2				
RC-1	-	Ruggedizer dimension adjustment with regard to processor height tolerance	X						
RC-2	-	Flash mezzanine device disconnection and error during high Z axis vibration	X						
RC-3	-	Mechanical tolerance and gap isolation adjustment	X	X					

4.6 Items Detailed Description - Functional E.C. Levels

NOTICE

Each item applies only to a specific group of E.C. levels.
Refer to the table available in section 4.3 “Revision Guide” page 8 to find the specific E.C. levels associated to a specific item.

Item #1 Missing implementation in CPLD: LED function - CRP 3984

Description : LED 1 to 3 indications are not compliant with the User's Guide description.
LED 4 and 5 are not driven by CPLD and remain lighted off.

Impact: No impact.

Workaround: Fixed by E.C. Level 02001

Item #2 Missing implementation in CPLD: ALMA2f reset - CRP 3985

Description : 250 ms SYSRESET_OUT timer implemented on CPLD is not required on VM6050 because it is managed by ALMA2f. VME bus requires a SYSRESET_OUT activation of 200 ms.
System controller signal (SYSCON) from VME bus has been inverted. A CPLD modification has needed to take into account the logic inversion.

Impact: No impact for SYSRESET_OUT 250 ms activation.
Reset value of bit 0 (LOC2VME) of VME_CTL register in CPLD has wrong value with regard to SYSCON signal for VME bus
Wrong SYSCON bit value in register GEO_ADD (@6A).
BIOS or OS may interpret a board as a system controller board while not.

Workaround: Fixed by E.C. Level 02001

Item #3 CPLD fix: Erroneous character displayed on COM1 - CRP 3986

Description : S1_M0 input signal on COM1 termination circuit not driven by CPLD.

Impact: No impact on input character. Inconsistent output character on serial line COM1.

Workaround: Fixed by E.C. Level 02001

Item #4 CPLD fix: Reset holding during 5 sec. at Power On - CRP 3987

Description : At Power On, the reset is held during 5 sec. (amber LED1) instead of a few seconds.

Impact: BIOS prompt is delayed around 5 seconds.

Workaround: Fixed by E.C. Level 02001

Item #5 CPLD fix: Reset deadlock - CRP 3976

Description : VM6050 is kept in reset if VME SYSRESET or front panel button is asserted more than 34 seconds.

Impact: Reset is held even if it releases. The only way to restart the VM6050 is to power down and power up the power supply of the board.

Workaround: Fixed by E.C. Level 02001

Item #6 DP and HDMI cable detection do not work - CRP 3989

Description : DP and HDMI cable detect hardware function not compatible with MOD-GX or specific graphic board developed by the customer.

Impact: DP or HDMI cable may be not detected when plugged on MOD-GX board.

Workaround: Fixed by E.C. Level 02001

Item #7 No BIOS prompt available when XMC is plugged in slot 1 - CRP 3990

Description : Two root causes explain this problem:

> Ibex-Peak I2C bus disturbance appears when XMC is plugged on slot 1. The reading of SPD (memory configuration) is corrupted and the board can not boot the BIOS.

> XMC reset on slot 1 is not driven by the CPLD, signal is high impedance.

Impact: Inconsistent character appears on serial line and VM6050 hang. No BIOS prompt available.

Workaround: Fixed by E.C. Level 02002

Item #8 Ibex-Peak watchdog does not work - CRP 3991

Description : On VM6050 board, the internal Ibex-Peak Watchdog does not work because the bit 5 of GCS register (No Reboot NR) is set on the PWROK signal activation (strap option). This pin is connected through a resistor to CPLD that disturbs the strap option configuration. Ibex-Peak has a weak internal pull down on this input.

Impact: Ibex-Peak watchdog does not work.

Workaround: Fixed by E.C. Level 02002

Item #9 Missing implementation in CPLD: PCI 32-bit register function (PMC slot 1) - CRP 3992

Description : Support features reg VM6050_PCIMode @0x08 (actually, the register returns always 0 value for PMC BUSMODE1 bit and it systematically indicates that PMC is plugged on PMC slot 1).
PCI M66EN: at power on loading of bit 0 of byte offset 0x103 of VPD EEPROM.

Impact: Erroneous information in register @0x08 of CPLD concerning PMC slot 1.

Workaround: Fixed by E.C. Level 02003

Item #10 PCI 64-bit of PMC slot 2 may hang - CRP 3993

Description : When using a PMC on slot 2 of the VM6050 board, an error can appear and PCI 64-bit bus can hang. PCI device of PMC is no more accessible with configuration cycle. Problem is more sensitive at cold temperature.

Impact: PCI 64-bit of PMC hang. PCI device of PMC is not accessible.
PCI express and PCI errors are recorded in error status register.

Workaround: Fixed by E.C. Level 02004

Item #11 Missing implementation in CPLD: Serial line configuration - CRP 3995

Description : EIA-422/485 serial line mode and termination configuration not yet implemented in CPLD code (support features register @0x07 VM6050_SERIAL_LINES_CTL).

Impact: EIA-232 serial line is the only serial line interface available on VM6050 for COM1 and COM2.

Workaround: Fixed by E.C. Level 02004

Item #12 PMC slot 1 clock skew not compliant with PCI 66 MHz Standard - CRP 4003

Description : The PMC clock signal is 10 cm longer than the other clock device signal on the same bus.

Impact: The PMC board may not be detected at power-on.

Workaround: Fixed by E.C. Level 02004

Item #13 PMC slot 2 clock skew not compliant with PCI 133 MHz Standard - CRP 4004

Description : The PMC clock signal is 10 cm longer than the other clock device signal on the same bus.

Impact: The PMC board may not be detected at power-on.

Workaround: Fixed by E.C. Level 02004

Item #14 Power failure after +3.3 VDC power rail backplane loss - CRP 3996

Description : The VM6050 board may be damaged with power failure default if the +3.3 VDC backplane power rail falls down while +5 VDC backplane power rail remains stable.
To avoid damage at power on, +5 VDC and +3.3 VDC must power-up and power-down at the same time.

Impact: VM6050 board damage with power failure default.

Workaround: Fixed by E.C. Level higher than 02008.

Item #15 ALMA2f may be not detected at Power On - CRP 3997

Description : 5 out of 1000 power-on, ALMA2f is not detected by BIOS around. VME bridge does not appear in the PCI list device under BIOS

Workaround: Fixed by E.C. Level 02005.

Item #16 VM6050 does not boot up to the BIOS/EFI prompt - CRP 3998 - CRP 4033

Description : 5 out of 1000 power-on, BIOS prompt is not available. LED 1 light is on (orange color). VM6050 board is held in system reset state.

Workaround: Fixed by E.C. Level 02005.

Item #17 5 sec. reset holding for some boards - CRP 3987

Description : For some boards, as item #04, the reset is held during 5 sec. instead of a few milliseconds.

Impact: BIOS boot is longer than other VM6050 board.

Workaround: Fixed by E.C. Level 02005.

Item #18 Inconsistent character send on console after shutdown/halt Linux command - CRP 3999

Description : After a shutdown or halt Linux command keyed at prompt, inconsistent character appears on console after Power Down message

Impact: This problem can hang tty terminal window used to display console.

Workaround: No workaround yet.

Item #19 PMC Kontron PMC-ETH2 not detected on PMC 32-bit slot 1 - CRP 4000

Description : The PMC Kontron PMC-ETH2 is not detected when it is plugged on PMC slot 1

Impact: PMC device is not seen under BIOS and OS.

Workaround: No workaround yet.

Item #20 No link or Tx/Rx error on Giga Ethernet port with 100m cable - CRP 4001

Description : When using a 100m Ethernet cable cat 5e on gigabit Ethernet port of VM6050, link may be not up or if it is up, the negation was made at 100Base-T instead of 1000Base-T.
When negotiation is 100Base-T, Rx and Tx error occurred on four Ethernet ports of VM6050 during test.

Impact: Ethernet transfer does not work with 100m cable (transfer error and negotiation fail)

Workaround: Use maximum 50m length cable .

Item #21 No GND connection for SA heatsink - CRP 4002

Description : SA and WA boards use a heatsink with spring mounting. Heatsink is isolated by alodine treatment and a black treatment finition. Then, electric connection cannot be established between spring and heatsink. The heatsink potential is high-Z.

On previous SBC board, GND connexion between board and heatsink was ensured by screw and heatsink thread.

Impact: Heatsink may be assimilated as an antenna and may disturb component on VM6050 board.

Workaround: No workaround yet.

Item #22 DisplayPort display not detected when +5VDC power rail from backplane is lower than 5.0V. - CRP 3859

Description : When +5VDC power rail from VME backplane is lower than 4.95V, DP display is not detected, and no image as BIOS prompt are displayed on screen.
This problem is more sensitive for cold temperature.

Impact: No image displayed on the DP display screen.
Poor resolution can be negotiated under Linux when temperature decreased under 20°C.

Workaround: Fixed in E.C. Level 02005.

Item #23 I2C levels are not respected on the input of I2C backplane - CRP 4040

Description : The LTC4300 I2C chip buffer does not respect, in worst case, the I2C specification for the low level input voltage. In some extreme conditions (voltage and temperature), I2C level may not be respected on IPMB and SMB bus (VME P1 connector).

Impact: Interface errors on IPMB and SMB bus (VME P0 connector) may appear in worst case.

Workaround: Fixed in E.C. Level 02006.
The LTC chip has been replaced by a chip Intersil ISL33002IUZ

Item #24 No reset propagation to VME in system controller mode - CRP 4073

Description : In system controller mode, the following local reset signals are not propagated to VME SYSRESET:
- the warm reset (register CF9h of Ibex Peak)
- the board reset via I2C backplane (LPC register 0x73)

Impact: No reset propagation to VME in system controller mode.

Workaround: ALMA2f must be programmed to propagate the local reset to VME SYSRESET (bit Loc2VME in register @ BAR+0x64)

Or fixed in E.C. Level 02006.
BIOS ID higher than 12184 is required.

Item #25 VME SYSRESET propagation to local reset may cause board dysfunction - CRP 4075

Description : The VME SYSRESET cannot be masked by Alma2f, a VME SYSRESET assertion causes a reset propagation to CPLD (A_RESETOUT#) and causes an internal reset of all register and logic of ALMA2f.
By default, the CPLD is set by BIOS to propagate the VME reset to the local reset, but if the propagation is disabled by user in CPLD by BIOS setup, Alma2f is reset while the other devices of the board continues to run.

Impact: May cause dysfunction of the board. If the VME to local propagation reset is disabled in BIOS setup, ALMA2f may be reseted by VME while the other components of the board are not reseted.

Workaround: Fixed in E.C. Level 02006 and E.C. Level 02016 (cPLD rev 0xD).
To avoid this issue, VME SYSRESET is always propagated to local reset by CPLD rev 0xD, maskable bit has removed. VME SYSRESET is no longer maskable.

Item #26 Reset holding during 4~5sec after hard reset - CRP 4064

Description : After a hard reset, the board is held in reset state during 4~5sec (orange LED1) instead of few milliseconds. Hard reset source are front panel reset, cPLD watchdog, I2C backplane reset

Impact: BIOS prompt is delayed around 5 seconds.

Workaround: Fixed in E.C. Level 02006 (cPLD rev 0xD).

Item #27 VME SYSRESET is not maskable and reset all component of the board - CRP 4131

Description : The propagation of VME to local reset cannot be masked. The VME reset is always propagated to local reset. The user cannot defined the reset behavior of VM6050 board when a VME SYSRESET occurred in VME chassis. The VM6050 will be completely reseted if a VME SYSRESET occurs.

Impact: VM6050 is always reseted when a VME SYSRESET is asserted on backplane.

Workaround: Fixed in E.C Level 2007 and E.C Level 02017 (ALMA2f rev 0x45).
In this new ALMA2f revision, bit 1 of 0x64 UTIL_RST register is used to mask the VME input reset (VME2LOCb bit), the reset value 0 indicates that VME input reset is not masked (then set to 1 to mask VME SYSRESET#). Require at minimum BIOS ID13078.

Item #28 Image flicker on HDMI/DVI display - CRP 4132

Description : In some case, device may cause image flicker on HDMI and DVI display. This issue occurs according to the PCH device sensibility and to monitor sensibility.

Impact: Image flicker may appear on HDMI or DVI display.

Workaround: Fixed in E.C Level 02007 and E.C Level 02017

Item #29 No picture displayed on monitor when using DisplayPort interface - CRP 4144

Description : In worst case when using DisplayPort interface in front of MOD-GX board, some VM6050 board may fail and DisplayPort monitor may remain in standby mode, BIOS prompt and setup are not displayed on screen. This problem does not concern HDMI, DVI and VGA interface.

Workaround: Fixed in E.C Levels 02008 and 02018. Or use DVI/HDMI mode instead of DisplayPort mode.

Item #30 GA (geo_id) value in reg 0x6A of CPLD sometimes wrong - CRP 4201

Description: The Geographical Address is latched from VME backplane signals GAn/GAP at power-on, but the latched value reported in cPLD reg 0x6A is sometimes wrong. This bug also has an impact on the board's mapping on the backplane I2C bus (cPLD I2C0): the board may be mapped at a wrong address or not at all (depending if parity on GAP is seen OK or not).

Workaround: Fixed in E.C Levels 02009 and 02019.

Item #31 Potential reboot due to noise on reset signal - CRP 4202

Description: In worst case, VM6050 board may restart the sequencing of internal power and reset in noisy environments. If this issue occurs, the VM6050 board restarts, a SYSRESET is generated on the VME backplane and causes the reset of all the boards plugged in the backplane.

Workaround: Fixed in E.C. Levels 02009 and 02019.

Item #32 CPLD watchdog issue - CRP 4205

Description: The watchdog has the following issues :

- spurious timeout if watchdog disabled before expiration and then timeout set to the value at which the watchdog counter was stopped,
- timeout = 0 not working (should give a 1s timeout with +0/+1s uncertainty)
- LED2 not red after reset by watchdog (cleared to green immediately by reset)
- wrong timeout when timeout updated while watchdog enabled (running)

Workaround: Fixed in E.C Levels 02009 and 02019.

Item #33 Glitches on serial lines at power-on and reset - CRP 4206

Description: On COM1: at power-on, there is a glitch, then a 50mS active pulse

On COM2: at power-on, there is a glitch, then a 3s active pulse, at reset, there's a 3s active pulse

Workaround: Fixed in E.C Levels 02009 and 02019. This EC level fixes COM1, but a 50mS active pulse still occurs on COM2 at power-on and reset. To remove it, update to BIOS ID>13281 to have COM2 fixed.

Item #34 OS halt/shutdown and SYSRESET issues - CRP 4207

Description: When halt/shutdown is run under OS, the board should halt with a "System halted" message:

- no SYSRESET must be generated even if "SYSRESET output" is set to "Enabled" in BIOS setup
- the board must restart if a SYSRESET occurs.

This is the standard expected behaviour on VME boards. But with Fedora 14 (not with Fedora 16 that does a "System halted") if the OS halt with a "Power down" message, the behavior is not the following.

- a SYSRESET is generated if "SYSRESET output" is set to "Enabled"
- the board does not restart if a SYSRESET occurs

Also if a SYSRESET occurs when the board is already in reset or no more reset for less than a second, this SYSRESET is ignored so the board can restart even if SYSRESET is still asserted.

Workaround: Fixed in E.C Levels 02009 and 02019.

Item #35 Wrong cPLD boot status after reset - CRP 4072

Description: After a reset, the boot status register @72 of cPLD is not re-initialized. For instance, a board which is reseted under Linux keeps its boot status as “OS” up to BIOS boot.

Impact: The impact is poor because the BIOS restarts. However the status boot indicates the board is under OS while it is under EFI/BIOS.

Workaround: No workaround.

Fix: Fixed by E.C. Level 02006.

Item #36 Obsolescence Management on SPI BIOS Flash – CRP 4312

Description: SPI flash used on VM6050 board as firmware boot device is obsolete. The device change requires BIOS modification.

Impact: No impact except if BIOS release is lower than ID15202 on board with E.C. Level 02029 or higher, in this case board does not boot. BIOS ID15202 and higher are compatible with all E.C. Levels.

Workaround: Not applicable.

Fix: Fixed by BIOS ID15202 and higher.

4.7 Items Detailed Description - RA Mechanical E.C. Levels

NOTICE

Each item applies only to a specific group of E.C. levels.
Refer to the table available in section 4.3 "Revision Guide" page 8 to find the specific E.C. levels associated to a specific item.

Item #RA-1 Ruggedizer dimension adjustment with regard to processor height tolerance

Description : The dimensions of the ruggedizer under processor have been adjusted to be fully compatible with the weak tolerance min/max of processor height.

Impact: None. Improve the industrial process.

Workaround: Fixed by E.C. Level xxxxxC1 or E.C. Level xxxxxC2.

Item #RA-2 PCB bow close to rear connector

Description : Because of a dimension error on a RA ruggedizer, a PCB bow is noted after the mounting of the ruggedizer to compensate the miss of matter on P1/P2 support area.

Impact: PCB bow on rear of the board.

Workaround: Fixed by E.C. Level xxxxxC1 by adding a ring or E.C. Level xxxxxC2 by drawing modification.

Item #RA-3 Mechanical tolerance and gap isolation adjustment

Description : Margins have been added to avoid having some components too close to the ruggedizer.

Impact: None. Improve the industrial process.

Workaround: Fixed by E.C. Level xxxxxC1 or E.C. Level xxxxxC2

Item #RA-4 No conductive area to Earth on the ruggedizer

Description : A conductive area is required to ruggedizer treated with black (nonconductive treatment). This conductive area located to board handle is used to connect the ruggedizer to the earth. On VM6050RA V01 ruggedizer, this area has not been spared and it has been treated with black anodization..

Impact: None. Earth is connected to the ruggedizer with front panel mounting screw.

Workaround: Fixed by E.C. Level xxxxxC2.
On E.C. Level xxxxxC1 check if the ruggedizer is connected to earth.

Item #RA-5 Mechanical tolerance adjustment on plot (integrated ring spacer) of ruggedizer

Description : Margins have been added on specific plot to avoid having some components too close to the ruggedizer.

Impact: None. Improve the industrial process.

Workaround: Fixed by E.C. Level xxxxxC3.

4.8 Items Detailed Description - RC Mechanical E.C. Levels

NOTICE

Each item applies only to a specific group of E.C. levels.
Refer to the table available in section 4.3 "Revision Guide" page 8 to find the specific E.C. levels associated to a specific item.

Item #RC-1 Ruggedizer dimension adjustment with regard to processor height tolerance

Description : The dimensions of the ruggedizer under processor have been adjusted to be fully compatible with the weak tolerance min/max of processor height.

Impact: None. Improve the industrial process.

Workaround: Fixed by E.C. Level xxxxxD1.

Item #RC-2 Flash mezzanine device disconnection and error during high Z axis vibration (option including USB or SATA mezzanine module)

Description : During high Z axis vibration errors and disconnection have been noted on USB mezzanine flash device of VM6050/RC board.

Impact: USB flash disconnection and data corruption may occur on the device.

Workaround: Workaround consist of having two points of glue between ruggedizer and flash mezzanine to maintain the module in its socket.
Fixed by E.C. Level xxxxxD1

Item #RC-3 Mechanical tolerance and gap isolation adjustment

Description : Margins have been added to avoid having some components too close to the ruggedizer.

Impact: None. Improve the industrial process.

Workaround: Fixed by E.C. Level xxxxxD2

5 / Revision Guide for MOD-GX

5.1 How to Use the Board Revision Guide Table

1. Find the E.C. Level associated to your board as described in the Chapter 2 "Board Identification" page 2.
2. Find the column associated to the E.C. Level of your board in this table.
3. Check for a specific item in the table lines:
   - 3.1. A x (cross) in the E.C. Level column indicates that this item applies to this E.C. Level.
   - 3.2. No x (cross) in the E.C. Level column indicates that this item does not apply to this E.C. Level.
   - 3.3. If the functionality described by the item is not available on your board don't take into account this item. To know the functionalities available or not on your board, read the User's Guide associated with your board version.

NOTICE

Each item is fully described in section 5.3 "Item Detailed Description" page 20.

5.2 Revision Guide Table

Item	CRP	DESCRIPTION	E.C. LEVEL				
			10000	10001	20000		
1	4013	DisplayPort not fully operating	X				
2	4014	DVI/HDMI display not detected when plugged on DisplayPort connector	X	X			

5.3 Items Detailed Description

NOTICE

Each item applies only to a specific group of E.C. levels.
Refer to the table available in section 5.2 “Revision Guide” page 19 to find the specific E.C. levels associated to a specific item.

Item #1 DisplayPort not fully Operating - CRP 4013

Description : Auxiliary signal of DisplayPort graphic interface are not operating on MOD-GX for both DisplayPort. Consequently, no image appears on screen when using a DisplayPort cable with a DisplayPort screen.
On the other hand, image is available under Linux in poor resolution when using a mDP/VGA adaptator.

Impact: No BIOS prompt available on both DisplayPort.

Workaround: Fixed by E.C. Level 10001 of MOD-GX

Item #2 DVI/HDMI display not detected when plugged on DisplayPort connector - CRP 4014

Description : No DVI or HDMI graphic interfaces are available on both DisplayPort connectors in front of MOD-GX-SA.
Cable detect signal used to detect HDMI cable with regard to DisplayPort cable drives a 1.8V high level instead of 3.3V. This level is not sufficient to switch the repeater device in HDMI/DVI configuration.
HDMI/DVI interface could be available on MOD-GX-RC because of different design for routing signal in rear.

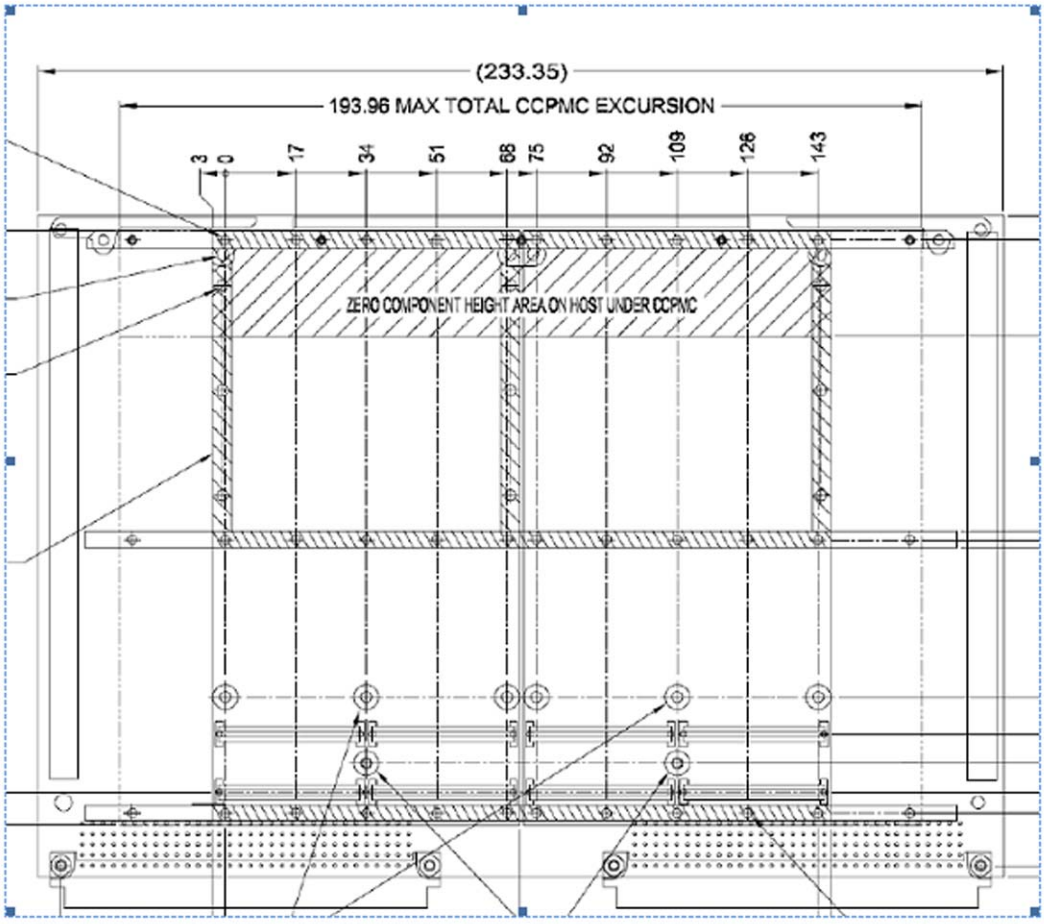
Impact: DVI/HDMI display cannot be used on VM6050 using MOD-GX PCB A.

Workaround: No Fix available on PCB A.

Fixed on PCB B in E.C. Level 20000

Appendix A - PMC Excursion

PMC Excursion



About Kontron

Kontron, a global leader in embedded computing technology and trusted advisor in IoT, works closely with its customers, allowing them to focus on their core competencies by offering a complete and integrated portfolio of hardware, software and services designed to help them make the most of their applications.

With a significant percentage of employees in research and development, Kontron creates many of the standards that drive the world's embedded computing platforms; bringing to life numerous technologies and applications that touch millions of lives. The result is an accelerated time-to-market, reduced total-cost-of-ownership, product longevity and the best possible overall application with leading-edge, highest reliability embedded technology

Kontron is a listed company. Its shares are traded in the Prime Standard segment of the Frankfurt Stock Exchange and on other exchanges under the symbol "KBC".
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