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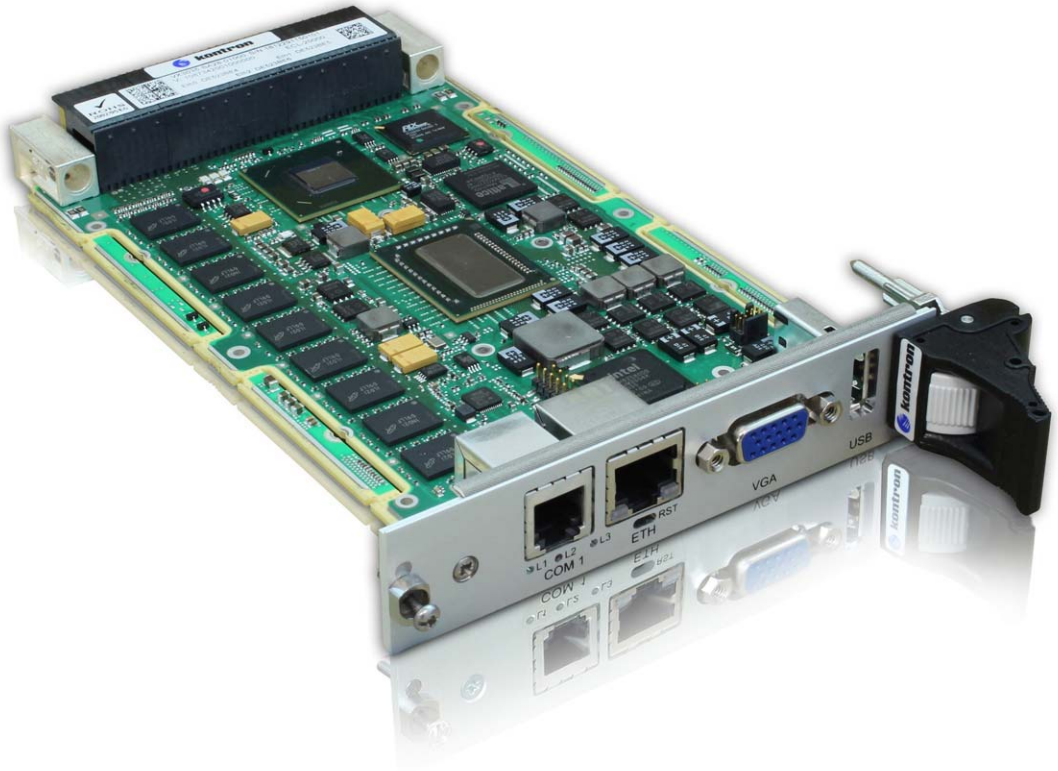
» VX3035 «



Hardware Release Notes

CA.DT.A96-6e - April 2015

Revision History

Publication Title:	VX3035 Hardware Release Notes	
Doc. ID:	CA.DT.A96-6e	
Rev.	Brief Description of Changes	Date of Issue
6e	Mechanical E.C. Level xxxxxA8 added	04-2015
5e	Sections “Revision Guide Table” and “Item Detailed Description” updated.	07-2014
4e	Functionnal E.C. Levels 30001, 30002 and 30004 added. Items 19 and 20 added. Mechanical E.C. Level A7 and item M7 added	06-2014
3e	Mechanical E.C. Levels A5 and A6 added.	01-2014
2e	Functional E.C. Levels 20005, 20007 and 30000 added. Mechanical E.C. Level A4 added.	09-2013
1e	Functional E.C. Levels 20000, 20002, 20004, 20006 added Mechanical E.C. Levels xxxxxA0, xxxxxA1, xxxxxA2, xxxxxA3 added.	05-2013
0e	Initial Version	06-2012

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Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Environmental protection is a high priority with Kontron.

Kontron follows the DEEE/WEEE directive.

You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- reduce waste arising from electrical and electronic equipment (EEE)
- make producers of EEE responsible for the environmental impact of their products, especially when they become waste
- encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- improve the environmental performance of all those involved during the lifecycle of EEE

Conventions

This guide uses several types of notice: Note, Caution, ESD.

Note: this notice calls attention to important features or instructions.


Caution: this notice alert you to system damage, loss of data, or risk of personal injury.


ESD: This banner indicates an Electrostatic Sensitive Device.

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix `0x' shows a hexadecimal number, following the `C' programming language convention.

The multipliers `k', `M' and `G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when `K', `M' and `G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

When describing transfer rates, `k' `M' and `G' mean $*10^3$, $*10^6$ and $*10^9$ *not $*2^{10}$ $*2^{20}$ and $*2^{30}$.*

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and CompactPCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Signal names ending with an asterisk (*) or a hash (#) denote active low signals; all other signals are active high.

Signal names follow the PICMG 2.0 R3.0 CompactPCI Specification and the PCI Local Bus 2.3 Specification.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions


Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.


Caution, Electric Shock!
Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction.

Table Of Contents

Chapter 1 - Introduction

This document describes the engineering evolution of the referenced products to the up-to-date ones which are detailed in the Kontron hardware documentation.

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

You will find in the following pages:

This document applies to all VX3035 Environment Classes (if available): Standard and Rugged Conduction-Cooled versions.

If a specific information applies only to a specific environment class, it is clearly specified in the information description. For example, the reference VX3035/RC applies only to VX3035 Rugged Conduction-Cooled environment class.

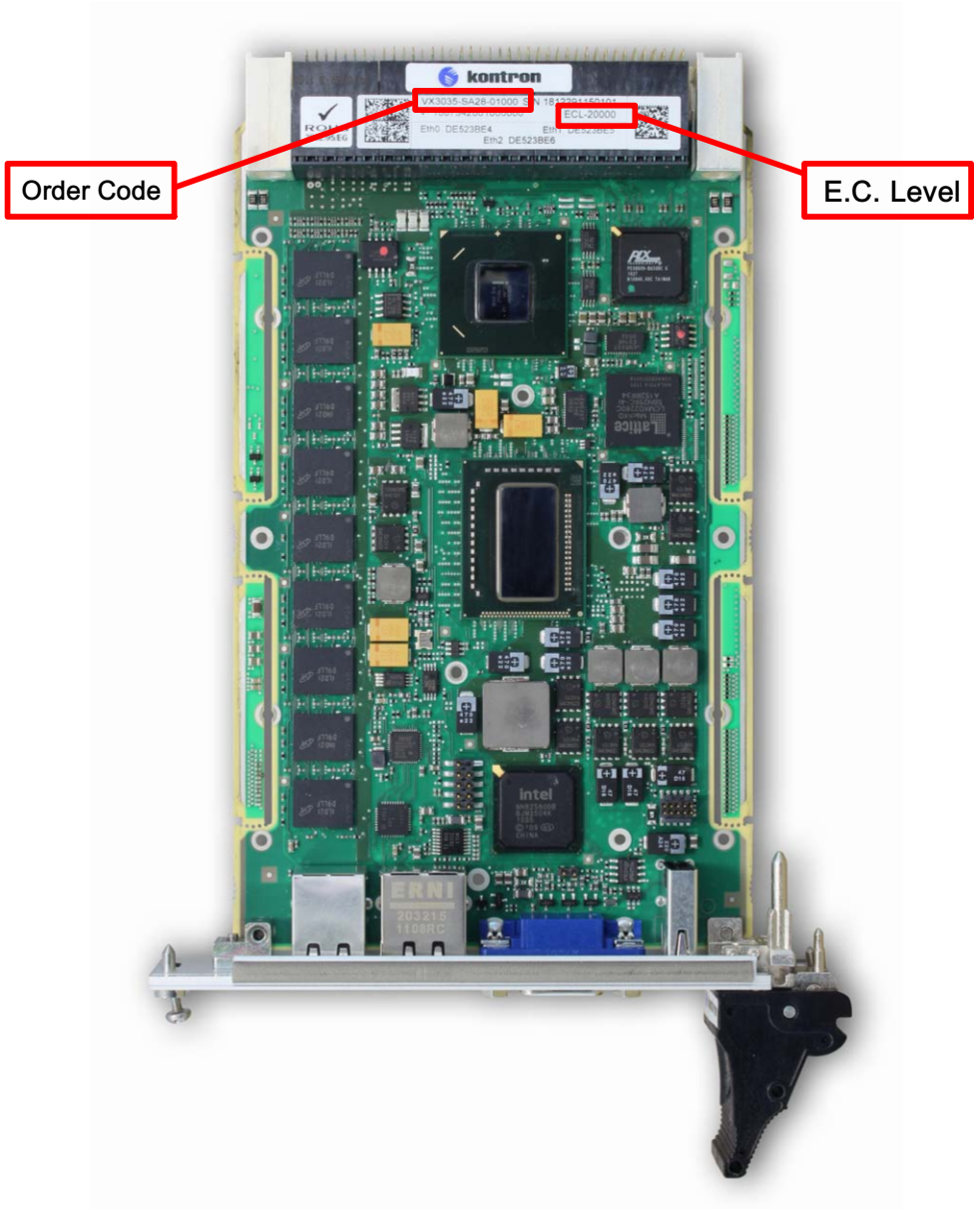
This document refers to the up-to-date release of the following hardware documentation:

> VX3035 User's Guide CA.DT.A95

Chapter 2 - Board Identification

Engineering Change Level and Order Code

The Engineering Change Level (E.C. Level) and Order Code information are available on the “Board Identification" label, located on the top side of the board.



Chapter 3 - General Information

Personal Injuries

> VX3035/SA

- Do not touch the CPUs heatsink while removing the board from a rack because it can get very hot.
- Be careful while handling the board, because of the cutting edges of the heatsink.
- Do not place the board on any surface or in any form of storage container until the board and its heatsink have cooled down to room temperature.

EMC Gasket

In order to protect the EMC gasket located in the front panel, be careful during the insertion of the boards in the rack. It is recommended to insert the boards in a rack starting from the higher slot number and extract them starting from the lowest slot number.

Power Supplies

On +5V and +12V power supplies, monotonic rise time no longer than 25 ms is required at Power on.

For a power off condition to be valid, the +5V and +12V power supply inputs should remain at 0V for at least one second.

VX3035/SA Handling

Do not lie the board on the CPUs heatsink to avoid damages on the processor.

Chapter 4 - Board Revision Guide

4.1 How to Use the Board Revision Guide Table

1. Find the E.C. Level associated to your board as described in the Chapter 2 “Board Identification" page 2.
2. Find the column associated to the E.C. Level of your board in this table.
3. Check for a specific item in the table lines:
   - 3.1. A x (cross) in the E.C. Level column indicates that this item applies to this E.C. Level.
   - 3.2. No x (cross) in the E.C. Level column indicates that this item does not apply to this E.C. Level.
   - 3.3. If the functionality described by the item is not available on your board don't take into account this item. To know the functionalities available or not on your board, read the User's Guide associated with your board version.

Each item is fully described in section 4.4 “Item Detailed Description" page 8.

4.2 Revision Guide Table - Functional E.C. Levels

E.C. Levels < 20000

Item	CRP	Description	E.C. Level					
			10000	10001	10002	10003	10004	10005
1	3899 3900	Speed limitation for high speed IOs (SATA, DP) when using Rear Transition Module	No impacted E.C. Level					
2	3918	SPI rescue flash not always protected	No impacted E.C. Level					
3	3901	Alignment key oxidation	No impacted E.C. Level					
4	4031	Insufficient noise immunity of onboard +3.3V	X	X				
5	4032	Operating ambient temperature limited to 35°C (applicable only on SA class)	X	X	X	X		

E.C. Levels ≥ 20000 and < 30000

Item	CRP	Description	E.C. Level					
			20000	20002	20004	20005	20006	20007
1	3899 3900	Speed limitation for high speed IOs (SATA, DP) when using Rear Transition Module	Not impacted E.C. Level					
2	3918	SPI rescue flash not always protected	Not impacted E.C. Level					
3	3901	Alignment key oxidation	Not impacted E.C. Level					
4	4031	Insufficient noise immunity of onboard +3.3V	Not Applicable					
5	4032	Operating ambient temperature limited to 35°C (applicable only on SA class)	Not Applicable					
6	4103	Insufficient noise immunity of onboard +3.3V	X					
7	4108	XDP debug interface not functional	X					
8	4110	USB power-distribution switches limitation to 500 mA maximum output continuous current	X					
9	4118	CPLD power sequencer not fully compliant with Intel specifications	X	X				
10	4112	CPLD SYSRESET generation not fully optimized	X	X				
11	4111	CPLD miscellaneous minor corrections	X	X				
12	4114	Bad EEPROM binary file for PEX8609 PCIe Switch	X	X	X	X		
13	4115	CPLD interruptions management for temperature alerts not very convenient	X	X	X	X		
14	4116	Unexpected SYSRESET behavior	X	X	X	X		
15	4121	Display ports hot plug does not work under BIOS	X	X	X	X	X	X
16	4122	Bad NVM binary file for 1000BaseT i82579 PHY INTEL chip	X	X	X	X	X	X
17	4120	Permanent black screens when the 3 graphics ports are simultaneously used	X	X	X	X	X	X
18	4127	Ethernet LED signals not properly routed to P2701 connector	X	X	X		X	
19	4199	Board hangs with infinite reset loop with special conditions about hyperthreading, core selection and VPX reset	X	X			X	X
20	-	Possible spurious pulse on internal power supplies during power on/off in system without VPX supply P3V3_AUX	X	X	X	X	X	X

E.C. Levels ≥ 30000

E.C. Level 30000 is functionnaly equivalent to E.C. Level 20005, but also suppresses the need of the rework wires used in E.C. Levels 2xxxx.

Item	CRP	Description	E.C. Level			
			30000	30001	30002	30004
1	3899 3900	Speed limitation for high speed IOs (SATA, DP) when using Rear Transition Module	Not impacted E.C. Level			
2	3918	SPI rescue flash not always protected	Not impacted E.C. Level			
3	3901	Alignment key oxidation	Not impacted E.C. Level			
4	4031	Insufficient noise immunity of onboard +3.3V	Not impacted E.C. Level			
5	4032	Operating ambient temperature limited to 35°C (applicable only on SA class)	Not impacted E.C. Level			
6	4103	Insufficient noise immunity of onboard +3.3V	Not impacted E.C. Level			
7	4108	XDP debug interface not functional	Not impacted E.C. Level			
8	4110	USB power-distribution switches limitation to 500 mA maximum output continuous current	Not impacted E.C. Level			
9	4118	CPLD power sequencer not fully compliant with Intel specifications	Not impacted E.C. Level			
10	4112	CPLD SYSRESET generation not fully optimized	Not impacted E.C. Level			
11	4111	CPLD miscellaneous minor corrections	Not impacted E.C. Level			
12	4114	Bad EEPROM binary file for PEX8609 PCIe Switch	X			
13	4115	CPLD interruptions management for temperature alerts not very convenient	X	X		
14	4116	Unexpected SYSRESET behavior	X	X		
15	4121	Display ports hot plug does not work under BIOS	X	X	X	X
16	4122 4087	Bad NVM binary file for 1000BaseT i82579 PHY INTEL chip	X			
17	4120	Permanent black screens when the 3 graphics ports are simultaneously used	X	X	X	X
18	4127	Ethernet LED signals not properly routed to P2701 connector	Not impacted E.C. Level			
19	4199	Board hangs with infinite reset loop with special conditions about hyperthreading, core selection and VPX reset	Not impacted E.C. Level			
20	-	Possible spurious pulse on internal power supplies during power on/off in system without VPX supply P3V3_AUX	X		X	

4.3 Revision Guide Table - Mechanical E.C. Levels

Item	CRP	Description	E.C. Levels								
			xxxxxA0	xxxxxA1	xxxxxA2	xxxxxA3	xxxxxA4	xxxxxA5	xxxxxA6	xxxxxA7	xxxxxA8
M1	4124	CPU heatsink attachment results in an important board bow	X								
M2	4117	No mechanical data available for the thermal adhesive for PCH heatsink attachment	X	X							
M3	4125	CPU heatsink not fully optimized	X	X	X						
M4	4123	Slight fretting corrosion could appear on SATA or USB flash mezzanine connector and battery mezzanine connector	X	X	X	X					
M5	4195	EMC leaks around front panel USB port	X	X	X	X	X				
M6	-	Front panel silkscreen font not set to ARIAL	X	X	X	X	X	X			
M7	4230	Insufficient quality of VGA cable attachment	X	X	X	X	X	X	X		
M8	4258	Improvement of Immunity against Electrostatic Discharges	X	X	X	X	X	X	X	X	

E.C. Levels xxxxxA3 and xxxxxA4 are equivalent.
E.C. Level xxxxxA4 is a manufacturing improvement of E.C. Level xxxxxA3

4.4 Item Detailed Description - Functional E.C. Levels

Each item applies only to a specific group of E.C. Levels.
Refer to the table available in section 4.2 “Revision Guide - Functional E.C. Levels” page 4 to find the specific E.C. Levels associated to a specific item.

Item # 1 Speed limitation for high speed IOs (SATA, DP) when using PB-VX3 Rear Transition Module - CRP 3899-3900

Description: Some SATA II 3 G/s devices are not detected by BIOS using PB-VX3 Rear Transition Module. The use of PIM additional module on PB-VX3 to connect graphic monitor on eDP is not optimized in terms of signal integrity. Black screen (loose of synchronization) may occur on eDP monitor especially if the ambient temperature is high (ie +55°C).

Impact: SATA II 3Gb/s link not recommended with PB-VX3. 1920x1080 eDP resolution not recommended with PB-VX3 and PIM additional module.

Solution: Fixed by use of PB-VX3-400 and PIM-VX3-410-1 modules.
No impacted E.C. Level.

Item # 2 SPI rescue flash not always protected - CRP 3918

Description: SPI rescue flash write protection not fully effective if SW1[3] is ON or NVMRO ON.

Impact: SPI rescue not always protected for writes cycles.

Solution: Fixed by BIOS ID12104.
No impacted E.C. Level.

Item # 3 Alignment key oxidation - CRP 3901

Description: Oxidation on VPX alignment key may appear after several weeks.

Impact: Bad earth connection.

Solution: Never occurs on VX3035 boards. Invalid erratum.
No impacted EC Level.

Item # 4 Insufficient noise immunity of onboard +3.3V - CRP 4031

Description: Noise was observed around onboard 3.3V generation component. This chip may not start correctly.

Impact: Some boards may not start.

Solution: Fixed in E.C. Level 10002.

Item # 5 Operating ambient temperature limited to 35°C - CRP 4032 (applicable only on SA class)

Description: The PCH does not have any cooling device attached. Setting the operating temperature above 35°C could lead the PCH to work over its max junction temperature (unless the specified airflow is increased).

Impact: No board dysfunctions observed at 55°C/ 20 cfm but working above Tj max could affect the PCH lifetime duration.

Solution: Fixed in E.C. Level 10004.

Item # 6 Insufficient noise immunity of onboard +3.3V - CRP 4103

Description: Noise was observed around onboard 3V3 generation component. This chip may not start correctly.

Impact: Some boards may not start.

Solution: Fixed in E.C. Level 20002.

Item # 7 XDP debug interface not functional - CRP 4108

Description: XDP port for CPU extended debug port connection does not work.

Impact: XDP debug interface not functional.

Solution: Fixed in E.C. Level 20002.

Item # 8 USB power distribution switches limitation to 500 mA maximum output continuous current - CRP 4110

Description: USB power over-current risk (see below the specific conditions) because not enough margin on the onboard USB power-distribution switches. They can only provide 500 mA maximum output continuous current.

Impact: No known functional impact.

Specifics conditions could cause USB power overcurrent:

- All USB 2.0 devices are high power: they can potentially and simultaneously require 500 mA each (100 mA each for low power devices).
- Customers specifics applications can require more than 500 mA on some USB 2.0 ports.

Solution: New power-distribution switches implemented. They can provide up to 1A maximum output continuous current.

Fixed in E.C. Level 20002.

Item # 9 CPLD power sequencer not fully compliant with Intel specifications - CRP 4118

Description: Some timings / delays in CPLD power sequencer are not fully compliant with Intel specifications.

Impact: No known functional impact.

Solution: Program the CPLD V7 version.

Fixed in E.C. Level 20004.

Item # 10 CPLD SYSRESET generation not fully optimized - CRP 4112

Description: Some VX3035 use cases could cause inopportune SYSRESET generation by the CPLD. It could disturb the components initialization and prevent the board starting or freeze the board.

Impact: No known functional impact.

Solution: Program the CPLD V7 version.

Fixed in E.C. Level 20004.

Item # 11 CPLD miscellaneous minor corrections - CRP 4111

Description: - CPLD led status read error issues in user mode.

- Potential issues on CPLD I2C master and auto-load because of a potential timing issue.

- CPLD potential interruptions management issues due to Fedora GPIO driver.

Impact: Known functional impact:

CPLD led status read error issues in user mode.

Solution: Program the CPLD V7 version.

Fixed in E.C. Level 20004.

Item # 12 Bad EEPROM binary file for PEX8609 PCIe switch - CRP 4114

Description: Bad programmation of the PEX8609 PCIe switch EEPROM (bad binary file).

Impact: No known functional impact during PCIe Gen2 operation (Linux stress tests in temperature between two VX3035 boards via VPX backplane). And during power-cycles (power ON /OFF) and Linux boot/reboot cycles. The PEX8609 PCIe switch is always properly detected.

Solution: Program the PEX8609 PCIe Switch EEPROM with the correct official binary file by “kvpx” EFI shell command: VX3030_VX6060_VX3035_eeprom_backplane_ PEX8609_Mod eNT.bin

Fixed in E.C. Level 20006.

Item # 13 CPLD interrruptions management for temperature alerts not very convenient - CRP 4115

Description: The alert issued by onboard thermal sensors LM73 and NUVOTON are signaled by interruptions but their deactivation is not properly handled in cPLD revision V7: either the interrupt must be masked or the status must be polled until the alert disappears.

Impact: No known critical impact.

Solution: Mask the thermal interrupt or wait for the end of the alert by polling.
Fixed in cPLD revision V8 (E.C. Level 20006)

CPLD V8 Default mode:

- No workaround = CPLD V7 interruption management mode (backward compatible mode).

CPLD V8 Enhanced mode:

- Interruptions acknowledgement on temperature alerts added.
- Interruptions generation when temperature alert appears or alert disappears.

Item # 14 Unexpected SYSRESET behavior - CRP 4116

a. Early reboot after local reset.

Description: When a VX3035 with SYSRESET enabled both from and to PCIe backplane is reset by Linux "reboot" command or EFI shell "reset" command, it will start rebooting 300 to 600 ms before the end of SYSRESET activation.

Impact: In PCIe systems with a VX3035 as system controller, the VX3035 may probe the backplane PCIe bus before PCIe agents are ready to respond, and the probe result will not be correct.

Solution: Delay PCIe probing after reset. Fixed in cPLD revision V8 (E.C. Level 20006).

b. Early reboot after external SYSRESET.

Description: A VX3035 which has its local reset asserted (signal PLTRST# asserted) during normal operation (ie not immediately after poweron), will ignore a SYSRESET activated by the backplane and could therefore restart before the SYSRESET de-activation.

Impact: Except at powerup where the VX3035 will behave normally, the VX3035 could start unexpectedly before a SYSRESET deactivation on VPX bus.

Solution: Ensure that all PCIe agents drive SYSRESET only at powerup or ensure that an early start of the VX3035 (ie before SYSRESET deassertion) has no impact on the system. Fixed in cPLD revision V8 (E.C. Level 20006).

c. SYSRESET asserted during halt.

Description: When a VX3035 is halted by Linux "halt" or "shutdown" command (signal PLTRST# is activated), the signal VPX SYSRESET is unexpectedly asserted.

Impact: Halting a VX3035 in a system will reset other PCIe agents if their SYSRESET input is enabled.

Solution: Disable SYSRESET output in VX3035 (through cPLD register 0x70) before issuing a halt. Fixed in cPLD revision V8 (E.C. Level 20006).

d. SYSRESET duration.

Description: The duration of SYSRESET varies from 300 ms to 600 ms (nominal).

Impact: No known impact but should be taken into account when synchronising several boards in a system.

Solution: Fixed in cPLD revision V8 (E.C. Level 20006)

Item # 15 DisplayPorts hot plug does not work under BIOS - CRP 4121

Description: Limitation: the DisplayPorts hot plug does not work under BIOS.

Nevertheless:

- DisplayPort hot plug is functional under OS Linux Fedora 14.
- DisplayPorts are full functional under BIOS and OS Fedora 14 on the whole SA temperature range.

Impact: DisplayPorts hot plug does not work under BIOS.

Solution: Do not hot plug under BIOS the DisplayPort cable(s).
Plug the DisplayPort cable(s) before the board starting (chassis power ON).
Under investigation.

Item # 16 Bad NVM binary file for 1000BASE-T i82579 PHY INTEL chip- CRP 4122-4087

Description: Because of bad NVM binary file for 1000BASE-T PHY i82579 INTEL chip, signal integrity slight violations can appear during IEEE802.3 compliance tests on 1000BASE-T front panel PHY i82579 link.

Impact: No known functional impact. 1000BASE-T front panel Ethernet of VX3035 board is fully functional on the whole SA and RC temperature ranges.

Solution: NVM for i82579 PHY is included in the BIOS.
Fixed with BIOS ID13127.

Item # 17 Permanent black screen when the 3 graphics ports are simultaneoulsy used - CRP 4120

Description: Limitation: When the VGA port (on the VX3035 front panel) and the two DisplayPorts (on the rear panel) are simultaneously connected to their graphics screens, they do not switch on. Nothing appears on the screens.

Impact: Permanent black screens when the 3 graphics ports are simultaneously used.

Solution: Do not simultaneously connect the 3 graphics ports.
Only two graphics ports can be simultaneously used (one DisplayPort and VGA port or the two DisplayPort).
Under investigation.

Item # 18 Ethernet LED signals not properly routed to P2701 connector - CRP 4127

Description: The VX3035 board features four extra Ethernet links on connector P2701, allowing the use of DB-ETH mezzanines. The "link" and "activity" LEDs of port ETH1 on P2701 are not properly routed.

Impact: No "activity" or "link" LEDs on Ethernet port ETH1 on P2701.

Solution: Fixed in E.C. Levels 20005 and 20007 with rework wires.
Fully fixed in E.C. Level 30000.

Item # 19 Board hangs with infinite reset loop with special conditions about hyperthreading, core selection and VPX reset - CRP 4199

Description: An infinite reset loop at BIOS startup, with LED1 blinking continuously red/green/off will occur when the following conditions are met:

- Boards with PLD versions V4, V5, V6 (any BIOS ID) or V8 (BIOS ID earlier than ID12347),
- One of the core has been disabled or hyperthreading has been disabled in BIOS setup,
- Board configured to enable both "VPX Reset Output" and "VPX SYSRESET Input" in BIOS setup.

This issue does not occur with PLD version V7.

Impact: Board does not start.

Solution: Fixed by PLD V7 (all BIOS IDs) and PLD V8 (BIOS ID12347 minimum).

Two workarounds are possible:

1. Disable either SYSRESET input or RESETs output.
2. Have all cores active and hyperthreading enabled.

To recover from infinite loop, boot on rescue BIOS, restore main BIOS from rescue (`kflash -c`), boot from main BIOS and update main BIOS to the expected version.

Item # 20 Possible spurious pulse on internal power supplies during power on/off in system without VPX supply P3V3_AUX

Description: At power-on or power-off, on VX3035 boards plugged in chassis without VPX rail P3V3_AUX, a spurious pulse may be generated on the P3V3 internal power supply (and also theroretically on other internal supplies). This spurious pulse has no impact on the behavior of board because it occurs 200 ms before the normal power sequence or during the power-off of the board and its duration is very short (~2ms). Should some other internal supplies show the same pulse at power-on, they could violate the power-on sequence of some multi-voltage components but the short duration of the pulse (a few milliseconds) is not deemed sufficient to impact significantly the MTBF of the board.

Nevertheless, a correction is recommended for new productions.

Impact: No functionnal impact. A possible impact on MTBF is theoretically possible but the conditions for this to occur have never shown up.

Solution: Fixed in E.C. Levels 30001 and 30004.

4.5 Item Detailed Description - Mechanical E.C. Levels

Each item applies only to a specific group of Mechanical E.C. Levels.
Refer to the table available in section 4.3 “Revision Guide - Mechanical E.C. Levels” page 7 to find the specific Mechanical E.C. Levels associated to a specific item.

Item #M1 CPU heatsink attachment results in an important board bow - CRP 4124

Description: On VX3035 PCB B, the four holes of the board's edges are used for the CPU heatsink attachment (RAD-VX3035- 3-V01). It results in an important board bow which generates stress on soldered components. Then, it could damage the board.

Impact: The board bow generates stress on soldered components. It could damage the board.

Solution: Mount the RAD-VX3035-3-V02 CPU heatsink which uses the three holes near the CPU (VX3035 PCB A like). It results in a significative board bow reduction. The board bow is now acceptable.

Fixed in Mechanical E.C. Level xxxxxA1.

Item #M2 No mechanical data is available for the thermal adhesive for PCH heatsink attachment - CRP 4117

Description: No thermal cycling data for the thermal adhesive for the PCH heatsink attachment. Thermal cycling data of the thermal adhesive reflects its mechanical behavior. It is an important parameter for a good PCH heatsink attachment.

Impact: Important risk: PCH heatsink could take off itself.

Solution: Use a new thermal adhesive for PCH heatsink attachment. See the mechanical IECP_VX3035_A2 for mechanical and thermal cycling data of the new thermal adhesive.

Fixed in Mechanical E.C. Level xxxxxA2.

Item #M3 CPU heatsink not fully optimized - CRP 4125

Description: The RAD-VX3035-3-V02 CPU heatsink is not fully optimized:

- CPU heatsink too high for 1 inch version.
- Springs strength not optimized.
- Safe air gap too low between components and the bottom face of the heatsink.

Impact: 1 inch slot heatsink incompatibility. No other known functional impact.

Solution: Mount the RAD-VX3035-3-V05 CPU heatsink:

- Heatsink height arranged for 0.8 and 1 inch compatibility.
- Springs strength optimized.
- Safe air gap increased between components and the heatsink bottom.

Fixed in Mechanical E.C. Level xxxxxA3.

Item #M4 Slight fretting corrosion could appear on SATA or USB flash mezzanine connector and battery mezzanine connector - CRP 4123

Description: Slight fretting corrosion could appear on SATA/USB flash mezzanine connector and battery mezzanine connector. No known functional impact during and after VITA 47 standard SA class vibrations tests.

Impact: No known functional impact during and after VITA 47 standard SA class vibrations tests.

Solution: Fixed in E.C. Level A4.

Item #M5 EMC leaks around front panel USB port - CRP 4195

Description: The front panel is not properly sealed with respect to EMC constraints and EMC leaks could occur around the USB connector. A "D-shape" EMC seal (Laird Technologie P/N 4053-PA-51H-01800) should be added on the internal side of the front panel, opposite to the existing seal.

Impact: The front panel USB port shows a reduced immunity to EMC. For example ESD test EN61000-4-2 with levels EN50121-4 (+6kV) applied on USB connector fails.

Solution: Fixed in Mechanical E.C. Level A5.

Item #M6 Front panel silkscreen font not set to ARIAL

Description: The font used for front panel silkscreen markings differs from the one of other Kontron products and should have been set to ARIAL.

Impact: No functional impact.

Solution: Fixed in Mechanical E.C. Level A6.

Item #M7 Insufficient quality of VGA cable attachment – CRP4230

Description: The attachment of a VGA cable to the front of the board requires to glue an aluminum plate to the front panel. This additional assembly leads to poor ground continuity and reduces ESD immunity. In addition, the jackpost face is not flushed by +/-0.75mm with the face of the VGA connector, as required per IPC-A-620 rule 9.1.1 (1 mm instead of 0.75 mm max).

Impact: Risk of EMI/ESD test failure around the VGA connector. Non optimum contact quality of VGA cable.

Solution: Fixed in mechanical E.C. Level A7 (front panel modified).

Item #M8 Improvement of Immunity against Electrostatic Discharges (ESD) – CRP4258

Description: The front panel of VX3035-SA passed the tests for +/-4 kV ESD contact discharges but fails levels +/-6 kV.

Impact: VX3035-SA fails test with +/- 6 kV ESD contact discharges.

Solution: To enhance immunity to +/- 6 kV ESD contact discharges, an EMC seal needs to be added between front panel and connectors COM1 and ETH. The mechanical kits KITSA-VX3035-1 and KITSA-VX3035-4 are both upgraded to version V06.

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