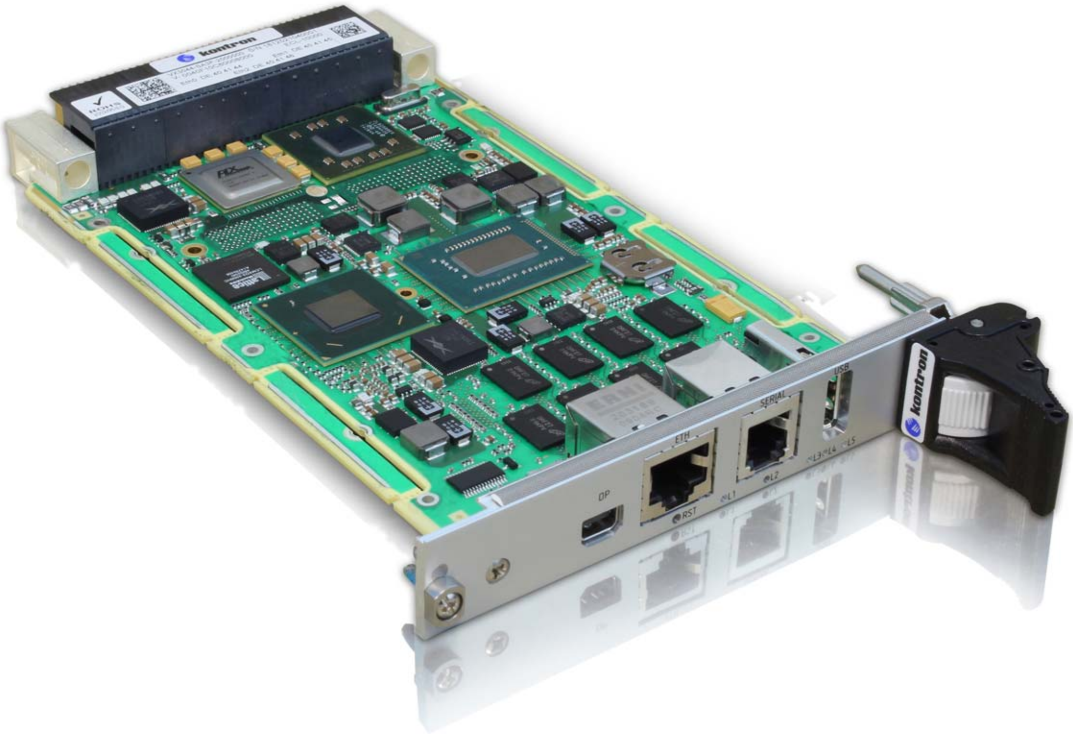
» VX304x «



Hardware Release Notes

CA.DT.A99-2e - December 2014

The pulse of innovation

Revision History

	Publication Title:	VX304x Hardware Release Notes
	Doc. ID:	CA.DT.A99-2e
Rev.	**Brief Description of Changes**	**Date of Issue**
2e	New functionnal E.C. Levels: 4x006 and 4x007. New mechanical E.C. Levels: xxxxxA6 (SA class), D1 (RC class with XMC), D2 (RC class without XMC). New section: 4.6 - REACh compliance	12-2014
1e	Functionnal E.C. Levels 2x002, 2x003, 2x004, 2x006, 3x003, 3x004, 3x005, 4x005, added. Mechanical E.C. Levels xxxxxA1, xxxxxA2, xxxxxA3, xxxxxA4, xxxxxA5 added	04-2014
0e	Initial Version	12-2012

Proprietary Note

This document contains information proprietary to Kontron. It may not be copied or transmitted by any means, disclosed to others, or stored in any retrieval system or media without the prior written consent of Kontron or one of its authorized agents.

The information contained in this document is, to the best of our knowledge, entirely correct. However, Kontron cannot accept liability for any inaccuracies or the consequences thereof, or for any liability arising from the use or application of any circuit, product, or example shown in this document.

Kontron reserves the right to change, modify, or improve this document or the product described herein, as seen fit by Kontron without further notice.

Trademarks

This document may include names, company logos and trademarks, which are registered trademarks and, therefore, proprietary to their respective owners.

Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Environmental protection is a high priority with Kontron.

Kontron follows the DEEE/WEEE directive.

You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- reduce waste arising from electrical and electronic equipment (EEE)
- make producers of EEE responsible for the environmental impact of their products, especially when they become waste
- encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- improve the environmental performance of all those involved during the lifecycle of EEE

Conventions

This guide uses several types of notice: Note, Caution, ESD.

Note: this notice calls attention to important features or instructions.

Caution: this notice alert you to system damage, loss of data, or risk of personal injury.

ESD: This banner indicates an Electrostatic Sensitive Device.

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix `0x' shows a hexadecimal number, following the `C' programming language convention.

The multipliers `k', `M' and `G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when `K', `M' and `G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

When describing transfer rates, `k' `M' and `G' mean $*10^3$, $*10^6$ and $*10^9$ *not* $*2^{10}$ $*2^{20}$ *and* $*2^{30}$.

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and CompactPCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Signal names ending with an asterisk (*) or a hash (#) denote active low signals; all other signals are active high.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.

Caution, Electric Shock!
Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction.

Table Of Contents

Chapter 1 - Introduction

This document describes the engineering evolution of the referenced products to the up-to-date ones which are detailed in the Kontron hardware documentation.

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

You will find in the following pages:

> How to identify the Engineering Change (E.C.) level and the Order Code of the board you have in hand: . . . . Chapter 2 page 2

> What is the important information related to the different revisions of the board and the VX304x User's Guide:
  - General information for VX304x boards . . . . Chapter 3 page 3
  - Information related to a specific E.C. level . . . . Chapter 4 page 6

In this document the term VX304x will be associated to the 3U VPX board family, including VX3042 dual core and VX3044 quad core module.

This document applies to all VX304x Environment Classes (if available): Standard and Rugged Conduction-Cooled versions.

If a specific information applies only to a specific environment class, it is clearly specified in the information description. For example, the reference VX304x/RC applies only to VX304x Rugged Conduction-Cooled environment class.

This document refers to the up-to-date release of the following hardware documentation:

> VX304x User's Guide CA.DT.A98

Please contact Kontron for further information regarding EFT (Early Field Test samples) E.C. Levels not shown in the following tables.

Chapter 2 - Board Identification

Engineering Change Level and Order Code

The Engineering Change Level (E.C. Level) and Order Code information are available on the “Board Identification" label, located on the top side of the board.

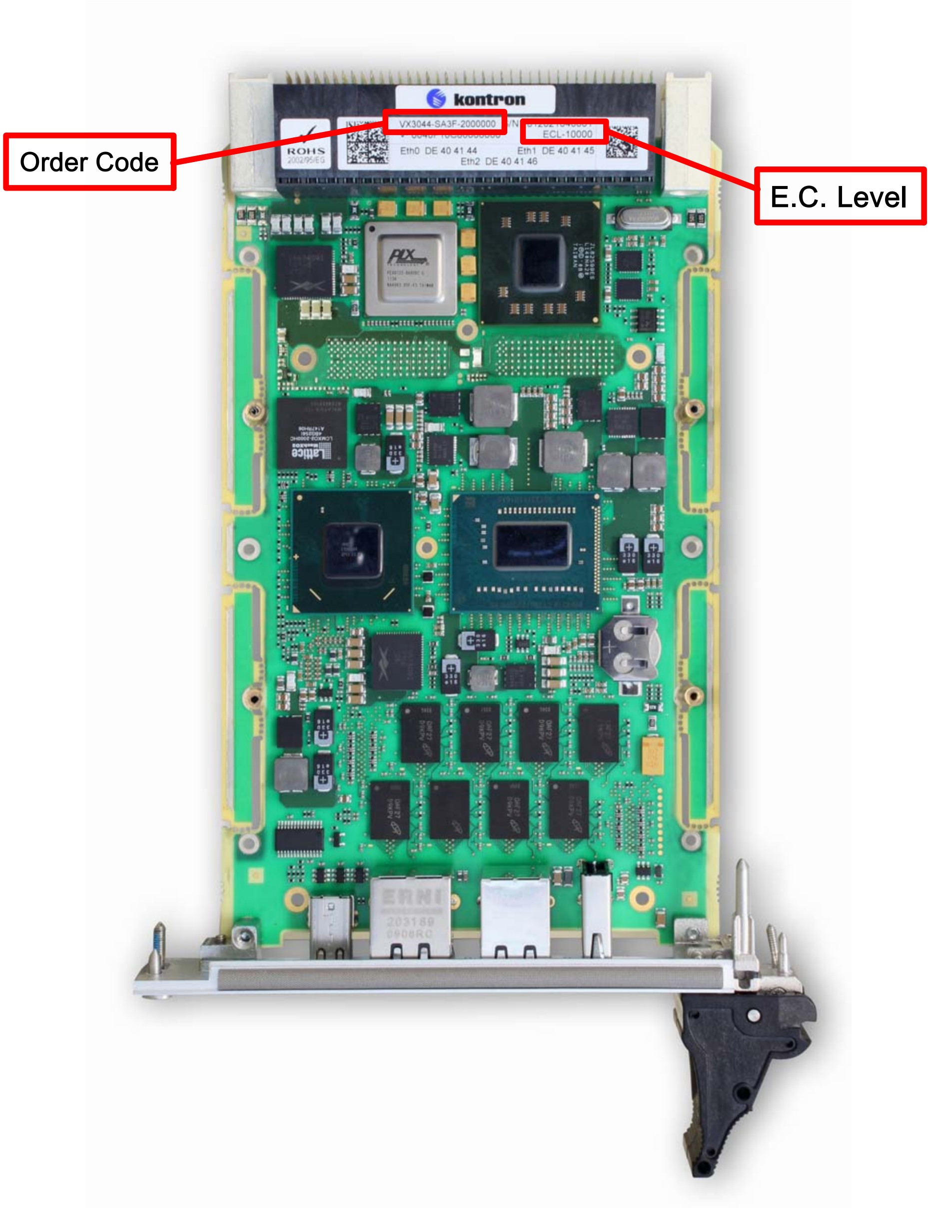


Figure 1: VX304x Identification

Chapter 3 - General Information

Personal Injuries

VX304x/SA

- Do not touch the CPUs heatsink while removing the board from a rack because it can get very hot.
- Be careful while handling the board, because of the cutting edges of the heatsink.
- Do not place the board on any surface or in any form of storage container until the board and its heatsink have cooled down to room temperature.

VX304x/RC

- Do not attempt to remove the board from chassis at high temperature (above 40°C) or at low temperature (below 10°C).
- Do not place the board on any surface or in any form of storage container until the board has cooled down to room temperature.

EMC Gasket

VX304x/SA

In order to protect the EMC gasket located in the front panel, be careful during the insertion of the boards in the rack. It is recommended to insert the boards in a rack starting from the higher slot number and extract them starting from the lowest slot number.

Power Supplies

On +5V and +12V power supplies, monotonic rise time shall comply with VS1/VS3 VPX standard rise time requirements.

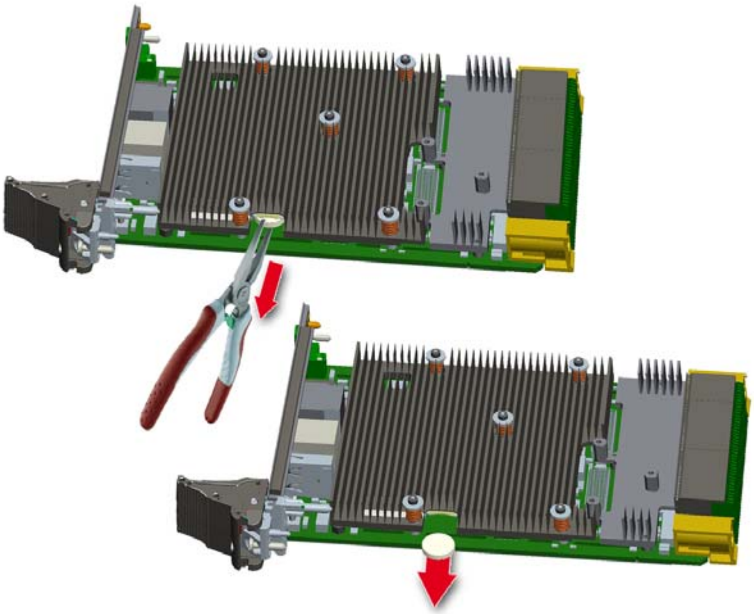
For a power off condition to be valid, the +5V and +12V power supply inputs should remain at 0V for at least one second.

VX304x/SA Handling

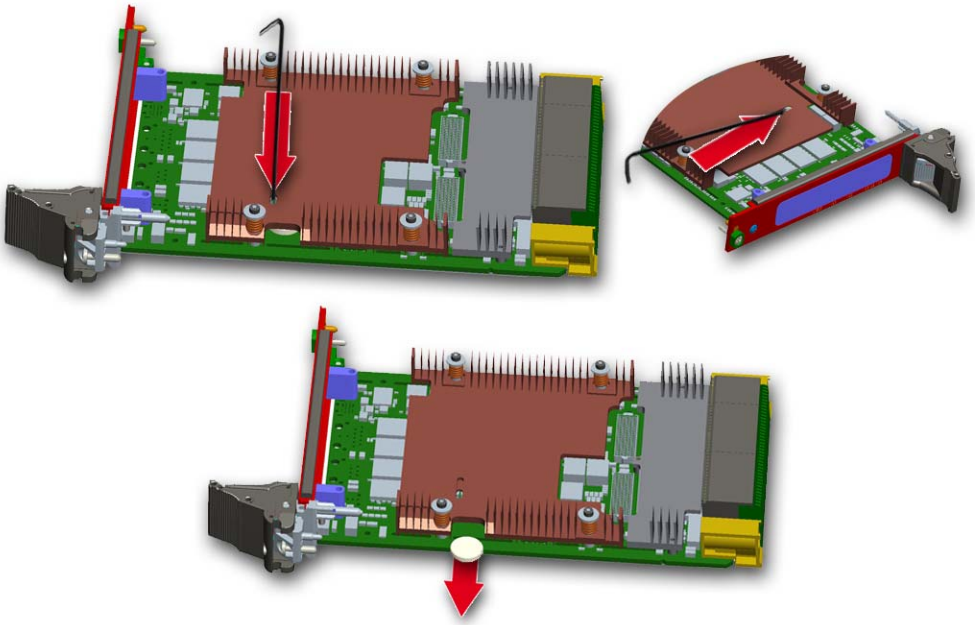
To avoid damaging the processor die, do not touch the heatsink while handling the board and do not lie the board upside down (on the heatsink).

Battery Replacement

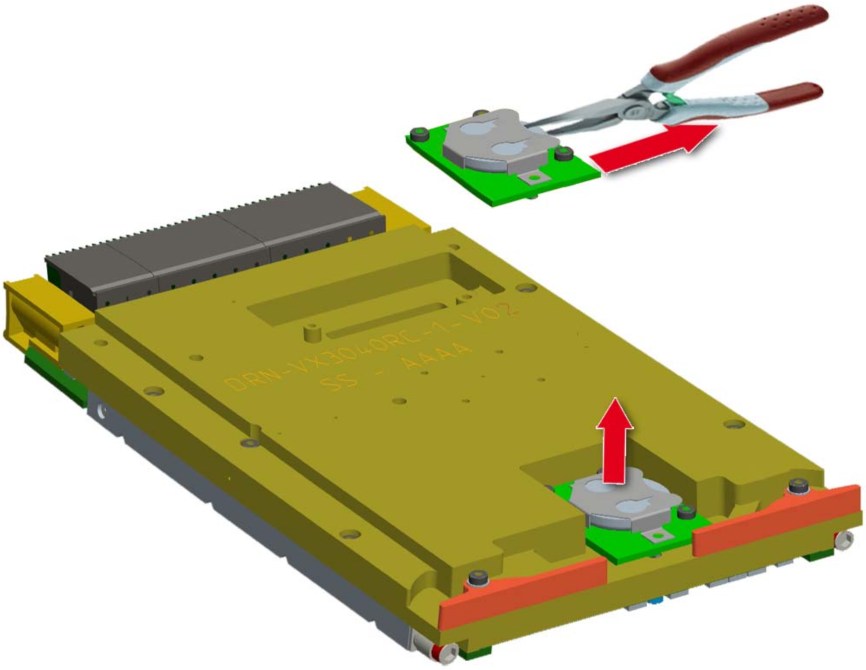
- Turn off the power.
- Get the battery outside of its holder:
  - on VX3040/SA boards with battery access on the side of the heatsink, by pulling it out with a small plier



  - on VX3040/SA boards with battery acces through an opening in the heatsink, by pushing it out with an Allen key 1.5 mm (Farnell 1779098 or equivalent) or 1/16.



- on VX3040/RC boards with a battery mezzanine, by removing the mezzanine from the VX3040 board and pulling out the battery with a plier.



> Place the new battery in the socket with the plus pole facing upwards.

Chapter 4 - Board Revision Guide

4.1 How to Use the Board Revision Guide Table

1. Find the E.C. Level associated to your board as described in the Chapter 2 “Board Identification" page 2.
2. Find the column associated to the E.C. Level of your board in this table.
3. Check for a specific item in the table lines:
    3.1. A x (cross) in the E.C. Level column indicates that this item applies to this E.C. Level.
    3.2. No x (cross) in the E.C. Level column indicates that this item does not apply to this E.C. Level.
    3.3. If the functionality described by the item is not available on your board don't take into account this item. To know the functionalities available or not on your board, read the User's Guide associated with your board version.

Note Each item is fully described in section 4.4 “Item Detailed Description" page 10.

4.2 Revision Guide Table - Functional E.C. Levels

For early boards in E.C.Level 1xxxxx please contact Kontron.

Item	CRP	Description	E.C. Levels									
			2x002	2x003	2x004	2x006	3x003	3x004	3x005	4x005	4x006	4x007
1	-	cPLD fails to reset local board via VPX SYSRESET	X	X								
2	-	cPLD power sequencer not fully compliant with Intel specifications (part 2)	X	X								
3	-	cPLD interrupts management for temperature alerts not very convenient	X	X								
4	-	Enhancement of the alert reporting done by cPLD via backplane I2C bus	X	X								
5	-	Enhancement about PCIe controller PEX875 (I2C bus, CRC error log)	X	X								
6	4116	a) Unexpected SYSRESET behavior: Early reboot after local reset. b) Unexpected SYSRESET behavior: Early reboot after external SYSRESET. c) Unexpected SYSRESET behavior: SYSRESET asserted during halt. d) Unexpected SYSRESET behavior: SYSRESET duration.	X	X								
7	-	Spurious SYSRESET at power-on	X	X								
8	-	Enhancement of port 80 handling	X	X								
9	-	Enhancement of reset management at power-up	X	X								
10	-	Enhancement of power monitoring management	X	X			(1)	(1)	(1)			
11	4049	16 GB dual rank memory speed configuration limited to DDR3-1333	X	X	X	X		X	X	X		
12	4056	COM2 RTS/CTS handshaking not functional.	X	X	X	X						
13	4082	cPLD programming through LPC interface may fail	X									
14	4080	1000BASE-T MDI common mode output voltage slightly out of IEEE 802.3 specification	X	X	X	X	X	X	X	X	X	X
15	4085	Correctable errors on PCIe gen3 backplane link	X	X	X	X	X	X	X	X	X	X
16	4084	High Definition Audio, XMC I/O, PCH PCIe1 x1 options limitations	X	X	X	X	X	X	X	X	X	X
17	4191 4193	Board hangs below 5°C with internal VCORE power supply failure	X	X	X							
18	4187	Board hangs with internal PEX8725 +0.9V power supply failure	X	X	X		X	X				
19	4213	Battery lifetime impacted by the reverse current of the protection diode	X	X	X	X	X	X				
20	4210	Corrupted EEPROM of PCIe controller PEX8725 cannot be restored	X	X								
21	4200	When reset to and from VPX is enabled, disabling CPU core or hyperthreading may lead to infinite reset loop.	X	X	X	X	X	X	X	X	X	X
22	4192	Wrong package size for RTC resistor in bill of material					X	X				
23	4189	Correctable ECC errors below -30°C - **RC Class only**					X	X	X	(2)	(2)	(2)
24	4188	Cold start failures at -40°C - **RC Class only**					X					

(1) This erratum cannot occur on PCB rev C (no 16 GB version built with this PCB revision).

(2) This erratum is not directly related to an E.C. Level but to a serial numbers. See details in item 23 description.

Item	CRP	Description	E.C. Levels									
			2x002	2x003	2x004	2x006	3x003	3x004	3x005	4x005	4x006	4x007
25	4209	Correctable errors on PCIe Gen2 link between CPU and 10 GEth controller i82599 at -40°C - RC Class only					X	X				
26	4252	Low Frequency Mode selection issue	X	X	X	X	X	X	X	X	X	X
27	4250	LED L5 lit up red (as in Processor Hot Event) when low frequency mode is forced via microswitch	X	X	X	X	X	X	X	X	X	X
28	-	Evolution: Bill of Material adjustments								X		
29	4249	Low internal 3.3V Standby power supply may generate voltage alert at high temperature	X	X	X	X	X	X	X	X	X	
30	4251 4186	Display instability when using Mini Display Port to VGA adapter	X	X	X	X	X	X	X	X	X	X
31	4212	Poor LPC performance	X	X	X	X	X	X	X	X	X	X
32	4253	XMC connectors height not compliant with VITA48.2 in 1 inch pitch configurations (12 mm XMC stack).	X	X	X	X	X	X	X	X	X	X

4.3 Revision Guide Table - Mechanical E.C. Levels

Mechanical E.C. Levels for SA Class Boards

Item	CRP	Description	E.C. Levels								
			xxxxxA0	xxxxxA1	xxxxxA2	xxxxxA3	xxxxxA4	xxxxxA5	xxxxxA6		
M1	4057	VPX PCIe switch PEX8725 needs an heat sink to withstand max temperature in SA class	X								
M2	4050	Cooling fins slightly twisted on first heat sink batches	X	X							
M3	4091	VX3044 mechanical configuration do not withstand VITA 47 EAC1 shocks/vibrations specifications	X	X	X	X	X				
M4	4092	XMC daughter card extraction may be difficult on VX304x with XMC option	X	X	X	X	X				
M5	-	Evolution: Compatibility with PCB revD	X	X	X	X	X	X			

Mechanical E.C. Levels for RC Class Boards with XMC slot

The order code of these boards is VX304x-RCxx-xxxxYxx where Y = 1 or 2

There is no mechanical erratum for this type of board. The up-to-date E.C. Level is D1.

The transition from E.C. Level D0 to D1 was related to production improvement and does not impact the product functionalities.

Mechanical E.C. Levels for RC Class Boards without XMC slot

The order code of these boards is VX304x-RCxx-xxxxYxx where Y ≠ 1 or 2

There is no mechanical erratum for this type of board. The up-to-date E.C. Level is D2.

An evolution has been implemented:

Item	CRP	Description	E.C. Levels		
			XxxxxD1	xxxxxD2	
M_RC_noXMC1	-	Production improvement. Suppression of one extractor.	X		

4.4 Item Detailed Description for Functional E.C. Levels

Each item applies only to a specific group of E.C. Levels.
Refer to the table available in section 4.2 "Revision Guide Table - Functional E.C. Levels" page 7 to find the specific E.C. Levels associated to a specific item.

Item #1 cPLD fails to reset local board via VPX SYSRESET

Description:	Activating VPX_RST bit in cPLD (reg 0x70 bit 2) resets only other boards in VPX chassis and not the local board itself, which is not compliant to specification. The only case when the local board is not reset is when VPX2LOC bit masks SYSRESET. Fixed in cPLD V6.
Impact:	Board not reset when expected
Solution:	Fixed in E.C. Levels 2x004, 3x004 and 4xxxx.

Item #2 cPLD power sequencer not fully compliant with Intel specifications (part 2)

Description:	The timing of PWROK signal in cPLD power sequencer is not compliant with Intel Panther Point PCH specifications (Chapter 8.7: PWROK should be generated not sooner than 99 ms after PCIe power rails). Fixed in cPLD V6.
Impact:	No known functional impact.
Solution:	Fixed in E.C. Level 2x004 and 3x004.

Item #3 cPLD interrupts management for temperature alerts not very convenient

Description:	The alert issued by onboard thermal sensors LM73 and NUVOTON are signaled by interrupts but their deactivation is not properly handled in cPLD revision V5: either the interrupt must be masked or the status must be polled until the alert disappears. Fixed by cPLD V6 (reg 0xF bit 2 changed to RW in order to be able to clear interrupt by writing 0 + generate an interrupt on the deactivation of the alert if interrupt has been cleared after assertion).
Impact:	No known critical impact.
Solution:	Workaround: Mask the thermal interrupt or wait for the end of the alert by polling. Fixed in E.C. Level 2x004 and 3x004.

Item #4 Enhancement of the alert reporting done by cPLD via backplane I2C bus

Description: Two status bits added in cPLD reg 0x74 :

- bit 7 for temp_alert (PLD_PECI_ALERT_n or PLD_PCH_TEMP_ALERT_n)
- bit 6 for POST error (PBIT run with error or RTC battery low; using information from registers 0x2 and 0x3)

Implemented in cPLD V6.

Impact: Enhancement: cPLD reports temp_alert and POST errors on backplane I2C

Solution: Enhancement: E.C. Level 2x004 and 3x004.

Item #5 Enhancement about PCIe controller PEX875 (I2C bus, CRC error log)

Description: Enhancement about PCIe controller PEX8725:

- Implementation of I2C access to PEX by cPLD: I2C bus routed between cPLD and PEX and I2C enable bit defined in cPLD (0x71 bit 0).
- EEPROM CRC error logged in cPLD (0x76 bit 0). Can be accessed from backplane I2C.

Implemented in cPLD V6 and with hardware modifications

Impact: Enhancement: I2C access to PCIe controller PEX8725 via cPLD and EEPROM CRC controlled.

Solution: Enhancement: E.C. Level 2x004 and 3x004.

Item #6 CRP 4116

a) Unexpected SYSRESET behavior: Early reboot after local reset

Description: When a VX3040 with SYSRESET enabled both from and to PCIe backplane is reset by Linux "reboot" command or EFI shell "reset" command, it will start rebooting 300 to 600 ms before the end of SYSRESET activation. Fixed in cPLD V6.

Impact: In PCIe systems with a VX3040 as system controller, the VX3040 may probe the backplane PCIe bus before PCIe agents are ready to respond, and the probe result will not be correct.

Solution: Workaround: Delay PCIe probing after reset.

Fixed in E.C. Level 2x004 and 3x004.

b) Unexpected SYSRESET behavior: Early reboot after external SYSRESET

Description: A VX3040 which has its local reset asserted (signal PLTRST# asserted) during normal operation (ie not immediately after power-on) will ignore a SYSRESET activated by the backplane and could therefore restart before the SYSRESET deactivation. Fixed in cPLD V6.

Impact: Except at power-up where the VX3035 will behave normally the VX3035 could start unexpectedly before a SYSRESET deactivation on VPX bus.

Solution: Workaround: Ensure that all PCIe agents drive SYSRESET only at powerup or ensure that an early start of the VX3040 (i.e. before SYSRESET deassertion) has no impact on the system. Fixed in E.C. Level 2x004 and 3x004.

c) Unexpected SYSRESET behavior: SYSRESET asserted during halt

Description: When a VX3040 is halted by Linux "halt" or "shutdown" command (signal PLTRST# is activated), the signal VPX SYSRESET is unexpectedly asserted. Fixed in cPLD V6.

Impact: Halting a VX3040 in a system will reset other PCIe agents if their SYSRESET input is enabled.

Solution:	Workaround: Disable SYSRESET output in VX3040 (through cPLD register 0x70) before issuing a halt. Fixed in E.C. Level 2x004 and 3x004.

d) Unexpected SYSRESET behavior: SYSRESET duration

Description:	The duration of SYSRESET varies from 300 ms to 600 ms (nominal). Fixed in cPLD V6.
Impact:	No known impact but should be taken into account when synchronising several boards in a system.
Solution:	Fixed in E.C. Level 2x004 and 3x004.

Item #7 Spurious SYSRESET at power-on

Description:	**Case 1**: When hyperthreading is disabled and SYSRESET output is enabled in the BIOS settings, a spurious SYSRESET pulse is generated 2s after power-on (the local reset issued by BIOS after deactivating hyperthreading is propagated on VPX bus). Fixed in cPLD V6 in conjunction with BIOS ID13010. **Case 2**: To avoid spurious SYSRESET at power-up, the cPLD must assert SYSRESET even if 3V3 standby powergood signal is not yet activated. Fixed in cPLD V6
Impact:	Spurious SYSRESET asserted at power up.
Solution:	Fixed in E.C. Level 2x004 and 3x004.

Item #8 Enhancement of port 80 handling

Description:	Snoop every write to port 80 and update cPLD register 0x75 accordingly. Implemented in cPLD V6.
Impact:	Enhancement of port 80 handling
Solution:	Enhancement: E.C. Level 2x004 and 3x004.

Item #9 Enhancement of reset management at power-up

Description:	Mask reset sources until all power supplies are ON to prevent a reset (SYSRESET for example) from doing transitions on PCH_SYSRST / RSMRST / SYS_PWROK during power-on. Implemented in cPLD V6.
Impact:	Enhancement of reset management.
Solution:	Enhancement: E.C. Level 2x004 and 3x004.

Item #10 Enhancement of power monitoring management

Description:	Added a 100 mS deglitch on VPX powergood in case of low VPX slew rate. Implemented in cPLD V6.
Impact:	Enhancement of power monitoring management
Solution:	Enhancement: E.C. Level 2x004

Item #11 16 GB dual rank memory speed configuration limited to DDR3-1333. - CRP 4049

Description: Because of possible correctable ECC errors in the memory interface at 1600 MHz, 16 GB dual rank memory configuration operates at 1333 MHz instead of 1600 MHz. A hardware fix has been defined but not implemented in an E.C. Level.

Impact: 16 GB dual rank memory speed configuration forced to DDR3-1333

Solution: A hardware fix has been defined but not implemented on PCB rev A (E.C. Level 1xxxx) or PCB rev B (E.C. Level 2xxxx). Boards with PCB rev C (E.C. Level 3xxxxx) cannot be impacted since this memory capacity was not built.

Fixed on PCB D for E.C. Level 4x006 and beyond.

Item #12 COM2 RTS/CTS Handshaking not functional - CRP 4056

Description: COM2 is only available with Rx/Tx simplified mode. No RTS/CTS handshaking available.

Impact: COM2 in Rx/Tx simplified mode only.

Solution: None. Fixed in E.C. Levels 3xxxx and 4xxxx.

Item #13 cPLD programming through LPC interface may fail - CRP 4082

Description: The cPLD programming process may fail when LPC bus interface is used. The JTAG interface must be used.

Impact: cPLD cannot be programmed from LPC bus interface.

Solution: Fixed in E.C. Level 2x003 and 4xxxx.

Item #14 1000BASE-T MDI common mode output voltage slightly out of IEEE 802.3 specification - CRP 4080

Description: 70 mV measured in worst case for MDI common mode out voltage , above 50 mV specified by IEEE 802.3.

Impact: There are no known functional failures.

Solution: Under investigation

Item #15 Correctable errors on PCIe gen3 backplane link - CRP 4085

Description: When set to gen3 speed mode, the PCIe controller PEX8725 reports correctable errors in its error counter. These errors are rare and do not alter data integrity nor performance.

Impact: Errors automatically corrected.

Solution: Under investigation

Item #16 High Definition Audio, XMC I/O, PCH PCIe1 options limitations - CRP 4084

Description: High Definition Audio (HDA), XMC I/O, PCH PCIe1 options not tested.

Impact: HDA, XMC I/O PCIe1 options are available but may be limited

Solution: If one of these options is required, contact Kontron.

Item #17 Board hangs below 5°C with internal VCORE power supply failure. - CRP 4191 & 4193

Description: On some boards and at low temperature (below 5°C), fast internal current variations on VCORE power supply may cause rare power supply failures. When this happens, the board hangs with LED1, LED3 and LED5 switched on in red. Two possible fixes:

- Disable C Ctates in BIOS setting menu.
- Hardware fix in E.C.Level 2x006.

Note: Different fix for VX3042 (E.C. Level 28006) and VX3044 (E.C. Level 20006)

Impact: Board fails with error state LED1, LED3, LED5 red. There is no risk of board damage.

Solution: VX3042: Fixed in E.C. Level 28006
VX3044: Fixed in E.C. Level 20006

Fixed in E.C. Level 3xxxx and 4xxxx.

Item #18 Board hangs with internal PEX8725 +0.9V power supply failure - CRP 4187

Description: Due to a flawed PCB footprint for Enpirion part EN63A0 allowing contact between a test pad and the thermal GND pad, PCIe controller power supply V_PEX may exhibit rare, erratic failures. This causes the board to hang with LED1, LED2 and LED5 switched on in red. This has happened only on RC boards under particular mechanical constraints, either at powerup or when running at high temperature. This is fixed by replacing the EN63A0 with a modified one (isolated test pads).

Impact: Board hangs with error state LED1, LED2, LED5 red. There is no risk of board damage.

Note: Failure never showed up on E.C.Levels 2xxxx.

Solution: Fixed in E.C. Level 2x006 and 3x005 and 4xxxx..

Item #19 Battery lifetime impacted by the reverse current of the protection diode - CRP 4213

Description: The reverse current of the diode initially selected to protect the battery output voltage (BAT54CW) is too high. The battery lifetime is reduced to 5 years (worst case leakage at 25°C) or event 8 months (worst case leakage at +85°C) from the 10 years originally specified. The reverse current of the diode initially selected to protect the battery output voltage (BAT54CW) is too high. The battery lifetime is reduced to 5 years (worst case leakage at 25°C) or event 8 months (worst case leakage at +85°C) from the 10 years originally specified. Fixed by changing diode part number.

Impact: Battery life time reduced to 5 years worst case (25°C) or 8 months worst case (85°C)

Solution: A hardware fix has been defined but not implemented on PCB rev B (E.C. Level 2xxxx).

Fixed in E.C. Levels 3x005 and 4xxxx.

Item #20 Corrupted EEPROM of PCIe controller PEX8725 cannot be restored via PCIe - CRP 4210

Description: Due to a limitation about mask BA of PCIe controller PEX8725 chipset, a corrupted EEPROM cannot be restored via PCIe access. The only way to restore content is to unsolder EEPROM, reprogram et re-solder.

Fixed in E.C. Level 2x004 by adding an I2C link between PEX8725 and PLD: the EEPROM can then be restored via I2C accesses.

Impact: If eeprom of PEX8725 is corrupted, this chipset will not be available.

Solution: Workaround: Unsolder, reprogramm, resolder EEPROM.
Fixed in E.C. Level 2x004, 3xxxx and 4xxxx.

Item #21 Disabling CPU core or hyperthreading leads to infinite reset loop - CRP 4200

Description: In the following configuration :

- Hyperthreading or some CPU cores disabled
- Board with cPLD version V1,V2,V3,V4 or with cPLD version V6,V7 but with BIOS < ID14038
- "VPX Resets Output" and "VPX SYSRESET Input" enabled

the board enters an infinite reset loop at BIOS startup, with LED3 blinking red/green/off.

Note: To recover, set switch "BIOS_FAILSAFE" SW2[2] on, enter setup (this will restore default configuration), exit saving changes, set switch back off.

Will be fixed in cPLD rev V8.

Impact: Infinite reset loop if all conditions are met.

Solution: Workaround: None (except disabling SYSRESET input or output, or keeping Hyperthreading/ cores enabled) - Fixed in future E.C. Level

Item #22 Wrong package size for RTC resistor in bill of material - CRP 4192

Description: Due, to erroneous bill of material in PCB REV C (E.C. Levels 3xxxx), the resistor R1718 connected to PCH Real Time Clock does not have the correct package (0603 instead of 0402). This has never impacted the RTC function.

Impact:	No known impact.
Solution:	Fixed in E.C. Level 3x005

Item #23 Correctable ECC errors below -30°C - RC Class Only - CRP 4189

Description:	On early RC class production batches implementing commercial DDR3 memory parts, single correctable ECC errors may show up below -30°C. . This error is not strictly related to an ECLevel but to a serial number
Impact:	No direct impact since single ECC errors are automatically corrected. Boards potentially impacted: up to serial number 1813xxxxxx289
Solution:	None for boards with serial number < 1813xxxxxx289 and showing errors. Fixed on boards manufactured after serial number 1813xxxxxx289.

Item #24 Cold start failures at -40°C - RC Class Only - CRP 4188

Description:	Due to insufficient switching frequency, the internal Vcore power supply may fail during cold start at low temperature (-20°C and below). When this happens, the board hangs with LED1, LED3 and LED5 switched on in red.
Impact:	Board fails with error state LED1, LED3, LED5 red. There is no risk of board damage.
Solution:	Fixed in E.C. Level 3x004 and 4xxxx.

Item #25 Correctable errors on PCIe Gen2 link between CPU and 10 GEth controller i82599 at -40°C - RC Class Only - CRP 4209

Description:	Due to erroneous bill of material, the crystal quartz Y2901 connected to i82599 (chipset 10GEthernet) is not in industrial grade. This could induce at low temperature (-40°C), correctable errors on the Gen2 PCIe link between the i82599 controller and the CPU. These errors are rare and do not alter data integrity nor performance.
Impact:	Errors automatically corrected.
Solution:	Fixed in E.C. Level 3x005 and 4xxxx.

Item #26 Low Frequency Mode selection issue - CRP 4252

Description:	Due to insufficient drive strength setting in cPLD, the selection of Low Frequency Mode by switches SW3.1=ON and SW3.2=ON may not work.
Impact:	Low Frequency Mode cannot be selected via SW3.1=ON and SW3.2=ON. **Note:** Failure never showed up in the field.
Solution:	Fixed in future E.C. Level

Item #27 L5 LED lit up red (as in Processor Hot Event) when Low Frequency Mode is selected - CRP 4250

Description:	When Low Frequency Mode is selected with microswitches SW3.1=ON and SW3.2=ON, the CPLD activates the signal PROCHOT to force the processor frequency to its smallest value (0.8GHz or 1.2 GHz). In this case, the L5 LED should not light up red as in Processor Hot Event (signal PROCHOT driven by processor to indicate overheating conditions).
Impact:	Misleading LED information.
Solution:	Fixed in future E.C. Level

Item #28 Evolution: Bill of Material adjustments

Description:	ECLevel 4x006 includes various adjustments of the components equipment to enhance power supplies efficiency, battery accessibility, fuse protection accuracy, dual die memory management.
Impact:	Enhancement. No functional impact.
Solution:	NA

Item #29 Low internal 3.3V Standby power supply may generate voltage alert at high temperature - CRP 4249

Description:	Due to insufficient margin between the output of internal 5V-to-3.3V_standby LDO and the minimum required voltage (3.136V) a voltage alert may be generated during high temperature operation (above 65°C).
Impact:	No functional impact. An error is reported in PBIT or other applications which monitor the internal 3.3V Standby power supply.
Solution:	Fixed in E.C. Level 4x007.

Item #30 Display instability when using Mini Display Port to VGA adapter - CRP 4251 & 4186

Description:	Due to lack of margin on Display Port signals, active adapters DP-to-VGA are prone to VGA instability
Impact:	VGA instability issues (black screen for about 1 sec).
Solution:	Do not use Mini Display Port to VGA adapters. Use only full Display Port passive cables.

Item #31 Poor LPC performance could impact FRAM accesses - CRP 4212

Description:	The expected single byte throughput on the LPC bus is 2.5 MB/sec but it has been measured at 400 kB/sec. The devices connected to this bus are the Trusted Platform Module (TPM), the SIO (serial), the CPLD and downstream I2C busses (EEPROM, NTC7802 sensor, FRAM). These devices will not be impacted except the FRAM which woud benefit from a higher datarate.

Impact:	Low performance on FRAM accesses.
Solution:	Under investigation. Please contact Kontron if high bandwith to FRAM is needed.

Item #32 XMC connectors height not compliant with VITA48.2 in 1 inch pitch configurations (12 mm XMC stack). - CRP 4253

Description:	VITA 42 and VITA 48 stipulate that when defining a 12 mm stack for a XMC slot (i.e. for a 1 inch pitch chassis), the additional 2 mm (from the standard 10 mm) must be provided by the mother board connectors. Since such connectors are not yet available by SAMTEC, the SAMTEC ASP-103612-04 suited for 10 mm stack is mounted on all versions of VX3040 (10 mm stack and 12 mm stack). Consequently, a 12 mm XMC stack can only be achieved by mounting a special connector on the XMC (SAMTEC ASP-153860-01).
Impact:	Standard XMC mezzanine with 10 mm stack cannot be mounted on RC boards or 1 inch SA boards.
Solution:	Workaround: Equip SAMTEC ASP-153860-01 or equivalent on the XMC to achieve 12 mm stack.

4.5 Item Detailed Description for Mechanical E.C. Levels

Each item applies only to a specific group of E.C. Levels.
Refer to the table available in section 4.3 “Revision Guide Table - Mechanical E.C. Levels” page 9 to find the specific E.C. Levels associated to a specific item.

Item #M1 VPX PCIe switch PEX8725 needs an heat sink to withstand max temperature in SA class - CRP 4057

Description: Depending on air flow conditions, the junction temperature of the VPX PCIe switch may rise above its maximum specification at 55°C ambient temperature.

An heat sink is necessary above 30°C ambient temperature.

Impact: VPX PCIe switch may fail above 30°C.

Solution: Fixed in E.C. Level A1

Item #M2 Cooling fins slightly twisted on first production batches - CRP 4050

Description: Heat sink part RAD-VX3040-1-V02 may present some cooling fins slightly twisted. Thermal performance is not altered.

Impact: No functional impact.

Solution: Fixed in E.C. Level A2

Item #M3 VX3044 mechanical configuration do not withstand Vita47 EAC1 shocks/vibrations specifications - CRP 4091

Description: VX3044 mechanical configuration does not withstand Vita47 EAC1 shocks/vibrations specifications. Some boards exhibit PCB flexture. To fix this, two side stiffeners and two stops have been added in E.C. Level A5.

Impact: Not fully VITA 47 EAC1 compliant.

Solution: Fixed in E.C. Level A5

Item #M4 XMC daughter card extraction may be difficult on VX304x with XMC option - CRP 4092

Description: XMC extraction is difficult without using a tool.

Impact: XMC extraction may be difficult.

Solution: Fixed in E.C. Level A5

Item #M5 Evolution: Compatibility with PCB revD

Description:	E.C. Level xxxxxA6 has been defined to adapt the heatsink to the PCB revD. Some modifications have also been added to allow Personnality Module equipments.
Impact:	Evolution. No functional impact.
Solution:	NA

4.6 Compliance to REACh Directive

4.6.1 Definitions

- **REACh Directive**: EU Directive 1907/2006
- **SVHC Candidate List**: June 16 2014; 155 substances
- **Communication Requirement per REACh Directive**: If any SVHC on candidate list is present in the product with a concentration above 0.1% by weight (ie 1000 ppm), the provider is obliged to inform the recipients of the article along the supply chain about the chemical name(s) and how the article can be safely used.
- **Article definition per REACh Directive**: Under REACh Directive, an article is defined as an object which during production is given a special shape, surface or design, which determines its function to a greater degree that does its chemical composition.

  Several objects can be identified on an electronic board: Electronic components, mechanical parts, thermal interfaces, labels, printed Circuit Board (PCB), bare board (electronic components assembled on PCB), whole board (bare board with mechanical parts)...

  Whether the 0.1% threshold should apply to the entire electronic board or to its individual components depends on the interpretation of the Directive and may differ from one country to another.
- **Part**: In this document, synonymous with electronic component.

4.6.2 SVHC List Verification

The verification performed by Kontron has been made at part level: Nine parts contain SVHC with concentration greater than 0.1% threshold as shown in the following table.

In the last row, the quantity of substance identified in these parts has been compared to the total mass of the bare board: the concentration is always well below the 0.1% threshold.

Manufacturer	Rayovac	Murata	Murata	Yageo	Yageo	Yageo	Yageo	Yageo	Yageo
Manufacturer Part Number	BR1225	GRM155R71C223KA01D	GRM188R60J225KE01D	YC124-JR-070RL	YC124JR-0710KL	YC124JR-0733RL	YC124JR-0739RL	YC124JR-0747KL	YC124JR-078K2L
Part Description	Lithium battery	Capacitor		Resistor array					
Qty	1	7	11	2	3	2	14	1	5
Subpart Name	Composition	Outer electrode-Glass		Primary glass					
Substance Name	1,2-dimethoxyethane	Diboron trioxide							
Substance CAS Number	110-71-4	1303-86-2							
Bare Board Mass (mg)	170000								
Part Mass (mg)	907.185	1.600	6.300	2.458					
Subpart Mass (mg)	NA	0.0191	0.1103	0.1103	0.0408				
Substance Quantity (mg)	81.64665	0.00382	0.02206	0.00326					
Concentration of Substance in Part (ppm)	9	0.23875	0.35016	0.13260					
Ratio Substance in Part / Bare Board Mass (ppm)	0.0480274	0.0000157	0.0001427	0.0000038	0.0000058	0.0000038	0.0000268	0.0000019	0.0000096

MAILING ADDRESS
Kontron Modular Computers S.A.S.
150 rue Marcelin Berthelot - BP 244
ZI TOULON EST
83078 TOULON CEDEX - France

TELEPHONE AND E-MAIL
+33 (0) 4 98 16 34 00
Sales: Order-ATD-Toulon@Kontron.com
Support: GSS-ATD-Toulon@Kontron.com

For further information about other Kontron products, please visit our Internet web site: www.kontron.com.