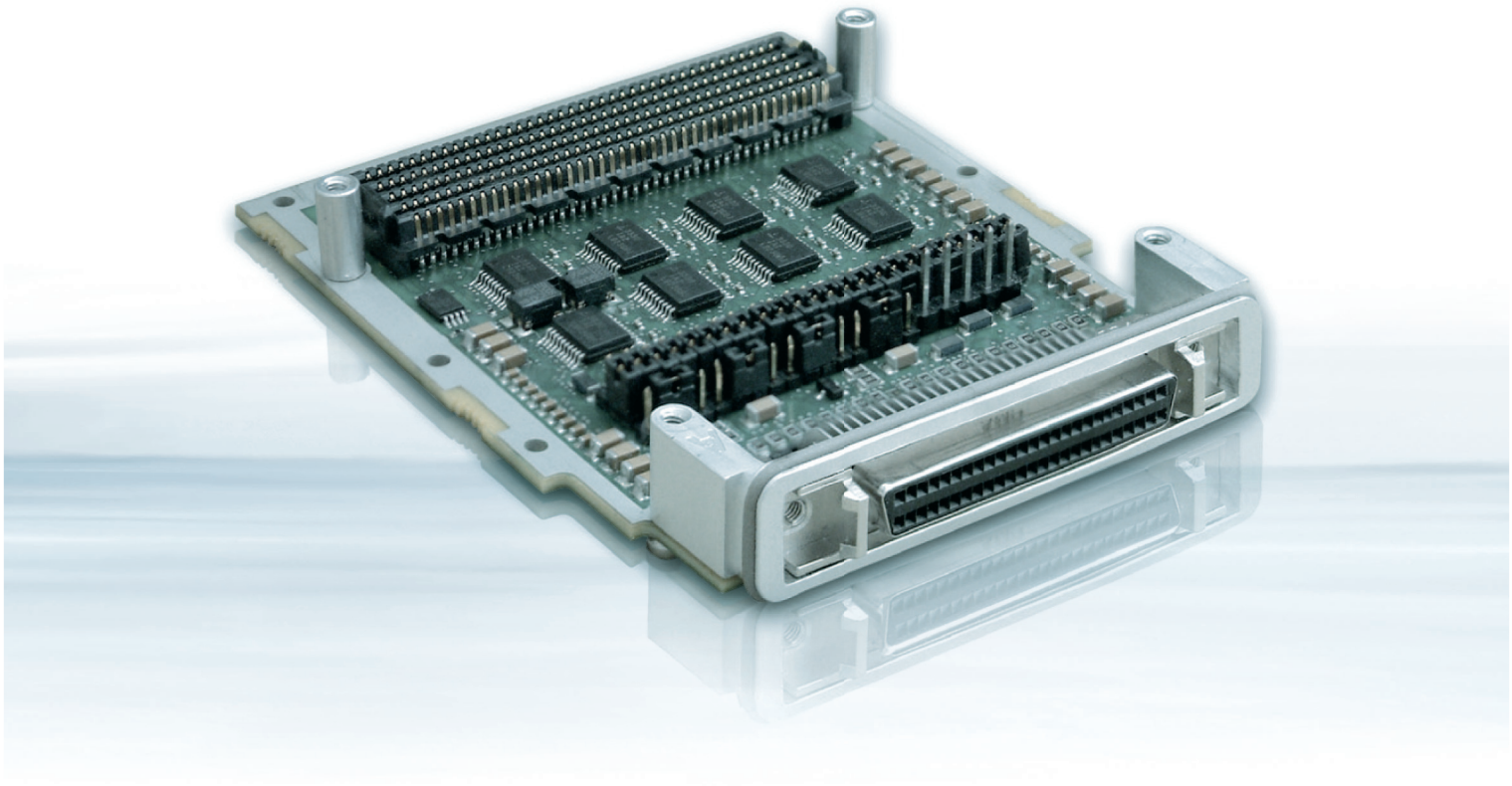
FMC-SERO



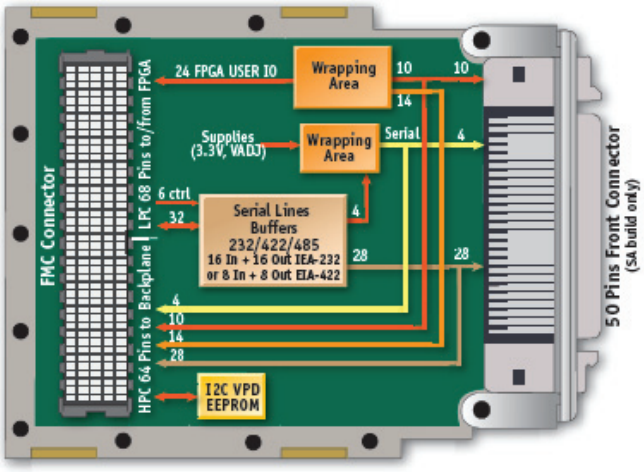
VITA 57 COMPLIANT FPGA MEZZANINE CARD (FMC)

- Buffering for up to 16 EIA-232 or 8 EIA-422/EIA-485 serial lines
- Up to 24 general purpose I/O from FPGA carrier
- Front and rear I/Os
- Air-cooled and conduction-cooled builds

FMC-SER0

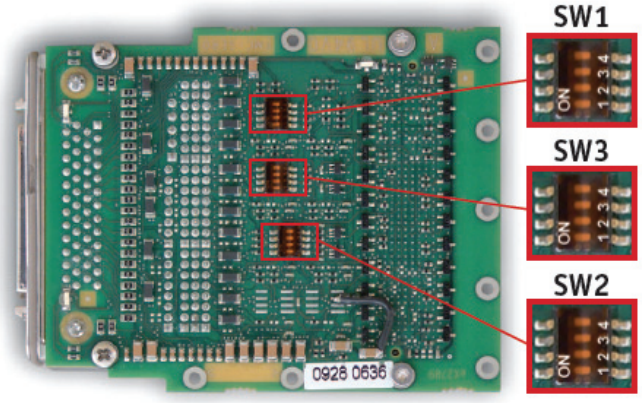
PRODUCT OVERVIEW

FMC-SER0 is an FMC HPC single-width module designed to interface with any VITA 57 host board such as Kontron VM6250 and VM6050 SBCs or VX3830 FMC carrier.
The FMC-SER0 is a VITA 57 mezzanine which features a High Pin Count (HPC) FMC connector and a 50-pin TYCO 0-787171-5 front connector For SA build, FMC-SER0 features two wrapping areas to select additional ground or GPIO on the connectors.



BOARD CONFIGURATION

Microswitches



MICROSWITCHES DESCRIPTION

SW1 - off (default position): no termination is activated

1	on: 100 Ohms resistor between RX1 and RX2 for differential termination
2	on: 100 Ohms resistor between RX3 and RX4 for differential termination
3	on: 100 Ohms resistor between RX5 and RX6 for differential termination
4	on: 100 Ohms resistor between RX7 and RX8 for differential termination

SW3 - off (default position): no termination is activated

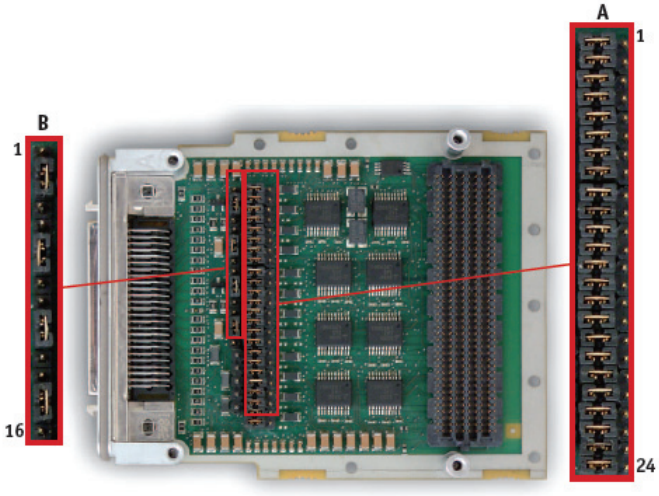
1	on: 100 Ohms resistor between RX9 and RX10 for differential termination
2	on: 100 Ohms resistor between RX11 and RX12 for differential termination
3	on: 100 Ohms resistor between RX13 and RX14 for differential termination
4	on: 100 Ohms resistor between RX15 and RX16 for differential termination

SW2 - off (default position): serial lines in EIA-422/485 mode

1	on: serial lines 1 to 4 operate in EIA-232 mode
2	on: serial lines 5 to 8 operate in EIA-232 mode
3	on: serial lines 9 to 12 operate in EIA-232 mode
4	on: serial lines 13 to 16 operate in EIA-232 mode

Jumpers / Wrapping Area (SA build only)

RC build features no jumpers, the default configuration being always enforced.



A Jumpers

Standard/default jumper position
GPIOn output on connector(s), n=1 to 24.
Alternate jumper position
Additionnal GND output instead of GPIOn on connector(s), n=1 to 24.

B Jumpers

PIN		PIN	
1	VADJ VITA 57	9	+5 V
2	TX15	10	TX16
3	TX15_ext	11	TX16_ext
4	Reserved	12	Reserved
5	Reserved	13	Reserved
6	RX15_ext	14	RX16_ext
7	RX15	15	RX16
8	+3.3 V	16	GND

Default jumper B positions:
Pins 2-3, 6-7, 10-11, 14-15, allowing RX/TX 15 and 16 to be propagated.

TECHNICAL INFORMATION

INTERFACE	- 24 FPGA GPIO front or rear - 16 EIA-232 or 8 EIA-422/EIA-485 EIA-232 or EIA-422/EIA-485 mode selection by group of 4 lines through micro switch or FPGA control - Two of the EIA-485 serial lines have a dedicated transmit enable from FPGA

FMC CONNECTOR PIN ASSIGNMENT

FMC CONNECTOR PIN NUMBER	FMC-SERO VITA 57 SIGNAL NAME FROM FPGA	FMC-SERO FROM FPGA I/O NAME	FMC-SERO VITA 57 SIGNAL NAME BACK TO REAR I/O	FMC CONNECTOR PIN NUMBER BACK TO REAR I/O	FMC CONNECTOR PIN NUMBER	FMC-SERO VITA 57 SIGNAL NAME FROM FPGA	FMC-SERO FROM FPGA I/O NAME	FMC-SERO VITA 57 SIGNAL NAME BACK TO REAR I/O	FMC CONNECTOR PIN NUMBER BACK TO REAR I/O
G6	LA0P	RX1	HA14P	J15	G21	LA20P	GPI07	HB2P	F22
G7	LA0N	RX2	HA14N	J16	G22	LA20N	GPI08	HB2N	F23
D9	LA1N	TX1	HA16P	E15	H25	LA21P	GPI09	HB10P	K31
D8	LA1P	TX2	HA16N	E16	H26	LA21N	GPI010	HB8P	F28
H7	LA2P	RX3	HA17P	K16	G24	LA22P	GPI011	HB10N	K32
H8	LA2N	RX4	HA17N	K17	G25	LA22N	GPI012	HB8N	F29
G10	LA3N	TX3	HA15P	F16	D23	LA23P	GPI013	HB14P	K34
G9	LA3P	TX4	HA15N	F17	D24	LA23N	GPI014	HB14N	K35
H10	LA4P	RX5	HA21P	K19	H28	LA24P	GPI015	HB12P	F31
H11	LA4N	RX6	HA21N	K20	H29	LA24N	GPI016	HB12N	F32
D12	LA5N	TX5	HA19P	F19	G27	LA25P	GPI017	HB17P	K37
D11	LA5P	TX6	HA19N	F20	G28	LA25N	GPI018	HB17N	K38
C10	LA6P	RX7	HA23P	K22	D26	LA26P	GPI019	HB20P	F37
C11	LA6N	RX8	HA23N	K23	D27	LA26N	GPI020	HB20N	F38
H14	LA7N	TX7	HB5P	E24	C26	LA27P	GPI021	HB18P	J36
H13	LA7P	TX8	HB5N	E25	C27	LA27N	GPI022	HB18N	J37
G12	LA8P	RX9	HB1P	J24	H31	LA28P	GPI023	HB16P	F34
G13	LA8N	RX10	HB1N	J25	H32	LA28N	GPI024	HB16N	F35
D15	LA9N	TX9	HB9P	E27	G18	LA16P	DXEN *(1)*		
D14	LA9P	TX10	HB9N	E28	G19	LA16N	DXEN1516 *(1)*		
C14	LA10P	RX11	HB11P	J30	G33	LA31P	LED1R-SW2.1 *(2)*		
C15	LA10N	RX12	HB11N	J31	G34	LA31N	LED1G-SW2.2 *(2)*		
H17	LA11N	TX11	HB19P	E33	G36	LA33P	LED2R-SW2.3 *(2)*		
H16	LA11P	TX12	HB19N	E34	G37	LA33N	LED2G-SW2.4 *(2)*		
G15	LA12P	RX13	HB15P	J33	G30	LA29P	reserved		
G16	LA12N	RX14	HB15N	J34	G31	LA29N	reserved		
D18	LA13N	TX13	HB21P	E36	H34	LA30P	reserved		
D17	LA13P	TX14	HB21N	E37	H35	LA30N	reserved		
C18	LA14P	RX15	HB6P	K28	H37	LA32P	reserved		
C19	LA14N	RX16	HB6N	K29	H38	LA32N	reserved		
H20	LA15N	TX15	HB4P	F25			GND	HA18P	J18
H19	LA15P	TX16	HB4N	F26			GND	HA18N	J19
D20	LA17P	GPIO01	HA20P	E18			GND	HA22P	J21
D21	LA17N	GPIO02	HA20N	E19			GND	HA22N	J22
C22	LA18P	GPIO03	HB3P	E21			GND	HB7P	J27
C23	LA18N	GPIO04	HB3N	E22			GND	HB7N	J28
H22	LA19P	GPIO05	HB13P	E30			GND	HB0P	K25
H23	LA19N	GPIO06	HB13N	E31			GND	HB0N	L26

(1) These signals control TXn outputs of buffers:
level 1: enabled
level 0: disabled
- DXEN: TX1,TX2,TX3,TX4,TX5,TX6,TX7,TX8,TX9,TX10, TX11,TX12,TX13,TX14
- DXEN1516 : TX15/TX16 pair

(2) These signals control the LEDs and also override if driven from FPGA the default mode of TXn/RXn buffers set by the switches:
level 1: EIA-422 or 485, LED OFF
level 0: EIA-232, LED ON
- LED1R_SW2.1: TX1, RX1, TX2, RX2, TX3, RX3, TX4, RX4
- LED1G_SW2.2: TX5, RX5, TX6, RX6, TX7, RX7, TX8, RX8
- LED2R_SW2.3: TX9, RX9, TX10, RX10, TX11, RX11, TX12, RX12
- LED2G_SW2.4: TX13, RX13, TX14, RX14, TX15, RX15, TX16, RX16

FRONT CONNECTOR PIN ASSIGNMENT (AIR COOLED VERSION ONLY)

The front connector is of type TYCO Part Number 0-787171-5.

(1) These pin numbers have been corrected since previous data-sheet (ref. #FMC-SERO# 10112011MB - Oct. 2011) to reflect actual connector pin assignment.

1	GND	50	RX_1	14	TX_9	37	HB13P_GPIO_5 / GND
2	TX_1	49	HA20P_GPIO_1 / GND	15	RX_10	36	TX_10
3	RX_2	48	TX_2	16	GND	35	RX_11
4	GND	47	RX_3	17	TX_11	34	HB13N_GPIO_6 / GND
5	TX_3	46	HA20N_GPIO_2 / GND	18	RX_12	33	TX_12
6	RX_4	45	TX_4	19	GND	32	RX_13
7	GND	44	RX_5	20	TX_13	31	GB2P_GPIO_7 / GND
8	TX_5	43	HB3P_GPIO_3 / GND	21	RX_14	30	TX_14
9	RX_6	42	TX_6	22	GND	29	RX_15
10	GND	41	RX_7	23	TX_15	28	HB2N_GPIO_8 / GND
11	TX_7	40	HB3N_GPIO_4 / GND	24	RX_16	27	TX_16
12	RX_8	39	TX_8	25	HB8P_GPIO_10 / GND	26	HB10P_GPIO_9 / GND
13	GND	38	RX_9				

ENVIRONMENTAL SPECIFCATION

	SA - STANDARD COMMERCIAL	RC - RUGGED CONDUCTION-COOLED
CONFORMAL COATING	Optional	Standard
AIRFLOW	1.5 m/s	NA
TEMPERATURE	VITA 47-Class AC1	VITA 47-Class CC4
COOLING METHOD	Convection	Conduction
OPERATING	0 °C to +55 °C	-40 °C to +85 °C
STORAGE	-45 °C to +85 °C	-45 °C to +85 °C
VIBRATION SINE (OPERATING)	20/500 Hz: 2 g	22/2,000 Hz: 5 g
RANDOM	VITA 47-Class V1	VITA 47-Class V3
SHOCK (OPERATING)	20 g/11 ms Half Sine	40 g/20 ms Half Sine
ALTITUDE (OPERATING)	-1,640 to 15,000 ft	-1,640 to 60,000 ft
RELATIVE HUMIDITY	90 % without condensation	95 % without condensation

ORDERING INFORMATION

ARTICLE	PART NO.	DESCRIPTION
SA - STANDARD COMMERCIAL		
FMC-SER0	FMC-SER0-SA-000	Air-cooled FPGA Mezzanine Card
RC - RUGGED CONDUCTION-COOLED		
FMC-SER0	FMC-SER0-RC-000	Conduction-cooled FPGA Mezzanine Card
ASSOCIATED PRODUCTS		
KIT-FMC	KIT-FMC-DEV	FMC/VITA 57 Development/test kit. Contains: Linux FPGA/ FMC EEPROM drivers, FPGA Test Image, User's Guide, FMC-SER0-SA-000 FMC card, USB FLASH Drive pre-loaded with Linux Fedora + VITA 57 drivers. Compatible with VM6250 (with FMC I/O option)
DRIVER / TEST	DR-6G-FMC	Linux Driver Kit for Development/Test FMC kit
ASSOCIATED DOCUMENTATION		
	SD.DT.F79	VITA 57 - Development Kit User's Guide
	SD.DT.F74	VITA 57 - Configuration

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