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» User Guide «

AM4150

Single Mid-Size AMC Module based on the
Freescale™ QorIQ™ P5020
Dual-Core Processor

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Kontron Modular Computers GmbH may be contacted via the following:

MAILING ADDRESS

Kontron Europe GmbH

Sudetenstraße 7

D - 87600 Kaufbeuren Germany

TELEPHONE AND E-MAIL

+49 (0) 800-SALESKONTRON

sales@kontron.com

For further information about other Kontron products, please visit our Internet web site: www.kontron.com.

Disclaimer

Table of Contents

List of Tables

List of Figures

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Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.

Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.

Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.

Note ...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

Warning!

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Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Warning!

This product has gold conductive fingers which are susceptible to contamination. Take care not to touch the gold conductive fingers of the AMC Card-edge connector when handling the board.

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Kontron grants the original purchaser of Kontron's products a ***TWO YEAR LIMITED HARDWARE WARRANTY*** as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of Kontron are valid unless the consumer has the express written consent of Kontron.

Kontron warrants their own products, excluding software, to be free from manufacturing and material defects for a period of 24 consecutive months from the date of purchase. This warranty is not transferable nor extendible to cover any other users or long-term storage of the product. It does not cover products which have been modified, altered or repaired by any other party than Kontron or their authorized agents. Furthermore, any product which has been, or is suspected of being damaged as a result of negligence, improper use, incorrect handling, servicing or maintenance, or which has been damaged as a result of excessive current/voltage or temperature, or which has had its serial number(s), any other markings or parts thereof altered, defaced or removed will also be excluded from this warranty.

If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

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Chapter 1

Introduction

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1. Introduction

1.1 Board Overview

The AM4150 is a highly integrated CPU board implemented as a Single, Mid-size Advanced Mezzanine Card (AMC) module. The design is based on the Freescale™ QorIQ™ P5020 dual-core Power Architecture® processor with integrated high-speed interconnect technology to balance processor performance with I/O system throughput for networking, storage, wireless infrastructure and general-purpose embedded applications.

The QorIQ™ P5020 processor is a highly integrated 64-bit system-on-chip (SOC) platform with up to 2.0 GHz core clock speed consisting of two e5500 cores, each with 32 kB L1 instruction cache, 32 kB L1 data cache and 512 kB backside L2 cache. Further processor features include a dual DDR3 memory interface, 2 MB shared L3 CoreNet platform cache (1 MB per memory channel), five Datapath Triple-Speed Ethernet Controllers (dTSECs), and either two x4 Serial RapidIO™ fabric interfaces or two x4 PCI Express I/O interfaces. Furthermore, one NAND flash memory (SSD) with up to 64 GB can be integrated into the AM4150 via a SATA Flash module.

The processor and the memory are soldered on the AM4150 which results in a robust design, higher Mean Time Between Failures (MTBF) and a significant improvement in cooling.

The AM4150 includes up to 8 GB unbuffered, dual-channel Double Data Rate (DDR3) memory with Error Checking and Correction (ECC) running at up to 1300 MHz. The board further provides up to 2 GB NAND flash memory via a NAND flash controller integrated in the processor.

As a “headless” AMC design (no onboard graphics controller), the AM4150 supports one standard RS-232 serial port (UART1) and up to two Gigabit Ethernet ports on the front panel as well as a variety of high-speed interconnect topologies to the system. In the Common Options Region up to two Gigabit Ethernet SerDes and up to two SATA interfaces are supported. In the Fat Pipes Region PCI Express, Serial RapidIO, and Gigabit Ethernet SerDes interfaces can be selected. In the Extended Options Region a debug port and a serial port are provided.

The AM4150 has full hot swap capability, which enables the board to be replaced, monitored and controlled without having to shut down the ATCA carrier board or the MicroTCA system. A dedicated Module Management Controller (MMC) is used to manage the board and support a defined subset of Intelligent Platform Management Interface (IPMI) commands and PICMG (ATCA/AMC) command extensions, which enables operators to detect and eliminate faults faster at module level. This includes monitoring several onboard temperature conditions, board voltages and the power supply status, managing hot swap operations, rebooting the board, etc. All in all, IPMI enhances the board’s availability and reliability while reducing the operating costs and the mean-time-to-repair.

Optimized for high-performance, packet-based telecom systems, the AM4150 is targeted towards, but not limited to the telecom market application such as radio network controllers, media streaming, traffic processing, database management and routing. The AM4150 also fits into all applications situated in industrial environments, including I/O intensive applications. The careful design and the selection of high temperature resistant components ensure a high product availability. This, together with a high level of scalability, reliability, and stability, make this state-of-the-art product a perfect core technology for long-life embedded applications.

The AM4150 is offered with various Board Support Packages such as VxWorks and Linux. Please contact Kontron for further information concerning the operation of the AM4150 with other operating systems.

1.2 Board-Specific Information

Due to the outstanding features of the AM4150, such as superior processing power and flexible interconnect topologies, this AMC board provides a highly scalable solution not only for a wide range of telecom and data network applications, but also for several highly integrated industrial environment applications with solid mechanical interfacing.

Some of the AM4150's outstanding features are:

- Support for the following processors:
  - Freescale™ QorIQ™ P5020 processor, 2.0 GHz, 800 MHz platform frequency
  - Freescale™ QorIQ™ P5020 processor, 1.6 GHz, 600 MHz platform frequency
- Up to 8 GB DDR3 SDRAM memory with ECC running at up to 1300 MHz
- AMC interconnection:
  - Common Options Region: up to two Gigabit Ethernet SerDes interfaces and up to two SATA ports
  - Fat Pipes Region: 8 lanes configurable for PCI Express, Serial RapidIO, and Gigabit Ethernet SerDes connections
  - Extended Options Region: serial port, debug port, two GPIs (on request), two GPOs (on request)
  - Bidirectional PCI Express reference clock (FCLKA)
- Full hot swap support
- Up to 2 GB NAND flash memory via a NAND flash controller integrated in the processor
- One serial port on front I/O (RS-232)
- Up to two Gigabit Ethernet ports on front I/O
- Up to 64 GB NAND flash memory via an optional SATA Flash module
- Two SPI boot flashes for two separate U-Boot bootloader images:
  - One standard SPI boot flash
  - One recovery SPI boot flash
- One 8 MB SPI flash for operating system use
- Dedicated IPMI Module Management Controller (MMC) with external MMC firmware flash
- Watchdog timer
- Multiple interfaces for debugging and manufacturing purposes
- Four bicolor User-Specific LEDs (providing debugging information, etc.)
- One onboard DIP switch (for selecting the SPI boot flashes, overwriting E-Keying, etc.)
- microSDHC socket
- Standard temperature range: -5°C to + 55°C
- Passive heat sink solution for forced airflow cooling
- Single Mid-size AMC module
- Denx U-Boot bootloader
- Designed to be compliant with the following specifications:
  - PICMG® AMC.0 R2.0, Advanced Mezzanine Card Specification
  - PICMG® AMC.1 R2.0, PCI Express™ on AdvancedMC™
  - PICMG® AMC.2 R1.0, Ethernet Advanced Mezzanine Card Specification
  - PICMG® AMC.4 R1.0, Serial RapidIO on AdvancedMC™ Specification
  - PICMG® MTCA.0 R1.0 Micro Telecommunications Computing Architecture Base Specification
  - IPMI - Intelligent Platform Management Interface Specification, v2.0, R1.0

1.3 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the AM4150.

Table 1-1: System Relevant Information

SUBJECT	INFORMATION

Hardware Requirements	The AM4150 can be installed on any AMC-supporting carrier board or MicroTCA backplane with the following AMC Card-edge connector port mapping:
	• Common Options Region ports 0-1:
	  • Up to two Gigabit Ethernet SerDes ports
	• Common Options Region ports 2-3:
	  • Up to two SATA ports
	• Fat Pipes Region ports 4-7:
	  • One x4 PCI Express interface or
	  • One x4 Serial RapidIO interface
	• Fat Pipes Region ports 8-11:
	  • One x4 PCI Express interface or
	  • One x4 Serial RapidIO interface or
	  • Up to three Gigabit Ethernet SerDes ports
	• Extended Options Region port 14:
	  • One debug port
	• Extended Options Region port 15:
	  • One serial port
	• Extended Options Region port 16:
	  • Two general purpose inputs (GPI), on request
	  • Two general purpose outputs (GPO), on request
	• Clock:
	  • Bidirectional PCI Express reference clock, FCLKA
	For further information on the AMC interconnection, refer to Chapter 2.11, “AMC Interconnection”.

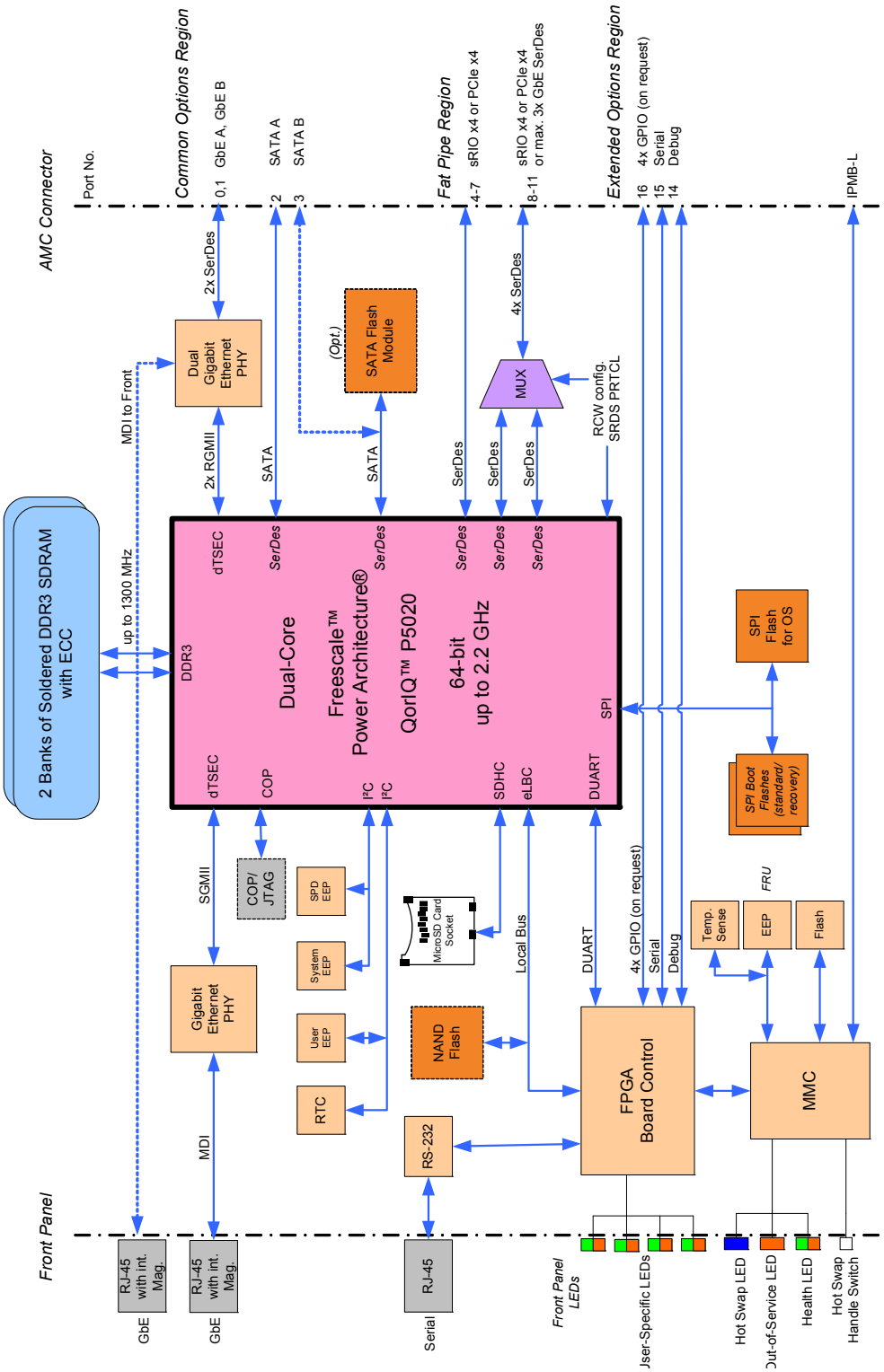
PCI Express Configuration	The AM4150 only supports the PCI Express root complex configuration; non-transparent bridge functionality is not supported.
Operating Systems	The board is offered with various Board Support Packages including VxWorks and Linux operating systems. For further information concerning the operating systems available for the AM4150, please contact Kontron.

1.4 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

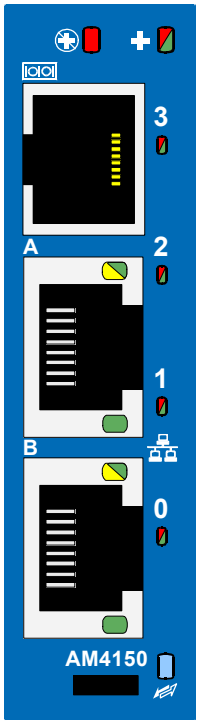
1.4.1 Functional Block Diagram

Figure 1-1: AM4150 Functional Block Diagram



1.4.2 Front Panel

Figure 1-2: AM4150 Front Panel



Module Management LEDs

- LED1 (red): Out-of-Service LED
- LED2 (red/green): Health LED
- HS LED (blue): Hot Swap LED

Connectors

- Serial Connector
- Gigabit Ethernet Connector

User-Specific LEDs 3..0

- ULED3 (red/green): AMC port 0 link status (green) + user-specific debug code (green) + general purpose (red/green/red+green)
- ULED2 (red/green): AMC port 1 link status (green) + user-specific debug code (green) + general purpose (red/green/red+green)
- ULED1 (red/green): User-specific debug code (green) + general purpose (red/green/red+green)
- ULED0 (red/green): User-specific debug code (green) + general purpose (red/green/red+green)

Integral Ethernet LEDs

- ACT (green): Ethernet Link/Activity
- SPEED (green/yellow/off): Ethernet Speed

Note ...

If the ULED 0..3 remain lit red after power-on, a failure is indicated before the U-Boot bootloader has started. For further information, please contact Kontron.

1.4.3 Board Layouts

Figure 1-3: AM4150 Board Layout (Top View)

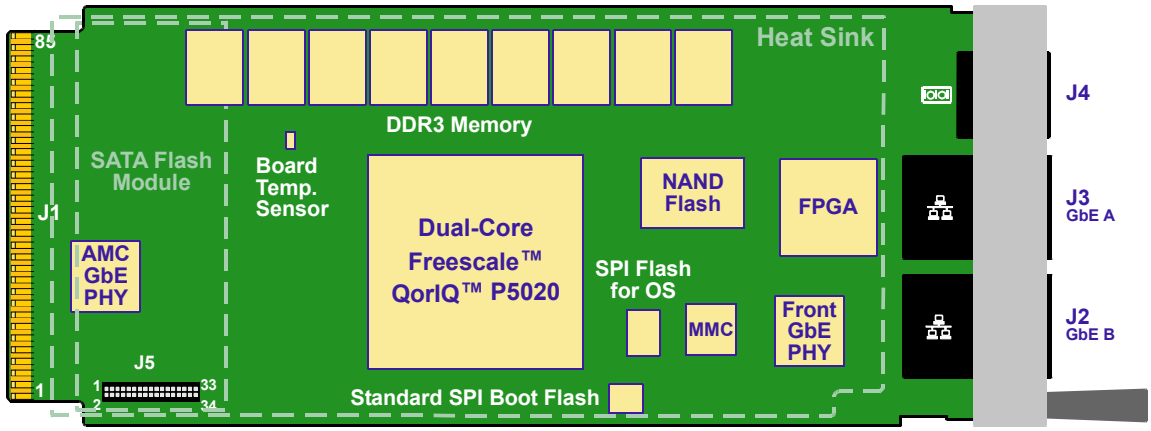
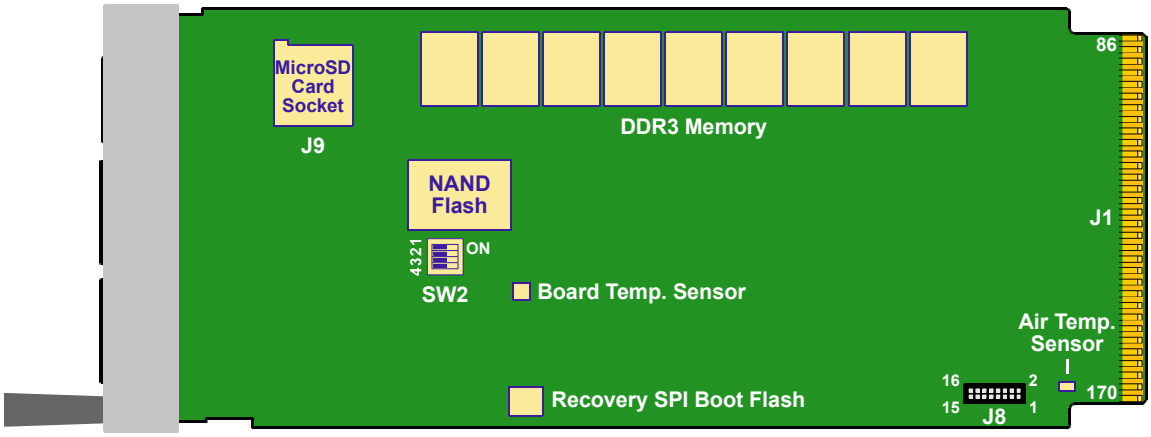


Figure 1-4: AM4150 Board Layout (Bottom View)



1.5 Technical Specification

Table 1-2: AM4150 Main Specifications

AM4150		SPECIFICATIONS
Processor	CPU	The AM4150 supports the following microprocessors: • Freescale™ QorIQ™ P5020 processor, 2.0 GHz, 800 MHz platform freq. • Freescale™ QorIQ™ P5020 processor, 1.6 GHz, 600 MHz platform freq. Further processor features: • Two 64-bit execution cores • System Memory interface with optimized support for dual-channel DDR3 SDRAM memory at 1300 MHz with ECC for the QorIQ™ P5020 processor with 2.0 GHz CPU frequency • System Memory interface with optimized support for dual-channel DDR3 SDRAM memory at 1200 MHz with ECC for the QorIQ™ P5020 processor with 1.6 GHz CPU frequency
	Integrated controllers	Controllers integrated in the CPU and utilized by the AM4150: eSDHC, eLBC, DUART, dTSEC, PCIe, sRIO, SPI, I²C.

Memory	Memory	Main memory:
		• Up to 8 GB, dual-channel DDR3 SDRAM memory with ECC running at up to 1300 MHz
		Cache structure:
		• 64 kB L1 cache for each core
		  • 32 kB instruction cache
		  • 32 kB data cache
		• 512 kB backside L2 cache for each core
		• 2 MB shared L3 CoreNet platform cache (1 MB per memory channel)
		Flash memory:
		• Two SPI boot flashes (2 x 2 MB) for U-Boot selectable via the DIP switch or the MMC
		• One 8 MB SPI flash for operating system use
		Mass storage device:
		• Up to 2 GB NAND flash via an integrated/embedded NAND flash controller
		• Up to 32 GB microSDHC flash via an integrated SDHC controller
		• Up to 64 GB NAND flash memory (SSD) via an optional onboard SATA Flash module
		Two serial EEPROMs with 64 kbit:
		• One for system data storage
		• One free for user data storage

Table 1-2: AM4150 Main Specifications (Continued)

AM4150		SPECIFICATIONS
AMC Interconnection	Gigabit Ethernet	Common Options Region ports 0-1: • Two Gigabit Ethernet SerDes ports (AMC port 1 switchable to front) Fat Pipes Region ports 8-10: • Up to three Gigabit Ethernet SerDes ports
	SATA	Common Options Region ports 2-3: • Up to two SATA ports
	SRIO	Fat Pipes Region ports 4-7: • One 4x Serial RapidIO interface operating in host or agent configuration, depending on configuration Fat Pipes Region ports 8-11: • One 4x Serial RapidIO interface operating in host or agent configuration, depending on configuration
	PCI Express	Fat Pipes Region ports 4-7: • One x4 PCI Express interface operating in root complex configuration Fat Pipes Region ports 8-11: • One x4 PCI Express interface operating in root complex configuration
	Debug Interface	Extended Options Region port 14: • One debug port
	Serial Interface	Extended Options Region port 15: • One serial port
	GPIO	Extended Options Region port 16: • Two general purpose inputs (GPI), on request • Two general purpose outputs (GPO), on request
	Clock	Clock: • Bidirectional PCI express reference clock (FCLKA)
Connectors	Front Panel Connectors	• Two Gigabit Ethernet ports on two RJ-45 connectors, J2 and J3 • One serial port (UART1) with RS-232 signal level on RJ-45 connector, J4
	Onboard Connectors	• Common on-chip processor (COP) debug port via 16-pin (2 x 8) pinrow 1.27 mm connector, J8
		• One extension connector, J5, for the SATA Flash module
	microSD card Socket	• Standard microSD socket, J9, accepts microSD and microSDHC cards
	AMC Card-edge Connector	• One 170-pin AMC Card-edge connector, J1
Switch	DIP Switch	One DIP switch for board configuration, SW2, consisting of four switches

Table 1-2: AM4150 Main Specifications (Continued)

AM4150		SPECIFICATIONS
LEDs	Module Management LEDs	• LED1 (red): Out-of-Service LED • LED2 (red/green/amber): Health LED • HS LED (blue): The hot swap indicator provides basic feedback to the user on the hot swap state of the module. The HS LED states are *off*, *short blink*, *long blink*, and *on*.
	User-Specific LEDs	• ULED3 (red/green): AMC port 0 link status (green) + user-specific debug code (green) + general purpose (red/green/red+green) • ULED2 (red/green): AMC port 1 link status (green) + user-specific debug code (green) + general purpose (red/green/red+green) • ULED1 (red/green): User-specific debug code (green) + general purpose (red/green/red+green) • ULED0 (red/green): User-specific debug code (green) + general purpose (red/green/red+green)
	Integral Ethernet LEDs	• Act (green): Ethernet Link/Activity • Speed (green/yellow/off): Ethernet Speed
Timer	Watchdog Timer	• Software-configurable, two-stage Watchdog with programmable timeout ranging from 125 ms to 4096 s in 16 steps • Serves for generating IRQ or hardware reset
	System Timer	There are several timers implemented in the CPU. For further information regarding these timers, refer to the CPU reference manual from Freescale.
IPMI	Module Management Controller	• NXP® ARM7 microcontroller with redundant 512 kB firmware flash and automatic roll-back strategy • The MMC carries out IPMI commands such as monitoring several onboard temperature conditions, board voltages and the power supply status, and managing hot swap operations. • The MMC is accessible via a local IPMB (IPMB-L) and one host Keyboard Controller Style Interface (KCS). • One MMC system EEPROM for FRU data and firmware private data
	Hot Swap	The AM4150 has full hot swap capability.
Thermal	Thermal Management	CPU and board overtemperature protection is provided by: • Three onboard temperature sensors for monitoring the board temperature • CPU temperature diode integrated in the QorIQ™ P5020 processor • Specially designed heat sink
General	Power Consumption	Refer to Chapter 5, “Power Considerations” for information related to the power consumption of the AM4150.
	Temperature Range	Operational: -5°C to +55°C Storage: -40°C to +70°C
	Mechanical	Single Mid-size module
	Dimensions	181.5 mm x 73.5 mm x 18.96 mm
	Board Weight	244 grams (with heat sink and front panel)

Table 1-2: AM4150 Main Specifications (Continued)

AM4150		SPECIFICATIONS
Software	Bootloader	DENX U-Boot (Universal Boot Loader) with Kontron-specific modifications to support the AM4150 requirements
	IPMI	Module Management Controller firmware providing the following features: • The MMC is accessible via IPMB-L and one KCS interface with interrupt support • The MMC firmware can be updated in the field through the KCS interface using the U-Boot bootloader and through all supported onboard interfaces using the update functions of the open-source tool “ipmitool”. For further information on the ipmitool refer to the sourceforge.net web site. • Two MMC flash images with automatic roll-back capability in case of an upgrade firmware failure • Board supervision and control extensions such as board reset, power and firmware flash control, etc.
	Operating Systems	The board is offered with various Board Support Packages including VxWorks and Linux operating systems. For further information concerning the operating systems available for the AM4150, please contact Kontron.

1.6 Standards

The AM4150 complies with the requirements of the following standards.

Table 1-3: Standards

COMPLIANCE	TYPE	STANDARD	TEST LEVEL
CE	Emission	EN55022 EN61000-6-3 EN300386	--
	Immission	EN55024 EN61000-6-2 EN300386	--
	Electrical Safety	EN60950-1	--
Mechanical	Mechanical Dimensions	IEEE 1101.10	--
Environmental and Health Aspects	Vibration (sinusoidal, operating)	GR-63-CORE EN300019-2-3 IEC61131-2 IEC60068-2-6	5-150 [Hz] frequency range 1 [g] acceleration 1 [oct/min] sweep rate 10 sweeps/axis 3 directions: x, y, z
	Shock (operating)	EN300019-2-3 IEC61131-2 IEC60068-2-27	15 [g] acceleration 11 [ms] pulse duration 3 shocks per direction 5 [s] recovery time 6 directions, ±x, ±y, ±z
	Climatic Humidity	IEC60068-2-78	93% RH at 40°C, non-condensing **(see note below)**
	WEEE	Directive 2002/96/EC	Waste electrical and electronic equipment
	RoHS	Directive 2002/95/EC	Restriction of the use of certain hazardous substances in electrical and electronic equipment

Note ...

Kontron performs comprehensive environmental testing of its products in accordance with applicable standards.

Customers desiring to perform further environmental testing of Kontron products must contact Kontron for assistance prior to performing any such testing. This is necessary, as it is possible that environmental testing can be destructive when not performed in accordance with the applicable specifications.

In particular, for example, boards **without conformal coating** must not be exposed to a change of temperature exceeding 1K/minute, averaged over a period of not more than five minutes. Otherwise, condensation may cause irreversible damage, especially when the board is powered up again.

Kontron does not accept any responsibility for damage to products resulting from destructive environmental testing.

1.7 Related Publications

The following publications contain information relating to this product.

Table 1-4: Related Publications

PRODUCT	PUBLICATION
ATCA	PICMG® 3.0 R3.0, AdvancedTCA® Base Specification, March 24, 2008
MicroTCA	PICMG® MTCA.0 R1.0, Micro Telecommunications Computing Architecture Base Specification, July 6, 2006
AMC	PICMG® AMC.0 R2.0, Advanced Mezzanine Card Base Specification, Nov. 15, 2006 PICMG® AMC.1 R2.0, PCI Express™ on AdvancedMC™, Oct. 8, 2008 PICMG® AMC.2 R1.0, Ethernet Advanced Mezzanine Card Specification, March 1, 2007 PICMG® AMC.4 R1.0, Serial RapidIO on AdvancedMC™ Specification, July 11, 2009
IPMI	IPMI - Intelligent Platform Management Interface Specification, v2.0 Document Revision 1.0, February 12, 2004 IPMI - Platform Management FRU Information Storage Definition, V1.0 Document Revision 1.1, September 27, 1999
PCI Express	PCI Express Base Specification Revision 2.0, Dec. 20, 2006
Serial RapidIO	RapidIO™ Interconnect Specification Part 6: LP-Serial Physical Layer Specification, Rev. 2.0.1, March 2008
Serial ATA	Serial ATA International Organization: Serial ATA Revision 2.6, 15th February 2007
Platform Firmware	DENX “U-Boot” (Universal Boot Loader) online documentation at www.denx.de
Kontron	Kontron’s Product Safety and Implementation Guide, ID 1021-9142
	Kontron’s AM4150 U-Boot Bootloader User Guide, ID 1052-0281
	Kontron’s AM4150 IPMI Firmware User Guide, ID 1052-5679

Chapter 2

Functional Description

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2. Functional Description

2.1 Processor

Freescale™ QorIQ™ communications platforms are the next-generation evolution of the leading PowerQUICC® communications processors. Built using high-performance Power Architecture® cores, Freescale™ QorIQ™ platforms enable a new era of networking innovation where the reliability, security and quality of service for every connection matters.

The AM4150 supports the high-performance, 64-bit, dual-core Freescale™ QorIQ™ P5020 processor with up to 2.0 GHz clock speed, two DDR3 memory controllers with ECC support, five dTSECs as well as two x4 PCI Express ports operating at up to 5.0 GT/s or two x4 sRIO ports operating with 2.5, 3.125 or 5.0 Gbaud.

The QorIQ™ P5020 processor delivers high performance at frequencies up to 2.0 GHz on a 45 nm technology platform for a wide variety of applications in the networking, telecom, military and industrial markets. The QorIQ™ P5020 cores can be combined as a fully symmetric multiprocessing system on a chip, or they can be operated with variable degrees of independence to perform asymmetric multiprocessing. A defining characteristic of the QorIQ™ P5020 processor is the ability to independently boot and reset each e5500 core.

The two high-performance, 72-bit DDR3 memory controllers provide up to 1300 MHz memory speed as well as support for error correction codes, a baseline requirement for any high-reliability system. Up to 2 GB NAND flash is supported on the AM4150 through the processor's 8-bit local bus. The three SPI flashes, two 2 MB flashes for U-Boot and one 8 MB flash for the OS, are supported through the processor's SPI controller.

The AM4150 uses various controllers integrated in the QorIQ™ P5020, such as dTSEC, eSDHC, eLBC, SPI, I²C, DUART, PCI Express®, and Serial RapidIO®. Advanced packet parsing, flow control and quality of service features are supported via these controllers.

Table 2-1: Features of the Processors Supported on the AM4150

FEATURE	QorIQ™ P5020 2.0 GHz	QorIQ™ P5020 1.6 GHz
Processor Base Frequency	2.0 GHz	1.6 GHz
L1 cache per core	64 kB	64 kB
Backside L2 cache per core	512 kB	512 kB
Shared L3 CoreNet platform cache	2 MB	2 MB
DDR3 Memory	up to 8 GB / 1300 MHz	up to 8 GB / 1200 MHz
Thermal Design Power	28 W	20.4 W
Package	FC-PBGA (1295)	FC-PBGA (1295)

2.2 Memory

The AM4150 supports a soldered, dual-channel (72-bit), Double Data Rate (DDR3) memory with Error Checking and Correcting (ECC) running at up to 1300 MHz (memory error detection and reporting of 1-bit and 2-bit errors and correction of 1-bit failures). The available memory configuration can be either 4 GB or 8 GB.

2.3 Timer

The AM4150 is equipped with the following timer:

- Real-Time Clock (RTC)

The AM4150 is equipped with an onboard high-precision real-time clock RV-8564-C2. The RV-8564-C2 RTC is register-compatible with the PCF8564A RTC from Philips/NXP. In addition, it provides a very tight frequency tolerance at low power consumption. The AM4150 does not include a 3 V lithium battery or a GoldCap power source for RTC backup.

2.4 Watchdog Timer

The AM4150 provides a Watchdog timer that is programmable for a timeout period ranging from 125 ms to 4096 s in 16 steps. Failure to trigger the Watchdog timer in time results in a system reset or an interrupt. In dual-stage mode, it results in a combination of both interrupt and reset if the Watchdog is not serviced. A hardware status flag will be provided to determine if the Watchdog timer generated the reset.

2.5 Power Monitor and Reset Generation

All onboard voltages on the AM4150 are supervised, which guarantees controlled power-up of the board. This is done by releasing the power-up reset signals after the threshold voltages have been passed.

2.6 Flash Memory

There are four flash devices available as described below, two SPI flashes for U-Boot, one NAND flash and one SPI flash for the OS.

2.6.1 SPI Flashes for U-Boot

The AM4150 provides two 2 MB SPI boot flashes for two separate U-Boot images, a standard SPI boot flash and a recovery SPI boot flash. The fail-over mechanism for the U-Boot recovery can be controlled via the MMC or the DIP switch SW2, switch 2.

If the standard SPI boot flash is corrupted, the MMC automatically enables the recovery SPI boot flash and boots the system again.

The SPI boot flashes include a hardware write protection option, which can be configured via the U-Boot. If write protection is enabled, writing to the SPI boot flashes is not possible.

Note ...

The U-Boot code and settings are stored in the SPI boot flashes. Changes made to the U-Boot settings are available only in the currently selected SPI boot flash. Thus, switching over to the other SPI boot flash may result in operation with different U-Boot code and settings.

2.6.2 NAND Flash

The AM4150 supports up to 2 GB of soldered NAND flash memory, which is an SLC-based NAND flash. It is optimized for embedded systems providing high performance, reliability and security.

2.6.3 SPI Flash for OS

The AM4150 supports 8 MB of soldered flash memory for the OS.

2.6.4 SATA Flash Module (Optional)

The AM4150 supports up to 64 GB of NAND flash memory (SSD) in combination with an optional SATA Flash module, which is connected to the onboard connector J5.

The SATA Flash module is an SLC-based SATA NAND flash drive with a built-in full hard-disk emulation and a high data transfer rate (sustained read rate with up to 100 MB/s and sustained write rate with up to 90 MB/s). It is optimized for embedded systems providing high performance, reliability and security.

Note ...

Write protection is available for this module. Please contact Kontron for further assistance if write protection is required.

2.7 System Data and User Data EEPROMs

The AM4150 provides two 64-kBit EEPROMs, one for system data storage and one which is free for user data storage. The user data EEPROM is accessible via the OS or an application. The system data EEPROM is reserved for system usage.

2.8 microSDHC Mass Storage

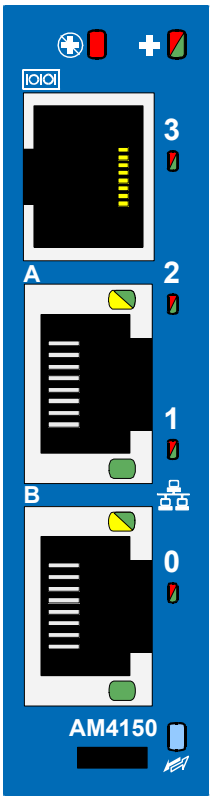
The AM4150 is provided with a microSDHC card socket, (J9), which accepts microSD and microSDHC cards up to 32 GB. If used, the card must be installed prior to installation of the AM4150 in a system.

2.9 Board Interfaces

2.9.1 Front Panel LEDs

The AM4150 is equipped with three Module Management LEDs and four User-Specific LEDs. The User-Specific LEDs can be configured via two onboard registers (see Chapter 4.4.10, “LED Configuration Register” and Chapter 4.4.11, “LED Control Register”).

Figure 2-1: Front Panel LEDs



Module Management LEDs

- LED1 (Out-of-Service LED)
- LED2 (Health LED)
- HS LED (Hot Swap LED)

User-Specific LEDs

- 3 ... 0 ULED3 ... 0

Table 2-2: Module Management LEDs Functions

LED	COLOR	STATE	NORMAL MODE	OVERRIDE MODE selectable by user or carrier, depending on PICMG LED command
LED1 (Out-of-Service LED)	red	off	Default	By user: • Only lamp test
		on	MMC out of service or in reset state	
		blinking	MMC firmware upgrade	
LED2 (Health LED)	green/ amber/ red	off	Payload is off; module is not powered	By user: • Only lamp test
		green	Module is healthy (normal operation) and all related sensors are within the specified range	
		amber	Payload is on and at least one sensor is out of range	
		red	Reserved	
HS LED (Hot Swap LED)	blue	on	a) Module ready for hot swap extraction, or b) Module has just been inserted in a powered system	By carrier: • On • Off • Slow/Fast Blinking By user: • Only lamp test
		blinking	Module hot swap in progress; module not ready for extraction	
		off	Module is in normal operation	

Note ...

For further information concerning the hot swap operation, refer to Chapter 3.3, Hot Swap Procedures.

Table 2-3: User-Specific LEDs Functions

LED	COLOR	FUNCTION DURING POWER-UP	FUNCTION IF USER-SPECIFIC DEBUG CODE ENABLED	DEFAULT FUNCTION AFTER BOOT-UP
ULED3	red	When lit up during power-up, it indicates a power failure.	—	Mode A (Gen. Purpose), Mode B or Port 80 Default: Mode B
	green	—	bit 7 and bit 3	
ULED2	red	—	—	Mode A (Gen. Purpose), Mode B or Port 80 Default: Mode B
	green	—	bit 6 and bit 2	
ULED1	red	When lit up during power-up, it indicates a hardware reset.	—	Mode A (Gen. Purpose), Mode B or Port 80 Default: Mode B
	green	—	bit 5 and bit 1	
ULED0	red	When lit up during power-up, it indicates a U-Boot boot failure	—	Mode A (Gen. Purpose), Mode B or Port 80 Default: Mode B
	green	—	bit 4 and bit 0	

How to Read the 8-Bit User-Specific Debug Code

Due to the fact that only 4 bits are available and 8 bits must be displayed, the user-specific debug code output is multiplexed on the User-Specific LEDs.

Table 2-4: User-Specific Debug Code Sequence

STATE	USER-SPECIFIC LEDs
0	All User-Specific LEDs are OFF; start of sequence
1	High nibble
2	Low nibble; state 2 is followed by state 0

The following is an example of the User-Specific LEDs' operation if the user-specific debug configuration is enabled via the LED Configuration Register (LCFG). For further information, refer to Chapter 4.4.10, LED Configuration Register.

Table 2-5: User-Specific Debug Code Example

	ULED3 BIT 7/3	ULED2 BIT 6/2	ULED1 BIT 5/1	ULED0 BIT 4/0	RESULT
HIGH NIBBLE	off (0)	on (1)	off (0)	off (0)	0x4
LOW NIBBLE	off (0)	off (0)	off (0)	on (1)	0x1
CODE					0x41

Note ...

Under normal operating conditions, the User-Specific LEDs should not remain lit during boot-up. They are intended to be used for debugging purposes. In the event that a User-Specific LED lights up during boot-up and the AM4150 does not boot, please contact Kontron for further assistance.

2.9.2 Module Handle

At the front panel, the AM4150 provides a module handle for module extraction, securing the module in the carrier/chassis and actuating the hot swap switch.

The module handle supports a three-position operation.

Figure 2-2: Module Handle Positions

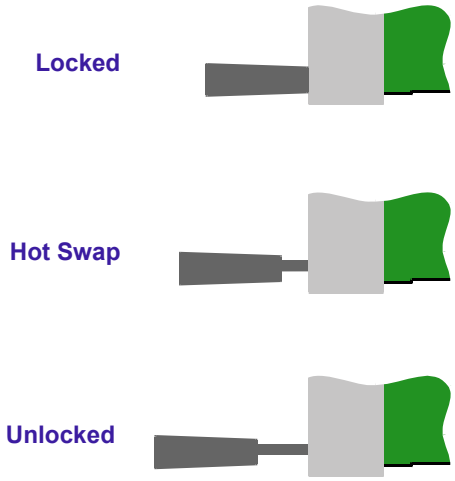


Table 2-6: Module Handle Positions

MODULE HANDLE POSITION	FUNCTION
Locked	When the AM4150 is installed, the module handle is pushed in the "Locked" position and the following actions result: • The module is locked in the carrier/chassis • The hot swap switch is actuated
Hot Swap	When an extraction process of the AM4150 is initiated, the module handle is pulled in the "Hot Swap" position and the following actions result: • The module is locked in the carrier/chassis • The hot swap switch is deactuated
Unlocked	When the module handle is pulled to the "Unlocked" position, the AM4150 can be fully extracted and the following actions result: • The module is unlocked in the carrier/chassis • The hot swap switch is deactuated

Note ...

For normal operation, the module handle must be in the "Locked" position.

2.9.3 General Purpose DIP Switch

The AM4150 is equipped with one general purpose, 4-bit DIP switch, SW2, used for board configuration.

For further information on the configuration of the DIP switch SW2, refer to Chapter 4.1, “DIP Switch Configuration”.

2.9.4 Debug Interfaces

The AM4150 provides several onboard options for hardware and software debugging, such as:

- Four bicolor user-specific LEDs for signaling hardware failures and user-specific debug code
- A COP debug connector, J8, to facilitate software debugging using an emulation probe

  The J8 connector is a 16-pin (2 x 8) pinrow connector with a 1.27 mm raster. There is an adapter available from Kontron for debug probes with 2.54 mm raster connectors.

The following figure and table provide pinout information for the J8 connector.

Figure 2-3: COP Debug Connector J8

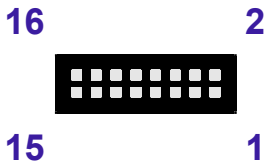


Table 2-7: COP Debug Connector J8 Pinout

FUNCTION	SIGNAL	PIN	PIN	SIGNAL	FUNCTION
–	NC	1	2	COP_TDO	JTAG data out
JTAG test reset	COP_TRST#	3	4	COP_TDI	JTAG data in
Power supply	V_3V3	5	6	NC	–
Reserved for “COP checkstop in” (not available on the CPU)	COP_CKSTP_IN#	7	8	COP_TCK	JTAG test clock
–	NC	9	10	COP_TMS	JTAG test mode select
Ground signal	GND	11	12	COP_SRST#	Reserved for “COP soft reset” (not available on the CPU)
–	NC	13	14	COP_HRST#	COP hard reset
Ground signal	GND	15	16	COP_CKSTP_OUT#	COP checkstop out

2.9.5 Serial Ports

The AM4150 provides two serial ports, UART1 and UART2, both fully compatible with the programming model of the PC16450 and the PC16550D UARTs.

The UART1 interface provides receive and transmit signals as well as additional signals for handshaking mode. UART1 is available on the front panel as a serial RS-232, 8-pin, RJ-45, connector J4. Data transfer rates up to 115.2 kB/s are supported.

The UART2 interface provides only receive and transmit signals. UART2 is available on the AMC port 15 in the Extended Options Region of the AMC Card-edge Connector as TTL 3.3 V signal level. Data transfer rates up to 115.2 kB/s are supported.

The following figure and table provide pinout information for the serial port connector J4.

Figure 2-4: Serial Con. J4 (UART1)

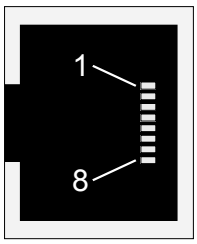


Table 2-8: Serial Con. J4 (UART1) Pinout

PIN	SIGNAL	FUNCTION	I/O
1	RTS	Request to send	O
2	Res.*	Reserved	--
3	TXD	Transmit data	O
4	GND	Signal ground	--
5	GND	Signal ground	--
6	RXD	Receive data	I
7	Res.*	Reserved	--
8	CTS	Clear to send	I

Note ...

* Pins 2 and 7 are reserved for factory purposes and must not be externally connected.

2.9.6 Serial Rapid I/O

The AM4150 provides two x4 Serial RapidIO revision 2.1 interfaces operating with up to 5.0 Gbaud. The Serial RapidIO operates as Host or Agent, provides an 8- or 16-bit system size, and can be routed to the AMC interconnection, Fat Pipes Region, ports 4-7 and 8-11.

2.9.7 Serial ATA Interface

The AM4150 provides up to two 3 Gb/s SATA interfaces, SATA A and SATA B. The SATA controllers are integrated in the QorIQ™ P5020 processor.

One SATA port is connected to the AMC port 2 in the Common Options Region of the AMC Card-edge Connector.

The other SATA port is connected to the SATA Flash module via the J5 connector. On request, the AM4150 is also provided with the second SATA port routed to the AMC port 3 in the Common Options Region of the AMC Card-edge Connector.

2.9.8 PCI Express Interfaces

The AM4150 provides two x4 PCI Express Gen 2 interfaces operating either at 5 GT/s or at 2.5 GT/s. The PCI Express interfaces operate as root complex and are routed to the AMC interconnection, Fat Pipes Region, ports 4-7 and 8-11.

2.9.9 Gigabit Ethernet Interfaces

The QorIQ™ P5020 processor integrates five enhanced triple-speed Ethernet controllers (dTSECs) distributed between two front Gigabit Ethernet interfaces and up to four AMC Gigabit Ethernet interfaces, all of them supporting 10BASE-T/100BASE-TX/1000BASE-T as well as 1000BASE-X (SerDes).

2.9.9.1 Gigabit Ethernet Port Assignment

The dTSECs are assigned both to the front I/O and to the AMC interconnection as indicated in the following table.

Table 2-9: Gigabit Ethernet Port Assignment

GIGABIT ETHERNET PORT	QorIQ™ P5020 dTSECs
Front I/O: GbE B (J2), RJ-45 copper port DTSEC4 is multiplexed between the front GbE B port (J2) and the AMC SerDes port 1 or 10. If GbE B is used, the AMC SerDes ports 1 and 10 are not available. For further information, refer to Table 2-11 and the U-Boot “sconf” command.	dTSEC4: RGMII (AMC GbE PHY)
Front I/O: RJ-45 copper port, GbE A (J3)	dTSEC3: SGMII (front GbE PHY)
AMC: SerDes port 0	dTSEC5: RGMII (AMC GbE PHY)
AMC: SerDes port 1 If dTSEC4, RGMII (AMC GbE PHY), is configured for the RJ-45 copper port GbE B (J2), it is not available for the AMC SerDes port 1.	dTSEC4: RGMII (AMC GbE PHY)
AMC: SerDes port 8	dTSEC1: GbE 1000BASE-X (AMC SerDes)
AMC: SerDes port 9	dTSEC2: GbE 1000BASE-X (AMC SerDes)
AMC: SerDes port 10 If dTSEC4, GbE 1000BASE-X (AMC SerDes), is configured for the AMC port 10, the front panel RJ-45 copper port GbE B (J2) and the AMC port 1 are not available.	dTSEC4: GbE 1000BASE-X (AMC SerDes)

2.9.9.2 Gigabit Ethernet Connectors

The Ethernet connectors, J2 (GbE B) and J3 (GbE A) are realized as RJ-45 connectors. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching is also supported (Auto-MDI/X).

Figure 2-5: GbE Con. J2/J3

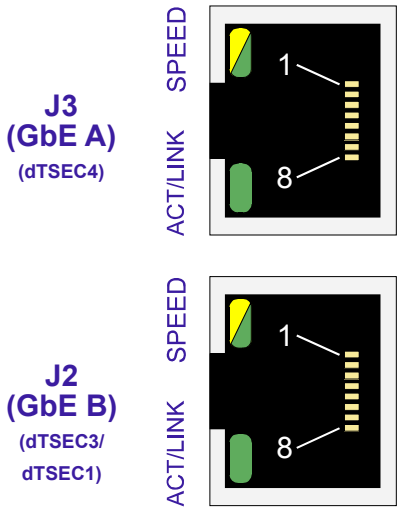


Table 2-10: GbE Connectors J2/J3 Pinout

PIN	MDI / STANDARD ETHERNET CABLE					
	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-	-	I/O	BI_DC+
5	-	-	-	-	I/O	BI_DC-
6	I	RX-	I	RX-	I/O	BI_DB-
7	-	-	-	-	I/O	BI_DD+
8	-	-	-	-	I/O	BI_DD-

Ethernet LED Status

ACT (green): This LED monitors network connection and activity. The LED lights up when a valid link (cable connection) has been established. The LED blinks when network packets are sent or received through the RJ-45 port. When this LED remains off, a valid link has not been established due to a missing or a faulty cable connection.

SPEED (green/yellow/off): This LED lights up to indicate a successful 100Base-TX or 1000BASE-T connection. When green, it indicates a 100Base-TX connection and when yellow it indicates a 1000Base-T connection. When not lit and the ACT-LED is active, the connection is operating at 10Base-T.

2.10 AMC Interconnection

The AM4150 communicates with the carrier board or the MicroTCA backplane via the AMC Card-edge connector, which is a serial interface optimized for high-speed interconnects. The AMC Card-edge connector supports a variety of fabric topologies divided into five functional groups:

- Fabric interface
- Synchronization clock interface
- System management interface
- JTAG interface
- Module power interface

The following sections provide detailed information on these interfaces.

2.10.1 Fabric Interface

The fabric interface is the real communication path and comprises 20 high-speed ports providing point-to-point connectivity for module-to-carrier and module-to-module implementations. The high-speed ports are separated in three logical regions as follows:

- Common Options Region
  - Ports 0-1: Up to two Gigabit Ethernet SerDes ports
  - Ports 2-3: Up to two SATA ports
- Fat Pipes Region
  - Ports 4-7: One x4 Serial RapidIO (host/agent) or one x4 PCI Express interface (root complex)
  - Ports 8-11: One x4 Serial RapidIO (host/agent) or one x4 PCI Express interface (root complex) or up to three Gigabit Ethernet SerDes interfaces
- Extended Options Region
  - Port 14: One debug port
  - Port 15: One serial port
  - Port 16: Two GPIs, two GPOs (all four on request)

Figure 2-6: AM4150 Port Mapping

	Port No.	AMC Standard Port Mapping	AM4150 Port Mapping
Basic Connector	TCLKA	Clocks	System Tick (on request)
	TCLKB		not used
	FCLKA		PCIe Reference Clock (bidirectional)
	0	Common Options Region	GbE SerDes
	1		GbE SerDes (switchable to front I/O)
	2		SATA
	3		SATA (optional)
	4	Fat Pipes Region	PCIe x4 or SRIO x4
	5		
	6		
	7		
Extended Connector	8	Fat Pipes Region	PCIe x4 or SRIO x4 or up to 3 x GbE SerDes
	9		
	10		
	11		
	12	Extended Options Region	not used
	13		not used
	14		Debug
	15		Serial
	TCLKC/D		2 x GPIs & 2 x GPOs (all on request)
	17		not used
	18		not used
	19		not used
	20		not used

2.10.2 Synchronization Clock Interface

On the AM4150, three PCI Express reference clock configurations are supported in accordance with the PCI Express Base Specification Revision 2.0 as follows:

1) AM4150 uses the PCI Express reference clock from AMC Card-edge connector (FCLKA)
2) AM4150 uses the local PCI Express reference clock and the AMC clock (FCLKA) is disabled.
3) AM4150 uses the local PCI Express reference clock and AM4150 generates PCI Express reference clock to the AMC Card-edge connector (FCLKA).

The PCI Express reference clock (FCLKA) configurations can be viewed in the U-Boot via the “sconf info” command. The reference clock is configured normally by the MMC (IPMI E-Keying). However, if necessary, it may be configured using the U-Boot “sconf” command. For further information, refer to the AM4150 U-Boot Bootloader User Guide.

Note ...

The PCI Express reference clock (FCLKA) configurations 1) and 3) mentioned above are applicable only when the CPU SerDes bank 1 uses 100 MHz clock supply. The AM4150 also provides configurations where the CPU SerDes bank 1 requires 125 MHz clock supply instead of 100 MHz. In such configurations, the AM4150 does not provide a clock signal on FCLKA.

The following table indicates all available interface configurations for the AMC ports 4-7 and 8-11 including the dedicated CPU SerDes clock supplies and the onboard SerDes multiplexer settings for the AMC ports 8-11.

Table 2-11: CPU SerDes Interface Configuration

SETTING	PROTOCOL USED ON		CPU SerDes Bank 1	CPU SerDes Banks 2 & 3	SerDes MUX Ports 8-11 connected to	U-BOOT "sconf" BASE CONFIG.
	Ports 4-7	Ports 8-11				
1	PCIe2 (2.5 GT/s)	PCIe1 (2.5 GT/s)	100 MHz	125 MHz	CPU SerDes Bank 1	3
2	PCIe2 (5 GT/s)	PCIe1 (2.5 GT/s)	100 MHz	125 MHz	CPU SerDes Bank 1	
3	PCIe2 (2.5 GT/s)	PCIe1 (5 GT/s)	100 MHz	125 MHz	CPU SerDes Bank 1	
4	PCIe2 (5 GT/s)	PCIe1 (5 GT/s)	100 MHz	125 MHz	CPU SerDes Bank 1	
5	SRIO1 (2.5 Gbaud)	SRIO2 (2.5 Gbaud)	100 MHz	125 MHz	CPU SerDes Bank 1	0
6	SRIO1 (5 Gbaud)	SRIO2 (2.5 Gbaud)	100 MHz	125 MHz	CPU SerDes Bank 1	
7	SRIO1 (2.5 Gbaud)	SRIO2 (5 Gbaud)	100 MHz	125 MHz	CPU SerDes Bank 1	
8	SRIO1 (5 Gbaud)	SRIO2 (5 Gbaud)	100 MHz	125 MHz	CPU SerDes Bank 1	
9	PCIe2 (2.5 GT/s)	2x SGMII (AMC ports 8-9)	100 MHz	125 MHz	CPU SerDes Bank 2	4
10	PCIe2 (5 GT/s)	2x SGMII (AMC ports 8-9)	100 MHz	125 MHz	CPU SerDes Bank 2	
11	SRIO1 (3.125 Gbaud)	SRIO2 (3.125 Gbaud)	125 MHz	100 MHz	CPU SerDes Bank 1	1
12	SRIO1 (3.125 Gbaud)	2x SGMII (AMC ports 8-9)	125 MHz	100 MHz	CPU SerDes Bank 2	2
13	SRIO1 (2.5 Gbaud)	2x SGMII (AMC ports 8-9)	100 MHz	125 MHz	CPU SerDes Bank 2	
14	SRIO1 (5 Gbaud)	2x SGMII (AMC ports 8-9)	100 MHz	125 MHz	CPU SerDes Bank 2	
15	PCIe2 (2.5 GT/s)	PCIe3 (2.5 GT/s) (AMC port 8) / up to 2x GbE SerDes (AMC ports 9-10)	100 MHz	100 MHz	CPU SerDes Bank 2	5
16	PCIe2 (5 GT/s)	PCIe3 (2.5 GT/s) (AMC port 8) / up to 2x GbE SerDes (AMC ports 9-10)	100 MHz	100 MHz	CPU SerDes Bank 2	

2.10.3 AMC Ports 4 - 7 SerDes Lane Assignment

The following table indicates the SerDes bank/lane/signal assignment of the AMC ports 4 - 7 for connecting an external SRIO or PCI Express device to the AM4150.

Table 2-12: AMC Ports 4 - 7 SerDes Bank/Lane/Signal Assignment

AMC PORT	SRIO1 CONTROLLER LANE	PCI EXPRESS 2 CONTROLLER LANE	CPU LANE
4	0	3	CPU SerDes Bank 1, lane H
5	1	2	CPU SerDes Bank 1, lane G
6	2	1	CPU SerDes Bank 1, lane F
7	3	0	CPU SerDes Bank 1, lane E

Note ...

As indicated in the table above, the PCI Express lanes are reversed on the CPU SerDes bank 1. In general, the PCI Express hardware layer supports automatic lane reversal. In standard MicroTCA systems, x4 PCI Express devices can be used on the AM4150 with no restrictions. To use x8 PCI Express devices with the AM4150, a special backplane is required.

For further information on the CPU SerDes interface configuration, please refer to Table 2-11.

2.10.4 AMC Ports 8 - 11 SerDes Lane Assignment

The following table indicates the SerDes bank/lane/signal assignment of the AMC ports 8 - 11 for connecting an external SRIO/PCI Express/Gigabit Ethernet SerDes device to the AM4150.

Table 2-13: AMC Ports 8 - 11 SerDes Bank/Lane/Signal Assignment

AMC PORT	SRIO2 CONTR. LANE	PCI EXPRESS CONTR. LANE	SGMII CONTR. LANE	CPU LANE
8	0	3 (PCIe 1)	--	CPU SerDes Bank 1, lane D
9	1	2 (PCIe 1)	--	CPU SerDes Bank 1, lane C
10	2	1 (PCIe 1)	--	CPU SerDes Bank 1, lane B
11	3	0 (PCIe 1)	--	CPU SerDes Bank 1, lane A
8	--	--	dTSEC 1 or PCIe3	CPU SerDes Bank 2, lane A
9	--	--	dTSEC 2	CPU SerDes Bank 2, lane B
10	--	--	dTSEC 4	CPU SerDes Bank 2, lane D
11	--	--	--	--

Note ...

As indicated in the table above, the PCI Express lanes are reversed on the CPU SerDes bank 1. In general, the PCI Express hardware layer supports automatic lane reversal. In standard MicroTCA systems, x4 PCI Express devices can be used on the AM4150 with no restrictions. For information on the use of x8 PCI Express endpoint devices with the AM4150, please contact Kontron.

For further information on the CPU SerDes interface configuration, please refer to Table 2-11.

2.10.5 System Management Interface

The system management interface is a port from the module to the carrier via the Local Intelligent Platform Management Bus (IPMB-L). The Module Management Controller uses this port for the communication with the carrier Intelligent Platform Management Controller (IPMC). The IPMB-L is a multi-master I²C bus.

2.10.6 JTAG Interface

JTAG support is provided on the AMC Card-edge connector. The JTAG interface is used for vendor product test and logic update.

On the AM4150, the FPGA JTAG port is connected to the AMC JTAG port.

2.10.7 Module Power Interface

The module power interface provides the management power (MP) and payload power (PWR). These two supply voltages have power-good indicators so that the system management can detect boot sequence events and nominal operating conditions.

The AM4150 operates with payload power in the range of 12 V ± 10%, and with management power of 3.3 V ± 5%.

The board supports removal and insertion in a managed slot as required by the AMC.0 specification.

2.10.8 Pinout of AMC Card-edge Connector J1

The AMC Card-edge connector is a high-speed serial interface with 170 pins. The following table provides the pinout of the AMC Card-edge connector J1. The shaded table cells indicate signals that are not used on the AM4150.

Table 2-14: Pinout of AMC Card-edge Connector J1

BASIC SIDE (COMPONENT SIDE 1)				EXTENDED SIDE (COMPONENT SIDE 2)			
PIN	SIGNAL	FUNCTION	DRIVEN BY	PIN	SIGNAL	FUNCTION	DRIVEN BY
1	GND	Logic Ground	-	170	GND	Logic Ground	-
2	PWR	Payload Power	Carrier	169	TDI	JTAG Test Data Input	Carrier
3	PS1#	Presence 1	AMC	168	TDO	JTAG Test Data Output	AMC
4	MP	Management Power	Carrier	167	TRST#	JTAG Test Reset Input	Carrier
5	GA0	Geographic Address 0	Carrier	166	TMS	JTAG Test Mode Select In	Carrier
6	RSV	Reserved (PCIe Reset Output on request)	AMC	165	TCK	JTAG Test Clock Input	Carrier
7	GND	Logic Ground	-	164	GND	Logic Ground	-
8	RSV	Reserved (System Write Protection on request)	-	163	Tx20+	Not Connected	-
9	PWR	Payload Power	Carrier	162	Tx20-	Not Connected	-
10	GND	Logic Ground	-	161	GND	Logic Ground	-
11	Tx0+	GbE-A Transmitter + (dTSEC 5)	AMC	160	Rx20+	Not Connected	-
12	Tx0-	GbE-A Transmitter - (dTSEC 5)	AMC	159	Rx20-	Not Connected	-
13	GND	Logic Ground	-	158	GND	Logic Ground	-
14	Rx0+	GbE-A Receiver + (dTSEC 5)	Carrier	157	Tx19+	Not Connected	-
15	Rx0-	GbE-A Receiver - (dTSEC 5)	Carrier	156	Tx19-	Not Connected	-
16	GND	Logic Ground	-	155	GND	Logic Ground	-
17	GA1	Geographic Address 1	Carrier	154	Rx19+	Not Connected	-
18	PWR	Payload Power	Carrier	153	Rx19-	Not Connected	-
19	GND	Logic Ground	-	152	GND	Logic Ground	-
20	Tx1+	GbE-B Transmitter + (dTSEC 4)	AMC	151	Tx18+	Not Connected	-
21	Tx1-	GbE-B Transmitter - (dTSEC 4)	AMC	150	Tx18-	Not Connected	-
22	GND	Logic Ground	-	149	GND	Logic Ground	-

Table 2-14: Pinout of AMC Card-edge Connector J1 (Continued)

BASIC SIDE (COMPONENT SIDE 1)				EXTENDED SIDE (COMPONENT SIDE 2)			
PIN	SIGNAL	FUNCTION	DRIVEN BY	PIN	SIGNAL	FUNCTION	DRIVEN BY
23	Rx1+	GbE-B Receiver + (dTSEC 4)	Carrier	148	Rx18+	Not Connected	-
24	Rx1-	GbE-B Receiver - (dTSEC 4)	Carrier	147	Rx18-	Not Connected	-
25	GND	Logic Ground	-	146	GND	Logic Ground	-
26	GA2	Geographic Address 2	Carrier	145	Tx17+	Not Connected	-
27	PWR	Payload Power	Carrier	144	Tx17-	Not Connected	-
28	GND	Logic Ground	-	143	GND	Logic Ground	-
29	Tx2+	SATA1 Transmitter +	AMC	142	Rx17+	Not Connected	-
30	Tx2-	SATA1 Transmitter -	AMC	141	Rx17-	Not Connected	-
31	GND	Logic Ground	-	140	GND	Logic Ground	-
32	Rx2+	SATA1 Receiver +	Carrier	139	Tx16+	Reserved (GPO1 on req.)	AMC
33	Rx2-	SATA1 Receiver -	Carrier	138	Tx16-	Reserved (GPO2 on req.)	AMC
34	GND	Logic Ground	-	137	GND	Logic Ground	-
35	Tx3+	Not Connected / SATA2 Transmitter +	AMC	136	Rx16+	Reserved (GPI1 on req.)	Carrier
36	Tx3-	Not Connected / SATA2 Transmitter -	AMC	135	Rx16-	Reserved (GPI2 on req.)	Carrier
37	GND	Logic Ground	-	134	GND	Logic Ground	-
38	Rx3+	Not Connected / SATA2 Receiver +	Carrier	133	Tx15+	Serial Port Transmit	AMC
39	Rx3-	Not Connected / SATA2 Receiver -	Carrier	132	Tx15-	Serial Port Receive	Carrier
40	GND	Logic Ground	-	131	GND	Logic Ground	-
41	ENABLE#	AMC Enable	Carrier	130	Rx15+	Not Connected	-
42	PWR	Payload Power	Carrier	129	Rx15-	Not Connected	-
43	GND	Logic Ground	-	128	GND	Logic Ground	-
44	Tx4+	PCIe-3 Transmitter + sRIO-0 Transmitter +	AMC	127	Tx14+	Debug serial data output	AMC
45	Tx4-	PCIe-3 Transmitter - sRIO-0 Transmitter -	AMC	126	Tx14-	Debug serial clock output	AMC
46	GND	Logic Ground	-	125	GND	Logic Ground	-
47	Rx4+	PCIe-3 Receiver + sRIO-0 Receiver +	Carrier	124	Rx14+	Reserved for EMI2_MDIO_1V2	AMC/ Carrier

Table 2-14: Pinout of AMC Card-edge Connector J1 (Continued)

BASIC SIDE (COMPONENT SIDE 1)				EXTENDED SIDE (COMPONENT SIDE 2)			
PIN	SIGNAL	FUNCTION	DRIVEN BY	PIN	SIGNAL	FUNCTION	DRIVEN BY
48	Rx4- Rx4+	PCIe-3 Receiver - sRIO-0 Receiver -	Carrier	123	Rx14- Rx14+	Reserved for EMI2_MDC_1V2	AMC
49	GND	Logic Ground	-	122	GND	Logic Ground	-
50	Tx5+ Tx5-	PCIe-2 Transmitter + sRIO-1 Transmitter +	AMC	121	Tx13+ Tx13-	Not Connected	-
51	Tx5- Tx5+	PCIe-2 Transmitter - sRIO-1 Transmitter -	AMC	120	Tx13- Tx13+	Not Connected	-
52	GND	Logic Ground	-	119	GND	Logic Ground	-
53	Rx5+ Rx5-	PCIe-2 Receiver + sRIO-1 Receiver +	Carrier	118	Rx13+ Rx13-	Not Connected	-
54	Rx5- Rx5+	PCIe-2 Receiver - sRIO-1 Receiver -	Carrier	117	Rx13- Rx13+	Not Connected	-
55	GND	Logic Ground	-	116	GND	Logic Ground	-
56	SCL_L	IPMB-L Clock	IPMI Agent	115	Tx12+ Tx12-	Not Connected	-
57	PWR	Payload Power	Carrier	114	Tx12- Tx12+	Not Connected	-
58	GND	Logic Ground	-	113	GND	Logic Ground	-
59	Tx6+ Tx6-	PCIe-1 Transmitter + sRIO-2 Transmitter +	AMC	112	Rx12+ Rx12-	Not Connected	-
60	Tx6- Tx6+	PCIe-2 Transmitter - sRIO-2 Transmitter -	AMC	111	Rx12- Rx12+	Not Connected	-
61	GND	Logic Ground	-	110	GND	Logic Ground	-
62	Rx6+ Rx6-	PCIe-2 Receiver + sRIO-2 Receiver +	Carrier	109	Tx11+ Tx11-	PCIe-0 Transmitter + sRIO-3 Transmitter +	AMC
63	Rx6- Rx6+	PCIe-2 Receiver - sRIO-2 Receiver -	Carrier	108	Tx11- Tx11+	PCIe-0 Transmitter - sRIO-3 Transmitter -	AMC
64	GND	Logic Ground	-	107	GND	Logic Ground	-
65	Tx7+ Tx7-	PCIe-0 Transmitter + sRIO-3 Transmitter +	AMC	106	Rx11+ Rx11-	PCIe-0 Receiver + sRIO-3 Receiver +	Carrier
66	Tx7- Tx7+	PCIe-0 Transmitter - sRIO-3 Transmitter -	AMC	105	Rx11- Rx11+	PCIe-0 Receiver - sRIO-3 Receiver -	Carrier
67	GND	Logic Ground	-	104	GND	Logic Ground	-
68	Rx7+ Rx7-	PCIe-0 Receiver + sRIO-3 Receiver +	Carrier	103	Tx10+ Tx10-	PCIe-1 Transmitter + sRIO-2 Transmitter + GbE SerDes Transmitter + (dTSEC 4)	AMC

Table 2-14: Pinout of AMC Card-edge Connector J1 (Continued)

BASIC SIDE (COMPONENT SIDE 1)				EXTENDED SIDE (COMPONENT SIDE 2)			
PIN	SIGNAL	FUNCTION	DRIVEN BY	PIN	SIGNAL	FUNCTION	DRIVEN BY
69	Rx7-	PCIe-0 Receiver - sRIO-3 Receiver -	Carrier	102	Tx10-	PCIe-1 Transmitter - sRIO-2 Transmitter - GbE SerDes Transmitter - (dTSEC 4)	AMC
70	GND	Logic Ground	-	101	GND	Logic Ground	-
71	SDA_L	IPMB-L Data	IPMI Agent	100	Rx10+	PCIe-1 Receiver + sRIO-2 Receiver + GbE SerDes Receiver + (dTSEC 4)	Carrier
72	PWR	Payload Power	Carrier	99	Rx10-	PCIe-1 Receiver - sRIO-2 Receiver - GbE SerDes Receiver - (dTSEC 4)	Carrier
73	GND	Logic Ground	-	98	GND	Logic Ground	-
74	TCLKA+	Reserved (Telecom Clock A+ on req.)	Carrier	97	Tx9+	PCIe-2 Transmitter + sRIO-1 Transmitter + GbE SerDes Transmitter + (dTSEC 2)	AMC
75	TCLKA-	Reserved (Telecom Clock A- on req.)	Carrier	96	Tx9-	PCIe-2 Transmitter - sRIO-1 Transmitter - GbE SerDes Transmitter - (dTSEC 2)	AMC
76	GND	Logic Ground	-	95	GND	Logic Ground	-
77	TCLKB+	Not Connected	AMC	94	Rx9+	PCIe-2 Receiver + sRIO-1 Receiver + GbE SerDes Receiver + (dTSEC 2)	Carrier
78	TCLKB-	Not Connected	AMC	93	Rx9-	PCIe-2 Receiver - sRIO-1 Receiver - GbE SerDes Receiver - (dTSEC 2)	Carrier
79	GND	Logic Ground	-	92	GND	Logic Ground	-
80	FCLKA+	PCIe Reference Clock +	Carrier	91	Tx8+	PCIe-3 Transmitter + (PCIe-0 Transmitter + for “sconf” base config. 5) sRIO-0 Transmitter + GbE SerDes Transmitter + (dTSEC 1)	AMC

Table 2-14: Pinout of AMC Card-edge Connector J1 (Continued)

BASIC SIDE (COMPONENT SIDE 1)				EXTENDED SIDE (COMPONENT SIDE 2)			
PIN	SIGNAL	FUNCTION	DRIVEN BY	PIN	SIGNAL	FUNCTION	DRIVEN BY
81	FCLKA-	PCIe Reference Clock -	Carrier	90	Tx8-	PCIe-3 Transmitter - (PCIe-0 Transmitter - for "sconf" base config. 5) sRIO-0 Transmitter - GbE SerDes Transmitter - (dTSEC 1)	AMC
82	GND	Logic Ground	-	89	GND	Logic Ground	-
83	PS0#	Presence 0	Carrier	88	Rx8+	PCIe-3 Receiver + (PCIe-0 Receiver + for "sconf" base config. 5) sRIO-0 Receiver + GbE SerDes Receiver + (dTSEC 1)	Carrier
84	PWR	Payload Power	Carrier	87	Rx8-	PCIe-3 Receiver - (PCIe-0 Receiver - for "sconf" base config. 5) sRIO-0 Receiver - GbE SerDes Receiver - (dTSEC 1)	Carrier
85	GND	Logic Ground	-	86	GND	Logic Ground	-

Warning!

When handling the board, take care not to touch the gold conductive fingers of the AMC Card-edge connector.

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

The following table lists the pins reserved for specific user purposes such PCI Express reset, global system write protection and Ethernet management interface.

Table 2-15: Reserved Pins Description

AMC PIN	AMC PORT	FUNCTION	I/O	SIGNALING VOLTAGE
6	--	Optional PCI Express reset output	O	3.3 V TTL level
8	--	Global system write protection	I	3.3 V TTL level
123	14	Reserved for EMI2_MDC_1V2	O	1.2 V level
124	14	Reserved for EMI2_MDIO_1V2	I/O	1.2 V level

Warning!

The pins listed above are reserved for optional use and must not be connected to circuitry with the wrong voltage or signal direction.

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

The following table lists the Extended Options Region pins with no differential signals.

Table 2-16: Extended Options Region Single-Ended Pins Description

AMC PIN	AMC PORT	FUNCTION	I/O	SIGNALING VOLTAGE
133	15	Tx serial port (UART2)	O	3.3V TTL level
132	15	Rx serial port (UART2)	I	3.3V TTL level
127	14	Debug serial data output	O	3.3V TTL level
126	14	Debug serial clock output	O	3.3V TTL level

Note ...

The Extended Options Region pins listed above do not have differential signals. They have 3.3V TTL signaling voltage.

The following table lists the JTAG pins used for programming the onboard logic.

Table 2-17: JTAG Pins Description

AMC PIN	SIGNAL	FUNCTION	I/O	SIGNALING VOLTAGE
169	TDI	JTAG Test Data Input	I	3.3V TTL level
168	TDO	JTAG Test Data Output	O	3.3V TTL level
167	TRST#	JTAG Test Reset Input	I	3.3V TTL level
166	TMS	JTAG Test Mode Select In	I	3.3V TTL level
165	TCK	JTAG Test Clock Input	I	3.3V TTL level

Note ...

The JTAG pins are connected to the onboard FPGA logic and can be used to programming the onboard logic. For further information, please contact Kontron.

2.11 Module Management

A dedicated Module Management Controller (MMC) on the AM4150 manages the module and supports a defined subset of IPMI commands and sensors. For information on IPMI, refer to the IPMI Firmware User Guide for the AM4150 Module.

2.11.1 Module Management Controller

The Module Management Controller is based on the NXP® ARM7 microcontroller and provides a dual 512 kB flash implementation with automatic roll-back strategy to the back-up copy, for example, if a firmware upgrade is interrupted or corrupted.

In addition, there is an MMC system EEPROM available for firmware private data and FRU data. Access to this EEPROM is only possible via IPMI commands.

The host processor communicates with the MMC via the Keyboard Controller Style (KCS) interface. The MMC is able to communicate directly with the FPGA via the I²C interface.

The MMC is used to manage the AM4150. For example, it monitors several onboard temperature conditions, board voltages and the power supply status, manages LEDs and operations, reboots the board, etc. Additionally, the MMC can intervene in the operating status of the system by reading temperature values, shutting down systems and generating alarm signals if fault conditions occur.

The MMC provides an IPMI watchdog in compliance with the AMC specification. The watchdog can be used to reset or power cycle the payload CPU. This enhances the board's characteristics and improves the system's reliability.

The MMC firmware is designed and specially made for AMC environments, and is compliant with the PICMG 3.0 and IPMI v2.0 rev 1.0 specifications.

2.11.2 MMC Signals Implemented on the AM4150

The MMC implements several signals to monitor and control the different board functions. The following tables indicate the signals implemented on the AM4150.

Table 2-18: Processor and Chipset Supervision

SIGNAL	DESCRIPTION	MMC FUNCTION
Board reset	Resets the complete board	Control reset circuit
Cold reset	Resets all host registers and the complete board	Control reset circuit
ASLEEP	Status of CPU sleep state	Monitor sleep state
SPI flash control	Control of fail-over mechanism for SPI U-Boot flashes	Control SPI flashes

Table 2-19: AMC-Specific Signals

SIGNAL	DESCRIPTION	MMC FUNCTION
GA[0:2]	Geographic address	Monitor
Hot swap LED	Hot swap LED	Control LED
Hot swap switch	Status of hot swap switch	Monitor hot swap switch
Out-of-Service LED	Out-of-Service LED	Control LED
Health LED	Health LED	Control LED

Table 2-20: Onboard Power Supply Supervision

SIGNAL	DESCRIPTION	MMC FUNCTION
AMC power enable	Control AMC board supply	Control power supply
Onboard power supply	Status of various onboard supply voltages	Monitor power good signals
Voltage 3.3 V	Board 3.3 V supply	Monitor voltage
Voltage 5 V	Board 5 V supply	Monitor voltage
Voltage AMC 3.3 V	AMC management power 3.3 V	Monitor voltage
Voltage AMC 12 V	AMC payload power 12 V	Monitor voltage

Table 2-21: Temperature Signals

SIGNAL	DESCRIPTION	MMC FUNCTION
Board temperature top side	Board temperature between QorIQ™ P5020 and DDR3 memory	Monitor temperature
Board temperature bottom side	Board temperature between QorIQ™ P5020 and DDR3 memory	Monitor temperature
Temperature of the air temperature sensor	Air temperature sensor near the AMC Card-edge connector	Monitor temperature
QorIQ™ P5020 CPU temperature diode	Temperature measurement by using the CPU-internal temperature diode	Monitor temperature

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Chapter 3

Installation

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3. Installation

The AM4150 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

3.1 Safety Requirements

The following safety precautions must be observed when installing or operating the AM4150. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

Warning!

AMC modules require, by design, a considerable amount of force in order to (dis)engage the module from/in the AMC carrier/backplane connector. For this reason, when inserting or extracting the module, apply only as much force as required to preclude damage to either the module's handle or the front panel.

DO NOT push on the module handle to seat the module in the carrier/backplane connector. Do not use the module handle as a grip to handle the board outside of the carrier or chassis slot.

Use of excessive force, bending or rotation of the module handle will result in damage to the handle or the module's locking mechanism. Kontron disclaims all liability for damage to the module or the system as a result of failure to comply with this warning.

ESD Equipment!

This AMC module contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

Warning!

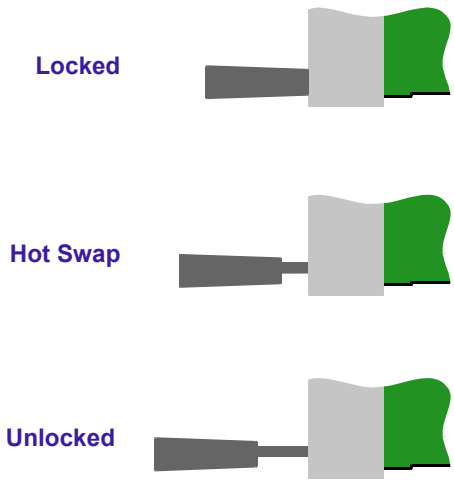
This product has gold conductive fingers which are susceptible to contamination. Take care not to touch the gold conductive fingers of the AMC Card-edge connector when handling the board.

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

3.2 Module Handle Positions

The module handle supports a three-position operation.

Figure 3-1: Module Handle Positions



Note ...

For normal operation, the module handle must be in the “Locked” position.

3.3 Hot Swap Procedures

The AM4150 is designed for hot swap operation. Hot swapping allows the coordinated insertion and extraction of modules without disrupting other operational elements within the system.

The procedures contained in this section are also applicable for “non-operating systems” with the exception of indications and functions which require power to be applied.

3.3.1 Hot Swap Insertion

To insert the AMC module proceed as follows:

1. Ensure that the safety requirements indicated section 3.1 are observed.

Warning!

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

2. Ensure that the module is properly configured for operation in accordance with the application requirements before installation. For information regarding the configuration of the AM4150 refer to Chapter 4.

Warning!

Care must be taken when applying the procedures below to ensure that neither the AM4150 nor other system boards are physically damaged by the application of these procedures.

3. Ensure that the module handle is in the “Unlocked” position.
4. Using the front panel as a grip, carefully insert the module into the slot designated by the application requirements until it makes contact with the carrier/backplane connector.
5. Apply pressure to the front panel until the module is properly seated in the carrier/backplane connector. This may require a considerable amount of force. Apply pressure only to the front panel, not the module handle. During seating in the connector, there is a noticeable “snapping” of the board into the connector. When the board is seated it should be flush with the carrier or system front panel.

   In the case of a running system, the following occurs:

   - The BLUE HS LED turns on.

     When the module is seated, the module management power is applied and the BLUE HS LED turns on. (No payload power is applied at this time).
6. Connect all external interfacing cables to the module as required and ensure that they are properly secured.
7. Push the module handle in the “Locked” position.

   When the module handle is in the “Locked” position, the module is locked and the hot swap switch is actuated.

In the case of a running system, the following occurs:

- The BLUE HS LED displays long blinks.

  When the carrier IPMI controller detects the module, it sends a command to the module to perform long blinks of the BLUE HS LED.

- The BLUE HS LED turns off.

  The Intelligent Platform Management Controller on the carrier reads the Module Current Requirements record and the AMC Point-to-Point Connectivity record.

  If the module FRU information is valid and the carrier can provide the necessary payload power, the BLUE HS LED will be turned off.

  The carrier now enables the payload power for the module.

Note ...

If the module FRU information is invalid or the carrier cannot provide the necessary payload power, the BLUE HS LED stops blinking and remains lit. Should this problem occur, please contact Kontron.

8. The AMC module is now ready for operation.

   For operation of the AM4150, refer to appropriate AM4150-specific software, application, and system documentation.

3.3.2 Hot Swap Extraction

To extract the AMC module proceed as follows:

1. Ensure that the safety requirements indicated in section 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!
2. Pull the module handle in the “Hot Swap” position.

   When the module handle is in the “Hot Swap” position, the extraction process of the module is initiated and the following occurs:

   - The BLUE HS LED displays short blinks.

     When the carrier/chassis IPMI controller receives the handle opened event, it sends a command to the MMC with a request to perform short blinks of the BLUE HS LED. This indicates that the module is waiting to be deactivated.

     Now the module waits for a permission from the higher level management (Shelf Manager or System Manager) to proceed with its deactivation.

     Once the module receives the permission to continue the deactivation, all used ports are disabled.

   - The BLUE HS LED turns on.

     The Intelligent Platform Management Controller on the carrier/chassis disables the module's payload power and the BLUE HS LED is turned on.

     Now the module is ready to be safely extracted.
3. Pull the module handle in the “Unlocked” position.
3. Disconnect any interfacing cables that may be connected to the module.
4. Disengage the module from the carrier/backplane connector by pulling on the module handle. This may require a considerable amount of force.

Warning!

Due care should be exercised when handling the module due to the fact that the heat sink can get very hot. Do not touch the heat sink when removing the module.

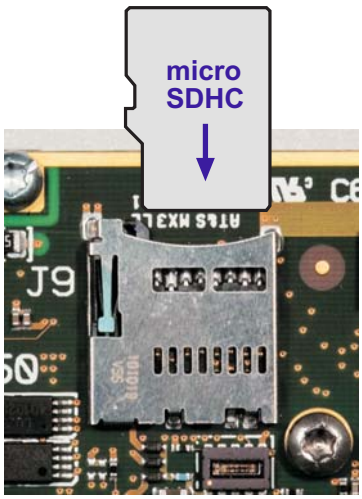
5. Using the front panel as a grip, remove the module from the carrier/chassis.
6. Dispose of the module as required.

3.4 Installation of a microSDHC Memory Card

The AM4150 supports microSD and microSDHC memory cards. The J9 microSDHC card socket is suitable for use with both card types. The AM4150 supports 1- or 4-bit SD mode and a data transfer of up to 200 Mbps in the 4-bit SD mode.

The figure below shows the orientation of the microSDHC memory card for insertion in the J9 socket.

Figure 3-2: J9 microSDHC Memory Card Socket



The microSDHC memory card must be installed prior to installation of the AM4150 in a system.

To install a microSDHC memory card, orient the card as shown above, insert it into the socket and then push it all the way into the socket. When properly installed, the card is latched in the socket.

To remove, push the card in until it is unlatched, then release the card (the card is forcibly ejected by a spring). Once unlatched and ejected, the card can be removed completely.

3.5 Installation of a SATA Flash Module

A SATA Flash module with up to 64 GB SATA NAND flash memory may be connected to the AM4150 via the onboard connector J5.

This optionally available module must be physically installed on the AM4150 prior to installation of the AM4150 in a system.

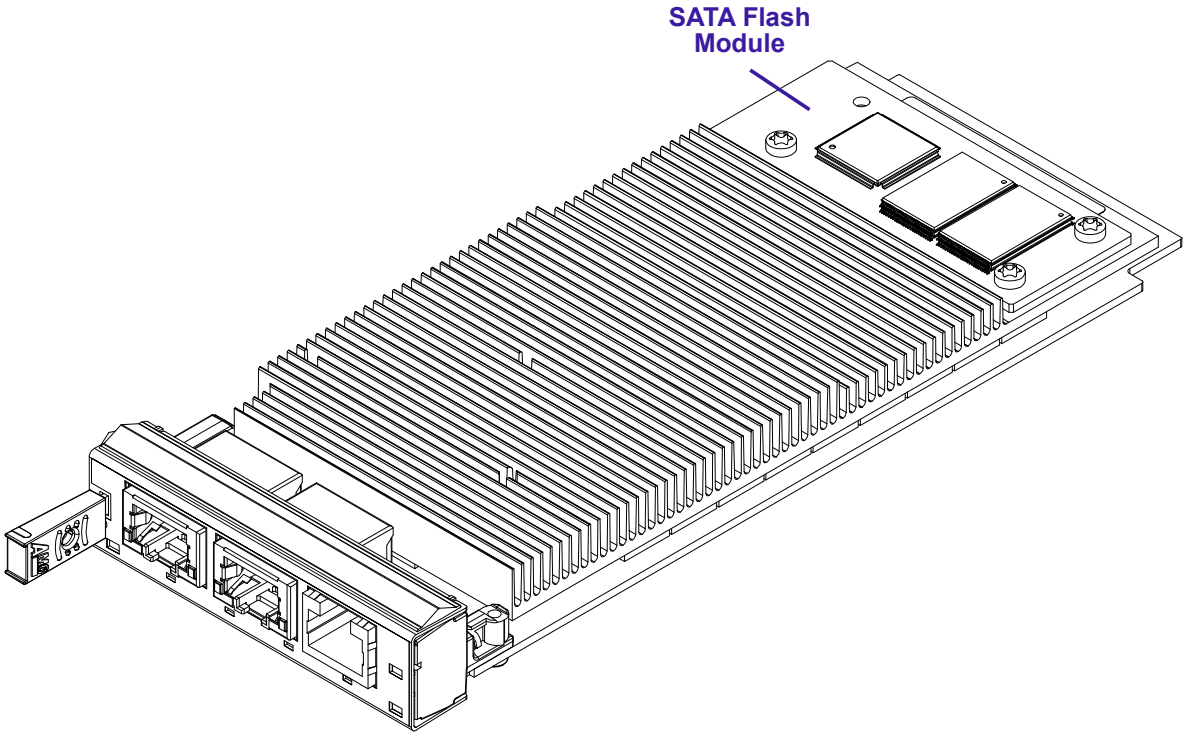
During installation it is necessary to ensure that the SATA Flash module is properly seated in the onboard connector J5, i.e. the pins are aligned correctly and not bent, prior to fixing the SATA Flash module with the respective screw.

Note ...

Only qualified SATA Flash modules from Kontron are authorized for use with the AM4150. Failure to comply with the above will void the warranty and may result in damage to the board or the system.

The following figure shows the placement of the SATA Flash module on the AM4150.

Figure 3-3: Placement of the SATA Flash Module



3.6 Software Installation

For information on software installation, please refer to the respective BSP manual.

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Chapter 4

Configuration

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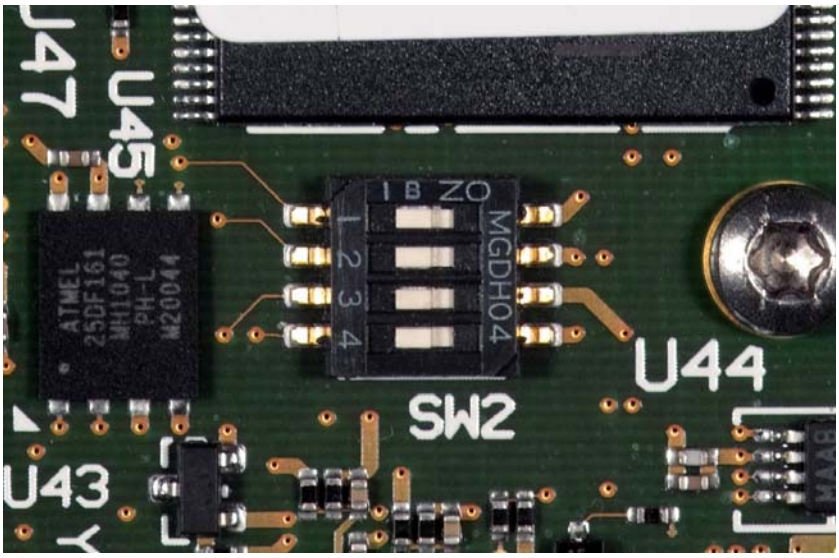
4. Configuration

4.1 DIP Switch Configuration

The AM4150 is equipped with one 4-bit DIP switch, SW2, used for board configuration.

Figure 4-1: DIP Switch SW2



The following tables indicate the functions of the switches integrated in the DIP switch SW2.

Table 4-1: DIP Switch SW2 Configuration

SWITCH	SETTING	DESCRIPTION
1	***OFF***	***Use AMC fabric port assignment configured in the MMC and indicated in the E-Keying data*** This configuration can be changed via the U-Boot “sconf” command.
	ON	Load and work with fail-safe AMC fabric configuration For further information on the fail-safe AMC fabric configuration refer to Table 4-2.
2	***OFF***	***Boot from the standard SPI boot flash***
	ON	Boot from the recovery SPI boot flash
3	***OFF***	Reserved
	ON	
4	***OFF***	Reserved
	ON	

The default setting is indicated by using italic bold.

Note ...

If the DIP switch SW2, switch 2, is set to ON, the SPI boot flash selection cannot be overwritten by the MMC.

Table 4-2: Fail-Safe AMC Fabric Configuration

FUNCTION	CONFIGURATION OF DIP SWITCH SW2, SWITCH 1 (ON)
Ports 4 - 7 Fabric Type	Off
Ports 4 - 7 Fabric Mode	Host/Root Complex
Ports 8 - 11 Fabric Type	Off
Ports 8 - 11 Fabric Type	Host/Root Complex
SRIO 4 - 7 System Size	8-bit
SRIO 4 - 7 Speed	3.125 Gbps
SRIO 8 - 11 System Size	8-bit
SRIO 8 - 11 Speed	3.125 Gbps
FCLK	FCLK only onboard generated and used

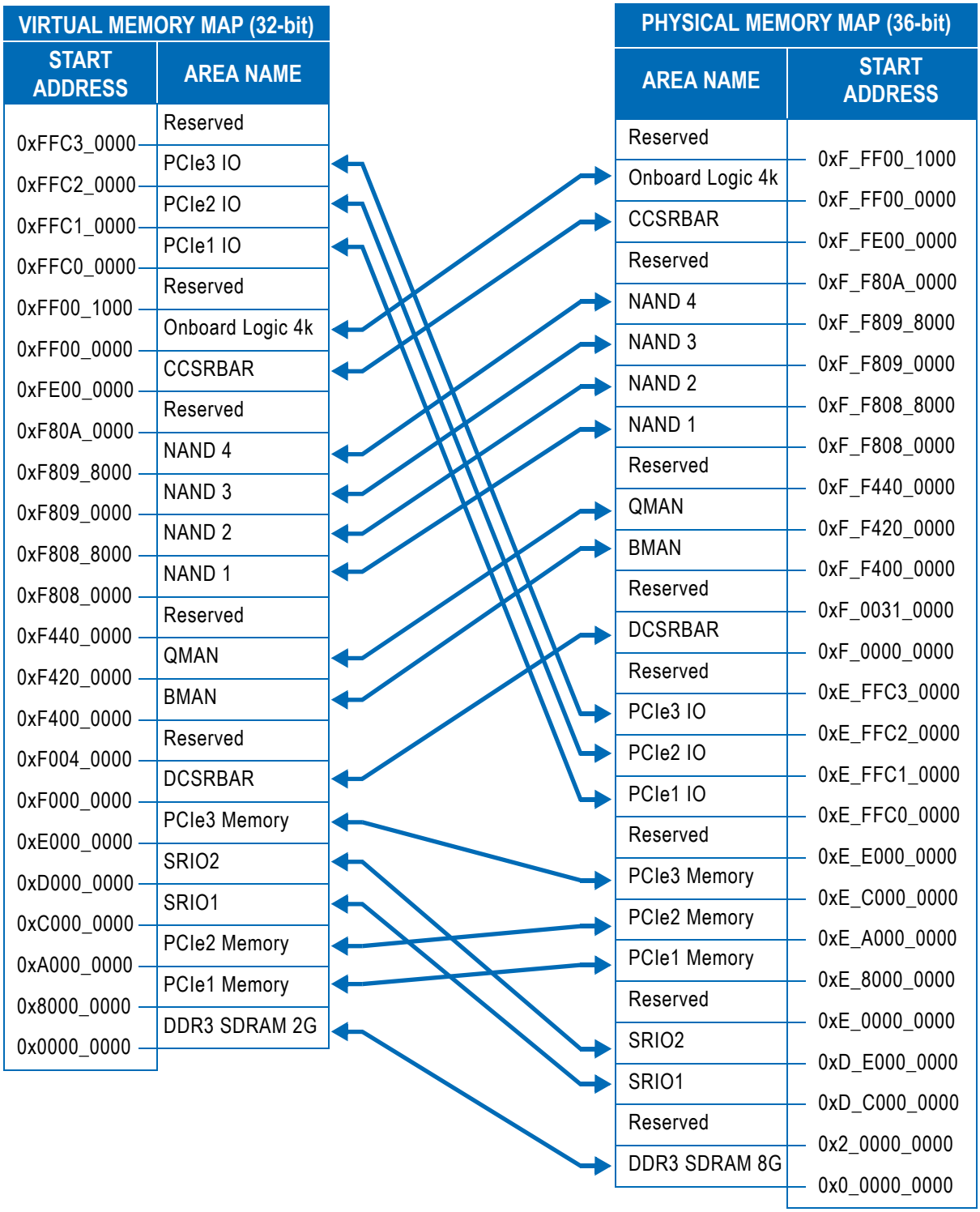
Note ...

In the Fail-Safe AMC fabric configuration, both front panel Gigabit Ethernet ports are available.

4.2 Memory Address Mapping

The following table indicates both the virtual and physical memory address map of the AM4150.

Table 4-3: AM4150 Virtual and Physical Memory Address Map



4.3 I/O Address Map

The following table sets out the AM4150-specific I/O registers.

Table 4-4: I/O Address Map

ADDRESS OFFSET	DEVICE
0x080	Debug Code Low Byte Register (POSTL)
0x081	Debug Code High Byte Register (POSTH)
0x082 - 0x085	Reserved
0x280	Status Register 0 (STAT0)
0x281 - 0x283	Reserved
0x284	Device Protection Register (DPROT)
0x285	Reset Status Register (RSTAT)
0x286	Board Interrupt Configuration Register (BICFG)
0x287	Reserved
0x288	Board ID High Byte Register (BIDH)
0x289	Board and PLD Revision Register (BREV)
0x28A	Geographic Addressing Register (GEOAD)
0x28B	Reserved
0x28C	Watchdog Timer Control Register (WTIM)
0x28D	Board ID Low Byte Register (BIDL)
0x28E - 0x28F	Reserved
0x290	LED Configuration Register (LCFG)
0x291	LED Control Register (LCTRL)
0x292 - 0x29F	Reserved
0xCA2; 0xCA3	MMC KCS interface

For the AM4150, the register address is composed of the base address of the Onboard Logic 4k indicated in the virtual memory map (see Table 4-3) and the respective address offset indicated in the I/O address map (Table 4-4):

register address = 0xFF00_0000 base + address offset.

For example, the register address of the Control Register 1 (CTRL1) is 0xFF00_0283 and consists of the base address 0xFF00_0000 and the address offset for the Control Register 1 0x283.

4.4 AM4150 Specific Registers

The following registers are special registers which the AM4150 uses to watch the onboard hardware special features and the AMC control signals.

Note ...

Take care when modifying the contents of these registers as the system may be relying on the state of the bits under its control.

4.4.1 Status Register 0 (STAT0)

The Status Register 0 holds general onboard and AMC control signals.

Table 4-5: Status Register 0 (STAT0)

REGISTER NAME		STATUS REGISTER 0 (STAT0)		
ADDRESS		0xFF00_0000 base + 0x280 offset = 0xFF00_0280		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	Res.	Reserved	0	R
6	BBEI	U-Boot boot end indication: 0 = U-Boot is booting 1 = U-Boot boot is finished	0	R/W
5 - 4	BFSS	SPI boot flash selection status: 00 = Standard SPI boot flash active 01 = Recovery SPI boot flash active 10 = External SPI boot flash active 11 = Reserved	N/A	R
3	DIP4	DIP switch SW2, switch 4 (Reserved): 0 = Off 1 = On	N/A	R
2	DIP3	DIP switch SW2, switch 3 (Reserved): 0 = Off 1 = On	N/A	R
1	DIP2	DIP switch SW2, switch 2 (Selection of boot flash): 0 = Off 1 = On	N/A	R
0	DIP1	DIP switch SW2, switch 1 (Selection of default configuration): 0 = Off 1 = On	N/A	R

Note ...

The BBEI bit can be set only once. It is cleared by a reset and cannot be cleared via software.

4.4.2 Device Protection Register (DPROT)

The Device Protection Register holds the write protect signals for non-volatile memory devices.

Table 4-6: Device Protection Register (DPROT)

REGISTER NAME		DEVICE PROTECTION REGISTER (DPROT)		
ADDRESS		0xFF00_0000 base + 0x284 offset = 0xFF00_0284		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	SWP	System write protection: 0 = Onboard non-volatile memory devices not write protected 1 = Onboard non-volatile memory devices write protected This bit reflects the state of the system hardware write protection signal (SYS_WP#).	0	R
6	Res.	Reserved	0	R
5	SDWP	microSD/microSDHC module write protection: 0 = Module not write protected 1 = Module write protected	0	R/W
4	NFWP	SPI flash for OS write protection: 0 = Flash not write protected 1 = Flash write protected	0	R/W
3	SEWP	SPD (Serial Presence Detect) EEPROM write protection: 0 = SPD EEPROM not write protected 1 = SPD EEPROM write protected	1	R/W
2	SFWP	SATA Flash module write protection: 0 = SATA Flash module not write protected 1 = SATA Flash module write protected	0	R/W
1	EEWP	System EEPROM write protection: 0 = System EEPROM not write protected 1 = System EEPROM write protected	1	R/W
0	BFWP	Write protection for the standard and recovery SPI boot flashes: 0 = Flashes not write protected 1 = Flashes write protected	0	R/W

4.4.3 Reset Status Register (RSTAT)

The Reset Status Register is used to determine the reset source.

Table 4-7: Reset Status Register (RSTAT)

REGISTER NAME		RESET STATUS REGISTER (RSTAT)		
ADDRESS		0xFF00_0000 base + 0x285 offset = 0xFF00_0285		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	PORS	Power-on reset status: 0 = System reset generated by software (warm reset) 1 = System reset generated by power-on (cold reset) Writing a '1' to this bit clears the bit.	1	R/W
6	Res.	Reserved	0	R
5	SRST	Software reset status: 0 = Reset is logged by MMC 1 = Reset is not logged by MMC The U-Boot/software sets the bit to inform the MMC that the next reset should not be logged. Writing a '1' from the host to this bit sets the bit. After this bit has been set, it may be cleared via the MMC.	0	R/W
4	Res.	Reserved	0	R
3	IPRS	MMC-controlled reset: 0 = System reset not generated by MMC 1 = System reset generated by MMC Writing a '1' to this bit clears the bit.	0	R/W
2 - 1	Res.	Reserved	00	R
0	WTRS	Watchdog timer reset status: 0 = System reset not generated by Watchdog timer 1 = System reset generated by Watchdog timer Writing a '1' to this bit clears the bit.	0	R/W

Note ...

The Reset Status Register is set to the default values by power-on reset, not by a warm reset.

4.4.4 Board Interrupt Configuration Register (BICFG)

The Board Interrupt Configuration Register holds a series of bits defining the interrupt routing for the Watchdog, the UART controller, and the MMC.

Table 4-8: Board Interrupt Configuration Register (BICFG)

REGISTER NAME		BOARD INTERRUPT CONFIGURATION REGISTER (BICFG)		
ADDRESS		0xFF00_0000 base + 0x286 offset = 0xFF00_0286		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 4	Res.	Reserved	0000	R
3 - 2	KCICF	MMC KCS interrupt configuration: 00 = Disabled 01 = IRQ11 10 = IRQ10 11 = Reserved	01	R/W
1 - 0	WICF	Watchdog interrupt configuration: 00 = Disabled 01 = IRQ9 10 = IRQ10 11 = Reserved	01	R/W

4.4.5 Board ID High Byte Register (BIDH)

Each Kontron board is provided with a unique 16-bit board-type identifier in the form of a hexadecimal number. The Board ID High Byte Register is located in the address 0x288. The Board ID Low Byte Register is located in the address 0x28D.

Table 4-9: Board ID High Byte Register (BIDH)

REGISTER NAME		BOARD ID HIGH BYTE REGISTER (BIDH)		
ADDRESS		0xFF00_0000 base + 0x288 offset = 0xFF00_0288		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 0	BIDH	Board identification: 0xD0C0 = AM4150	0xD0	R

4.4.6 Board and PLD Revision Register (BREV)

The Board and PLD Revision Register signals to the software when differences in the board and the Programmable Logic Device (PLD) require different handling by the software. It starts with the value 0x00 for the initial board prototypes and will be incremented with each change in hardware as development continues.

Table 4-10: Board and PLD Revision Register (BREV)

REGISTER NAME		BOARD AND PLD REVISION REGISTER (BREV)		
ADDRESS		0xFF00_0000 base + 0x289 offset = 0xFF00_0289		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 4	BREV	Board revision	N/A	R
3 - 0	PREV	PLD revision	N/A	R

4.4.7 Geographic Addressing Register (GEOAD)

This register holds the AMC geographic address (site number) used to assign the Intelligent Platform Management Bus (IPMB) address to the AM4150.

Table 4-11: Geographic Addressing Register (GEOAD)

REGISTER NAME		GEOGRAPHIC ADDRESSING REGISTER (GEOAD)		
ADDRESS		0xFF00_0000 base + 0x28A offset = 0xFF00_028A		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 5	Res.	Reserved	000	R
4 - 0	GA	AMC geographic address	N/A	R

Note ...

The AMC geographic addressing register is set to the default values by power-on reset, not by a warm reset.

4.4.8 Watchdog Timer Control Register (WTIM)

The AM4150 has one Watchdog timer provided with a programmable timeout ranging from 125 msec to 4096 sec. Failure to strobe the Watchdog timer within a set time period results in a system reset or an interrupt. The interrupt mode can be configured via the Board Interrupt Configuration Register (0xFF00_0x286).

There are four possible modes of operation involving the Watchdog timer:

- Timer only mode
- Reset mode
- Interrupt mode
- Dual stage mode

At power on the Watchdog is not enabled. If not required, it is not necessary to enable it. If required, the bits of the Watchdog Timer Control Register must be set according to the application requirements. To operate the Watchdog, the mode and time period required must first be set and then the Watchdog enabled. Once enabled, the Watchdog can only be disabled or the mode changed by powering down and then up again. To prevent a Watchdog timeout, the Watchdog must be retriggered before timing out. This is done by writing a ‘1’ to the WTR bit. In the event a Watchdog timeout does occur, the WTE bit is set to ‘1’. What transpires after this depends on the mode selected.

The four operational Watchdog timer modes can be configured by the WMD[1:0] bits, and are described as follows:

Timer only mode - In this mode the Watchdog is enabled using the required timeout period. Normally, the Watchdog is retriggered by writing a ‘1’ to the WTR bit. In the event a timeout occurs, the WTE bit is set to ‘1’. This bit can then be polled by the application and handled accordingly. To continue using the Watchdog, write a ‘1’ to the WTE bit, and then retrigger the Watchdog using WTR. The WTE bit retains its setting as long as no power down-up is done. Therefore, this bit may be used to verify the status of the Watchdog.

Reset mode - This mode is used to force a hard reset in the event of a Watchdog timeout. In addition, the WTE bit is not reset by the hard reset, which makes it available if necessary to determine the status of the Watchdog prior to the reset.

Interrupt mode - This mode causes the generation of an interrupt in the event of a Watchdog timeout. The interrupt handling is a function of the application. If required, the WTE bit can be used to determine if a Watchdog timeout has occurred.

Dual stage mode - This is a complex mode where in the event of a timeout two things occur: 1) an interrupt is generated, and 2) the Watchdog is retriggered automatically. In the event a second timeout occurs following the first timeout, a hard reset will be generated. The second timeout period is the same as the first. If the Watchdog is retriggered normally as specified above, operation continues. The interrupt generated at the first timeout is available to the application to handle the first timeout if required. As with all of the other modes, the WTE bit is available for application use.

Table 4-12: Watchdog Timer Control Register (WTIM)

REGISTER NAME		WATCHDOG TIMER CONTROL REGISTER (WTIM)		
ADDRESS		0xFF00_0000 base + 0x28C offset = 0xFF00_028C		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	WTE	Watchdog timer expired status bit 0 = Watchdog timer has not expired 1 = Watchdog timer has expired. Writing a '1' to this bit resets it to 0.	0	R/W
6 - 5	WMD	Watchdog mode 00 = Timer only mode 01 = Reset mode 10 = Interrupt mode 11 = Cascaded mode (dual-stage mode)	00	R/W
4	WEN/WTR	Watchdog enable / Watchdog trigger control bit: 0 = Watchdog timer not enabled Prior to the Watchdog being enabled, this bit is known as WEN. After the Watchdog is enabled, it is known as WTR. Once the Watchdog timer has been enabled, this bit cannot be reset to 0. As long as the Watchdog timer is enabled, it will indicate a '1'. 1 = Watchdog timer enabled Writing a '1' to this bit causes the Watchdog to be retriggered to the timer value indicated by bits WTM[3:0].	0	R/W
3 - 0	WTM	Watchdog timeout settings: 0000 = 0.125 s 0001 = 0.25 s 0010 = 0.5 s 0011 = 1 s 0100 = 2 s 0101 = 4 s 0110 = 8 s 0111 = 16 s 1000 = 32 s 1001 = 64 s 1010 = 128 s 1011 = 256 s 1100 = 512 s 1101 = 1024 s 1110 = 2048 s 1111 = 4096 s	0000	R/W

4.4.9 Board ID Low Byte Register (BIDL)

Each Kontron board is provided with a unique 16-bit board-type identifier in the form of a hexadecimal number. The Board ID Low Byte Register is located in the address 0x28D. The Board ID High Byte Register is located in the address 0x288.

Table 4-13: Board ID Low Byte Register (BIDL)

REGISTER NAME		BOARD ID LOW BYTE REGISTER (BIDL)		
ADDRESS		0xFF00_0000 base + 0x28D offset = 0xFF00_028D		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 0	BIDL	Board identification: 0xD0C0 = AM4150	0xC0	R

4.4.10 LED Configuration Register (LCFG)

The LED Configuration Register holds a series of bits defining the onboard configuration of the front panel User-Specific LEDs.

Table 4-14: LED Configuration Register (LCFG)

REGISTER NAME		LED CONFIGURATION REGISTER (LCFG)		
ADDRESS		0xFF00_0000 base + 0x290 offset = 0xFF00_0290		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 4	Res.	Reserved	0000	R
3 - 0	LCON	User-Specific LED Configuration 0000 = Debug [1)] 0001 = Mode A [2)] 0010 = Mode B [3)] (default) 0011 - 1111 = Reserved	0010	R/W

Regardless of the selected configuration, the User-Specific LEDs are used to signal a number of fatal onboard hardware errors, such as:

ULED3: Power failure (red)
ULED2: Reserved
ULED1: Hardware reset (red)
ULED0: U-Boot boot failure (red)

[1)] In Debug mode, the User-Specific LEDs build a binary vector to display an 8-bit value which has been written by the user in register 0x080. In doing so, the higher 4-bit nibble of the 8-bit output code is displayed followed by the lower nibble followed by a pause.

ULED3: User-Specific LED 3: bit 7 and bit 3 (green)
ULED2: User-Specific LED 2: bit 6 and bit 2 (green)
ULED1: User-Specific LED 1: bit 5 and bit 1 (green)
ULED0: User-Specific LED 0: bit 4 and bit 0 (green)

For further information on reading the 8-bit output Code, refer to Chapter 2.9.1, “Front Panel LEDs”.

[2)] Configured for Mode A, the User-Specific LEDs are dedicated to functions as follows:

ULED3: User-Specific LED 3 controlled by host (red/green/red+green)
ULED2: User-Specific LED 2 controlled by host (red/green/red+green)
ULED1: User-Specific LED 1 controlled by host (red/green/red+green)
ULED0: User-Specific LED 0 controlled by host (red/green/red+green)

[3)] Configured for Mode B, the User-Specific LEDs are dedicated to functions as follows:

ULED3: Ethernet Link Status of Gigabit Ethernet on AMC port 0 (green)
ULED2: Ethernet Link Status of Gigabit Ethernet on AMC port 1 (green)
ULED1: Reserved
ULED0: Reserved

4.4.11 LED Control Register (LCTRL)

The LED Control Register is used to switch on and off the front panel User-Specific LEDs.

Table 4-15: LED Control Register (LCTRL)

REGISTER NAME		LED CONTROL REGISTER (LCTRL)		
ADDRESS		0xFF00_0000 base + 0x291 offset = 0xFF00_0291		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 4	ULCMD	User-Specific LED command: 0000 = Get User-Specific LED 0 0001 = Get User-Specific LED 1 0010 = Get User-Specific LED 2 0011 = Get User-Specific LED 3 0100 - 0111 = Reserved 1000 = Set User-Specific LED 0 1001 = Set User-Specific LED 1 1010 = Set User-Specific LED 2 1011 = Set User-Specific LED 3 1100 - 1111 = Reserved	0000	R/W
3 - 0	ULCOL	User-Specific LED color: 0000 = Off 0001 = Green 0010 = Red 0011 = Red+green 0100 - 1111 = Reserved	0000	R/W

Note ...

This register can only be used if the User-Specific LEDs indicated in the “User-Specific LED Configuration Register” (Table 4-14) are configured in Mode A.

4.4.12 MMC Keyboard Controller Style Interface

The host processor communicates with the MMC using one Keyboard Controller Style interface, which is defined in the IPMI specification. The KCS interface has the addresses 0xFF00_0CA2 and 0xFF00_0CA3.

Chapter 5

Power Considerations

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5. Power Considerations

5.1 AM4150 Voltage Ranges

The AM4150 board has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The AM4150 requires two power sources, the module management power for the MMC (nominal: 3.3V DC) and a single payload power (nominal: 12V DC) for the module components.

The following table specifies the ranges for the different input power voltages within which the board is functional. The AM4150 is not guaranteed to function if the board is not operated within the operating range.

Table 5-1: DC Operational Input Voltage Ranges

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE	OPERATING RANGE
Payload Power (nominal: 12V DC)	10.0 V min. to 14.0 V max.	10.8 V min. to 13.2 V max.
Module Management Power (nominal: 3.3V DC)	3.0 V min. to 3.6 V. max. (±10%)	3.135 V min. to 3.465 V max. (±5%)

Warning!

The AM4150 must not be operated beyond the absolute range indicated in the table above. Failure to comply with the above may result in damage to the board.

5.2 Carrier Power Requirements

5.2.1 Payload Power

Payload power is the power provided to the module from the carrier or the backplane for the main function of the module. The payload power voltage should be selected at the higher end of the specified voltage range. The maximum continuous current limit value is based on the AMC module's power limit of 80 W. At the minimum supply voltage of 10.8 V, the 80 W requires approximately 7.4 A.

The payload power voltage shall be at least 10.8 V and not more than 13.2 V at the module contacts during normal conditions under all loads (see Table 5-1, “DC Operational Input Voltage Ranges”). The bandwidth-limited periodic noise due to switching power supplies or any other source shall not exceed 200 mV peak to peak.

5.2.2 Payload and MMC Voltage Ramp

Power supplies must comply with the following guidelines in order to be used with the AM4150:

- Beginning at 10% of the nominal output voltage, the voltage must rise within > 0.1 ms to < 20 ms to the specified regulation range of the voltage. Typically: > 5 ms to < 15 ms.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.

The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal Vout.

5.2.3 Module Management Power

The module management power is used only for the Module Management Controller (MMC), which has a very low power consumption. The management power voltage measured on the AMC at the connector shall be 3.3 V ± 5% and the maximum current is 150 mA (see Table 5-1, “DC Operational Input Voltage Ranges”).

5.2.4 Power Sequencing for Unmanaged Systems

The AM4150 configures itself for unmanaged mode if the payload power (PWR) ramps in the same time frame as the module management power (MP).

To ensure that unmanaged mode is entered the payload power (PWR) should not ramp up later than 100 ms after the management power (MP) is stable and MMC is running.

If payload power (PWR) ramps up later than 500 ms after the management power (MP) the board is configured in managed mode.

5.3 Payload Power Consumption of the AM4150

The goal of this description is to provide a method to calculate the payload power consumption for the AM4150 board with different configurations and applications. The processor and the memory dissipate the majority of the payload power.

The payload power consumption tables below list the voltage and power specifications for the AM4150 board using the Freescale™ QorIQ™ P5020 processor in different speed grades. The values were measured using an AMC carrier with two power supplies, one for the AM4150 payload and the other for the carrier, fan and management power.

The software used were U-Boot and Linux. All measurements were conducted at a temperature of 22°C with a nominal payload power of 12 V and with one COM port connected.

The following AMC fabric interfaces were active during the measurements:

- AMC Common Options Region, ports 0-1
- U-Boot “sconf” base configuration 0:
  - SRIO1 enabled, AMC ports 4-7 (no external SRIO device connected)
  - SRIO2 enabled, AMC ports 8-11 (no external SRIO device connected)

The module management power is below 0.45 W and it has therefore not been taken into considerations during the measurements.

The measured values varied, because the power consumption was dependent on the processor activity.

Note ...

The power consumption values indicated in the tables below can vary depending on the ambient temperature or the system workload. This can result in deviations of the power consumption values of up to 25%.

The payload power consumption was measured using the following processors:

- Freescale™ QorIQ™ P5020 processor, 2.0 GHz
- Freescale™ QorIQ™ P5020 processor, 1.8 GHz
- Freescale™ QorIQ™ P5020 processor, 1.6 GHz

with the following software and under the following testing conditions:

- AM4150 in U-Boot shell mode
- AM4150 with Linux, IDLE Mode
- AM4150 with Linux “stress” load tool

The following tables indicate the payload power consumption of the AM4150 with 4 or 8 GB DDR3 SDRAM and with ECC and memory cache line interleave enabled. The measurements were made with the AM4150 in U-Boot mode as well as with the Linux operating system, 32-bit.

Table 5-2: AM4150 in U-Boot Shell Mode

NOMINAL VOLTAGE	P5020 2.0 GHz	P5020 1.8 GHz	P5020 1.6 GHz
12 V	24 W	23 W	22 W

Table 5-3: AM4150 with Linux in Idle Mode

NOMINAL VOLTAGE	P5020 2.0 GHz	P5020 1.8 GHz	P5020 1.6 GHz
12 V	23.5 W	22.5 W	21.5 W

Table 5-4: AM4150 with Linux and Maximum Processor Work Load (“stress” tool)

NOMINAL VOLTAGE	P5020 2.0 GHz	P5020 1.8 GHz	P5020 1.6 GHz
12 V	29 W	27.5 W	26 W

5.4 Payload Power Consumption of AM4150 Accessories

The following table indicates the payload power consumption of AM4150 accessories.

Table 5-5: Payload Power Consumption of AM4150 Accessories

MODULE	PAYLOAD POWER
microSD / microSDHC card	approx. 0.1 W
Gigabit Ethernet port connected on the front panel (per interface)	approx. 1.0 W

5.5 IPMI FRU Payload Power Consumption

The following table indicates the IPMI FRU payload power consumption.

Table 5-6: IPMI FRU Payload Power Consumption

AM4150 with P5020 2.0 GHz	AM4150 with P5020 1.8 GHz	AM4150 with P5020 1.6 GHz
39 W	34 W	33 W

Chapter 6

Thermal Considerations

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6. Thermal Considerations

This chapter provides system integrators with the necessary information to satisfy thermal and airflow requirements when implementing AM4150 applications. To ensure optimal operation and long-term reliability of the AM4150, all onboard components must remain within the maximum temperature specifications. The most critical components on the AM4150 are the processor and the memory. Operating the AM4150 above the maximum operating limits will result in permanent damage to the board. To ensure functionality at the maximum temperature, the Module Management Controller supports several temperature monitoring and control features.

6.1 Board Thermal Monitoring

The AM4150 includes three onboard temperature sensors accessible via the Module Management Controller for monitoring the board and inlet area temperatures. For the location of the temperature sensors, refer to Figure 1-4, AM4150 Board Layout (Top View) and Figure 1-4, AM4150 Board Layout (Bottom View).

6.2 Processor Thermal Monitoring

To allow optimal operation and long-term reliability of the AM4150, the Freescale™ QorIQ™ P5020 processor must remain within the maximum die temperature specification. The maximum die temperature for the processor is 105°C.

The Freescale™ QorIQ™ P5020 processor provides a temperature diode to detect excessive temperature conditions of the processor die. The processor die temperature can be read out via the Module Management Controller.

Note ...

The processor does not provide any active means of temperature regulation. It only makes the die temperature available to the Module Management Controller. Temperature regulation is provided via IPMI and/or adequate airflow in accordance with the operating limits indicated in this chapter.

6.3 System Airflow

The AM4150 is equipped with a specifically designed heat sink to ensure the best possible basis for operational stability and long-term reliability. Coupled together with system chassis, which provide variable configurations for forced airflow, controlled active thermal energy dissipation is guaranteed.

The physical size, shape, and construction of the heat sink ensures the lowest possible thermal resistance. In addition, it has been specifically designed to efficiently support forced airflow concepts as found in modern AMC carriers and MicroTCA systems.

When developing applications using the AM4150, the system integrator must be aware of the overall system thermal requirements. The MicroTCA systems must satisfy these thermal requirements.

Thermal Characteristic Diagrams

The thermal characteristic diagrams shown in the following sections illustrate the maximum ambient air temperature as a function of the volumetric flow rate for the power consumption indicated. The diagrams are intended to serve as guidance for reconciling board and system with the required computing power considering the thermal aspect. One diagram per processor version is provided. When operating the AM4150 below the corresponding curve within the recommended operating range, the processor runs steadily and in the safe operating area. When operated above the corresponding curve, the processor must be immediately protected from thermal destruction by the chassis thermal management and returned to the safe operating area.

A flow rate of 20 cfm is a typical value for a standard *Kontron* MicroTCA system. For other systems the available flow rate will differ. The maximum ambient operating temperature must be recalculated and/or measured for such environments. For the calculation of the maximum ambient operating temperature, the processor junction temperature must never exceed the specified limit for the involved processor.

How to read the diagram

Select a specific processor and choose a specific working point within the recommended operating range. For a given flow rate there is a maximum airflow input temperature (= ambient temperature) provided. Below this operating point, safe operation is guaranteed. Above this operating point, the chassis thermal management must immediately become active and take the necessary steps to protect the processor from thermal destruction. The minimum flow rate provided must not be less than the value specified in the diagram.

Volumetric flow rate

The volumetric flow rate refers to an airflow through a fixed cross-sectional area (i.e. slot width x depth. The volumetric flow rate is specified in m³/s (cubic-meter-per-second) or cfm (cubic-feet-per-minute) respectively.

Conversion: 1 cfm = 0.00047 m³/s; 1 m³/s = 2118.9 cfm

The following figures illustrate the operational limits of the AM4150 taking into consideration power consumption vs. ambient air temperature vs. flow rate.

Note ...

The maximum airflow input temperature was measured at the bottom of the AMC module just before the air flowed over the board.

Warning!

Operating the AM4150 above the operating limits may result in damage to the board or the system and will void the warranty.

Figure 6-1: Operating Limits of the AM4150 with QorIQ™ P5020, 2.0 GHz

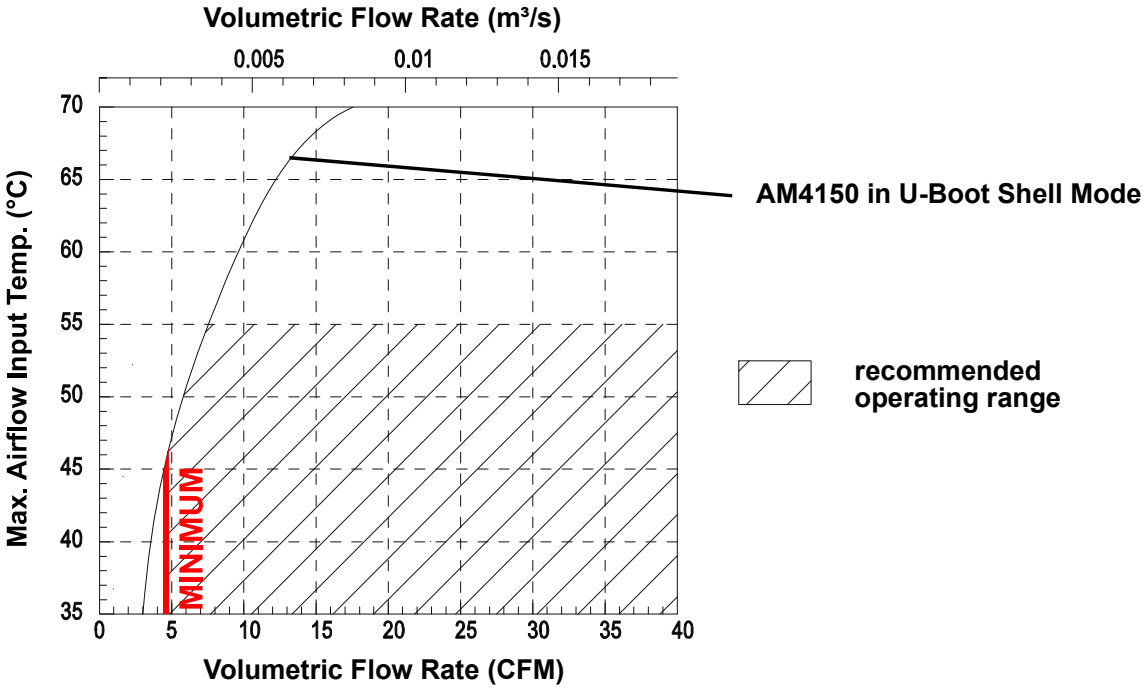


Figure 6-2: Operating Limits of the AM4150 with QorIQ™ P5020, 1.8 GHz

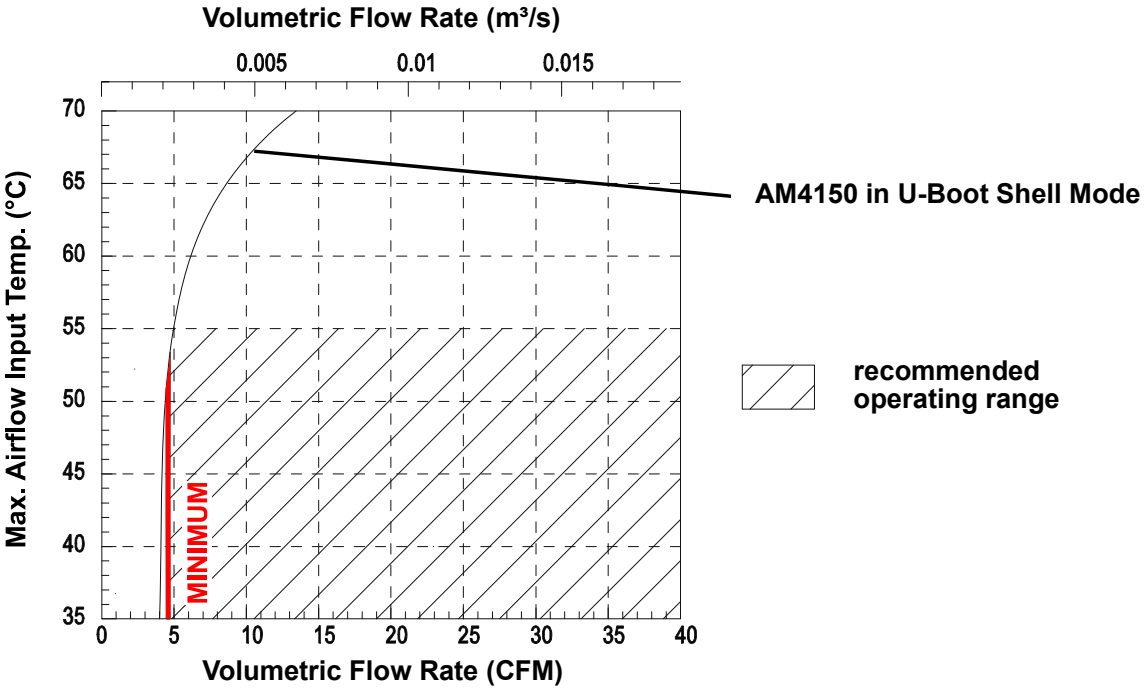
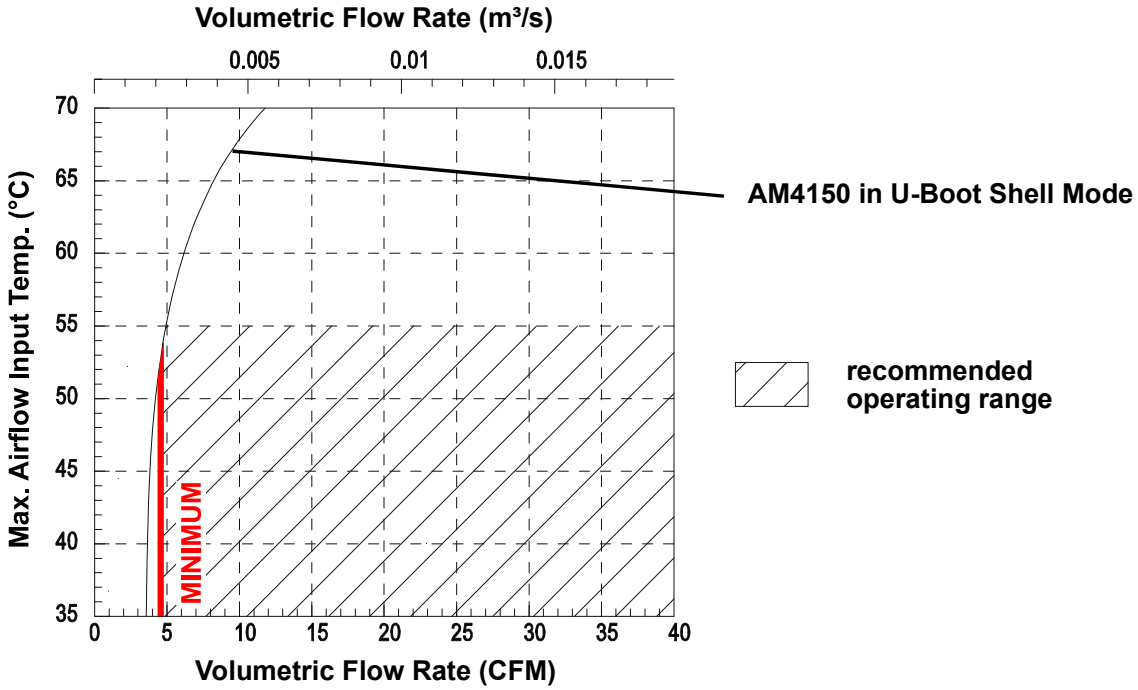


Figure 6-3: Operating Limits of the AM4150 with QorIQ™ P5020, 1.6 GHz

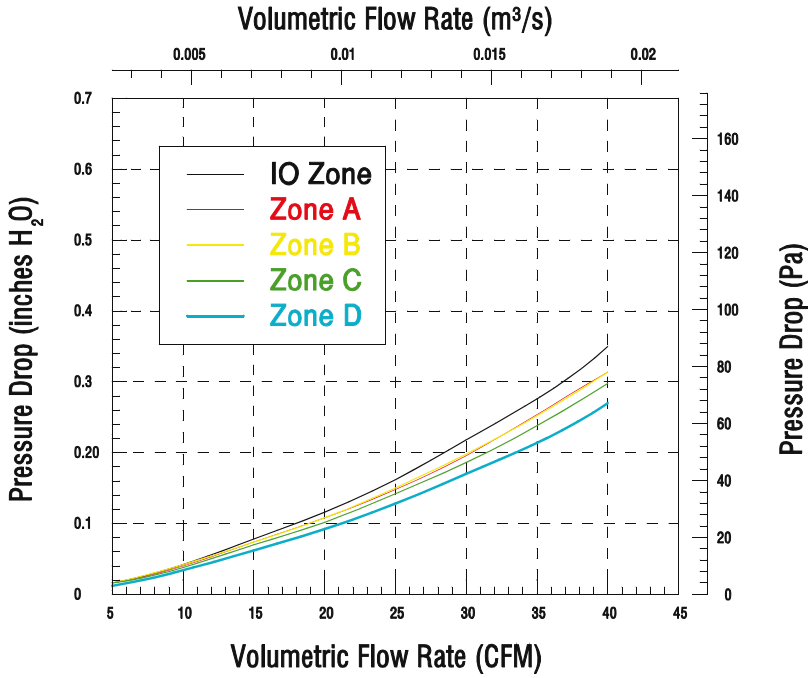


6.3.1 Airflow Impedance

In order to determine the cooling requirements of the AM4150, the airflow impedance of an AM4150 module has been determined via measurement. No card guides or struts have been used for the measurements because the resulting airflow impedance depends on individual configuration of the AMC carrier or MicroTCA system.

The following figure shows the airflow impedance curves of an AM4150 module.

Figure 6-4: AM4150 Airflow Impedance



The following table indicates the pressure drop ranging from 5 to 40 cfm volumetric flow rates.

Table 6-1: AM4150 Airflow Impedance by Zone [N/m²]

VOLUMETRIC FLOW RATE [CFM]	PRESSURE DROP [N/m²]				
	I/O ZONE	ZONE A	ZONE B	ZONE C	ZONE D
5	4,2	3,9	3,9	3,9	3,2
10	10,4	10,0	10,4	9,4	8,4
15	19,5	18,2	18,2	17,2	15,2
20	28,7	26,7	26,7	25,3	22,7
25	40,5	36,8	37,5	35,5	31,8
30	54,0	49,0	49,3	46,3	42,3
35	68,5	63,1	62,5	59,1	53,1
40	86,9	77,9	78,3	73,9	67,3

Table 6-2: AM4150 Airflow Impedance by Zone [inches H_2O]

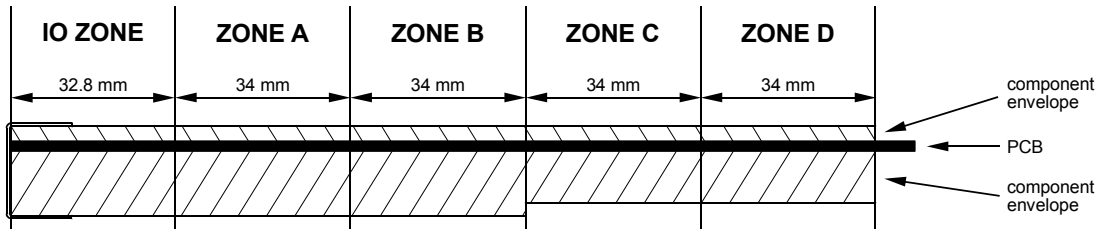
VOLUMETRIC FLOW RATE [CFM]	PRESSURE DROP [inches H_2O]				
	I/O ZONE	ZONE A	ZONE B	ZONE C	ZONE D
5	0,02	0,02	0,02	0,02	0,01
10	0,04	0,04	0,04	0,04	0,03
15	0,08	0,07	0,07	0,07	0,06
20	0,12	0,11	0,11	0,10	0,09
25	0,16	0,15	0,15	0,14	0,13
30	0,22	0,20	0,20	0,19	0,17
35	0,27	0,25	0,25	0,24	0,21
40	0,35	0,31	0,31	0,30	0,27

6.3.2 Airflow Paths

The area between the front panel and the AMC Card-edge connector is divided into five zones, one I/O zone and four uniform thermal zones, A, B, C, and D. The PICMG AMC.0 Specification states that the uniformity of the airflow paths' resistance should provide an impedance on the A, B, C, and D zones that is within ± 25% of the average value of the four thermal zones.

The following figure shows the thermal zones of an AM4150.

Figure 6-5: Thermal Zones of the AM4150 Module



The following table indicates the deviation of the airflow rate of an AM4150 module.

Table 6-3: AM4150 Deviation of the Airflow Rate [%]

VOLUMETRIC FLOW RATE [CFM]	DEVIATION OF THE AIRFLOW RATE [%]			
	ZONE A	ZONE B	ZONE C	ZONE D
5	-0.7	-3.3	1.1	2.9
10	0.0	-2.2	0.0	2.2
15	0.7	-2.0	-0.2	1.5
20	1.0	-2.0	-0.5	1.5
25	1.1	-1.9	-0.5	1.3
30	1.3	-1.8	-0.6	1.1
35	1.4	-1.8	-0.7	1.1
40	1.4	-1.7	-0.7	1.1

Note ...

The AM4150 module has an airflow rate deviation of max. ± 3.5% of the average value of the four thermal zones (max. ± 25% is allowed).

Positive deviation means increased airflow.

Negative deviation means decreased airflow.

Note ...

The AM4150 module provides an open area of 40%. According to the PICMG AMC.0 Specification, an open area of 20 to 70% perpendicular to the airflow path is recommended.

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Appendix A

SATA Flash Module

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A. SATA Flash Module

The AM4150 provides an optional SATA Flash module with up to 64 GB NAND flash memory. The SATA Flash module is connected to the AM4150 via the board-to-board connectors J5 located on the AM4150 and J2 located on the SATA Flash module. The SATA Flash module has been optimized for embedded systems providing high performance, reliability and security.

A.1 Technical Specifications

Table A-1: SATA Flash Module Main Specifications

SATA FLASH MODULE		SPECIFICATIONS
Interface	Board-to-Board Connector	One 34-pin, male, board-to-board connector, J2
Memory	Memory	Up to 64 GB SLC-based NAND flash memory • Built-in full hard disk emulation • Up to 100 MB/s read rate • Up to 90 MB/s write rate
General	Power Consumption	typ. 1.0 W 3.3 V supply
	Temperature Range	Operational: -5°C to +55°C Standard Storage: -40°C to +70°C
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	70 mm x 28 mm
	Board Weight	ca. 14 grams

Note ...

Write protection is available for this module. Please contact Kontron for further assistance if write protection is required.

A.2 SATA Flash Module Layout

The SATA Flash module includes one board-to-board connector, J2, for connection to the AM4150.

Figure A-1: SATA Flash Module Layout (Bottom View)