» User Guide «

CP6002

6U CompactPCI Processor Board based on the Intel® Core™ i7 Processor with the Intel® QM57 Chipset

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Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.

Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.

Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.

Note ...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

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High Voltage Safety Instructions

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Caution, Electric Shock!

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Special Handling and Unpacking Instructions

ESD Sensitive Device!

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It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Kontron grants the original purchaser of Kontron's products a ***TWO YEAR LIMITED HARDWARE WARRANTY*** as described in the following. However, no other warranties that may be granted or implied by anyone on behalf of Kontron are valid unless the consumer has the express written consent of Kontron.

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If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

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Chapter 1

Introduction

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1. Introduction

1.1 Board Overview

The CP6002 is a highly integrated 6U CompactPCI system controller board based on the multi-chip Intel® Core™ i7 processor combined with the mobile Intel® QM57 Express chipset.

The board supports the Intel® Core™ i7-610E processor with 2.53 GHz frequency, the Intel® Core™ i7-620LE processor with 2.0 GHz frequency, and the Intel® Core™ i7-660UE processor with 1.33 GHz frequency, all with 64 kB L1 cache, 256 kB L2 cache and 4 MB L3 cache, as well as the Intel® Celeron® P4505 processor with 1.86 GHz frequency and 64 kB L1 cache, 512 kB L2 cache, 2 MB L3 cache. The processors are built on 32-nm technology and provided in a BGA package.

The CP6002 includes up to 8 GB, dual-channel Double Data Rate (DDR3) memory with Error Checking and Correcting (ECC) running at 1066 MHz. The graphics controller and the memory controller are integrated in the processor.

The CP6002 provides support for up to two PMC/XMC modules, up to 32 GB SATA Flash memory (SSD) or one 2.5" HDD/SSD, and one CompactFlash card.

The board also includes up to four Intel® 82574L Gigabit Ethernet controllers utilizing x1 lane PCI Express interconnections to the Intel® QM57 chipset and implemented as up to two ports on front I/O and two ports on rear I/O (PICMG 2.16).

The CP6002 comes with six Serial ATA interfaces with RAID support, one SATA NAND or HDD/SSD, one CompactFlash, and four on the rear I/O; one high-resolution graphics interface (VGA/DP/HDMI); and up to two PMC/XMC slots (64-bit/66 MHz PCI or 64-bit/100 MHz PCI-X or x8 PCI Express interfaces). In addition, six USB 2.0 ports are available on the board, two on front I/O and four on rear I/O. Further interfaces include two COM ports, one RS-232 port implemented as an RJ-45 connector (only available on the CP6002-R1) on the front panel and routed to rear I/O as well as one RS-422 port on the rear I/O.

The board supports a configurable 64-bit/66 MHz PCI or PCI-X, hot swap CompactPCI interface. When installed in the system slot, the interface is enabled, and when installed in a peripheral slot, the CP6002 is isolated from the CompactPCI bus.

The CP6002 further provides Intelligent Platform Management Interface (IPMI) support. On request, the CP6002 provides safety and security features via a Trusted Platform Module (TPM) 1.2.

The CP6002 is offered in three versions, one with a single PMC/XMC (CP6002-R1) and two with two PMCs/XMCs (CP6002-R1-MC and CP6002-R2-MC). The CP6002-R1 can further accommodate an onboard 2.5" SATA HDD/SSD and provides two Gigabit Ethernet ports, one VGA (CRT) port, one COM port and two USB ports on the front panel. The CP6002-R1-MC and CP6002-R2-MC provide one Gigabit Ethernet port, one DisplayPort and two USB ports on the front panel. CP6002-R1 and CP6002-R1-MC are designed for standard application environments whereas CP6002-R2-MC is available with an extended operating temperature range, is ruggedized for high shock and vibration environments and provides support for conduction cooled PMCs/XMCs.

Designed for stability, the board fits into applications situated in industrial environments, including I/O intensive applications where only one slot is available for the CPU, making it a perfect core technology for long-life applications. Components with high temperature tolerance have been selected from embedded technology programs, and therefore offer long-term availability.

The board is offered with various Board Support Packages including Windows and Linux operating systems. For further information concerning the operating systems available for the CP6002, please contact Kontron.

1.2 Board-Specific Information

The CP6002 is a CompactPCI single-board computer based on the Intel® Core™ i7 processor and specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

Some of the CP6002's outstanding features are:

- Support for the following processors:
  - Intel® Core™ i7-610E (SV), 2.53 GHz, 4 MB L3 cache
  - Intel® Core™ i7-620LE (LV), 2.0 GHz, 4 MB L3 cache
  - Intel® Core™ i7-660UE (ULV), 1.33 GHz, 4 MB L3 cache
  - Intel® Celeron® P4505 (SV), 1.86 GHz, 2 MB L3 cache
- Intel® QM57 Express chipset
- Up to 8 GB, dual-channel, DDR3 SDRAM memory with ECC running at 1066 MHz
- Integrated 3D high-performance graphics controller with three high-resolution graphics interfaces (VGA/DP/HDMI/DVI)
- 64-bit/66 MHz PCI or PCI-X CompactPCI interface (PICMG 2.0)
- Two PMC slots with PCI functionality, 64-bit/66 MHz PCI or 64-bit/100 MHz PCI-X interface; one PMC slot provides rear I/O support
- Two XMC slots utilizing a x8 lane PCI Express interconnection
- Four Intel® 82574L Gigabit Ethernet controllers for:
  - Up to two Gigabit Ethernet interfaces on front I/O
  - Two Gigabit Ethernet interfaces on rear I/O (PICMG 2.16)
- Six Serial ATA interfaces with SATA RAID 0/1/5/10 support:
  - Two onboard Serial ATA interfaces
  - Four Serial ATA interfaces on the rear I/O
- Socket for one Serial ATA 2.5" hard disk drive (HDD) or solid state drive (SSD)
- Socket for one Serial ATA Flash module (SSD)
- CompactFlash socket
- Six USB ports:
  - Two USB 2.0 ports on the front panel
  - Four USB 2.0 ports on the rear I/O
- Two COM ports:
  - One RS-232 COM port either on the front panel or on the rear I/O
  - One RS-422 COM port on the rear I/O
- TCG 1.2 compliant Trusted Platform Module (TPM), on request
- Two SPI boot flashes for two separate uEFI BIOS images:
  - One standard SPI boot flash
  - One recovery SPI boot flash
- Watchdog timer
- Battery-backed real-time clock (RTC)
- Three onboard DIP switches for board configuration
- Hot swap capability: as system controller or as peripheral device
- Supports PICMG Packet Switching Backplane Specification 2.16
- IPMI compliant Baseboard Management Controller
- 4HP, 6U CompactPCI
- Passive heat sink solution for forced-airflow cooling
- Several rear I/O configurations

- Rear I/O on J3 and J5; optionally on J4 for PMC only
- Two GPIOs on J5 (on request)
- AMI Aptio®, a uEFI-compliant platform firmware

1.3 System Expansion Capabilities

1.3.1 PMC/XMC Module

The CP6002 has up to two PMC/XMC slots and provides a 3.3V PCI/PCI-X interface running with up to 64-bit/100 MHz for PMCs as well as up to two x8 PCI Express interfaces for XMCs. One PMC/XMC interface is rear I/O capable. The PMC/XMC slots provide support for a wide range of standard PMC/XMC and conduction-cooled PMC/XMC modules with PCI/PCI-X/PCI Express interfaces including all of Kontron's PMC/XMC modules and provides an easy and flexible way to configure the CP6002 for various application requirements. For information on the PMC interface, please refer to chapter 2.10.8, "PMC Interface".

1.3.2 CP6002-MK2.5SATA Assembly Kit

The CP6002 comes with an optional CP6002-MK2.5SATA assembly kit comprised of one CP6001-EXT-SATA module and the necessary components needed for mounting the module on the CP6002. The CP6001-EXT-SATA module is required for connecting an onboard 2.5" Serial ATA HDD or SSD to the CP6002. For further information concerning the CP6001-EXT-SATA module, please refer to Appendix A.

1.3.3 Serial ATA Flash Module

The CP6002 provides support for up to 32 GB of Serial ATA Flash memory in combination with an optional Serial ATA Flash module, which is connected to an onboard extension connector. For further information concerning the Serial ATA Flash module, please refer to Appendix B.

1.4 Version Comparison

Table 1-1: Version Comparison

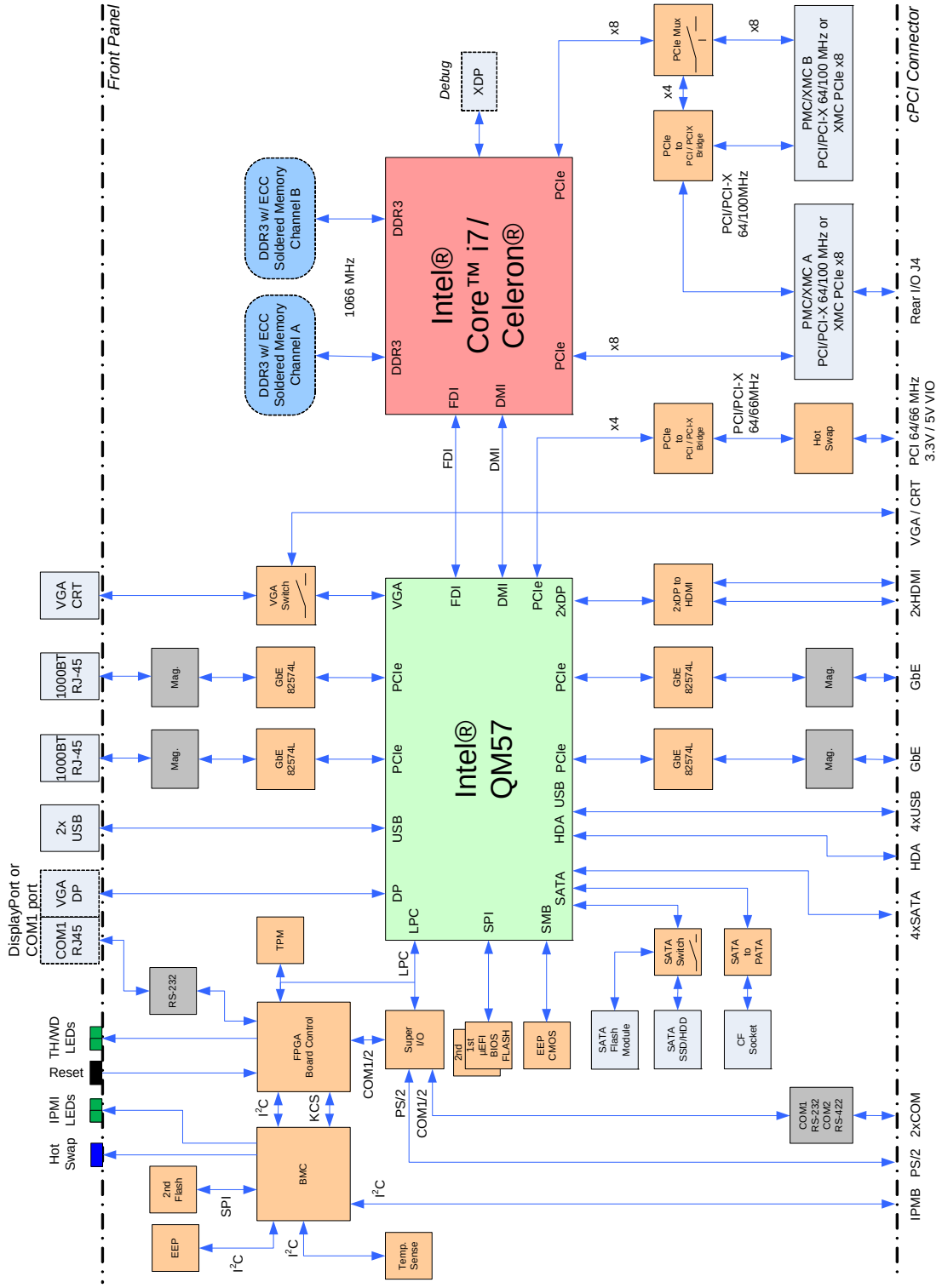
FEATURE	CP6002-R1	CP6002-R1-MC	CP6002-R2-MC
CPU	Intel® Core™ i7-610E, 2.53 GHz Intel® Core™ i7-620LE, 2.0 GHz- Intel® Core™ i7-660UE, 1.33 GHz Intel® Celeron® P4505, 1.86 GHz	Intel® Core™ i7-610E, 2.53 GHz Intel® Core™ i7-620LE, 2.0 GHz- Intel® Core™ i7-660UE, 1.33 GHz Intel® Celeron® P4505, 1.86 GHz	Intel® Core™ i7-620LE, 2.0 GHz- Intel® Core™ i7-660UE, 1.33 GHz
Operating Temperature	0°C to +60°C	0°C to +60°C	0°C to +60°C (standard) -40°C to +70°C (extended)
Board Stiffener	--	--	1
PMC/XMC	1	2	--
Conductive-cooled PMC/XMC	--	--	2
2.5" SATA HDD/SSD	1	--	--
CompactFlash	1	1	--
Front Ethernet port	2	1	1
Front VGA port	1	--	--
Front RS-232 port	1	--	--
Front DisplayPort	--	1	1
Shock/Vibration	Standard	Standard	Extended

1.5 Board Diagrams

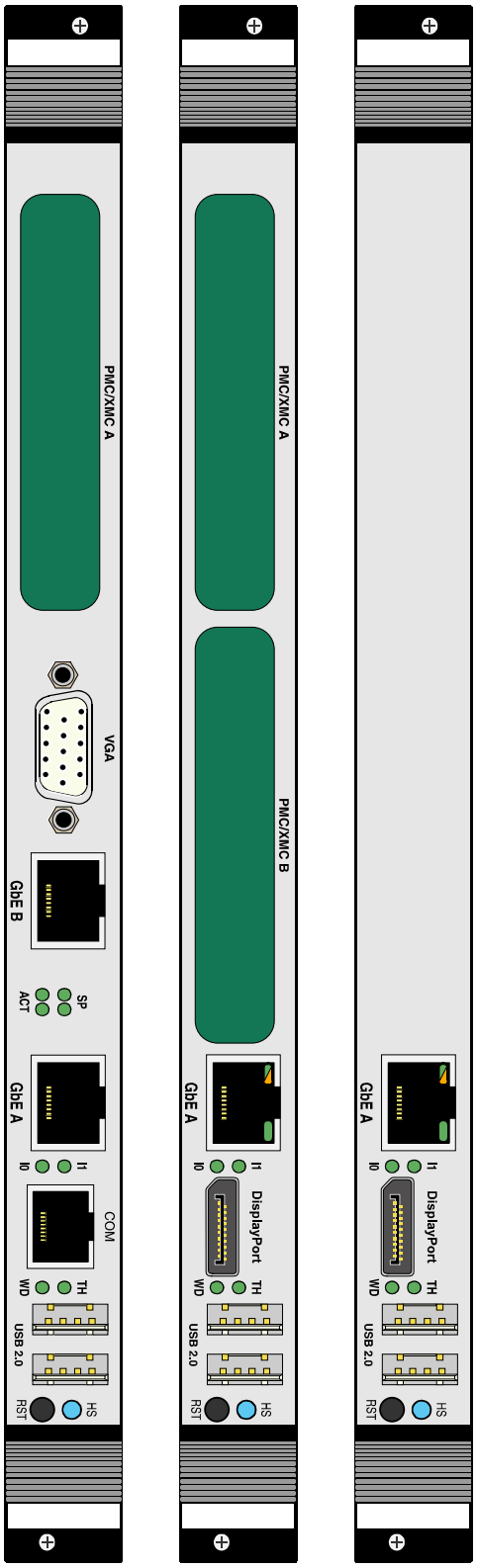
The following diagrams provide additional information concerning board functionality and component layout.

1.5.1 Functional Block Diagram

Figure 1-1: CP6002 Functional Block Diagram



1.5.2 Front Panels



CP6002-R1 CP6002-R1-MC CP6002-R2-MC

Figure 1-2: CP6002 Front Panels

Legend:

IPMI LEDs:

I0/I1 (green): Indicate the software status of the IPMI controller

Status LEDs:

WD (green): Watchdog Status

TH (green): Temperature Status

HS (blue): Hot Swap Control

Ethernet LEDs on CP6002-R1:

ACT (green): Ethernet Link/Activity

SPEED (green): Ethernet Speed

Ethernet LEDs on CP6002-R1-MC and CP6002-R2-MC:

ACT (green): Ethernet Link/Activity

SPEED (green/orange/off): Ethernet Speed

1.5.3 Board Layout

Figure 1-3: CP6002-R1 Board Layout – Top View

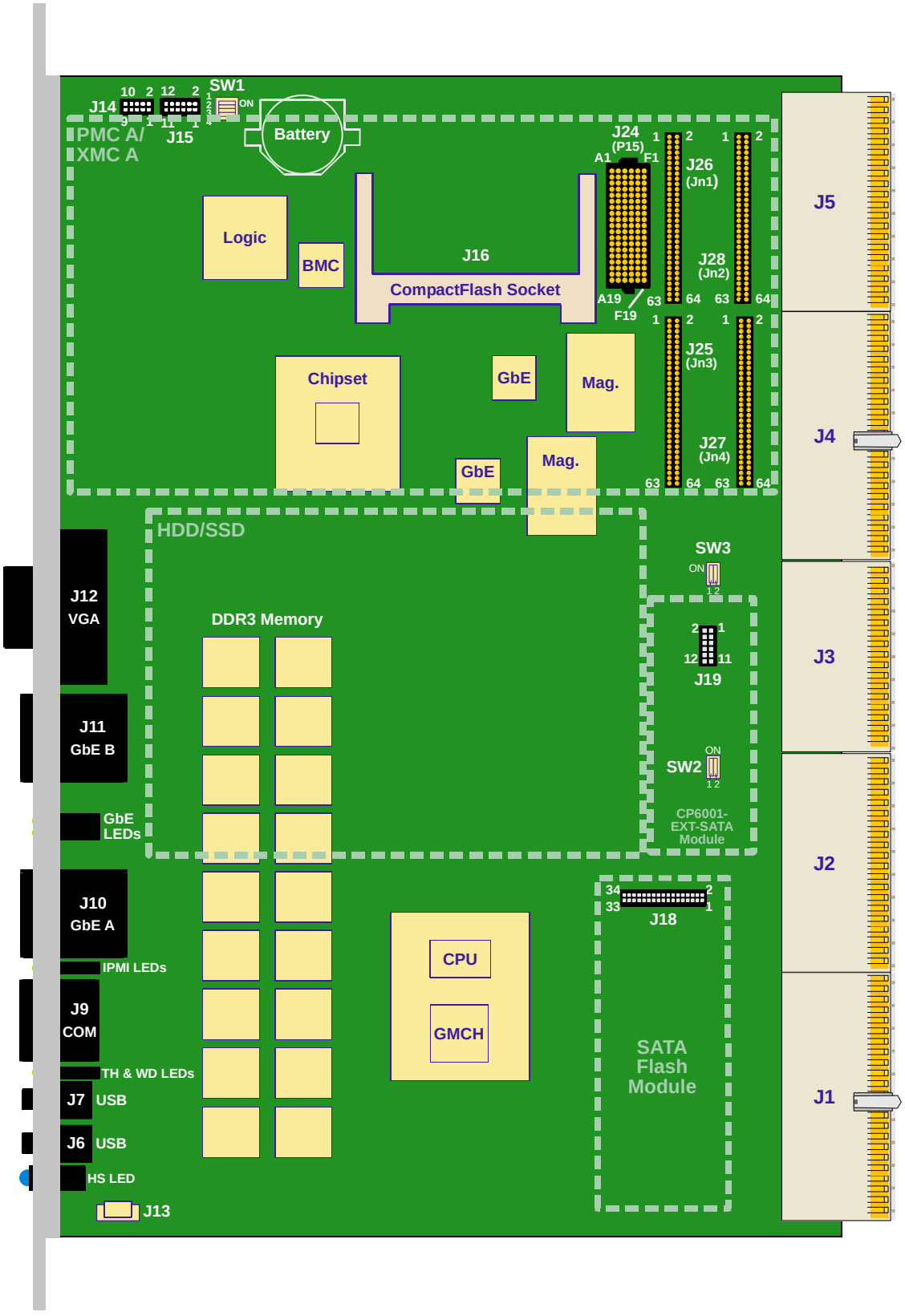


Figure 1-4: CP6002-R1-MC Board Layout – Top View

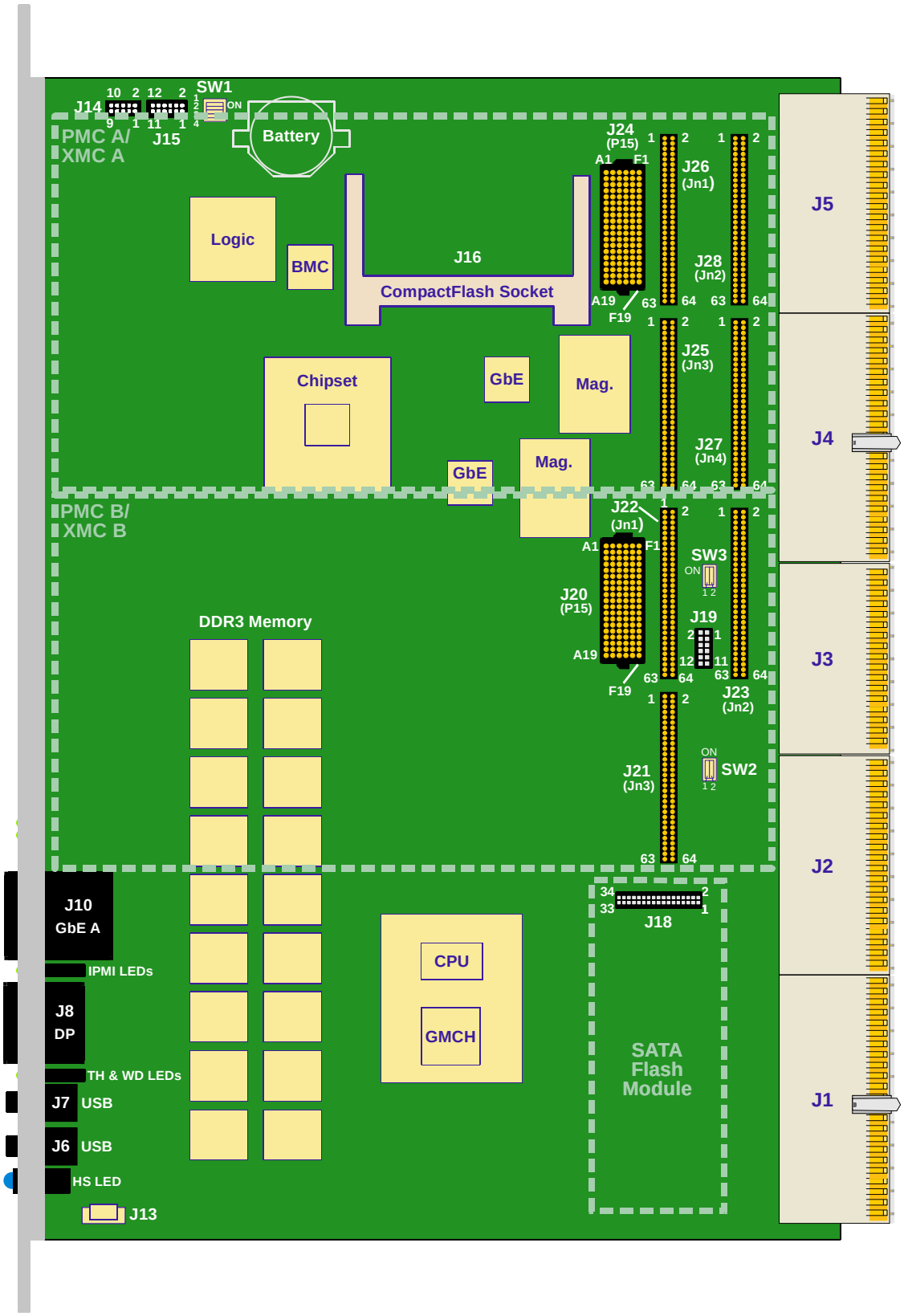


Figure 1-5: CP6002-R2-MC Board Layout – Top View

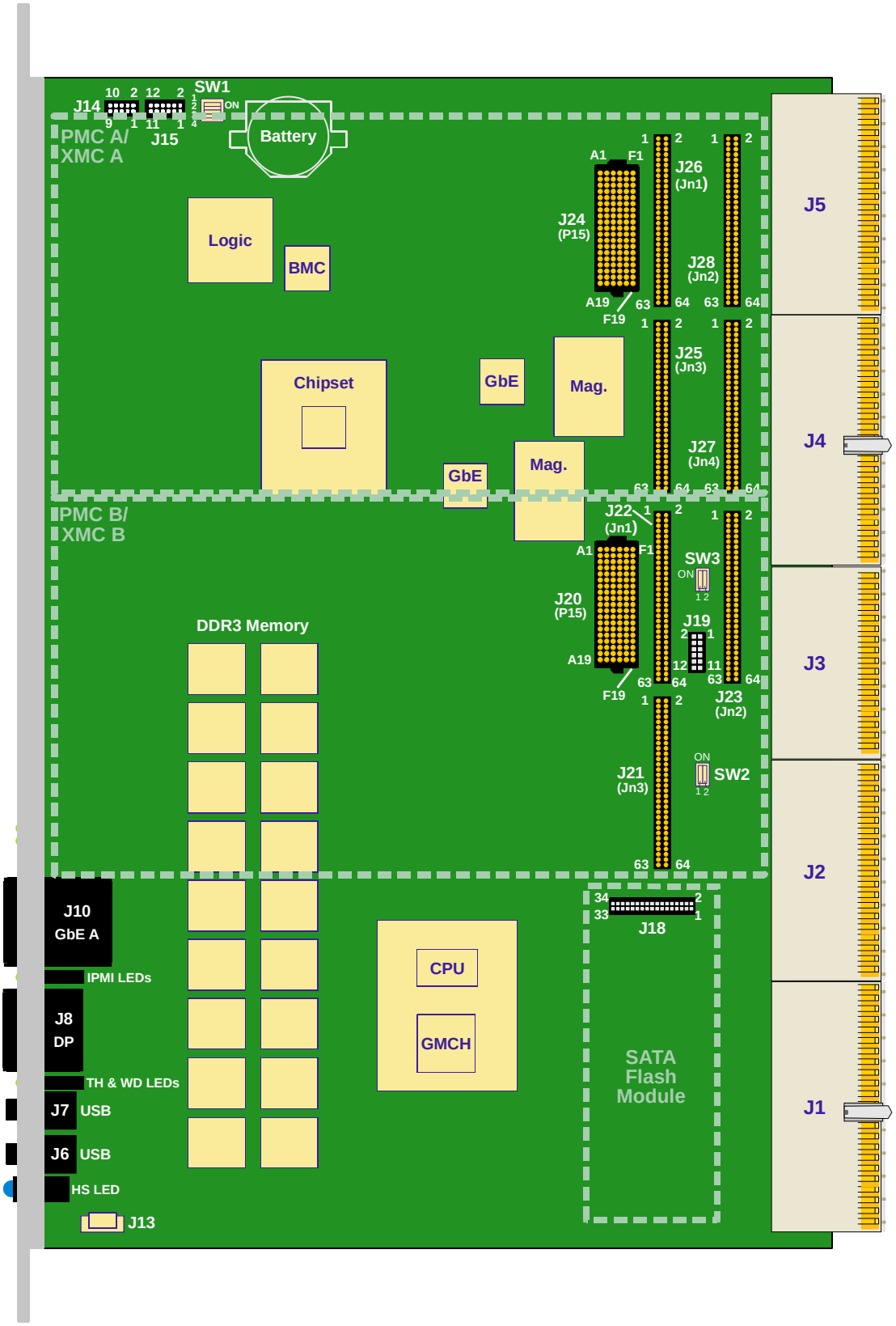
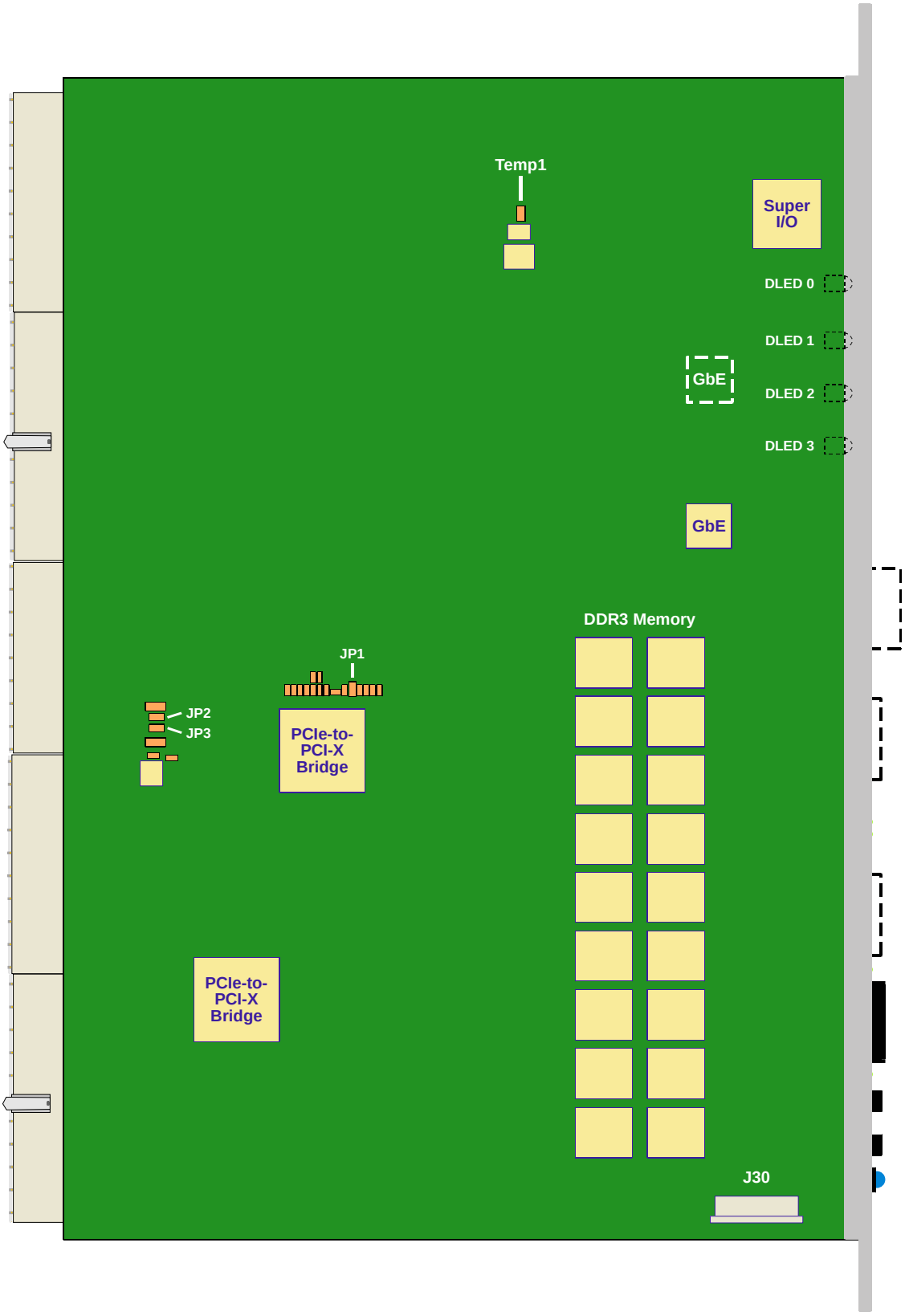


Figure 1-6: CP6002 Board Layout – Bottom View



1.6 Technical Specification

Table 1-2: CP6002 Main Specifications

FEATURES		SPECIFICATIONS
Processor and Memory	CPU	The CP6002 supports the following microprocessors: • Intel® Core™ i7-610E (SV), 2.53 GHz, 4 MB L3 cache • Intel® Core™ i7-620LE (LV), 2.0 GHz, 4 MB L3 cache • Intel® Core™ i7-660UE (ULV), 1.33 GHz, 4 MB L3 cache • Intel® Celeron® P4505 (SV), 1.86 GHz, 2 MB L3 cache Further processor features: • Two execution cores • Intel® Hyper-Threading Technology (Core™ i7) • Intel® 64 Architecture • Intel® Turbo Boost Technology (Core™ i7) • Intel® Intelligent Power Sharing (Core™ i7) • System Memory interface with optimized support for dual-channel DDR3 SDRAM memory at 1066 MHz with ECC • Integrated 2D and 3D Graphics Engines • DMI and FDI interfaces to the Intel® QM57 chipset • Two x8 PCI Express 2.0 ports operating at 2.5 GT/s Please contact Kontron for further information concerning the suitability of other Intel processors for use with the CP6002.

	Memory	Main Memory:
		• Up to 8 GB, dual-channel DDR3 SDRAM memory with ECC running at 1066 MHz
		Cache Structure:
		• 64 kB L1 cache for each core
		  • 32 kB instruction cache
		  • 32 kB data cache
		• Up to 512 kB L2 shared instruction/data cache for each core
		• Up 4 MB L3 shared instruction/data cache shared between both cores
		Flash Memory:
		• CompactFlash with true IDE mode (CP6002-R1 and CP6002-R1-MC)
		• Two redundant SPI boot flashes (2 x 8 MB) for two separate uEFI BIOS images
		• Up to 32 GB NAND Flash via an onboard Serial ATA Flash module (SSD)
		Serial EEPROM with 64 kbit

Table 1-2: CP6002 Main Specifications (Continued)

FEATURES		SPECIFICATIONS
Chipset	Intel® QM57	Mobile Intel® QM57 Express Chipset: • One x4 and four x1 PCI Express 2.0 ports operating at 2.5 GT/s • SATA host controller with six ports, 3 Gbit/s data transfer rate and RAID 0/1/5/10 support • USB 2.0 host interface with up to 14 USB ports available (only six ports are used on the CP6002) • SPI Flash interface support • Low Pin Count (LPC) interface • PCI interface, 32-bit/33 MHz (not used on the CP6002) • Power management logic support • Enhanced DMA controller, interrupt controller, and timer functions • System Management Bus (SMBus) compatible with most I²C™ devices • DMI and FDI interfaces to the processor • High Definition Audio (HDA) interface • Analog display port • Three digital display ports • Integrated RTC
Integrated Controller	Graphics controller	High-performance 3D graphics controller integrated in the processor: • Supports resolutions up to 2560 x 1600 pixels @ 60 Hz • Support for two independent displays • Dynamic Video Memory Technology (DVMT)
Interfaces	CompactPCI	Compliant with CompactPCI Specification PICMG 2.0 R 3.0: • System controller operation • 64-bit/66 MHz PCI or PCI-X master interface with dedicated PCIe-to-PCI-X bridge • 3.3V or 5V signaling levels (universal signaling support) Compliant with the Packet Switching Specification PICMG 2.16. When installed in a peripheral slot, the CP6002 is isolated from the CompactPCI bus. It receives power from the backplane and supports rear I/O and, if the system supports it, packet switching (in this case up to two channels of Gigabit Ethernet).
	Rear I/O	The following interfaces are routed to the rear I/O connector J3, J4 and J5: • COM1 and COM2 (RS-232 and RS-422 signaling); no buffer on the rear I/O module is necessary • 4 x USB 2.0 • 1 x CRT VGA, 2 x HDMI/DVI (with HDCP 1.4 support) • 1 x HDA • 2 x Gigabit Ethernet (compliant with PICMG 2.16, R 1.0) • 4 x SATA • 1 x rear I/O interconnection to PMC/XMC slot A • 2 x GPIOs (on request)

Table 1-2: CP6002 Main Specifications (Continued)

	FEATURES	SPECIFICATIONS
Interfaces	Hot Swap Compatible	The CP6002 supports System Master hot swap functionality and application-dependent hot swap functionality when used in a peripheral slot. When used as a System Master, the CP6002 supports individual clocks for each slot and the ENUM signal handling is in compliance with the PICMG 2.1 Hot Swap Specification.
	Gigabit Ethernet	Up to four 10 Base-T/100 Base-TX/1000 Base-T Gigabit Ethernet interfaces based on up to four Intel® 82574L Ethernet PCI Express bus controllers: • Up to two RJ-45 connectors on the front panel • Two ports on the rear I/O (PICMG 2.16) • Automatic mode recognition (Auto-Negotiation) • Automatic cabling configuration recognition (Auto-MDI/X)
	USB	Six USB ports supporting UHCI and EHCI: • Two type A USB 2.0 connectors on the front panel • Four USB 2.0 ports on the rear I/O interface
	Serial	Two 16C550-compatible UARTs (RS-232/RS-422 signaling): • One RS-232 port on the front panel and routed to rear I/O, COM1 • One RS-422 port on the rear I/O, COM2

	PMC	Up to two PMC slots:
		• Onboard mezzanine connectors for standard PMC modules:
		  • Four connectors for PMC/XMC slot A (Jn1-Jn4)
		  • Three connectors for PMC/XMC slot B (Jn1-Jn3), optional
		• Up to 64-bit/66 MHz PCI or up to 64-bit/100 MHz PCI-X interface with dedicated PCIe-to-PCI-X bridge
		• Only 3.3V PCI signaling voltage
		• Rear I/O supported through the CompactPCI connector J4 (slot A)
		• Supported voltages: 3.3 V, 5 V, +12 V, and -12 V

	XMC	Up to two XMC slots: • One onboard XMC connector (P15) for PMC/XMC Slot A • One onboard XMC connector (P15) for PMC/XMC Slot B, optional • Up to x8 lanes PCI Express per XMC slot • Rear I/O supported through the PMC connector (Jn4) to the CompactPCI connector J4 (slot A)
	Keyboard and Mouse	Keyboard and mouse are supported: • USB support

Table 1-2: CP6002 Main Specifications (Continued)

FEATURES		SPECIFICATIONS
Interfaces	Mass Storage	CompactFlash (CP6002-R1 and CP6002-R1-MC): • CompactFlash socket for type I and II CompactFlash cards (DMA capable true IDE mode) • The CompactFlash is always configured as IDE master • The CompactFlash interface is realized via a SATA-to-PATA bridge One Serial ATA interface for: • Up to 32 GB Flash memory via an onboard Serial ATA Flash module (SSD), or • Onboard 2.5" hard disk drive (HDD) or solid state drive (SSD) is supported via the SATA extension connector, J19, in combination with the CP6001-EXT-SATA module Integrated Serial ATA Host Controllers: • Provide support for independent DMA operation on six ports • Data transfer rates up to 300 MB/s • High-performance RAID 0/1/5/10 functionality on all SATA ports
Sockets	Front Panel Connectors	CP6002-R1: • VGA: 15-pin, D-Sub connector, J12 • USB: two 4-pin, type A connectors, J6 and J7 • Ethernet: two 8-pin, RJ-45 connectors, J10 and J11 • COM: one 8-pin, RJ-45 connector, J9 CP6002-R1-MC and CP6002-R2-MC: • USB: two 4-pin, type A connectors, J6 and J7 • Ethernet: one 8-pin, RJ-45 connector, J10 • DisplayPort: one 20-pin DisplayPort connector, J8
	Onboard Connectors	CP6002-R1: • PMC/XMC Slot A: Four PMC connectors, J25 - J28 (Jn1 - Jn4) • PMC/XMC Slot A: One XMC connector, J24 (P15) • One 12-pin SATA extension connector, J19, for CP6001-EXT-SATA • One 34-pin extension connector, J18, for SATA Flash module (SSD) • JTAG connector, J15 • Extension connector, J14 • XDP-SFF (debug) connector, J30 • CompactFlash socket, J16 • CompactPCI Connectors J1 - J5 • Hot Swap connector J13 CP6002-R1-MC and CP6002-R2-MC: • PMC/XMC Slot A: Four PMC connectors, J25 - J28 (Jn1 - Jn4) • PMC/XMC Slot B: Three PMC connectors, J21 - J23 (Jn1 - Jn3) • PMC/XMC Slot A: One XMC connector, J24 (P15) • PMC/XMC Slot B: One XMC connector, J20 (P15) • One 34-pin extension connector, J18, for SATA Flash module (SSD) • JTAG connector, J15 • Extension connector, J14 • XDP-SFF (debug) connector, J30 • CompactFlash socket, J16 (CP6002-R1-MC) • CompactPCI Connectors J1 - J5 • Hot Swap connector J13

Table 1-2: CP6002 Main Specifications (Continued)

FEATURES		SPECIFICATIONS
Switches	DIP Switches	Three onboard DIP switches, SW1, SW2, and SW3, for board configuration
	Reset Switch	One front panel hardware reset switch
	Hot Swap Switch	One switch for hot swap purposes integrated in the front panel handle in accordance with PICMG 2.1 Rev. 2.0.
LEDs	System LEDs	System Status LEDs: • I0/I1 (green): Indicate the software status of the IPMI controller • WD (green): Watchdog Status • TH (green): Temperature Status • HS (blue): Hot Swap Control Debug LEDs: • DLED0-3: Onboard LEDs for debugging purposes (located on the rear side of the board)
	Ethernet LEDs	Gigabit Ethernet Status on CP6002-R1: • ACT (green): Ethernet Link/Activity • SPEED (green): Ethernet Speed Gigabit Ethernet Status on CP6002-R1-MC and CP6002-R2-MC: • ACT (green): Ethernet Link/Activity • SPEED (green/orange/off): Ethernet Speed
Timer	Watchdog Timer	• Software-configurable, two-stage Watchdog with programmable timeout ranging from 125 ms to 4096 s in 16 steps • Serves for generating IRQ or hardware reset
	System Timer	• The Intel® QM57 chipset contains three 8254-style counters which have fixed uses • In addition to the three 8254-style counters, the Intel® QM57 chipset includes eight individual high-precision event timers that may be used by the operating system. They are implemented as a single counter each with its own comparator and value register.
IPMI	Baseboard Management Controller	• NXP® ARM7 microcontroller with redundant 512 kB Firmware Flash and automatic roll-back strategy • The BMC carries out IPMI commands such as monitoring several onboard temperature conditions, board voltages and the power supply status, and managing hot swap operations. • The BMC is accessible via two IPMBs (through the J1 and J2 connectors) and one host Keyboard Controller Style (KCS) interface.

	Thermal Management	CPU and board overtemperature protection is provided by:
		• Temperature sensors integrated in processor:
		  • Two temperature sensors for monitoring the processor cores
		  • One temperature sensor for monitoring the graphics controller and the memory controller
		• One temperature sensor integrated in the Intel® QM57 chipset for monitoring the chipset
		• One onboard temperature sensor for monitoring the board temperature
		• Specially designed heat sinks

Table 1-2: CP6002 Main Specifications (Continued)

FEATURES		SPECIFICATIONS
Security	TPM	Trusted Platform Module (TPM) 1.2 for enhanced hardware- and software-based data and system security (on request)
Software	uEFI BIOS	AMI Aptio®, AMI's next-generation BIOS firmware based on the uEFI Specification and the Intel Platform Innovation Framework for EFI. • LAN boot capability for diskless systems (standard PXE) • Redundant image; automatic fail-safe recovery in case of a damaged image • Non-volatile storage of setting in the SPI Flash (battery only required for the RTC) • Compatibility Support Module (CSM) providing legacy BIOS compatibility based on AMIBIOS8 • Command shell for diagnostics and configuration • uEFI shell commands executable from mass storage device in a Pre-OS environment (open interface) • IPMI support in the command shell
	Software IPMI	Board Management Controller Firmware providing the following features: • The BMC is accessible via two IPMBs and one KCS interface with interrupt support • The BMC Firmware can be updated in field through all supported interfaces using the function "fwum..." of the open-source tool "ipmitool". For further information on the ipmitool refer to the sourceforge.net website. • Two BMC Flash banks with automatic roll-back capability in case of an upgrade firmware failure • Board supervision and control extensions such as board reset, power and SPI Flash control, and boot order configuration
	Operating Systems	The board is offered with various Board Support Packages including Windows and Linux operating systems. For further information concerning the operating systems available for the CP6002, please contact Kontron.

Table 1-2: CP6002 Main Specifications (Continued)

	FEATURES	SPECIFICATIONS
General	Mechanical	6U, 4HP, CompactPCI-compliant form factor
	Power Consumption	See Chapter 5 for details.
	Temperature Ranges	Operational: 0°C to +60°C Standard (depending on processor version and airflow in the system) -40°C to +70°C Extended (CP6002-R2-MC) without TPM Storage: -55°C to +85°C Without hard disk and without battery  *Note ...* When a battery is installed, refer to the operational specifications of the battery as this determines the storage temperature of the CP6002 (See "Battery" below).  *Note ...* When additional components are installed, refer to their operational specifications as this will influence the operational and storage temperature of the CP6002.
	Battery	3.0V lithium battery for RTC with battery socket. Recommended type: CR1632 Temperature ranges: Operational: -20°C to +70°C typical (refer to the battery manufacturer's specifications for exact range) Storage: -55°C to +70°C typical (no discharge)
	Climatic Humidity	93% RH at 40 °C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	233.35 mm x 160 mm
	Board Weight	CP6002-R1: 500 g (with heat sink but without mezzanine cards) CP6002-R1-MC: 500 g (with heat sink but without mezzanine cards) CP6002-R2: 720 g (with heat sink but without mezzanine cards)

1.7 Standards

The board complies with the requirements of the following standards:

Table 1-3: Standards for the CP6002

TYPE	ASPECT	STANDARD	REMARKS
CE	Emission	EN55022 EN61000-6-3	--
	Immission	EN55024 EN61000-6-2	--
	Electrical Safety	EN60950-1	--
Mechanical	Mechanical Dimensions	IEEE 1101.10	--
Environmental	Climatic Humidity	IEC60068-2-78	--
	WEEE	Directive 2002/96/EC	Waste electrical and electronic equipment
	RoHS	Directive 2002/95/EC	Restriction of the use of certain hazardous substances in electrical and electronic equipment
	Vibration (Sinusoidal)	IEC60068-2-6	Ruggedized version test parameters: • 10-300 (Hz) frequency range • 2 (g) acceleration • 1 (oct/min) sweep rate • 10 cycles/axis • 3 axes
	Single Shock	IEC60068-2-27	Ruggedized version test parameters: • 30 (g) acceleration • 9 (ms) shock duration half sine • 3 number of shocks per direction (total: 18) • 6 directions • 5 (s) recovery time
	Permanent Shock	IEC60068-2-29	Ruggedized version test parameters: • 15 (g) acceleration • 11 (ms) shock duration half sine • 500 number of shocks per direction • 6 directions • 5 (s) recovery time

Note ...

Kontron performs comprehensive environmental testing of its products in accordance with applicable standards.

Customers desiring to perform further environmental testing of Kontron products must contact Kontron for assistance prior to performing any such testing. This is necessary, as it is possible that environmental testing can be destructive when not performed in accordance with the applicable specifications.

In particular, for example, boards **without conformal coating** must not be exposed to a change of temperature exceeding 1K/minute, averaged over a period of not more than five minutes. Otherwise, condensation may cause irreversible damage, especially when the board is powered up again.

Kontron does not accept any responsibility for damage to products resulting from destructive environmental testing.

In addition, the CP6002-R2-MC complies with the following standards as well.

Table 1-4: Additional Standards for the CP6002-R2-MC

TYPE	ASPECT	STANDARD	REMARKS
Environmental	Random Vibration (Broadband)	ANSI/VITA 47, Class V2	Test parameters: • 5-100 (Hz) frequency range: +3dB slope • 100-1000 (Hz) freq. range: 0.04 (g^2/Hz) • 1000-2000 (Hz) freq. range: -6dB slope • 7.619 g (rms) • 60 (min) test duration/axis • 3 axes
	Single Shock	ANSI/VITA 47, Class OS1	Test parameters: • 20 (g) acceleration • 11 (ms) shock duration half sine • 3 shocks per direction • 6 directions • 5 (s) recovery time

1.8 Related Publications

The following publications contain information relating to this product.

Table 1-5: Related Publications

PRODUCT	PUBLICATION
CompactPCI Systems and Boards	CompactPCI Specification PICMG 2.0, Rev. 3.0 CompactPCI Packet Switching Backplane Specification PICMG 2.16 Rev. 1.0 CompactPCI System Management Specification PICMG 2.9 Rev. 1.0 CompactPCI Hot Swap Specification PICMG 2.1 Rev. 2.0
	IPMI - Intelligent Platform Management Interface Specification v2.0 (without LAN support)
	Kontron CompactPCI Backplane Manual, ID 24229
PMC Module	IEEE 1386-2001, IEEE Standard for a Common Mezzanine Card (CMC) Family IEEE 1386.1-2001, IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)
XMC Module	ANSI/VITA 42.0-200x XMC Switched Mezzanine Card Auxiliary Standard ANSI/VITA 42.3-2006 XMC PCI Express Protocol Layer Standard
CCPMC Modules	VITA 20-2001 (R2005)
CompactFlash Cards	CF+ and CompactFlash Specification Revision 2.1
Platform Firmware	Unified Extensible Firmware Interface (uEFI) Specification, Version 2.1
All Kontron products	Product Safety and Implementation Guide, ID 1021-9142
Kontron	CP6002 uEFI BIOS User Guide, ID 1039-1612
	CP6002 IPMI Firmware User Guide: ID 1039-1613

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Chapter 2

Functional Description

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2. Functional Description

2.1 Processor

The board supports the Intel® Core™ i7-610E processor with 2.53 GHz clock speed, the Intel® Core™ i7-620LE processor with 2.0 GHz clock speed, the Intel® Core™ i7-660UE processor with 1.33 GHz clock speed, and the Intel® Celeron® P4505 processor with 1.86 GHz clock speed.

The processor used on the CP6002 includes an integrated high-performance graphics controller and a DDR3 dual-channel memory controller with ECC support as well as one x16 PCI Express 2.0 port operating at 2.5 GT/s. They support various technologies, such as:

- Intel® Hyper-Threading Technology (Core™ i7)
- Intel® Turbo Boost Technology (Core™ i7)
- Intel® Intelligent Power Sharing (Core™ i7)
- Intel® SpeedStep® Technology
- Intel® Virtualization Technology
- Intel® Streaming SIMD Extensions 4.1
- Intel® Streaming SIMD Extensions 4.2
- Intel® 64 Architecture
- Execute Disable Bit

The Intel® Hyper-Threading Technology allows one execution core to function as two logical processors. When this feature is used on the CP6002, four processor cores are present to the operating system. This results in higher processing throughput and improved performance on the multithreaded software. This feature must be enabled in the uEFI BIOS in order to be available.

The Intel® Turbo Boost Technology and the Intel® Intelligent Power Sharing technology allow the processor and the graphics controller to opportunistically and automatically run faster than its rated operating clock frequency if it is operating below power, temperature, and current limits. This feature must be enabled in the uEFI BIOS for the processor and graphics controller to operate with maximum performance.

The Intel® SpeedStep® technology enables real-time dynamic switching of the voltage and frequency between several modes. This is achieved by switching the bus ratios, the core operating voltage, and the core processor speeds without resetting the system.

The Intel® Core™ i7 processors used on the CP6002 have the following multi-level cache structure:

- 64 kB L1 cache for each core
  - 32 kB instruction cache
  - 32 kB data cache
- 256 kB L2 instruction/data cache for each core
- 4 MB L3 shared instruction/data cache shared between both cores

The Intel® Celeron® processor used on the CP6002 has the following multi-level cache structure:

- 64 kB L1 cache for each core
  - 32 kB instruction cache
  - 32 kB data cache
- 512 kB L2 instruction/data cache for each core
- 2 MB L3 shared instruction/data cache shared between both cores

Table 2-1: Features of the Processors Supported on the CP6002

FEATURE	Core™ i7-610E (SV) 2.53 GHz	Core™ i7-620LE (LV) 2.0 GHz	Core™ i7-660UE (ULV) 1.33GHz	Celeron® P4505 (ULV) 1.86 GHz
High Frequency Mode (HFM)	2.53 GHz	2.0 GHz	1.33 GHz	1.86 GHz
Low Frequency Mode (LFM)	1.2 GHz	1.2 GHz	666 MHz	933 MHz
Maximum Turbo Frequency	3.2 GHz	2.8 GHz	2.4 GHz	--
L1 cache per core	64 kB	64 kB	64 kB	64 kB
L2 cache per core	256 kB	256 kB	256 kB	512 kB
L3 cache	4 MB	4 MB	4 MB	2 MB
DDR3 Memory	up to 8 GB / 1066 MHz	up to 8 GB / 1066 MHz	up to 8 GB / 1066 MHz	up to 8 GB / 1066 MHz
Graphics Base Frequency	500 MHz	266 MHz	166 MHz	500 MHz
Graphics Max. Dynamic Frequency	766 MHz	566 MHz	500 MHz	667 MHz
Thermal Design Power	35 W	25 W	18 W	35 W
Package	BGA (1288)	BGA (1288)	BGA (1288)	BGA (1288)

2.2 Memory

The CP6002 supports a soldered, dual-channel (144-bit), Double Data Rate (DDR3) memory with Error Checking and Correcting (ECC) running at 1066 MHz (memory error detection and reporting of 1-bit and 2-bit errors and correction of 1-bit failures). The available memory configuration can be either 4 GB or 8 GB.

However, when the internal graphics controller is enabled, the amount of memory available to applications is less than the total physical memory in the system. For example, the chipset's Dynamic Video Memory Technology dynamically allocates the proper amount of system memory required by the operating system and the application.

2.3 Intel® QM57 Express Chipset

The CP6002 is equipped with the mobile Intel® QM57 Express Chipset, a highly integrated platform controller hub (PCH) with the following features:

- Two x4 or eight x1 PCI Express 2.0 ports operating at 2.5 GT/s
- SATA host controller with six ports, 3 Gbit/s data transfer rate and RAID 0/1/5/10 support
- USB 2.0 host interface with up to 14 USB 2.0 ports available (only six ports are used on the CP6002)
- SPI interface support
- Low Pin Count (LPC) interface
- PCI interface, 32-bit/33 MHz (not used on the CP6002)
- Power management logic support
- Enhanced DMA controller, interrupt controller, and timer functions
- System Management Bus (SMBus) compatible with most I²C™ devices
- DMI and FDI interfaces to the processor
- Intel® High Definition Audio Interface
- Analog display port
- Three digital display ports
- Integrated RTC

2.4 Timer

The CP6002 is equipped with the following timers:

- Real-Time Clock
  The Intel® QM57 chipset integrates an MC146818B-compatible real-time clock with 256 Byte CMOS RAM. All CMOS RAM data remain stored in an additional EEPROM device to prevent data loss.
- Counter/Timer
  Three 8254-style counter/timers are included on the CP6002 as defined for the PC/AT.
- The Intel® QM57 chipset integrates eight high-precision event timers.

2.5 Watchdog Timer

The CP6002 provides a Watchdog timer that is programmable for a timeout period ranging from 125 ms to 4096 s in 16 steps. Failure to trigger the Watchdog timer in time results in a system reset or an interrupt. In dual-stage mode, a combination of both interrupt and reset if the Watchdog is not serviced. A hardware status flag will be provided to determine if the Watchdog timer generated the reset.

2.6 Battery

The CP6002 is provided with a 3.0 V “coin cell” lithium battery for the RTC. For further information concerning the battery and its replacement, refer to Chapter 3.5.7, Battery Replacement.

2.7 Reset

The CP6002 is automatically reset by a precision voltage monitoring circuit that detects a drop in voltage below the acceptable operating limit of 4.7 V for the 5 V line and below 3.1 V for the 3.3 V line, or in the event of a power failure of the DC/DC converters. Other reset sources include the Watchdog timer and the push-button switch on the front panel. The CP6002 responds to any of these sources by initializing local peripherals.

A reset will be generated if one the following events occurs:

- +5 V supply falls below 4.7 V (typ.)
- +3.3 V supply falls below 3.1 V (typ.)
- Power failure of at least one onboard DC/DC converter
- Push-button "RESET" pressed (on the front panel)
- Watchdog expired
- CompactPCI backplane PRST input
- CompactPCI backplane RST input (software-configurable when the board is in peripheral mode)

2.8 Flash Memory

The CP6002 provides Flash interfaces for redundant uEFI BIOS, the SATA Flash module and a CompactFlash card.

2.8.1 SPI Boot Flash for uEFI BIOS

The CP6002 provides two SPI boot flash chips (2 x 8 MB) for two separate uEFI BIOS images, a standard SPI boot flash and a recovery SPI boot flash. The fail-over mechanism for the uEFI BIOS recovery can be controlled via the BMC or the DIP switch SW3, switch 2.

The SPI boot flash includes a hardware write protection option, which can be configured via the uEFI BIOS. If write protection is enabled, the SPI boot flash cannot be written to.

The SPI boot flash includes a hardware write protection option, which can be configured via the uEFI BIOS. If write protection is enabled, the SPI boot flash cannot be written to.

Note ...

The uEFI BIOS code and settings are stored in the SPI boot flashes. Changes made to the uEFI BIOS settings are available only in the currently selected SPI boot flash.Thus, switching over to the other SPI boot flash may result in operation with different uEFI BIOS code and settings.

2.8.2 Serial ATA Flash Module (optional)

The CP6002 supports up to 32 GB of Serial ATA Flash memory in combination with an optional Serial ATA Flash module, which is connected to the onboard connector J18.

The Serial ATA Flash module is an SLC-based SATA NAND Flash drive with a built-in full hard-disk emulation and a high data transfer rate (sustained read rate with up to 100 MB/s and sustained write rate with up to 90 MB/s). It is optimized for embedded systems providing high performance, reliability and security.

Note ...

Write protection is available for this module. Contact Kontron for further assistance if write protection is required

2.8.3 CompactFlash Socket (CP6002-R1 and CP6002-R1-MC)

A CompactFlash socket, J16, is available on the CP6002-R1 and CP6002-R1-MC versions for connecting a CompactFlash card to the board.

CompactFlash cards of type I or II with DMA and true IDE functionality are supported.

The CompactFlash socket is connected to the PATA-to-SATA bridge and is set to master configuration.

2.9 Trusted Platform Module 1.2 (On Request)

The CP6002 has been designed to support the Trusted Platform Module (TPM) 1.2. This feature is available on request. TPM1.2 is a security chip specifically designed to provide enhanced hardware- and software-based data and system security. It stores sensitive data such as encryption and signature keys, certificates and passwords, and is able to withstand software attacks to protect the stored information.

Hardware features of the TPM 1.2:

- TCG 1.2 compliant Trusted Platform Module (TPM)
- Security architecture based on the Infineon SLE66CXxxPE security controller family
- EEPROM for TCG firmware enhancements and for user data and keys
- Advanced Crypto Engine (ACE) with RSA support up to 2048-bit key length
- Hardware accelerator for SHA-1 hash algorithm
- True Random Number Generator (TRNG)
- Tick counter with tamper detection
- Protection against Dictionary Attack
- Intel® Trusted Execution Technology Support
- Full personalization with Endorsement Key (EK) and EK certificate

2.10 Board Interfaces

2.10.1 Front Panel LEDs

The CP6002 is equipped with two IPMI LEDs (I0 and I1), one Watchdog Status LED (WD LED), one Temperature Status LED (TH LED), one Hot Swap LED (HS LED) and up to four Ethernet LEDs. Their functionality is described in the following chapters and reflected in the registers (except for the I0 and I1 LEDs) mentioned in Chapter 4, Configuration.

2.10.1.1 IPMI and Hot Swap LEDs

The IPMI LEDs I0 and I1 show the software status of the IPMI controller. The Hot Swap LED indicates when the board may be extracted. It can be switched on or off by software and may be used, for example, to indicate that the shutdown process is finished and the board is ready for extraction.

The following table indicates the function of the IPMI LEDs and the Hot Swap LED.

Table 2-2: IPMI and Hot Swap LEDs Function

LED	COLOR	STATE	NORMAL MODE	OVERRIDE MODE
LED I0	green	off	BMC operating	By user: Only lamp test
		slow blinking	BMC request attention of the SMS/SMM	
		fast blinking	Send/receive data through the IPMB bus	
		on steady	BMC not operating	
LED I1	green	off	BMC not operating	By user: Only lamp test
		slow blinking	BMC heart beat	
		fast blinking	Send/receive data through the KCS interface	
		on steady	Health error detected	
HS LED (Hot Swap LED)	blue	on	a) Board ready for hot swap extraction, or b) Board has just been inserted in a powered system	By SMS/SMM: On, Off, Slow / Fast Blinking By user: Only lamp test
		blinking	Board hot swap in progress; board not ready for extraction	
		off	Board is in normal operation (do not extract the module)	

2.10.1.2 Watchdog and Temperature Status LEDs

The CP6002 provides one Watchdog Status LED (WD LED) and one Temperature Status LED (TH LED).

Note ...

If the TH LED flashes at regular intervals, it indicates that the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Upon assertion of Thermtrip, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature.

Once activated, Thermtrip remains latched until a cold restart of the CP6002 is undertaken (all power off and then on again).

Table 2-3: Watchdog and Temperature Status LEDs Function

LED	COLOR	FUNCTION DURING BOOT-UP	FUNCTION AFTER BOOT-UP
WD LED	green	The WD LED is not lit during boot-up.	Watchdog Status The WD LED states are: • Off: Watchdog inactive • On: Watchdog active, waiting to be triggered • Blinking: Watchdog expired
TH LED	green	The TH LED is not lit during boot-up.	Temperature Status The TH LED states are: • Off: If the CPU and chipset temperature is below the maximum die temperature • On: In case of overtemperature of the CPU, i.e. the CPU has reached a temperature above the maximum die temperature • Blinking: If the CPU has been shut off, i.e. the CPU has reached a temperature above 125°C. In this event, all debug LEDs (LED3..LED0) are red as well.

2.10.2 DIP Switches SW1, SW2 and SW3

The CP6002 is equipped with one 4-bit DIP switch, SW1, and two 2-bit DIP switches, SW2 and SW3, which enable the board to be configured according to the application requirements. DIP Switch SW1 is used for uEFI BIOS boot configuration. DIP Switch SW2 is used for configuring the CompactPCI interface. DIP Switch SW3 is used for configuring the PMC interface.

Table 2-4: DIP Switch SW1 Function

SWITCH	FUNCTION
1	POST Code indication
2	SPI Flash boot selection
3	Reserved
4	Clear uEFI BIOS settings

Table 2-5: DIP Switch SW2 Function

SWITCH	FUNCTION
1	PCI frequency of the CompactPCI interface
2	PCI/PCI-X mode of the CompactPCI interface

Table 2-6: DIP Switch SW3 Function

SWITCH	FUNCTION
1	PCI/PCI-X frequency multiplier configuration
2	PCI/PCI-X mode of the PMC interface

For further information on the configuration of the DIP switches, refer to Chapter 4.1, “DIP Switches SW1, SW2 and SW3 Configuration”.

2.10.3 USB Interfaces

The CP6002 supports six USB 2.0 ports: two on the front I/O, and four on the rear I/O. On the four rear I/O ports it is strongly recommended to use a cable below 3 metres in length for USB 2.0 devices. All seven ports are high-speed, full-speed, and low-speed capable.

One USB peripheral may be connected to each port. For connecting more USB devices to the CP6002 than there are available ports, an external USB hub is required.

Note ...

The USB host interfaces can be used with maximum 500 mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short-circuit protection is provided. All the signal lines are EMI-filtered.

2.10.3.1 USB Connectors J6 and J7

The CP6002 has two USB 2.0 interfaces that are implemented as two 4-pin, type A USB connectors on the front panel, J6 and J7, with the following pinout:

Figure 2-1: USB Con. J6 and J7

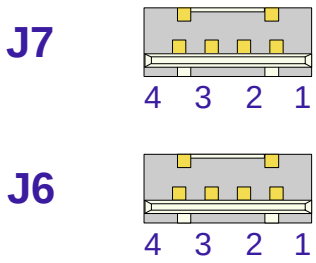


Table 2-7: USB Con. J6 and J7 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	VCC	VCC	--
2	UV0-	Differential USB-	I/O
3	UV0+	Differential USB+	I/O
4	GND	GND	--

2.10.4 Integrated Graphics Controller

The processor includes a highly integrated graphics accelerator delivering high-performance 3D and 2D graphics capabilities. The internal graphics controller has two independent display pipes allowing for support of two independent display screens.

Integrated 3D and 2D graphics:

- Intel® Dynamic Video Memory Technology
- Intel® Graphics Performance Modulation Technology
- Intel® Smart 2D Display Technology
- Full hardware acceleration for MPEG-2, VC-1 and AVC
- DirectX 10 support
- OpenGL 2.1 support
- 1 x DisplayPort interface with 2560 x 1600 pixels @ 60 Hz
- 2 x HDMI/DVI display interface with 1920 x 1200 pixels @ 60 Hz
- 1 x CRT display interface with 2048 x 1536 pixels with 32-bit color @ 75 Hz

2.10.4.1 Graphics Memory Usage

The processor supports the Dynamic Video Memory Technology (Intel® DVMT) with up to 352 MB memory. This technology ensures the most efficient use of all available memory for maximum 3D graphics performance. DVMT dynamically responds to application requirements allocating display and texturing memory resources as required.

2.10.4.2 Analog VGA Connector (CP6002-R1)

The CP6002-R1 provides on the front panel one 15-pin female connector, J12, used to connect an analog VGA monitor.

Figure 2-2: D-Sub VGA Con. J12

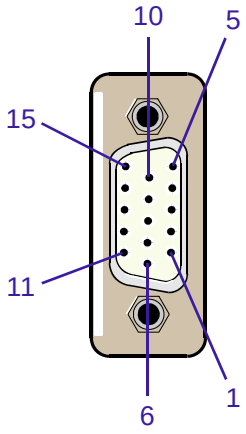


Table 2-8: D-Sub VGA Connector J12 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	Red	Red video signal output	O
2	Green	Green video signal output	O
3	Blue	Blue video signal output	O
13	Hsync	Horizontal sync.	TTL Out
14	Vsync	Vertical sync.	TTL Out
12	Sdata	I^2C data (EDID)	I/O
15	Sclk	I^2C clock (EDID)	I/O
9	VCC	Power +5V, 1.5 A fuse protection	O
5,6,7,8,10	GND	Ground signal	--
4,11	NC	--	--

Note ...

If the automatic VGA detection mechanism on the CP6002 is used, the user must ensure that the VGA cable and the connected monitor have a Ground signal on pin 10. Otherwise the interface is not operable.

Note ...

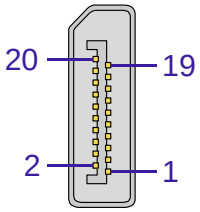
The VGA interface can be used both on the front panel and on the rear I/O. However, the VGA signals are switched to front I/O or rear I/O, depending on the uEFI BIOS setting.

2.10.4.3 DisplayPort Interface (CP6002-R1-MC and CP6002-R2-MC)

The CP6002-R1-MC and the CP6002-R2-MC provide one DisplayPort interface implemented as a 20-pin DisplayPort connector, J8, on the front panel. Additionally, the Intel® QM57 chipset provides a DisplayPort interoperability support for CRT/DVI/HDMI displays through a cable adapter.

The following figure illustrates the DisplayPort connector J8.

Figure 2-3: DisplayPort Connector J8



The following table indicates the pinout of the DisplayPort connector J8.

Table 2-9: DisplayPort Connector J8 Pinout

I/O	FUNCTION	SIGNAL	PIN		SIGNAL	FUNCTION	I/O
--	Power 3.3 V, 0.5 A fuse protection	PWR	20	19	RETURN	Return for power	--
I	Hot Plug Detect	HP_DET	18	17	AUX_CH-	Auxiliary Channel-	I/O
--	Signal ground	GND	16	15	AUX_CH+	Auxiliary Channel+	I/O
--	Signal ground	GND	14	13	HDMI_SEL	DP/HDMI/DVI Select	I
--	Signal ground	GND	12	11	ML(3)-	Data Lane3-	O
O	Data Lane3+	ML(3)+	10	9	GND	Signal ground	--
O	Data Lane2-	ML(2)-	8	7	ML(2)+	Data Lane2+	O
--	Signal ground	GND	6	5	ML(1)-	Data Lane1-	O
O	Data Lane1+	ML(1)+	4	3	ML(0)-	Data Lane0-	O
--	Signal ground	GND	2	1	ML(0)+	Data Lane0+	O

2.10.5 COM Ports

The CP6002 provides two COM ports, COM1 and COM2. COM1 is available on the front panel as a serial RS-232, 8-pin, RJ-45 connector (on CP6002-R1 only), J9, and on the rear I/O simultaneously. COM2 is only available as an RS-422 interface on the rear I/O.

COM1 and COM2 are fully compatible with the 16550 controller. The rear I/O COM1 port includes a complete set of handshaking and modem control signals. The COM1 and COM2 ports provide maskable interrupt generation. The data transfer on the COM ports is up to 115.2 kbit/s.

The following figure and table provide pinout information for the serial connector J9 (COM1).

Figure 2-4: Serial Con. J9 (COM1)

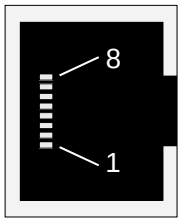


Table 2-10: Serial Con. J9 (COM1) Pinout

PIN	SIGNAL	FUNCTION	I/O
1	RTS	Request to send	O
2	DTR	Data terminal ready	O
3	TXD	Transmit data	O
4	GND	Signal ground	--
5	GND	Signal ground	--
6	RXD	Receive data	I
7	DSR	Data set ready	I
8	CTS	Clear to send	I

Note ...

COM1 can be used either on the front panel or on the rear I/O. It is not possible to use COM1 on the front panel and the rear I/O simultaneously.

Note ...

The CP6002 provides two jumpers, JP2 and JP3, used to activate the bus termination for the RS-422 (COM2) port.

For further information on the JP2 and JP3 jumpers, refer to Chapter 4.2, Jumper Description.

2.10.6 Gigabit Ethernet

The CP6002 board provides up to four 10Base-T/100Base-TX/1000Base-T Ethernet interfaces. They are based on up to four Intel® 82574L Gigabit Ethernet controllers, which are all connected to the PCI Express interface.

The controllers support auto-negotiation (automatic speed detection), auto MDI-X (automatic wire switching), and boot from LAN.

Up to two Gigabit Ethernet ports are available on the front panel as RJ-45 connectors (one on CP6002-R1-MC and CP6002-R2-MC; two on CP6002-R1), and two Gigabit Ethernet ports are available on the rear I/O in accordance with the PICMG 2.16 specification.

Figure 2-5: GbE Con. J10 and J11

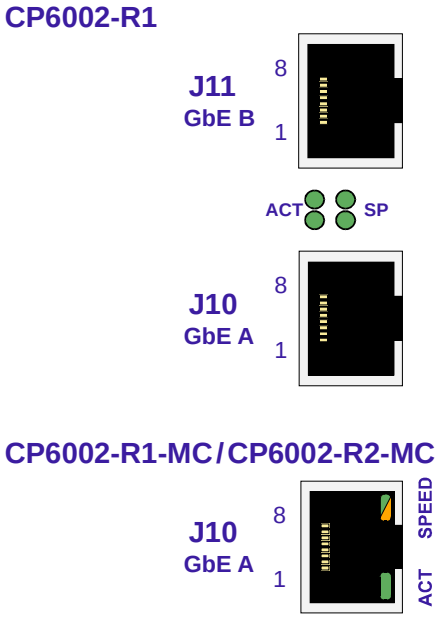


Table 2-11: Pinout of GbE Con. J10 and J11

PIN	MDI / STANDARD ETHERNET CABLE					
	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-	-	I/O	BI_DC+
5	-	-	-	-	I/O	BI_DC-
6	I	RX-	I	RX-	I/O	BI_DB-
7	-	-	-	-	I/O	BI_DD+
8	-	-	-	-	I/O	BI_DD-

Note ...

The Ethernet transmission can operate effectively using a CAT5 cable with a maximum length of 100 m.

Ethernet LED Status

Ethernet LEDs on CP6002-R1:

ACT (green): This LED monitors network connection and activity. When this LED is lit, it means that a link has been established. The LED blinks when network packets are sent or received through the RJ-45 port. When this LED is not lit, there is no link established.

SPEED (green): This LED lights up to indicate a successful 1000Base-T connection. When not lit and the ACT LED is active, the connection is operating at 10Base-T or 100Base-TX.

Ethernet LEDs on CP6002-R1-MC and CP6002-R2-MC:

ACT (green): This LED monitors network connection and activity. When this LED is lit, it means that a link has been established. The LED blinks when network packets are sent or received through the RJ-45 port. When this LED is not lit, there is no link established.

SPEED (green/orange/off): This LED lights up to indicate a successful 100Base-TX or 1000Base-T connection. When green it indicates a 100Base-TX connection and when orange it indicates a 1000Base-TX connection. When not lit and the ACT LED is active, the connection is operating at 10Base-T.

2.10.7 Serial ATA Interface

The CP6002 provides six Serial ATA (SATA) interfaces with RAID support (0,1,5,10). Two interfaces are used for onboard devices and four SATA interfaces are available only on the rear I/O.

The onboard SATA interfaces support SATA I (1.5 Gbit/sec) and SATA II (3.0 Gbit/sec).

One onboard SATA interface is used to support a CompactFlash card. The other onboard SATA interface is used to support either a 2.5" HDD/SSD or the SATA Flash module. The 2.5" HDD/SSD is connected to the board via the CP6001-EXT-SATA module and the onboard connector J19. The SATA Flash module is connected to the board via the onboard connector J18. If both SATA devices are installed, the SATA Flash module is activated.

For further information on the CP6001-EXT-SATA, refer to Appendix A. For further information on the SATA Flash Module, refer to Appendix B.

2.10.8 PMC Interface

The CP6002 provides up to two PMC/XMC slots, A and B. The PCI/PCI-X interface used for the PMCs is realized via a dedicated PCI Express-to-PCI-X bridge. This interface is configurable for either 64-bit/66 MHz PCI or 64-bit/100 MHz PCI-X operation and is compliant with the IEEE 1386.1-2001 specification, which defines a PCI electrical interface for the CMC (Common Mezzanine Card) form factor. The board provides only 3.3V PMC PCI/PCI-X signaling environment.

The PMC module installed in slot A is connected to the CP6002 via the connectors J25 - J28 (Jn1 - Jn4). The PMC module installed in slot B is connected to the CP6002 via the connectors J21 - J23 (Jn1 - Jn3). The Jn1 and Jn2 connectors provide the signals for the 32-bit PCI bus. The 64-bit extension for the PMC interface is supported by the Jn3 connector. User-defined I/O signals are supported on Jn4 and are connected to the CompactPCI rear I/O connector J4.

Note ...

Due to the fact that the PMC rear I/O pinout supports only low-speed signals, the Kontron SCSI PMC board (PMC 261) cannot be used on the rear I/O.

Note ...

It is not possible to operate a PMC device in slot A if an XMC device is operated in slot B. Refer to Chapter 3.5.5, for further information on the PMC/XMC installation possibilities.

The PCI Express-to-PCI-X bridge detects the PCI mode (PCI or PCI-X) and the bus speed (33 MHz, 66 MHz or 100 MHz) via two PCI control signals: PCIXCAP on Jn1 (pin 39) and M66EN on Jn2 (pin 47). The following configurations are supported by the PMC interface.

Table 2-12: PMC PCI/PCI-X Configuration

FREQUENCY	MODE	M66EN Jn2, PIN 47	PCIXCAP Jn1, PIN 39	DIP SWITCH SW3 SWITCH 1
33 MHz	PCI	Low	Low	OFF
66 MHz	PCI	High	Low	OFF
66 MHz	PCI-X	--	Pull-down resistor	OFF
100 MHz	PCI-X	--	High	ON

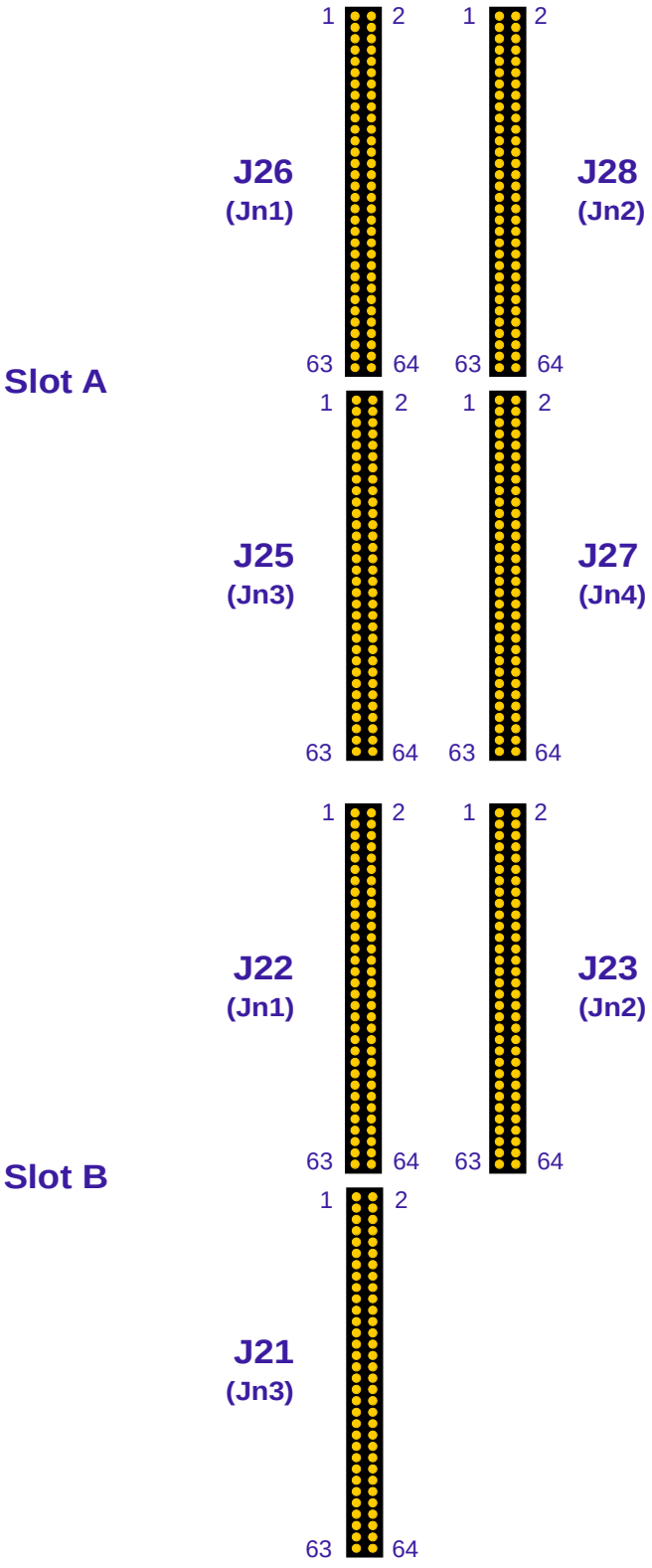
The default configuration of the DIP switch SW3, switch 1, is off. If this switch is set to off, the PCI/PCI-X interface frequency is 33 MHz or 66 MHz.

Warning!

DIP switch SW3, switch 1, must be set in accordance with Table 2-12.

Failure to comply with the above will cause unexpected system error due to non-compliance of the PMC subsystem with the PCI-X specification.

Figure 2-6: PMC Connectors



2.10.8.1 PMC Connectors Pinout

Table 2-13: PMC Connectors Jn1 (J22, J26) and Jn2 (J23, J28) Pinout

J22 and J26 (Jn1)				J23 and J28 (Jn2)			
SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL
TCK (pull-up)	1	2	-12V	+12V	1	2	TRST# (pull-down)
Ground	3	4	INTA#	TMS (pull-up)	3	4	TDO (NC)
INTB#	5	6	INTC#	TDI (pull-up)	5	6	Ground
BUSMODE1# (NC)	7	8	+5V	Ground	7	8	PCI-RSV (NC)
INTD#	9	10	PCI-RSV (NC)	PCI-RSV (NC)	9	10	PCI-RSV (NC)
Ground	11	12	3V3-AUX (NC)	BUSMODE2# (pull-up)	11	12	+3.3V
CLK	13	14	Ground	RST#	13	14	BUSMODE3# (GND)
Ground	15	16	GNT#	+3.3V	15	16	BUSMODE4# (GND)
REQ#	17	18	+5V	RSV	17	18	Ground
V (I/O)	19	20	AD[31]	AD[30]	19	20	AD[29]
AD[28]	21	22	AD[27]	Ground	21	22	AD[26]
AD[25]	23	24	Ground	AD[24]	23	24	+3.3V
Ground	25	26	C/BE[3]	IDSEL	25	26	AD[23]
AD[22]	27	28	AD[21]	+3.3V	27	28	AD[20]
AD[19]	29	30	+5V	AD[18]	29	30	Ground
V (I/O)	31	32	AD[17]	AD[16]	31	32	C/BE[2]#
FRAME#	33	34	Ground	Ground	33	34	PMC-RSV (NC)
Ground	35	36	IRDY#	TRDY#	35	36	+3.3V
DEVSEL#	37	38	+5V	Ground	37	38	STOP#
PCIXCAP	39	40	LOCK#	PERR#	39	40	Ground
PCI-RSV (NC)	41	42	PCI-RSV (NC)	+3.3V	41	42	SERR#
PAR	43	44	Ground	C/BE[1]#	43	44	Ground
V (I/O)	45	46	AD[15]	AD[14]	45	46	AD[13]
AD[12]	47	48	AD[11]	M66EN	47	48	AD[10]
AD[09]	49	50	+5V	AD[08]	49	50	+3.3V
Ground	51	52	C/BE[0]#	AD[07]	51	52	PMC-RSV (NC)
AD[06]	53	54	AD[05]	+3.3V	53	54	PMC-RSV (NC)
AD[04]	55	56	Ground	PMC-RSV (NC)	55	56	Ground
V (I/O)	57	58	AD[03]	PMC-RSV (NC)	57	58	PMC-RSV (NC)
AD[02]	59	60	AD[01]	Ground	59	60	PMC-RSV (NC)
AD[00]	61	62	+5V	ACK64#	61	62	+3.3V
Ground	63	64	REQ64#	Ground	63	64	PMC-RSV (NC)

Table 2-14: PMC Connectors Jn3 (J21, J25) and Jn4 (J27) Pinout

J21 and J25 (Jn3)				J27 (Jn4)			
SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL
PCI-RSV (NC)	1	2	Ground	Rear I/O	1	2	Rear I/O
Ground	3	4	C/BE[7]	Rear I/O	3	4	Rear I/O
C/BE[6]	5	6	C/BE[5]	Rear I/O	5	6	Rear I/O
C/BE[4]	7	8	Ground	Rear I/O	7	8	Rear I/O
V(I/O)	9	10	PAR64	Rear I/O	9	10	Rear I/O
AD[63]	11	12	AD[62]	Rear I/O	11	12	Rear I/O
AD[61]	13	14	Ground	Rear I/O	13	14	Rear I/O
Ground	15	16	AD[60]	Rear I/O	15	16	Rear I/O
AD[59]	17	18	AD[58]	Rear I/O	17	18	Rear I/O
AD[57]	19	20	Ground	Rear I/O	19	20	Rear I/O
V(I/O)	21	22	AD[56]	Rear I/O	21	22	Rear I/O
AD[55]	23	24	AD[54]	Rear I/O	23	24	Rear I/O
AD[53]	25	26	Ground	Rear I/O	25	26	Rear I/O
Ground	27	28	AD[52]	Rear I/O	27	28	Rear I/O
AD[51]	29	30	AD[50]	Rear I/O	29	30	Rear I/O
AD[49]	31	32	Ground	Rear I/O	31	32	Rear I/O
Ground	33	34	AD[48]	Rear I/O	33	34	Rear I/O
AD[47]	35	36	AD[46]	Rear I/O	35	36	Rear I/O
AD[45]	37	38	Ground	Rear I/O	37	38	Rear I/O
V(I/O)	39	40	AD[44]	Rear I/O	39	40	Rear I/O
AD[43]	41	42	AD[42]	Rear I/O	41	42	Rear I/O
AD[41]	43	44	Ground	Rear I/O	43	44	Rear I/O
Ground	45	46	AD[40]	Rear I/O	45	46	Rear I/O
AD[39]	47	48	AD[38]	Rear I/O	47	48	Rear I/O
AD[37]	49	50	Ground	Rear I/O	49	50	Rear I/O
Ground	51	52	AD[36]	Rear I/O	51	52	Rear I/O
AD[35]	53	54	AD[34]	Rear I/O	53	54	Rear I/O
AD[33]	55	56	Ground	Rear I/O	55	56	Rear I/O
V(I/O)	57	58	AD[32]	Rear I/O	57	58	Rear I/O
PCI-RSV (NC)	59	60	PCI-RSV (NC)	Rear I/O	59	60	Rear I/O
PCI-RSV (NC)	61	62	Ground	Rear I/O	61	62	Rear I/O
Ground	63	64	PCI-RSV (NC)	Rear I/O	63	64	Rear I/O

Note ...

The signals from the J27 (Jn4) PMC connector are routed to the J4 CompactPCI rear I/O connector in such a way that they can only be used for low-speed signals.

2.10.9 XMC Interface

The CP6002 provides up to two PMC/XMC slots, A and B, for installing up to two XMC modules via the XMC connectors (P15) J20 and J24. The board uses up to two x8 PCI Express 2.0 interfaces operating at 2.5 GT/s and compliant with the ANSI/VITA 42.0 and ANSI/VITA 42.3 specifications. User-defined I/O signals are also supported on PMC/XMC slot A via the PMC connector J27 (Jn4) and are connected to the CompactPCI rear I/O connector J4.

Note ...

Only XMC modules with one board-to-board connector (P15) can be used with the CP6002.

Figure 2-7: XMC Con. J20 and J24

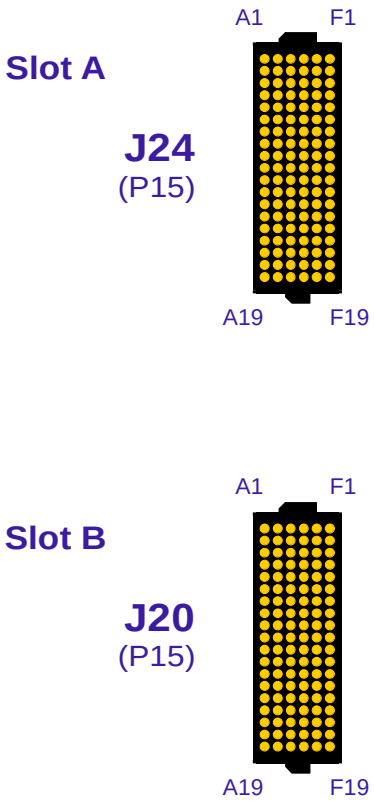


Table 2-15: XMC Connector J20 and J24 Pinout

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR
4	GND	GND	TCK	GND	GND	MRSTO#
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR
6	GND	GND	TMS	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR
8	GND	GND	TDI	GND	GND	-12V
9	NC (RFU)	NC (RFU)	NC (RFU)	NC (RFU)	NC (RFU)	VPWR
10	GND	GND	NC (TDO)	GND	GND	GA0
11	PER0p0	PER0n0	NC (MBIST#)	PER0p1	PER0n1	VPWR
12	GND	GND	GA1	GND	GND	MPRE-SENT#
13	PER0p2	PER0n2	3.3V AUX	PER0p3	PER0n3	VPWR
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	NC (RFU)	PER0p5	PER0n5	VPWR
16	GND	GND	NC (MVMRO)	GND	GND	MSCL
17	PER0p6	PER0n6	NC (RFU)	PER0p7	PER0n7	NC (RFU)
18	GND	GND	NC (RFU)	GND	GND	NC (RFU)
19	CLK+0	CLK-0	NC (RFU)	NC (WAKE#)	ROOT0#	NC (RFU)

Legend:

RFU Reserved for future use

VPWR 5V power supply for the XMC module

2.10.10 Debug Interface

The CP6002 provides several onboard options for hardware and software debugging, such as:

- Four bicolor debug LEDs (DLED0..3), which indicate hardware failures, uEFI BIOS POST codes and user-configurable outputs
- One JTAG connector, J15, for programming the onboard logic
- One XDP-SFF, processor JTAG connector, J30, for facilitating the debug and uEFI BIOS software development

2.10.11 CompactPCI Interface

The CP6002 supports a flexibly configurable, hot swap CompactPCI interface. In the system slot the PCI/PCI-X interface is in the transparent mode, and in the peripheral slot the CompactPCI interface is isolated so that it cannot communicate with the CompactPCI bus. This mode is known as "passive mode".

2.10.11.1 Board Functionality when Installed in System Slot

In a system slot, the CompactPCI interface can be either a 64-bit/66 MHz PCI or PCI-X interface via a dedicated PCI Express-to-PCI-X bridge from Pericom (PI7C9X130).

The CP6002 supports up to seven peripheral slots with 33 MHz and up to 4 peripheral slots with 66 MHz through a backplane.

The PCI Express-to-PCI-X bridge detects the PCI mode (PCI or PCI-X) and the bus speed (33 MHz or 66 MHz) via two PCI control signals on J1: PCIXCAP (pin B16) and M66EN (pin D21). The following configurations are supported by the CompactPCI interface.

Table 2-16: CompactPCI PCI/PCI-X Configuration

FREQUENCY	MODE	M66EN J1, PIN D21	PCIXCAP J1, PIN B16	DIP SWITCH SW2 SWITCH 1	DIP SWITCH SW2 SWITCH 2
33 MHz	PCI	Low	Low	OFF	OFF
33 MHz	PCI	--	Low	OFF	ON
66 MHz	PCI	High	Low	OFF	OFF
66 MHz	PCI	High	--	ON	OFF
66 MHz	PCI-X	--	Pull-down resistor	OFF	OFF

Note ...

To support 66 MHz PCI/PCI-X frequency, the CompactPCI signaling voltage (VI/O) must be 3.3 V.

The CP6002 provides automatic voltage detection for the VI/O to switch the PCI frequency to 33 MHz in an 5V environment.

2.10.11.2 Board Functionality when Installed in Peripheral Slot (Passive Mode)

In a peripheral slot, the board receives power but does not communicate on the CompactPCI bus; all CompactPCI signals are isolated.

In this configuration, the communication is achieved via the two Gigabit Ethernet ports as defined in the PICMG 2.16 specification.

2.10.11.3 Packet Switching Backplane (PICMG 2.16)

The CP6002 supports two Gigabit Ethernet ports on the J3 connector in accordance with the CompactPCI Packet Switching Backplane Specification PICMG 2.16. The two ports are connected in the chassis via the CompactPCI Packet Switching Backplane to the Fabric slots "A" and "B".

The PICMG 2.16 feature can be used in the system slot and in the peripheral slot as well.

2.10.11.4 Hot Swap Support

To ensure that a board may be removed and replaced in a working bus without disturbing the system, the following additional features are required:

- Power ramping
- Precharge
- Hot swap control and status register bits
- Automatic interrupt generation whenever a board is about to be removed or replaced
- A Hot Swap LED to indicate that the board may be safely removed

2.10.11.5 Power Ramping

On the CP6002 a special hot swap controller is used to ramp up the onboard supply voltage. This is done to avoid transients on the +3.3V, +5V, +12V and -12V power supplies from the hot swap system. When the power supply is stable, the hot swap controller generates an onboard reset to put the board into a definite state.

2.10.11.6 Precharge

Precharge is provided on the CP6002 by a resistor on each signal line (PCI bus) connected to a +1V reference voltage.

2.10.11.7 Handle Switch

A microswitch is situated in the extractor handle. The status of the handle is included in the onboard logic. The microswitch is connected to the onboard connector J13.

2.10.11.8 ENUM# Interrupt

If the board is operated in the system slot, the ENUM signal is an input.

2.10.11.9 Hot Swap LED

The blue HS LED can be switched on or off by software. It may be used, for example, to indicate that the shutdown process is finished and the board is ready for extraction.

2.10.12 CompactPCI Bus Connector

The complete CompactPCI connector configuration comprises up to five connectors designated as J1 to J5. Their functions are as follows:

- J1/J2: 64-bit CompactPCI interface with PCI bus signals, arbitration, clock and power
- J3, J4 and J5 have rear I/O interface functionality
- J4 only has optional rear I/O functionality from the PMC module

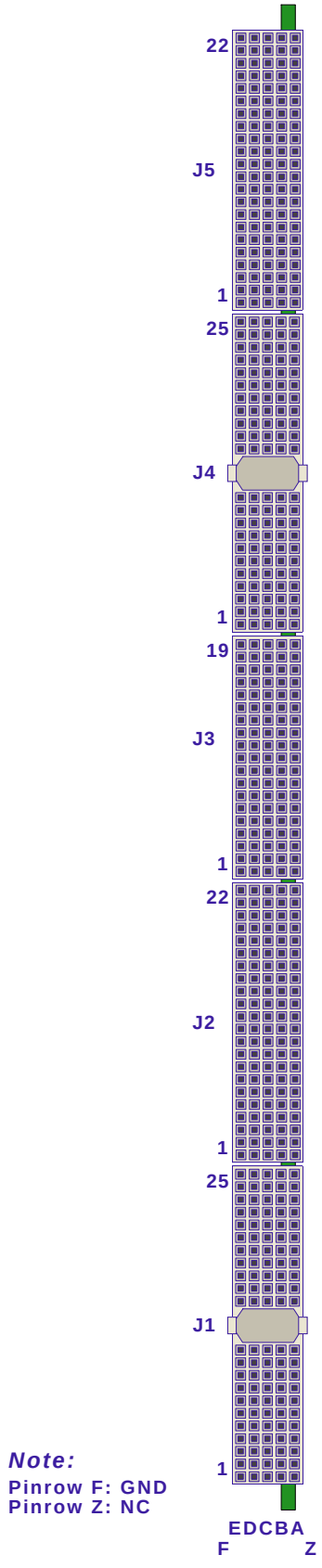
The CP6002 is designed for a CompactPCI bus architecture. The CompactPCI standard is electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

2.10.12.1 CompactPCI Connector Keying

The CompactPCI connectors support guide lugs to ensure a correct polarized mating.

The CP6002 supports universal PCI VI/O signaling voltages with one common termination resistor configuration and includes a PCI VI/O voltage detection circuit. If the PCI VI/O voltage is 5 V, the maximum supported PCI frequency is 33 MHz.

Figure 2-8: CompactPCI Con. J1-J5



2.10.12.2 CompactPCI Connectors J1 and J2 Pinout

The CP6002 is provided with two 2 mm x 2 mm pitch female CompactPCI bus connectors, J1 and J2.

Table 2-17: CompactPCI Bus Connector J1 System Slot Pinout

PIN	Z	A	B	C	D	E	F
25	NC	5V	REQ64#	ENUM#	3.3V	5V	GND
24	NC	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	NC	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	NC	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	NC	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	NC	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	NC	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	NC	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	NC	3.3V	IPMB SCL	IPMB SDA	GND	PERR#	GND
16	NC	DEVSEL#	PCIXCAP	V(I/O)	STOP#	LOCK#	GND
15	NC	3.3V	FRAME#	IRDY#	BDSEL#	TRDY#	GND
14-12	Key Area						
11	NC	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	NC	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	NC	C/BE[3]#	NC	AD[23]	GND	AD[22]	GND
8	NC	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	NC	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	NC	REQ0#	CPCI_Present#	3.3V	CLK0	AD[31]	GND
5	NC	RSV	RSV	RST#	GND	GNT0#	GND
4	NC	IPMB PWR	Health#	V(I/O)	RSV	RSV	GND
3	NC	INTA#	INTB#	INTC#	5V	INTD#	GND
2	NC	TCK	5V	TMS	NC	TDI	GND
1	NC	5V	-12V	TRST#	+12V	5V	GND

Table 2-18: CompactPCI Bus Connector J1 Peripheral Slot Pinout

PIN	Z	A	B	C	D	E	F
25	NC	5V	*	*	3.3V	5V	GND
24	NC	*	5V	V(I/O)	*	*	GND
23	NC	3.3V	*	*	5V	*	GND
22	NC	*	GND	3.3V	*	*	GND
21	NC	3.3V	*	*	*	*	GND
20	NC	*	GND	V(I/O)	*	*	GND
19	NC	3.3V	*	*	GND	*	GND
18	NC	*	GND	3.3V	*	*	GND
17	NC	3.3V	IPMB SCL	IPMB SDA	GND	*	GND
16	NC	*	*	V(I/O)	*	*	GND
15	NC	3.3V	*	*	BDSEL#	*	GND
14-12	Key Area						
11	NC	*	*	*	GND	*	GND
10	NC	*	GND	3.3V	*	*	GND
9	NC	*	NC	*	GND	*	GND
8	NC	*	GND	V(I/O)	*	*	GND
7	NC	*	*	*	GND	*	GND
6	NC	*	CPCI_Present#	3.3V	*	*	GND
5	NC	RSV	RSV	RST#**	GND	*	GND
4	NC	IPMB PWR	Healthy#	V(I/O)	RSV	RSV	GND
3	NC	*	*	*	5V	*	GND
2	NC	TCK	5V	TMS	NC	TDI	GND
1	NC	5V	-12V	TRST#	+12V	5V	GND

Note ...

A * indicates that the signal normally present at this pin is disconnected from the CompactPCI bus when the CP6002 is inserted in a peripheral slot.

** When the CP6002 is inserted in a peripheral slot, the function of the RST# signal can be enabled or disabled.

Table 2-19: 64-bit CompactPCI Bus Connector J2 System Slot Pinout

PIN	Z	A	B	C	D	E	F
22	NC	GA4	GA3	GA2	GA1	GA0	GND
21	NC	CLK6	GND	RSV	RSV	RSV	GND
20	NC	CLK5	GND	RSV	GND	RSV	GND
19	NC	GND	GND	IPMB2_SDA	IPMB2_SCL	IPMB2_Alert	GND
18	NC	RSV	RSV	RSV	GND	RSV	GND
17	NC	RSV	GND	PRST#	REQ6#	GNT6#	GND
16	NC	RSV	RSV	DEG#	GND	RSV	GND
15	NC	RSV	GND	FAL#	REQ5#	GNT5#	GND
14	NC	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	NC	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	NC	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	NC	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	NC	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	NC	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	NC	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	NC	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	NC	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	NC	C/BE[5]#	NC	V(I/O)	C/BE[4]#	PAR64	GND
4	NC	V(I/O)	RSV	C/BE[7]#	GND	C/BE[6]#	GND
3	NC	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	NC	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	NC	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

Table 2-20: 64-bit CompactPCI Bus Connector J2 Peripheral Slot Pinout

PIN	Z	A	B	C	D	E	F
22	NC	GA4	GA3	GA2	GA1	GA0	GND
21	NC	*	GND	RSV	RSV	RSV	GND
20	NC	*	GND	RSV	GND	RSV	GND
19	NC	GND	GND	IPMB2_SDA	IPMB2_SCL	IPMB2_Alert	GND
18	NC	RSV	RSV	RSV	GND	RSV	GND
17	NC	RSV	GND	*	*	*	GND
16	NC	RSV	RSV	DEG#	GND	RSV	GND
15	NC	RSV	GND	FAL#	*	*	GND
14	NC	*	*	*	GND	*	GND
13	NC	*	GND	V(I/O)	*	*	GND
12	NC	*	*	*	GND	*	GND
11	NC	*	GND	V(I/O)	*	*	GND
10	NC	*	*	*	GND	*	GND
9	NC	*	GND	V(I/O)	*	*	GND
8	NC	*	*	*	GND	*	GND
7	NC	*	GND	V(I/O)	*	*	GND
6	NC	*	*	*	GND	*	GND
5	NC	*	NC	V(I/O)	*	*	GND
4	NC	V(I/O)	RSV	*	GND	*	GND
3	NC	*	GND	*	*	*	GND
2	NC	*	*	SYSEN#	*	*	GND
1	NC	*	GND	*	*	*	GND

Note ...

A * indicates that the signal normally present at this pin is disconnected from the CompactPCI bus when the CP6002 is inserted in a peripheral slot.

2.10.12.3 CompactPCI Rear I/O Connectors J3-J5 and Pinout

The CP6002 board provides optional rear I/O connectivity for peripherals. Standard PC interfaces are implemented and assigned to the front panel and to the rear I/O connectors J3, and J5. The J4 connector serves for providing rear I/O interfacing for the PMC module.

When the rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus, the rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the system rear I/O feature a special backplane is necessary. The CP6002 with rear I/O is compatible with all standard 6U CompactPCI passive backplanes with rear I/O support.

The CP6002 conducts all I/O signals through the rear I/O connectors J3, J4 and J5.

Table 2-21: CompactPCI Rear I/O Connector J3 Pinout

PIN	Z	A	B	C	D	E	F
19	NC	RIO_VCC	RIO_VCC	RIO_3.3V	RIO_+12V	RIO_-12V	GND
18	NC	LPa_DA+	LPa_DA-	GND	LPa_DC+	LPa_DC-	GND
17	NC	LPa_DB+	LPa_DB-	GND	LPa_DD+	LPa_DD-	GND
16	NC	LPb_DA+	LPb_DA-	GND	LPb_DC+	LPb_DC-	GND
15	NC	LPb_DB+	LPb_DB-	GND	LPb_DD+	LPb_DD-	GND
14	NC	LPa:LINK	LPb:LINK	LPab:CT1	RSV	FAN:SENSE2	GND
13	NC	LPa:ACT	LPb:ACT	RSV	RSV	FAN:SENSE1	GND
12	NC	RSV	RSV	GND	RSV	RSV	GND
11	NC	RSV	RSV	GND	RSV	RSV	GND
10	NC	USB1:VCC	USB0:VCC	GND	USB3:VCC	USB2:VCC	GND
9	NC	USB1:D-	USB1:D+	GND	USB3:D-	USB3:D+	GND
8	NC	USB0:D-	USB0:D+	GND	USB2:D-	USB2:D+	GND
7	NC	RIO_3.3V	RSV	RIO_ID3	RIO_ID4	SPEAKER	GND
6	NC	VGA:RED	VGA:GREEN	VGA:SDA	DEBUG:CLK	DEBUG:DAT	GND
5	NC	VGA:BLUE	VGA:HSYNC	VGA:VSYNC	VGA:SCL	RSV	GND
4	NC	RSV	RSV	SP1:TX-	SP1:TX+	RSV	GND
3	NC	RSV	RSV	SP1:RX-	SP1:RX+	RSV	GND
2	NC	SP0:RI	SP0:DTR	SP0:CTS	SP0:TX	RSV	GND
1	NC	SP0:RTS	SP0:RX	SP0:DSR	SP0:DCD	RIO_ID1	GND

Warning!

The RIO_XXX signals are power supply **OUTPUTS** to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module.

Failure to comply with the above will result in damage to your board.

The following table describes the signals of the J3 connector.

Table 2-22: CompactPCI Rear I/O Connector J3 Signals

SIGNAL	DESCRIPTION
SP0	COM1 signaling (RS-232)
SP1	COM2 signaling (RS-422)
VGA	Graphic signaling
USB0 to USB3	USB Port signaling
SPEAKER	Standard PC speaker
FAN	Fan speed sensoring
DEBUG	Debug output
LPa	Rear I/O LAN Port A
LPb	Rear I/O LAN Port B

Note ...

The VGA interface can be used both on the front panel and on the rear I/O. However, the VGA signals are switched to front I/O or rear I/O, depending on the uEFI BIOS setting.

Note ...

COM1 can be used either on the front panel or on the rear I/O. It is not possible to use COM1 on the front panel and on the rear I/O simultaneously.

Table 2-23: CompactPCI Rear I/O Connector J4 Pinout

PIN	Z	A	B	C	D	E	F
25	NC	PIM:1	PIM:3	GND	PIM:2	PIM:4	GND
24	NC	PIM:5	PIM:7	GND	PIM:6	PIM:8	GND
23	NC	NC	RIO_VCC	GND	NC	RIO_3.3V	GND
22	NC	PIM:9	PIM:11	GND	PIM:10	PIM:12	GND
21	NC	PIM:13	PIM:15	GND	PIM:14	PIM:16	GND
20	NC	GND	GND	GND	GND	GND	GND
19	NC	PIM:17	PIM:19	GND	PIM:18	PIM:20	GND
18	NC	PIM:21	PIM:23	GND	PIM:22	PIM:24	GND
17	NC	GND	GND	GND	GND	GND	GND
16	NC	PIM:25	PIM:27	GND	PIM:26	PIM:28	GND
15	NC	PIM:29	PIM:31	GND	PIM:30	PIM:32	GND
14 -12	Key Area						
11	NC	PIM:33	PIM:35	GND	PIM:34	PIM:36	GND
10	NC	PIM:37	PIM:39	GND	PIM:38	PIM:40	GND
9	NC	GND	GND	GND	GND	GND	GND
8	NC	PIM:41	PIM:43	GND	PIM:42	PIM:44	GND
7	NC	PIM:45	PIM:47	GND	PIM:46	PIM:48	GND
6	NC	GND	GND	GND	GND	GND	GND
5	NC	PIM:49	PIM:51	GND	PIM:50	PIM:52	GND
4	NC	PIM:53	PIM:55	GND	PIM:54	PIM:56	GND
3	NC	GND	GND	GND	GND	GND	GND
2	NC	PIM:57	PIM:59	GND	PIM:58	PIM:60	GND
1	NC	PIM:61	PIM:63	GND	PIM:62	PIM:64	GND

The signals from the J4 CompactPCI rear I/O connector are routed to the J27 (Jn4) PMC connector in such a way that can only be used for low-speed signals.

Note ...

Due to the fact that the PMC rear I/O pinout supports only low-speed signals, the Kontron SCSI PMC board (PMC 261) cannot be used on the rear I/O.

Table 2-24: CompactPCI Rear I/O Connector J5 Pinout

PIN	Z	A	B	C	D	E	F
22	NC	SATA:LED	PWM1:OUT	GND	PWM2:OUT	BATT (3.0V)	GND
21	NC	HDA:SYNC	HDA:RST	GND	HDA:SDOUT	SYS_WP#	GND
20	NC	RSV (GPIO0)	HDA:SDIN1	GND	RSV (GPIO1)	HDA:SDIN2	GND
19	NC	GND	GND	GND	HDA:SDIN0	HDA:BITCLK	GND
18	NC	HDMI2:D0+	HDMI2:D0-	GND	GND	GND	GND
17	NC	HDMI2:D2+	HDMI2:D2-	GND	HDMI2:D1+	HDMI2:D1-	GND
16	NC	RSV	HDMI2:HPDET	GND	RSV	RSV	GND
15	NC	HDMI2:CLK+	HDMI2:CLK-	GND	HDMI2:SDA	HDMI2:SDC	GND
14	NC	GND	GND	GND	GND	GND	GND
13	NC	HDMI1:D0+	HDMI1:D0-	GND	HDMI1:D1+	HDMI1:D1-	GND
12	NC	HDMI1:D2+	HDMI1:D2-	GND	RSV	RSV	GND
11	NC	RSV	HDMI1:HPDET	GND	HDMI1:SDA	HDMI1:SDC	GND
10	NC	HDMI1:CLK+	HDMI1:CLK-	GND	SMB:SDA	SMB:SCL	GND
9	NC	GND	GND	GND	GND	GND	GND
8	NC	HT3:TX+	HT3:TX-	GND	HT3:RX+	HT3:RX-	GND
7	NC	GND	GND	GND	GND	GND	GND
6	NC	HT2:TX+	HT2:TX-	GND	HT2:RX+	HT2:RX-	GND
5	NC	GND	GND	GND	GND	GND	GND
4	NC	HT1:TX+	HT1:TX-	GND	HT1:RX+	HT1:RX-	GND
3	NC	GND	GND	GND	GND	GND	GND
2	NC	HT0:TX+	HT0:TX-	GND	HT0:RX+	HT0:RX-	GND
1	NC	GND	GND	GND	GND	GND	GND

The following table describes the signals of the J5 connector.

Table 2-25: CompactPCI Rear I/O Connector J5 Signals

SIGNAL	DESCRIPTION
HT0..HT3	SATA Port 0..3 Signaling
SMB	System Management Bus Signaling
HDMI1	HDMI signaling
HDMI2	HDMI signaling
HDA	High-definition audio signaling
PWM	Pulse width modulation output for fan
SATA	Serial ATA LED signaling
GPIO	General purpose digital input/output (on request)
SYS_WP#	System write protection for non-volatile memory devices
BATT (3.0V)	Back-up power input for RTC and CMOS RAM

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Chapter 3

Installation

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3. Installation

The CP6002 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

3.1 Safety Requirements

The following safety precautions must be observed when installing or operating the CP6002. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

Caution!

If your board type is not specifically qualified as being hot swap capable, switch off the CompactPCI system power before installing the board in a free CompactPCI slot. Failure to do so could endanger your life or health and may damage your board or system.

Note...

Certain CompactPCI boards require bus master and/or rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure that your system is provided with an appropriate free slot in which to insert the board.

ESD Equipment!

This CompactPCI board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

3.2 CP6002 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the CP6002 in a system. Procedures for standard removal and hot swap operations are found in their respective chapters.

To perform an initial installation of the CP6002 in a system proceed as follows:

1. Ensure that the safety requirements indicated Chapter 3.1 are observed.

Warning!

Failure to comply with the instruction above may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the CP6002 refer to Chapter 4. For the installation of CP6002 specific peripheral devices and rear I/O devices refer to the appropriate chapters in Chapter 3.

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP6002 nor other system boards are physically damaged by the application of these procedures.

3. To install the CP6002 perform the following:
   1. Ensure that no power is applied to the system before proceeding.

Warning!

Even though power may be removed from the system, the CP6002 front panel cables and, when installed, the RIO transition module front panel cables may have power applied which comes from an external source.

In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins.

It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting).

Kontron disclaims all liability for damages or injuries resulting from failure to comply with the above.

Warning!

When performing the next step, **DO NOT** push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

   2. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.

3. Using both ejector handles, engage the board with the backplane. When the ejector handles are locked, the board is engaged.
4. Fasten the two front panel retaining screws.
5. Connect all external interfacing cables to the board as required.
6. Ensure that the board and all required interfacing cables are properly secured.

The CP6002 is now ready for initial operation. Except for the uEFI BIOS, at this point there is no other software installed. For software installation and further operation of the CP6002, refer to appropriate CP6002 software (uEFI BIOS, BSP, OS), application, and system documentation.

3.3 Standard Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP6002 nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.

Warning!

Even though power may be removed from the system, the CP6002 front panel cables and, when installed, the RIO transition module front panel cables may have power applied which comes from an external source.

In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins.

It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting).

Kontron disclaims all liability for damages or injuries resulting from failure to comply with the above.

3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.

Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.
7. Dispose of the board as required.

3.4 Hot Swap Procedures

While the CP6002 is designed for hot swap operation, hot swapping depends on the type of backplane in use, the system controller's capabilities (if applicable), and the application which controls the hot swapping process.

3.4.1 System Master Hot Swap

Hot swapping of the CP6002 itself when used as the system controller is possible, but will result in any event in a cold start of the CP6002 and consequently a reinitialization of all peripheral boards. Exactly what should or actually transpires in such a situation is a function of the application and is not addressed in this manual. The user must refer to appropriate application documentation for applicable procedures for this case. In any event, the safety requirements above must be observed.

3.4.2 Peripheral Hot Swap Procedure

This procedure assumes that the system supports hot swapping, and that the replacement for the board to be hot swapped is configured hardware- and software-wise for operation in the application. Further, it assumes that the application has performed all functions required to support hot swapping of the CP6002.

Warning!

Do not proceed with the following procedures without being explicitly instructed to do so by the application.

Kontron disclaims all liability for damages or injuries resulting from failure to comply with the above.

To hot swap the CP6002 proceed as follows:

1. Ensure that the safety requirements indicated in Chapter 3.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

Warning!

Care must be taken when applying the procedures below to ensure that neither the CP6002 nor other system boards or application components are physically damaged by the application of these procedures.

2. Unlock both board ejection handles ensuring that the Hot Swap handle has activated the hot swap switch (this occurs with a very small amount of movement of the handle).

Warning!

Once the Hot Swap ejection handle has been unlocked, do not attempt to re-lock this handle.

Re-locking the Hot Swap handle at this time may result in improper operation of the CP6002 or the application, or possibly cause damage to the application system.

Note ...

What actually transpires at this time is a function of the application. In any event, when the Hot Swap ejection handle is opened, the blue HS LED should start to blink and at some point in time (depends on the OS and application) it should transition to being on steady. When the HS LED is on steady, this indicates to the operator that hot swapping of the CP6002 may proceed.

If the blue HS LED does not come on steady, either the system does not support hot swap or a malfunction has occurred. In this event, the application is responsible for handling this situation and must provide the operator with appropriate guidance to remedy the situation.

Warning!

Once the Hot Swap ejection handle has been unlocked, the management controller instructs the payload to prepare for shutdown. Normally the payload will react accordingly and configure itself for shutdown.

In the event the payload does not complete configuring for shutdown within five minutes, the management controller will initiate a forced payload shutdown. In this case, the blue HS LED should transition to steady on shortly thereafter.

3. When the HS LED lights up steady, proceed with the next step of this procedure. If the LED does not light up steady, refer to appropriate application documentation for further action.
4. Disconnect any interfacing cables that may be connected to the board.

Warning!

The CP6002 front panel cables and, when installed, the RIO transition module front panel cables may have power applied which comes from an external source.

In addition, these cables may be connected to devices that can be damaged by electrostatic discharging or short-circuiting of pins.

It is the responsibility of the system designer or integrator to ensure that appropriate measures are taken to preclude damage to the system or injury to personnel which may arise from the handling of these cables (connecting or disconnecting).

Kontron disclaims all liability for damages or injuries resulting from failure to comply with the above.

5. Unscrew the front panel retaining screws.

Warning!

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

6. Using the ejector handles, disengage the board from the backplane and carefully remove it from the system.
7. Dispose of the “old” board as required observing the safety requirements indicated in Chapter 3.1.
8. Obtain the replacement CP6002 board.
9. Connect all required interfacing cables to the board.

Warning!

When performing the next step, **DO NOT** push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

10. Carefully insert the “new” board into the “old” board slot until it makes contact with the backplane connectors.
11. Using both ejector handles, engage the board with the backplane and lock both handles.

Note ...

What actually transpires at this time is a function of the application. In any event, when the Hot Swap ejection handle is closed, the blue HS LED should come on steady, then begin to blink, and at some point in time (depends on the OS and application) it should transition to being off. When the HS LED is off, this indicates that the CP6002 is now operating.

If the blue HS LED remains on steady, the Hot Swap ejection handle is not locked. Lock the handle to proceed.

If the blue HS LED does not stop blinking a malfunction has occurred. In this event, the application is responsible for handling this situation and must provide the operator with appropriate guidance to remedy the situation.

12. Fasten the front panel retaining screws.
    Hot swap of the CP6002 is now complete.

3.5 Installation of CP6002 Peripheral Devices

The CP6002 is designed to accommodate various peripheral devices, such as USB devices, Serial ATA devices, PMC/XMC devices, rear I/O devices, etc. The following figure shows the placement of the SATA Flash module and the CP6001-EXT-SATA module, which is required for connecting an onboard HDD/SSD to the CP6002.

Figure 3-1: CP6002-R1 with Peripheral Devices

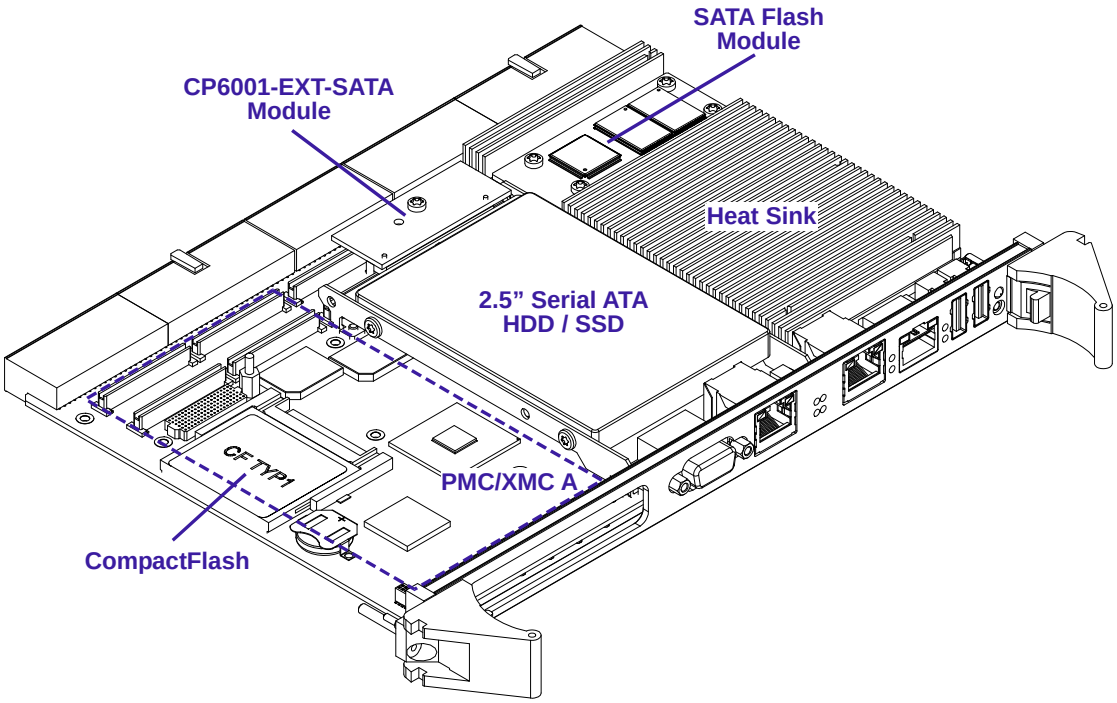


Figure 3-2: CP6002-R1-MC with Peripheral Devices

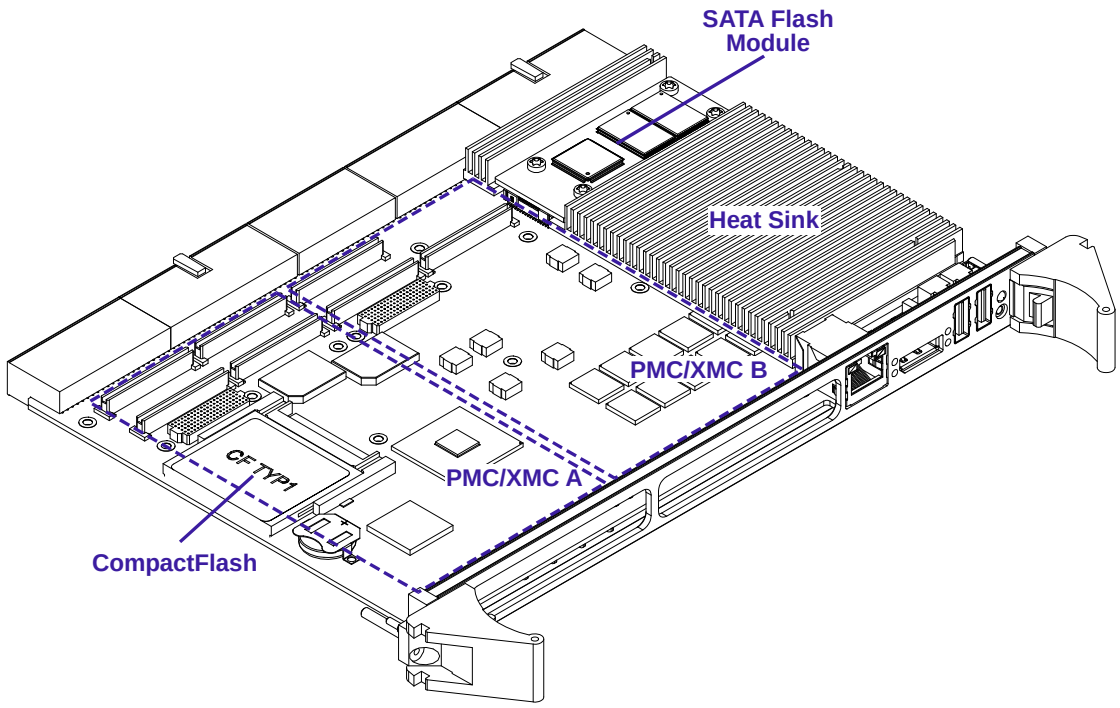
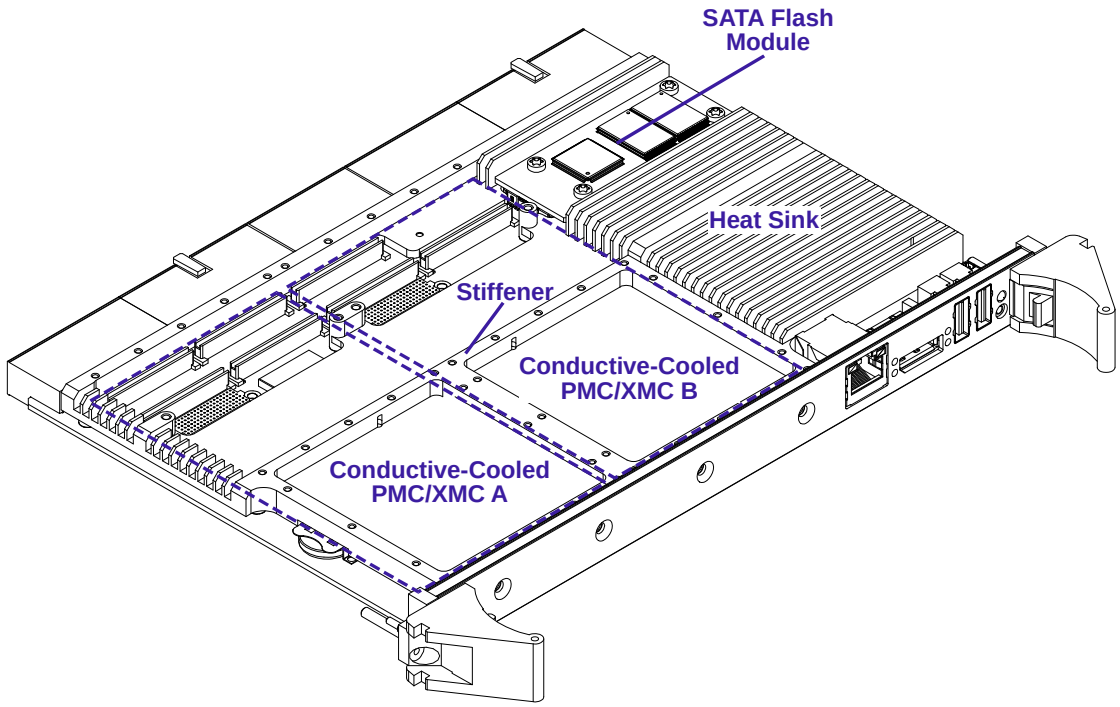


Figure 3-3: CP6002-R2-MC with Peripheral Devices



The following chapters provide information regarding installation aspects of peripheral devices.

3.5.1 USB Device Installation

The CP6002 supports all USB Plug and Play computer peripherals (e.g. keyboard, mouse, printer, etc.).

Note ...

All USB devices may be connected or removed while the host or other peripherals are powered up.

3.5.2 SATA Flash Module Installation

A SATA Flash module may be connected to the CP6002 via the onboard connector, J18.

This optionally available module must be physically installed on the CP6002 prior to installation of the CP6002 in a system.

During installation it is necessary to ensure that the SATA Flash module is properly seated in the onboard connector J18, i.e. the pins are aligned correctly and not bent.

Note ...

Only qualified SATA Flash modules from Kontron are authorized for use with the CP6002. Failure to comply with the above will void the warranty and may result in damage to the board or the system.

3.5.3 CompactFlash Installation

The CompactFlash socket supports all available CompactFlash ATA cards type I and type II.

Note ...

The CP6002 does not support removal and reinsertion of the CompactFlash storage card while the board is in a powered-up state. Connecting the CompactFlash cards while the power is on, which is known as "hot plugging", may damage your system.

3.5.4 Onboard 2.5” HDD/SSD Installation

One 2.5” SATA HDD/SSD may be directly connected to the board via the J19 connector and the adapter module CP6001-EXT-SATA. This module is required to provide Serial ATA interfacing to the HDD/SSD. For further information regarding the CP6001-EXT-SATA module, refer to Appendix A.

3.5.5 PMC/XMC Module Installation

The CP6002 supports the installation of up to two PMC modules and up to two XMC modules, depending on board version.

For the initial installation and standard removal of all PMC/XMC modules, refer to the documentation provided with the module.

Prior to installation or removal, ensure that the safety requirements indicated in Chapter 3.1 of this user guide are observed. Particular attention must be paid to the warning regarding the heat sink!

The following table indicates the installation possibilities of PMC/XMC modules on the CP6002.

Table 3-1: PMC/XMC Module Installation

SLOT A	SLOT B	OPERATION
PMC	PMC	Yes
XMC	XMC	Yes
XMC	PMC	Yes
PMC	XMC	No
Not installed	PMC/XMC	Yes
PMC/XMC	Not installed	Yes

3.5.6 Rear I/O Device Installation

For physical installation of rear I/O devices, refer to the documentation provided with the device itself.

Note ...

COM1 can be used either on the front panel or on rear I/O. It is not possible to use COM1 on the front panel and the rear I/O simultaneously.

3.5.7 Battery Replacement

The CP6002 is provided with a 3.0 V “coin cell” lithium battery for the RTC.

To replace the battery, proceed as follows:

- Turn off power.
- Remove the battery.
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A suitable battery type is CR1632.

Note ...

The user must be aware that the battery's operational temperature range is less than the CP6002's storage temperature range.

For exact range information, refer to the battery manufacturer's specifications.

Note ...

Care must be taken to ensure that the battery is correctly replaced.

The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.

Dispose of used batteries according to the manufacturer's instructions.

The typical life expectancy of a 125 mAh battery (CR1632) is 3 - 4 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.
To ensure that the lifetime of the battery has not been exceeded it is recommended to exchange the battery after 2 - 3 years.

3.6 Software Installation

The installation of the Ethernet and all other onboard peripheral drivers is described in detail in the relevant Driver Kit files.

Installation of an operating system is a function of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.

Note ...

Users working with pre-configured operating system installation images for Plug and Play compliant operating systems, for example Windows® XP, Windows® XP Embedded, must take into consideration that the stepping and revision ID of the chipset and/or other onboard PCI devices may change. Thus, a re-configuration of the operating system installation image deployed for a previous chipset stepping or revision ID is in most cases required. The corresponding operating system will detect new devices according to the Plug and Play configuration rules.

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Chapter 4

Configuration

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4. Configuration

4.1 DIP Switches SW1, SW2 and SW3 Configuration

The CP6002 is equipped with one 4-bit DIP switch, SW1, and two 2-bit DIP switches, SW2 and SW3, which enable the board to be configured according to the application requirements. DIP Switch SW1 is used for uEFI BIOS boot configuration. DIP Switch SW2 is used for configuring the PMC interface. DIP Switch SW3 is used for configuring the CompactPCI interface.

Figure 4-1: DIP Switch SW1

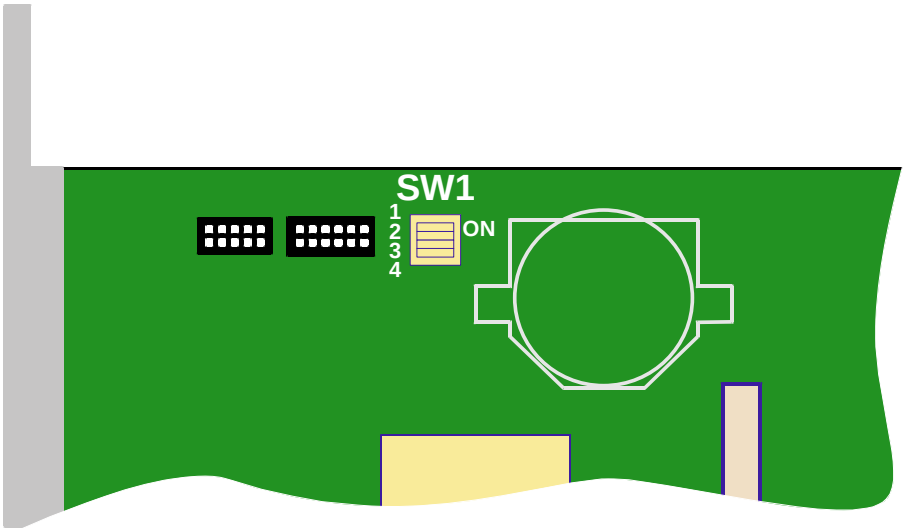

Table 4-1: DIP Switch SW1 for Boot Configuration

SWITCH 1	SETTING	DESCRIPTION
1	*OFF*	*Boot-up with POST Code indication on the DLEDs*
	ON	Boot-up with no POST Code indication on the DLEDs
2	*OFF*	*Boot from default SPI Flash*
	ON	Boot from the alternative SPI Flash
3	*OFF*	Reserved
	ON	
4	*OFF*	*Boot using the currently saved uEFI BIOS settings*
	ON	Clear the uEFI BIOS settings and use the default values

The default settings are indicated by using italic bold.

To clear the uEFI BIOS settings, proceed as follows:

1. Set the DIP Switch SW1, switch 4, to the ON position.
2. Apply power to the system.
3. Wait 30 seconds and then remove power from the system. During this time period no messages are displayed.
4. Set the DIP Switch SW1, switch 4, to the OFF position.

Figure 4-2: DIP Switches SW2 and SW3

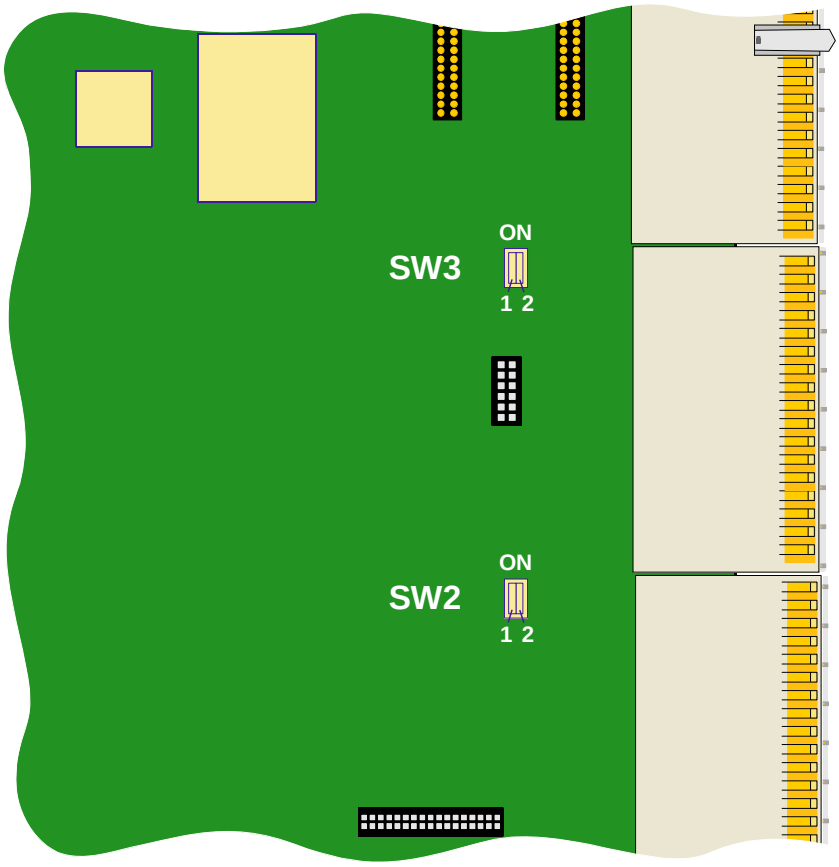

Table 4-2: DIP Switch SW2 for CompactPCI Interface Configuration

SWITCH 1	SETTING	DESCRIPTION
1	*OFF*	*PCI 33 MHz/66 MHz auto detection via the CompactPCI backplane*
	ON	PCI frequency configured to 33 MHz
2	*OFF*	*PCI/PCI-X mode auto detection via the CompactPCI backplane*
	ON	CP6002 configured to PCI mode

Table 4-3: DIP Switch SW3 for PMC Interface Configuration

SWITCH 1	SETTING	DESCRIPTION
1	*OFF*	*PCI/PCI-X frequency multiplier configured to 33 MHz*
	ON	PCI/PCI-X frequency multiplier configured to 25 MHz
2	*OFF*	*PCI/PCI-X mode auto detection via the PMC module*
	ON	PMC interface configured to PCI mode

The default settings of the DIP switches are indicated by using italic bold.

4.2 Jumper Description

The CP6002 has three jumpers JP1, JP2, and JP3. JP1 is reserved for further use. JP2 and JP3 are used to activate the bus termination for COM2. For the location of the jumpers, refer to Figure 1-6.

4.2.1 COM2 Termination Jumper Settings

When COM2 is used and is the last device on the RS-422 bus, then the RS-422 interface must provide termination resistance. The purpose of the jumpers JP2 and JP3 is to enable this line termination resistor (120 ohm).

Table 4-4: JP2 Jumper Setting for RS-422 TXD Termination (COM2)

JP2	DESCRIPTION
Open	*TXD termination inactive*
Closed	TXD termination active (soldered jumper or 0 ohm resistor in 0805 package)

The default setting is indicated by using italic bold.

Table 4-5: JP3 Jumper Setting for RS-422 RXD Termination (COM2)

JP3	DESCRIPTION
Open	*RXD termination inactive*
Closed	RXD termination active (soldered jumper or 0 ohm resistor in 0805 package)

The default setting is indicated by using italic bold.

4.3 I/O Address Map

The following table indicates the CP6002-specific registers. The blue-shaded table cells indicate BMC-specific registers.

Table 4-6: I/O Address Map

ADDRESS	DEVICE
0x080 -	uEFI BIOS POST Code Low Byte Register (POSTL)
0x081	uEFI BIOS POST Code High Byte Register (POSTH)
0x082 - 0x083	Reserved
0x084	Debug Low Byte Register (DBGL)
0x085	Debug High Byte Register (DBGH)
0x280	Status Register 0 (STAT0)
0x281	Status Register 1 (STAT1)
0x282	Control Register 0 (CTRL0)
0x283	Control Register 1 (CTRL1)
0x284	Device Protection Register (DPROT)
0x285	Reset Status Register (RSTAT)
0x286	Board Interrupt Configuration Register (BICFG)
0x287	Status Register 2 (STAT2)
0x288	Board ID High Byte Register (BIDH)
0x289	Board and PLD Revision Register (BREV)
0x28A	Geographic Addressing Register (GEOAD)
0x28B	Reserved
0x28C	Watchdog Timer Control Register (WTIM)
0x28D	Board ID Low Byte Register (BIDL)
0x28E - 0x28F	Reserved
0x290	Debug LED Configuration Register (DLCFG)
0x291	Debug LED Control Register (DLCTRL)
0x292 - 0x29C	Reserved
0x29D	IPMI Controller Status Register 0 (ICSTA0)
0x29E	IPMI Controller Status Register 1 (ICSTA1)
0x29F	IPMI Reset Status Register (IRSTA)
0xCA2; 0xCA3	IPMI KCS interface

4.4 CP6002-Specific Registers

The following registers are special registers which the CP6002 uses to watch the onboard hardware special features and the CompactPCI control signals.

Normally, only the system uEFI BIOS uses these registers, but they are documented here for application use as required.

Note ...
Take care when modifying the contents of these registers as the system uEFI BIOS may be relying on the state of the bits under its control.

4.4.1 Status Register 0 (STAT0)

The Status Register 0 holds general/common status information.

Table 4-7: Status Register 0 (STAT0)

REGISTER NAME		STATUS REGISTER 0 (STAT0)		
ADDRESS		0x280		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	HSHS	Hot swap handle status: 0 = Hot swap handle in closed position 1 = Hot swap handle in open position	N/A	R
6	BBEI	uEFI BIOS boot end indication: 0 = uEFI BIOS is booting 1 = uEFI BIOS boot is finished	0	R
5 - 4	BFSS	Boot Flash selection status: 00 = Primary boot Flash active 01 = Secondary boot Flash active 10 = External boot Flash active 11 = Reserved	N/A	R
3	DIP4	DIP switch SW1, switch 4	N/A	R
2	DIP3	DIP switch SW1, switch 3	N/A	R
1	DIP2	DIP switch SW1, switch 2	N/A	R
0	DIP1	DIP switch SW1, switch 1	N/A	R

4.4.2 Status Register 1 (STAT1)

The Status Register 1 holds board-specific status information.

Table 4-8: Status Register 1 (STAT1)

REGISTER NAME		STATUS REGISTER 1 (STAT1)		
ADDRESS		0x281		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	C66EN	CPCI PCI speed (M66EN signal): 0 = 33 MHz 1 = 66 MHz	N/A	R
6	CVIO	CPCI backplane VI/O voltage configuration: 0 = 3.3V VI/O voltage 1 = 5V VI/O voltage	N/A	R
5	P66EN	PMC PCI speed (M66EN signal): 0 = 33 MHz 1 = 66 MHz	N/A	R
4	Res.	Reserved	0	R
3	CSYS	CPCI system slot identification (SYSEN signal): 0 = Installed in a system slot 1 = Installed in a peripheral slot	0	R
2	CENUM	CPCI system enumeration (ENUM signal): 0 = Indicates the insertion or removal of a hot swap system board 1 = No hot swap event	1	R
1	CFAL	CPCI power supply status (FAL signal): 0 = Power supply failure 1 = Power in normal state	1	R
0	CDEG	CPCI power supply status (DEG signal): 0 = Power derating 1 = Power in normal state	1	R

4.4.3 Control Register 0 (CTRL0)

The Control Register 0 holds one bit for specifying the boot Flash to be updated.

Table 4-9: Control Register 0 (CTRL0)

REGISTER NAME		CONTROL REGISTER 0 (CTRL0)		
ADDRESS		0x282		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 6	VGAM	VGA mode configuration: 00 = Automatic VGA Front Detection 01 = Front VGA (uEFI BIOS default for CP6002-R1) 10 = Rear VGA (uEFI BIOS default for CP6002-R1-MC/CP6002-R2-MC) 11 = VGA disabled	N/A	R/W
5	BFUS	Boot Flash update selection: 0 = Select default boot Flash for update 1 = Select alternative boot Flash for update	0	R/W
4 - 0	Res.	Reserved	00000	R

4.4.4 Control Register 1 (CTRL1)

The Control Register 1 holds board-specific control information.

Table 4-10: Control Register 1 (CTRL1)

REGISTER NAME		CONTROL REGISTER 1 (CTRL1)		
ADDRESS		0x283		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	SRST	SATA Flash module reset: 0 = Reset of SATA Flash module 1 = SATA Flash module running	1	R/W
6	VRST	Integrated graphics controller configuration: 0 = Graphics controller disabled 1 = Graphics controller enabled	1	R
5	Res.	Reserved	0	R
4	CRST	Board reset via CPCI interface when installed in peripheral slot: 0 = Disable board reset via CPCI interface 1 = Enable board reset via CPCI interface	0	R/W
3	XRST	Reset via XMC device: 0 = Disable board reset via XMC device 1 = Enable board reset via XMC device	0	R/W
2-0	Res.	Reserved	000	R

4.4.5 Device Protection Register (DPROT)

The Device Protection Register holds the write protect signals for Flash devices.

Table 4-11: Device Protection Register (DPROT)

REGISTER NAME		DEVICE PROTECTION REGISTER (DPROT)		
ADDRESS		0x284		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 2	Res.	Reserved	000000	R
1	EEWP	EEPROM write protection: 0 = EEPROM not write protected 1 = EEPROM write protected Writing a '1' to this bit sets the bit. If this bit is set, it cannot be cleared.	0	R/W
0	BFWP	Boot Flash write protection: 0 = Boot Flash not write protected 1 = Boot Flash write protected Writing a '1' to this bit sets the bit. If this bit is set, it cannot be cleared.	0	R/W

4.4.6 Reset Status Register (RSTAT)

The Reset Status Register is used to determine the host's reset source.

Table 4-12: Reset Status Register (RSTAT)

REGISTER NAME		RESET STATUS REGISTER (RSTAT)		
ADDRESS		0x285		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	PORS	Power-on reset status: 0 = System reset generated by software (warm reset) 1 = System reset generated by power-on (cold reset) Writing a '1' to this bit clears the bit.	N/A	R/W
6	Res.	Reserved	0	R
5	SRST	Software reset status: 0 = Reset is logged by BMC 1 = Reset is not logged by BMC The uEFI BIOS/software sets this bit to inform the BMC that the next reset should not be logged. Writing a '1' from the host to this bit sets the bit. After setting the bit, it may be cleared via the BMC (using the IPMI Reset Status Register and an I²C access from the BMC to this register by writing a '1' to the SRST bit).	0	R/W
4	Res.	Reserved	0	R
3	IPRS	IPMI controller reset: 0 = System reset not generated by IPMI 1 = System reset generated by IPMI Writing a '1' to this bit clears the bit.	0	R/W
2	FPRS	Front panel push button reset status: 0 = System reset not generated by front panel reset 1 = System reset generated by front panel reset Writing a '1' to this bit clears the bit.	0	R/W
1	CPRS	CompactPCI reset status (PRST signal): 0 = System reset not generated by CPCI reset input 1 = System reset generated by CPCI reset input Writing a '1' to this bit clears the bit.	0	R/W
0	WTRS	Watchdog timer reset status: 0 = System reset not generated by Watchdog timer 1 = System reset generated by Watchdog timer Writing a '1' to this bit clears the bit.	0	R/W

Note ...

The reset status register is set to the default values by power-on reset, not by PCI reset.

4.4.7 Board Interrupt Configuration Register (BICFG)

The Board Interrupt Configuration Register holds a series of bits defining the interrupt routing for the Watchdog. If the Watchdog timer fails, it can generate an IRQ5 interrupt.

The enumeration signal is generated by a hot swap compatible board after insertion and prior to removal. The system uses this interrupt signal to force software to configure the new board. The derate signal indicates that the power supply is beginning to derate its power output.

Table 4-13: Board Interrupt Configuration Register (BICFG)

REGISTER NAME		BOARD INTERRUPT CONFIGURATION REGISTER (BICFG)		
ADDRESS		0x286		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	Res.	Reserved	0	R/W
6	CFICF	CPCI fail signal interrupt configuration (FAL signal): 0 = Disabled 1 = Enabled	0	R/W
5	CEICF	CPCI enumeration signal to IRQ5 routing (ENUM signal): 0 = Disabled 1 = Enabled	0	R/W
4	CDICF	CPCI derate signal to IRQ5 routing (DEG signal): 0 = Disabled 1 = Enabled	0	R/W
3 - 2	KICF	BMC KCS interrupt configuration 00 = Disabled 01 = IRQ11 10 = IRQ10 11 = Reserved	00	R
1 - 0	WICF	Watchdog interrupt configuration: 00 = Disabled 01 = IRQ5 10 = Reserved 11 = Reserved	00	R/W

4.4.8 Status Register 2 (STAT2)

The Status Register 2 holds board-specific status information.

Table 4-14: Status Register 2 (STAT2)

REGISTER NAME		STATUS REGISTER 2 (STAT2)		
ADDRESS		0x287		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 2	Res.	Reserved	000000	R
1	XAP	XMC device in slot A: 0 = Not present 1 = Present	N/A	R
0	XAB	XMC device in slot B: 0 = Not present 1 = Present	N/A	R

4.4.9 Board ID High Byte Register (BIDH)

Each Kontron board is provided with a unique 16-bit board-type identifier in the form of a hexadecimal number. The Board ID High Byte Register is located in the address 0x288. The Board ID Low Byte Register is located in the address 0x28D.

Table 4-15: Board ID High Byte Register (BIDH)

REGISTER NAME		BOARD ID HIGH BYTE REGISTER (BIDH)		
ADDRESS		0x288		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 0	BIDH	Board identification: CP6002-R1/CP6002-R1-MC: 0xB340 CP6002-R2-MC: 0xB341	0xB3	R

4.4.10 Board and PLD Revision Register (BREV)

The Board and PLD Revision Register signals to the software when differences in the board and the Programmable Logic Device (PLD) require different handling by the software. It starts with the value 0x00 and will be incremented with each change in hardware as development continues.

Table 4-16: Board and PLD Revision Register (BREV)

REGISTER NAME		BOARD AND PLD REVISION REGISTER (BREV)		
ADDRESS		0x289		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 4	BREV	Board revision	N/A	R
3 - 0	PREV	PLD revision	N/A	R

4.4.11 Geographic Addressing Register (GEOAD)

This register holds the CompactPCI geographic address (site number) used to assign the Intelligent Platform Management Bus (IPMB) address to the CP6002.

Table 4-17: Geographic Addressing Register (GEOAD)

REGISTER NAME		GEOGRAPHIC ADDRESSING REGISTER (GEOAD)		
ADDRESS		0x28A		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 5	Res.	Reserved	000	R
4 - 0	GA	Geographic address	N/A	R

Note ...

The Geographic Addressing Register is set to the default values by power-on reset, not by PCI reset.

4.4.12 Watchdog Timer Control Register (WTIM)

The CP6002 has one Watchdog timer provided with a programmable timeout ranging from 125 msec to 4096 sec. Failure to strobe the Watchdog timer within a set time period results in a system reset or an interrupt. The interrupt mode can be configured via the Board Interrupt Configuration Register (0x286).

There are four possible modes of operation involving the Watchdog timer:

- Timer only mode
- Reset mode
- Interrupt mode
- Dual stage mode

At power on the Watchdog is not enabled. If not required, it is not necessary to enable it. If required, the bits of the Watchdog Timer Control Register must be set according to the application requirements. To operate the Watchdog, the mode and time period required must first be set and then the Watchdog enabled. Once enabled, the Watchdog can only be disabled or the mode changed by powering down and then up again. To prevent a Watchdog timeout, the Watchdog must be retriggered before timing out. This is done by writing a ’1’ to the WTR bit. In the event a Watchdog timeout does occur, the WTE bit is set to ’1’. What transpires after this depends on the mode selected.

The four operational Watchdog timer modes can be configured by the WMD[1:0] bits, and are described as follows:

Timer only mode - In this mode the Watchdog is enabled using the required timeout period. Normally, the Watchdog is retriggered by writing a ’1’ to the WTR bit. In the event a timeout occurs, the WTE bit is set to ’1’. This bit can then be polled by the application and handled accordingly. To continue using the Watchdog, write a ’1’ to the WTE bit, and then retrigger the Watchdog using WTR. The WTE bit retains its setting as long as no power down-up is done. Therefore, this bit may be used to verify the status of the Watchdog.

Reset mode - This mode is used to force a hard reset in the event of a Watchdog timeout. In addition, the WTE bit is not reset by the hard reset, which makes it available if necessary to determine the status of the Watchdog prior to the reset.

Interrupt mode - This mode causes the generation of an interrupt in the event of a Watchdog timeout. The interrupt handling is a function of the application. If required, the WTE bit can be used to determine if a Watchdog timeout has occurred.

Dual stage mode - This is a complex mode where in the event of a timeout two things occur: 1) an interrupt is generated, and 2) the Watchdog is retriggered automatically. In the event a second timeout occurs immediately following the first timeout, a hard reset will be generated. The second timeout period is the same as the first. If the Watchdog is retriggered normally, operation continues. The interrupt generated at the first timeout is available to the application to handle the first timeout if required. As with all of the other modes, the WTE bit is available for application use.

Table 4-18: Watchdog Timer Control Register (WTIM)

REGISTER NAME		WATCHDOG TIMER CONTROL REGISTER (WTIM)		
ADDRESS		0x28C		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	WTE	Watchdog timer expired status bit 0 = Watchdog timer has not expired 1 = Watchdog timer has expired. Writing a '1' to this bit resets it to 0.	0	R/W
6 - 5	WMD	Watchdog mode 00 = Timer only mode 01 = Reset mode 10 = Interrupt mode 11 = Cascaded mode (dual-stage mode)	00	R/W
4	WEN/WTR	Watchdog enable / Watchdog trigger control bit: 0 = Watchdog timer not enabled Prior to the Watchdog being enabled, this bit is known as WEN. After the Watchdog is enabled, it is known as WTR. Once the Watchdog timer has been enabled, this bit cannot be reset to 0. As long as the Watchdog timer is enabled, it will indicate a '1'. 1 = Watchdog timer enabled Writing a '1' to this bit causes the Watchdog to be retriggered to the timer value indicated by bits WTM[3:0].	0	R/W
3 - 0	WTM	Watchdog timeout settings: 0000 = 0.125 s 0001 = 0.25 s 0010 = 0.5 s 0011 = 1 s 0100 = 2 s 0101 = 4 s 0110 = 8 s 0111 = 16 s 1000 = 32 s 1001 = 64 s 1010 = 128 s 1011 = 256 s 1100 = 512 s 1101 = 1024 s 1110 = 2048 s 1111 = 4096 s	0000	R/W

4.4.13 Board ID Low Byte Register (BIDL)

Each Kontron board is provided with a unique 16-bit board-type identifier in the form of a hexadecimal number. The Board ID Low Byte Register is located in the address 0x28D. The Board ID High Byte Register is located in the address 0x288.

Table 4-19: Board ID Low Byte Register (BIDL)

REGISTER NAME		BOARD ID LOW BYTE REGISTER (BIDL)		
ADDRESS		0x28D		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7 - 0	BIDL	Board identification: CP6002-R1/CP6002-R1-MC: 0xB340 CP6002-R2-MC: 0xB341	N/A	R

4.4.14 Debug LED Configuration Register (DLCFG)

The Debug LED Configuration Register holds a series of bits defining the onboard configuration of the onboard debug LEDs (DLED 0..3). For the location of the debug LEDs, refer to Figure 1-6.

Table 4-20: Debug LED Configuration Register (DLCFG)

REGISTER NAME		DEBUG LED CONFIGURATION REGISTER (DLCFG)		
ADDRESS		0x290		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-4	Res.	Reserved	0000	R
3-0	DLCON	Debug LED Configuration 0000 = POST [1)] 0001 = Mode A [2)] 0010 - 1111 = Reserved	0001	R/W

[1)] In uEFI BIOS POST mode, the Debug LEDs build a binary vector to display uEFI BIOS POST code during the pre-boot phase. In doing so, the higher 4-bit nibble of the 8-bit uEFI BIOS POST code is displayed followed by the lower nibble followed by a pause. uEFI BIOS POST code is displayed in general in green color.

DLED3: POST bit 3 and bit 7 (green)
DLED2: POST bit 2 and bit 6 (green)
DLED1: POST bit 1 and bit 5 (green)
DLED0: POST bit 0 and bit 4 (green)

[2)] Configured for Mode A, the Debug LEDs are dedicated to functions as follows:

DLED3: Debug LED 3 (red/green/red+green)
DLED2: Debug LED 2 (red/green/red+green)
DLED1: Debug LED 1 (red/green/red+green)
DLED0: Debug LED 0 (red/green/red+green)

Besides the configurable functions described above, the Debug LEDs fulfill also a basic debug function during the power-up phase as long as the first access to Port 80 is processed. If an LED lights red and stays red, than a basic error is present on the board. The following debug functions are defined and displayed during this initialization phase.

DLED3: PGOOD, Power Good status not reached (red)
DLED2: CPU catastrophic error (red)
DLED1: RST, PCI reset active / not deactivated (red)
DLED0: uEFI BIOS boot failure (red)

4.4.15 Debug LED Control Register (DLCTRL)

This register is used to switch on and off the Debug LEDs.

Table 4-21: Debug LED Control Register (LCTRL)

REGISTER NAME		DEBUG LED CONTROL REGISTER (DLCTRL)		
ADDRESS		0x291		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7-4	DLCMD	Debug LED command: 0000 = Get DLED 0 0001 = Get DLED 1 0010 = Get DLED 2 0011 = Get DLED 3 0100 - 0111 = Reserved 1000 = Set DLED 0 1001 = Set DLED 1 1010 = Set DLED 2 1011 = Set DLED 3 1100 - 1111 = Reserved	0000	R/W
3-0	DLCOL	Debug LED color: 0000 = Off 0001 = Green 0010 = Red 0011 = Red+green 0100 - 1111 = Reserved	0000	R/W

Note ...

This register can only be used if the Debug LEDs indicated in the “Debug LED Configuration Register” (Table 4-18) are configured in Mode A.

4.5 BMC-Specific Registers

The following registers are special registers which the CP6002 uses to monitor and configure the Board Management Controller.

4.5.1 IPMI Controller Status Register 0 (ICSTA0)

The IPMI Controller Status Register 0 describes the onboard control signals.

Table 4-22: IPMI Controller Status Register 0 (ICSTA0)

REGISTER NAME		IPMI CONTROLLER STATUS REGISTER 0 (ICSTA0)		
ADDRESS		0x29D		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	HFSEL	Boot Flash selection: 0 = Select default boot Flash device 1 = Select alternative boot Flash device	0	R
6 - 3	Res.	Reserved	0000	R
2	HPWRB	Power button signal to PCH: 0 = No power button signal to PCH 1 = Power button signal generated to PCH	0	R
1	HRST	Host reset: 0 = Host controller is running 1 = Host controller is in reset state	0	R
0	HPGD	Power-on host reset (cold reset): 0 = Host controller is running 1 = Host controller is in reset state (cold reset) The power-on host reset resets all FPGA registers and resets the host.	0	R

Note ...

This register can be configured only by the IPMI controller and is set to the default values by power-on reset, not by PCI reset.

4.5.2 IPMI Controller Status Register 1 (ICSTA1)

The IPMI Controller Status Register 1 describes the processor signals.

Table 4-23: IPMI Controller Status Register 1 (ICSTA1)

REGISTER NAME		IPMI CONTROLLER STATUS REGISTER 1 (ICSTA1)		
ADDRESS		0x29E		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	IPCE	Processor catastrophic error (CATERR signal): 0 = Processor is at its normal operating temperature 1 = Processor has experienced a catastrophic error and cannot continue to operate	0	R
6 - 4	Res.	Reserved	000	R
3	IPHOTL	Processor overtemperature detection (PROCHOT signal): 0 = Processor is at its normal operating temperature 1 = Processor was above the safe operating area Writing a '1' from the BMC to this bit clears the bit.	0	R
2	Res.	Reserved	0	R
1	IPTH	Processor critical overtemperature detection (THERMTRIP signal): 0 = Processor is at its normal operating temperature 1 = Processor temperature is above 125°C	0	R
0	IPHOT	Processor overtemperature detection (PROCHOT signal): 0 = Processor is at its normal operating temperature 1 = Processor temperature is above the maximum die temperature	0	R

Note ...

This register can be configured only by the IPMI controller and is set to the default values by power-on reset, not by PCI reset.

4.5.3 IPMI Reset Status Register (IRSTA)

The IPMI Reset Status Register is used to determine the BMC reset source.

Table 4-24: IPMI Reset Status Register (IRSTA)

REGISTER NAME		IPMI RESET STATUS REGISTER (IRSTA)		
ADDRESS		0x29F		
BIT	NAME	DESCRIPTION	RESET VALUE	ACCESS
7	IPORS	Power-on reset detection (IPMI side): 0 = System reset generated by software (warm reset) 1 = System reset generated by power-on (cold reset) This bit may be cleared only by the BMC. Writing a '1' by BMC to this bit clears the bit.	N/A	R
6	Res.	Reserved	0	R
5	SRST	Software reset status: 0 = Reset is logged by the BMC 1 = Reset is not logged by the BMC uEFI BIOS sets the bit to inform the BMC that the next reset should not be logged. This bit can be set only by the host through the use of the RSTAT register (by writing a '1' to the SRST bit). Writing a '1' by BMC to this bit clears the bit.	0	R
4	Res.	Reserved	0	R
3	IPRS	BMC controller reset: 0 = System reset not generated by the BMC 1 = System reset generated by the BMC Writing a '1' by BMC to this bit clears the bit.	0	R
2 - 1	Res.	Reserved	0	R
0	WTRS	Watchdog timer reset status: 0 = System reset not generated by the Watchdog timer 1 = System reset generated by the Watchdog timer Writing a '1' by BMC to this bit clears the bit.	0	R

Note ...

The IPMI Reset Status Register is set to the default values by power-on reset, not by PCI reset.

4.5.4 IPMI Keyboard Controller Style Interface

The host processor communicates with the BMC using one Keyboard Controller Style (KCS) interface, which is defined in the IPMI specification. The KCS interface is on the I/O location 0xCA2 and 0xCA3, and configured as regular ISA interrupt.

Chapter 5

Power Considerations

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5. Power Considerations

5.1 System Power

The considerations presented in the ensuing chapters must be taken into account by system integrators when specifying the CP6002 system environment.

5.1.1 CP6002 Baseboard

The CP6002 baseboard itself has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the CP6002 should be carefully tested to ensure compliance with these ratings.

Table 5-1: Maximum Input Power Voltage Limits

SUPPLY VOLTAGE	MAXIMUM PERMITTED VOLTAGE
+3.3 V	+3.6 V
+5 V	+5.5 V
+12 V	+14.0 V
-12 V	-14.0 V

Warning!

The maximum permitted voltage indicated in the table above must not be exceeded. Failure to comply with the above may result in damage to your board.

The following table specifies the ranges for the different input power voltages within which the board is functional. The CP6002 is not guaranteed to function if the board is not operated within the prescribed limits.

Table 5-2: DC Operational Input Voltage Ranges

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE	RECOMMENDED RANGE
+3.3 V	3.2 V min. to 3.47 V max.	3.3 V min. to 3.47 V max.
+5 V	4.85 V min. to 5.25 V max.	5.0 V min. to 5.25 V max.
+12 V	11.4 V min. to 12.6 V max.	12 V min. to 12.6 V max.
-12 V	-11.4 V min. to -12.6 V max.	Only for PMC/XMC

5.1.2 Backplane

Backplanes to be used with the CP6002 must be adequately specified. The backplane must provide optimal power distribution for the +3.3 V, +5 V and +12 V power inputs.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under-dimensioned cabling or bridges, high resistance connections, etc. must be avoided. It is recommended to use POSITRONIC or M-type connector backplanes and power supplies where possible.

5.1.3 Power Supply Units

Power supplies for the CP6002 must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. An industrial power supply unit should be able to provide at least twice as much power as the entire system requires.

As the design of the CP6002 has been optimized for minimal power consumption, the power supply unit shall be stable even without minimum load.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for backplane input line resistance variations due to temperature changes, etc.

5.1.3.1 Start-Up Requirement

Power supplies must comply with the following guidelines, in order to be used with the CP6002:

- Beginning at 10% of the nominal output voltage, the voltage must rise within > 0.1 ms to < 20 ms to the specified regulation range of the voltage. Typically: > 5 ms to < 15 ms.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.
- The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal Vout.

5.1.3.2 Power-Up Sequence

The +5 VDC output level must always be equal to or higher than the +3.3 VDC output during power-up and normal operation.

Both voltages must reach their minimum in-regulation level not later than 20 ms after the output power ramp start.

5.1.3.3 Tolerance

The tolerance of the voltage lines is described in the CompactPCI specification (PICMG 2.0 R3.0). The recommended measurement point for the voltage is the CompactPCI connector on the CPU board.

The following table provides information regarding the required characteristics for each board input voltage.

Table 5-3: Input Voltage Characteristics

VOLTAGE	NOMINAL VALUE	TOLERANCE	MAX. RIPPLE (p-p)	REMARKS
5 V	+5.0 VDC	+5%/-3%	50 mV	Main voltage
3.3 V	+3.3 VDC	+5%/-3%	50 mV	--
+12 V	+12 VDC	+5%/-5%	240 mV	Required
-12 V	-12 VDC	+5%/-5%	240 mV	Not required
VI/O (PCI) voltage	+3.3 VDC or +5 VDC	+5%/-3%	50 mV	--
GND	Ground, not directly connected to potential earth (PE)			

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

5.1.3.4 Regulation

The power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

Warning!

All of the input voltages must be functionally coupled to each other so that if one input voltage fails, all other input voltages must be regulated proportionately to the failed voltage. For example, if the +5V begins to decrease, all other input voltages must decrease accordingly. This is required in order to preclude cross currents within the CP6002.

Failure to comply with above may result in damage to the board or improper system operation.

Note ...

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until the capacitors are discharged. If the voltage rises again before it has gone below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

5.2 Power Consumption

The goal of this description is to provide a method to calculate the power consumption for the CP6002 baseboard and for additional configurations. The processor and memory dissipates the majority of the thermal power.

The power consumption tables below list the voltage and the power specifications for the CP6002 board and its accessories. The values were measured using an 8-slot passive CompactPCI backplane with two power supplies, one for the CPU, and the other for the hard disk.

The operating systems used were uEFI shell and Windows® XP, 32-bit, with Intel® Turbo Boost Technology and Intel® Intelligent Power Sharing enabled. All measurements were conducted at a temperature of 25°C. The measured values varied, because the power consumption was dependent on the processor activity.

Note ...

The power consumption values indicated in the tables below can vary depending on the ambient temperature or the system performance. This can result in deviations of the power consumption values of up to 10%.

The payload power consumption was measured using the following processors:

- Intel® Core™ i7-660UE (ULV), 1.33 GHz, 4 MB L3 cache
- Intel® Core™ i7-620LE (LV), 2.0 GHz, 4 MB L3 cache
- Intel® Core™ i7-610E (SV), 2.53 GHz, 4 MB L3 cache
- Intel® Celeron® P4505 (SV), 1.86 GHz, 2 MB L3 cache

with the following firmware and under the following testing conditions:

- CP6002 in EFI shell
  For this measurement the processor cores were active (no power management enabled) and the graphics controller was in idle state (no application running).
- CP6002 with Windows® XP, 32-bit, processor and graphics controller in idle state
  For this measurement all processor cores and the graphics controller were in idle state (no application running).
- CP6002 with Windows® XP, 32-bit, maximum processor workload with graphics controller in idle state
  For this measurement all processor cores were operating at maximum workload and the graphics controller was in idle state (e.g. dual screen output configuration with no video application running). These values represent the power dissipation reached under realistic, OS-controlled applications with the processor operating at maximum performance.
- CP6002 with Win.® XP, 32-bit, maximum processor and graphics controller workload
  These values represent the maximum power dissipation achieved through the use of specific tools to heat up the processor and graphics controller. These values are unlikely to be reached in real applications.

The following tables indicate the power consumption of the CP6002 with 4 GB DDR3 SDRAM in dual-channel mode. The measurements were made with the CP6002 in EFI Shell mode as well as with the Windows® XP operating system, 32-bit.

Table 5-4: CP6002 in EFI Shell

POWER (typ.)	Intel® Core™ i7-660UE (ULV) 1.33 GHz	Intel® Core™ i7-620LE (LV) 2.0 GHz	Intel® Core™ i7-610E (SV) 2.53 GHz	Intel® Celeron® P4505 (SV) 1.86 GHz
12 V	0.1 W	0.1 W	0.1 W	0.1 W
5 V	8 W	13.0 W	17.0 W	11 W
3.3 V	17 W	17.0 W	17.0 W	18 W
Total	25.1 W	30.1 W	34.1 W	29.1 W

Table 5-5: CP6002 with Win. XP and Processor and Graphics in Idle State

POWER (typ.)	Intel® Core™ i7-660UE (ULV) 1.33 GHz	Intel® Core™ i7-620LE (LV) 2.0 GHz	Intel® Core™ i7-610E (SV) 2.53 GHz	Intel® Celeron® P4505 (SV) 1.86 GHz
12 V	0.1 W	0.1 W	0.1 W	0.1 W
5 V	1.5 W	1.5 W	1.5 W	2 W
3.3 V	13 W	13.0 W	13.0 W	18 W
Total	14.6 W	14.6 W	14.6 W	20.1 W

Table 5-6: CP6002 with Win. XP and Max. Processor Workload and Graphics in Idle State

POWER (typ.)	Intel® Core™ i7-660UE (ULV) 1.33 GHz	Intel® Core™ i7-620LE (LV) 2.0 GHz	Intel® Core™ i7-610E (SV) 2.53 GHz	Intel® Celeron® P4505 (SV) 1.86 GHz
12 V	0.1 W	0.1 W	0.1 W	0.1 W
5 V	10 W	17.0 W	24.0 W	19 W
3.3 V	16 W	17.0 W	18.0 W	19 W
Total	26.1 W	34.1 W	42.1 W	38.1 W

Table 5-7: CP6002 with Win. XP and Maximum Processor and Graphics Workload

POWER (typ.)	Intel® Core™ i7-660UE (ULV) 1.33 GHz	Intel® Core™ i7-620LE (LV) 2.0 GHz	Intel® Core™ i7-610E (SV) 2.53 GHz	Intel® Celeron® P4505 (SV) 1.86 GHz
12 V	0.1 W	0.1 W	0.1 W	0.1 W
5 V	12 W	20.0 W	27.0 W	23 W
3.3 V	20 W	22.0 W	25.0 W	25 W
Total	32.1 W	42.1 W	52.1 W	48.1 W

5.2.1 Power Consumption of the CP6002 Accessories

The following table indicates the power consumption of the CP6002 accessories.

Table 5-8: Power Consumption of CP6002 Accessories

MODULE	POWER 5 V	POWER 3.3 V
DDR3 SDRAM update from 4 GB to 8 GB	—	approx. 1.0 W
SATA Flash module	—	approx. 0.5 W

5.2.2 Power Consumption of the Gigabit Ethernet Controller

The following table indicates the power consumption of the Intel® 82574L GbE controller.

Table 5-9: Power Consumption of the Gigabit Ethernet Controller

ETHERNET PORT	POWER 5 V	POWER 3.3 V
Intel® 82574L (routed to GbE A, B, C, and D), one 1000 Mb/s Ethernet port plugged	—	approx. 0.5 W

5.3 Start-Up Currents of the CP6002

The following table indicates the basic start-up currents of the CP6002 during the first 2-3 seconds after power has been applied (power-on or hot-swap insertion).

Table 5-10: Start-Up Currents of the CP6002

POWER		Intel® Core™ i7-660UE (ULV) 1.33 GHz	Intel® Core™ i7-620LE (LV) 2.0 GHz	Intel® Core™ i7-610E (SV) 2.53 GHz	Intel® Celeron® P4505 (SV) 1.86 GHz
5 V	peak	2.4 A	2.4 A	2.4 A	2.4 A
	average	0.4 A	0.4 A	0.4 A	0.4 A
3.3 V	peak	8.8 A	8.8 A	8.8 A	8.8 A
	average	2.7 A	2.7 A	2.7 A	2.7 A

For further information on the start-up current, please contact Kontron.

5.4 Maximum Power Consumption of PMC/XMC Modules

A maximum power of 7.5 W is available on each PMC/XMC slot. This is in accordance with the draft standard P1386/Draft 2.4a. The maximum power of 7.5 W can be arbitrarily divided on the 3.3 V and 5 V voltage lines.

The following table indicates the current of each PMC/XMC module.

Table 5-11: PMC/XMC Module Current

VOLTAGE	CONTINUOUS CURRENT	PEAK CURRENT
3.3 V	2.27 A	3.0 A
5 V	1.5 A	2.0 A
+12 V	0.6 A	0.8 A
-12 V	0.4 A	0.4 A

Note ...

If the CP6002 is equipped with two PMC/XMCs, the current at +12 V is limited to 0.6 A total (e.g. one PMC/XMC module with 0.4 A and one PMC/XMC module with 0.2 A).

If the CP6002 is equipped with two PMC/XMCs, the current at -12 V is limited to 0.4 A total (e.g. one PMC/XMC module with 0.2 A and one PMC/XMC module with 0.2 A).

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Chapter 6

Thermal Considerations

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6. Thermal Considerations

The following chapters provide system integrators with the necessary information to satisfy thermal and airflow requirements when implementing CP6002 applications.

6.1 Board Internal Thermal Monitoring

To ensure optimal operation and long-term reliability of the CP6002, all onboard components must remain within the maximum temperature specifications. The most critical components on the CP6002 are the processor and the chipset. Operating the CP6002 above the maximum operating limits will result in permanent damage to the board. To ensure functionality at the maximum temperature, the Board Management Controller supports several temperature monitoring and control features.

The CP6002 includes several temperature sensors board to measure the onboard temperature values and regulate the board's power consumption:

- Thermal sensors integrated in the processor
- Thermal sensor integrated in the chipset
- Onboard temperature sensor Temp1 (see Figure 1-6 for its placement)

The onboard temperature sensor Temp1 is accessible via the Board Management Controller. For information on the temperature sensors integrated in the CPU and the chipset, refer to Chapter 6-2 and Chapter 6-3.

6.2 Processor Thermal Monitoring

To allow optimal operation and long-term reliability of the CP6002, the Intel® processor must remain within the maximum die temperature specifications.

The maximum die temperature for Intel® Core™ i7 multi-chip processors is as follows:

- Processor die: 105°C
- Graphics and memory controller die: 100°C

The maximum die temperature for Intel® Celeron® P4505 multi-chip processor is as follows:

- Processor die: 90°C
- Graphics and memory controller die: 85°C

The Intel® processor uses the Adaptive Thermal Monitor feature to protect the processor from overheating and includes the following on-die temperature sensors:

- Two Digital Thermal Sensors (DTS) for the processor cores
- One Digital Thermal Sensor (DTS) for the graphics controller and the memory controller
- Catastrophic Cooling Failure Sensor (THERMTRIP#)

These sensors are integrated in the processor and work without any interoperability of the Board Management Controller, the uEFI BIOS or the software application. Enabling the Thermal Control Circuit in the uEFI BIOS allows the processor to maintain a safe operating temperature without the need for special software drivers or interrupt handling routines.

6.2.1 Digital Thermal Sensor (DTS)

The Intel® processor includes three on-die Digital Thermal Sensors (DTS), two for the processor cores and one for the graphics controller and the memory controller. They can be read via an internal register of the processor. The temperature returned by the Digital Thermal Sensor will always be at or below the maximum operating temperature. Via the Digital Thermal Sensors, the uEFI BIOS, the Board Management Controller or the application software can measure the processor die temperature.

6.2.2 Adaptive Thermal Monitor

The Adaptive Thermal Monitor feature reduces the processor power consumption and the temperature when the processor silicon exceeds the Thermal Control Circuit (TCC) activation temperature until the processor operates at or below its maximum operating temperature. The temperature at which the Adaptive Thermal Monitor activates the Thermal Control Circuit is not user-configurable.

The processor core power reduction is achieved by:

- Frequency/VID Control (by reducing the processor core voltage)
- Clock Modulation (by turning the internal processor core clocks off and on)

Adaptive Thermal Monitor dynamically selects the appropriate method. uEFI BIOS is not required to select a specific method as with previous-generation processors supporting Intel® Thermal Monitor 1 (TM1) and Intel® Thermal Monitor 2 (TM2).

The Adaptive Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

6.2.3 Frequency/VID Control

Frequency/VID Control reduces the processor's operating frequency (using the core ratio multiplier) and the input voltage (using VID signals). This combination of lower frequency and VID results in a reduction of the processor power consumption. This method is similar to Intel® Thermal Monitor 2 (TM2) in previous generation processors.

When the processor temperature reaches the TCC activation point, the event is reported to the Board Management Controller.

Running the processor at the lower frequency and voltage will reduce power consumption and should allow the processor to cool off. If the processor temperature does not drop below the TCC activation point, a second frequency and voltage transition will take place. This sequence of temperature checking and Frequency/VID reduction will continue until either the minimum frequency has been reached or the processor temperature has dropped below the TCC activation point. If the processor temperature remains above the TCC activation point even after the minimum frequency has been reached, then Clock Modulation at that minimum frequency will be initiated.

Note ...

When the TH LED on the front panel is lit after boot-up, it indicates that the processor or the graphics controller is above the maximum die temperature.

6.2.3.1 Clock Modulation

Clock Modulation reduces power consumption by rapidly turning the internal processor core clocks off and on at a duty cycle that should reduce power dissipation (typically a 30-50% duty cycle). This method is similar to Intel® Thermal Monitor 1 (TM1) in previous generation processors.

Once the temperature has dropped below the maximum operating temperature, the TCC goes inactive and clock modulation ceases.

Note ...

When the TH LED on the front panel is lit after boot-up, it indicates that the processor or the graphics controller is above the maximum die temperature.

6.2.4 Catastrophic Cooling Failure Sensor

The Catastrophic Cooling Failure Sensor protects the processor from catastrophic overheating. The Catastrophic Cooling Failure Sensor threshold is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 125°C. Once activated, the event remains latched until the CP6002 undergoes a power-on restart (all power off and then on again).

This function cannot be enabled or disabled in the uEFI BIOS. It is always enabled to ensure that the processor is protected in any event.

Note ...

When all TH LED on the front panel are blinking, it indicates that the processor temperature is above 125°C.

6.3 Chipset Thermal Monitor Feature

The Intel® QM57 chipset includes one on-die Thermal Diode Sensor to measure the chipset die temperature.

The maximum Intel® QM57 chipset case temperature is 111°C.

6.4 External Thermal Regulation

To ensure the best possible basis for operational stability and long-term reliability, the CP6002 is equipped with a heat sink. Coupled together with system chassis, which provides variable configurations for forced airflow, controlled active thermal energy dissipation is guaranteed. The physical size, shape, and construction of the heat sink and ensures the lowest possible thermal resistance. In addition, the CP6002 has been specifically designed to efficiently support forced airflow as found in modern CompactPCI systems.

Thermal Characteristic Graphs

The thermal characteristic graphs shown on the following sections illustrate the maximum ambient air temperature as a function of the volumetric airflow rate for the power consumption indicated. The diagrams are intended to serve as guidance for reconciling board and system with the required computing power considering the thermal aspect. One diagram per CPU version and ruggedization level is provided. There are up to two curves representing upper level working points based on different levels of average CPU utilization. When operating below the corresponding curve, the CPU runs steadily without any intervention of thermal supervision. When operated above the corresponding curve, various thermal protection mechanisms may take effect resulting in temporarily reduced CPU performance or finally in an emergency stop in order to protect the CPU and the chipset from thermal destruction. In real applications this means that the board can be operated temporarily at a higher ambient temperature or at a reduced flow rate and still provide some margin for temporarily requested peak performance before thermal protection will be activated.

An airflow of 2.0 m/s to 3.0 m/s is a typical value for a standard *Kontron* ASM rack. For other racks or housings the available airflow will differ. The maximum ambient operating temperature must be recalculated and/or measured for such environments. For the calculation of the maximum ambient operating temperature, the processor and chipset junction temperature must never exceed the specified limit for the involved processor and chipset.

Thermal characteristic curves

- Thermal characteristic curve of the CP6002 with Maximum Processor Work Load and the graphics controller off or idle
  This load complies with the Maximum Processor Work Load and the graphics controller off or idle indicated in Chapter 5.2, “Power Consumption of the CP6002”, Table 5-6.
- Thermal characteristic curve of the CP6002 with Maximum Processor and Graphics Controller Work Load
  This load complies with the Maximum Processor and Graphics Controller Work Load indicated in Chapter 5.2, “Power Consumption of the CP6002”, Table 5-7.

How to read the diagram

Select a specific CPU and choose a specific working point. For a given flow rate there is a maximum airflow input temperature (= ambient temperature) provided. Below this operating point, thermal supervision will not be activated. Above this operating point, thermal supervision will become active protecting the CPU from thermal destruction. The minimum airflow rate provided must be more than the value specified in the diagram.

Volumetric flow rate

The volumetric flow rate refers to an airflow through a fixed cross-sectional area (i.e. slot width x depth. The volumetric flow rate is specified in m^3/h (cubic-meter-per-hour) or cfm (cubic-feet-per-minute) respectively.

Conversion: 1 cfm = 1.7 m^3/h; 1 m^3/h = 0.59 cfm

Airflow

At a given cross-sectional area and a required flow rate, an average, homogeneous airflow speed can be calculated using the following formula:

Airflow = Volumetric flow rate / area.

The airflow is specified in m/s (meter-per-second) or in fps (feet-per-second) respectively.

Conversion: 1 fps = 0.3048 m/s; 1 m/s = 3.28 fps

The following figures illustrate the operational limits of the CP6002 taking into consideration power consumption vs. ambient air temperature vs. airflow rate. The measurements were made based on a 4HP slot and with both processor cores enabled.

6.4.1 Operational Limits for the CP6002

Figure 6-1: CP6002-R1 and CP6002-R1-MC with i7-660UE, 1.33 GHz

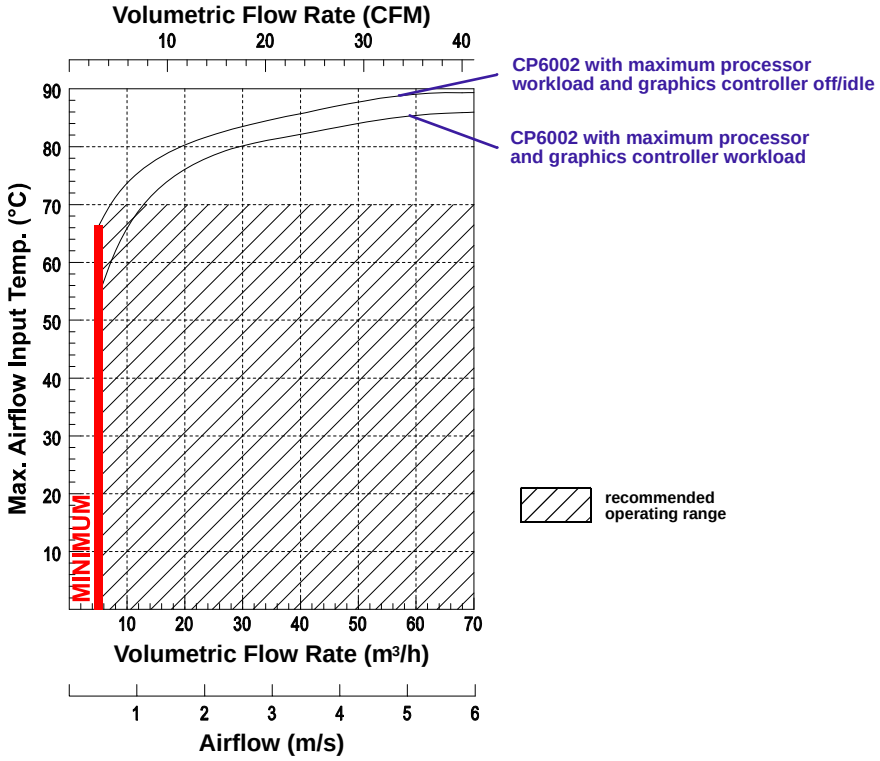


Figure 6-2: CP6002-R1 and CP6002-R1-MC with i7-620LE, 2.0 GHz

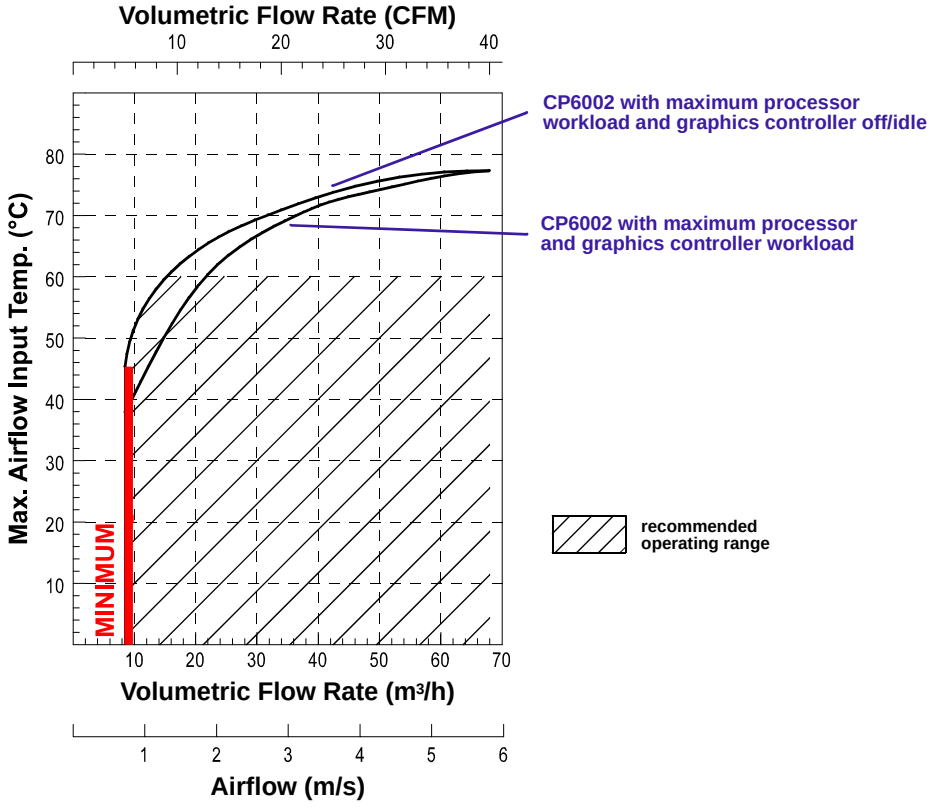


Figure 6-3: CP6002-R1 and CP6002-R1-MC with i7-610E, 2.53 GHz

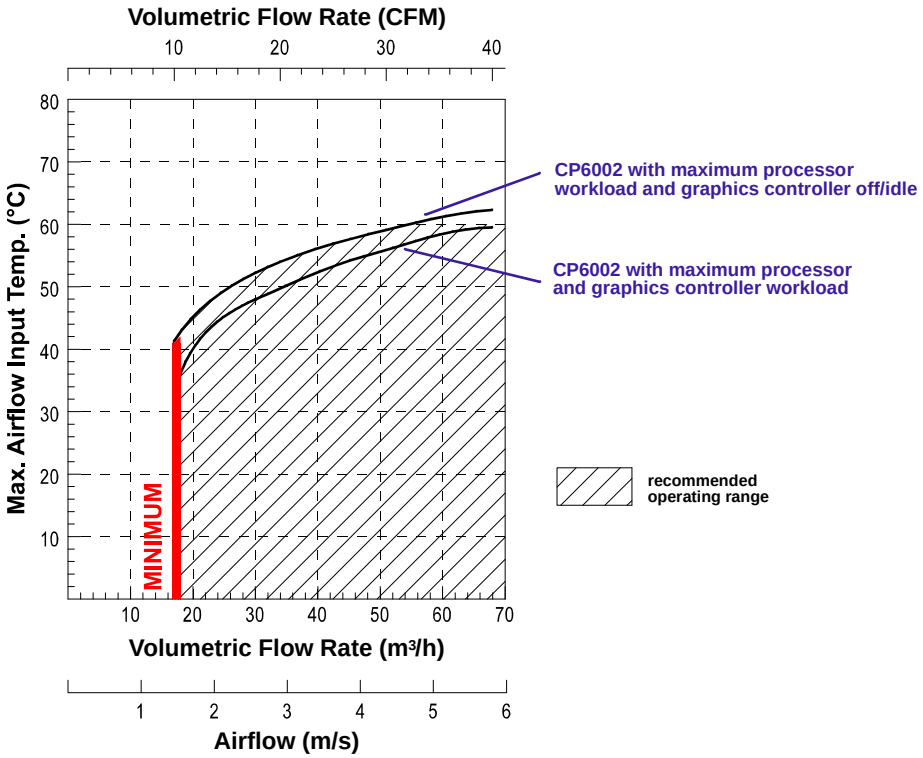


Figure 6-4: CP6002-R1 and CP6002-R1-MC with Celeron® P4505, 1.86 GHz

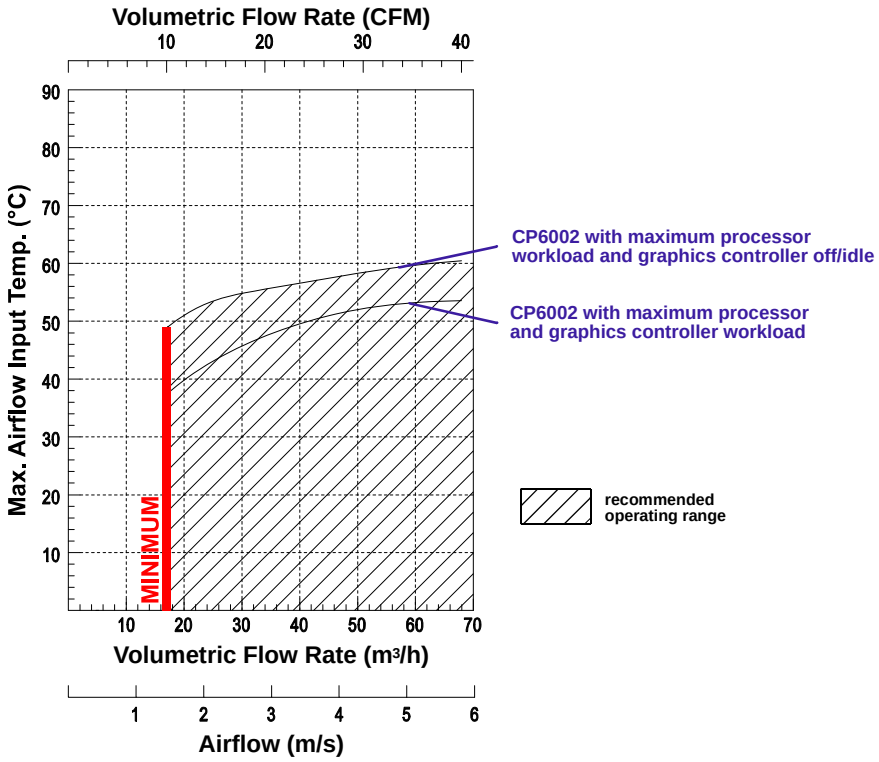
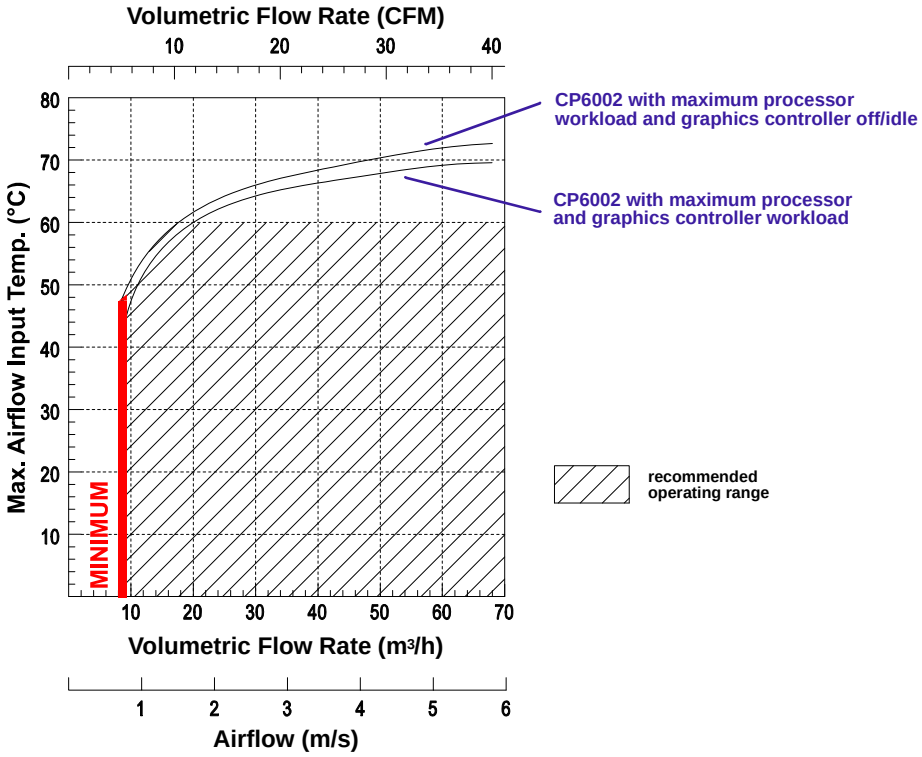


Figure 6-5: CP6002-R2-MC with i7-620LE, 2.0 GHz



6.4.2 Peripherals

When determining the thermal requirements for a given application, peripherals to be used with the CP6002 must also be considered. Devices such as HDDs, SSDs, PMC modules, XMC modules, and SATA Flash modules which are directly attached to the CP6002 must also be capable of being operated at the temperatures foreseen for the application. It may very well be necessary to revise system requirements to comply with operational environment conditions. In most cases, this will lead to a reduction in the maximum allowable ambient operating temperature or even require active cooling of the operating environment.

Warning!

As Kontron assumes no responsibility for any damage to the CP6002 or other equipment resulting from overheating of the CPU, it is highly recommended that system integrators as well as end users confirm that the operational environment of the CP6002 complies with the thermal considerations set forth in this document.

Appendix A

CP6002-MK2.5SATA

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A. CP6002-MK2.5-SATA Assembly Kit

The optional CP6002-MK2.5-SATA assembly kit includes the CP6001-EXT-SATA module and the necessary components required for mounting the module on the CP6002.

A.1 CP6001-EXT-SATA Module Overview

The CP6001-EXT-SATA module has been designed for use with the CP6002 board from Kontron and enables the user to connect an onboard 2.5" Serial ATA HDD or SSD to the CP6002.

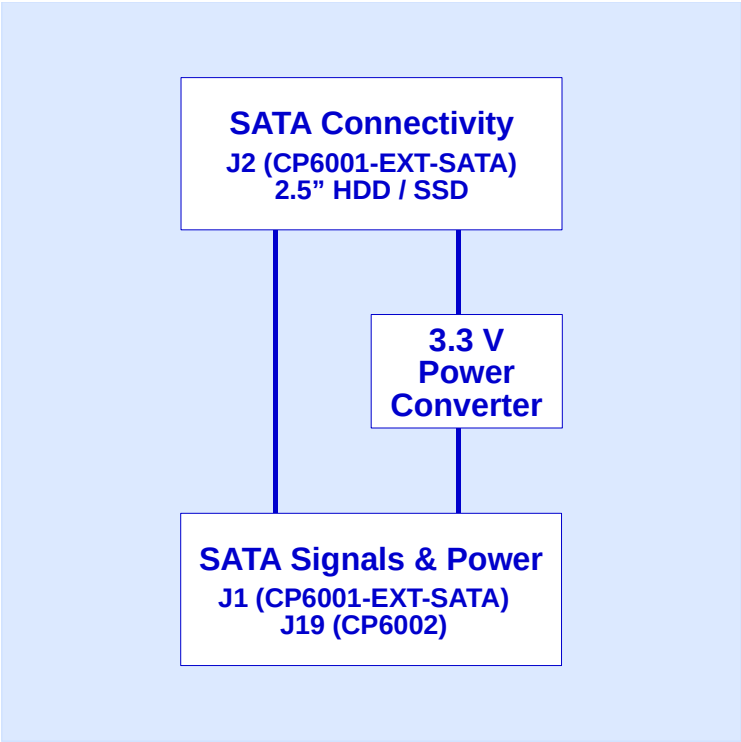
A.2 Technical Specifications

Table A-1: CP6001-EXT-SATA Main Specifications

CP6001-EXT-SATA		SPECIFICATIONS
Interfaces	Board-to-Board Connectors	One 12-pin, male, board-to-board connector, J1
	Serial ATA Connector	One 22-pin Serial ATA connector, J2
General	Power Supply for SATA devices	3.3 V and 5 V (12 V not available)
	Temperature Range	Operating temp.: 0°C to +60°C Storage temp.: -55°C to +85°C
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	54 mm x 27.5 mm
	Board Weight	ca. 6 grams (without HDD/SSD)

A.3 CP6001-EXT-SATA Functional Block Diagram

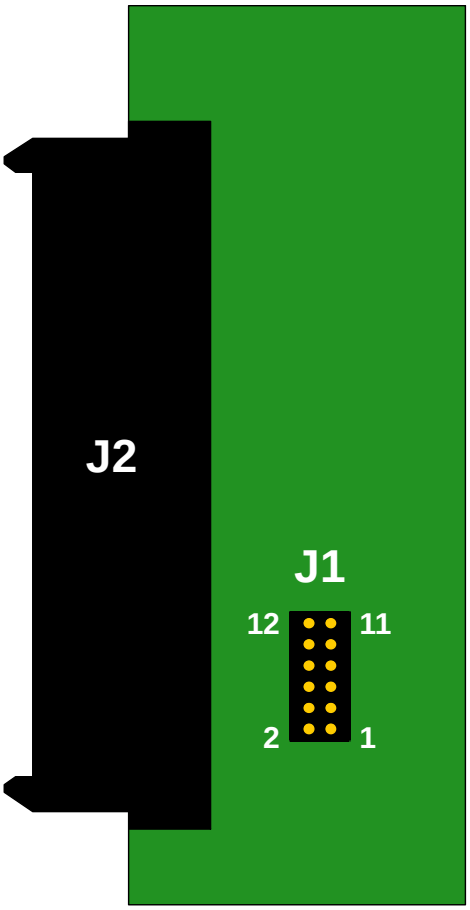
Figure A-1: CP6001-EXT-SATA Functional Block Diagram



A.4 CP6001-EXT-SATA Module Layout

The CP6001-EXT-SATA module includes one board-to-board connector, J1, and one SATA connector, J2.

Figure A-2: CP6001-EXT-SATA Module Layout



A.5 Module Interfaces

A.5.1 Board-to-Board Connectors J1 and J3

The board-to-board connector, J1, on the CP6001-EXT-SATA module is connected to the SATA extension connector, J19, on the CP6002.

Table A-2: Board-to-Board Connector J1 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	SATA_RX-	Differential Receive -	O
2	GND	Ground signal	--
3	SATA_RX+	Differential Receive +	O
4	GND	Ground signal	--
5	GND	Ground signal	--
6	5V	5V power	--
7	SATA_TX-	Differential Transmit -	I
8	GND	Ground signal	--
9	SATA_TX+	Differential Transmit +	I
10	GND	Ground signal	--
11	GND	Ground signal	--
12	5V	5V power	--

A.5.2 SATA Connector J2

The SATA connector, J2, on the CP6001-EXT-SATA module is connected to the 2.5” SATA HDD/SSD mounted on the CP6002. The SATA connector is divided into two segments, a signal segment and a power segment.

Figure A-3: SATA Connector J2

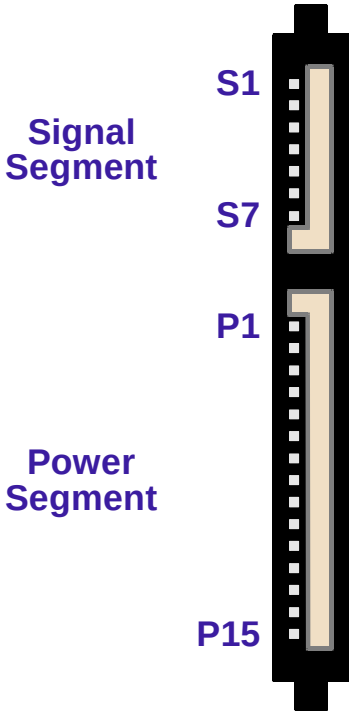


Table A-3: SATA Connector J2 Pinout

PIN	SIGNAL	FUNCTION	I/O
Signal Segment Key			
S1	GND	Ground signal	--
S2	SATA_TX+	Differential Transmit+	O
S3	SATA_TX-	Differential Transmit-	O
S4	GND	Ground signal	--
S5	SATA_RX-	Differential Receive-	I
S6	SATA_RX+	Differential Receive+	I
S7	GND	Ground signal	--
Signal Segment “L”			
Central Connector Polarizer			
Power Segment “L”			
P1	3.3V	3.3V power	--
P2	3.3V	3.3V power	--
P3	3.3V	3.3V power	--
P4	GND	Ground signal	--
P5	GND	Ground signal	--
P6	GND	Ground signal	--
P7	5V	5V power	--
P8	5V	5V power	--
P9	5V	5V power	--
P10	GND	Ground signal	--
P11	RES	Reserved	--
P12	GND	Ground signal	--
P13	12V (NC)	Not connected	--
P14	12V (NC)	Not connected	--
P15	12V (NC)	Not connected	--
Power Segment Key			

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Appendix B

SATA Flash Module

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B. SATA Flash Module

The CP6002 provides an optional SATA Flash module with up to 32 GB NAND Flash memory. The SATA Flash module is connected to the CP6002 via the board-to-board connectors J18 located on the CP6002 and J1 located on the SATA Flash module. The SATA Flash module has been optimized for embedded systems providing high performance, reliability and security.

B.1 Technical Specifications

Table B-1: SATA Flash Module Main Specifications

SATA FLASH MODULE		SPECIFICATIONS
Interface	Board-to-Board Connector	One 34-pin, male, board-to-board connector, J1
Memory	Memory	Up to 32 GB SLC-based NAND Flash memory • Built-in full hard disk emulation • Up to 100 MB/s read rate • Up to 90 MB/s write rate
General	Power Consumption	typ. 0.5 W 3.3 V supply
	Temperature Range	Operational: 0°C to +60°C Standard -40°C to +70°C Extended (for CP6002-R2-MC) Storage: -55°C to +85°C
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	70 mm x 28 mm
	Board Weight	ca. 14 grams

Note ...

Write protection is available for this module. Contact Kontron for further assistance if write protection is required

B.2 SATA Flash Module Layout

The SATA Flash module includes one board-to-board connector, J1, for connection to the CP6002.

Figure B-1: SATA Flash Module Layout (Bottom View)