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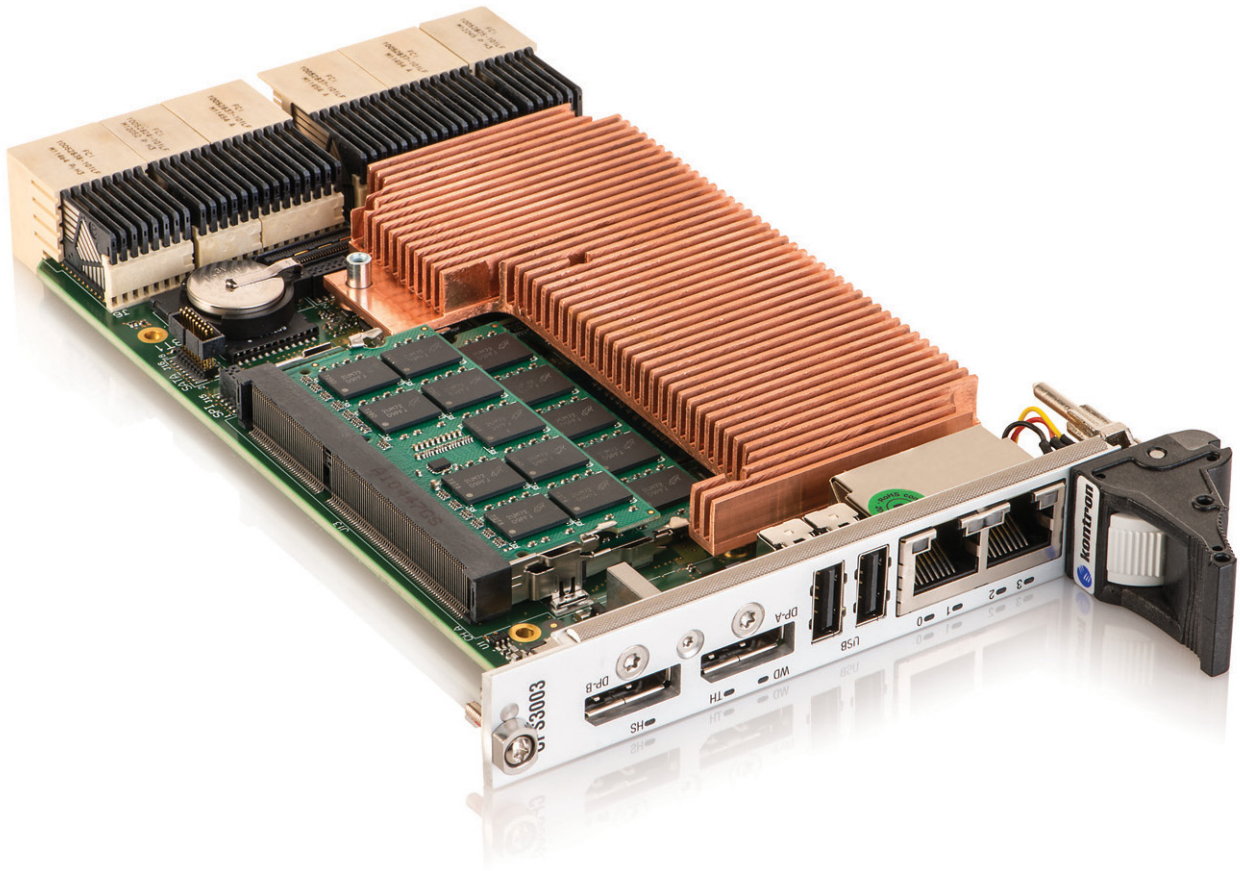

CPS3003-SA

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1.0	Initial issue	13-May-2013

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Disclaimer

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1 Introduction

1.1 Board Overview

CompactPCI® Serial, adopted by the PICMG consortium in 2011, describes a new base standard. The CompactPCI Serial standard introduces a completely new connector that enables a higher signal density and supports even higher transmission frequencies of up to 12 Gb/s as well as modern point-to-point connections such as PCI Express®, SATA, Ethernet and USB on the backplane.

The CPS3003-SA is a highly integrated 3U CompactPCI Serial CPU board based on Intel®'s 3rd Generation Core™ i7 technology in combination with the mobile Intel® QM77 Express Chipset. The CPU board comes with a multi-core CPU package scalable from the dual-core ULV 1.7 GHz Intel® Core™ i7-3517UE up to the quad-core 2.1 GHz i7-3612QE processor. The powerful PCH Intel® QM77 provides a variety of interfaces either routed to front, onboard or the CompactPCI Serial connectors. Memory-demanding applications can make use of up to 16 GB, 1600 MHz DDR3 SDRAM with Error Checking and Correction (ECC). As another security feature, the CPS3003-SA provides a Trusted Platform Module (TPM) which offers hardware-based encryption mechanisms to create, seal or store keys and other important system data.

For graphics intensive applications, the CPS3003-SA offers an excellent graphics performance with integrated DirectX®11, OpenGL 3.1 and OpenCL 1.1 support as well as three independent graphics outputs.

The CPS3003-SA comes with a comprehensive I/O feature set supporting the latest high-speed interfaces such as USB 3.0, SATA 6Gb/s or PCI Express® 3.0. Communication interfaces available on the front panel are two DisplayPort, two USB 2.0 and two Gigabit Ethernet ports. Serial interfaces available on the CompactPCI Serial connectors P1 to P5 are eight USB ports, four SATA interfaces and 17x PCI Express® links. Additional interfaces available on the P6 CompactPCI Serial rear I/O connector are two Gigabit Ethernet interfaces, two USB ports, one DisplayPort and two serial ports.

By adding one of the four extension modules – Smart Extension Module, SATA Flash Module, CPS3003-EXTIO or CPS3003-BRIDGE - the CPS3003-SA's I/O and storage capabilities will be further extended.

The board is offered with various Board Support Packages including Windows, VxWorks and Linux operating systems. For further information concerning the operating systems available for the CP3003-SA, please contact Kontron.

1.2 System Expansion Capabilities

1.2.1 CPS3003-EXTIO Extension Module (8 HP)

The CPS3003-EXTIO module for the 8 HP CPS3003-SA version provides one USB 3.0 port, one COM port, and one CFast socket on the front panel. For further information on the CPS3003-EXTIO extension module, refer to Chapter 6.

1.2.2 CPS3003-BRIDGE Extension Module (9 HP)

The CPS3003-BRIDGE module for the 9 HP CPS3003-SA version provides one USB 3.0 port, one COM port, and one CFast socket on the front panel. In addition, the CPS3003-BRIDGE module is equipped with a PCI Express-to-PCI bridge which converts PCI Express signals into PCI signals and makes them available on the CompactPCI interface. For further information on the CPS3003-BRIDGE extension module, refer to Chapter 7.

1.2.3 CPS-RIO3-01 Rear Transition Module

The CPS-RIO3-01 rear transition module provides comprehensive rear I/O functionality, such as one DisplayPort, two COM ports, two Gigabit Ethernet ports, one USB 3.0 port, and one USB 2.0 port. For further information on the CPS-RIO3-01 rear transition module, refer to Chapter 8.

1.2.4 Smart Extension Module

The Smart Extension Module can be used with the 4 HP CPS3003-SA and expands the onboard I/O capability providing one additional SATA cable connector as well as one USB 2.0 connector thereby facilitating the connection to system-internal USB and SATA devices. For further information on the Smart Extension Module, refer to Chapter 9.

1.2.5 SATA Flash Module

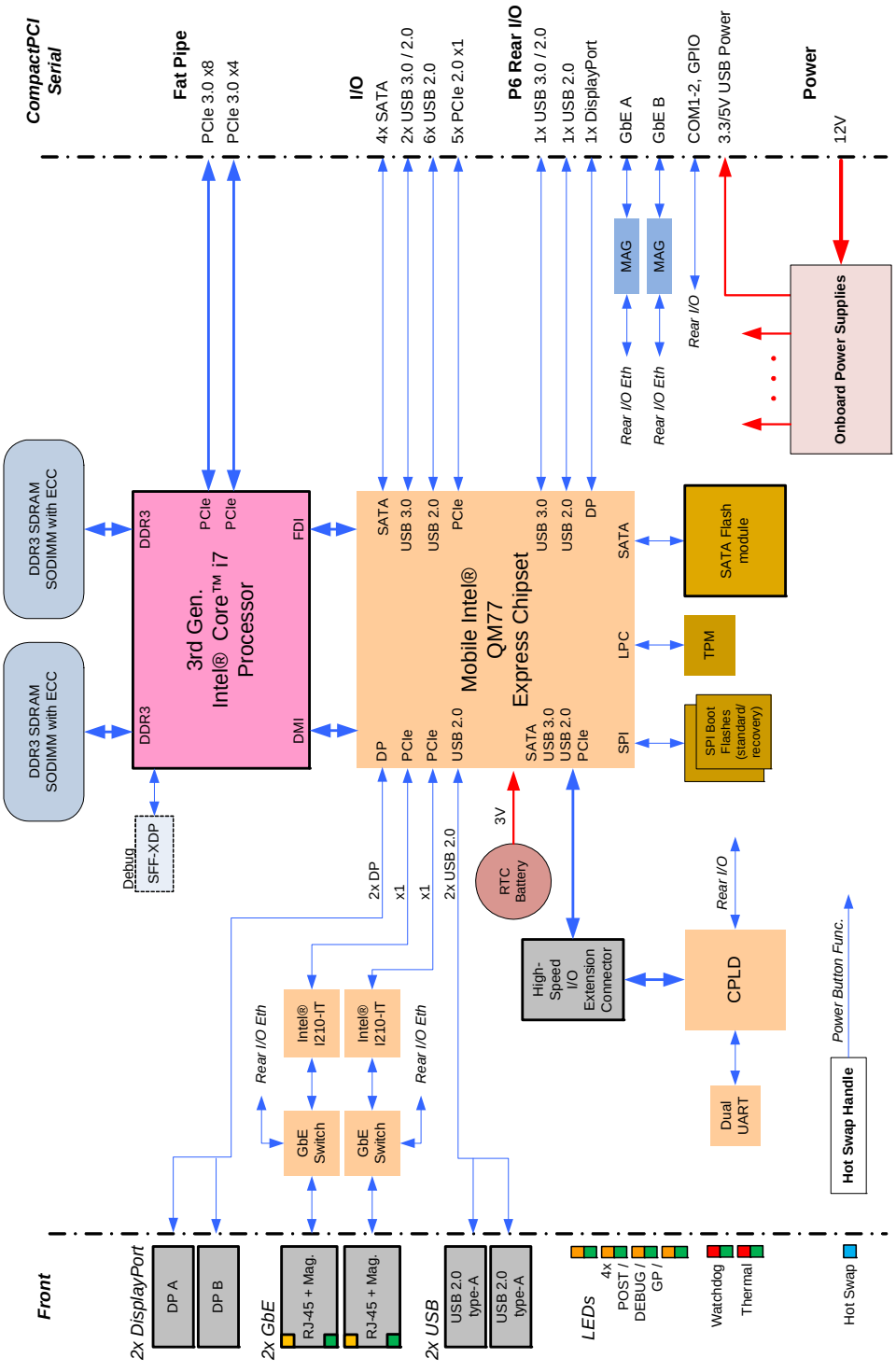
The SATA Flash module can be used with the 4 HP CPS3003-SA and provides up to 32 GB of SLC NAND flash memory. For further information on the SATA Flash module, refer to Chapter 10.

1.3 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

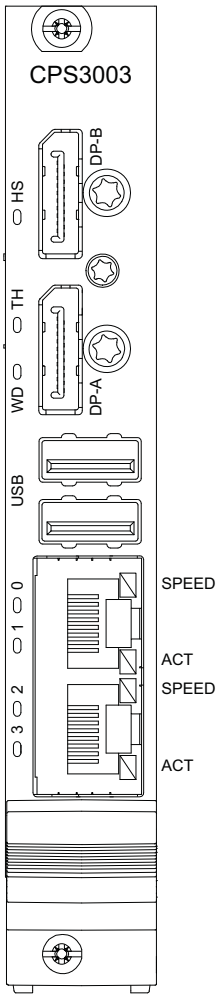
1.3.1 Functional Block Diagram

Figure 1: CPS3003-SA Functional Block Diagram



1.3.2 Front Panel

Figure 2: 4 HP CPS3003-SA Front Panel



System Status LEDs

HS (blue):	Hot Swap Status
TH (red/green):	Temperature Status
WD (green):	Watchdog Status

General Purpose LEDs

LED3..0 (red/green/red+green): General Purpose / POST Code

Note: If the General Purpose LEDs 3..0 are lit red during boot-up, a failure is indicated before the uEFI BIOS has started.

Integral Ethernet LEDs

ACT (green):	Ethernet Link/Activity
SPEED (orange):	1000BASE-T Ethernet Speed
SPEED (green):	100BASE-TX Ethernet Speed
SPEED (off) + ACT on:	10BASE-T Ethernet Speed

Note: For information regarding the front panel of the 8 HP CPS3003-SA with a CPS3003-EXTIO extension module, refer to Chapter 6.

For information regarding the front panel of the 9 HP CPS3003-SA with a CPS3003-BRIDGE extension module, refer to Chapter 7.

1.3.3 Board Layout

Figure 3: 4 HP CPS3003-SA Board Layout (Top View)

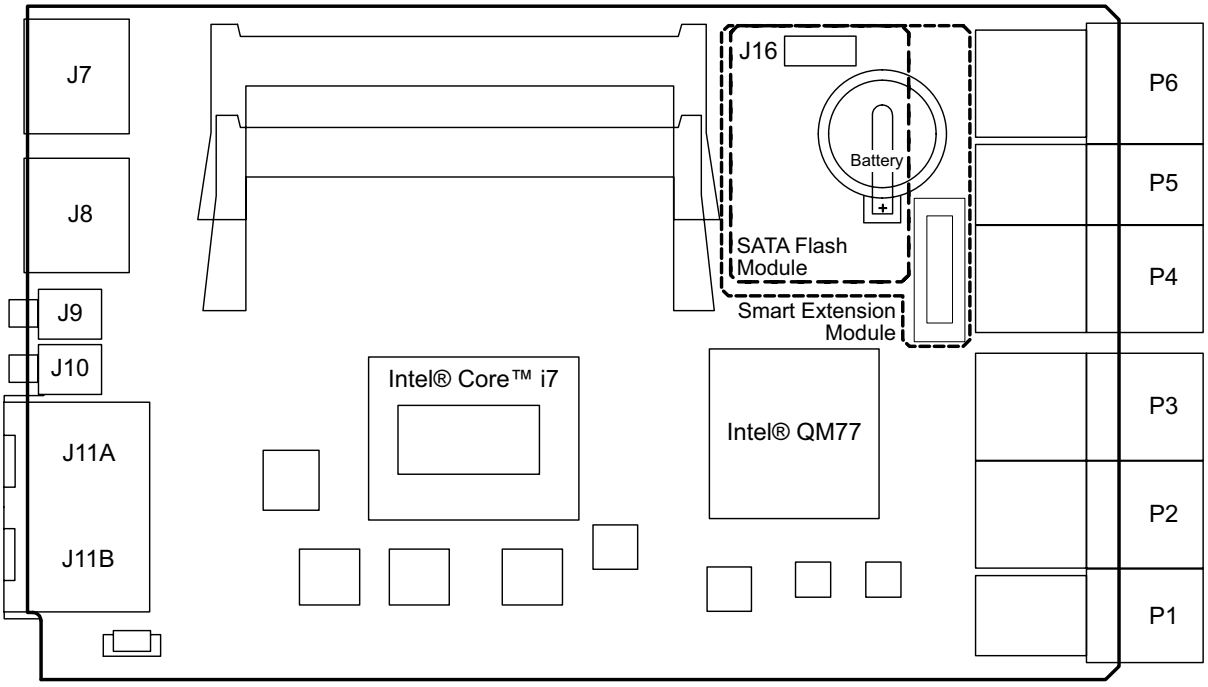
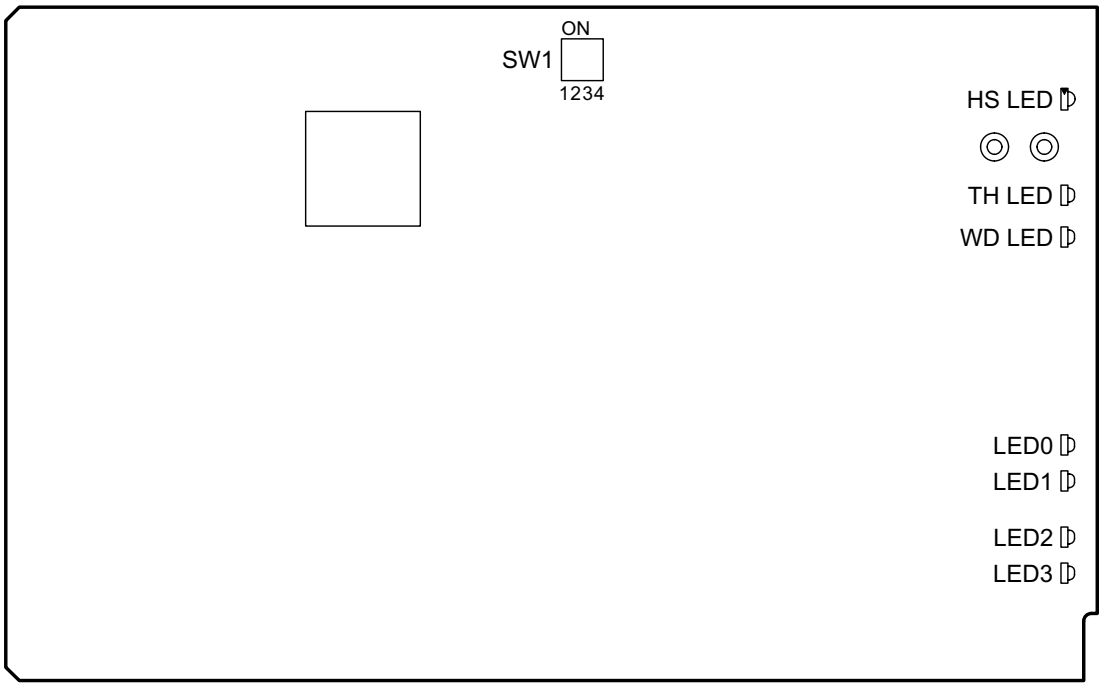


Figure 4: 4 HP CPS3003-SA Board Layout (Bottom View)



1.4 Technical Specification

Table 1: CPS3003-SA Main Specifications

FEATURES		SPECIFICATIONS
Processor & Chipset	CPU	The CPS3003-SA supports the following 3rd generation processors: » Quad-core Intel® Core™ i7-3612QE (SV), 2.1 GHz, 6 MB L3 cache » Dual-core Intel® Core™ i7-3555LE (LV), 2.5 GHz, 4 MB L3 cache » Dual-core Intel® Core™ i7-3517UE (ULV), 1.7 GHz, 4 MB L3 cache
	Graphics Controller	High-performance 3D graphics controller integrated in the processor
	PCH	Mobile Intel® QM77 Express Chipset
Memory	Main Memory	Up to 16 GB, dual-channel DDR3 SDRAM memory with ECC running at 1600 MHz on two SODIMM sockets
	Flash Memory	Two 8 MB SPI boot flash chips for two separate uEFI BIOS images Up to 32 GB SLC NAND flash via an onboard SATA Flash module (SSD)
	EEPROM	EEPROM with 64 kbit
Interfaces	CompactPCI Serial	CompactPCI Serial interface: » Compliant with PICMG® CPCI-S.0 R 1.0 CompactPCI® Serial Specification » Support for the following interfaces: » 7x PCI Express® (1 x8 PCI Express 3.0 on fat pipe, 1 x4 PCI Express 3.0 on fat pipe and 5 x1 PCI Express 2.0) » 4 x SATA (2 x SATA 6 Gb/s, 2 x SATA 3 Gb/s) » 2 x USB 3.0 » 8 x USB 2.0 » 2 x Gigabit Ethernet » 12 V power supply » Hot swap capability » Capability of operation both in system slot and in peripheral slot When installed in a peripheral slot, all interfaces except for the Ethernet interfaces and rear I/O interfaces are isolated from the CompactPCI Serial interface.
	CompactPCI Serial Rear I/O	The following interfaces are routed to the CompactPCI Serial rear I/O connector P6: » COMA and COMB, or COMA and GPIO (all ports have 3.3V LVTTL signaling) » 2 x USB 2.0 » USB 3.0 » DisplayPort » 2x Gigabit Ethernet » System control signals » Input for RTC backup
	Gigabit Ethernet	Two 10 Base-T/100 Base-TX/1000 Base-T Gigabit Ethernet interfaces based on two Intel® I210-IT Ethernet controllers. Both interfaces are individually switchable to front I/O or rear I/O and provide Wake-on-LAN support.

Table 1: CPS3003-SA Main Specifications (Continued)

FEATURES		SPECIFICATIONS
Interfaces	USB	Up to 17 USB ports: » 8 x USB 2.0 on the CompactPCI Serial interface » 2 x USB 3.0 on the CompactPCI Serial interface » 2 x USB 2.0 ports on the front I/O » 2 x USB 2.0 ports on the rear I/O interface » 1 x USB 3.0 port on the rear I/O interface » 1 x USB 2.0 on the CPS3003-EXTIO/CPS3003-BRIDGE extension module » 1 x USB 3.0 on the CPS3003-EXTIO/CPS3003-BRIDGE extension module
	Serial	Two 16C550-compatible UARTs: » COMA available on the CPS3003-EXTIO/CPS3003-BRIDGE extension module or on the rear I/O » COMB or GPIO available on the rear I/O only
	SATA	Six SATA ports: » 2 x SATA 3 Gb/s onboard » 2 x SATA 6 Gb/s on the CompactPCI Serial interface » 2 x SATA 3 Gb/s on the CompactPCI Serial interface High-performance RAID 0/1/5/10 functionality on all SATA ports
	I/O Extension Interfaces	I/O extension to 8 HP board version via the CPS3003-EXTIO module: » CFast (SATA 3 Gb/s) » USB 3.0 » COMA (RS-232) » Reset button » SATA activity LED I/O extension to 9 HP board version via the CPS3003-BRIDGE module: » CFast (SATA 3 Gb/s) » USB 3.0 » COMA (RS-232) » Reset button » SATA activity LED » CompactPCI interface I/O extension of CPS3003-SA via the Smart Extension Module: » SATA 3 Gb/s » USB 2.0
Sockets	Front Panel Connectors	DP: two DisplayPort connectors, J7 and J8 USB: two 4-pin, type A connectors, J9 and J10 Ethernet: dual RJ-45 connector, J11A/B
	Onboard Connectors	CompactPCI Serial connectors P1 to P6 18-pin extension connector for the SATA Flash module (SSD), J16 Two 204-pin DDR3 SODIMM sockets 60-pin, high-speed I/O extension connector

Table 1: CPS3003-SA Main Specifications (Continued)

FEATURES		SPECIFICATIONS
LEDs / Switches	Front Panel LEDs	System Status LEDs: » HS (blue): Hot Swap Status » TH (red/green): Temperature Status » WD (green): Watchdog Status General Purpose LEDs: » LED3..0 (red/green/red+green): General Purpose / POST Code Ethernet LEDs: » ACT (green): Network / Link Activity » SPEED (green/orange): Network Speed
	DIP Switch	One DIP switch, SW1, for board configuration
Timer	Real Time Clock	Real-time clock with 256 Byte CMOS RAM; battery-backup available
	Watchdog Timer	Software-configurable, two-stage Watchdog with programmable timeout ranging from 125 ms to 4096 s in 16 steps Serves for generating IRQ or hardware reset
Sys. Management	Thermal Management	CPU and board overtemperature protection is provided by: » Up to four Digital Thermal Sensors (DTS), one for each core » One Digital Thermal Sensor (DTS) for the processor graphics controller » One temperature sensor integrated in the Intel® QM77 Chipset for monitoring the chipset » Specially designed heat sinks
Security	TPM	Trusted Platform Module (TPM) 1.2 for enhanced hardware- and software-based data and system security
Software	uEFI BIOS	AMI Aptio® BIOS firmware based on the uEFI Specification and the Intel Platform Innovation Framework for EFI: » LAN boot capability for diskless systems (standard PXE) » Redundant image; fail-safe recovery in case of a damaged image » Non-volatile storage of setting in the SPI boot flash (battery only required for the RTC) » Compatibility Support Module (CSM) providing legacy BIOS compatibility based on AMIBIOS8 » Command shell for diagnostics and configuration » EFI Shell commands executable from mass storage device in a Pre-OS environment (open interface)
	Operating Systems	There are various operating systems available for the CPS3003-SA. For further information, please contact Kontron.

Table 1: CPS3003-SA Main Specifications (Continued)

FEATURES		SPECIFICATIONS
General	Power Consumption	See Chapter 4 for details.
	Temperature Range	Operational: 0°C to +60°C Standard (depending on processor version and air-flow in the system) -40°C to +85°C Extended (with Intel® Core™ i7-3517UE, 1.7 GHz ULV processor only) Storage: -40°C to +85°C Without hard disk and without battery
	Battery	3.0V lithium battery for RTC; Battery type: UL-approved CR1632 Temperature ranges: Operational (load): -20°C to +70°C typical (refer to the battery manufacturer's specifications for exact range) Storage (no load): -40°C to +70°C typical
	Climatic Humidity	93% RH at 40 °C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	100 mm x 160 mm 3U, 4 HP, CompactPCI Serial-compliant form factor
	Board Weight	4 HP CPS3003-SA with: » Intel® Core™ i7-3612QE (SV), 2.1 GHz, copper heat sink: 530 grams » Intel® Core™ i7-3555LE (LV), 2.5 GHz, aluminum heat sink: 330 grams » Intel® Core™ i7-3517UE (ULV), 1.7 GHz, aluminum heat sink: 330 grams The above-mentioned board weight refers to the 4 HP CPS3003-SA without extension modules such as SATA Flash module or Smart Extension Module.

Note: For a description of the additional interfaces available on the 8 HP and 9 HP board versions, refer to Chapter 6, CPS3003-EXTIO Extension Module, and Chapter 7, CPS3003-BRIDGE Extension Module, respectively.

1.5 Standards

This product complies with the requirements of the following standards.

Table 2: Standards

TYPE	ASPECT	STANDARD
CE	Emission	EN55022, EN50121-3-2, EN61000-6-3
	Immission	EN55024, EN50121-3-2, EN61000-6-2
	Electrical Safety	EN60950-1
Mechanical	Mechanical Dimensions	IEEE 1101.10
Environmental	Climatic Humidity	IEC60068-2-78
	WEEE	Directive 2002/96/EC Waste electrical and electronic equipment
	RoHS 2	Directive 2011/65/EU Restriction of the use of certain hazardous substances in electrical and electronic equipment

In addition, boards ordered with the ruggedized service comply with the following standards as well.

Table 3: Additional Standards for Boards Ordered with Ruggedized Service

TYPE	ASPECT	STANDARD	REMARKS
Environmental	Vibration (Sinusoidal)	IEC60068-2-6 IEC61131-2	Ruggedized version test parameters: 9-150 (Hz) frequency range 1 (g) acceleration 1 (oct/min) sweep rate 10 cycles/axis 3 axis
	Single Shock	IEC60068-2-27 IEC61131-2	Ruggedized version test parameters: 15 (g) acceleration 11 (ms) shock duration half sine 3 number of shocks per direction (total: 18) 6 directions 5 (s) recovery time

Note: Customers desiring to perform further environmental testing of the CPS3003-SA must contact Kontron for assistance prior to performing any such testing.

Boards **without conformal coating** must not be exposed to a change of temperature which can lead to condensation. Condensation may cause irreversible damage, especially when the board is powered up again.

Kontron does not accept any responsibility for damage to products resulting from destructive environmental testing.

1.6 Related Publications

The following publications contain information relating to this product.

Table 4: Related Publications

PRODUCT	PUBLICATION
CompactPCI Serial Systems	PICMG® CPCI-S.0 R 1.0 CompactPCI® Serial Specification
CompactPCI Systems	PICMG 2.0, Rev. 3.0 CompactPCI Specification
CFast	CFast Specification Revision 1.1
Platform Firmware	Unified Extensible Firmware Interface (uEFI) specification, version 2.3.1
All Kontron products	Product Safety and Implementation Guide, ID 1021-9142

2 Functional Description

2.1 Processor and Chipset

The CPS3003-SA supports the Intel® Core™ i7-3612QE, the Intel® Core™ i7-3555LE, and the Intel® Core™ i7-3517UE processors in combination with the mobile Intel® QM77 Express Chipset.

Table 5: Features of the Processors Supported on the CPS3003-SA

FEATURE	Core™ i7-3612QE (SV) 2.1 GHz	Core™ i7-3555LE (LV) 2.5 GHz	Core™ i7-3517UE (ULV) 1.7 GHz
Processor Cores	four	two	two
Processor Base Frequency	2.1 GHz	2.5 GHz	1.7 GHz
Maximum Turbo Frequency	3.3 GHz	3.2 GHz	2.8 GHz
Hyper-Threading	supported	supported	supported
SpeedStep®	supported	supported	supported
L1 cache per core	64 kB	64 kB	64 kB
L2 cache per core	256 kB	256 kB	256 kB
L3 cache	6 MB	4 MB	4 MB
DDR3 Memory	up to 16 GB / 1600 MHz	up to 16 GB / 1600 MHz	up to 16 GB / 1600 MHz
Graphics Base Frequency	650 MHz	550 MHz	350 MHz
Graphics Max. Dynamic Frequency	1.0 GHz	950 MHz	950 MHz
Thermal Design Power	35 W	25 W	17 W

For further information about the processors used on the CPS3003-SA, please visit the Intel website. For further information concerning the suitability of other Intel processors for use with the CPS3003-SA, please contact Kontron.

2.1.1 Integrated Processor Graphics Controller

The 3rd gen. Intel® Core™ i7 processor includes a highly integrated processor graphics controller delivering high-performance 3D, 2D graphics capabilities. The integrated processor graphics controller has three independent display pipes allowing for support of multiple display configurations and provides three digital ports capable of driving resolutions up to 2560 x 1600 pixels @ 60 Hz through DisplayPort and up to 1920x1200 pixels @ 60Hz using HDMI/DVI.

2.2 Memory

The CPS3003-SA supports a dual-channel (72-bit) DDR3 memory with Error Checking and Correcting (ECC) running at 1600 MHz. It provides two 204-pin sockets for two DDR3 ECC SODIMM modules that support up to 16 GB system memory. The maximum memory size per channel is 8 GB. The available memory module configuration can be either 4 GB, 8 GB or 16 GB. However, when the internal processor graphics controller is enabled, the amount of memory available to applications is less than the total physical memory in the system. The chipset's Dynamic Video Memory Technology, for example, dynamically allocates the proper amount of system memory required by the operating system and the application.

Note: Only qualified DDR3 ECC SODIMM modules from Kontron are authorized for use with the CPS3003-SA. Replacement of the SODIMM modules by the customer without authorization from Kontron will void the warranty.

2.3 Watchdog Timer

The CPS3003-SA provides a Watchdog timer that is programmable for a timeout period ranging from 125 ms to 4096 s in 16 steps.

The Watchdog timer provides the following modes or operation:

- Timer-only mode
- Reset mode
- Interrupt mode
- Dual-stage mode

In dual-stage mode, a combination of both interrupt and reset is generated if the Watchdog is not serviced.

2.4 Battery

The CPS3003-SA is provided with an UL-approved CR1632, 3.0 V, “coin cell” lithium battery for the RTC. Power for the RTC may be provided either from the 4 HP/8 HP/9 HP CPS3003-SA or from the backplane/rear transition module, i.e. only one battery may be used at a time in a system. When a battery is installed, refer to the operational specifications of the battery as this determines the storage temperature of the CPS3003-SA.

2.5 Flash Memory

The CPS3003-SA provides flash interfaces for the uEFI BIOS and the SATA Flash module.

2.5.1 SPI Boot Flash for uEFI BIOS

The CPS3003-SA provides two 8 MB SPI boot flashes for two separate uEFI BIOS images, a standard SPI boot flash and a recovery SPI boot flash. The fail-over mechanism for the uEFI BIOS recovery can be controlled via the DIP switch SW1, switch 2. The SPI boot flash includes a hardware write protection option, which can be configured via the uEFI BIOS. If write protection is enabled, the SPI boot flash cannot be written to.

Note: The uEFI BIOS code and settings are stored in the SPI boot flashes. Changes made to the uEFI BIOS settings are available only in the currently selected SPI boot flash. Thus, switching over to the other SPI boot flash may result in operation with different uEFI BIOS code and settings.

2.5.2 SATA Flash Module

The 4 HP CPS3003-SA supports up to 32 GB flash memory in combination with an optional SATA Flash module. The SATA Flash module cannot be used in conjunction with the Smart Extension Module, the CPS3003-EXTIO module or the CPS3003-BRIDGE module.

2.6 Trusted Platform Module 1.2

The CPS3003-SA supports the Trusted Platform Module (TPM) 1.2. TPM1.2 is a security chip specifically designed to provide enhanced hardware- and software-based data and system security. TPM1.2 is based on the Atmel AT97SC3204 security controller and stores sensitive data such as encryption and signature keys, certificates and passwords, and is able to withstand software attacks to protect the stored information.

2.7 Board Interfaces

2.7.1 Front Panel LEDs

The CPS3003-SA provides three system status LEDs, such as one Hot Swap Status LED (HS LED), one temperature status LED (TH LED) and one Watchdog status LED (WD LED), as well as four General Purpose/POST code LEDs (LED3..0). Their functionality is described in the following chapters and reflected in the registers mentioned in Chapter 4, Configuration.

2.7.1.1 System Status LEDs

Table 6: System Status LEDs Function

LED	COLOR	STATE	FUNCTION
HS LED	blue	Off	Board in normal operation. Do not extract the board.
		Blinking	Hot swap in progress
		On	Board ready for hot swap extraction
TH LED	red / green	Off	Power failure
		Green	Board in normal operation
		Red	CPU has reached maximum allowable operating temperature and the performance has been reduced
		Red blinks	CPU temperature above 125°C (CPU has been shut off) In this event, all General Purpose LEDs (LED3 - 0) are blinking red as well.
WD LED	red / green	OFF	Watchdog inactive
		Green	Watchdog active, waiting to be triggered
		Red	Watchdog expired

Note: If the TH LED flashes red at regular intervals, it indicates that the processor junction temperature has reached a level beyond which permanent silicon damage may occur and the processor has been shut off. To turn to normal operation, the power must be switched off and then on again.

2.7.1.2 General Purpose LEDs

The General Purpose LEDs (LED3..0) are designed to indicate the boot-up POST code after which they are available to the application. If the LED3..0 are lit red during boot-up, a failure is indicated. In this event, please contact Kontron for further assistance.

The POST code is indicated during the boot-up phase. After boot-up, the LEDs indicate General Purpose or Port 80 signals, depending on the uEFI BIOS settings. The default setting after boot-up is General Purpose.

Table 7: General Purpose LEDs Function

LED	COLOR	FUNCTION DURING BOOT-UP	FUNCTION DURING uEFI BIOS POST (if POST code config. is enabled)	FUNCTION AFTER BOOT-UP
LED3	red	Power failure	--	General Purpose or Port 80 **Default: General Purpose**
	green	--	uEFI BIOS POST bit 3 and bit 7	
	red+green	--	--	
LED2	red	CPU catastrophic error	CPU catastrophic error	General Purpose or Port 80 **Default: General Purpose**
	green	--	uEFI BIOS POST bit 2 and bit 6	
	red+green	--	--	
LED1	red	Hardware reset	--	General Purpose or Port 80 **Default: General Purpose**
	green	--	uEFI BIOS POST bit 1 and bit 5	
	red+green	--	--	
LED0	red	uEFI BIOS boot failure	--	General Purpose or Port 80 **Default: General Purpose**
	green	--	uEFI BIOS POST bit 0 and bit 4	
	red+green	--	--	

For further information regarding the configuration of the General Purpose LEDs, refer to Chapter 3.3.4, LED Configuration Register, and Chapter 3.3.5, LED Control Register.

Note: The bit allocation for Port 80 is the same as for the POST code.

How to Read the 8-Bit POST Code

Due to the fact that only 4 LEDs are available and 8 bits must be displayed, the POST code output is multiplexed on the General Purpose LEDs.

Table 8: POST Code Sequence

STATE	GENERAL PURPOSE LEDs
0	All LEDs are OFF; start of POST sequence
1	High nibble
2	Low nibble; state 2 is followed by state 0

The following is an example of the General Purpose LEDs' operation if the POST configuration is enabled (see also Table 7, "General Purpose LED Function").

Table 9: POST Code Example

	LED3	LED2	LED1	LED0	RESULT
HIGH NIBBLE	off (0)	on (1)	off (0)	off (0)	0x4
LOW NIBBLE	off (0)	off (0)	off (0)	on (1)	0x1
POST CODE	0x41				

Note: Under normal operating conditions, the General Purpose LEDs should not remain lit during boot-up. They are intended to be used only for debugging purposes. In the event that a General Purpose LED lights up during boot-up and the CPS3003-SA does not boot, please contact Kontron for further assistance.

2.7.2 USB Interfaces

The CPS3003-SA provides 13 USB 2.0 ports:

- Two on front I/O
- Eight on the CompactPCI Serial interface
- Two on the CompactPCI Serial connector P6 used for rear I/O
- One for I/O extension modules (CPS3003-EXTIO, CPS3003-BRIDGE, Smart Extension Module)

The CPS3003-SA provides four USB 3.0 ports:

- Two on the CompactPCI Serial interface
- One on the CompactPCI Serial connector P6 used for rear I/O
- One for I/O extension modules (CPS3003-EXTIO, CPS3003-BRIDGE)

On the front panel, the CPS3003-SA has two standard, type A, USB 2.0 connectors, J7 and J8.

2.7.3 DisplayPort Interfaces

The CPS3003-SA provides three standard DisplayPort interfaces for connection to monitors:

- Two on the front panel implemented as standard DisplayPort connectors, J7 and J8
- One on the CompactPCI Serial connector P6 used for rear I/O

2.7.4 Serial Ports

The CPS3003-SA provides two serial ports:

- COMA (3.3V LVTTL) available either on the I/O extension module or one on the CompactPCI Serial connector P6 used for rear I/O
- COMB (3.3V LVTTL) on the CompactPCI Serial connector P6 used for rear I/O

COMA and COMB are fully compatible with the 16C550 controller and include a complete set of handshaking and modem control signals. The COMA and COMB ports provide maskable interrupt generation. The data transfer on the COM ports is up to 115.2 kbit/s.

2.7.5 Gigabit Ethernet

The CPS3003-SA board includes two 10Base-T/100Base-TX/1000Base-T Ethernet ports based on two Intel® I210-IT Ethernet controllers, which are connected to the x1 PCI Express interfaces of the Intel® QM77 Express Chipset. The Gigabit Ethernet interfaces are individually switchable between front I/O and rear I/O and provide Wake-on-LAN support.

Note: In order to use the Wake-on-LAN feature, the power supply must not be switched off (+5V stand-by voltage cannot be used). The CPS3003-SA does not turn off the main power supply after an operating system shutdown in order to support Wake-on-Lan.

The Gigabit Ethernet interfaces are implemented as a two standard RJ-45 Ethernet connectors, J11A/B on the front panel.

2.7.6 SATA Interfaces

The CPS3003-SA provides six SATA ports:

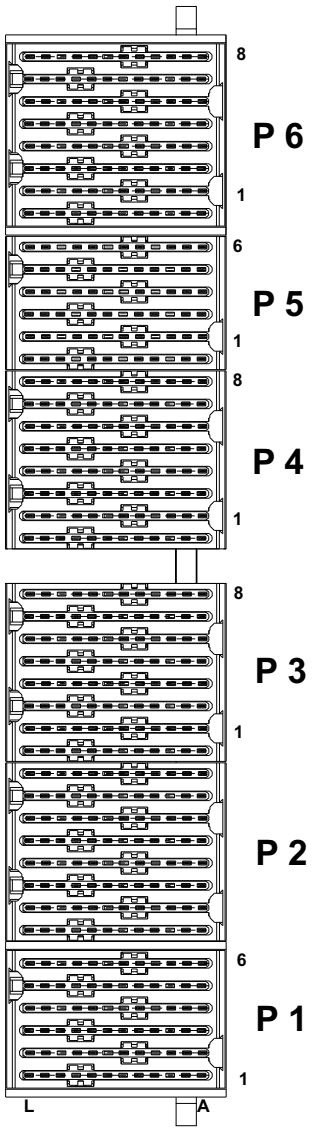
- One SATA 3 Gb/s port for the SATA Flash module
- One SATA 3 Gb/s port on for the I/O extension modules
- Two SATA 6 Gb/s ports on the CompactPCI Serial interface
- Two SATA 3 Gb/s ports on the CompactPCI Serial interface

All six SATA interfaces provide high-performance RAID 0/1/5/10 functionality.

2.7.7 CompactPCI Serial Interface

This interface is comprised of six CompactPCI Serial connectors, P1 to P6. The connector P6 provides rear I/O capability, which is currently not defined in the CompactPCI Serial specification. Refer to Tables 16 and 17 for pinout information for this connector.

Figure 5: CompactPCI Serial Connectors P1 to P6



2.7.7.1 CompactPCI Serial Connectors P1 to P5

The following tables provide pinout information for connectors P1 to P5.

Table 10: Legend for CompactPCI Serial Connectors P1 to P5

SIGNAL TYPE	SIGNAL	I/O	DESCRIPTION
CompactPCI Serial	PS_ON#	O	Power supply control signal
	PRST#	I	Push button reset
	PWR_FAIL#/GA1	I	Power supply fail (GA1 in peripheral slot)
	RST#	O	Reset signal
	SYSEN#	I	System slot identification
	PWRBTN#/GA0	I	Power button(GA0 in peripheral slot)
	GA2, GA3	I	Geographical addressing
	WAKE_IN#	I	Wake signal
	I2C_SDA	I/O	I2C system management bus data
	I2C_SCL	O	I2C system management bus clock
Power	+12V	I	+12 V power supply
	GND	-	Ground
	STANDBY	I	5V standby power supply
SATA	x_SATA_Tx-, x_SATA_Tx+	O	Differential pair of SATA transmit lines, ports 1 to 8
	x_SATA_Rx-, x_SATA_Rx+	I	Differential pair of SATA receive lines, ports 1 to 8
SGPIO	SATA_SCL	O	Clock signal
	SATA_SL	O	Last clock of a bit stream
	SATA_SDO	O	Serial data output bit stream
	SATA_SDI	I	Serial data input bit stream
PCI Express	x_PE_Tx00-.. x_PE_Tx07-, x_PE_Tx00+..x_PE_Tx07+	O	Differential PCI Express transmitter lanes 0 to 7 for link 1 and 2 (x = 1 or x = 2)
	x_PE_Rx00-..x_PE_Rx07-, x_PE_Rx00+..x_PE_Rx07+	I	Differential PCI Express receiver lanes 0 to 7 for link 1 and 2 (x = 1 or x = 2)
	x_PE_Tx00-..x_PE_Tx03-, x_PE_Tx00+..x_PE_Tx03+	O	Differential PCI Express transmitter lanes 0 to 3 for link 3 to link 8 (x = 3 to 8)
	x_PE_Rx00-.. x_PE_Rx03-, x_PE_Rx00+..x_PE_Rx03+	I	Differential PCI Express receiver lanes 0 to 3 for link 3 to link 8 (x = 3 to 8)
	x_PE_CLK-, x_PE_CLK+	O	Differential 100 MHz reference clock for link 1 to 8 (x = 1 to 8)
	x_PE_CLKE#	I	Presence Detect (x = 1 to 8)
USB	x_USB3_Tx-, x_USB3_Tx+	O	Differential pair of USB 3.0 transmit lines, port 1 to port 8 (x = 1 to 8)
	x_USB3_Rx-, x_USB3_Rx+	I	Differential pair of USB 3.0 receive lines, port 1 to port 8 (x = 1 to 8)
	x_USB2-, x_USB2+	I/O	Differential pair of USB 2.0 lines, port 1 to port 8 (x = 1 to 8)
IO	IO	I/O	User I/O

Note: In the following tables signals highlighted in white have not been implemented or are reserved.

Table 11: Pinout for CompactPCI Serial Connector P1

1_PE_ Rx03-	1_PE_ Rx03+	GND	1_PE_ Tx03-	1_PE_ Tx03+	GND	1_PE_ Rx02-	1_PE_ Rx02+	GND	1_PE_ Tx02-	1_PE_ Tx02+	GND	6
GND	1_PE_ Rx01-	1_PE_ Rx01+	GND	1_PE_ Tx01-	1_PE_ Tx01+	GND	1_PE_ Rx00-	1_PE_ Rx00+	GND	1_PE_ Tx00-	1_PE_ Tx00+	5
1_SATA_ Rx-	1_SATA_ Rx+	GND	1_SATA_ Tx-	1_SATA_ Tx+	GND	reserved	reserved	GND	1_ USB2 -	1_ USB2 +	GND	4
GA3	SATA_ SL	SATA_ SCL	GA2	SATA_ SDO	SATA_ SDI	PWR_ FAIL#	1_USB3 _Rx-	1_USB3 _Rx+	PWR BTN#	1_USB3 _Tx-	1_USB3 _Tx+	3
SYSEN#	reserved	GND	WAKE_ IN#	PRST#	GND	RST#	PS_ON#	GND	I2C_ SDA	I2C_ SCL	GND	2
GND	+12V	+12V	GND	+12V	+12V	GND	+12V	+12V	GND	STANDBY	+12V	1
L	K	J	I	H	G	F	E	D	C	B	A	

Table 12: Pinout for CompactPCI Serial Connector P2

4_ USB2 -	4_ USB2 +	IO	3_ USB2 -	3_ USB2 +	GND	2_ USB2 -	2_ USB2 +	GND	IO	IO	GND	8
GND	IO	IO	GND	IO	IO	GND	IO	IO	GND	IO	IO	7
2_PE_ Rx07-	2_PE_ Rx07+	GND	2_PE_ Tx07-	2_PE_ Tx07+	GND	2_PE_ Rx06-	2_PE_ Rx06+	GND	2_PE_ Tx06-	2_PE_ Tx06+	GND	6
GND	2_PE_ Rx05-	2_PE_ Rx05+	GND	2_PE_ Tx05-	2_PE_ Tx05+	GND	2_PE_ Rx04-	2_PE_ Rx04+	GND	2_PE_ Tx04-	2_PE_ Tx04+	5
2_PE_ Rx03-	2_PE_ Rx03+	GND	2_PE_ Tx03-	2_PE_ Tx03+	GND	2_PE_ Rx02-	2_PE_ Rx02+	GND	2_PE_ Tx02-	2_PE_ Tx02+	GND	4
GND	2_PE_ Rx01-	2_PE_ Rx01+	GND	2_PE_ Tx01-	2_PE_ Tx01+	GND	2_PE_ Rx00-	2_PE_ Rx00+	GND	2_PE_ Tx00-	2_PE_ Tx00+	3
1_PE_ Rx07-	1_PE_ Rx07+	GND	1_PE_ Tx07-	1_PE_ Tx07+	GND	1_PE_ Rx06-	1_PE_ Rx06+	GND	1_PE_ Tx06-	1_PE_ Tx06+	GND	2
GND	1_PE_ Rx05-	1_PE_ Rx05+	GND	1_PE_ Tx05-	1_PE_ Tx05+	GND	1_PE_ Rx04-	1_PE_ Rx04+	GND	1_PE_ Tx04-	1_PE_ Tx04+	1
L	K	J	I	H	G	F	E	D	C	B	A	

Table 13: Pinout for CompactPCI Serial Connector P3

8_SATA _Rx-	8_SATA _Rx+	GND	8_SATA _Tx-	8_SATA _Tx+	GND	7_SATA _Rx-	7_SATA _Rx+	GND	7_SATA _Tx-	7_SATA _Tx+	GND	8
GND	6_SATA _Rx-	6_SATA _Rx+	GND	6_SATA _Tx-	6_SATA _Tx+	GND	5_SATA _Rx-	5_SATA _Rx+	GND	5_SATA _Tx-	5_SATA _Tx+	7
4_SATA _Rx-	4_SATA _Rx+	GND	4_SATA _Tx-	4_SATA _Tx+	GND	3_SATA _Rx-	3_SATA _Rx+	GND	3_SATA _Tx-	3_SATA _Tx+	GND	6
GND	2_SATA _Rx-	2_SATA _Rx+	GND	2_SATA _Tx-	2_SATA _Tx+	GND	8_USB3 _Rx-	8_USB3 _Rx+	GND	8_USB3 _Tx-	8_USB3 _Tx+	5
7_USB3 _Rx-	7_USB3 _Rx+	GND	7_USB3 _Tx-	7_USB3 _Tx+	GND	6_USB3 _Rx-	6_USB3 _Rx+	GND	6_USB3 _Tx-	6_USB3 _Tx+	GND	4
GND	5_USB3 _Rx-	5_USB3 _Rx+	GND	5_USB3 _Tx-	5_USB3 _Tx+	GND	4_USB3 _Rx-	4_USB3 _Rx+	GND	4_USB3 _Tx-	4_USB3 _Tx+	3
3_USB3 _Rx-	3_USB3_ Rx+	GND	3_USB3 _Tx-	3_USB3 _Tx+	GND	2_USB3 _Rx-	2_USB3_ Rx+	GND	2_USB3 _Tx-	2_USB3 _Tx+	GND	2
GND	8_ USB2 -	8_ USB2 +	GND	7_ USB2 -	7_ USB2 +	GND	6_ USB2 -	6_ USB2 +	GND	5_ USB2 -	5_ USB2 +	1
L	K	J	I	H	G	F	E	D	C	B	A	

Table 14: Pinout for CompactPCI Serial Connector P4

6_PE_ Rx03-	6_PE_ Rx03+	GND	6_PE_ Tx03-	6_PE_ Tx03+	GND	6_PE_ Rx02-	6_PE_ Rx02+	GND	6_PE_ Tx02-	6_PE_ Tx02+	GND	8
GND	6_PE_ Rx01-	6_PE_ Rx01+	GND	6_PE_ Tx01-	6_PE_ Tx01+	GND	6_PE_ Rx00-	6_PE_ Rx00+	GND	6_PE_ Tx00-	6_PE_ Tx00+	7
5_PE_ Rx03-	5_PE_ Rx03+	GND	5_PE_ Tx03-	5_PE_ Tx03+	GND	5_PE_ Rx02-	5_PE_ Rx02+	GND	5_PE_ Tx02-	5_PE_ Tx02+	GND	6
GND	5_PE_ Rx01-	5_PE_ Rx01+	GND	5_PE_ Tx01-	5_PE_ Tx01+	GND	5_PE_ Rx00-	5_PE_ Rx00+	GND	5_PE_ Tx00-	5_PE_ Tx00+	5
4_PE_ Rx03-	4_PE_ Rx03+	GND	4_PE_ Tx03-	4_PE_ Tx03+	GND	4_PE_ Rx02-	4_PE_ Rx02+	GND	4_PE_ Tx02-	4_PE_ Tx02+	GND	4
GND	4_PE_ Rx01-	4_PE_ Rx01+	GND	4_PE_ Tx01-	4_PE_ Tx01+	GND	4_PE_ Rx00-	4_PE_ Rx00+	GND	4_PE_ Tx00-	4_PE_ Tx00+	3
3_PE_ Rx03-	3_PE_ Rx03+	GND	3_PE_ Tx03-	3_PE_ Tx03+	GND	3_PE_ Rx02-	3_PE_ Rx02+	GND	3_PE_ Tx02-	3_PE_ Tx02+	GND	2
GND	3_PE_ Rx01-	3_PE_ Rx01+	GND	3_PE_ Tx01-	3_PE_ Tx01+	GND	3_PE_ Rx00-	3_PE_ Rx00+	GND	3_PE_ Tx00-	3_PE_ Tx00+	1
L	K	J	I	H	G	F	E	D	C	B	A	

Table 15: Pinout for CompactPCI Serial Connector P5

8_PE_ CLK-	8_PE_ CLK+	8_PE_ CLKE#	7_PE_ CLK-	7_PE_ CLK+	7_PE_ CLKE#	6_PE_ CLK-	6_PE_ CLK+	6_PE_ CLKE#	5_PE_ CLK-	5_PE_ CLK+	5_PE_ CLKE#	6
4_PE_ CLKE#	4_PE_ CLK-	4_PE_ CLK+	3_PE_ CLKE#	3_PE_ CLK-	3_PE_ CLK+	2_PE_ CLKE#	2_PE_ CLK-	2_PE_ CLK+	1_PE_ CLKE#	1_PE_ CLK-	1_PE_ CLK+	5
8_PE_ Rx03-	8_PE_ Rx03+	GND	8_PE_ Tx03-	8_PE_ Tx03+	GND	8_PE_ Rx02-	8_PE_ Rx02+	GND	8_PE_ Tx02-	8_PE_ Tx02+	GND	4
GND	8_PE_ Rx01-	8_PE_ Rx01+	GND	8_PE_ Tx01-	8_PE_ Tx01+	GND	8_PE_ Rx00-	8_PE_ Rx00+	GND	8_PE_ Tx00-	8_PE_ Tx00+	3
7_PE_ Rx03-	7_PE_ Rx03+	GND	7_PE_ Tx03-	7_PE_ Tx03+	GND	7_PE_ Rx02-	7_PE_ Rx02+	GND	7_PE_ Tx02-	7_PE_ Tx02+	GND	2
GND	7_PE_ Rx01-	7_PE_ Rx01+	GND	7_PE_ Tx01-	7_PE_ Tx01+	GND	7_PE_ Rx00-	7_PE_ Rx00+	GND	7_PE_ Tx00-	7_PE_ Tx00+	1
L	K	J	I	H	G	F	E	D	C	B	A	

2.7.7.2 CompactPCI Serial Connector P6

The following table provides pinout information for connector P6. This connector is a designed to provide support for rear I/O.

Table 16: Legend for CompactPCI Serial Connector P6

SIGNAL TYPE	SIGNAL	I/O	DESCRIPTION
CompactPCI Serial	GPIO_CFG#	I	Serial/GPIO configuration select
	RTM_ID0, RTM_ID1	I	Rear transition module information
	SYS_WP#	I	System write protect
	BP(I/O)	I/O	Backplane I/O
Power	3V3	O	3.3V power supply (max. 0.5 A)
	5V	O	5V power supply (max. 0.5 A)
	Battery	I	RTC backup power supply
Ethernet	x_ETH_A..D- x_ETH_A..D+	I/O	Ethernet differential pairs A to D, ports 1 and 2 (x = 1 to 2)

Table 16: Legend for CompactPCI Serial Connector P6 (Continued)

SIGNAL TYPE	SIGNAL	I/O	DESCRIPTION
Serial	1CTS, 1DCD, 1DSR, 1DTR, 1RIN, 1RTS, 1RXD, 1TXD	I/O	COMA serial port
	2CTS/GPI1, 2DCD/GPI3, 2DSR/GPI2, 2DTR/GPO2, 2RIN/GPI4, 2RTS/GPO1, 2RXD/GPI0, 2TXD/GPO0	I/O	COMB serial port or GPIOs
DisplayPort	1_DP_0..3-/+	O	Differential pairs 0 to 3 of DisplayPort lanes
	1_DP_SCL	O	HDMI port control clock
	1_DP_SDA	I/O	HDMI port control data
	1_DP_AUX-/+	I/O	Differential pair for auxiliary channel data
	1_DP_HPD	I	Hot plug detect
USB	1_USB3_Tx-, 1_USB3_Tx+	O	Differential pair of USB 3.0 transmit lines
	1_USB3_Rx-, 1_USB3_Rx+	I	Differential pair of USB 3.0 receive lines
	x_USB2-, x_USB2+	I/O	Differential pair of USB 2.0 lines, port 1 to port 2 (x = 1 to 2)
	x_USB5V	O	Power supply for USB ports (x = 1 to 2) (max. 0.5 A)

Note: In the following table signals highlighted in white have not been implemented or are reserved.

Table 17: Pinout for CompactPCI Serial Connector P6

RTM_ID0	2DCD/ GPI3	2DTR/ GPO2	RTM_ID1	2RIN/ GPI4	2DSR/ GPI2	GND	1_DP_ AUX+	1_DP_ AUX-	GND	1_DP_ SDA	1_DP_ SCL	8
2RXD/ GPI0	2TXD/ GPO0	GND	2CTS/ GPI1	2RTS/ GPO1	GND	1_DP_2+	1_DP_2-	GND	1_DP_3+	1_DP_3-	GND	7
GND	1DCD	1DTR	GND	1RIN	1DSR	GND	1_DP_0+	1_DP_0-	GND	1_DP_1+	1_DP_1-	6
1RXD	1TXD	GND	1CTS	1RTS	GND	BP(I/O)	BP(I/O)	GND	BP(I/O)	BP(I/O)	GND	5
GND	2_USB2 +	2_USB2 -	GND	1_USB2 +	1_USB2 -	GND	1_USB3_ Tx+	1_USB3_ Tx-	GND	1_USB3_ Rx+	1_USB3_ Rx-	4
SYS_WP#	GPIO_ CFG#	GND	2_USB _5V	1_USB _5V	GND	5V	3V3	GND	1_DP_ HPD	Battery	GND	3
GND	2_ETH_ A+	2_ETH_ A-	GND	2_ETH_ B+	2_ETH_ B-	GND	2_ETH_ C+	2_ETH_ C-	GND	2_ETH_ D+	2_ETH_ D-	2
1_ETH_ A+	1_ETH_ A-	GND	1_ETH_ B+	1_ETH_ B-	GND	1_ETH_ C+	1_ETH_ C-	GND	1_ETH_ D+	1_ETH_ D-	GND	1
L	K	J	I	H	G	F	E	D	C	B	A	

3 Configuration

3.1 DIP Switch Configuration

The DIP switch SW1 provides switches for board configuration: POST code indication, SPI boot flash selection, system write protection configuration and uEFI BIOS configuration.

Figure 6: DIP Switch SW1

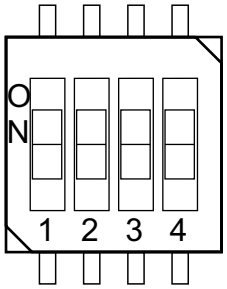


Table 18: DIP Switch SW1 Functionality

SWITCH	SETTING	FUNCTIONALITY
1	***OFF***	***Boot-up with POST code indication on LED3..0***
	ON	Boot-up with no POST code indication on LED3..0
2	***OFF***	***Boot from the standard SPI boot flash***
	ON	Boot from the recovery SPI boot flash
3	***OFF***	***Non-volatile memory write protection disabled*** (if no other write protection sources are enabled)
	ON	Non-volatile memory write protection enabled
4	***OFF***	***Boot using the currently saved uEFI BIOS settings***
	ON	Clear the uEFI BIOS settings and use the default values

The default setting is indicated by using italic bold.

To clear the uEFI BIOS settings and the passwords, proceed as follows:

1. Set DIP switch SW1, switch 4, to the ON position.
2. Apply power to the system.
3. Wait 30 seconds and then remove power from the system. During this time period no messages are displayed.
4. Set DIP switch SW1, switch 4, to the OFF position.

3.2 System Write Protection

The CPS3003-SA provides write protection for non-volatile memories via the DIP switch SW1, the uEFI Shell and a backplane pin. If one of these sources is enabled, the system is write protected. Please contact Kontron for further information before using these functions.

3.3 CPS3003-SA-Specific Registers

Table 19: CPS3003-SA-Specific Registers

ADDRESS	DEVICE
0x284	Write Protection Register (WPROT)
0x285	Reset Status Register (RSTAT)
0x28C	Watchdog Timer Control Register (WTIM)
0x290	LED Configuration Register (LCFG)
0x291	LED Control Register (LCTRL)
0x292	General Purpose Output Register (GPOUT)
0x293	General Purpose Input Register (GPIN)

3.3.1 Write Protection Register (WPROT)

The Write Protection Register holds the write protect signals for non-volatile devices.

Table 20: Write Protection Register (WPROT)

ADDRESS		0x284							
BIT		7	6	5	4	3	2	1	0
NAME		SWP	Reserved			SFWP	DSWP	BSWP	SSWP
ACCESS		R	R			R/W	R	R	R/W
RESET		0	000			0	0	0	0
BITFIELD		DESCRIPTION							
7	SWP	System write protection status: 0 = Onboard non-volatile memory devices not write protected 1 = Onboard non-volatile memory devices write protected							
3	SFWP	SATA Flash module write protection: 0 = SATA Flash module included in system write protection 1 = SATA Flash module not included in system write protection If this bit is programmed once, it cannot be reprogrammed.							
2	DSWP	This bit reflects the state of the system write protection via DIP switch: 0 = System not write protected (if BSWP or SSWP not set to '1') 1 = System write protected							
1	BSWP	This bit reflects the state of the system write protection via backplane (SYS_WP#): 0 = System not write protected (if DSWP or SSWP not set to '1') 1 = System write protected							
0	SSWP	This bit reflects the state of the system write protection via software: 0 = System devices not write protected (if DSWP or BSWP not set to '1') 1 = System write protected If this bit is programmed once, it cannot be reprogrammed.							

Note: As the uEFI BIOS programs the Write Protection Register at start-up, it cannot be written to again. Thus, this register is read-only.

3.3.2 Reset Status Register (RSTAT)

The Reset Status Register is used to determine the host's reset source.

Table 21: Reset Status Register (RSTAT)

ADDRESS	0x285							
BIT	7	6	5	4	3	2	1	0
NAME	PORS	Reserved				FPRS	CPRS	WTRS
ACCESS	R/W	R				R/W	R/W	R/W
RESET	N/A	0000				0	0	0

BITFIELD		DESCRIPTION
7	PORS	Power-on reset status: 0 = System reset generated by warm reset 1 = System reset generated by power-on (cold) reset Writing a '1' to this bit clears the bit.
2	FPRS	Front panel push button reset status (CPS3003-EXTIO/CPS3003-BRIDGE): 0 = System reset not generated by front panel reset 1 = System reset generated by front panel reset Writing a '1' to this bit clears the bit.
1	CPRS	CompactPCI Serial reset status (PRST signal): 0 = System reset not generated by CompactPCI Serial reset input 1 = System reset generated by CompactPCI Serial reset input Writing a '1' to this bit clears the bit.
0	WTRS	Watchdog timer reset status: 0 = System reset generated by Watchdog timer 1 = System reset generated by Watchdog timer Writing a '1' to this bit clears the bit.

Note: The Reset Status Register is set to default values by power-on (cold) reset, not by a warm reset.

3.3.3 Watchdog Timer Control Register (WTIM)

Table 22: Watchdog Timer Control Register (WTIM)

ADDRESS	0x28C							
BIT	7	6	5	4	3	2	1	0
NAME	WTE	WMD		WEN/WTR	WTM			
ACCESS	R/W	R/W		R/W	R/W			
RESET	0	00		0	0000			

BITFIELD		DESCRIPTION
7	WTE	Watchdog timer expired status bit: 0 = Watchdog timer has not expired 1 = Watchdog timer has expired. Writing a '1' to this bit resets it to 0.
6..5	WMD	Watchdog mode: 00 = Timer only mode 01 = Reset mode 10 = Interrupt mode 11 = Cascaded mode (dual-stage mode)
4	WEN/WTR	Watchdog enable / Watchdog trigger control bit: 0 = Watchdog timer not enabled Prior to the Watchdog being enabled, this bit is known as WEN. After the Watchdog is enabled, it is known as WTR. Once the Watchdog timer has been enabled, this bit cannot be reset to 0. As long as the Watchdog timer is enabled, it will indicate a '1'. 1 = Watchdog timer enabled Writing a '1' to this bit causes the Watchdog to be retriggered to the timer value indicated by bits WTM[3..0].
3..0	WTM	Watchdog timeout settings: 0000 = 0.125 s 0001 = 0.25 s 0010 = 0.5 s 0011 = 1 s 0100 = 2 s 0101 = 4 s 0110 = 8 s 0111 = 16 s 1000 = 32 s 1001 = 64 s 1010 = 128 s 1011 = 256 s 1100 = 512 s 1101 = 1024 s 1110 = 2048 s 1111 = 4096 s

3.3.4 LED Configuration Register (LCFG)

The LED Configuration Register holds a series of bits defining the onboard configuration for the front panel General Purpose LEDs.

Table 23: LED Configuration Register (LCFG)

ADDRESS	0x290							
BIT	7	6	5	4	3	2	1	0
NAME	Reserved				LCON			
ACCESS	R				R/W			
RESET	0000				0000			

BITFIELD		DESCRIPTION
3..0	LCON	LED3..0 configuration: 0000 = POST Mode (LEDs build a binary vector to display Port 80 signals) 0001 = General Purpose Mode (LEDs are controlled via the LCTRL register) 0010 - 1111 = Reserved

Beside the configurable functions described above, LED3..0 fulfill also a basic debug function during the power-up phase as long as the first access to Port 80 is processed. For further information on reading the 8-bit uEFI BIOS POST Code, refer to Chapter 2.7.1.2, “General Purpose LEDs”.

3.3.5 LED Control Register (LCTRL)

The LED Control Register enables the user to switch on and off the front panel General Purpose LEDs.

Table 24: LED Control Register (LCTRL)

ADDRESS	0x291							
BIT	7	6	5	4	3	2	1	0
NAME	LCMD				LCOL			
ACCESS	R/W				R/W			
RESET	0000				0000			

BITFIELD		DESCRIPTION	
7..4	LCMD	LED command:	
		0000 = Get LED0	1000 = Set LED0
		0001 = Get LED1	1001 = Set LED1
		0010 = Get LED2	1010 = Set LED2
		0011 = Get LED3	1011 = Set LED3
		0100 - 0111 = Reserved	1100 - 1111 = Reserved
3..0	LCOL	LED color: 0000 = Off 0001 = Green 0010 = Red 0011 = Red+Green 0100 - 1111 = Reserved	

Note: The LED Control Register can only be used if the General Purpose LEDs indicated in the “LED Configuration Register” (see Table 23) are configured in General Purpose Mode.

3.3.6 General Purpose Output Register (GPOUT)

The General Purpose Output Register holds the general purpose output signals of the rear I/O CompactPCI Serial connector P6. This register can be used only if the CPS3003-SA is ordered as a rear I/O version and the rear I/O GPIO operation is configured through the dedicated rear transition module configuration signal on the CompactPCI Serial connector P6.

Table 25: General Purpose Output Register (GPOUT)

ADDRESS	0x292							
BIT	7	6	5	4	3	2	1	0
NAME	Reserved					GPO2	GPO1	GPO0
ACCESS	R					R/W	R/W	R/W
RESET	00000					0	0	0

BITFIELD		DESCRIPTION
2..0	GPO2..0	General purpose output signals: 0 = Output low 1 = Output high

3.3.7 General Purpose Input Register (GPIN)

The General Purpose Input Register holds the general purpose input signals of the rear I/O CompactPCI Serial connector P6. This register can be used only if the CPS3003-SA is ordered as a rear I/O version and the rear I/O GPIO operation is configured through the dedicated rear transition module configuration signal on the CompactPCI Serial connector P6.

Table 26: General Purpose Input Register (GPIN)

ADDRESS	0x293							
BIT	7	6	5	4	3	2	1	0
NAME	Reserved			GPI4	GPI3	GPI2	GPI1	GPI0
ACCESS	R			R	R	R	R	R
RESET	000			1	1	1	1	1

BITFIELD		DESCRIPTION
4..0	GPI4.. 0	General purpose input signals: 0 = Input low 1 = Input high

Note: The CPS3003-SA provides pull-up resistors on the rear I/O signal pins GPI[4..0], which leads to the default setting “input high” if the inputs are not connected.

4 Power Considerations

4.1 CPS3003-SA Voltage Ranges

The CPS3003-SA has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The CPS3003-SA requires one main supply voltage (nominal: +12V DC). Stand-by voltage (nominal: +5V DC) is not required on the CPS3003-SA.

The system power supply must comply with the CompactPCI® Serial specification.

The following table specifies the ranges for the input power voltage within which the board is functional.

Table 27: DC Operational Input Voltage Range

INPUT SUPPLY VOLTAGE	OPERATING RANGE
Main Supply Voltage (nominal: +12V DC)	10.8 V min. to 13.2 V max.

Note: Failure to comply with the instructions above may result in damage to the board or improper operation.

4.2 Power Consumption

The goal of this description is to provide a method to calculate the power consumption for the CPS3003-SA baseboard and for additional configurations. The processor and the memory dissipate the majority of the thermal power.

The power consumption measurements were carried out using the following testing parameters:

- CPS3003-SA installed in the system slot
- Ethernet ports not connected
- 4 GB DDR3 SDRAM in dual-channel mode
- +12V main supply voltage
- 2.5 m/s airflow

The operating systems used were uEFI Shell and Windows® 7, 64-bit. All measurements were conducted at an ambient temperature of 25 °C. The power consumption values indicated in the tables below can vary depending on the ambient temperature. This can result in deviations of the power consumption values of up to 15%.

The power consumption was measured using the following the 3rd generation processors:

- Intel® Core™ i7-3612QE (SV) quad-core processor, 2.1 GHz, 6 MB L3 cache
- Intel® Core™ i7-3555LE (LV) dual-core processor, 2.5 GHz, 4 MB L3 cache
- Intel® Core™ i7-3517UE (ULV) dual-core processor, 1.7 GHz, 4 MB L3 cache

The power consumption was measured using the following configurations:

» Work load: uEFI Shell

For this measurement the processor cores were active, the graphics controller was in idle state (no application running) and Intel® Turbo Boost Technology was enabled.

» Work load: Idle

For this measurement all processor cores and the graphics controller were in idle state (no application running) and Intel® Turbo Boost Technology was enabled.

» Work load: Typical

For this measurement all processor cores were operating at maximum work load and the graphics controller was performing basic operation (e.g. dual-screen output configuration with no 3D graphics application running) while Intel® Turbo Boost Technology was disabled. These values represent the power dissipation reached under realistic, OS-controlled applications with the processor operating at maximum performance.

» Work load: Maximum

These values represent the maximum power dissipation achieved through the use of specific tools to heat up the processor cores and graphics controller. For this measurement Intel® Turbo Boost Technology was enabled. These values are unlikely to be reached in real applications.

Table 28: CPS3003-SA Power Consumption

WORK LOAD	TURBO BOOST	Intel® Core™ i7-3612QE (SV) 2.1 GHz	Intel® Core™ i7-3555LE (LV) 2.5 GHz	Intel® Core™ i7-3517UE (ULV) 1.7 GHz
uEFI Shell	on	14 W	14 W	14 W
Idle	on	13 W	12 W	11 W
Typical	off	29 W	24 W	17 W
Maximum	on	46 W	38 W	29 W

Note: The Intel® Core™ i7-3517UE (ULV) 1.7 GHz processor provides a software-configurable Thermal Design Power (TDP) that allows for reduction of the power consumption by up to 3.0 W. TDP can be configured via the **kboardconfig** uEFI Shell command. For information on this command, refer to the Chapter 12, uEFI BIOS.

The following table indicates the power consumption of the CPS3003-SA accessories.

Table 29: Power Consumption of CPS3003-SA Accessories

MODULE	POWER CONSUMPTION
DDR3 SDRAM update from 4 GB to 8 GB	approx. 1.0 W
DDR3 SDRAM update from 4 GB to 16 GB	approx. 2.0 W
SATA Flash module	approx. 1.0 W
Gigabit Ethernet (per interface)	approx. 0.5 W

5 Thermal Considerations

The thermal characteristic graphs shown in the following sections are intended to serve as guidance for reconciling the required computing power with the necessary system volumetric airflow over the ambient temperature. The graphs contain two curves representing upper level working points based on different levels of average CPU utilization. When operating below the corresponding curve, the CPU runs without any intervention of thermal supervision (the CPU is below 105°C). When operated above the corresponding curve, various thermal protection mechanisms may take effect resulting in temporarily reduced CPU performance or finally in an emergency stop (the CPU is at 125°C) in order to protect the CPU and the chipset from thermal destruction. In real applications this means that the board can be operated temporarily at a higher ambient temperature or at a reduced flow rate and still provide some margin for temporarily requested peak performance before thermal protection will be activated.

An airflow of 2.0 m/s to 3.0 m/s is a typical value for a standard *Kontron* ASM rack. For other racks or housings the available airflow will differ. The maximum ambient operating temperature must be determined for such environments.

How to read the diagram

Select a specific CPU and choose a specific working point. For a given flow rate there is a maximum airflow input temperature (= ambient temperature) provided. Below this operating point, thermal supervision will not be activated. Above this operating point, thermal supervision will become active protecting the CPU from thermal destruction. The minimum airflow rate provided must be more than the value specified in the diagram.

Volumetric flow rate

The volumetric flow rate refers to an airflow through a fixed cross-sectional area (i.e. slot width x depth. The volumetric flow rate is specified in m^3/h (cubic-meter-per-hour) or cfm (cubic-feet-per-minute) respectively.

Conversion: 1 cfm = 1.7 m^3/h; 1 m^3/h = 0.59 cfm

Airflow

At a given cross-sectional area and a required flow rate, an average, homogeneous airflow speed can be calculated using the following formula:

Airflow = Volumetric flow rate / area.

The airflow is specified in m/s (meter-per-second) or in fps (feet-per-second) respectively.

Conversion: 1 fps = 0.3048 m/s; 1 m/s = 3.28 fps

The following figures illustrate the thermal operational limits of the CPS3003-SA taking into consideration power consumption vs. ambient air temperature vs. airflow rate.

Note: The CPS3003-SA must be operated within the thermal operational limits indicated below.

5.1 Operational Limits for the CPS3003-SA

Figure 7: CPS3003-SA with i7-3612QE (SV), 2.1 GHz

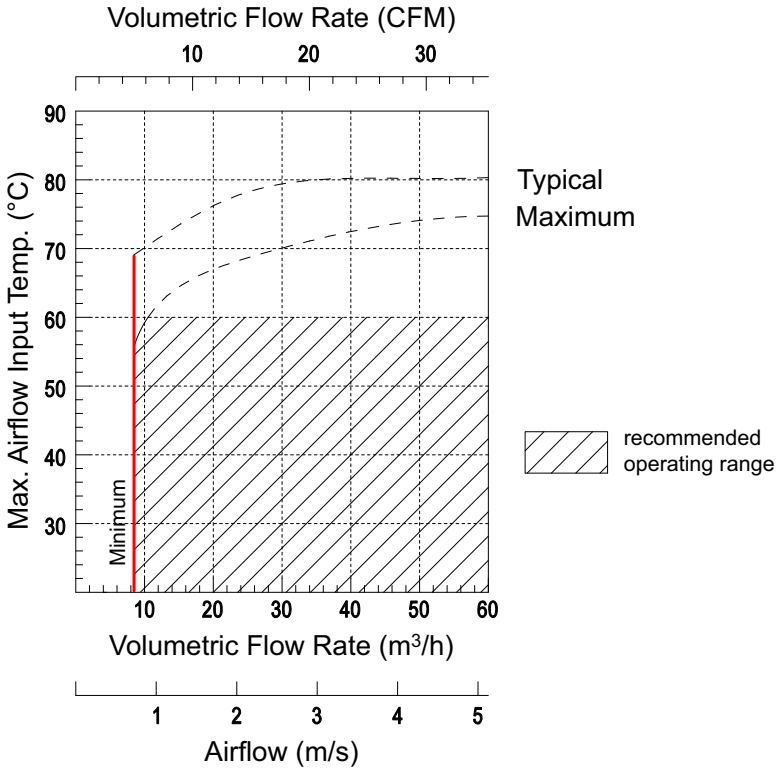


Figure 8: CPS3003-SA with i7-3555LE (LV), 2.5 GHz

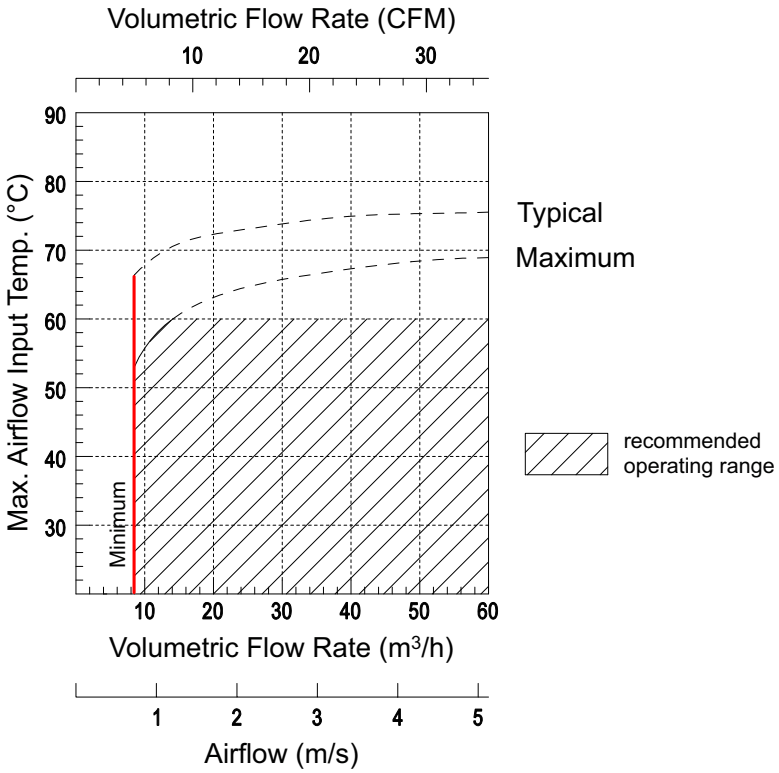
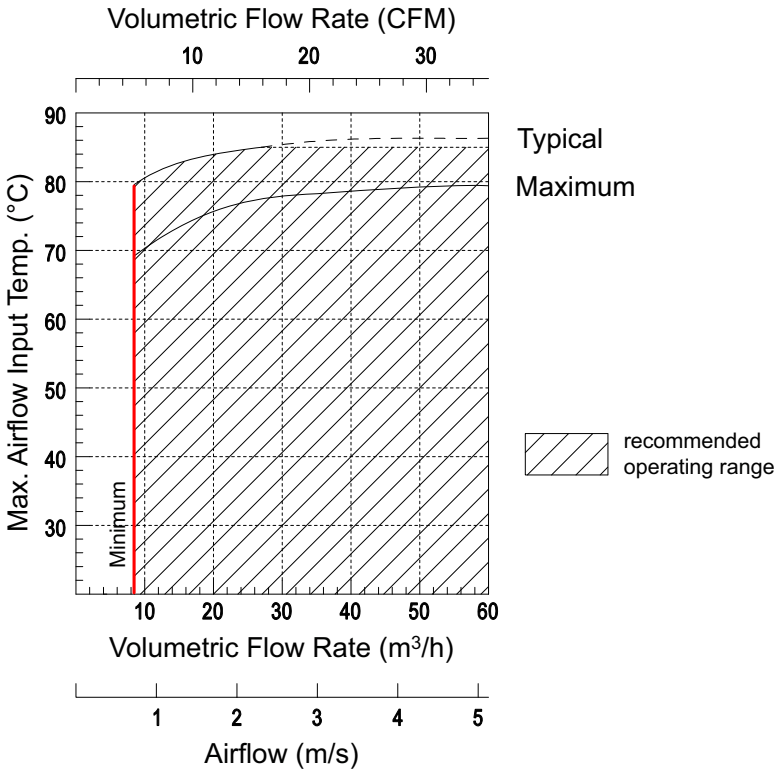


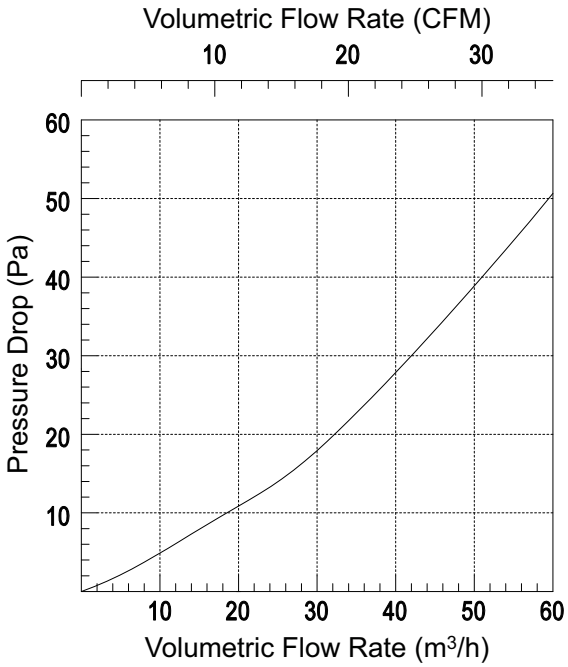
Figure 9: CPS3003-SA with i7-3517UE (ULV), 1.7 GHz



5.2 Airflow Impedance

To determine the cooling requirements of the CPS3003-SA, the airflow impedance has been measured. No card guides or struts have been used for the measurements because the resulting airflow impedance depends on individual configuration system.

Figure 10: CPS3003-SA Airflow Impedance



6 CPS3003-EXTIO Extension Module

6.1 Overview

The CPS3003-EXTIO is a factory-installed mezzanine extension module which along with an 8 HP front panel provides additional interfaces, such as:

- One USB 3.0 port
- One COM port (RJ-45 connector)
- One CFast socket
- One Reset switch
- One SATA activity LED

Note: If the CPS3003-EXTIO module is mounted on the CPS3003-SA, the SATA Flash module / Smart Extension Module cannot be used with the CPS3003-SA.

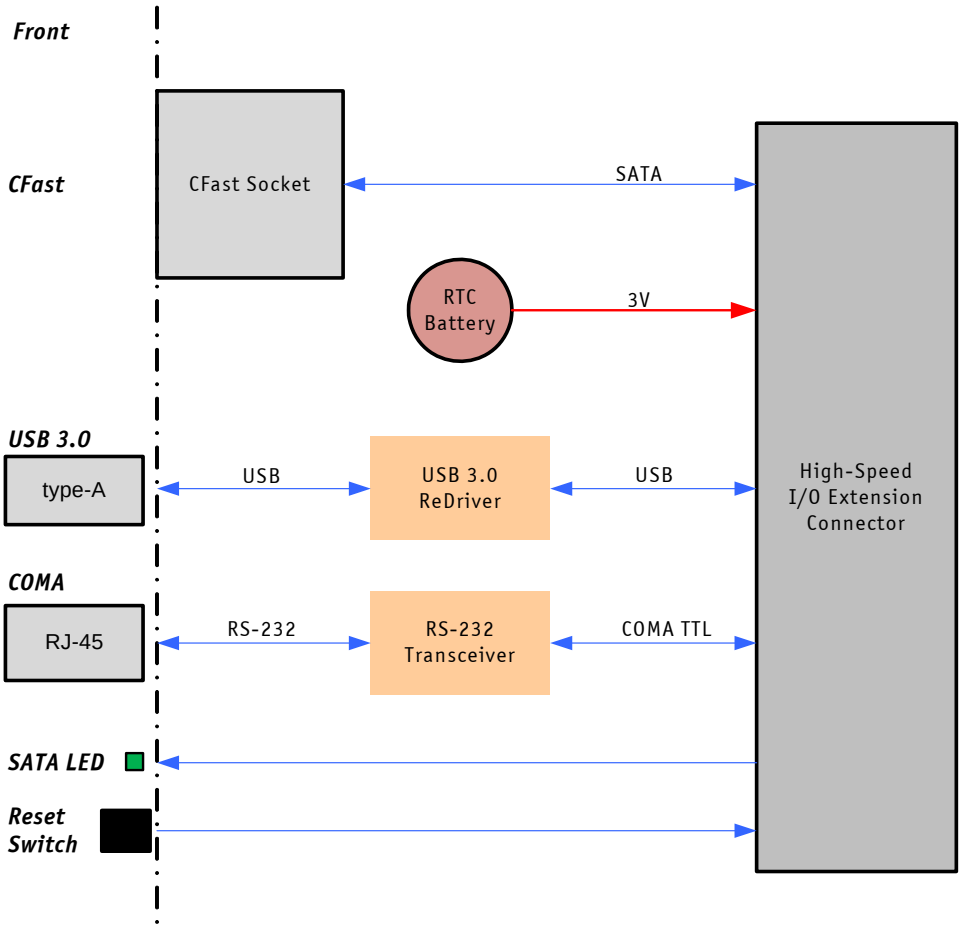
6.2 Technical Specifications

Table 30: CPS3003-EXTIO Module Specifications

FEATURES		SPECIFICATIONS
Front Panel Interfaces	CFast Socket	One CFast card socket, J4
	USB	One USB 3.0, type A connector, J5
	Serial Port	One 16C550-compatible serial port, COMA (RS-232) RJ-45 connector, J3
LEDs/ Switches	SATA LED (front panel)	One LED (green), indicates SATA activity
	Switch (front panel)	Reset switch, guarded
General	Power Consumption	Power consumption without CFast card and peripheral devices connected: approx. 1.0 W
	Temperature Range	Operational: 0°C to +60°C Standard -40°C to +85°C Extended Storage: -40°C to +85°C Without battery **Note:** When a battery is installed, refer to the operational specifications of the battery as this determines the storage temperature of the CPS3003-EXTIO module (see "Battery" below).
	Battery	3.0V lithium battery for RTC; Battery type: UL-approved CR2025 Temperature ranges: Operational (load): -20°C to +70°C typical (refer to the battery manufacturer's specifications for exact range) Storage (no load): -40°C to +70°C typical
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	CPS3003-EXTIO: 100 mm x 160 mm CPS3003-SA with CPS3003-EXTIO: 3U, 8 HP, CompactPCI Serial-compliant form factor
	Board Weight	100 grams (without CFast card)

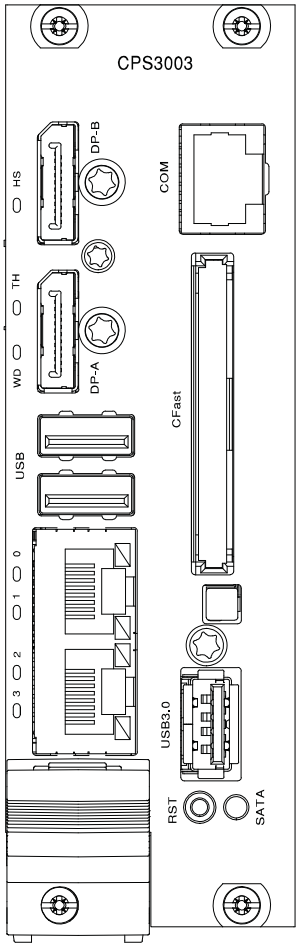
6.3 CPS3003-EXTIO Module Functional Block Diagram

Figure 11: CPS3003-EXTIO Module Functional Block Diagram



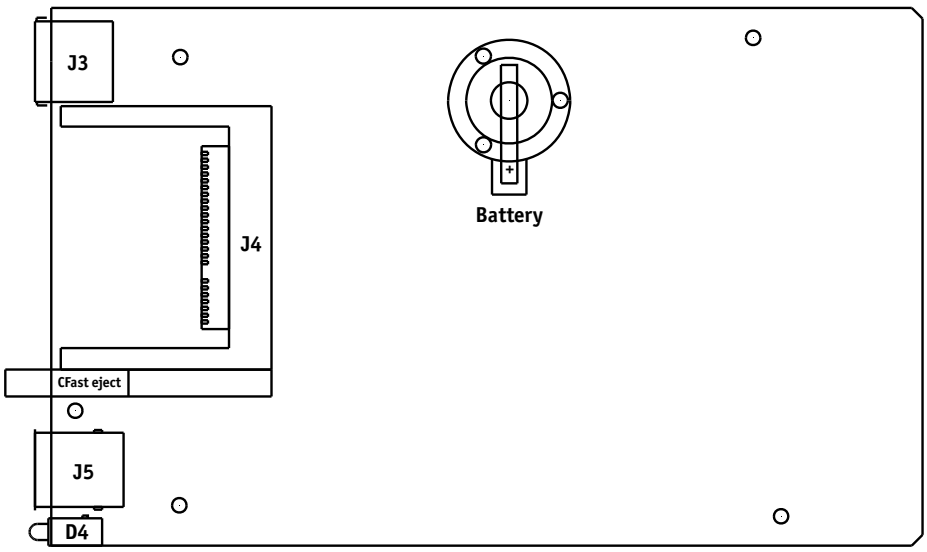
6.4 Front Panel of the CPS3003-SA with CPS3003-EXTIO Module

Figure 12: Front Panel of the 8 HP CPS3003-SA with CPS3003-EXTIO Module



6.5 CPS3003-EXTIO Module Board Layout

Figure 13: CPS3003-EXTIO Module Board Layout (Top View)



6.6 Module Interfaces (Front Panel and Onboard)

6.6.1 USB Interface

The CPS3003-EXTIO provides one standard, type A, USB 3.0 connector, J5.

6.6.2 Serial Port

The serial port is implemented as an 8-pin RJ-45 connector, J3.

Figure 14: Serial Port Connector J3

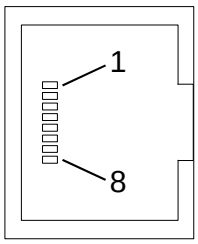


Table 31: Serial Port Connector J3 Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	RTS	Request to send	O
2	DTR	Data terminal ready	O
3	TXD	Transmit data	O
4	GND	Signal ground	--
5	GND	Signal ground	--
6	RXD	Receive data	I
7	DSR	Data send request	I
8	CTS	Clear to send	I

6.6.3 CFast Card Socket

To enable flexible flash expansion, a CFast card socket, J4, is available on the 8 HP CPS3003-SA with CPS3003-EXTIO.

7 CPS3003-BRIDGE Extension Module

7.1 Overview

The CPS3003-BRIDGE is a factory-installed mezzanine extension module which along with an 9 HP front panel provides additional interfaces as well as interfacing from the CPS3003-SA to a CPCI backplane in a hybrid-system:

- One USB 3.0 port
- One COM port (RJ-45 connector)
- One CFast socket
- One Reset switch
- One SATA activity LED
- CPCI backplane connectors

Note: If the CPS3003-BRIDGE module is mounted on the CPS3003-SA, the SATA Flash module / Smart Extension Module cannot be used with the CPS3003-SA.

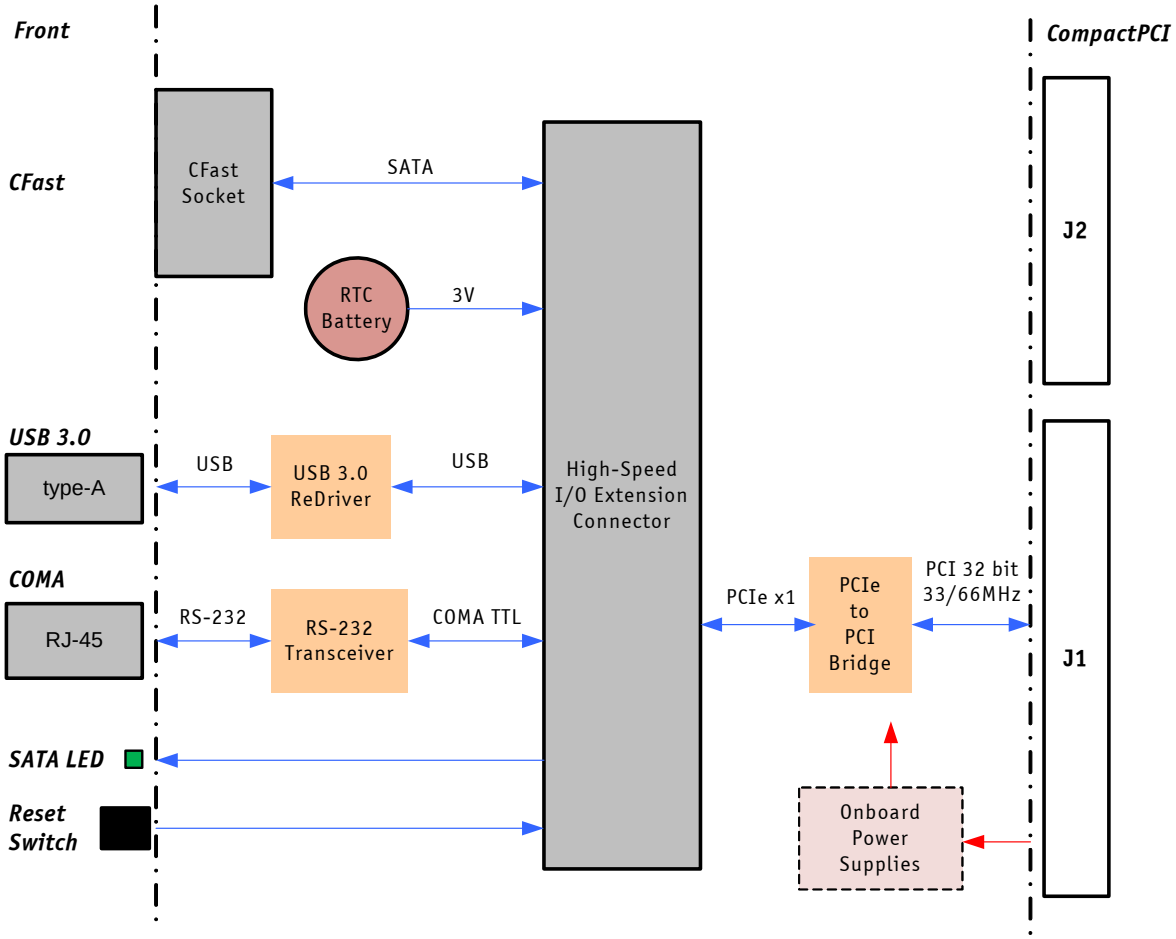
7.2 Technical Specifications

Table 32: CPS3003-BRIDGE Module Specifications

FEATURES		SPECIFICATIONS
Front Panel Interfaces	CFast Socket	One CFast card socket, J4
	USB	One USB 3.0, type A connector, J5
	Serial Port	One 16C550-compatible serial port (COMA), RJ-45 connector; J3
Onboard Interfaces	CompactPCI	Standard CPCI J1 and J2 connectors for interfacing the CPS3003-BRIDGE to a standard CPCI backplane **Note:** This configuration provides CompactPCI Serial and CompactPCI interfacing in a hybrid system.
LEDs/ Switches	SATA LED (front panel)	One LED (green), indicates SATA activity
	Switch (front panel)	Reset switch, guarded
General	Power Consumption	Power consumption without CFast card and peripheral devices connected: approx. 1.5 W
	Temperature Range	Operational: 0°C to +60°C Standard -40°C to +85°C Extended Storage: -40°C to +85°C Without battery **Note:** When a battery is installed, refer to the operational specifications of the battery as this determines the storage temperature of the CPS3003-EXTIO module (see "Battery" below).
	Battery	3.0V lithium battery for RTC; Battery type: UL-approved CR2025 Temperature ranges: Operational (load): -20°C to +70°C typical (refer to the battery manufacturer's specifications for exact range) Storage (no load): -40°C to +70°C typical
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	CPS3003-BRIDGE: 100 mm x 160 mm CPS3003-SA with CPS3003-BRIDGE: 3U, 9 HP, CompactPCI Serial-compliant form factor
	Board Weight	130 grams (without CFast card)

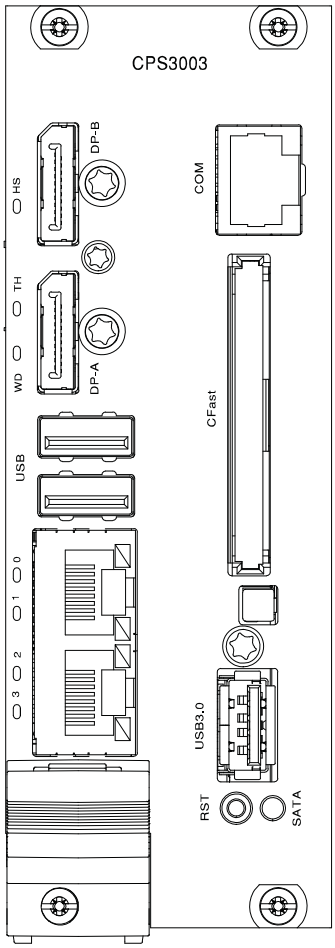
7.3 CPS3003-BRIDGE Module Functional Block Diagram

Figure 15: CPS3003-BRIDGE Module Functional Block Diagram



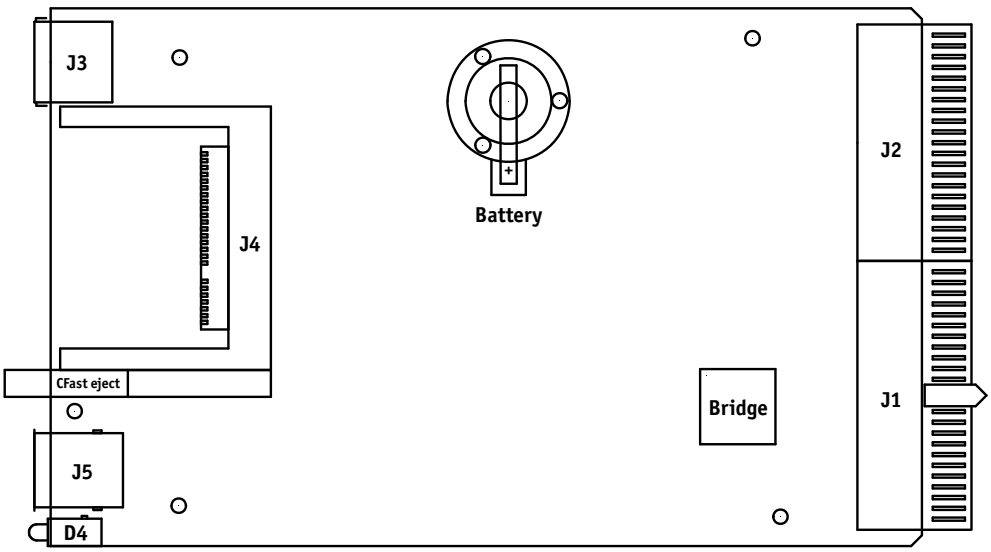
7.4 Front Panel of the CPS3003-SA with CPS3003-BRIDGE Module

Figure 16: Front Panel of the 9 HP CPS3003-SA with CPS3003-BRIDGE Module



7.5 CPS3003-BRIDGE Module Board Layout

Figure 17: CPS3003-EXTIO Module Board Layout (Top View)



7.6 Module Interfaces (Front Panel and Onboard)

7.6.1 USB Interface

The CPS3003-BRIDGE provides one standard, type A, USB 3.0 connector, J5.

7.6.2 Serial Port

The serial port is implemented as an 8-pin RJ-45 connector, J3.

Figure 18: Serial Port Connector J3

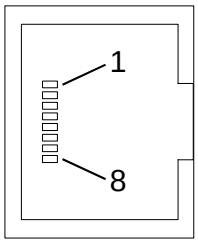


Table 33: Serial Port Connector J3 Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	RTS	Request to send	O
2	DTR	Data terminal ready	O
3	TXD	Transmit data	O
4	GND	Signal ground	--
5	GND	Signal ground	--
6	RXD	Receive data	I
7	DSR	Data send request	I
8	CTS	Clear to send	I

7.6.3 CFast Card Socket

To enable flexible flash expansion, a CFast card socket, J4, is available on the 9 HP CPS3003-SA with CPS3003-BRIDGE.

7.6.4 CompactPCI Interfaces

The CPS3003-SA provides two standard CompactPCI connectors, J1 and J2, with the following functionality:

- J1: 32-bit CompactPCI interface with PCI bus signals, arbitration, clock and power
- J2: arbitration and clock

The CPS3003-SA is capable of driving up to four 33/66 MHz CompactPCI slots with individual arbitration and clock signals.

7.6.5 CompactPCI Connector Keying

The CPS3003-SA supports universal (3.3 V and 5 V) PCI V(I/O) signaling voltages. Therefore, the CPS3003-SA can be inserted in both, 3.3 V and 5 V CompactPCI systems and provides itself no guide lug.

8 CPS-RIO3-01 Rear Transition Module

8.1 Overview

The CPS3003-SA provides rear I/O connectivity for peripherals. Some standard PC interfaces are implemented and assigned to the front panel and to the rear I/O connector rJ6 on the CPS3003-SA. When the CPS-RIO3-01 rear transition module is used, the signals of some of the main board/front panel connectors are routed to the module interface.

To support the rear I/O feature, a 3U CompactPCI Serial backplane with rear I/O support on the rear backplane connector rP6 is required. The CPS-RIO3-01 rear transition module provides the following interfaces:

- One CompactPCI Serial rear I/O
- One USB 2.0 port
- One USB 3.0 port
- Two Gigabit Ethernet ports without LED signals
- Two COM ports (onboard headers)
- One DisplayPort
- System write protection jumper

8.2 Technical Specifications

Table 34: CPS-RIO3-01 Rear Transition Module Specifications

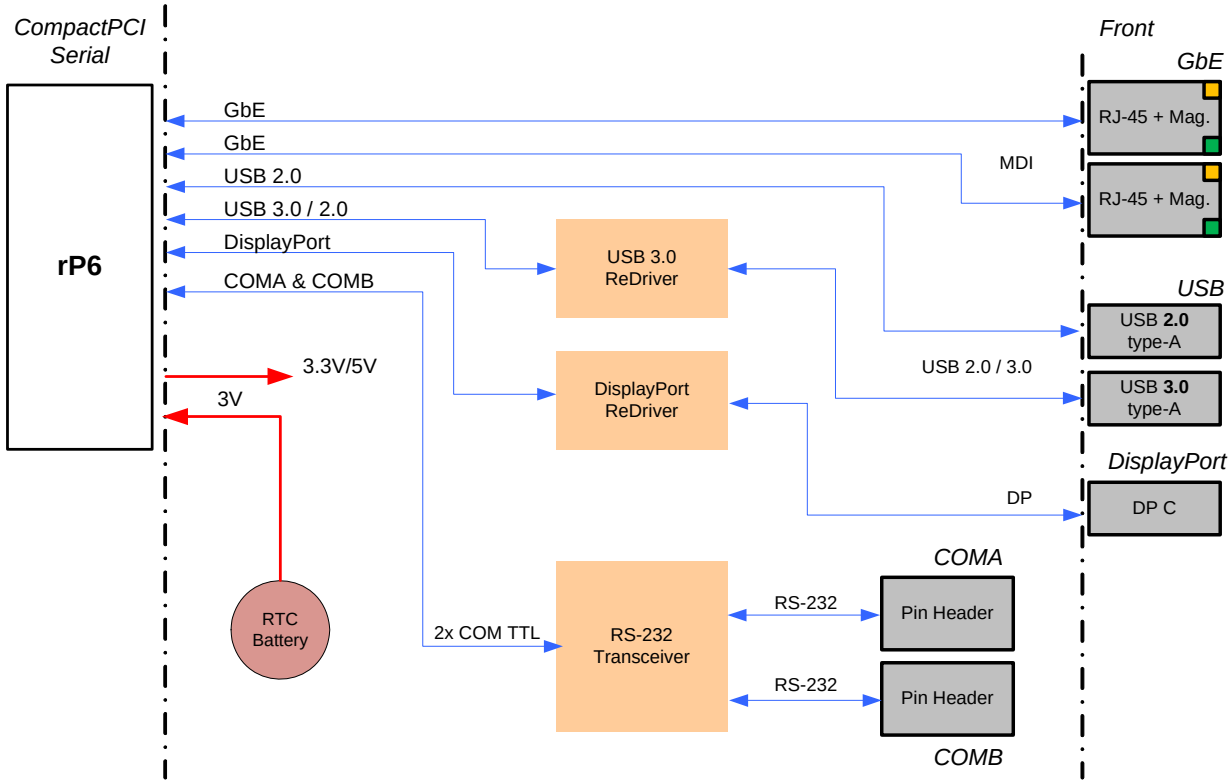
FEATURES		SPECIFICATIONS
External Interfaces	USB 2.0	One USB 2.0 type A connector, J4
	USB 3.0	One USB 3.0 type A connector, J3
	DisplayPort	One DisplayPort connector, J5
	Ethernet	Two Gigabit Ethernet interfaces implemented as dual RJ-45 connector without LEDs, J2A/B
Internal Interfaces	CompactPCI Serial	CompactPCI Serial connector, rJ6, for rear I/O backplane connection
	Serial	Two COM ports (COMA and COMB) implemented as two 10-pin, 2.54 mm onboard connectors with full modem support, J7 (COMB) and J8 (COMA)
General	Power Consumption	Power consumption without peripheral devices connected: approx. 1.0 W
	Temperature Range	Operational: 0°C to +60°C Standard -40°C to +85°C Extended Storage: -40°C to +85°C Without battery **Note:** When a battery is installed, refer to the operational specifications of the battery as this determines the storage temperature of the CPS3003-EXTIO module (see "Battery" below).
	Battery	3.0V lithium battery for RTC; Battery type: UL-approved CR2025 Temperature ranges: Operational (load): -20°C to +70°C typical (refer to the battery manufacturer's specifications for exact range) Storage (no load): -40°C to +70°C typical

Table 34: CPS-RIO3-01 Rear Transition Module Specifications (Continued)

FEATURES		SPECIFICATIONS
General	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	100 mm x 80 mm (4 HP)
	Board Weight	120 grams

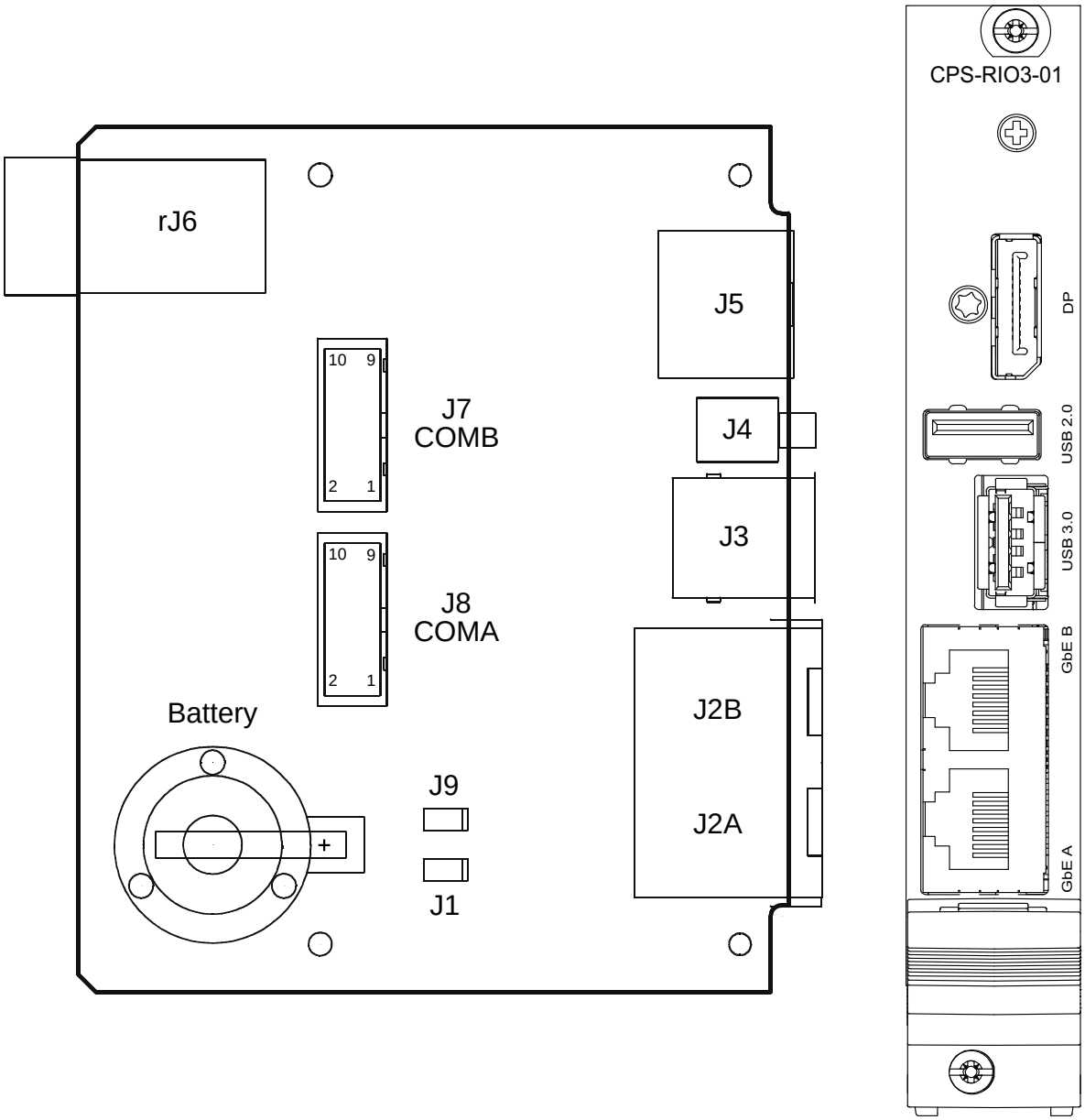
8.3 CPS-RIO3-01 Module Functional Block Diagram

Figure 19: CPS-RIO3-01 Module Functional Block Diagram



8.4 CPS-RIO3-01 Rear Transition Module Layout

Figure 20: CPS-RIO3-01 Rear Transition Module Layout



8.5 Module Interfaces

8.5.1 USB Interfaces

The CPS-RIO3-01 rear transition module provides one standard, type A, USB 2.0 connector, J4, and one standard, type A, USB 3.0 connector, J3.

8.5.2 DisplayPort Interface

The CPS-RIO3-01 provides one standard DisplayPort connector.

8.5.3 Gigabit Ethernet Interface

Two Gigabit Ethernet interfaces are available on the CPS-RIO3-01. The Ethernet connectors are realized as RJ-45 connectors without LEDs.

8.5.4 COM Interface

The CPS-RIO3-01 rear transition module provides two COM ports, COMA and COMB, for connection to RS-232 devices. The COM signals are available on the onboard 10-pin serial port connectors J7 (COMB) and J8 (COMA).

The following table provides pinout information for the onboard serial port connectors J7 and J8. Refer to the module layout figure for connector and pin locations.

Table 35: Serial Port Connectors J7 (COMB) and J8 (COMA) Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	DCD	Data carrier detect	I
2	DSR	Data send request	I
3	RXD	Receive data	I
4	RTS	Request to send	O
5	TXD	Transmit data	O
6	CTS	Clear to send	I
7	DTR	Data terminal ready	O
8	RI	Ring indicator	I
9	GND	Signal ground	--
10	NC	Not connected	--

8.5.5 Rear I/O Interface on CompactPCI Serial Connector rP6

For pinout information regarding this interface, refer to the P6 description in the “Functional Description” chapter of this User Guide.

8.5.6 System Write Protection

The jumper J9 provides hardware setting of system write protection of non-volatile memory on the CPS3003-SA. For further information refer to the “Configuration” chapter of this User Guide.

9 Smart Extension Module

9.1 Overview

The 4 HP CPS3003-SA provides an optional Smart Extension Module for facilitating the connection to system-internal USB and SATA devices. The Smart Extension Module includes one SATA cable connector as well as one USB 2.0 connector.

Note: When the Smart Extension Module is mounted on the CPS3003-SA, the SATA Flash module , the CPS3003-EXTIO module or the CPS3003-BRIDGE module cannot be used with the CPS3003-SA.

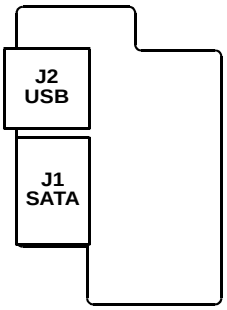
9.2 Technical Specifications

Table 36: Smart Extension Module Specifications

	FEATURES	SPECIFICATIONS
Interfaces	USB Connector	One 4-pin, type A, standard USB 2.0 connector, J2
	SATA Connector	One 7-pin, L-form standard SATA connector, J1
General	Temperature Range	Operational: 0°C to +60°C Standard -40°C to +85°C Extended Storage: -40°C to +85°C
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	48 mm x 33 mm **Note:** If a Smart Extension Module is installed on the CPS3003-SA, the board exceeds 4 HP.
	Board Weight	11 grams

9.3 Smart Extension Module Layout

Figure 21: Smart Extension Module Layout (Top View)



9.4 Module Interfaces

9.4.1 USB Interface

The Smart Extension Module provides one standard, type A, USB 2.0 connector, J2.

9.4.2 SATA Interface

The Smart Extension Module provides one high-performance SATA interface. The SATA interface is implemented as one standard SATA cable connector, J1, which is used to connect a standard HDD/SSD or another SATA device to the CPS3003-SA via the Smart Extension Module.

10 SATA Flash Module

10.1 Overview

The 4 HP CPS3003-SA provides an optional SATA Flash module with up to 32 GB NAND flash memory. The SATA Flash module is connected to the CPS3003-SA via the J16 connector located on the CPS3003-SA and the J1 connector located on the SATA Flash module.

Note: If the SATA Flash module is mounted on the CPS3003-SA, the Smart Extension Module , the CPS3003-EXTIO module or the CPS3003-BRIDGE module cannot be used with the CPS3003-SA.

10.2 Technical Specifications

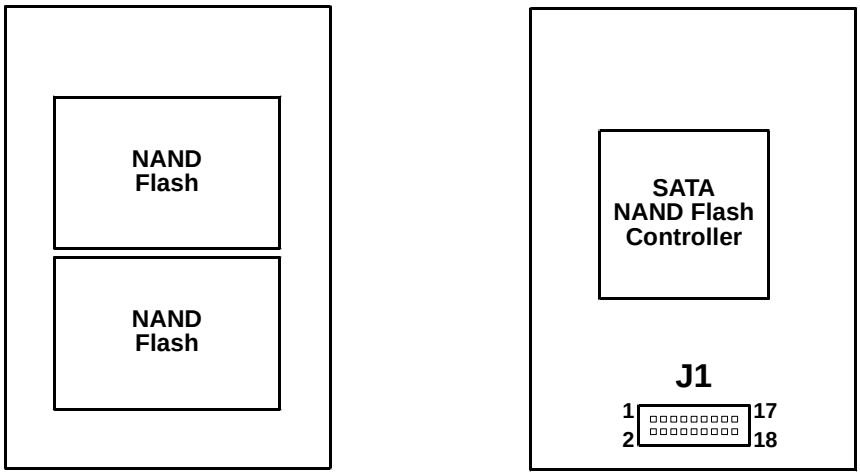
Table 37: SATA Flash Module Specifications

FEATURES		SPECIFICATIONS
Interface	Board-to-Board Connector	One 18-pin, female, board-to-board connector, J1
Memory	Memory	Mezzanine module that provides: » Up to 32 GB SLC-based NAND flash memory » Built-in full hard disk emulation » Up to 60 MB/s read rate » Up to 55 MB/s write rate
General	Power Consumption	approx. 1.0 W
	Temperature Range	Operational: 0°C to +60°C Standard -40°C to +85°C Extended Storage: -40°C to +85°C
	Climatic Humidity	93% RH at 40°C, non-condensing (acc. to IEC 60068-2-78)
	Dimensions	38 mm x 27 mm
	Board Weight	ca. 6 grams

Note: Write protection is available for the SATA Flash module. Please contact Kontron for further assistance if write protection is required.

10.3 SATA Flash Module Layout

Figure 22: SATA Flash Module Layout (Top and Bottom Views)



11 Installation

This chapter is oriented towards an application environment. Some aspects may, however, be applicable to a development environment.

11.1 Safety

To ensure personnel safety and correct operation of this product, the following safety precautions must be observed:

- All operations involving the CPS3003-SA require that personnel be familiar with system equipment, safety requirements and the CPS3003-SA.
- This product contains electrostatically sensitive components which can be seriously damaged by electrical static discharge (ESD). Therefore, proper handling must be ensured at all times.
- Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.
- Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.
- Do not touch components, connector-pins or traces.

Kontron assumes no liability for any damage resulting from failure to comply with these requirements.

11.2 General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

11.3 Board Installation

The CPS3003-SA is designed for use either as a system board or as an autonomous CPU board in a peripheral slot.

When installed in the system slot, the CPS3003-SA provides all required functions for supporting the hot swapping of peripheral boards which are capable of being hot swapped.

When installed in a peripheral slot, the CPS3003-SA operates autonomously, meaning that it only draws power from the backplane.

11.3.1 Hot Swap Insertion

Prior to following the steps below, ensure that the safety requirements are met.

To insert the CPS3003-SA in a running system proceed as follows:

1. Ensure that the board ejection handle is open.
2. Insert the board into the slot designated until it makes contact with the backplane connectors.
3. Using the ejector handle, engage the board with the backplane. When the ejector handle is closed, the board is engaged.
4. The blue HS LED turns on and then off indicating that the CPS3003-SA is operating.
5. Fasten the front panel retaining screws.
6. Connect all external interfacing cables to the board as required.

11.3.2 Hot Swap Removal

Prior to following the steps below, ensure that the safety requirements are met. When removing a board from the system, particular attention must be paid to the components which may be hot, such as heat sink, etc.

To remove the CPS3003-SA from a running system proceed as follows:

1. Unlock the board ejection handle by pressing its release button.
   The blue HS LED starts blinking indicating that the shut down process has begun.
2. The HS LED turns on steady indicating that the CPS3003-SA may be removed from the system.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.
5. Using the ejector handle, disengage the board from the backplane and remove it from the system.

11.4 CFast Card Installation

The CPS3003-SA provides support for a CFast card via the CPS3003-EXTIO or the CPS3003-BRIDGE extension module. For the location of the CFast card socket on the CPS3003-EXTIO and CPS3003-BRIDGE extension modules, refer to Chapter 6 and Chapter 7, respectively.

To preclude damage or data loss when removing the CFast Card, ensure that the operating system has been informed of the pending removal and that the OS has indicated that it is safe to proceed.

11.5 Rear Transition Module Installation

The CPS-RIO3-01 rear transition module does not support hot swapping. Therefore, the system must have power removed to install or remove the CPS-RIO3-01 rear transition module. Before extracting the CPS-RIO3-01 rear transition module, ensure that all connected cables are disconnected.

11.6 Battery Replacement

The CPS3003-SA RTC may be backed up using a single 3.0 V “coin cell” lithium battery from one of three possible points of installation:

- onboard
- on an extension module
- on the rear transition module

Only one battery may be installed at a time. Refer to Table 1 for battery requirements.

12 uEFI BIOS

12.1 Starting the uEFI BIOS

The CPS3003-SA is provided with a Kontron-customized, pre-installed and configured version of Aptio® (referred to as uEFI BIOS in this manual), AMI's BIOS firmware based on the Unified Extensible Firmware Interface (uEFI) specification and the Intel® Platform Innovation Framework for EFI. This uEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the CPS3003-SA.

The uEFI BIOS comes with a Setup program which provides quick and easy access to the individual function settings for control or modification of the uEFI BIOS configuration. The Setup program allows the accessing of various menus which provide functions or access to sub-menus with more specific functions of their own.

To start the uEFI BIOS Setup program, follow the steps below:

1. Power on the board.
2. Wait until the first characters appear on the screen (POST messages or splash screen).
3. Press the <DEL> or <F2> key.
4. If the uEFI BIOS is password-protected, a request for password will appear.

Enter either the User password or the Administrator password (see Chapter 12.2.3, Security Menu), press <RETURN>, and proceed with step 5.

5. A Setup menu will appear.

The CPS3003-SA uEFI BIOS Setup program uses a hot key-based navigation system. A hot key legend is located in the right frame on most Setup screens. The following table provides information concerning the usage of these hot keys.

Table 38: Navigation

HOT KEY	DESCRIPTION
<F1>	The <F1> key is used to invoke the General Help window.
<F2>	The <F2> key is used to restore the previous values.
<F3>	The <F3> key is used to load the defaults.
<F4>	The <F4> key is used to save the current settings and exit the uEFI BIOS Setup.
→ ←	The *Right and Left* <Arrow> keys are used to select a major Setup screen. For example: Main Screen, Advanced Screen, Chipset Screen, etc.
↑ ↓	The *Up and Down* <Arrow> keys are used to select a Setup function or a sub-screen.
+ -	The *Plus and Minus* <Arrow> keys are used to change the field value of a particular Setup function, for example, system date and time.
<ESC>	The <ESC> key is used to exit a menu or the uEFI BIOS Setup. Pressing the <ESC> key in a sub-menu causes the next higher menu level to be displayed. When the <ESC> key is pressed in a major Setup menu, the uEFI BIOS Setup is terminated without saving any changes made.
<Enter>	The <Enter> key is used to execute a command or select a menu.

12.2 Setup Menus

The Setup utility features four menus listed in the selection bar at the top of the screen:

- Main Menu
- Boot Menu
- Security Menu
- Save and Exit Menu

The Setup menus are selected via the left and right arrow keys. The currently active menu and the currently active uEFI BIOS Setup item are highlighted in white.

Each Setup menu provides two main frames. The left frame displays all the functions that can be configured. They are displayed in blue. Functions displayed in gray provide information about the status or the operational configuration. The right frame displays the key legend. Above the key legend there is an area reserved for a text message. When a function is selected in the left frame, it is displayed in white. Often a text message will accompany it.

12.2.1 Main Menu

Upon entering the uEFI BIOS Setup program, the Main menu screen is displayed. This screen lists the Main menu sub-screens and provides basic system information as well as functions for setting the system time and date.

Table 39: Main Menu Sub-Screens and Functions

SUB-SCREEN	FUNCTION	DESCRIPTION
Trusted Computing	TPM Support	Specifies the TPM configuration settings
	Current Status Information	Displays TPM status
CPU Configuration	CPU Configuration	Indicates general information about the installed CPU
	Max Freq Ratio	Selects the CPU frequency so as to make a reduction in power consumption when higher performance is not required To ensure that the maximum desired frequency is not exceeded, the CPU turbo mode must be disabled using the **kboardconfig** uEFI Shell command.
Firmware Update Configuration	Me FW Image Re-Flash	Enables/disables Intel Management Engine (ME) firmware re-flashing
USB Configuration	USB Devices	Indicates general information about the USB devices detected
	Legacy USB Support	Enables/disables legacy USB support This function is required for booting from USB devices and for operating systems which do not support USB themselves (mainly DOS and some BootLoaders).
	USB3.0 Support	Enables/disables USB 3.0 support
	XHCI Hand-off	Enables a workaround for operating systems without XHCI Hand-Off support The XHCI ownership change should be claimed by the XHCI driver.

Table 39: Main Menu Sub-Screens and Functions (Continued)

SUB-SCREEN	FUNCTION	DESCRIPTION
USB Configuration	EHCI Hand-off	Enables a workaround for operating systems without EHCI Hand-Off support The EHCI ownership change should be claimed by the EHCI driver.
	USB Mass Storage Driver Support	Enables USB Mass Storage Driver support
	USB transfer time-out	Selects the timeout in seconds that the USB core will wait for Control, Bulk, and Interrupt transfers
	Device reset time-out	Selects the timeout in seconds that the POST will wait for a USB mass storage device to become ready after start unit command
	Device power-up delay	Determines the maximum time the device will take before it properly reports itself to the Host Controller "Auto" uses a default value: for a Root port it is 100 ms, for a Hub port the delay is taken from Hub descriptor. If the "Manual" option is chosen, the device power up delay in seconds field will be enabled to accept a delay ranging from 1 to 40 seconds.
	Mass Storage Devices	Determines the emulation type of a mass storage device "Auto" enumerates devices according to their media format. Optical drives are emulated as "CDROM" and drives with no media will be emulated as drive type.
Serial Port Console Redirection [1)]	COM0	The COM0 port (serial port 0) corresponds to the COMA port
	Console Redirection	Enables/disables console redirection for the COMA port
	Console Redirection Settings	Provides functions for specifying the console redirection configuration settings for the COMA port
	COM1	The COM1 port (serial port 1) corresponds to the COMB port
	Console Redirection	Enables/disables console redirection for the COMB port
	Console Redirection Settings	Provides functions for specifying the console redirection configuration settings for the COMB port
	Serial Port for Out-of-Band Management/ Windows Emergency Management Services (EMS)	Controls the presence and content of the ACPI serial port redirection table (SPCR). This table is mainly used by the Windows server variants to provide Windows Emergency Management Services (EMS). This functionality is totally independent from serial redirection of other console output.
	Console Redirection	Adds/prevents the system from adding the SPCR table to the ACPI tables. The OS can further use the information provided for serial redirection services.
	Console Redirection Settings	Provides functions for specifying the console redirection configuration settings for the Out-of-Band Management / Windows Emergency Management Services (EMS).

Table 39: Main Menu Sub-Screens and Functions (Continued)

SUB-SCREEN	FUNCTION	DESCRIPTION
Intel ICC	New SSC Mode	Specifies the requested Spread Spectrum Clock (SSC) mode Please leave this function at the default setting to ensure reliable system operation. Changing the setting may lead to system instability.
	New SSC Spread Percentage	Specify the requested Spread Spectrum Clock (SSC) in 0.01% increments
	Apply Settings Immediately	Makes the setting of the “New SSC Spread Percentage” immediately valid if <RETURN> is pressed The changes will not remain valid after reboot.
	Apply Settings Permanently After Reboot	Makes the setting of the “New SSC Spread Percentage” permanently valid after reboot if <RETURN> is pressed

[1] Serial Port Console redirection can be used to remotely operate system settings and the uEFI console.

12.2.2 Boot Menu

This Boot Menu screen lists the functions for boot configuration and boot device priority.

Table 40: Boot Menu Functions

FUNCTION	DESCRIPTION
Setup Prompt Timeout	Sets an additional time the POST should wait for the operator to press the key to enter the uEFI BIOS Setup The time is entered in seconds.
Bootup NumLock State	Sets the state of the keyboard’s numlock function after POST
Quiet Boot	Displays either POST output messages or a splash screen during boot-up
Fast Boot	Enables/disables boot with initialization of a minimal set of devices required to launch active boot option
GateA20 Active	Enables/disables GateA20
Option ROM Messages	Controls the messages of the loaded PCI option ROMs If set to “Force BIOS”, a BIOS-compatible output is forced. This will show the option ROM messages. If set to “Keep Current”, the current video mode is kept. This will suppress option ROM messages. Option ROMs requiring interactive inputs may not work properly in this mode.
Interrupt 19 Trap Response	Specifies if legacy PCI option ROMs are allowed to capture software interrupt 19h
Launch CSM	Enables/disables CSM support
Boot Option Filter	Controls which devices the system can boot to
Launch PXE OpROM Policy	Controls the execution of the uEFI and Legacy PXE OpROM
Launch Storage OpROM Policy	Controls the execution of the uEFI and Legacy Storage OpROM
Other PCI Device ROM Policy	Controls the execution of OpROMs other than Network, Mass Storage and Video
PXE Boot Device	Controls which onboard Ethernet device is used for PXE boot

Table 40: Boot Menu Functions (Continued)

FUNCTION	DESCRIPTION
Boot Option #1..2	Form the boot order and are dynamically generated These functions represent either a legacy BBS (BIOS Boot Specification) class of devices or a native EFI boot entry. Press <RETURN> on each option to select the BBS class / EFI boot entry desired.
Hard Drive BBS Priorities	Leads to a sub-menu that allows configuring the boot order for a specific device class These options are only visible if at least one device for this class is present. These functions are dynamically generated.

12.2.3 Security Menu

This screen provides information about the passwords and functions for specifying the security settings.

Table 41: Security Menu Functions

FUNCTION	DESCRIPTION
Administrator Password	Changes or deletes the Administrator password If there is already a password installed, the system asks for this first. To clear a password, simply enter nothing and acknowledge by pressing <RETURN>. To set a password, enter it twice and acknowledge by pressing <RETURN>.
User Password	Sets, changes or deletes the User password If there is already a password installed, the system asks for this first. To clear a password, simply enter nothing and acknowledge by pressing <RETURN>. To set a password, enter it twice and acknowledge by pressing <RETURN>.
HDD Security Configuration	Allows access to set, modify and clear the harddisk User password The harddisk User password must be set to enable harddisk security. This function is only available if a HDD/SSD is detected which supports this function.

Note: The Administrator, User, and harddisk User passwords are case-sensitive.

12.2.3.1 Modes of Security

Table 42: Modes of Security

SETTING	DESCRIPTION
No password is set	Booting the system as well as entering the Setup is unsecured.
Only Administrator password is set	Booting the system is unsecured. For entering the Setup, the Administrator password is required.
Only User password is set	The password is required for booting the system as well as for entering the Setup menu. On every startup, the user will be asked for the password.
Both User and Administrator passwords are set	Either the User or the Administrator password is required for booting the system as well as for entering the Setup menu. If the User password is entered here, limited access to the Setup is granted. Entering the Administrator password provides full access to all Setup entries.

Note: The CPS3003-SA provides no factory-set passwords.

12.2.3.2 Remember the Password

It is highly recommended to keep a record of all passwords in a safe place. Forgotten passwords may lead to being completely locked out of the system.

If the system cannot be booted because neither the uEFI BIOS User password nor the Administrator password are known, refer to the Chapter 3.1, for information about clearing the uEFI BIOS settings, or contact Kontron for further assistance.

Note: The harddisk User password cannot be cleared using the above method.

12.2.4 Save and Exit Menu

This screen provides functions for handling changes made to the uEFI BIOS settings and the exiting of the Setup program.

Table 43: Save and Exit Menu Functions

FUNCTION	DESCRIPTION
Save Changes and Exit	Saves all changes made within the Setup to flash and continues the boot process as long as no option was altered that requires a reboot
Discard Changes and Exit	Discards all changes made within the Setup and continues the boot process
Save Changes and Reset	Saves all changes made within the Setup to flash and performs a reboot afterwards
Discard Changes and Reset	Discards all changes made within the Setup and performs a reboot afterwards
Save Changes (Save Options)	Saves all changes made within the Setup to flash and returns to Setup
Discard Changes (Save Options)	Discards all changes made within the Setup and returns to Setup
Restore Defaults (Save Options)	Restores all tokens to factory default
Save as User Defaults (Save Options)	Saves all current settings as user default The current Setup state can later be restored using “Restore User Defaults”.
Restore User Defaults (Save Options)	Restores all tokens to settings previously stored by “Save as User Defaults”
Boot Override	This group of functions includes a list of tokens, each of them corresponding to one device within the boot order. Select a drive to immediately boot that device regardless of the current boot order. If booting to uEFI Shell this way, an exit from the shell returns to Setup.

Note: The Setup will ask for confirmation prior to executing the above-mentioned commands.

12.3 The uEFI Shell

The Kontron uEFI BIOS features a built-in and enhanced version of the uEFI Shell. For a detailed description of the available standard shell scripting refer to the EFI Shell User's Guide. For a detailed description of the available standard shell commands, refer to the EFI Shell Command Manual. Both documents can be downloaded from the EFI and Framework Open Source Community homepage (http://sourceforge.net/projects/efi-shell/files/documents/).

Please note that not all shell commands described in the EFI Shell Command Manual are provided by the Kontron uEFI BIOS.

12.3.1 Introduction, Basic Operation

The uEFI Shell forms an entry into the uEFI boot order and is the first boot option by default.

12.3.1.1 Entering the uEFI Shell

To enter the uEFI Shell, follow the steps below:

1. Power on the board.
2. Wait until the first characters appear on the screen (POST messages or splash screen).
3. Ignore the message: "Press the <DEL> or <F2> key".
4. Press the ESC key within 5 seconds after a message such as the one below appears:

```
EFI Shell version 2.31 [4.651]
Current running mode 1.1.2
Device mapping table
blk0     :Removable HardDisk - Alias hd33b0b0b fs0
          Acpi(PNP0A03,0)/Pci(1D|7)/Usb(1, 0)/Usb(1, 0)/HD(Part1,Sig17731773)
...
Press the ESC key within 5 seconds to skip startup.nsh, and any other key to
continue.
```

The output produced by the device mapping table can vary depending on the board's configuration.

If the ESC key is pressed before the 5-second timeout has elapsed, the shell prompt is shown:

```
Shell>
```

12.3.1.2 Exiting the uEFI Shell

To exit the uEFI Shell, follow one of the steps below:

1. Boot the OS using the **kboot** uEFI Shelll command.
2. Boot the OS from the next device in the boot order using the **exit** uEFI Shelll command.
3. Reset the board using the **reset** uEFI Shell command.

12.3.2 Kontron-Specific uEFI Shell Commands

The Kontron uEFI implementation provides the following additional commands related to the specific HW features of the Kontron system.

Table 44: Kontron-Specific uEFI Shell Commands

COMMAND	DESCRIPTION
kBiosRevision	Displays the current uEFI BIOS revision
kboardconfig	Configures non-volatile board settings
kboardinfo	Shows a summary of board-specific data
kboot	Boots a legacy OS Not to be used for uEFI BootLoaders! If the requested device is not present, boot returns to shell. This command cannot boot native uEFI-aware operating systems. But since these are bootable from shell by calling their boot-loader, this is not necessary either. If a requested device is present but not bootable, uEFI continues to boot with the next bootable device in the boot order.
kbootnsh	Manages the flash-stored startup script If the shell is launched by the boot process, it executes a shell script stored in the flash. If the shell script terminates, the shell will continue the boot process. However, the shell script can also contain any other boot command.
kclearnvram	Clears the NVRAM to restore the system's default settings Since all uEFI settings are stored inside the NVRAM, the default settings are loaded after invoking this command.
kflash	Programs and verifies the SPI boot flashes holding the uEFI BIOS code uEFI BIOS binary files must be available from connected mass storage devices, such as USB flash drive or harddisk.
kmkramdisk	Creates a RAMdisk of variable size This command is used to perform file operations when no real filesystem is connected to the system.
kpassword	Controls uEFI Setup and Shell passwords This command is used to determine the status of both passwords (set or not set) and to set or clear the uEFI Shell and Setup passwords. Both user and superuser (Administrator) passwords can be controlled with this command. Call without options to get current password status. Entering an empty password clears the password.
kresetconfig	Controls the board's reset behavior This command controls if the board shall react on a CompactPCI Serial backplane reset if it is used in a peripheral slot. It has no effect if the board is installed in the CompactPCI Serial system slot. The parameter of this command is volatile and set to off at the next start.
kSettings	Verifies the validity of the Setup settings This command is used to create a binary file of the current Setup settings. This file can later be used to check whether the settings have changed or not. To use this command, a device with a FAT file system is required to be connected.
kwdt	Configures the Kontron onboard Watchdog This command is used to enable the Kontron onboard Watchdog with reset target before OS boot. This can be used to detect if the OS fails to boot and react by reset.

The uEFI Shell commands are not case-sensitive. Each uEFI Shell command is provided with a detailed online help that can be invoked by entering “<cmd> <space> <-?>” in the command line.

12.4 uEFI Shell Scripting

12.4.1 Startup Scripting

If the ESC key is not pressed and the timeout is run out, the uEFI Shell tries to execute some startup scripts automatically. It searches for scripts and executes them in the following order:

1. Kontron flash-stored startup script
2. If there is no Kontron flash-stored startup script present, the uEFI-specified **`startup.nsh`** script is used. This script must be located on the root of any of the attached FAT formatted disk drive.
3. If none of the startup scripts is present or the startup script terminates, the default boot order is continued.

12.4.2 Create a Startup Script

Startup scripts can be created using the uEFI Shell built-in editor **edit** or under any OS with a plain text editor of your choice. To create a startup shell script, simply save the script on the root of any FAT-formatted drive attached to the system. To copy the startup script to the flash use the **kbootnsh** uEFI Shell command.

In case there is no mass storage device attached, the startup script can be generated in a RAM disk and stored in the SPI boot flash using the **kmkramdisk** uEFI Shell command.

12.4.3 Examples of Startup Scripts

12.4.3.1 Automatic Booting from USB Flash Drive

Automatic booting is made from a USB flash drive, if present, otherwise the boot is made from the harddrive.

```
kboot -t usb-harddrive
kboot -t harddrive
```

If neither a USB flash drive nor a harddrive is present, the boot order is continued.

12.4.3.2 Execute Shell Script on Other Harddrive

This example (**startup.nsh)** executes the shell script named **bootme.nsh** located in the root of the first detected disc drive (**fs0**).

```
fs0:
bootme.nsh
```

12.4.3.3 Enable Watchdog and Control PXE Boot

The uEFI Shell provides environment variables used to control the execution flow.

The following sample start-up script shows two uEFI Shell environment variables, **wdt_enable** and **pxe_first**, used to control the boot process and the Watchdog.

```
echo -off
echo “Executing sample startup.nsh...”
if %wdt_enable% == “on” then
   kwdt -t 15
   echo “Watchdog enabled”
endif
if %pxe_first% == “on” then
   echo “forced booting from network”
   kboot -t network
endif
```

To create uEFI Shell environment variables, use the **set** uEFI Shell command as shown below:

```
Shell> set wdt_enable on
Shell> set pxe_first on
Shell> set
   pxe_first : on
   wdt_enable : on
Shell> reset
```

12.4.3.4 Handling the Startup Script in the SPI Boot Flash

In case there is no mass storage device attached, the startup script can be generated in a RAM disk and stored in the SPI boot flash using the following instructions:

1. Press <ESC> during power-up to log into the uEFI Shell.

2. Create a RAM disk and set the proper working directory as shown below:

```
Shell> kmkramdisk -s 3 myramdisk
Shell> myramdisk:
```

3. Enter the sample start-up script mentioned above in this section using the **edit** uEFI Shell command.

```
myramdisk:\> edit boot.nsh
```

4. Save the start-up script to the SPI boot flash using the **kbootnsh** uEFI Shell command.

```
myramdisk:\> kbootnsh -p boot.nsh
```

5. Reset the board to execute the newly installed script using the **reset** uEFI Shell command.

```
myramdisk:\> reset
```

6. If a script is already installed, it can be edited using the following **kbootnsh** uEFI Shell commands.

```
myramdisk:\> kbootnsh -g boot.nsh
myramdisk:\> edit boot.nsh
```

12.5 Updating the uEFI BIOS

BIOS updates are typically delivered as an Update CD ISO image. This ISO image needs just to be burned to a CD and booted. Follow the menu for updating the uEFI BIOS.

12.5.1 uEFI BIOS Fail-Over Mechanism

The CPS3003-SA has two SPI boot flashes programmed with the uEFI BIOS, a standard SPI boot flash and a recovery SPI boot flash. The basic idea behind that is to always have at least one working uEFI BIOS flash available regardless if there have been any flashing errors or not.

12.5.2 Updating Procedure

An Update CD ISO image is provided for flashing the latest uEFI BIOS on the standard SPI boot flash. The standard SPI boot flash can also be programmed with the latest uEFI BIOS via the **kflash -p** uEFI Shell command.

Note: To have the same content in both SPI boot flashes, clone the standard SPI boot flash to the recovery SPI boot flash using the **kflash** uEFI Shell Command.

12.5.3 uEFI BIOS Recovery

In case of the standard SPI boot flash being corrupted and therefore the board not starting up, the board can be booted from the recovery SPI boot flash if the DIP switch SW1, switch 2 is set to ON. For further information, refer to the Chapter 3.1, DIP Switch Configuration.

Note: The uEFI BIOS code and settings are stored in the SPI boot flashes. Changes made to the uEFI BIOS settings are available only in the currently selected SPI boot flash. Thus, switching over to the other SPI boot flash may result in operation with different uEFI BIOS code and settings.

12.5.4 Determining the Active Flash

Sometimes it may be necessary to check which flash is active. On the AMI Aptio-based uEFI BIOS, the information is available using the **kboardinfo** uEFI Shell command.

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