cPCI-MXS and cPCI-CXS

6U CompactPCI System Processor

TECHNICAL REFERENCE MANUAL

Version 1.0
December 1999

ref.: M1023_1.0

FOREWORD

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DOCUMENTATION SURVEY

CPCI-MXS/CXS Technical Reference Manual, Rev. 1.0

Your comments are valuable for us and will contribute to improve the quality of this product by completing and returning this form.

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   _____

   _____

Note : The latest release of the Technical Reference Manuals are available at

http://www.teknor.com/Technical_Information/English/man_extracts.htm

Please send your comments to :

Teknor Applicom inc
Technical Writing dept
616 Curé Boivin, Boisbriand
(Québec), Canada, J7G 2A7

Optional

Name _____

Company _____

Address _____

_____

Additional Comments

Your computer board has a standard non-rechargeable lithium battery. To preserve the battery lifetime, **the battery enable jumper is removed when you receive the board**. If you do not have any jumper cap, we suggest you to use the Watchdog Timer jumper cap.

EXERCISE CAUTION WHILE REPLACING LITHIUM BATTERY

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

ATTENTION

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie.

Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabriquant.

ACHTUNG

Explosionsgefahr bei falschem Batteriewechsel.

Verwenden Sie nur die empfohlenen Batterietypen des Herstellers. Entsorgen Sie die verbrauchten Batterien laut Gebrauchsanweisung des Herstellers.

ATENCION

Puede explotar si la pila no este bien reemplazada.

Solo reemplazca la pila con tipas equivalentes segun las instrucciones del manifacturo. Vote las pilas usadas segun las instrucciones del manifacturo.

IMPORTANT

J1 and J2 are de-facto industry standard as defined by PICMG

J3, J4 and J5 are user-defined connectors and will vary from various manufacturers. Contact our Technical Support to verify pinout compatibility with other chassis backplane vendors.

POWERING-UP THE SYSTEM

If you should encounter a problem, verify the following items:

- Make sure that all connectors are properly connected.
- Verify your boot diskette.
- If the system still does not start up properly, you should try booting your system with only the power cord and video monitor connected to the board this is the minimum required to see if the board is working).
- If you still are not able to start up your system, please refer to the emergency Procedure in the Appendix Section.
- If you still are not able to get your board up and running, contact our technical Support department for assistance.

PREVENTING VIRUSES

Teknor Applicom Inc. takes every precaution against computer viruses. For your protection, we have *safely sealed* all utility diskettes. If the seal is broken, **do not use the diskette**. Contact our Technical Support department for further instructions at (450) 437-5682 (Canada).

To safeguard against computer viruses in general, do not freely lend your utility diskettes and regularly perform virus scans on all your computer systems.

BIOS UPGRADE & AUTOMATIC CPLD HARDWARE UPGRADE

During the first system bootup after you update the Boot Block Flash BIOS with the UPGBIOS utility, the BIOS may need to upgrade the CPLD devices. **In such a case, do not interrupt the system in any way (power down, reset, mouse or keyboard functions). The devices will be damaged and your board rendered inoperative if you disturb the CPLD hardware upgrade process!**

If your device upgrade was successful, the following message is displayed under the "Status:" line prior to rebooting:

```
Update complete successfully, wait for the automatic reboot.
Rebooting in 5 second(s).
```

If the update is not successful, the following message appears under the "Status:" line:

```
ERROR: general failure programming CPLDs!
Please contact Teknor Applicom's technical support.
```

You must contact Teknor's technical support for further instructions.

ADAPTER CABLES

While adapter cables are provided from various sources, the pinout is often different. The direct crimp design offered by Teknor allows the simplest cable assembly. All cables are available from Teknor Sales Department.

YEAR 2000 COMPLIANCE NOTE

Important Note:

All systems with which Teknor products interface and/or the data that they receive must be themselves year 2000 (Y2K) compliant. Equally as well, any customer using a Teknor Y2K compliant product may experience problems with operating system and/or application software that do not correctly read the date (you should consult Teknor Y2K website information page and obtain the specific product Y2K compliance letter to confirm product compliance).

E*ven if the Operating system is Y2K compatible, application programs that use time and date may not properly handle or use the century data, and this can lead to failures in a system that is otherwise Y2K compatible*.

This date recognition problem does not result from any fault of the hardware, but from how the Time and Date are accessed or handled by the software. If the software reads the RTC directly, it could fail as the transition occurs, because the BIOS or Operating System has not had a chance to update the century byte. All programs should use either the appropriate OS calls or BIOS interrupt functions to access time and date information. Programs must also properly utilize all of the data that is returned, as the BIOS or Operating system could return the proper century data, but if the application ignores this data, a failure could result. The customer should check with its operating system and/or application software vendor(s) to determine what, if any, Y2K issues their installed software could have. If possible, the customer should consider performing tests to verify proper Y2K operation prior to December 31, 1999. If testing is to be performed, ensure that the test system is configured exactly like the systems in question.

Remember to test the OS, hardware, and all applications that are or will be installed on the system.

There is no way for Teknor to determine or predict the choice of operating systems, system software, or applications our customers will make. Teknor claims no legal responsibility for problems that may result from action or inaction taken regarding this information. Teknor provides this information as a service to our customers, knowing that software problems might result if this issue is not properly understood and addressed. Teknor strongly encourages all customers to investigate this matter fully.

DISCLAIMER

All information on Teknor Y2K readiness and Teknor product Y2K compliance is found at Teknor's Y2K website information page located at:

http://www.teknor.com/Technical_Information/English/Year2000.htm

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UNPACKING AND SAFETY PRECAUTIONS

Static Electricity

Since static electricity can damage the board, the following precautions should be taken:

1. Keep the board in its antistatic package, until you are ready to install it.
2. Touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
3. Handle the board by the edges.

Storage Environment

Electronic boards are sensitive devices. Do not handle or store devices near strong electrostatic, electromagnetic, magnetic or radioactive fields.

Power Supply

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

Unpacking

Follow these recommendations while unpacking:

1. After opening the box, save it and the packing material for possible future shipment.
2. Remove the board from its antistatic wrapping and place it on a grounded surface.
3. Inspect the board for damage. If there is any damage, or items are missing, notify Teknor immediately.

When unpacking you will find:

1. One cPCI-MXS , Mobile Pentium® II / III system processor
   or one CPCI-CXS, Celeron system processor
2. One Quick Reference sheet
3. One CDROM containing drivers.

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PART 1

PRODUCT DESCRIPTION

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1.1 PRODUCT SPECIFICATIONS

The cPCI-MXS and cPCI-CXS CompactPCI® industrial system processor features:

- Intel's enhanced performance Pentium® processor.
  - cPCI-MXS: low power Mobile Pentium® II processor, 333 MHz or low power Mobile Pentium®III 400 and 500MHz, 256KB on-die L2 pipelined burst cache.
  - cPCI-CXS: Celeron™ Processor up to 433MHz in a 370-pin PPGA Package with on-die 128KB L2 pipelined burst cache.
- 440BX AGP set.
- Supporting up to 768 MB SDRAM with parity or ECC.
- PCI Ultra DMA/33 IDE, SCSI-3.
- 64-bit AGP SVGA CRT controller.
- CompactFlash™ Disk interfacing on secondary EIDE channel, user upgradable, master/slave.
- Ports available
  - Two Universal Serial Bus (USB).
  - Two 10/100Mbps Ethernet.
  - Four serial ports (three RS-232 only: COM1, 2 and 4; one RS-232/422/485: COM3).
  - One Parallel port, bi-directional with all IEEE 1284 protocols supported with BIOS selectable IRQs and addressing.
  - Mouse and keyboard available through front plate or Rear Transition Module.
  - SCSI, 16-bit Ultra Wide up to 40Mbps, 8-bit Fast SCSI-2 up to 10Mbps, 8-bit Ultra SCSI up to 20Mbps (Adaptec AIC7880).
- Floppy interface (360KB to 1.44MB).
- Optional hard disk/floppy mezzanine module for high level of integration.
- High availability controller capable to detect the insertion or removal of HA CPCI peripheral boards.
- J3/J4/J5 connectors to handle I/O signals such as serial, parallel, and USB ports, Ethernet and video, SCSI, and IDE interfaces, keyboard, speaker, mouse, and reset signals, SMBus.

Software:

- Enable/disable of Ethernet and SCSI ports by software.
- Enable/disable of video by hardware.
- Serial/parallel port mapping/disable by software
- Remote operation/monitoring (VT-100 serial port console redirection),
- Programmable two-stage watchdog timer by software
- Fully compatible with existing application software using platforms PC and MS-DOS®, Windows® 3.1, Windows® 95, Windows® NT, Windows® 2000, OS/2® Warp, QNX™, NOVELL™, and UnixWare™.
- Supports: Advanced Configuration and Power Interface (ACPI 1.0), Advanced Power Management (APM 1.2), advanced thermal management (resume, overheat alarm and auto slow down) and Green support.
- Hardware monitor (voltages, temperature, and fan speed),

- Power failure circuit
- Two year warranty.

The cPCI-MXS and cPCI-CXS can be purchased either for front plate I/O interfacing (video serial port, Ethernet) or RTM (Rear Transition Module) I/O interfacing (no interconnection capability available on the front plate) through CPCI I/O connectors and backplane.

CompactPCI Connectors

Rear panel CPCI connectors are PICMG 2.0 Rev2.1 CompactPCI™ specification compliant. CompactPCI connectors are located at the rear edge of the board. The complete CPCI connector configuration is composed of five connectors referred to as J1, J2, J3, J4, and J5.

Their function is described below:

J1/J2 * carry out arbitration and PCI bus signals, and power.

J3/J4/J5 * handle I/O signals.

CompactPCI™ connector is also known as 2mm Hard Metric connector.

> NOTE
>
> J1-J5 are marked as P1-P5 on the cPCI-MXS silk screen.

1.2 HOT SWAP CAPABILITY

The cPCI-MXS and cPCI-CXS support Hot Swap capability which means that hot swappable boards can be removed from or installed in the system while online (without powering-down the system).

Hot Swap consists of board hardware with the Hot Swap additions to the Hardware Connection Layer, and the Hot-Plug Service. Upon insertion of the board (any hot swappable board but the system host, cPCI-MXS or cPCI-CXS), the hardware connection layer will initialize the board and the Hot-Plug Service provides the means for reconfiguring the system.

High Availability is an attribute of a system designed to keep running (maintain availability) in the event of a system component failure. To provide a high degree of availability, a system requires a higher degree of control.

High Availability (HA) uses a higher degree of control than just indicating insertion and extraction. HA systems are able to control the Hardware Connection Process. To do this, the capabilities of the system are extended to allow software control of a board's hardware connection state. A hardware connection sequence is made possible through the use of different pin lengths and the process ends with the mating of the shortest pin (BD_SEL#).

The platform adds hardware to provide more control of each board's Hardware Connection Layer. The signals: BD_SEL#, HEALTHY#, and PCI_RST# are used to individually control each slot of the system.

BD_SEL# is one of the shortest pins. This pin is the last to mate and the first to break contact. This ensures that the sensing of its connection takes place at a time when all other pins are reliably connected. It is driven low to enable power on. For systems not implementing hardware connection control, it is grounded on the backplane.

HEALTHY# is used to acknowledge the health of the board. It signals that a board is suitable to be released from reset and allowed onto the PCI bus. In an HA system, the software can detect a faulty board when it fails to assert HEALTHY# after BD_SEL# has been asserted. A running board can also become not healthy at any time.

PCI_RST# as defined by the CompactPCI® Specification, is a bussed signal on the backplane, driven by the system host. Platforms may implement this signal as a radial signal from the Hot Swap Controller to further control the electrical connection process. Platforms that do this must OR the system host's reset signal with the slot specific signal to maintain the bussed signal's function.

The Software Connection Control resources on the board provide a signal (ENUM#) for system host notification and a switch and LED to interface with the operator.

Full Hot Swap boards drive the ENUM# signal to the system host to indicate a service request. This signal is provided to notify the system host that either a board has been freshly inserted or is about to be extracted. This signal informs the system host that the configuration of the system has changed. The system host then performs any necessary maintenance such as installing a device driver upon board insertion, or unloading drivers for hot swap boards that are about to be extracted. The application that is using the board is also notified that the resource will no longer be available.

The Hot Swap Switch allows the operator to indicate desire to extract the board. A blue LED, located on the front of the board, is illuminated when it is safe to extract the board. This LED indicates that system software has been placed in a state for orderly extraction of the board. The hardware connection layer provides protection only for the hardware during insertions and extractions. This method allows the operator to insert or extract boards without the extra step of reconfiguring the system at the console.

All actions are initiated by the operator, and must be performed in the correct sequence for proper system operation.

Full Hot Swap boards present the following resources to software executing on the system host (nominally implementing the Hot-Plug Service and Hot-Plug System Driver)

- An ENUM# signal, which is an open collector (open drain) bussed signal, to signal a change in status for the board.
- A switch, actuated with the lower ejector handle, indicated the beginning of the extraction process or end of the insertion process.
- An LED to indicate the status of the software connection process.
- A set of four control and status bits on each board allows the system host's software to determine the source of the ENUM# signal and control the LED.

Full Hot Swap boards allow the full range of system capabilities.

1.3 INTERFACING WITH THE ENVIRONMENT

CPCI

The cPCI-MXS and cPCI-CXS system processors are provided for rack-mounted systems to offer the highest modularity. Through the J1/J2 segment, the board can drive up to seven external CompactPCI slots, supporting individual REQ/GNT arbitration pair signals and clock.

NOTE

All I/O signals are available in front I/O and rear I/O configuration.

A. In front I/O configuration, the following I/Os signals are available on the faceplate : SVGA, COM1, Ethernet 1 and 2, keyboard and mouse. All other I/Os are connected to J3-J5.

B. In Rear I/O configuration, all I/O signals are connected to J3-J5

A backplane dedicated to the cPCI-MXS and cPCI-CXS is provided by Teknor, and is referred to as cBP

08R CPCI Passive Backplane.

Mezzanine

The mezzanine is a hardware interface concept introduced by Teknor to increase the I/O connectivity of the cPCI-MXS and cPCI-CXS, but respecting the dual slot 6U form factor restrictions.

The onboard mezzanine connector features PCI bus, IDE, floppy, keyboard and mouse signals, for potential mezzanine applications: Teknor provides an optional storage mezzanine composed with a hard drive, a floppy disk drive.

Bridge A bridge can be added on the mezzanine to support 7 extra slots.

A complete *CompactPCI* development system CxP-0816 is also available from Teknor.

1.4 COMPATIBILITY WITH TEKNOR PRODUCTS

The cPCI-MXS and cPCI-CXS System Processors are members of the Teknor's CompactPCI product family.

The boards are fully compliant with the PICMG 2.0 Rev.2.1 and PICMG 2.1 CompactPCI specifications.

When building a basic environment around the cPCI-MXS or cPCI-CXS, the platform may be composed of any of the following devices:

- cPCI-MXS 6U System Processor
- cPCI-CXS 6U System Processor
- cMC Mezzanine card with hard disk and floppy disk drive
- cMCB Mezzanine card with bridge, hard disk and floppy disk
- cSM-DVDHD Storage module with DVD and Hard Disk
- cSM-DVD Storage module with DVD only
- CxP0816 including
    - 8U 19-inch enclosure
    - Front loaded hot swappable 2U fan tray
    - Power supply (300W ATX or 350W AC or DC in single or redundant configuration)
    - One of the following backplanes

      cBP-08R : 8 slots CompactPCI (PICMG 2.1)

      cBP-16R, 16 slots CompactPCI (PICMG 2.1)

      cTBP-08R, Telephony 8 slots HA CompactPCI (PICMG 2.5)

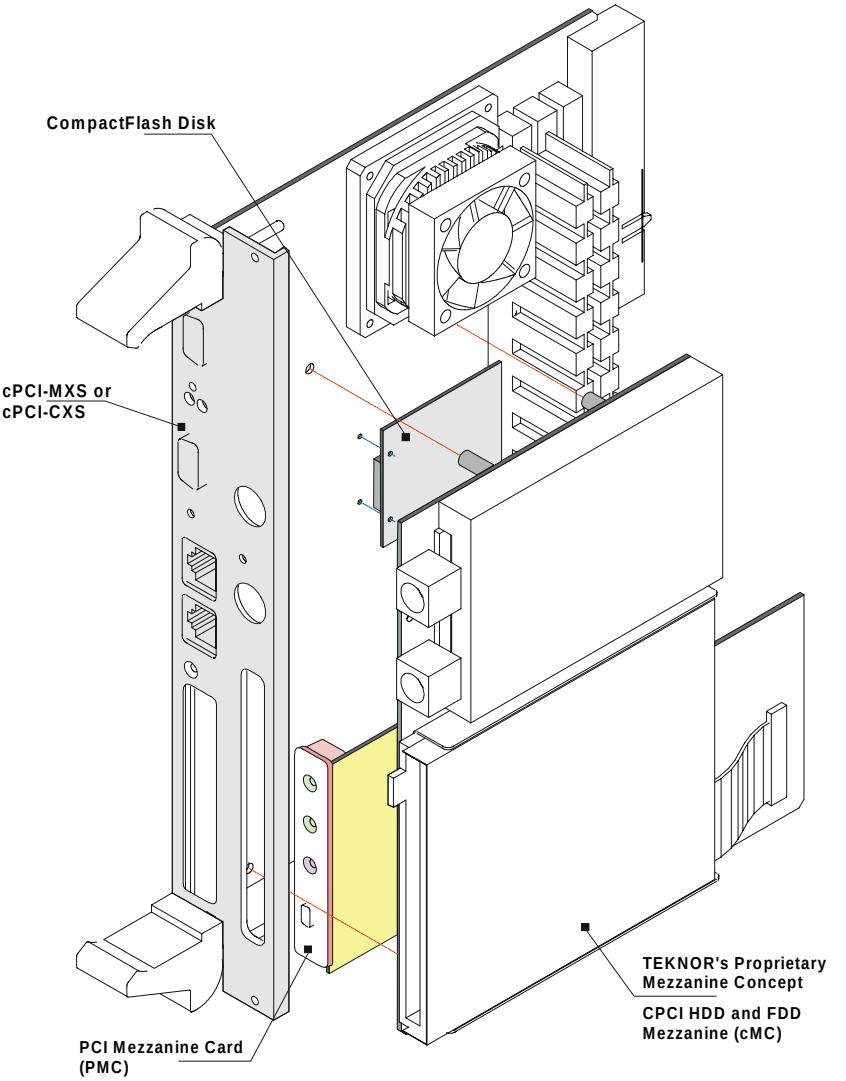
      cTBP-16R 16 slots Telephony HA CompactPCI (PICMG 2.5)

- cTM80-STD2S 6Ux8HPx80mm Rear Transition Module, standard pinout.

1.4.1 Mezzanine Card Concept

The capability of the cPCI-MXS or cPCI-CXS to connect with other devices is enforced by PCI Mezzanine Cards (PMC).

A fully equipped cPCI-CXS board may appear as follows:



1.4.2 Teknor's Mezzanine Concept

This is Teknor's concept to expand the I/O capability of the board. It is built around two connectors:

- Mezzanine connector handling IDE0 and floppy disk drive signals.
- Mezzanine connector handling a complete PCI signal set (primary bus) including the REQ/GNT arbitration signal pair.

These two connectors represent an open door for future development of expansion and I/O mezzanine cards.

A Mezzanine Card referred to as cMC and cMCB are available from Teknor.

1.4.3 PMC Concept

PCI Mezzanine Card (PMC) is a standard specification that allows PCI I/O devices to be connected to the PCI bus. It conforms to the ANSI/IEEE P1386.1 specification that defines Standard Physical and Environmental Layers for PMC devices.

The cPCI-MXS and cPCI-CXS feature the PMC concept onboard to provide an extra method to support the 32-bit I/O devices available on the market.

PMC devices connect directly to standard PMC connectors. A mechanical cutout (with its EMI proof cap) is provided to allow integrated connectors and indicators to be available directly on the front plate through PMC card.

1.4.4 CompactFlash Feature

The cPCI-MXS and cPCI-CXS boards also support standard CompactFlash disk through a CompactFlash module.

CompactFlash disk is a method of storing and transferring data. It is supported on the board as a standard IDE drive and connects to the secondary EIDE interface.

The CompactFlash drive can be set as a Master or Slave device and combined with any standard hard disk drive by setting the jumper W11 (see Section 3.1, setting jumpers).

CompactFlash is installed on J60 for the cPCI-MXS and J18 for the cPCI-CXS connector. For more information on CompactFlash installation and setups, please refer to Section 2.1 – *CompactFlash Interface*.

PART 2

ONBOARD FEATURES

1. COMPACTFLASH INTERFACE
2. ENHANCED IDE INTERFACES
3. ETHERNET INTERFACES
4. FLOPPY DISK INTERFACE
5. PS/2 KEYBOARD AND MOUSE INTERFACE
6. PARALLEL PORT
7. POWER MANAGEMENT
8. SCSI INTERFACE
9. SERIAL PORTS
10. THERMAL MANAGEMENT
11. USB INTERFACES
12. VIDEO INTERFACES

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2.1 COMPACTFLASH INTERFACE

The board supports an IDE compatible flash disk by using a CompactFlash module. CompactFlash (C-Flash) disks are the resident industry-standard ATA/IDE subsystem for application, data, image, and audio storage. They have the same functionality and capabilities as intelligent disk drives, but with the advantages of being very compact, rugged (typical M.T.B.F. is 1,000,000 hours) and low power. The cPCI-MXS/CXS supports all CompactFlash sizes presently available and future sizes when available.

The C-Flash disk connects on the cPCI-MXS or cPCI-CXS via the onboard Flash Disk connector.

Related Jumpers

cPCI-MXS : W11 to set the CompactFlash disk as master or slave.
cPCI-CXS : W3 to set the CompactFlash disk as master or slave.

BIOS Settings

Section 4.1.2 Main Menu: Hard Disk autodetect to set the type of hard disk.

Setups

The CompactFlash disk connects directly on the Secondary EIDE interface. It must be declared the same way as a standard hard disk using the BIOS setup program (Autodetect function).

To setup the CompactFlash disk for Master or Slave configuration, use the CompactFlash jumper located on the system processor.

To locate and install this jumper, please refer to Section 3.1, *Setting Jumpers*.

NOTE

Since device use ATA/IDE interface, no specific flash disk driver is required for various operating systems.

2.2 ENHANCED IDE INTERFACES

The board features two channel Bus Master PCI EIDE dedicated to Primary and Secondary IDE logical interfaces. Each channel supports up to two IDE devices (including CD-ROMs, hard disks, plus CompactFlash on the secondary IDE interface) with independent timings, in Master/Slave combination.

Signal Paths

The primary IDE interface is available through both the CPCI I/O connector and the Mezzanine connector.

The secondary IDE interface is only available through the CPCI I/O connector.

Related Jumpers

None

BIOS Settings

Section 4.1.11 Integrated Peripherals.

The IDE interfaces supports PIO mode 4 transfers up to 14MB/sec and Bus Master IDE transfer up to 33MB/sec (Ultra-DMA 33). It does not consume any ISA DMA resources and integrates 16x32-bit buffers for optimal transfers.

CAUTION

When connecting IDE devices to the Primary IDE interface (IDE0), Master and Slave devices must be shared in respect of the device allocation on both the CPCI I/O connector and the mezzanine

Two Master devices (or two Slave devices) must not be installed on the same interface at the same time.

2.3 ETHERNET INTERFACES

Both Ethernet controllers reside on the Primary PCI bus and are therefore Plug and Play by default.

Each interface supports 10Base-T and 100Base-TX specifications: 10Mbps and 100Mbps network speeds are automatically detected and switched.

Signal Path

See note on page 1.5.

Related Jumpers

None.

BIOS Settings

Section 4.1.11 Integrated Peripherals: Enable/Disable Ethernet Controller.

2.3.1 Front Plate Configuration

Ethernet 1 and 2 signals are available on front plate connectors only when the board is ordered for front access.

Activity and link indicators are built in connector.

2.3.2 CPCI I/O Configuration

Ethernet 1 and 2 signals are available on CPCI I/O connectors only when the board is ordered for rear access.

CAUTION

The combination of both front and rear panel configurations is not supported.

The Boot from LAN capability is supported. To enable the option, use the BIOS Setup program. Please refer to Section 4.1 BIOS Setup Program.

A diskette entitled “Network Drivers for Intel 82559 is included with the cPCI-MXS and the cPCI-CXS. It contains network drivers for most common operating systems.

2.4 FLOPPY DISK INTERFACE

The onboard floppy disk controller is IBM PC XT/AT compatible (single and double density). It handles 3.5” and 5.25”, low and high density disks. Up to two drives can be supported in any combination.

Signal Paths

The Floppy Disk Controller interface is available through the CPCI I/O connector and through the Mezzanine connector (see section 1.4.1)

Related Jumpers

None.

BIOS Settings

Section 4.1.4 Standard CMOS: Select type of floppy.
Section 4.1.11 Integrated Peripherals: Enable/Disable onboard FDC Controller.

2.5 PS/2 KEYBOARD / PS/2 MOUSE INTERFACE

The onboard keyboard controller is 8042 software compatible. PS/2 Keyboard and mouse signals are available through an output that supports direct connection to the interface. Since signals of both devices are combined on the same connector, a Y-cable is required to split the signals and feed a standard AT keyboard and a PS/2 mouse.

Signal Path

PS/2 keyboard and PS/2 mouse signals are available through J5 CPCI I/O connector and J14 Mezzanine connector (same connector number for cPCI-MXS and cPCI-CXS)

Related Jumpers

None.

BIOS Settings

11.3.7 Integrated Peripherals : USB Keyboard Support; PS/2 Mouse Function Control

2.6 PARALLEL PORT

The cPCI-MXS or cPCI-CXS features one multi-mode parallel port. It is compatible with Standard Mode IBM PC/XT, PC/AT, and PS/2 compatible bi-directional parallel port, Enhanced Parallel Port (EPP), and Enhanced Capabilities Port (ECP).

Signal Path

The Parallel Port interface is only available through J5 CPCI I/O connector.

Related Jumpers

None

BIOS Settings

Section 4.1.11 Integrated Peripherals: Onboard Parallel Port; Parallel Port Mode

The differences between Standard, EPP, and ECP modes appear in the signal assignation of the pins on the connector. Differences are described as follows:

Pin Number (J5)	Standard Mode	EPP Mode	ECP Mode
A15	SLCT	-	SLCT
B15	PE	-	PERROR[1], ACKREVERS[2]
C15	BUSY	WAIT	BUSY[1], PERIPHACK[2]
D15	/ACK	/INTR	/ACK
E16	/SLCTIN	/ADDRSTRB	/SLCTIN
B17	/INIT	-	/INIT[1], /REVERSERQST[2]
D17	/ERR	-	/FAULT[1], /PERIPHRQST[2]
A18	ALF	DATASTB	ALF[1], HOSTACK[2]
E17	PD0	PD0	PD0
C17	PD1	PD1	PD1
A17	PD2	PD2	PD2
D16	PD3	PD3	PD3
C16	PD4	PD4	PD4
B16	PD5	PD5	PD5
A16	PD6	PD6	PD6
E15	PD7	PD7	PD7

[1] Compatible mode

[2] High Speed Mode

NOTE

To operate in EPP or ECP mode, ensure the peripheral is designed to work in this mode and the BIOS setup is configured to support it.

2.6.1 Standard Mode

The Standard mode is unidirectional. It is supported to maintain the compatibility with the IBM PC standard.

2.6.2 EPP Mode

The EPP (Enhanced Parallel Port) mode consists of a hardware independent method of accessing a parallel port configured as EPP. It provides support for single I/O cycle as well as the high performance block I/O transfers. The EPP mode always uses the most optimum method for I/O transfers. For example, if the hardware supports it, EPP mode will perform 32-bit I/O block transfers.

EPP mode assumes that the parallel port can be used to connect more than one peripheral device using multiplexor or daisy chain configurations.

A multiplexor is an external device that permits up to eight parallel port devices to share a single parallel port.

A daisy chain device has two ports: input and output. The input port is connected either to the host parallel port or the daisy chain device in front of it. The output is used to connect the next peripheral device to the daisy chain. The last device, however, can be one without daisy chain support.

2.6.3 ECP Mode

ECP (Extended Capabilities Port) works the same as EPP mode, but it will take precedence over the EPP mode when addressing multiple logical devices in a single physical product. While the EPP mode may intermix read and write operations without any overhead or protocol handshaking, the ECP mode negotiates data transfers using a request from the host and an acknowledgment from the peripheral.

NOTE

For more information on the ECP protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard (available from Microsoft Corporation) or contact our Technical Support department.

2.7 POWER MANAGEMENT

Power Management features are supported at the BIOS level. All Power Management options are described in Section 4.1.8 – *Power Management Setup*.

2.8 SCSI INTERFACE

The boards feature wide UltraSCSI interface with 32-bit PCI bus master support and zero wait state transfer capabilities.

The Wide UltraSCSI interface supports operation up to 40Mbytes/sec. Signals are available through J4 CPCI I/O connector.

Signal Path

SCSI interface signals are only available through the J4 CPCI I/O connector or through RTM (Rear Transition Module).

Related Jumpers

W8 – To determine the SCSI termination (hardware, software or disabled) (same jumper number for cPCI-MXS and cPCI-CXS).

BIOS Settings

11.3.7 Integrated Peripherals: Enable/Disable the Onboard PCI SCSI Chip.

To operate with SCSI devices the onboard SCSI controller must enabled through the AWARD BIOS setup program.

To configure or view the default configuration setting for the SCSI host adapter, use the Adaptec SCSISelect utility available on the LAN Boot & SCSI Utility diskette 2.

To install the appropriate SCSI driver for a specific operating system, use the EZ-SCSI software available on the SCSI Utility diskette 1.

2.9 SERIAL PORTS

Four full function serial ports are provided on the board for asynchronous serial communications. They are 16C550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 50baud to 112Kbaud.

Each serial port is specified as follows:

Designation	Communication Mode	Output Path
Serial Port 1	RS-232	Front Plate DB-9, CPCI J5
Serial Port 2	RS-232	CPCI J3
Serial Port 3	RS-232, RS-422, RS-485	CPCI J5
Serial Port 4	RS-232	CPCI J3
Serial Port 3	Infrared	CPCI-J3

UART registers are individually addressable and fully programmable.

2.9.1 COM1

Serial Port 1 is buffered directly for RS-232 operation. Signals include the complete signal set for handshaking, modem control, interrupt generation, and data transfer. When assigned as COM1, the port is 100% compatible with the IBM-AT serial port in RS-232 mode.

Signal Path

COM1 signal path depends on the output configuration you have ordered for the board

Related Jumpers

W2 (Cpci-MXS) or W5 (cPCI-CXS) – Remote reset on COM1 or COM2 or disabled

BIOS Settings

Section 4.1.11 Integrated Peripherals : Enable/Disable Onboard FDC Controller;
Select Com Port Address of COM1

- **Remote Reset**

A remote hardware reset of the cPCI-MXS and cPCI-CXS is possible by sending a break on the COM1 or COM2 (see section 2.9.1 for Remote Reset jumper setting). A break is simple an abnormally long start bit (100ms or more) on the incoming data line. A break signal is embedded in the data, so no special wire is required.

Related Jumpers

W2 (cPCI-MXS) or W5 (cPCI-CXS) – Remote reset on COM1 or COM2 or disabled to select whether the serial port 1 or 2 is used to control the remote reset

Bios Settings

None

The remote reset will work in RS-232 and RS-422 modes. It will also work with a modem, since the modem will repeat the break signal over the telephone network. All major telecommunication software have the capability of sending a break signal, usually by pressing the CTRL-B keys or the ALT-B keys on the keyboard. Only a standard telephone line and a modem in auto-answer mode are needed. They only limitation is that the communication speed must be 1200bps or more. If the communication speed is to slow, a false reset can occur.

The break signal is entirely detected by hardware.

For truly remote operation, use the VT-100 mode, which allows remote BIOS setup and console redirection.

- **Front Plate Configuration**

  The COM1 signals are available through a DB-9 connector located on the front plate.

- **CPCI I/O Configuration**

  The complete signal set is tied to the P5 CPCI I/O connector to be used through the RTM.

2.9.2 COM2

COM2 is buffered directly for RS-232 operations and is 16C550 PC-Compatible. The interface includes the complete signal set for handshaking, modem control, interrupt generation, and data transfer.

The COM2 port is 100% compatible with the IBM-AT serial port.

Signal Path
Serial Port 2 signals are only available through the P3 CPCI I/O connector

Related Jumpers
None

BIOS Settings
Section 4.1.11 Integrated Peripherals: Onboard Serial Port 2

2.9.3 COM3

The Serial Port 3 supports Infrared, RS-232, RS-422, and RS-485 operation modes. When assigned as COM3, the port is 100% compatible with the IBM-AT serial port in RS-232 mode.

RS-422 and RS-485 modes allow communication using differential signals through one pair of wires (RS-485) or two (RS-422) to increase the noise immunity during data transfers.

RS-422 and RS-485 protocols offer advantages such as increased speed over longer distances or improved reliability over similar RS-232 setups.

Signal Path

In RS-232, RS-422, and RS-485 operation modes Serial Port 3 signals are only available through the P5 CPCI I/O connector.

In Infrared mode, signals are available through the P3 CPCI I/O connector.

Related Jumpers

W9 & W10 (cPCI-MXS), W7 & W9 (cPCI-CXS) to connect/disconnect RS-422/RS-485 termination resistors (see Section 3.1, Setting Jumpers)

BIOS Settings

11.3.7 Integrated Peripherals: Onboard Serial Port 3; Serial Port 3 Mode.

Upon a power-up or reset, the COM3 interface circuits are automatically configured for the operation mode setup in the BIOS. The Serial Port 3 signal assignation on the P5 CPCI I/O connector depends on the operation mode (RS-232, RS-422, or RS-485) it has been set:

Pin Number (J5)	RS-232	RS-422	RS-485
A11	/JDCD2	/DCD	/DCD
C11	JRXD2	RX(-)	RX/TX(-)
D11	/JDSR2	DSR	DSR
E11	JTXD2	TX(-)	-
A12	/JRTS2	RX(+)	RX/TX(+)
B12	/JCTS2	TX(+)	-
C12	/JRI2	/RI	/RI
E12	/JDTR2	/DTR	/DTR

- **Infrared Mode:**

  Infrared (IR) interface signals are provided to drive IR module for remote operations through Serial Port 3. When set in IR mode, the IR interface supports multi-protocol infrared operations. The IR interface is IrDA 1.1 compliant, and supports TEMIC/HP modules, SHARP ASK IR, and consumer IR.

- **RS-232 Protocol:**

  When configured for RS-232 operation mode, the Serial Port 3 is 100% compatible with the IBM-AT serial port signals.

- **RS-422 Protocol:**

  The RS-422 protocol (Full Duplex) uses both RX and TX lines during a communication session.

> **CAUTION**
>
> In RS-422 mode, W9 and W10 (cPCI-MXS) or W7 and W9 (cPCI-CXS) jumper caps must be installed to connect the 120 ohms termination resistors (See Section 3.1 *Jumper Settings*)

- **RS-485 Protocol:**

The RS-485 protocol (Half Duplex) also uses differential signals during a communication session. It differs from the RS-422 mode as it offers the ability to transmit and receive over the same pair of wires, and allows the sharing of the communication line by multiple stations. This configuration (also known as Party Line) allows only one system to take control of the communication line at the time.

In RS-485 mode, the RX lines are used as the transceiver lines, and the RTS signal is used to control the direction of the RS-485 buffer.

When set for RS-485 mode in the BIOS, upon power-up or reset, the transceiver is by default in receiver mode to prevent unwanted perturbation on the line. Party line operation mode requires termination resistors to be installed at both ends of the network.

CAUTION

When installing the cPCI-MXS or cPCI-CXS at one end of the network, W9 and W10 (cPCI-MXS) or W7 and W9 (cPCI-CXS) jumper caps must be installed to connect the 120 ohms termination resistors (See Section 3.1 – *Setting Jumpers*).

2.9.4 COM4

The Serial Port 4 is buffered directly for RS-232 operations and is 16C550 PC-Compatible. The interface includes the complete signal set for handshaking, modem control, interrupt generation, and data transfer.

When assigned as COM4 logical port, the port is 100% compatible with the IBM-AT serial port.

Signal Path

COM4 signals are only available through the P3 CPCI I/O connector.

Related Jumpers

None

BIOS Settings

11.3.7 Integrated Peripherals: Onboard Serial Port 4; IRQ Line for Com4.

2.10 THERMAL MANAGEMENT

Two temperature sensors are provided to supervise the thermal environment. One is used to monitor the CPU die temperature, while the second one, located on the CPU casing, allows the monitoring of the ambient temperature around the CPU.

The temperature is controlled according to two temperature levels, the Low temperature limit, which indicates normal operating conditions, and the High temperature limit, which indicates an overheating condition.

The temperature management consists in reducing the CPU clock speed throttling when the temperature goes over the high limit (overheating condition) and suspending the throttling operation as soon as the temperature returns under the low temperature limit (normal condition).

The clock speed may be throttled by a CPU overheating due to the fan failure. In such a case, the temperature control is triggered as soon as the temperature reaches the high temperature limit of the die.

The ambient temperature of the CPU raises up due to an augmentation of the temperature in the casing. In that case, the clock speed will be slowed down as soon as the ambient temperature reaches the high ambient temperature value.

Thermal management operations are controlled by the BX chipset, and settings are provided through the BIOS setup program interface, *Thermal Management Setup* option (See Section 4.1.10 *CPU Board Feature Setup, Thermal management Options).*

2.11 USB INTERFACES

Signals for two USB ports are available through the CPCI I/O connector (P5 on cPCI-MXS, J5 on cPCI-CXS)

USB is becoming the new essential peripheral interface. The USB strengths are as follows: capability to daisy chain as many as 127 devices per interface, fast bi-directional, isochronous/asynchronous interface, 12Mbps transfer rate, and standardization of peripheral interfaces into a single format.

Signal Paths

Both USB 0 and USB 1 interface signals are available through the CPCI I/O connector (P5 or J5).

Related Jumpers

None

BIOS Settings

11.3.5 PnP/PCI Configuration: Assign IRQ For USB

USB supports Plug and Play and hot swapping operations (OS level). These user-friendly features allow USB devices to be automatically attached, configured and detached, without reboot or running setup.

The cPCI-MXS and cPCI-CXS boards fully support the standard universal host controller interface (UHCI) and uses standard software drivers that are UHCI-compatible.

2.12 VIDEO INTERFACE

The high-performance video capability of the board is based on the latest Accelerated Graphics Port (AGP) technology. The video controller, Intel 69000, with its integrated 2Meg of high performance SDRAM is capable of CRT resolutions up to 1024 x 768 x 64K colors or 1280 x 1024 x 256 colors.

The video interface features 64-bit 2D graphics engine, 64-bit GUI accelerator engine with multiple window video acceleration.

Signal Path

The VGA video signal path depends on the output configuration you have ordered for the board.

Related Jumpers

W7 (cPCI-MXS), W6 (cPCI-CXS) to enable or disable onboard VGA feature.
See section 3.1 – *Jumper Settings*

BIOS Settings

11.3.5 PnP/PCI Configuration: Init Display First; Assign IRQ for VGA

- **Front Plate Configuration**
  VGA interface signals are available on J8, standard VGA connector, located on the front plate of the board, only when the board is ordered for front access operations. This configuration allows direct connection of CRT display onto the board.

- **CPCI I/O Configuration**
  VGA interface signals are available on J4 CPCI I/O connector only when the board is ordered for rear panel output operations.

2.12.1 Supported Resolutions

The maximum video resolution and performance depend directly on the drivers running with your software application. Resolution and number of colors specification are listed below:

Resolution	Number of Colors
640x480, 800x600, 1024x768, 1280x1024	256 (8 bits)
640x480, 800x600, 1024x768	65,536 (16 bits)
640x480, 800x600	16.8 million (24 bits)
640x480, 800x600	16.8 million (32 bits)

2.12.2 Major Features Description

- **VGA Compatibility**

  The video controller includes all registers and data paths required for VGA controller, and supports extensions to VGA, including resolutions up to 800x600x16.8 million colors non-interlaced. 16-bit images are displayed at up to 1024x768 resolution.

  2D Graphics Engine

  The 2D graphics engine is an advanced 64-bit three-operand engine that accelerates BitBLTs as line draws, polygon draw, and polygon fill. The 2D graphics engine also performs video and bitmap scaling, and data overlay.

PART 3

Installing the Board

1. SETTING JUMPERS
2. REGISTER'S DESCRIPTION
3. ONBOARD INTERCONNECTIVITY
4. CUSTOMIZING THE BOARD
5. PROCESSOR AND FAN
6. BACKUP BATTERY
7. INSTALLING THE MEMORY
8. SUPERVISION FEATURES
9. BUILDING A CPCI SYSTEM
10. CPCI I/O SYSTEM
11. J4 (P4 FOR MXS) SIGNAL SPECIFICATION
12. J5. (P5 FOR MXS) SIGNAL SPECIFICATION

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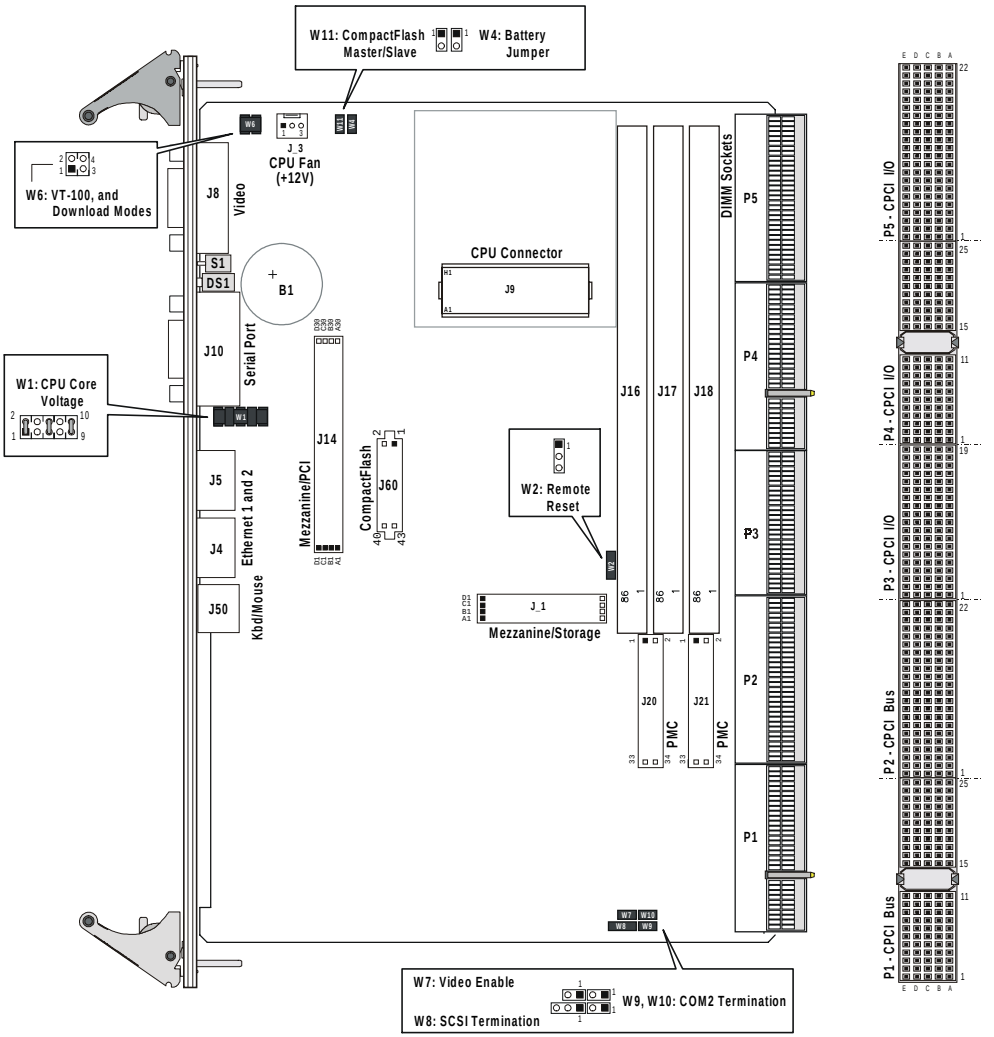
3.1 SETTING JUMPERS

3.1.1 Jumper Description for the cPCI-MXS and the cPCI-CXS

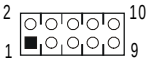
Description	Jumper cPCI-	
	MXS	**CXS**
CPU Core Voltage - Use this jumper to setup the core voltage according to your CPU specification.	**W1**	**None**
Bus Speed – Selects Bus speed at 66MHz or 100MHz.	**None**	**W2**
Remote Reset – To select COM1 or COM2 as a source for the remote hardware reset.	**W2**	**W5**
CompactFlash Setting – Use this connector to setup the CompactFlash device in Master or Slave configuration.	**W11**	**W3**
Onboard Battery – Connects or Disconnects the battery to/from the board circuitry.	**W4**	**W4**
VT-100 Mode (1-2) – When enabled, allows VT100 or ANSI terminal connection **Download Mode (2-3)** – When enabled, allows data serial download from a remote computer.	**W6**	**W1**
Onboard Video – Use this jumper to enable or disable the onboard video feature.	**W7**	**W6**
SCSI Termination – Use this jumper to disable SCSI termination or select the termination control method from Software Controlled and Hardware Controlled options.	**W8**	**W8**
COM2 Termination – Use these jumpers to connect or disconnect termination resistors on/from Serial Port 3 when set for RS-422/RS-485 operation mode 0.	**W9 W10**	**W7 W9**

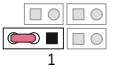
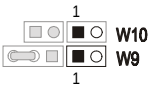
3.1.2 cPCI-MXS Connector and Jumper Location



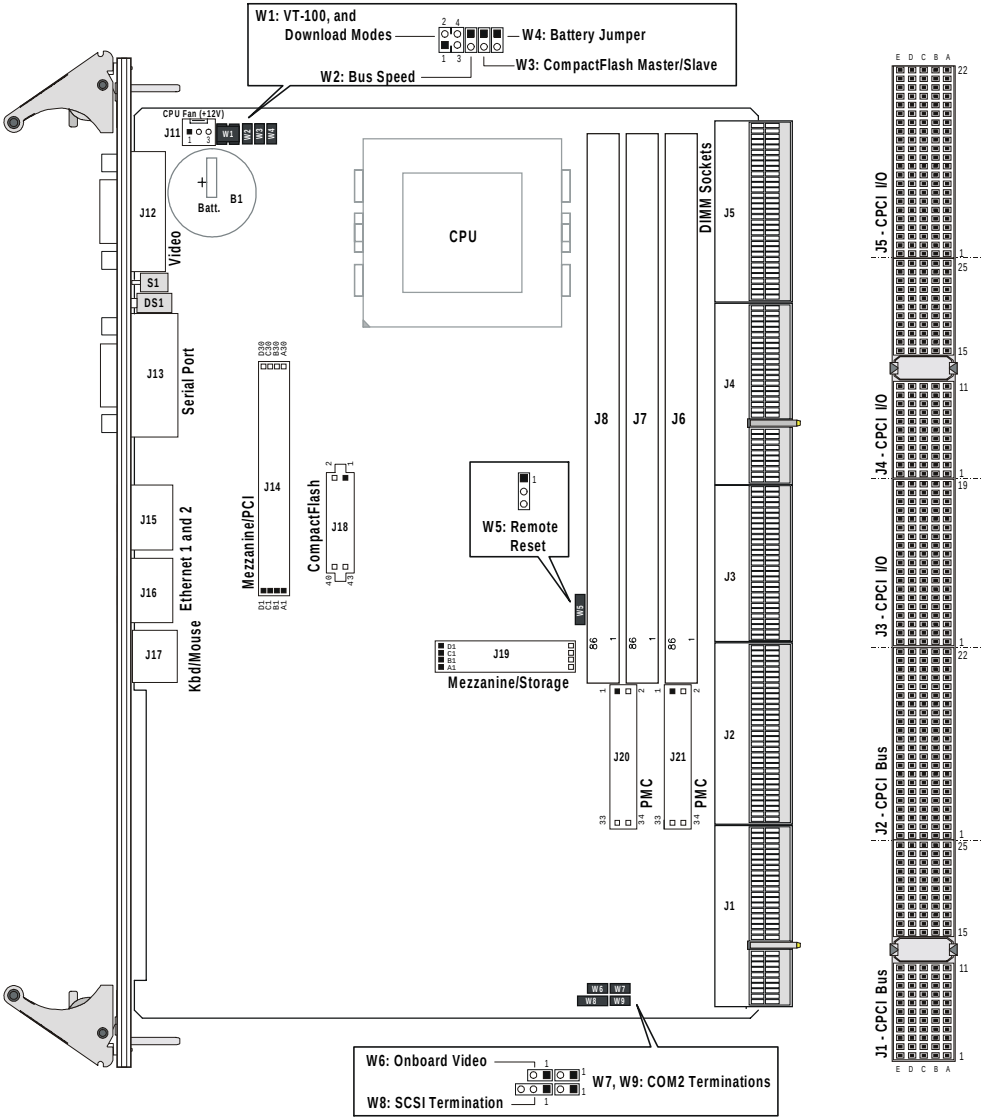
NOTE P1-P5 correspond to PICMG's definition of J1-J5

3.1.3 cPCI-MXS – Jumper Settings

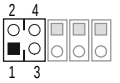
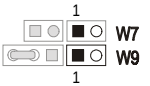
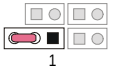
<table>
<tr><th>JUMPER</th><th>CONFIGURATION (DEFAULT SETTING = *)</th></tr>
<tr><td>W1
 
</td><td>
<table>
<tr><th>W1 - CPU Core Voltage</th><th>1-2</th><th>3-4</th><th>5-6</th><th>7-8</th><th>9-10</th></tr>
<tr><td>(333Mhz)</td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>1.6V *</td><td>on</td><td>off</td><td>on</td><td>off</td><td>on</td></tr>
</table>
Careful attention should be taken when installing a processor. Faulty jumper settings can damage both the board and the processor
</td></tr>
<tr><td>W2
 
</td><td>
<table>
<tr><th>W2 Remote Reset</th><th></th></tr>
<tr><td>Through COM1</td><td>1-2</td></tr>
<tr><td>Through COM2</td><td>2-3</td></tr>
<tr><td>Disabled *</td><td>off</td></tr>
</table>
</td></tr>
<tr><td> 

W4</td><td>
<table>
<tr><th>W4 - Onboard Battery</th><th></th></tr>
<tr><td>Connected</td><td>on</td></tr>
<tr><td>Disconnected *</td><td>off</td></tr>
</table>
Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.
</td></tr>
<tr><td>W6
  </td><td>
<table>
<tr><th>W6 - VT100/Download Mode</th><th></th></tr>
<tr><td>VT-100 mode</td><td>1-2</td></tr>
<tr><td>Download mode</td><td>2-3</td></tr>
<tr><td>Normal mode *</td><td>off</td></tr>
</table>
</td></tr>
<tr><td>W7
 
</td><td>
<table>
<tr><th>W7 - Onboard Video</th><th></th></tr>
<tr><td>Disabled</td><td>on</td></tr>
<tr><td>Enabled *</td><td>off</td></tr>
</table>
</td></tr>
<tr><td>W8
 
</td><td>
<table>
<tr><th>W8 - SCSI Termination</th><th></th></tr>
<tr><td>Software controlled</td><td>1-2</td></tr>
<tr><td>Hardware controlled *</td><td>2-3</td></tr>
<tr><td>Disabled</td><td>off</td></tr>
</table>
</td></tr>
<tr><td> 
</td><td>
<table>
<tr><th>W9, W10 - COM2 Terminations</th><th>W9</th><th>W10</th></tr>
<tr><td>RS-422/485 modes only</td><td></td><td></td></tr>
<tr><td>With termination resistors</td><td>on</td><td>on</td></tr>
<tr><td>Without termination resistors*</td><td>off</td><td>off</td></tr>
</table>
</td></tr>
<tr><td>W11
 
</td><td>
<table>
<tr><th>W11 - CompactFlash</th><th></th></tr>
<tr><td>Master</td><td>on</td></tr>
<tr><td>Slave *</td><td>off</td></tr>
</table>
</td></tr>
</table>

3.1.4 cPCI-CXS Connector and Jumper Layout



3.1.5 cPCI-CXS Jumper settings

JUMPER	CONFIGURATION (DEFAULT SETTING = *)
W1 	**W1 - VT100/Download Mode** VT-100 mode: 1-2 Download mode: 2-3 Normal mode *: off
 W2	**W2 Bus Speed** 66/100MHz: off 66MHz: on
 W3	**W3 - CompactFlash** Master: on Slave *: off
 W4	**W4 - Onboard Battery** Connected: on Disconnected *: off Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dose of used batteries according to the manufacturer's instructions.
W5 	**W5 Remote Reset** Through COM1: 1-2 Through COM2: 2-3 Disabled *: off
W6 	**W6 - Onboard Video** Disabled: on Enabled *: off
	**W7, W9 - COM2 Terminations** RS-422/485 modes only: W9 on, W10 on With termination resistors: W9 on, W10 on Without termination resistors*: W9 off, W10 off
W8 	**W8 - SCSI Termination** Software controlled: 1-2 Hardware controlled *: 2-3 Disabled: off

3.2 REGISTER'S DESCRIPTION

3.2.1 RS232/RS485

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x190*	NU	NU	NU	RS485	RS232	ST1	NU	NU
WRITE	0x190*	NU	NU	NU	RS485	RS232	ST1	NU	NU
Power-up Default					0	1	0		

ST1 : Enable RTS2 to be used as 485TX ENABLE when in 485 mode
RS232 : Enable UART2 RS232 operation
RS485 : Enable UART2 RS422 and 485 operation

The serial port 2 mode can be controlled by setting three bits. Here are the possibilities.

Mode	Bit RS232	Bit RS485	Bit ST1
RS232	1	0	X
RS422	0	1	0
RS485	0	1	1

1.2.2 History and monitor status

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x191*	PBRST	NU	WDO	NU	NU	NU	NU	PFO
WRITE	0x191*	NU	NU	NU	NU	NU	NU	NU	NU
Power-up Default									

PFO : Read the external power fail flag
PBRST : When high, indicate that the last system reset was caused by push button reset switch
WDO : When high, indicate that the last system reset was caused by watchdog time out

1.2.3 Multimedia, History status

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x192*	NU	NU	NU	NU	NU	WD_LOCK	NU	CLRHIS
WRITE	0x192*	NU	NU	NU	NU	NU	WD_LOCK	NU	CLRHIS
Power-up Default							1		1

CLRHIS : When low, clear all history bits
WD_LOCK : When high, lock the state of the enable bit for the digital watchdog

1.2.4 Monitoring status and I/O access

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x193*	NU	NU	NU	NU	IDCHIP	NU	I2C_CLK	I2C_DATA
WRITE	0x193*	NU	NU	NU	NU	IDCHIP	NU	I2C_CLK	I2C_DATA
Power-up Default						0		0	0

I2C_DATA : I2C data
I2C_CLK : I2C Clock
IDCHIP : One-wire clock/data for silicon ID chip

1.2.5 Uart 3 PnP configuration

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x194*	CND3	CIS3_1	CIS3_0	CBAS3_1	CBAS3_0	Reserved	Reserved	Reserved
WRITE	0x194*	CND3	CIS3_1	CIS3_0	CBAS3_1	CBAS3_0	Reserved	Reserved	Reserved
Power-up Default		0	0	0	0	1	0	0	1

CND3 : When low, decode the base address.
CIS3_[1..0] : COM port interrupt select.
CBAS3_[1..0] : COM base address select.

The serial port 3 & 4 interrupt can be controlled in the following way.

CIS	Bit 1	Bit 0
IRQ 3	0	0
IRQ 4	0	1
IRQ 5	1	0
IRQ 7	1	1

The serial port 3 & 4 base address can be controlled in the following way.

CBAS	Bit 1	Bit 0
3F8	0	0
2F8	0	1
3E8	1	0
2E8	1	1

1.2.6 Uart 4 PnP configuration

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x195*	CND4	CIS4_1	CIS4_0	CBAS4_1	CBAS4_0	NU	NU	Reserved
WRITE	0x195*	CND4	CIS4_1	CIS4_0	CBAS4_1	CBAS4_0	NU	NU	NU
Power-up Default		0	0	0	1	1			

CND4 : When low, decode the base address
CIS4_ : [1..0] COM port interrupt select.
CBAS4_ : [1..0] COM base address select.

1.2.7 Digital watchdog

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x196*	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
WRITE	0x196*	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
Power-up Default		0	0	0	1				

WDEN : Enable/disable digital watchdog.
WDD[2..0] : Duration of digital watch dog.

The digital watchdog duration can be controlled in the following way.

WDD[2..0]	NMI(T)	RESET(T)
000	16T	NMI(T)+8T
001	64T	NMI(T)+8T
010	256T	NMI(T)+8T
011	1024T	NMI(T)+8T
100	4096T	NMI(T)+8T
101	16384T	NMI(T)+8T
110	65536T	NMI(T)+8T
111	262144T	NMI(T)+8T

Time-out selection with T = 1.08ms (TBC)

1.2.8 NMI control

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x197*	BATFEN	BATFLT	NU	NU	NU	NU	WDNMIEN	WDNMI
WRITE	0x197*	BATFEN	NU	NU	NU	NU	NU	WDNMIEN	NU
Power-up Default		0						0	

WDNMI : When high, signal NMI from watchdog time-out.
WDNMIEN : Enable NMI generation from digital watchdog
BATFLT : When high, signal NMI from local RTC battery monitor
BATFEN : Enable NMI generation for bat fault.

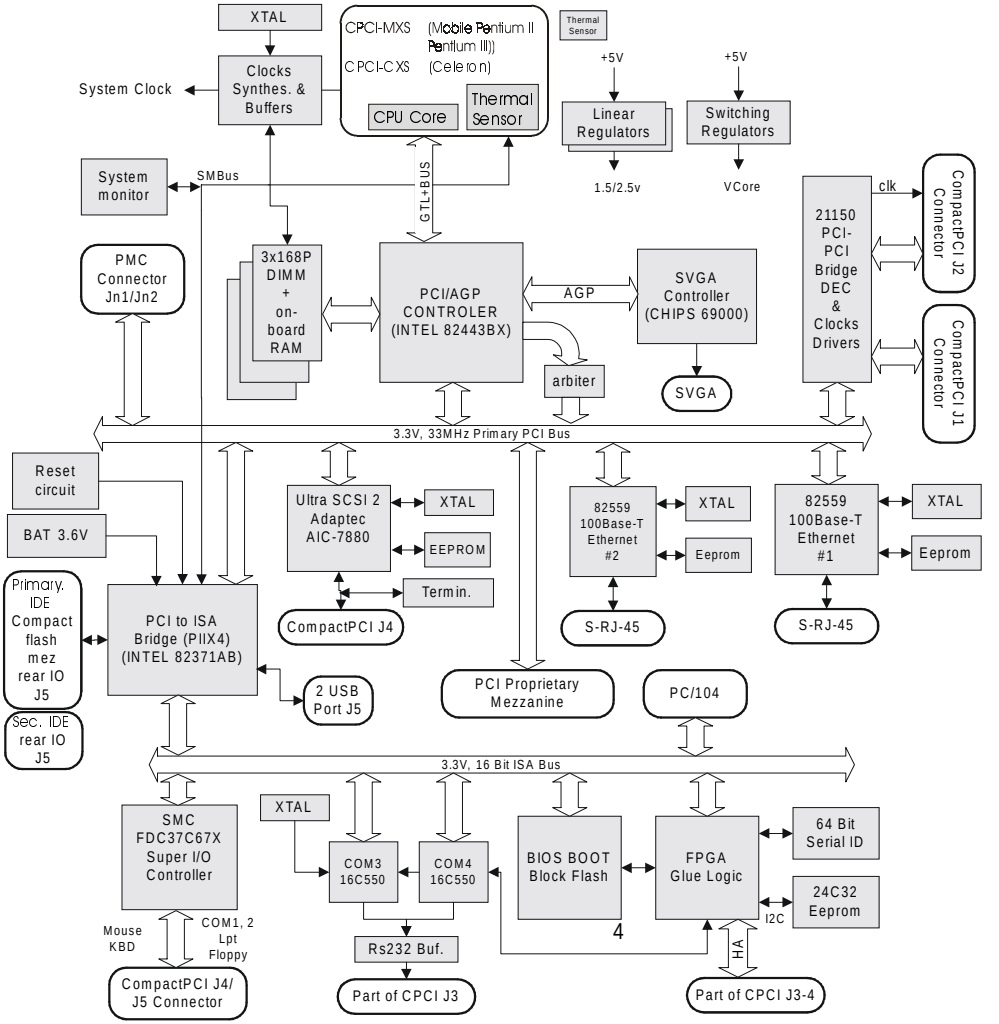
1.2.9 Register BITs description (summary)

CPLD	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x190*	NU	NU	NU	RS485	RS232	ST1	NU	NU
WRITE	0x190*	NU	NU	NU	RS485	RS232	ST1	NU	NU
READ	0x191*	PBRST	NU	WDO	NU	NU	NU	NU	PFO
WRITE	0x191*	NU	NU	NU	NU	NU	NU	NU	NU
READ	0x192*	NU	NU	NU	NU	NU	WD_LOCK	NU	_CLRHIS
WRITE	0x192*	NU	NU	NU	NU	NU	WD_LOCK	NU	_CLRHIS
READ	0x193*	NU	NU	NU	NU	IDCHIP	NU	I2C_CLK	I2C_DATA
WRITE	0x193*	NU	NU	NU	NU	IDCHIP	NU	I2C_CLK	I2C_DATA
READ	0x194*	_CND3	CIS3_1	CIS3_0	CBAS3_1	CBAS3_0	Reserved	Reserved	Reserved
WRITE	0x194*	_CND3	CIS3_1	CIS3_0	CBAS3_1	CBAS3_0	Reserved	Reserved	Reserved
READ	0x195*	_CND4	CIS4_1	CIS4_0	CBAS4_1	CBAS4_0	NU	NU	Reserved
WRITE	0x195*	_CND4	CIS4_1	CIS4_0	CBAS4_1	CBAS4_0	NU	NU	NU
READ	0x196*	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
WRITE	0x196*	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
READ	0x197*	BATFEN	BATFLT	NU	NU	NU	NU	WDNMIEN	WDNMI
WRITE	0x197*	BATFEN	NU	NU	NU	NU	NU	WDNMIEN	NU
READ	0x198*	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
WRITE	0x198*	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
READ	0x199*	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
WRITE	0x199*	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
READ	0x19A*	NU	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
WRITE	0x19A*	NU	NU	NU	NU	NU	NU	NU	NU
READ	0x19B*	NU	NU	NU	Reserved	Reserved	Reserved	Reserved	Reserved
WRITE	0x19B*	NU	NU	NU	NU	NU	NU	NU	NU

The base address for the Supervisor I/O Register, which is used for such functions as power fail detection and the watchdog timer can be set to 190h, 290h, and 390h (see *Chipset Features Setup*).

3.3 ONBOARD INTERCONNECTIVITY

1.3.1 cPCI-MXS and cPCI-CXS Block Diagram



The cPCI-MXS or cPCI-CXS is not only a matter of computation power. The boards also provide a high capability to interface with peripherals through three integrated chipsets:

- Host-to-PCI bridge for CompactPCI bus drives 7 CPCI slots. 443BX from Intel: interface with the processor (host), system memory, video controller, and Primary PCI bus (3.3V / 33MHz).
- PCI-to-PCI bridge - 21150 from DEC: manage the PCI bus signals on J1 and J2 CPCI connectors. When used with a CompactPCI backplane, the board can drive directly up to seven CPCI slots in PCI bus Master configuration.
- PCI-to-ISA bridge - 82371AB PIIX4 from Intel: interface the ISA bus to the Primary PCI bus.

1.3.2 Mobile Pentium® II / III processor

The cPCI-MXS system board supports the Intel's Low Power 266MHz and 333MHz Mobile Pentium®II processor and Low Power 400MHz and 500MHz Pentium III processor (Higher clock speeds will be available when Intel will release the corresponding parts).

It consists of a Pentium® II / III processor core with an integrated second level cache of 256KB (on-die, full CPU speed, ECC capable) and a 64-bit high performance front side bus (66MHz: 266/333MHz CPUs and 100MHz: 400/500 MHz CPUs) bus speeds are supported).

The processor interfaces to the 440BX AGPset through the 64-bit low power GTL + data bus interface.

1.3.3 CELERON®

The cPCI-CXS system board supports the Intel Celeron™ processor 300A, 366 and 433MHz in PPGA370 Package. It consists of a Celeron core, with a second level cache of 128KB (on-die, full CPU speed, ECC capable). The front side bus speed is set by software to 66MHz or 100MHz depending on the CPU installed. However, it can be forced to 66MHz by setting a hardware jumper.

The processor interfaces to the 440BX AGPset through the 64-bit low power GTL + data bus interface.

1.3.4 North Bridge Chipset

This chipset consist of 443BX AGPset, 64/72-bit SDRAM data interface with ECC support, Low Power GTL Bus, five PCI arbitration channels, PCI bus rev. 2.1, Accelerated Graphics Port Interface (AGP). The bus is optimized for 66MHz or 100MHz operation.

1.3.5 21150 PCI-to-PCI Bridge

The 21150 is a 32/32-bit 33MHz PCI-to-PCI bridge that allows the board to support up to ten loads on its secondary PCI bus through a passive backplane. The bridge is fully compliant with the PCI Local Bus Specification, Rev. 2.1. It provides full support for delayed transactions, which enables the buffering of memory read, I/O and configuration transactions. The 21150 have separate posted write, read data and delayed transaction queues with a high buffering capability.

In addition, it supports buffering of simultaneous multiple posted writes and delayed transactions in both directions.

The PCI-to-PCI bridge allows the Primary and Secondary PCI buses to operate concurrently. This means that a master and a target on the same PCI bus can communicate while the other PCI bus is busy. This traffic isolation may increase system performance in applications where system resources are highly used.

1.3.6 82371AB PCI-to-ISA Bridge / IDE Xcelerator (PIIX4)

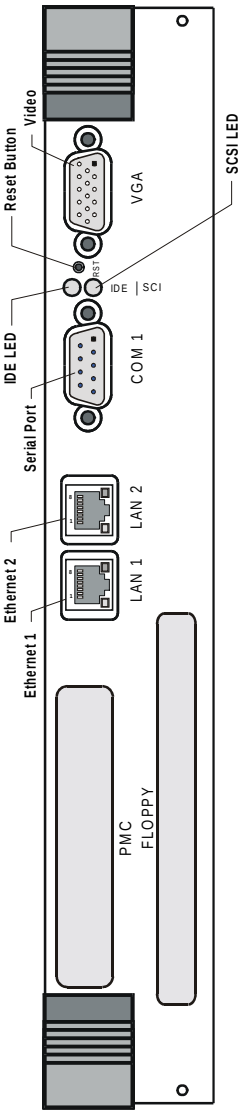
The PCI-to-ISA bridge is configured to support signals to directly drive IDE interfaces, USB ports, extra communication ports (Serial Ports 3 and 4), and standard Serial Ports (1 and 2), floppy disk drives, mouse and keyboard through a super I/O controller (FDC37C672).

1.3.7 Onboard Connectors and Headers

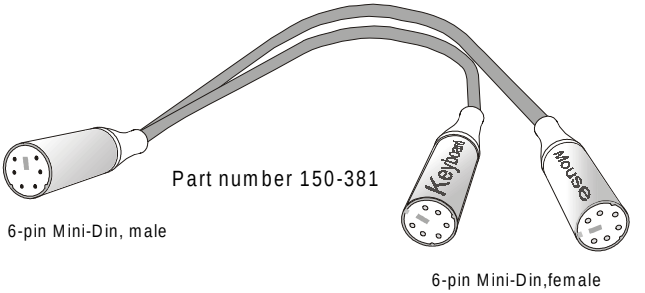
Description	CPCI		Comments
	MXS	CXS	
Fan Header	J3	J11	The +12V DC CPU fan power supply is provided through this header as well as a speed sense input for the fan.
Processor Socket	J9	J9	MXS : Mobile Pentium II / III connector CXS : Celeron connector.
CompactFlash	J60	J18	This connector is dedicated to the Teknor's CompactFlash module to support CompactFlash disk.
Battery	B1	B1	CMOS backup battery connector.
PCI Mezzanine	J14	J14	This connector handles PCI bus signals to the mezzanine.
Storage Mezzanine	J1	J19	This connector is implemented to support floppy drive and hard disk signals.
PMC	J21	J20	The PCI Mezzanine Card (PMC) connectors support one standard PMC device.
DIMM Sockets	J16/17/18	J6/J7/J8	Supports 168-pin 64/72-bit DIMMs, up to 768MB of RAM.
CompactPCI Bus	P1/P2*	J1/J2	J1- CPCI bus signals and power. J2 – Additional system slot signals.
CompactPCI I/O	P3*	J3	Serial Ports 2/3/4, Ethernet 1, power.
CompactPCI I/O	P4/P*5	J4/J5	Supports PS/2 mouse, serial ports 1 and 2, first IDE channel, parallel port, keyboard, speaker, floppy disk, reset, USB, SMBus, and power signals.
Ethernet ½	J4/J5	J15/J16	RJ-45 connectors with built-in activity and link indicators.
VGA	J8	J12	Supports standard 15-pin DSUB female connector.
COM1	J10	J13	Supports standard 9-pin DSUB male connector.
Keyboard/Mouse	J50	J17	Mouse and keyboard signals are combined on a standard 9-pin DSUB female connector.

NOTE P1-P5 correspond to PICMG's definition of J1-J5

1.3.8 Front Plate Connectors and Indicators

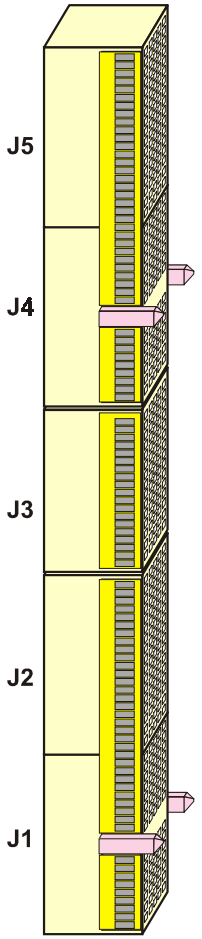


Name		Description	Comments
MXS	CXS		
J8	J12	Video Connector	Standard 15-pin DSUB female connector
S1	S1	Reset Button	Use a small tool to press the button and proceed to a hardware reset of the board
DS1	DS1	IDE/SCSI LEDs	When lit, indicate there is an activity on IDE/SCSI devices
J10	J13	Com Port 1	Standard 9-pin DSUB male connector
J4/J5	J15/J16	Ethernet 1 and 2	RJ-45 connectors with built-in activity and link indicators
J50	J17	Keyboard and Mouse	To connect a keyboard and/or a mouse through this connector, you need a Y shaped splitter cable (Teknor part number 150-381)



The front plate supports a PMC cutout and a cap that also act as an EMI shield when there are no PMC device installed.

1.3.9 CompactPCI Connectors



- **CPCI J5 Connector (P5 on the cPCI-MXS)**

  Supports PS/2 mouse, serial ports 1 and 3, primary IDE channel, parallel port, keyboard, speaker, floppy disk, reset, USB, SMBus and power signals.

- **CPCI J4 Connector (P4 on the cPCI-MXS)**

  Supports Ethernet1, secondary IDE channel, SCSI, VGA, and power signals.

- **CPCI J3 Connector (P3 on the cPCI-MXS)**

  Supports serial ports 2, 3 (Infrared), and 4, V-Port, Ethernet1, and power signals.

- **CPCI J2 Connector (P2 on the cPCI-MXS)**

  Supports additional system slot signals, and power.

- **CPCI J1 Connector (P1 on the cPCI-MXS)**

  Supports CPCI bus signals, and power.

NOTE P1-P5 correspond to PICMG's definition of J1-J5

3.4 CUSTOMIZING THE BOARD

1.4.1 Processor and Fan

cPCI-MXS

Your board will be installed with the Mobile Pentium® II processor 333MHz or Pentium III processor, Low Power 500MHz and its adequate cooling system.

cPCI-CXS

Your board will be installed with the CELERON processor and its adequate cooling system. Available speeds are 300, 366 and 433MHz.

Since CPUs are very sensitive components, particular attention should be given while installing a processor on the board. Improper installation may damage the board and/or the CPU.

CAUTION

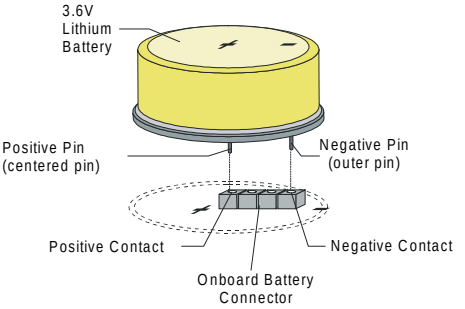
Since CPUs are very sensitive components, particular attention should be given while installing a processor on the board. Improper installation may damage the board and/or the CPU

Before installing a processor on your board, **you must contact our technical support** for the installation procedure

1.4.2 Backup Battery

An onboard 3.6V lithium battery is provided to backup BIOS setup values and the real time clock (RTC).

When replacing, the battery must be connected as follows:



WARNING

Danger of explosion if battery is incorrectly replaced

Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

1.4.3 Installing the Memory

3.4.3.1 SDRAM System Memory

The cPCI-MXS and cPCI-CXS support three 168-pin DIMM (Dual In-Line Memory Module) sockets for memory configuration from 8MB to 768MB of Synchronous DRAM.

The memory characteristics must conform to the following:

- 1.15 inch height, 168-pin DIMM
- Standard 3.3V only,
- 64-bit and 72-bit modules, single-sided or double-sided
- Unbuffered 100MHz (SDRAM),
- Serial Presence Detect (SPD) EEPROM,
- Errors Checking and Correction (ECC) capabilities or parity bit with 72-bit modules,
- Compliant with Intel's PC SDRAM Unbuffered DIMM Specification (100MHz) Rev. 1.0.

At least 8MB of memory must be installed on the board for proper operation. Modules can be installed in any socket and order. The total system memory is equal to the sum of the memory module size installed in the three DIMM sockets.

NOTE

When populating with more than one memory module, each socket must be installed with the same memory type (64/72-bit), however the capacity of each module may be different from the other.

The recommended DIMM devices are listed in the table below.

Vendor's part number	DIMM's description	Vendor's Name
CTK32M/P100S	ECC SDRAM 32MB 4M*72 PC100 1.15"HT	CENTON
4X72CQ2X8S4E	ECC SDRAM 32MB 4M*72 PC100 1.15"HT	ROCKY MOUNTAIN RAM
DIM-200472V2S08G1	ECC SDRAM 32MB 4M*72 PC100 1.15"HT	SHIKATRONICS
DIM200472V5S08G	ECC SDRAM 32MB 4M*72 PC100 1.15"HT	SHIKATRONICS
CTK64M/P100S	ECC SDRAM 64MB 8M*72 PC100 1.15"HT	CENTON
8X72PC8X8S4E	ECC SDRAM 64MB 8M*72 PC100 1.15"HT	ROCKY MOUNTAIN RAM
DIM200872V4S8G1	ECC SDRAM 64MB 8M*72 PC100 1.15"HT	SHIKATRONICS
CTK128M/P100S	ECC SDRAM 128MB 16M*72 PC100 1.15"	CENTON
DIM-201672V4S08G1	ECC SDRAM 128MB 16M*72 PC100 1.15"	SHIKATRONICS
VM374S1723-GL	ECC SDRAM 128MB 16M*72 PC100 1.15"	VIRTIUM
CFHKQARV4VU420G	ECC SDRAM 256MB 32M*72 PC100 1.15"	CENTON
CTK256M/P100S	ECC SDRAM 256MB 32M*72 PC100 1.15"	CENTON
DIM203272VDS08GS	ECC SDRAM 256MB 32M*72 PC100 1.15"	SHIKATRONICS
VM374S3323-GL	ECC SDRAM 256MB 32M*72 PC100 1.15"	VIRTIUM

3.4.3.2 DIMM Installation

To install the DIMMs in the sockets, proceed as follows:

1. With the board flat on the table, turn it so that the front plate is facing you.
2. Hold the module vertically so that the bottom connector key is on the right. Insert the fingers into the socket. The socket's keys will ensure a correct mating.
3. Press firmly on the top edge of the memory module to engage it into the socket. The module is fully inserted when the retaining clips snap into notches located at each end of the module.

If necessary, work your way by inserting the other modules, one by one.

To remove the DIMMs from the sockets, pull simultaneously on the retaining clips located on each side of the socket. Once the module has snapped out, pull gently on it.

1.4.4 Supervision Features

The cPCI-MXS and cPCI-CXS provide a set of programmable I/O registers to setup the Intel PIIX4 (I/O addresses 4030h to 4037h) and the XILINX FPGA (I/O addresses programmable at 190h-193h, 290h-293h or 390h-393h using the AWARD Chipset Features Setup).

Only register bits needed to program the power fail detection and watchdog functions are described below.

3.4.4.1 Power Fail Monitoring

The power failure detector status can be readout from one bit of the system register located at the address 4031h (See table below). The detection conforms to the following conditions (* = active low signal):

It always monitors the +5V power supply. When it drops below 4.65V (typical), the system is reset.

It can monitor the onboard battery. When the battery is in a low condition (below 2.9V typical), the PFO* (power fail output) signal goes low. The status of the PFO* signal can be read at I/O address 4031h, bit 1 (0 = failed, 1 = good). An interrupt handler can then service the interrupt. If you choose not to generate an NMI, you can use an algorithm to detect a low battery condition and respond accordingly.

Register	Bit #	Function	Software Programming
4030h	0-7	Reserved	Reserved
4031h	0, 2-7	Reserved	Reserved
	1	Power Fail Output (Internal/External Battery or External Power Source)	Read: 0 = Failed, 1 = Good
4032h	0, 2-7	Reserved	Reserved
	1	Watchdog Stage 1 Status	Read: 0 = Timed out, 1 = Normal
4034h	0-7	Reserved	Reserved
4035h	0-1, 4-7	Reserved	Reserved
	2	Watchdog enable	Write: 1 = Disable, 0 = Enable
	3	Watchdog reset	Write: 1-0-1 (toggle) to activate the watchdog (when enabled)
4036h	0-7	Reserved	Reserved
4037h	0-7	Reserved	Reserved

For more information, contact the Technical Support department

3.4.4.2 Watchdog

The function of a watchdog is to reset the CPU board if the processor is not able to generate a trigger for longer than the watchdog time-out period. This feature is useful in embedded systems where human supervision is not required or impossible

The cPCI-MXS or cPCI-CXS provides a two-stage digital watchdog with software programmable time-out period.

Following a reset of any source, the watchdog is disabled. The watchdog can be enabled by software.

Dual Stage Watchdog

Enabling the Programmable Watchdog

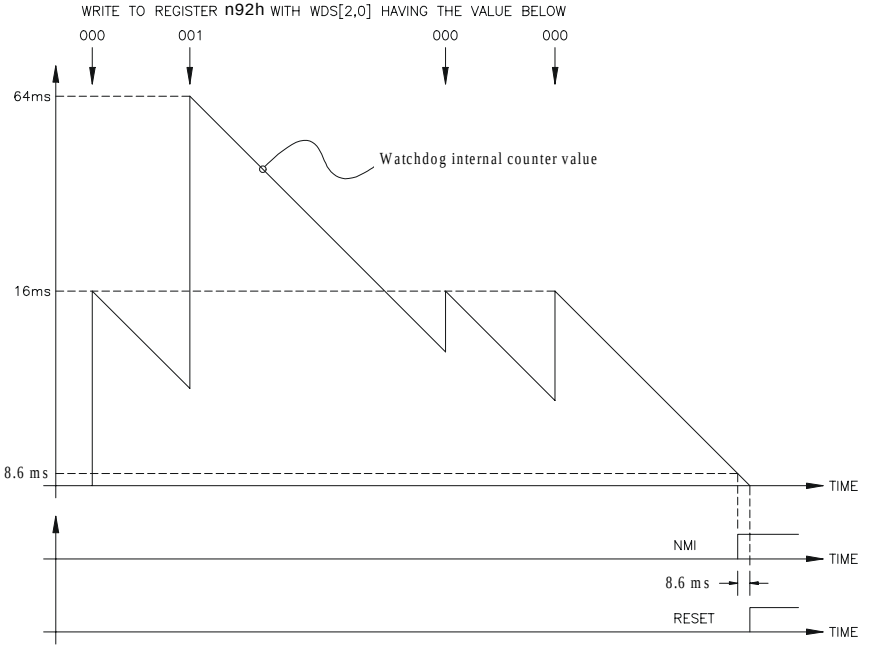
To enable the programmable watchdog, first unlock the enable bit by clearing the lock bit in register 0x92h (bit 2), then set th4e bit WDEN (bit 7) in register n92h and relock it by setting the lock bit in register 0x92 (bit 2). The following is an example in C language :

```
#define TekReg 0x190                    // define base address (0x190, 0x290 or 0x390
void ArmWatchdog(void)
{
    outp{TekReg+2,  inp(TekReg+2) & 0xFB);      // unlock watchdog enable bit
    outp{TekReg+6,  inp(TekReg+6) | 0xF0);      // enable and trigger at max time-out
    outp{TekReg+2,  inp(TekReg+2) | 0x04);      // lock watchdog enable bit
}
```

Triggering the Programmable Watchdog

To trigger the programmable watchdog, the processor writes to register n92h (n=1, 2 or 3). The action of writing to the register is the trigger and the value written to the register tells the watchdog the current time-out to use (see register n92h description). For a fixed time-out, the software simply writes a constant in register x92h.

A variable refresh is possible as shown below:



The programmable watchdog can be viewed as a decrementing counter that is initialized by a write to register n92h. The processor must initialize the counter to prevent it from reaching count 0 (timeout).

The following C language procedure can be used to trigger the programmable watchdog.

```
#define TekReg 0x190                    // define base address (0x190, 0x290 or 0x390)
void TrigWatchdog(timeout)     // select timeout at runtime: 0x80 = 0.016s,
                               // 0x90 = 0.065s, 0xA0 = 0.261s, ...
{
   outp(TekReg+6,(inp(TekReg+6) & 0x0F) | (timeout & 0xF0));
}
```

Time-out

The programmable watchdog has two stages: the first stage has a variable time-out while the second stage has a fixed one.

The first stage time-out is chosen at runtime from eight preset values (see table below). The first stage time-out generates an NMI interrupt (if enabled in register n92h). An appropriate NMI handler must be written, otherwise this will be treated as a parity error by the default BIOS NMI handler; see register n92h description for a suggestion on how to do this.

The second stage times-out 8.6ms ±10% (depending on the temperature) after the first one and generates a master reset.

WDS[2,0]	NMI Timeout	RESET Timeout
000	0.016s	0.016s + 1ms
001	0.065s	0.065s + 1ms
010	0.261s	0.261s + 1ms
011	1.044s	1.044s + 1ms
100	4.174s	4.174s + 1ms
101	16.69s	16.69s + 1ms
110	66.79s	66.79s + 1ms
111	267.1s	267.1s + 1ms

A reset from the programmable watchdog is latched for reset source identification; see reset history description in Section 4.3.

3.4.4.3 Thermal Management

The thermal management is built around two digital temperature sensors and a thermal watchdog. Both devices can be programmed to set their outputs when the temperature of the processor or the ambient temperature exceeds a programmable high limit, and reset its output when the temperature is under a programmable low limit. A special routine is implemented to throttle the CPU clock until the temperature falls below the programmed low limit.

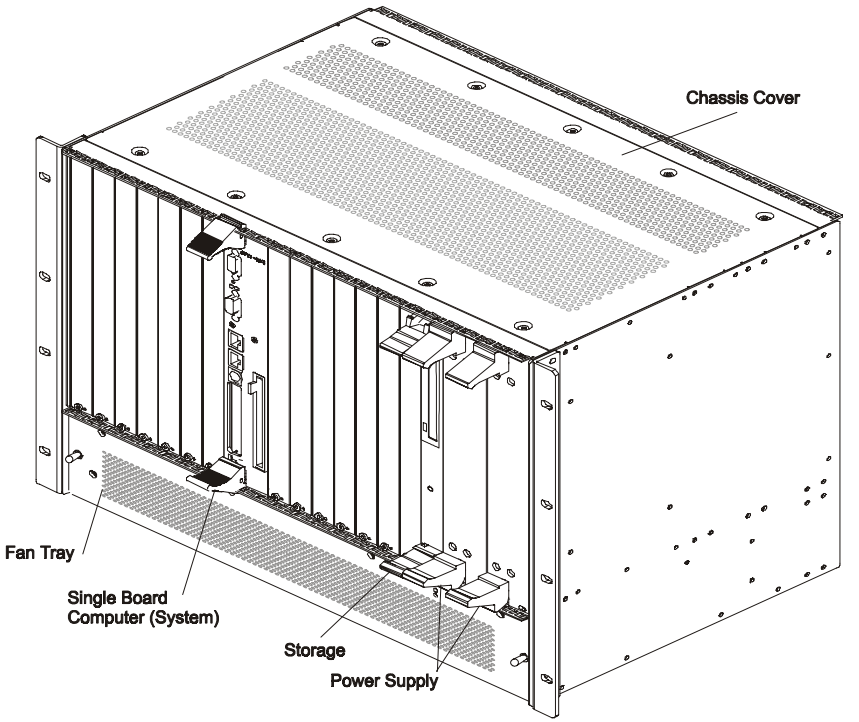
Please refer to Section 4.1.10 *CPU/Board Features Setup– Thermal Management Options* for a complete information on thermal management setups.

3.5 BUILDING A CPCI SYSTEM

When building a CompactPCI system, a minimum requirement consists in: a chassis, a CompactPCI backplane, a storage module, a power supply unit, and a ventilation system.

The main AC power is drawn to the chassis components through an IEC power plug with a 2-stage filter, fuse holder and power switch. All power features are provided at the rear of the chassis.

The chassis may be used either as a desktop system or a rack-mount bay.



CxP0816

3.5.1 Backplane

An entry-level backplane is provided by Teknor. It is referred to as cBP-08R. It features 8 CPCI slots (one PCI I/O segment), and includes P3-P5 I/O connectors on all slots.

A 16-CPCI-slot backplane (cBP-16R) is also available from Teknor. It supports two PCI I/O segment: one is driven directly by the system processor while the other is managed through a PCI-to-PCI bridge implemented on the cMCB-2RC mezzanine card (Storage/PCI-to-PCI mezzanine).

All Teknor's CompactPCI backplanes feature pass-through connectors (P3-P5) to support Rear Panel I/O connections.

IMPORTANT

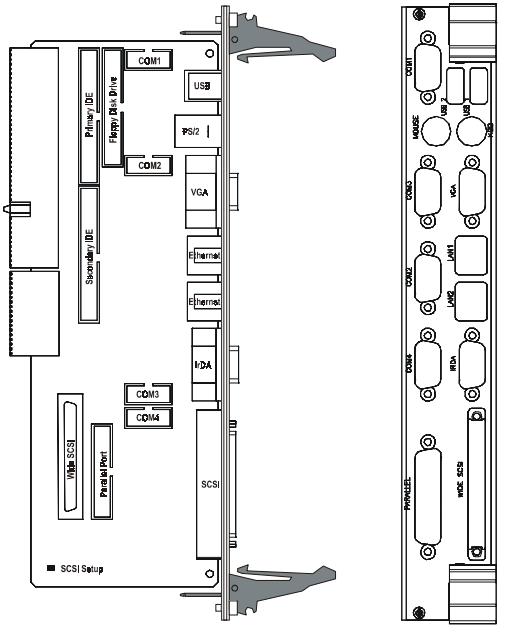
J1 and J2 are de-facto industry standard as defined by PICMG.

J3, J4 and J5 are user-defined connectors and will vary from various manufacturers. Contact our Technical Support to verify pinout compatibility with other chassis backplane vendors.

3.5.2 Rear-Panel I/O

This feature is intended to issue the I/O capabilities of the system processor to the rear of the enclosure using a Rear I/O Transition module (cTM80-STD2S).

The Rear I/O Transition module gathers all the I/O signals of the CPU board and makes them easily accessible through standard headers and connectors located at the rear of enclosure. The Rear I/O Transition module (cTM80-STD2S) is illustrated below:



3.5.3 Storage Devices

A mezzanine card (cMC or cMCB-2RC) attaches directly to the system processor. 6U form factor storage modules are supported when using the cBP-08R backplane.

There are two ways of supplying data storage with Teknor's product line.

1. cMC : Mezzanine Card that is installed directly onto the processor board.
2. cSM-DVD : 6U form factor storage module that is front loaded into the CxP0816 chassis.

3.5.4 Power Supply

6U power supply modules featuring load sharing redundant mode and hot-swap capabilities allow on-site replacements of defective module while the system remains powered.

A standard ATX power supply unit is also supported.

3.5.5 Fan Tray

The ventilation unit of the enclosure conforms to the global requirement of the system in fully loaded configuration.

3.5.6 Installing the Board into a Bay

The cPCI-MXS and cPCI-CXS are mechanical Eurocard form factor boards. It takes advantages of the IEEE1101.10 specifications that ensure a mechanical interchange capability between different plug-in elements in sub-racks.

Due to the high-density pinout of the Hard Metric connector, some precautions must be taken when connecting or disconnecting a board to/from a backplane:

1. Rail guides must be installed on the enclosure to slide the board to the backplane.
2. Do not use force if there is any mechanical resistance while inserting the board.
3. Screw the front plate to the enclosure to firmly attach the board to its enclosure.
4. Use the extractor handles to disconnect and extract the board from its enclosure.

3.5.7 Connector Keying

CompactPCI connector support guide lugs to ensure a correct polarized mating. A proper mating is enhanced by the use of color coded keys for 3.3V and 5V operation.

Color coded keys prevent inadvertent installation of a 5V peripheral board in a 3.3V slot. The cPCI-MXS and cPCI-CXS are universal. It do not support coding key. The PCI bus does not require to be keyed. Backplane connectors must always be keyed according to the signaling (VIO) level.

Coding Key Colors are defined as follows:

Signaling Voltage	Key Color
3.3V	Cadmium Yellow
5V	Brilliant Blue
Universal board (5V and 3.3V)	none
-48V	Red

3.5.8 Bus Mastering

The cPCI-MXS and cPCI-CXS provide seven pairs of REQ/GNT (0-6) arbitration signals through the Secondary PCI bus. This means the board is capable of driving up to seven CPCI slots with PCI Bus Master capabilities.

3.5.9 Connection

To install the cPCI-MXS and cPCI-CXS boards into a bay, proceed as follows:

1. Power off your CompactPCI system
2. Locate the 6U system slot
3. Remove the front plate of the slot where you intend to insert the cPCI-MXS or cPCI-CXS.
4. Ensure the module is properly aligned with the guide-rails and slide it gently until it touches the backplane connector

> **WARNING**
>
> 1. Some mechanical parts of the guide-rail are fragile (shield contacts and clips). Do not use force to insert and connect a CompactPCI module.
> 2. If there is any mechanical resistance while you insert a module, first ensure there is no mechanical obstacle and check for the alignment of all parts.

5. To engage the board's connectors into the backplane connector, press simultaneously on the front plate.
6. Fasten the module using the fellow-plate fixing screw to secure the module to the system chassis.

To remove the module from the chassis, proceed as follows:

1. Power-off the system.
2. Remove the front plate fixing screws.
3. Press the handle to act as a lever to disengage the CompactPCI connector from the backplane.
4. Pull on the handle and gently remove the board.

3.6 CPCI I/O SIGNALS

This section describes integrated feature signals available on rear panel CPCI I/O connectors (P3, P4 and p5 for the cPCI-MXS, and J3, J4, and J5 for the cPCI-CXS).

3.6.1 J3 (P3 for MXS) Signal Specification

3.6.2 Ethernet LEDS

Signal	Pin Assignation	Description
SPEEDLED 0-1	A6, E6	Speed LED signal
LINKLED 0-1	B6, D6	Link integrity LED signal
ACTLED 0-1	C6, A7	Transmit / receive activity LED signal

3.6.3 Ethernet 1

Signal	Pin Assignation	Description
ETX+1	A9	Ethernet 1 High Transmit Data line
ETX-1	B9	Ethernet 1 Low Transmit Data line
ERX+1	C9	Ethernet 1 High Receive Data line
ERX-1	D9	Ethernet 1 Low Receive Data line

3.6.4 COM3

Signal	Pin Assignation	Description
/DCD3	A13	Data Carrier Detect
RXD3	C13	Receive Data
/DSR3	D13	Data Set Ready
TXD3	E13	Transmit Data
/RTS3	A14	Ready To Send
/CTS3	B14	Clear To Send
/RI3	C14	Ring Indicator
/DTR3	E14	Data Terminal Ready

3.6.5 COM4

Signal	Pin Assignation	Description
/DCD4	A11	Data Carrier Detect
RXD4	C11	Receive Data
/DSR4	D11	Data Set Ready
TXD4	E11	Transmit Data
/RTS4	A12	Ready To Send
/CTS4	B12	Clear To Send
/RI4	C12	Ring Indicator
/DTR4	E12	Data Terminal Ready

3.6.6 IDE LED Signals.

Signal	Pin Assignation	Description
/S-IDE-ACT	B18	Secondary IDE activity
/P-IDE-ACT	C18	Primary IDE activity

3.6.7 IR COM2

Signal	Pin Assignation	Description
COM2-IRRX	D18	IR receive data line (Serial Port 2)
COM2-IRTX	E18	IR transmit data line (Serial Port 2)

3.6.8 Hot Swap HA (High Availability) signals

Signal	Pin Assignation	Description
BDSEL S2-S5	A15, B15, E15, D19	Board Select, one of the shortest pins (the last to mate and the first to break contact).
HEALTHY S2-S4	A16, B16, D17	Used to acknowledge the health of the board
PCIRST S2-S4	A17, C15, E17	Used to indicate the CompactPCI Bus reset signal

3.6.9 Miscellaneous Signals

Signal	Pin Assignation	Description
/PWRBT	A19	ACPI Reserved
EXT-SMI	B19	System Management Interrupt Input
PX4-NMI	C19	Non Maskable Interrupt Input
PWROK-33	E19	High when 3.3V supply is valid on the board

3.7 J4 (P4 FOR MXS) SIGNAL SPECIFICATION

3.7.1 Power Management

Signal	Pin Assignation	Description
I2C-CLK	A1	I2C clock signal
I2C-DATA	B1	I2C data signal
LID	C1	Reserved
/EXT-FAN0-FAIL	D1	Enclosure fan 0 fail
/EXT-FAN1-FAIL	E1	Enclosure fan 1 fail
/SM-BYPASS	A2	Reserved

3.7.2 SCSI Interface

Signal	Pin Assignation	Description
SCD 0-15	E7, D7, C7, B7, A7, E6, D6, C6, E2, D2, C2, B2, E8, D8, C8, B8	SCSI Data – The SCSI data lines drive the ID during arbitration and selection, and command and data information as well as status and messages.
/IO	A3	In/Out – Indicates the In direction when asserted and the Out direction when not asserted.
/SREQ	B3	Request – A target will assert REQ to indicate a byte is ready or is needed by the Target.
/CD	C3	Command/Data – Indicates Command or message phase when asserted, and Data phase when not asserted.
/SSEL	D3	SCSI Select – The line is driven after a successful arbitration to select as an initiator or reselect as a target and otherwise it is received.
/SMSG	E3	SCSI Message - Indicates a Message phase when asserted, and Command or Data phase when not asserted.
/RST	A4	Reset – Signal is interpreted as a hard reset and will clear all commands pending on the SCSI bus.
/ACK	B4	Acknowledge – Indicate a byte is ready for or was received from the Target.
/BSY	C4	Busy – Handshake signal used during arbitration.
/SATN	E4	Attention – This line is activated when a special condition occurs.
/WIDEPS	B5	Wide Present – When Low, indicates that a wide (16-bit) cable is present.
TERMPWR	C5, D5	Termination Power.
/SDPH, /SDPL	A8, B6	SCSI High/Low Parity – Provide odd parity for data lines.

3.7.3 Video Interface

Signal	Pin Assignation	Description
VSDA	D9	Video serial data line (video I2C)
VSCL	A10	Video serial clock line (video I2C)
HSYNC	B10	Horizontal sync line
VSYNC	C10	Vertical sync line
RED	D10	Analog Red video signal
GREEN	E10	Analog Green video signal
BLUE	A11	Analog Blue video signal

3.7.4 Ethernet 1 Interface

Signal	Pin Assignation	Description
ETX+0	A16	Ethernet 1 High Transmit Data line
ETX-0	B16	Ethernet 1 Low Transmit Data line
ERX+0	C16	Ethernet 1 High Receive Data line
ERX-0	D16	Ethernet 1 Low Receive Data line

3.7.5 Hot Swap HA (High Availability) signals

Signal	Pin Assignation	Description
BDSEL S6-S8	C11, E20, B25	Board Select, one of the shortest pins (the last to mate and the first to break contact).
HEALTHY S5-S8	C9, D15, C22, C25	Used to acknowledge the health of the board
PCIRST S5-S8	E9, E15, A25, D25	Used to indicate the CompactPCI Bus reset signal

3.7.6 IDE 1 Interface

Signal	Pin Assignation	Description
/BRSTDRV	A17	
SDD 0-15	B20, E19, C19, A19, D18, B18, E17, C17, D17, A18, C18, E18, B19, D19, A20, C20	Sec. Disk Data – These signals are used to transfer data to or from the IDE device.
SDREQ	A21	Sec. Disk DMA Request - This signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer.
/SDIOW	C21	Sec. Disk I/O Write – In normal IDE mode, this is the command to the IDE device that it may latch data from SDD lines.
/SDIOR	E21	Sec. Disk I/O Read – In normal IDE mode, this is the command to the IDE device that it may drive data on SDD lines.
SIORDY	B22	Sec. I/O Channel Ready – In normal mode, this input signal is driven directly by the corresponding IDE device IORDY signal.
/SDDACK	D22	Sec. DMA Acknowledge – This signal directly drives the IDE device /DMACK signal. It is asserted to indicate to IDE DMA slave devices that a given data transfer cycle is a DMA data transfer cycle.
IRQ15	E22	
/IOCS16	A23	
SDA 0-2	D23, B23, E23	Sec. Disk Address – These signals indicates which byte in either the ATA command block or control block is being addressed.
/SCS1, /SCS3	A24, B24	Secondary Chip Select - For ATA control register.
SEC-PD1	C24	
/FAL1	E24	

IDE 1 (IDE 1) is assigned to the Secondary IDE logical interface. It supports directly two IDE devices configured as master and slave devices.

3.8 J5 (P5 FOR MXS) SIGNAL SPECIFICATION

3.8.1 IDE 0 Interface

Signal	Pin Assignation	Description
/BRSTDRV	A1	
/BRSTDRV	B1	
PDD 0-15	B4, E3, C3, A3, D2, B2, E1, C1, D1, A2, C2, E2, B3, D3, A4, D4	Prim. Disk Data – These signals are used to transfer data to or from the IDE device.
PDREQ	A5	Prim. Disk DMA Request - This signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer.
/PDIOW	C5	Prim. Disk I/O Write – In normal IDE mode, this is the command to the IDE device that it may latch data from SDD lines.
/PDIOR	E5	Prim. Disk I/O Read – In normal IDE mode, this is the command to the IDE device that it may drive data on SDD lines.
PIORDY	B5	Prim. I/O Channel Ready – In normal mode, this input signal is driven directly by the corresponding IDE device IORDY signal.
/PDDACK	D5	Prim. DMA Acknowledge – This signal directly drives the IDE device /DMACK signal. It is asserted to indicate to IDE DMA slave devices that a given data transfer cycle is a DMA data transfer cycle.
IRQ14	E4	IRQ14 line
/IOCS16	A6	IOCS16 line
PDA 0-2	D6, C7, E6	Prim. Disk Address – These signals indicates which byte in either the ATA command block or control block is being addressed.
/PCS1, /PCS3	A7, B7	
PRI-PD1	D7	
/PDIAG	C6	

3.8.2 USB 0 and 1 Interfaces

Signal	Pin Assignation	Description
USBD1-0 (+/-)	B18, C18, D19, E19	USB Data – Differential data path for USB 0 and 1 ports
USBG 1-0	B19, D18	USB Ground – Differential ground reference for USB 0 and 1 ports
USBV 1-0	C19, E18	USB Voltage – Differential power level for USB 0 and 1 ports

3.8.3 Floppy Disk Interface

Signal	Pin Assignation	Description
/FD-DRVEN 0-1	E7, A8	Drive 0-1 density select
/FD-INDEX	B8	Index
/FD-MTR 0-1	C8, A9	Motor 0-1 enable
/FD-DS 0-1	E8, D8	Drive 0-1 select
/FD-DIR	B9	Direction
/FD-STEP	C9	Step pulse
/FD-WDATA	D9	Write disk data
/FD-WGATE	E9	Write gate
/FD-TRK0	A10	Track 0
/FD-WRTPRT	B10	Write protected
/FD-RDATA	C10	Read disk data
/FD-HDSEL	D10	Head select
/FD-DSKCHG	E10	Disk change

3.8.4 COM2

Signal	Pin Assignation	Description
/JDCD2	A11	Data Carrier Detect
JRXD2	C11	Receive Data
/JDSR2	D11	Data Set Ready
JTXD2	E11	Transmit Data
/JRTS2	A12	Ready To Send
/JCTS2	B12	Clear To Send
/JRI2	C12	Ring Indicator
/JDTR2	E12	Data Terminal Ready

3.8.5 COM1

Signal	Pin Assignation	Description
/JDCD1	A13	Data Carrier Detect
JRXD1	C13	Receive Data
/JDSR1	D13	Data Set Ready
JTXD1	E13	Transmit Data
/JRTS1	A14	Ready To Send
/JCTS1	B14	Clear To Send
/JRI1	C14	Ring Indicator
/JDTR1	E14	Data Terminal Ready

3.8.6 Parallel Port

Signal	Pin Assignation	Description
SLCT	A15	Printer select
PE	B15	Paper end
BUSY	C15	Busy signal
/ACK	D15	Acknowledge handshake
PD 0-7	E17, C17, A17, D16, C16, B16, A16, E15	Parallel port data bus
/SLCTIN	E16	Printer select
ALF	A18	Auto line feed
/INIT	B17	Initiate output
/ERR	D17	Error at printer
/STB	A19	Strobe signal

3.8.7 Miscellaneous Signals

Signal	Pin Assignation	Description
/SMBDATA	B20	Onboard SMbus data
/SMBALERT	C20	Onboard SMbus Alert (CPU overheating)
SMBCLK	E20	Onboard SMbus Clock
/PBRST	A22	Reset
/DIAG-OC	C22	Reserved
SPK-OUT	E22	Speaker signal

3.8.8 Keyboard Interface

Signal	Pin Assignation	Description
KDATA	A21	Keyboard data
KCLK	B21	Keyboard clock
VCC-KBD	C21	Keyboard power

3.8.9 Mouse Interface

Signal	Pin Assignation	Description
MDATA	D21	Mouse data
MCLK	E21	Mouse clock

PART 4

SOFTWARE SETUPS

1. BIOS SETUP PROGRAM
2. UPDATING OR RESTORING THE BIOS IN FLASH
3. VT100 MODE

4.1 BIOS SETUP PROGRAM

All relevant information for operating the board and connected peripherals is stored in the CMOS memory. A battery holds this information when the board is powered off, and the BIOS Setup program is required to make changes to the setup.

Make sure that the BIOS is properly configured prior to installing the operating system and its drivers.

To boot from the Ethernet interface, ensure that the *Boot from LAN* option is set to "Enabled" at the BIOS level (BIOS Features Setup option), and refer to the installation procedure in the LAN Boot & SCSI utility diskettes.

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided you need to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters but the *Standard CMOS Setup*, if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP default values provide optimum performance settings for all devices and system features.

NOTES

Make sure you setup the BIOS Setup software prior to installing your operating system and your drivers.

For systems that need the BIOS to first attempt to boot from LAN, follow these steps:

1. Set the *Boot From LAN First* option to "Enabled" in the BIOS Setup's *BIOS Features Setup*
2. Follow the complete procedure in the Boot From LAN utility diskette

4.1.1 Accessing the BIOS setup program

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the cPCI-MXS and cPCI-CXS system processors. The CPCI-MXS and CPCI-CXS use the AWARD Setup program, a setup utility in flash memory that is accessed by pressing the DELETE key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

CAUTION
Before modifying CMOS setup parameters, ensure that the W4 battery selection jumper is installed to enable the CMOS battery back up (please refer to Section 3.1).

To run the AWARD Setup program incorporated in the ROM BIOS:

Turn on or reboot the system.

Hit the DELETE key before or when the message - "Press DEL To Enter SETUP" appears near the bottom of the screen.

The main menu of the AWARD BIOS CMOS Setup Utility appears on the screen.

```
                    TEKNOR APPPLICOM T1023 BIOS VERSION 2.0
                              CMOS SETUP UTILITY
                          AWARD SOFTWARE, INC. (2A69TU00)

STANDARD CMOS SETUP                    LOAD BIOS DEFAULTS
BIOS FEATURES SETUP                    LOAD SETUP DEFAULTS
CHIPSET FEATURES SETUP                 SUPERVISOR PASSWORD
POWER MANAGEMENT SETUP                 USER PASSWORD
THERMAL MANAGEMENT SETUP               IDE HDD AUTO DETECTION
PNP/PCI CONFIGURATION                  SAVE & EXIT SETUP
INTEGRATED PERIPHERALS                 EXIT WITHOUT SAVING

Esc     :      Quit                    ↑ ↓ → ←      :      Select Item
F10     :      Save & Exit Setup       (Shift)F2    :      Change Color

                        Time, Date, Hard Disk Type . . .
```

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS Default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP Default values provide optimum performance settings for all devices and system features.

CAUTION

These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

4.1.2 Main Menu

The Main Menu includes the following categories:

Category	Description
Standard CMOS Setup	This Setup page includes all the items in a standard, AT-compatible BIOS (date, time, hard disk type, floppy disk type, video adapter type, memory…).
BIOS Features Setup	This Setup page includes all the items of AWARD's special enhanced features.
Chipset Features Setup	This Setup page includes all the items of the chipset's special features.
Power Management Setup	This Setup page sets power conservation options.
PnP/PCI Configuration	This Setup page sets plug and play and PCI configuration options.
CPU/Board Features Setup	This Setup page sets processor speed, thermal management and board monitoring options.
Integrated Peripherals	I/O susbsystems that depend on the integrated peripherals controller in your system.
Load Bios Defaults	The BIOS defaults are fail safe settings which consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.
Load Setup Defaults	The Setup defaults are the optimal settings that provide the optimum performance for all devices and system features. **If the CMOS RAM is corrupted, the Setup defaults are loaded automatically.**
Supervisor/User Password Setting	Change, set or disable the password. It allows you to limit the access to the system and the Setup, or only to the Setup.
IDE HDD Auto Detection	Forces the detection of the IDE hard disk drives parameters and puts them in the Standard CMOS Setup page.
Save & Exit	After having modified the BIOS Setup, you can save the configuration in CMOS RAM and the Flash BIOS, by selecting this option.
Exit Without Saving	This option is used to exit AWARD Setup without saving the configuration to CMOS RAM or Flash BIOS.

4.1.3 Setups

The arrow keys (↑ ↓ → ←) are used to highlight items on the menu and the PAGEUP and PAGEDOWN keys are used to change the entry values for the highlighted item. To enter in a submenu, press the ENTER key. Also, you can press the F1 key to obtain help information or the ESC key to close a menu or to quit the program.

Key	Function
↑	Moves to previous item.
↓	Moves to next item.
←	Moves to the item a the left.
→	Moves to the item at the right.
ESC	When in the Main Menu: Quits program (Answer 'Y' to save changes into CMOS). When in other screens: Exits and returns to the Main Menu.
PAGEUP or +	Increases the numeric value or changes value.
PAGEDOWN or -	Decreases the numeric value or changes value.
F5	When in the Main Menu: Restores the previous setup values for all the BIOS parameters (except Standard CMOS Setup) which were displayed when you entered the program. When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup or Integrated Peripherals Setup: Restores the previous setup values for that setup screen only.
F6	When in the Main Menu: Loads the BIOS Defaults of all the BIOS parameters (except Standard CMOS Setup). The BIOS Defaults are fail safe settings, which consists of the safest set of parameters. When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup or Integrated Peripherals Setup: Loads the BIOS Defaults for all the BIOS parameters for that setup screen only.
F7	When in the Main Menu: Loads the Setup Defaults for all the BIOS parameters (except Standard CMOS Setup). When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup or Integrated Peripherals Setup: Loads the Setup Defaults for the BIOS parameters for that setup screen only. If the CMOS RAM is corrupted, the Setup defaults are loaded automatically.
F10	When in the Main Menu: Saves all the CMOS changes and exit.

4.1.4 Standard CMOS Setups

Function	Description
Date/Time	The current values for each category are displayed. Enter new values through the keyboard.
Hard Disks	Two IDE controllers are defined on the cPCI-MXS and Cpci-CXS boards. The Primary and Secondary controllers can both have two disks: Master Disk or Slave Disk. Only three settings are available for the hard disk type: Auto, User and None. Type 1 to 46 are not predefined in the system: Use auto-detect or enter the parameters for the type in the user-defined.
Drive A / Drive B	Select the type of floppy disk installed for drive A and drive B.
Video	This option specifies the basic type of display adapter card installed in the system.
Halt on	This option specifies the type of errors that will stop the system during the BIOS booting procedure. A message asks that you press F1 to continue or press the DELETE key to enter Setup. The settings are: All errors, No errors, All but keyboard, All but diskette, and All but disk/key (default setting).
Memory	This display-only option indicates the amount of Base, Extended and other types of memory installed in the system.

4.1.5 Saving & Exiting Operations

Use one of the following options available from the Main Menu:

Function	Description
Save & Exit	After having modified the BIOS Setup, you can save the configuration in CMOS RAM and the Flash BIOS, by selecting this option.
Exit Without Saving	This option is used to exit AWARD Setup without saving the configuration to CMOS RAM or Flash BIOS.

4.1.6 BIOS Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Virus Warning	Dis.	Dis.	En. / Dis.	When Enabled, you receive a warning message if a program (specifically, a virus) attempts to write to the boot sector or the partition table of the hard disk drive. You should then run an anti-virus program. Keep in mind that this feature protects only the boot sector, not the entire hard drive. **Note: Many disk diagnostic programs and OS setups (e.g., Win95 setup), that access the boot sector table, can trigger the virus warning message. If you plan to run such a program, we recommend that you first disable the virus warning.**
Quiet POST	Dis.	Dis.	En./Dis.	At the power on self-test (POST), only the AWARD logo and the "Press DEL to enter SETUP" message appears.
Quick Power On Self Test	Dis.	En.	En./Dis.	Select Enabled to reduce the amount of time required running the POST. A quick POST skips certain steps. We recommend that you enable quick POST to save time, since most major OS do their own tests
Full Screen Logo Show	Dis.	Dis.	En./Dis.	When enabled, a full screen bitmap (.BMP) picture will appear during the POST or you can have a logo being displayed if you ask for a "Special Modification Request".
Boot from LAN First	Dis.	Dis.	En./Dis.	If Enabled, the BIOS will first attempt to boot from the LAN. The complete procedure for this function is available on the "Boot from LAN" utility diskette.
Raid Card Boot First	Dis.	Dis.	En./Dis.	If Enabled, the BIOS will first attempt to boot from the RAID disk card.
Boot Sequence	A,C, SCSI	C,A, SCSI	A,C,SCSI; C,A,SCSI; C,CDROM,A; CDROM,C,A; D,A,SCSI; E,A,SCSI; F,A,SCSI; SCSI,A,C; SCSI,C,A; C only; LS/ZIP,C.	This option defines the searching order in the BIOS for the boot device(s). **Note: The Boot from LAN First and Raid Card Boot First options take precedence over this option.**
Swap Floppy Drive	Dis.	Dis.	En./Dis.	Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B.
Boot Up Floppy Seek	En.	Dis.	En./Dis.	When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360KB floppy drives have 40 tracks; drives with 720KB, 1.2MB, and 1.44MB capacity all have 80 tracks. Because very few modern PCs have 40 track floppy drives, we recommend that you set this field to "Disabled" to save time.
Drive A Boot Permit	En.	En.	En./Dis.	When Disabled, this option will not permit booting from Drive A.
Floppy Disk Access Control	R/W	R/W	R/W, Read Only	When Read Only, this option will not permit writing to the floppy disk.

BIOS Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Report No FDD For Win 95	No	No	Yes, No	Select Yes to release IRQ6 when the system contains no floppy drive, for compatibility with Windows 95 logo certification. In the Integrated Peripherals screen, select NO or the Onboard FDC Controller option.
Hard Disk Write Protect	Dis.	Dis.	En./Dis.	When Enabled, this option will not permit writing to the hard disk.
HDD S.M.A.R.T. Capability	Dis.	En.	En./Dis.	When Enabled, the Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.) features of the HDD are supported. S.M.A.R.T is used for prediction of device degradation and/or faults.
Delay For HDD (Secs)	0	0	0-15	This number of seconds inserted prior to HDD initialization. 0 is disabled.
OS Select For DRAM > 64MB	Non-OS/2	Non-OS/2	Non-OS/2, OS/2	Select OS2 only if you are running OS/2 with greater than 64MB of RAM.
Gate A20 Option	Norm.	Fast	Normal, Fast	When Fast, enables fast switching of Gate A20 via the 440BX chipset, instead of the keyboard controller.
Security Option	Setup	Setup	Setup, Normal	If you have set a password, select whether the password is required every time the system boots (“System” option), or only when you enter Setup (“Setup” option).
Diskette Access For	All	All	All, Supervisor	When this option is set to Supervisor and the Security option to System, all floppy disk accesses (read/write) are limited to the Supervisor (supervisor password required).
Boot Up NumLock Status	On	On	On, Off	Control the state of the NumLock key when the system boots. When set to “On”, the numeric keypad generates numbers instead of controlling cursor operations.
Typematic Rate Setting	Dis.	En.	En./Dis.	When Disabled, the following two items (Typematic Rate and Typematic Delay) are irrelevant. Keystrokes repeat at a rate determined by the keyboard controller in your system. When Enabled, you can select a typematic rate and a typematic delay.
Typematic Rate (Chars/s)	30	30	6-30 char/sec.	When the typematic rate setting is Enabled, you can select a typematic rate (the rate at which characters repeat when you hold down a key).
Typematic Delay (msec)	250	250	250-1000 ms	When the typematic rate setting is Enabled, you can select a typematic delay (the delay before keystrokes begin to repeat when you hold down a key).
VT100 Settings				
Comport	1	1	1,2,3,4	Use this option to select which COM port will be used for VT100
Speed	Auto	Auto	Auto, 2400, 9600, 19200, 38400, 57600, 115200	Select the baud rate of COM port. being used in VT100 mode.
Parity	None	None	None, Odd, Mark, Even, Space	Use this option to select the parity .
Data	8	8	7, 8	Use this option to specify the number of data bits being used.
Stop	1	1	1, 2	Use this option to specify the number of stop bits being used.

4.1.7 Chipset Features Setup

This part of the setup allows you to define chipset-specific options and features.

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
CPU Internal Cache	Dis.	En.	En./Dis.	Enables or Disables the CPU Internal Cache (L1 cache).
External Cache	Dis.	En.	En./Dis.	Enables or Disables the External Cache (L2 cache).
CPU L2 Cache ECC Checking	Dis.	En.	En./Dis.	Enables or Disables ECC Checking for L2 cache. **Note: processors provided by Teknor support ECC. However, not all Pentium® II / III processors support ECC. Check Intel's website to know if your processor supports ECC:** http://developer.intel.com/support/processors/pentiumII/identify.htm.
SDRAM RAS-to-CAS Delay	3	3	2, 3	**Note: Upon boot-up, the BIOS will detect and display the optimal value for the SDRAM options (first four options in this menu), if it is different from the Setup value. You must enter the AWARD Setup, and set the options at the suggested value if you want the best performance.** This option inserts a timing delay between the CAS and RAS strobe signals, used when SDRAM is written to, read from, or refreshed. The number selected is the number of clocks to be inserted between a row activate command and either a read or write command.
SDRAM RAS Precharge Time	3	3	2, 3	Selects the number of CPU clocks for the RAS precharge. If an insufficient number of cycles is allowed for the RAS to accumulate its charge before SDRAM refresh, the refresh may be incomplete and the DRAM may fail to retain data.
SDRAM CAS Latency Time	3	3	2, 3	This option controls the number of clocks between when a read command is sampled by the SDRAMs and when the chipset samples read data from the SDRAMs. Select 3 for 3 DCLKs and 2 for 2 DCLKs. If a given row is populated with a registered SDRAM DIMM, an extra clock is inserted between the read command and when the chipset samples read data.
SDRAM Precharge Control	Dis.	Dis.	En./Dis.	When Enabled, all CPU cycles to SDRAM result in an All Banks Precharge Command on the SDRAM interface.
DRAM Data Integrity Mode	Non-ECC	ECC	ECC, Non-ECC	When set to ECC, allows auto-correction of the data read from memory. The ECC error flags' status register and the error pointer are updated if error correction occurs in this mode. When set to Non-Ecc, no error checking or error reporting is done. This option will work in ECC mode only if all installed memory banks supports ECC (Error Checking and Correction)
Memory Hole At 15M-16M	Dis.	Dis.	En./Dis.	You can reserve this area of system memory for ISA adapter ROM. When this area is reserved, it cannot be cached. The user information of peripherals that need to use this area of system memory usually discusses their memory requirements.
Video BIOS Cacheable	Dis.	En.	En./Dis.	Selecting Enabled allows caching of the video BIOS ROM at C0000h plus the VGA BIOS size, resulting in better video performance. However, in any program writes to this memory area, a system error may occur.
Video RAM Cacheable	Dis.	En.	En./Dis.	When Enabled, video memory region is cacheable. Some off-board video card drivers may behave strangely; in such a case, disable this option.
8 Bit I/O Recovery Time	3	1	1-8, NA	The I/O recovery mechanism adds bus clock cycles between PCI-originated I/O cycles to the ISA bus. This delay takes place because the PCI bus is much faster than the ISA bus. These two fields let you add recovery time (in bus clock cycles) for 8-bit and 16-bit I/O.
16 Bit I/O Recovery Time	2	1	1-4, NA	

Chipset Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
PCI/VGA Palette Snoop	Dis.	Dis.	En./Dis.	Palette snooping allows multiple VGA devices operating on different buses to handle data from the CPU on each set of palette registers. When set to Enabled, data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA device's palette registers, permitting the palette registers of both to be identical. When set to Disabled, data read and written by the CPU is only directed to the PCI VGA device's palette registers.
Passive Release	En.	En.	En./Dis.	When Enabled, CPU to PCI bus accesses are allowed during passive release otherwise the arbiter only accepts another PCI master access to local SDRAM.
Delayed Transaction	Dis.	Dis.	En./Dis.	The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specifications version 2.1.
Supervisor I/O Base Address	190h	190h	190h, 290h, 390h	This option determines the base address for the Supervisor I/O Register, which is used for such functions as power fail detection and the watchdog timer.
Power-Supply Type	AT	AT	AT, ATX	This option selects the type of power supply.
AGP Aperture Size (MB)	64	64	4 to 256	This option selects the size in megabytes of the AGP Aperture.
Video BIOS Shadow	En.	En.	En./Dis.	Software that resides in a read-only memory (ROM) chip on a device is called *firmware*. Award permits shadowing of firmware such as the system BIOS, video BIOS, and similar operating instructions that come with some expansion peripherals. Shadowing copies from ROM into system RAM, where the CPU can read it through the 64-bit DRAM bus. Firmware not shadowed must be read by the system through the 8 or 16-bit ISA bus. Shadowing improves the performance of the system BIOS and similar firmware for expansion peripherals. Enable shadowing into each section of memory separately. Many system designers hardwire shadowing of the system BIOS and eliminate a System BIOS Shadow option. Note that on a PCI VGA card (on board or off-board), the VGA BIOS is always shadowed. Video BIOS shadows into memory area C0000 plus the VGA BIOS size. The remaining areas between C0000 and DFFFF shown on the BIOS Features Setup screen may be occupied by other expansion card firmware. If an expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies to shadow it into the correct area of RAM.
C8000-CBFFF	En.	En.	En./Dis.	
CC000-CFFFF	En.	En.	En./Dis.	
D0000-D3FFF	En.	En.	En./Dis.	
D4000-D7FFF	En.	En.	En./Dis.	
D8000-DBFFF	En.	En.	En./Dis.	
DC000-DFFFF	En.	En.	En./Dis.	

4.1.8 Power Management Setup

This part of the setup configures power conservation options.

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
ACPI Function	Dis.	En.	En./Dis.	The Advanced Configuration and Power Interface (ACPI) allows Operating System Direct Power Management (OSPM) and make advanced configuration architectures possible. When Enabled, the OS supports ACPI or OSPM (e.g., Win98, Windows NT5 and Windows 2000 **Note: When Enabled, and the OS is ACPI compliant, the OS setting take precedence over all settings in this menu.**
Power Management	User Def.	User Def.	User Define, Min Saving, Max Saving	This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. Max Saving: Maximum power savings. Inactivity period is 1 minute in each mode. Min Saving: Minimum power savings. Inactivity period is the maximum setting in each mode (1 hour for Doze, Standby and Suspend). User Define: Set each mode individually. Select time-out periods in the PM Timers section (see below).
PM Control by APM	Yes	Yes	Yes, No	If Yes, the OS can control the PM by APM calls. If No, the BIOS will control the PM (Power Management)
Video Off Method	V/H SYNC + Blank	V/H SYNC + Blank	Blank Screen V/H SYNC+Blank, DPMS,	Determines the manner in which the monitor is blanked. V/H SYNC + Blank: System turns off vertical and horizontal synchronization ports and writes blanks to the video buffer. DPMS Support: Select this option if your monitor supports the Display Power Management Signaling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsystem to select video power management values. Blank Screen: System only writes blanks to the video buffer.
Video Off After	Standby	Standby	NA, Suspend, Standby, Doze,	As the system moves from lesser to greater power-saving modes, select the mode **in which you want the monitor to blank.**
Doze Mode	Dis.	Dis	Disable 1min to 1h	After the selected period of system inactivity (1 minute to 1 hour), the CPU clock runs at lower speed while all other devices still operate at full speed.
Standby Mode	Dis.	Dis.	Disable 1min to 1h	After entering Doze mode and the selected period of system inactivity (1 minute to 1 hour) has elapsed, the video shuts off while all other devices still operate at full speed.
Suspend Mode	Dis.	Dis.	Disable 1min to 1h	After entering Standby mode and the selected period of system inactivity (1 minute to 1 hour) has elapsed, all devices including the CPU shut off and the system waits for an event to wake them up again.
HDD Power Down	Dis.	Dis.	Disable 1-15min	After the selected period of drive inactivity (1 to 15 minutes), the hard disk drive powers down while all other devices remain active. The HDD power down mode is only available if the hard drive has this capability.
HDD Down When Suspend	En.	En.	En./Dis.	When Enabled and the system goes in Suspend Mode, the hard disk is shut down.
Throttle Duty Cycle	75.0%	75.0%	12.5%-75.0%	When the system enters Doze mode, the CPU clock runs only part of the time. You may select the percentage of time that the clock **does not run.** When 12.5% is selected, the CPU is running at nearly Full Speed and if 75% is selected, the CPU will be idle at 75% of time.
PCI / VGA Act-Monitor	Dis.	Dis.	En./Dis.	When Enabled, continuous video activity restarts the global timer for Standby mode.
Soft-OFF by PWR-BTTN	Instant-off	Instant-off	Instant-off, Delay 4 sec.	This option only works with an ATX power supply. It allows two configurations for the power button: Instant-off for power supply on/off switch, or Delay 4 sec. for entering Suspend Mode after pressing the button at least 4 seconds.

Power Management Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Resume by Ring	Dis.	En.	En./Dis.	When Enabled and a modem is connected to a COM port, allows a modem ring to re-activate the CPU when in Suspend mode.
IRQ 8 Break Suspend	Dis.	En.	En./Dis.	When Enabled, the RTC alarm interrupt is monitored to allow an interrupt to awaken the system when in Doze, Standby or Suspend Mode.
Resume by Alarm	Dis.	Dis.	En./Dis.	When Enabled, allows setup of a time to re-activate the CPU when in Suspend mode with the options Date (of Month) Alarm and Time (hh:mm:ss) Alarm. **Note: The IRQ 8 Break Suspend option in this setup screen must be Enabled to use the RTC alarm.**
Reload Global Timer Events:				
IRQ[3-7,9-15], NMI	Dis.	En.	En./Dis.	When any of the options below is Enabled, monitoring of the interrupt will occur to allow an interrupt to awaken the system when in Doze, Standby or Suspend Mode.
Primary IDE 0	Dis.	En.	En./Dis.	
Primary IDE 1	Dis.	En.	En./Dis.	
Secondary IDE 0	Dis.	En.	En./Dis.	
Secondary IDE 1	Dis.	En.	En./Dis.	
Floppy Disk	Dis.	En.	En./Dis.	
Serial Port	En.	En.	En./Dis.	
Parallel Port	Dis.	En.	En./Dis.	

4.1.9 PnP/PCI Configuration

This part of the setup configures PnP/PCI options.

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
PNP OS Installed	Yes	No	Yes, No	If the operating system (OS) is Plug and Play (for example Windows 95), select "**Yes**" if you want the OS to allocate resources according to Plug and Play standards, or "**No**" if you want the same resource allocations at every system boot-up. Select "**No**" when the OS is **not** Plug and Play (for example, DOS). **Note: When set to "Yes", only the boot devices will get Resources.**
Resources Controlled By	Auto	Man.	Auto, Man.	The Award Plug and Play BIOS can automatically configure all the boot and Plug and Play-compatible devices. If you select Auto, all the interrupt requests (IRQs) and DMA assignment fields disappear as well as Used Mem Base Address and Lenght as the BIOS automatically assigns them.
Reset Configuration Data	Dis.	Dis.	En./Dis.	Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.
IRQ *n* Assigned To	PCI/ISA PnP	PCI/ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific interrupt, such as IRQ4 for serial port 1. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for an IRQ line, this resource will not be available for PCI/ISA PnP.
DMA *n* Assigned To	PCI/ISA PnP	PCI/ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system DMA channel as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific DMA channel. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for a DMA channel, this resource will not be available for PCI/ISA PnP.
Init Display First	Onboard	Onboard	PCI Slot, Onboard, AGP	Initializes the specified video display. The chosen display becomes the primary display. Other display devices are ignored by the BIOS and configured by the OS.
Assign IRQ For VGA	Dis.	Dis.	En./Dis.	When Enabled, the video card is assigned an IRQ.
Assign IRQ For USB	En.	En.	En./Dis.	When Enabled, the USB is assigned an IRQ. When Disabled, the IRQ is freed up for another purpose.
PCI Latency Timer	32	32	0-255 (integers)	This option specifies the value of the Latency Timer for the PCI bus master, in units of PCI bus clocks.
Used MEM Base Address	N/A	N/A	N/A, C800, CC00, D000, D400, D800, DC00	Select a base address for the memory area used by any peripheral that requires high memory.
Used MEM length	16K	16K	16K, 32K, 48K, 64K	Select a base address for the memory area used by any peripheral that requires high memory. When this option is not set to N/A, the menu for used memory lengths available is displayed.

4.1.10 CPU/Board Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Current Processor(s) Speed	nnn	nnn	nnn	This option displays the current processor speed.
Front Side Bus Speed	nnn	nnn	nnn	This option displays the current Front Side Bus speed. This speed is selected by the CPU auto-detection logic.
Thermal Management Options:				
. Thermal Management	Dis.	Dis.	En./Dis.	When this option is enabled, the CPU temperature is monitored. Whenever the CPU overheats, the CPU slows down to lower the temperature.
. Thermal Audio Alarm	Dis.	Dis.	En./Dis.	When the Thermal Management option and this option are enabled, a continuous audible alarm is sounded when the temperature specified in the Overheat Alarm options is reached. Such an alarm may not be supported by the Operating System.
. CPU 1 Die Temperature	-	-	Varies	Displays the current die (internal) CPU temperature, when Thermal Management is enabled.
. Resume Alarm (°C)	50	50	10-70	The CPU will be slowed down (Doze mode) when it reaches the selected Overheat Alarm (°C) temperature. Full speed (Normal mode) will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 4° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm.
. Overheat Alarm (°C)	70	70	30-90	The CPU will be slowed down (Doze mode) when it reaches the selected Overheat Alarm (°C) temperature. Full speed (Normal mode) will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 4° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm
. CPU1 Local Temperature	-	-	Varies	Displays the current case (external) CPU temperature, when Thermal Management is enabled.
. Resume Alarm (°C)	42	42	10-70	The CPU will be slowed down (Doze mode) when it reaches the selected Overheat Alarm (°C) temperature. Full speed (Normal mode) will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 4° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm.
. Overheat Alarm (°C)	50	50	30-90	
Save CMOS in Flash	Dis.	Dis.	En./Dis.	Saving CMOS memory content into Flash Memory will prevent to loose CMOS options when battery fails.
Watchdog Timer	Dis	Dis	En./Dis.	This option enables the Watchdog option when the POST is running.
Watchdog After POST	Ds	Dis	En./Dis.	This option enables Watchdog circuit after the POST sequence
Watchdog Duration (ms)	262144	262144	64 to 262144	Use this option to setup duration time (in ms) of the Watchdog timing circuitry.
Current CPU Fan 1 and 2 speed	-	-	Varies	Speed sensing device sets this value according to the fan speed. If no fan is installed or if a fan has no tachymetric capability, this value will be 0.
Current Vcpp1 and 2	-	-	Varies	This value is set according to the actual value of Vcpp1 & Vcpp2
Vin values : +12V, +5V, +3.3V, +2.5V	-	-	Varies	The values of these voltages are each displayed according to the current value.

4.1.11 Integrated Peripherals

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
On-Chip Primary/Secondary	En.	En.	En./Dis.	Select Enabled to activate the Primary/Secondary IDE channel. The four options below appear only if the On-Chip Primary option is enabled.
On-Chip Primary IDE				
Master PIO Slave PIO Master UDMA Slave UDMA	Auto	Auto	Auto, Modes 0-4	Use this option to set a PIO mode (0-4) for each of the onboard IDE devices. Modes 0 through 4 provide successively increased performance and speed. In Auto mode, the system automatically determines the best mode for each device. If you select a mode that the drive does not support, it may not work, so choose a lesser value or Auto to see the best mode for the drive.
On-Chip Secondary IDE				
Master PIO Slave PIO Master UDMA Slave UDMA	Dis.	Auto	Auto, Disabled.	Ultra DMA/33 implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If your hard drive and your system software both support Ultra DMA/33, select Auto to enable BIOS support.
IDE HDD Block Mode	Dis.	En.	En./Dis.	Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.
Onboard PCI SCSI Chip	En.	En.	En./Dis.	Enables/disables the onboard SCSI controller.
Ethernet Controller 1 and 2	En.	En.	En./Dis.	Enables/disables the onboard Ethernet controller.
USB Keyboard Support	OS	OS	OS/BIOS	This option is for DOS and BIOS support only (Win 95 has it is own drivers). **It does not enable or disable the USB controller.**
PS/2 Mouse Function Control	Auto	Auto	Auto/Dis.	When set to Auto, the PS/2 mouse is automatically enabled, if it is present.
Onboard FDC Controller	En.	En.	En./Dis.	Select Disabled to disable the onboard floppy disk controller (FDC).
Onboard Serial Port 1	3F8/ IRQ4	3F8/ IRQ4	Dis, 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3	Select a COM port address and IRQ# for Serial Port 1
Onboard Serial Port 2	Dis	2F8	3F8,2F8, 3E8, 2E8 Disabled	Select a COM port address for Serial Port 2.
IRQ Line	3	3	3,4,5,7	Sets IRQ line for serial port 2
Onboard Serial Port 3	3E8/ IRQ4	3E8/ IRQ4	Dis, 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3	Select a COM port address and IRQ# for Serial Port 3
Serial Port 3 Mode	RS-232	RS-232	RS-232 RS-422 RS-485	Select the operation mode for Serial Port 3.
Onboard Serial Port 4	Dis	2E8	3F8,2F8, 3E8, 2E8 Disabled	Select a COM port address for serial port 4.
IRQ Line	3	3	3,4,5,7	Sets the IRQ line for serial port 4.
Onboard Parallel Port	378/ IRQ7	378/ IRQ7		Select a LPT address and IRQ# for the physical parallel (printer) port. Possible settings are: Disabled, 3BC/IRQ7, 378/IRQ7, 278/IRQ5,
Parallel Port Mode	ECP + EPP1.9	ECP + EPP1.9		Select an operating mode for the onboard parallel port. Select ECP or EPP unless you are certain both your hardware and software does not support ECP or EPP mode. Possible settings are SPP, EPP1.9+SPP, ECP, ECP+EPP1.9, Normal, EPP1.7+SPP, ECP+EPP1.7
ECP Mode Use DMA	3	3	1, 3	Select a DMA channel for the parallel port.

4.2 UPDATING OR RESTORING THE BIOS IN FLASH

4.2.1 UBIOS.EXE 4.0 - BIOS update and copy utility.

> **IMPORTANT**
> This utility is used to update the BIOS on Teknor's single board computer. To ensure the success of this operation, please read entirely these instructions before using this program.

You can this utility in 2 different modes :

Interactive Mode: In this mode the program is menu-driven. This mode is explained in section 4.2.4

Batch Mode: It is also possible to run the program without menus by a command which specifies the selected options and files with parameters. This mode is explained in section 4.2.4.4

4.2.2 How to do a successful update

UBIOS needs to be run in DOS 3.3 or higher or compatible environment.

1. Take note of your special BIOS options such as drive settings, hard disks and custom settings.
   After the update, these options will be set to their default values and all changes will need to be re-entered.
2. Ensure you have the proper BIOS file required to execute the update.
   These files may be obtained from Teknor WEB site, by Teknor technical support or by UBIOS itself.
   Refer to the 'How to do a successful copy' for details about the last source.
3. Boot in a driver free environment. **No Hi-memory driver must be loaded**.
   To boot with a free environment, follow these steps :
   - **In DOS**:
     Boot with the F5 key pressed, this will disable config.sys and autoexec.bat interaction.
   - **In Windows 9x**:
     Boot with the F8 key pressed and choose *'safe mode command prompt only'* option.

4. Call the UBIOS program and follow the instruction menu. To do a complete BIOS update, select item 'A) Update all BIOS'.

4.2.3 How to do a successful copy

Follow the same procedure as above.

To do a complete BIOS copy, select item '**a) Copy all BIOS'.**

Advanced functionality

Advanced functionality are resumed in the UBIOS help mode.
To call UBIOS help page, use UBIOS /?

VT-100 mode

UBIOS can be used without a screen in Teknor's VT-100 mode. This mode transfers all screen and keyboard text activity through the serial port.

To use UBIOS in vt-100, use the /vt argument like: UBIOS /vt

In this mode, scan code keys are not transmitted. These keys include the 'home', 'end', 'Pg Up', 'Pg Dn' keys that can be useful to UBIOS. To bypass this limitation, the numerical keypad can be used.

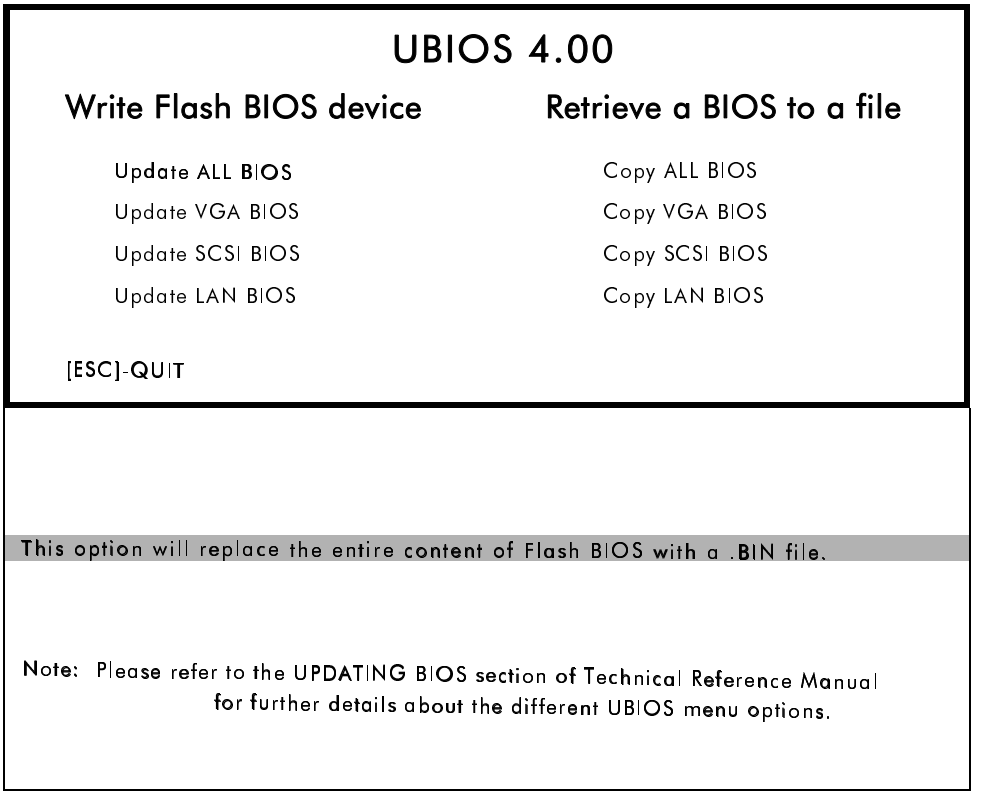
'7' will be assigned to 'home',
'8' to the up arrow,
'9' to 'Pg Dn'
…
'5' will be assigned to the 'Esc' key.

4.2.4 UBIOS - Interactive Mode

To run the program in interactive mode, type "UBIOS" from the DOS prompt and the UBIOS 4.0 presentation screen will be displayed. To continue, hit any key on the keyboard. This brings you to the main menu.

4.2.4.1 Main Menu

The main menu appears below:



The main menu displays two groups of options: Write Flash BIOS device and Retrieve a BIOS to a file. The first group allows you to update the Flash BIOS device with a BIOS file stored on disk. The second group allows you to copy the contents of the Flash BIOS device to files on disk.

In the above menu, the option **Update ALL BIOS** is highlighted and the option is described in the shaded row below. Move the arrow keys to highlight other options.
To **select** the highlighted option, press ENTER.
To **exit the program**, press the ESC key when you are in the main menu.

There are four types of BIOS files appearing on the main menu:

1. ALL BIOS File: This file combines all BIOS files contained in the Flash BIOS device in a single file. It has the .BIN extension.

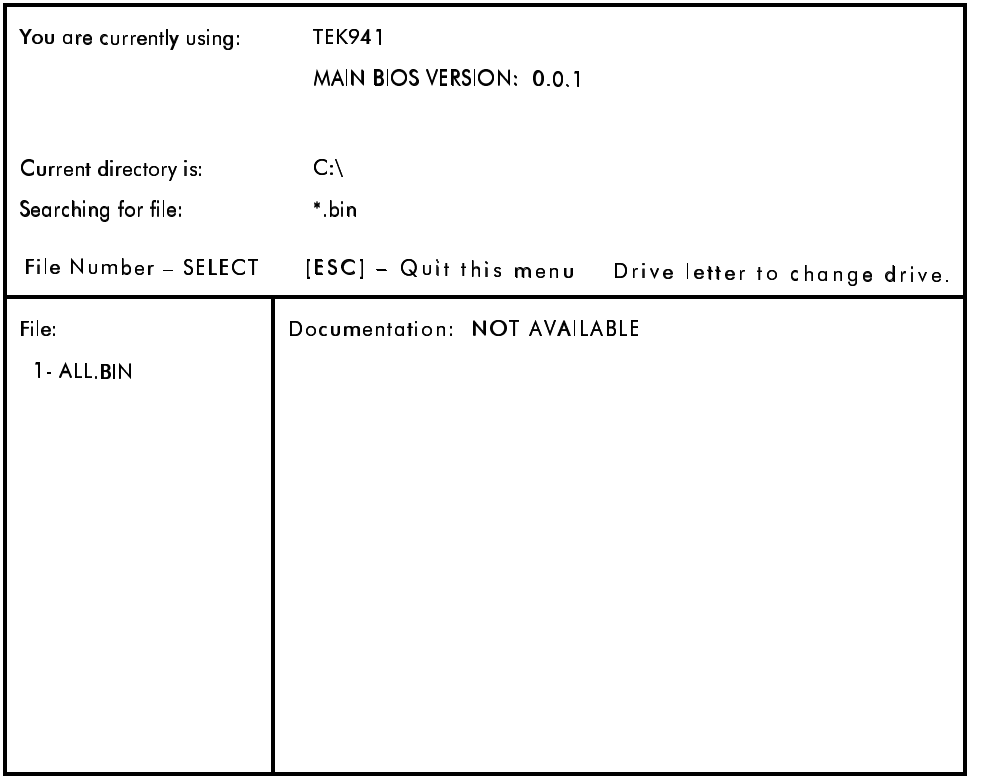
2. VGA BIOS File: This file contains the VGA BIOS section of the Flash BIOS. There are two possible types of VGA BIOS files: files with the .VGA extension (supports CRT displays only) and files with the .BFP extension (supports CRT and Flat Panel displays).

3. SCSI BIOS File: This file contains the SCSI BIOS section of the Flash BIOS. It has the .BIN or .SCS extension.

4. LAN BIOS File: This file contains the LAN BIOS section of the Flash BIOS. It has the .BIN extension.

4.2.4.2 Updating Flash BIOS

If you select one of the **Update** options from the main menu, a screen similar to the following is displayed:



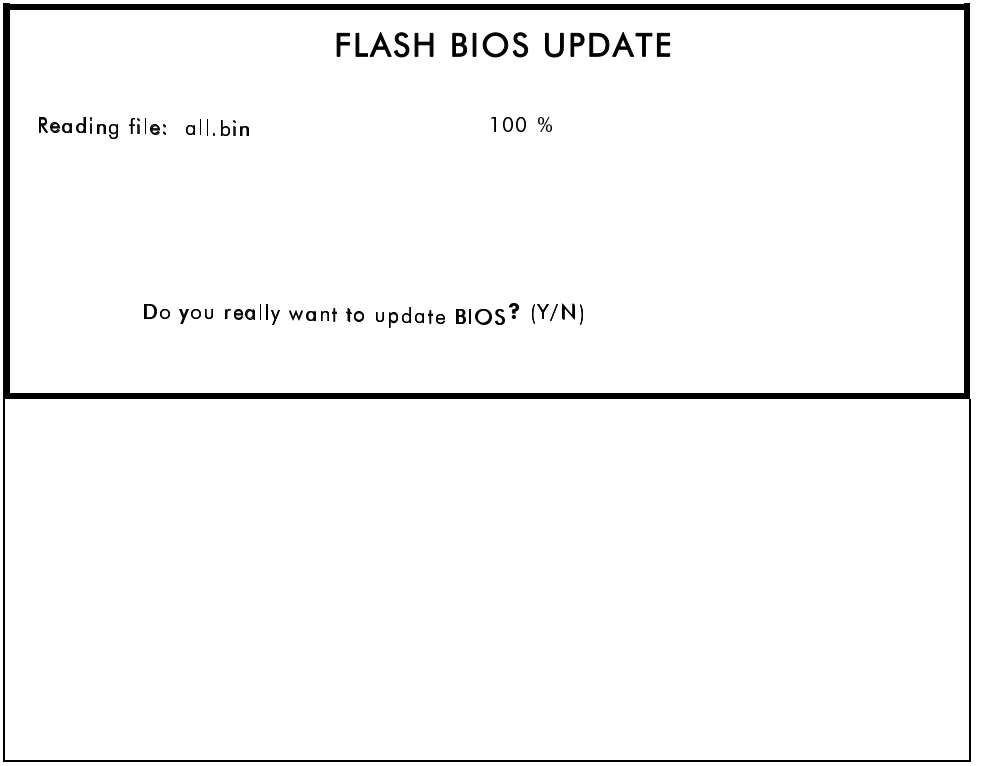
Files of the type you selected in the main menu and which are in the current directory are displayed in the **File** window.

To change directory, type the drive letter. If there are any files of the type you selected in this directory, they will be displayed in the **File** window.

The **Documentation** window displays “NOT AVAILABLE”. It will be used in the future for displaying the contents of a .doc file.

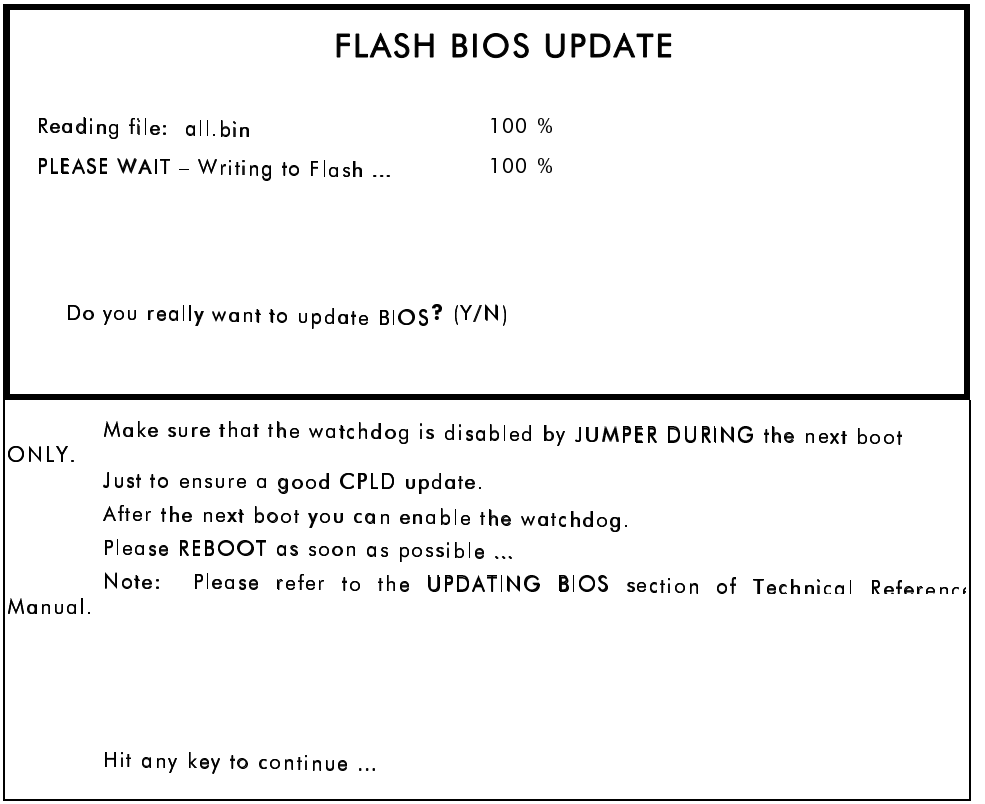
If you want to return to the previous menu, press the ESC key.

To select a file from the **File** window, in order to update the Flash BIOS with this file, type the file number which appears before the filename in the list. A new screen is displayed as shown below. This is the Flash BIOS Update screen. You must first confirm if you want to update the Flash BIOS with the selected file (the filename appears next to **Reading file)**, by typing "Y" for Yes, "N" for No.



If you choose to update the file, by typing "Y", the program will write the file to Flash. The progress of the operation is indicated in percentage completed, next to **PLEASE WAIT – Writing to Flash …**

When the update is over the screen will appear as follow:

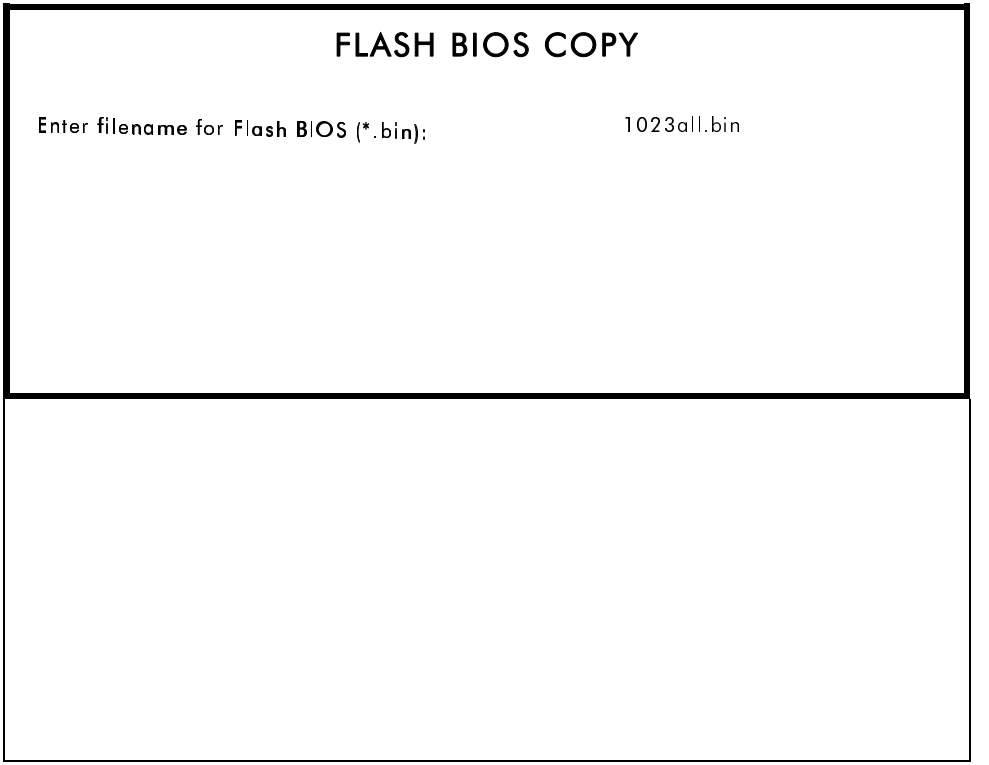


To return to the main menu, hit any key on the keyboard.

> **NOTE**
> There may be slight changes to the Flash BIOS Update screen compared to those shown here for an Update ALL BIOS operation. Also, if an error occurs, these will be indicated on the screen.

4.2.4.3 Copying Flash BIOS

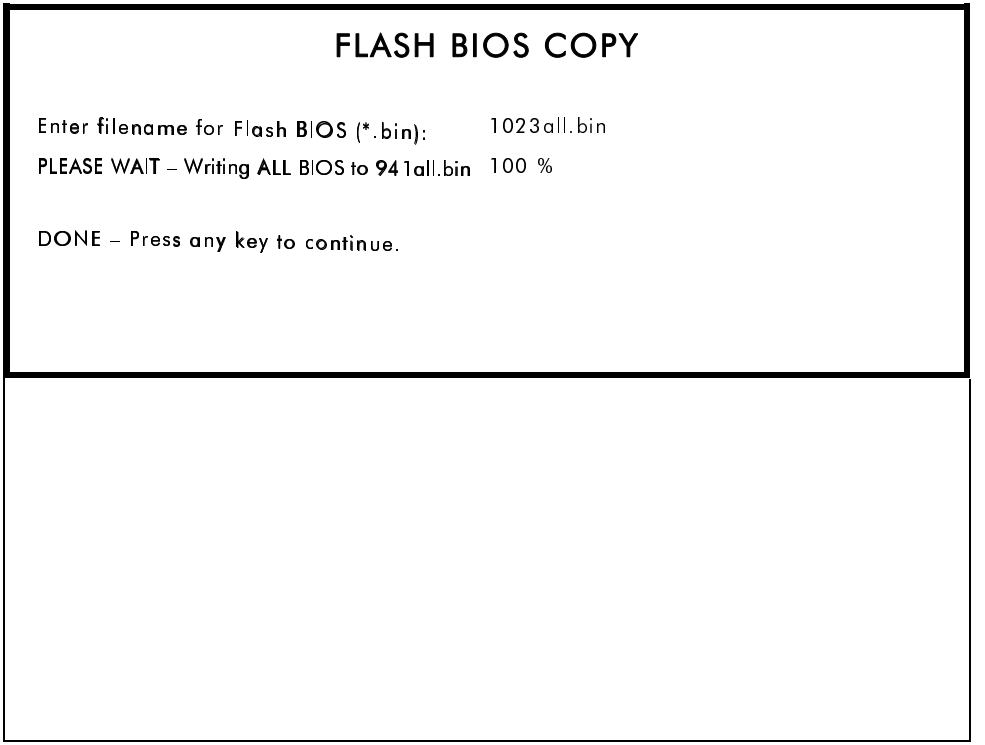
If you select one of the **Copy** options from the main menu, a screen similar to the following is displayed:



You begin a Flash Copy operation, by typing a filename (including the extension) for the file you are creating. In the above example, the filename entered was “1023all.bin”.

Press ENTER to proceed.

The progress of the operation will display on the screen in percentage completed. The example shown on the following page is for the Copy ALL BIOS option.



If the filename entered for the BIOS file already exists, the following message will appear on the screen:

File already exits! Overwrite? (Y/N)

If you choose to overwrite the existing file, its content will be lost.

To return to the main menu, hit any key on the keyboard.

NOTE
There may be slight changes to the Flash BIOS Copy screen compared to those shown here for an Copy ALL BIOS operation. Also, if an error occurs, these will be indicated on the screen.

4.2.4.4 UBIOS – BATCH MODE

While files can be manually selected using the Interactive Mode, Flash BIOS Update or Copy can be achieved through Batch Mode.

The command line format is as follows:

UBIOS /B [operation] [filetype] [filename] [options] where:

/B or /-B specifies that this is a Batch Mode command.

[operation] is the Flash BIOS operation you wish to perform, and can be replaced with one of three letters: U for Update, C for Copy, or V for Verify (used to compare the contents of the Flash BIOS device and the specified BIOS file).

[filetype] is the filetype of the BIOS file to program (with an update operation) or to create (with a copy operation), and can be replaced with one of the following:

ALL	for All BIOS files in a single file with the .BIN extension,
VGA	for VGA BIOS file with the .VGA or .BFP extension,
SCSI	for SCSI BIOS file with the .BIN extension,
LAN	for LAN BIOS file with the .BIN extension.

[filename] is the name of the BIOS file (including the extension) to program (with an update operation) or to create (with a copy operation), and can be replaced with the filename which corresponds to the filetype. For example, if "VGA" was listed as filetype, then the filename could be "FLAT.BFP".

[options] these are optional parameters that may be added:

/C This option will not clear the CMOS Setup when updating main BIOS (AMIBIOS), however this is not recommended since the CMOS Setup should be updated when the main BIOS is changed.

/R Instructs UBIOS to reset the board upon completion of an operation.

/VT For VT100 compatibility.

/? To get a summary of the Batch Mode options from UBIOS. It will display a Batch options summary of valid UBIOS command lines. The same help information will also be displayed each time UBIOS detects an error in the command line.

4.2.5 Automatic CPLD Hardware Upgrade After a BIOS Update

During the first system bootup after you update the Flash BIOS device with the UBIOS utility, the BIOS may need to upgrade the CPLD devices.

This message appears on the screen when the BIOS writes to the devices:

```
A hardware upgrade will be performed on some CPLDs. Follow the instructions
below with special care. Do not disturb the process.

DO NOT RESET OR POWER DOWN THE BOARD!!!

   □□□ Device 1 □□□   0% □□□□□□□□□□□□□□□□□□□□ 100%
   □□□ Device 2 □□□   0% □□□□□□□□□□□□□□□□□□□□ 100%

Status :
         Please wait...
```

The color of the boxes displayed in the message indicates these functions:

Device OK	Green
Device busy	Blue
Device will be updated	Red

If your device upgrade was successful, the following message is displayed under the "Status:" line prior to rebooting:

```
Update complete successfully, wait for the automatic reboot.
Rebooting in 5 second(s).
```

If the update is not successful, the following message appears under the "Status:" line:

```
ERROR: general failure programming CPLDs!

Please contact Teknor Industrial Computers technical support.
```

You must contact Teknor's technical support for further instructions.

> **WARNING**
>
> Whenever the BIOS performs a CPLD hardware upgrade, **disable the watchdog and do not interrupt the system in any way (power down, reset, mouse or keyboard functions). The devices will be damaged and your board rendered inoperational if you disturb the update process!**

4.3 VT100 MODE

The VT100 operating mode allows remote setups of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

4.3.1 Requirements

The terminal should emulate a VT100 or ANSI terminal. Terminal emulation programs such as Telix or Procom can also be used.

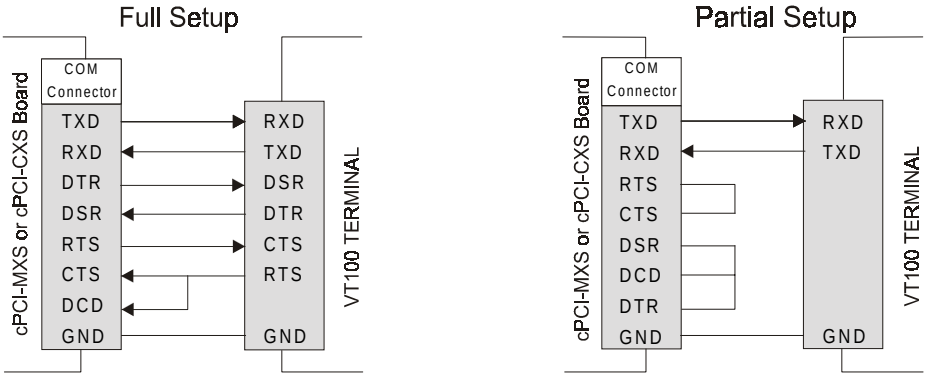
4.3.2 Setup & Configuration

Follow these steps to set up the VT100 mode:

1. Connect a monitor and a keyboard to your board and turn on the power.
2. Enter into the CMOS Setup program in the “BIOS Feature Setup”
3. Select the VT100 mode and the appropriate COM port and save your setup.
4. Connect the communications cable as shown in the next page.

> NOTE
>
> If you do not require a full cable for your terminal, you can set up a partial cable by using only the TXD and RXD lines. To ignore control lines simply loop them back as shown in VT100 Partial Setup cable diagram.

5. Configure your terminal to communicate using the same parameters as in CMOS Setup.
6. Reboot the board.
7. Use the remote keyboard and display to setup the BIOS.
8. Save the setup, exit, and disconnect the remote computer from the board to operate in stand-alone configuration.



4.3.3 Running WIthout a Terminal

The board can boot up without a screen or terminal attached. If the speed is set to Auto and no terminal is connected, the speed is set to 75,200 bauds.

Furthermore, you can run without any console at all by simply not enabling VT100 Mode and by disabling the onboard video function.0

PART 5

APPENDICES

A. BOARD SPECIFICATIONS

B. MEMORY & I/O MAPS

C. INTERRUPT LINES

D. BOARD DIAGRAMS

E. CONNECTOR PINOUTS

F. BIOS SETUP ERROR CODES

G. EMERGENCY PROCEDURE

A. Board Specifications

cPCI-MXS & cPCI-CXS	DESCRIPTION
Overview	CompactPCI System Processor board
Supported Microprocessors	cPCI-MXS Pentium® II Low Power 333MHz or Pentium III Processor – Low Power 500MHz cPCI-CXS Celeron® 300A, 366, 433 and higher in PPGA packages as technology becomes available.
CHIPSET	Intel 440BX AGPset. 21-signal High-Availability controller: Select, Healthy, Reset for 7 CPCI I/O slots.
Bus Interface	Front side bus up to 100MHz CompactPCI bus,32-bit (33MHz) through J1 and J2 (P1 and 92 for MXS) PCI-PCI bridge: DEC 21150; supports up to 7 REQ/GNT for fully loaded CompactPCI® system PCI Mezzanine (PMC) Proprietary Mezzanine with PCI bus, FD and EIDE support SMBus (for power management of CPU temperature monitoring, DRAM control, clock buffers and power control)
Cache Memory	cPCI-MXS : Level 1: 16/16KB instruction/Data CPU-internal Level 1 Level 2: 256KB internal, 64-bit wide, pipelined burst cPCI-CXS : Level 1: 16/16KB instruction/Data CPU-internal Level 1 Level 2: 128KB internal, 64-bit wide, pipelined burst
System Memory	Three 168-pin Latching DIMM sockets, 64/72-bit Up to 768Mb of SDRAM with parity or ECC (for single bit error correction and double bit error detection)
Data Path	64-bit on CPU and video memory; 32-bit on local PCI and CompactPCI
Interrupts	11 edge sensitive and configurable 4 PCI level sensitive, configurable to any interrupt vector for PnP compatibility.
Flash Memory	512KB for BIOS field upgrade; Silicon Serial ID TAG for unique board identification accessible via software.
Video	64-bit AGP video controller (Intel 69000) with 2MB video memory CRT resolutions up to 1024 x 768 x 64K colors or 1280 x 1024 x 256 colors

Board Specifications (continued)

Clock/Calendar	Real-time clock with (replaceable) battery backup, CMOS RAM
Connectors in "Front" configuration	*Front Plate* CRT — 15-pin D-Sub COM1 — 9-pin D-Sub Ethernet 1 and 2 — 2 x RJ-45 with built-in LEDs PS/2 mouse + Keyboard — 6-pin mini-DIN
Interfaces on J3/J4/J5	*Rear CPCI I/O Connectors (J3/J4/J5)* *(Rear-panel transition module, cTM80-STD2S available separately)* CRT, Parallel Port, Speaker I/F, Ethernet (2), SCSI, Fan fail monitoring, Serial Ports (4), SMBus, Reset Switch, PS/2 mouse, EIDE (2), USB (2), I^2C, Infrared, Keyboard, Floppy disk I/F *Onboard Expansions* PCI Mezzanine Card PMC. Proprietary mezzanine. CompactFlash.
I/O	**I/O** — SMC FDC37C672 **USB Ports** — Two **Serial Ports** — Four (three RS-232, COM1, 2, 4; Com3 configurable as RS-422/485) **Parallel Port** — One bi-directional with all IEEE 1284 protocols supported with BIOS selectable IRQs and addressing **Floppy Disk** — Support for two drives (360KB to 1.44MB) **EIDE** — Two channel Bus Master PCI EIDE; support for four IDE Type 4 drives (master/slave configuration); LBA, PIO Mode 0-4 and Ultra DMA/33. **CompactFlash™** — Optional bootable CompactFlash™ disk interfaces to primary EIDE channel, user upgradable, master/slave. **SCSI** — Supports 16-bit Ultra Wide SCSI up to 40MB/s, 8-bit Fast SCSI-2 up to 10MB/s, 8-bit Ultra SCSI up to 20MB/s (Adaptec AIC7880) **Ethernet** — Two 10/100Mb/s Ethernet, PCI 10/100Base-TX ports (Inter 82559 controller) HD / FD Mezzanine Card: Optionally onboard using Teknor's cMC series mezzanine cards. **HD/FD Mezzanine Card** — Optionally onboard using Teknor's cMC series mezzanine cards
Supervisory	Two-stage software programmable Watchdog timer drives NMI on 1st

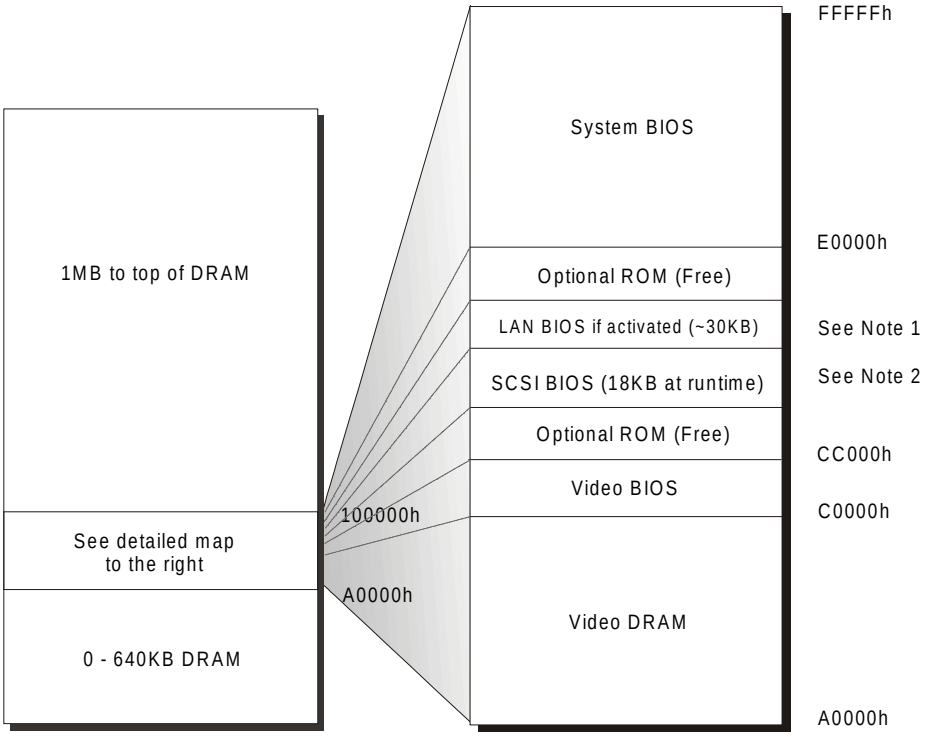
	stage and system reset on 2nd stage. Programmable CPU temperature monitor/alarm Power failure/low battery detector Front Panel LED : IDE activity, SCSI activity, Ethernet and link activity
OS Compatibility	MS-DOS™, Windows® 95/98, Windows®NT, VxWorks™, pSOS™, QNX™, Linux, Novell, and Solaris Mechanical.
BIOS Features	Award Elite BIOS 4.51 in Boot Block Flash with recovery code; save CMOS in Flash option, and boot from LAN capability. Auto configuration, extended setup. CC000-E0000 address blocking; PnP tables. Setup console redirection to serial port *(VT100 mode) with CMOS setup access. Software enable/disable of onboard Ethernet & SCSI; hardware enable/disable of onboard video Diskless, keyboardless and videoless operation extensions. System, video, SCSI, LAN and extension BIOS shadowing. Programmable bus and I/O speeds, and memory wait states Advanced security feature for floppy and HDD; DMI & HDD S.M.A.R.T. support. Advanced Configuration and Power Interface (ACPI 1.0), Advanced Power Management (APM 1.2), advanced thermal management (resume, overheat alarm and auto slow-down), and Green support.
Mechanical	Compliant to IEEE 1101.10, compliant to PICMG2.0 Rev 2.1) 233x160x41 mm / 9.2 x 6.3 x 1.6 in, 6U x 8HP (dual slot) Mechanically 233x160x20.5 mm / 9.2 x 6.3 x 0.8 in;6U x 4HP (single slot) Mechanically
Power Requirements	Supply Voltages : +3.3, ±-5%, +5V ±5%, +12V ±5% Supply Current:***** +3.3V, 2.0 Amps maximum +5V, 3.5 Amps maximum +12V, 0.75 Amps maximum Power Dissipation cPCI-MXS : 40W maximum cPCI-CXS: 53W maximum * cPCI-MXS : Pentium II, Low Power 333MHz with 32MB SDRAM cPCI-CXS : Celeron processor 300MHz with 32MB SDRAM

Board Specifications (continued)

Environmental		Operating	Storage and Transit
	Temperature	0-60°C / 32-140°F	-40 to +70°C / -40 to 158°F
	Humidity	5% to 95% @ 40°C/104°F non-condensing	5% to95% @ 40°C/104°F non-condensing
	Altitude	4,572m / 15,000 ft	15,240m / 50,000ft
	Shock	Designed to meet IEC 68-2-27	
	Vibration	Designed to meet IEC 68-2-6	
	Reliability	MTBF: cPCI-MXS : 32,000 hours @ 55°C/131°F (MIL-HDBK-217F) cPCI-CXS : 95,000 hours without fan, >32,000 hours with fan @ 55°C/131°F (MIL-HDBK-217F) Board serial number in EEPROM USB, keyboard and mouse protected by self-resetting fuse 2 year limited warranty Designed to meet or exceed : Safety: UL1950, CSA C22.2 No 950, EN 60950, IEC950 EMI/EMC FCC 47 CFR Part 15/CISPR22, Class B, CE Mark to EN55022/EN50082	

B. MEMORY & I/O MAPS

B.1 MEMORY MAPPING



Note 1 : LAN BIOS address may vary

Note 2 : SCSI BIOS address may vary.
Size is only 2KB if no device.

Address	Function
00000-9FFFF	0-640 KB DRAM
A0000-BFFFF	Video DRAM
C0000-CBFFF	Video BIOS
CC000-FFFFF	Optional ROM (Free)
	LAN BIOS around 30KB if activated, address may vary
	SCSI BIOS 18KB at runtime, 2KB if no device, address may vary
E0000-FFFFF	System BIOS
100000-Top of DRAM	1 MB - Top of DRAM

B.2 I/O MAPPING

Address	Optional Address	Optional Address	Optional Address	Function
000-01F				DMA Controller 1
020-03F				Interrupt Controller 1
040-05F				Timer
060-06F				Keyboard
070-07F				Real-time clock
080-09F				DMA Page Register
0A0-0BF				Interrupt Controller 2
0C0-0DF				DMA Controller 2
0F0-0F1, 0F8-0FF				Math Coprocessor
190-197	290-297	390-397		Teknor Control Port
1F0-1F7, 3F6				Primary IDE
170-177, 376				Secondary IDE
3F0-3F7	370-377			Floppy Disk
378-37A	3BC-3BE	278-27A		Parallel Port (LPT1 by default)
3F8-3FF (COM1)	2F8-2FF (COM2)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 2 (COM2 by default)
3C0-3CF, 3D0-3DF, 3B0-3BB				Graphics Controller (I2C Port)

C. Interrupt Lines

C.1 IRQ LINES

The board is fully PC compatible with interrupt steering for PCI plug and play compatibility.

Controller # 1		Controller # 2	
IRQ 0	Timer Output 0	IRQ 8	Real-Time Clock
IRQ 1	Keyboard (Output Buffer Full)	IRQ 9	Available [1]
IRQ 2	Cascade Controller # 2	IRQ 10	Available [1]
IRQ 3*	Serial Port 2	IRQ 11	Available [1]
IRQ 4*	Serial Port 1	IRQ 12	PS/2 Mouse
IRQ 5*	Parallel Port 2 or Available [1]	IRQ 13	Coprocessor Error
IRQ *6	Floppy Controller	IRQ 14	Primary IDE * or available [1]
IRQ 7*	Parallel Port 1 or Available [1]	IRQ 15	Secondary IDE * or available [1]

* :All functions marked with an asterisk (*) can be disabled or reconfigured.
1 Available lines service on board and external PCI/ISA PnP devices or a Legacy ISA device.

C.2 DMA CHANNELS

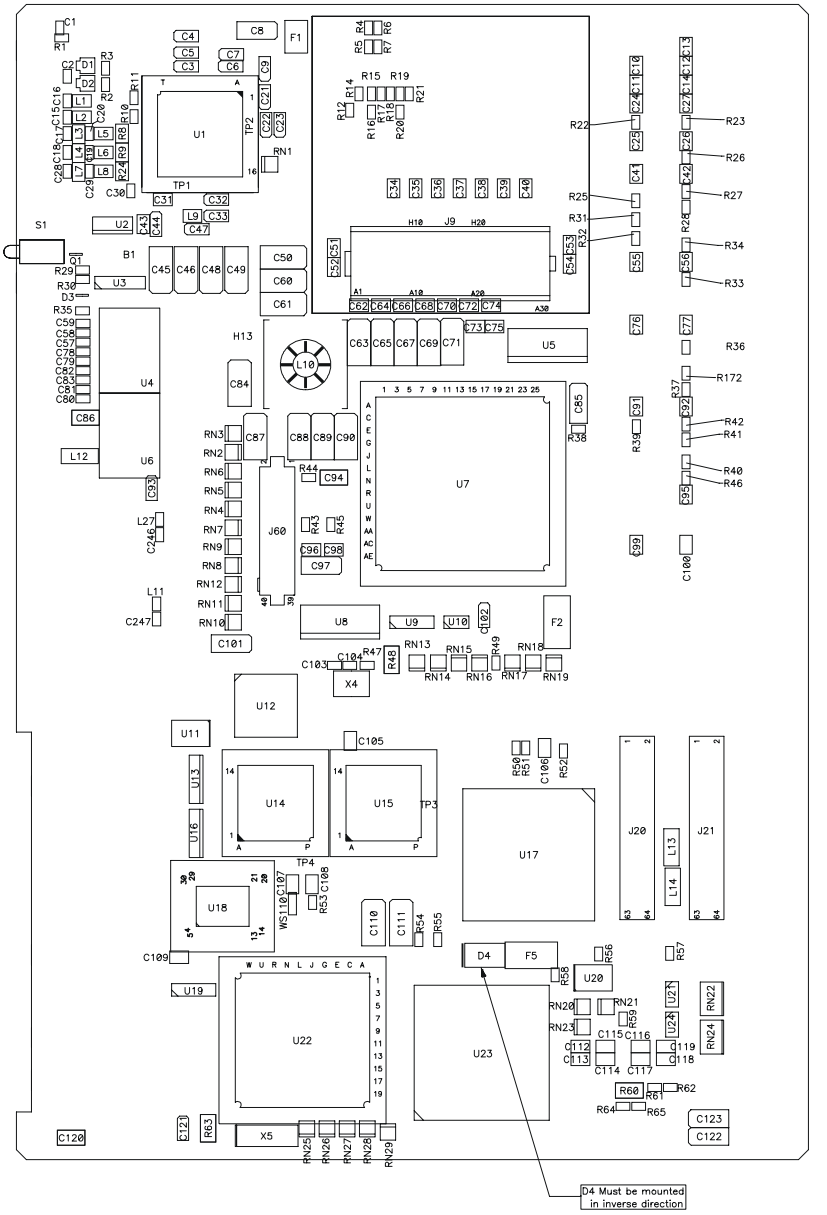
The cPCI-MXS and cPCI-CXS integrate the functionality of two 8237 DMA controllers. Eight DMA channels are available.

According to Plug and Play standards, the system BIOS automatically allocates DMA Channel 1 or 3 for the parallel port's ECP mode. Channel 2 is reserved for the floppy controller and Channel 4 is used to cascade Channels 0 through 7 to the microprocessor.

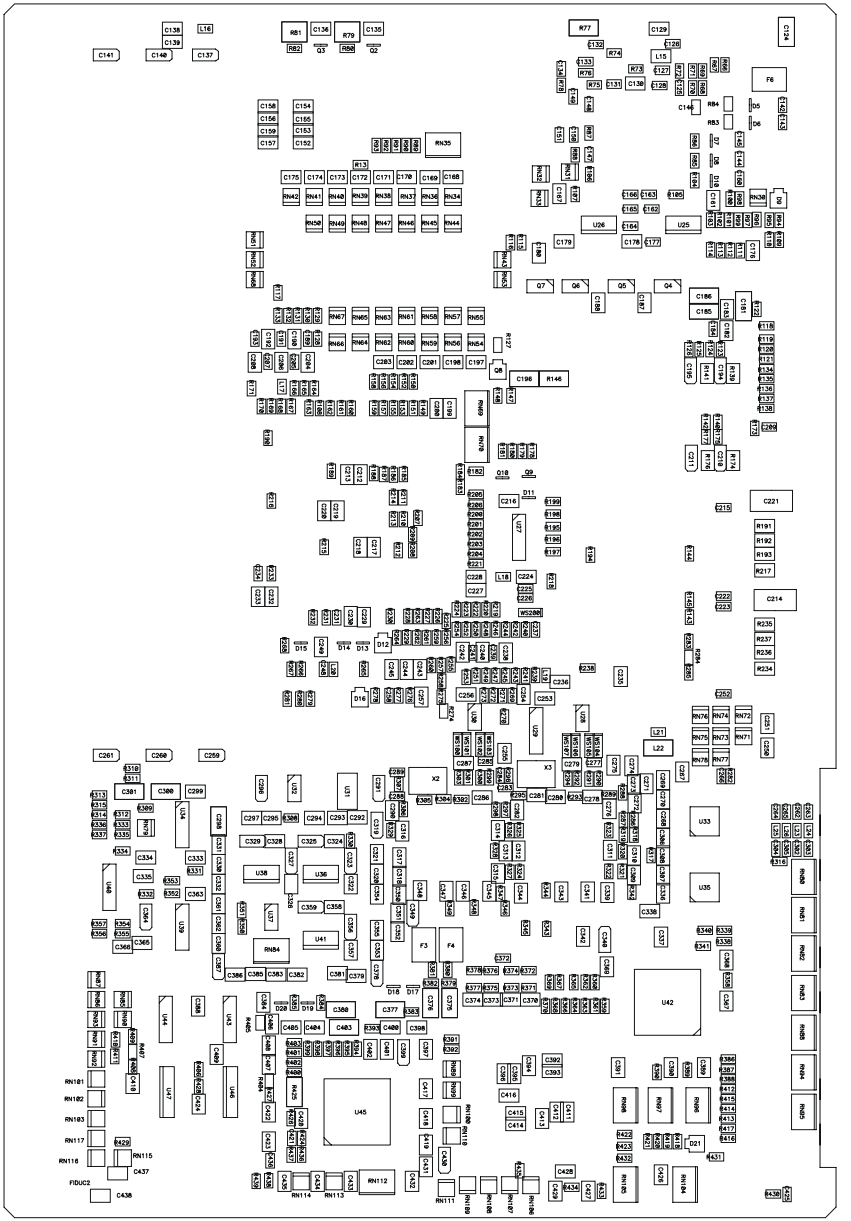
DMA Channel	Function
DMA 0	Available
DMA 1	PnP available (ECP)
DMA 2	Floppy controller
DMA 3	PnP available (ECP)
DMA 4	Cascade controller # 1
DMA 5	PnP available
DMA 6	PnP available
DMA 7	PnP available

D. BOARD DIAGRAMS

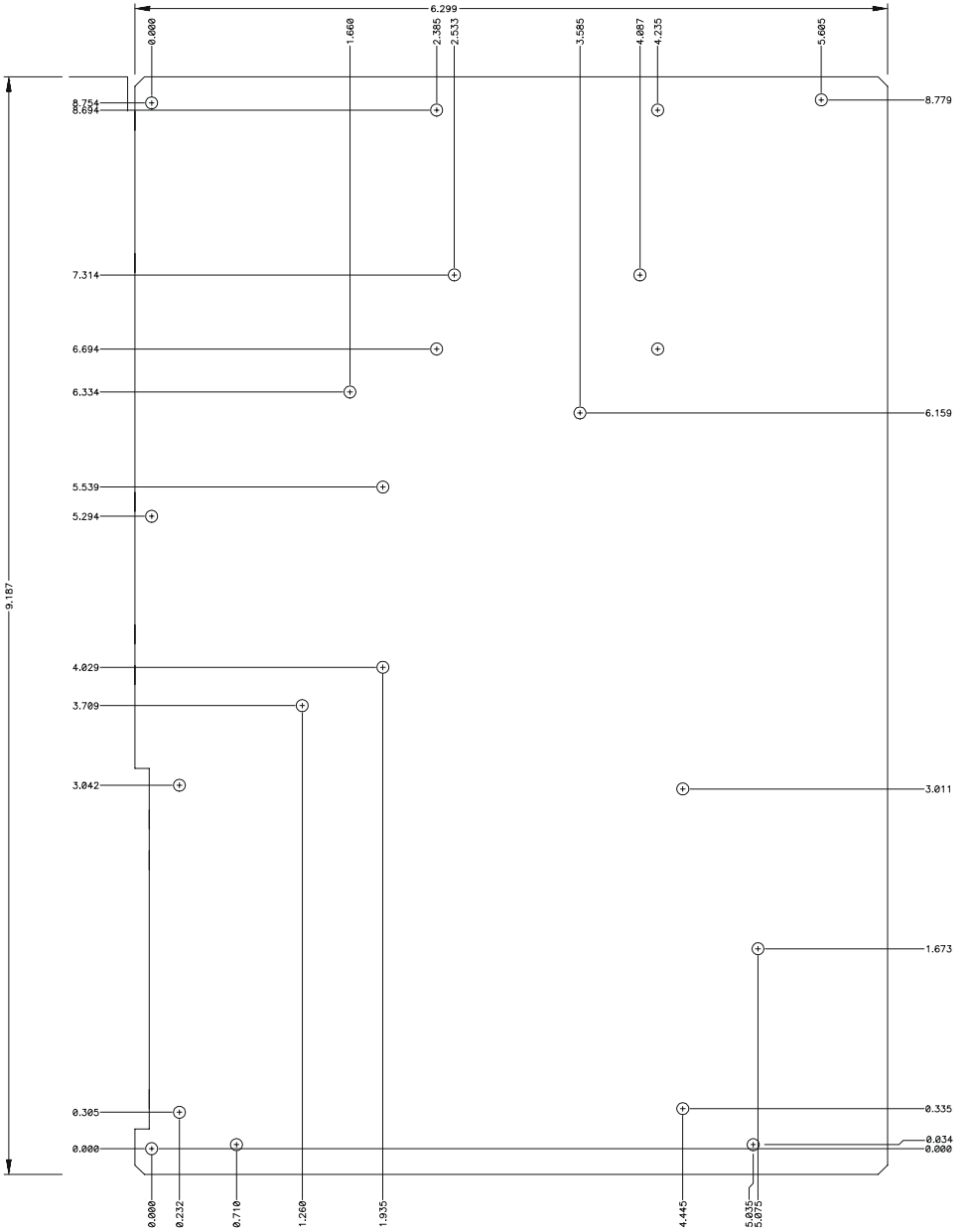
D.1 ASSEMBLY TOP DIAGRAM - CPCI-MXS



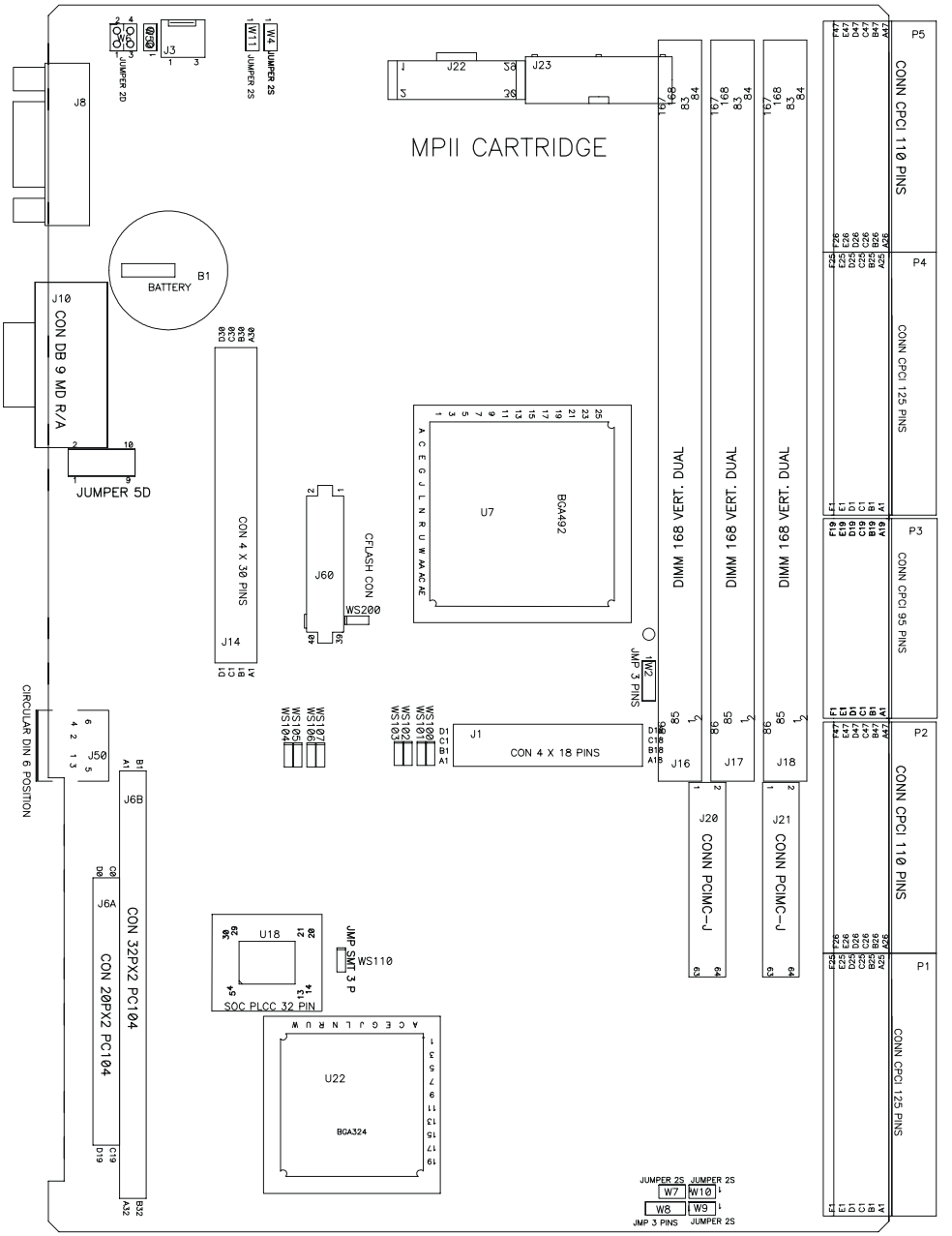
D.2 ASSEMBLY BOTTOM DIAGRAM - CPCI-MXS



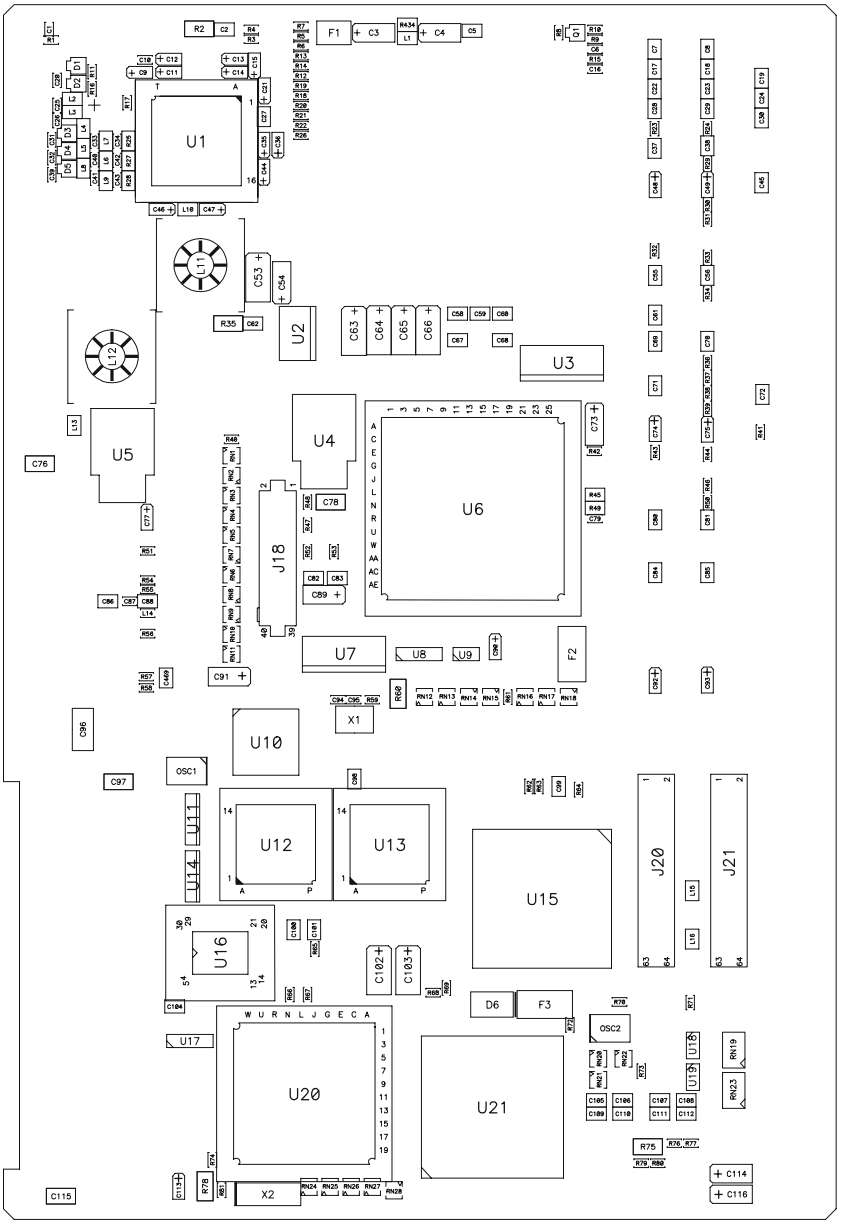
D.3 MOUNTING HOLES - cPCI-MXS



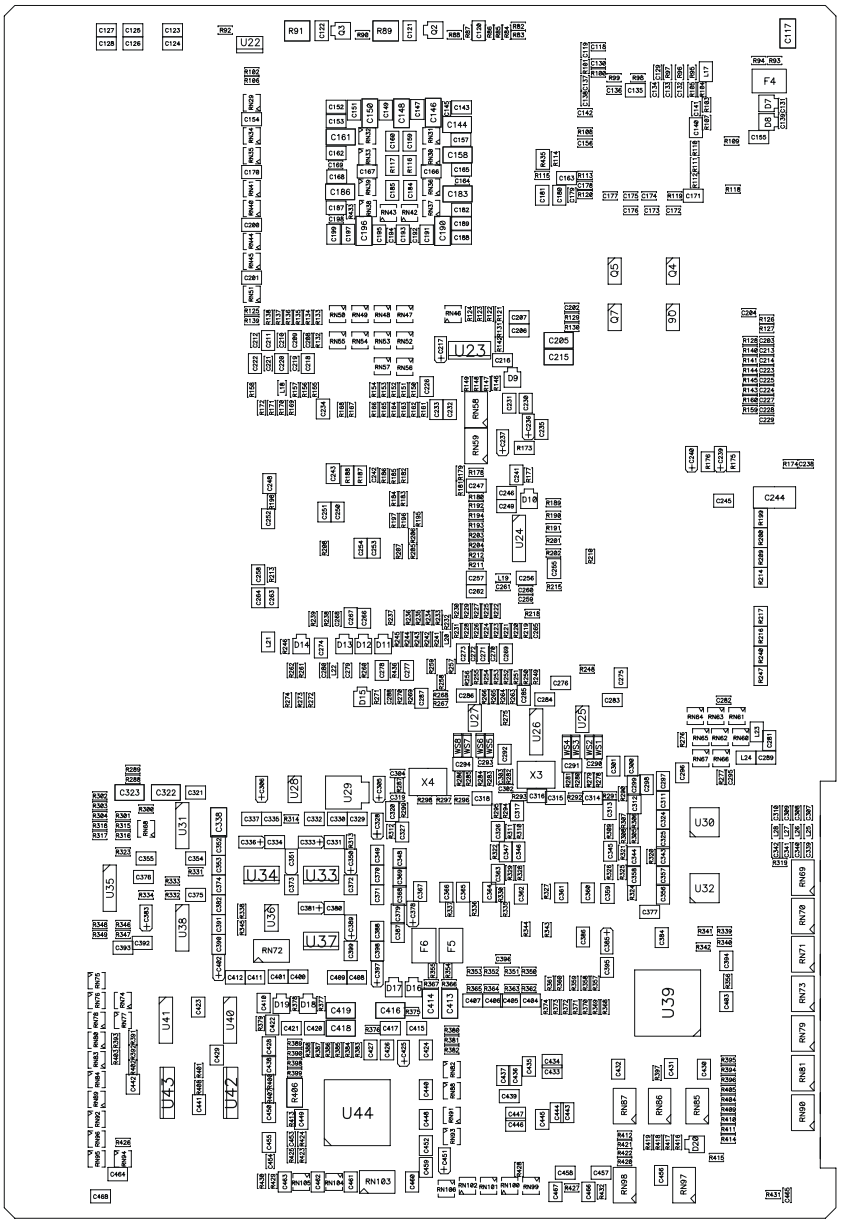
D.4 CONNECTOR C.S. - CPCI-MXS



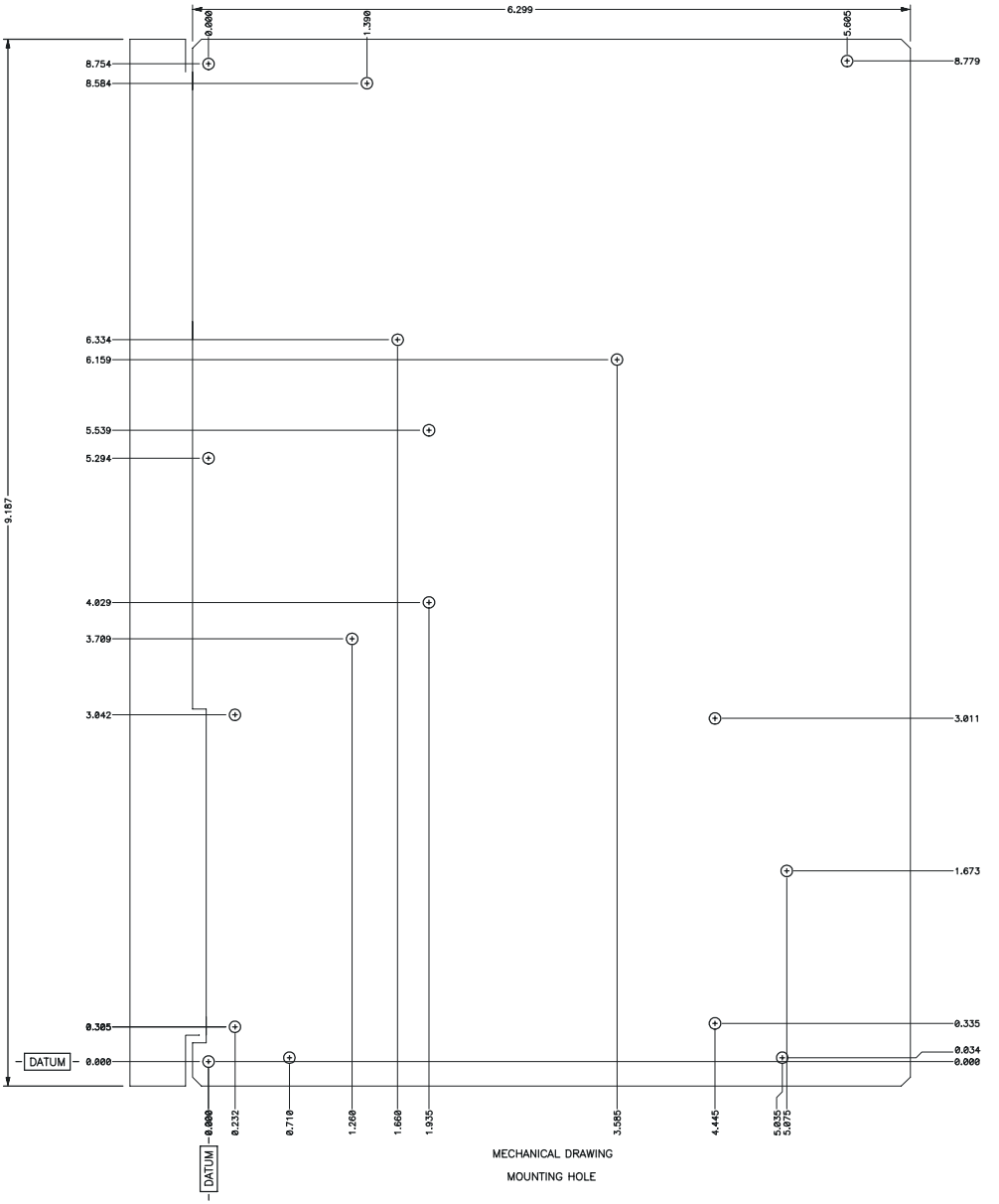
D.5 ASSEMBLY TOP DIAGRAM - CPCI-CXS



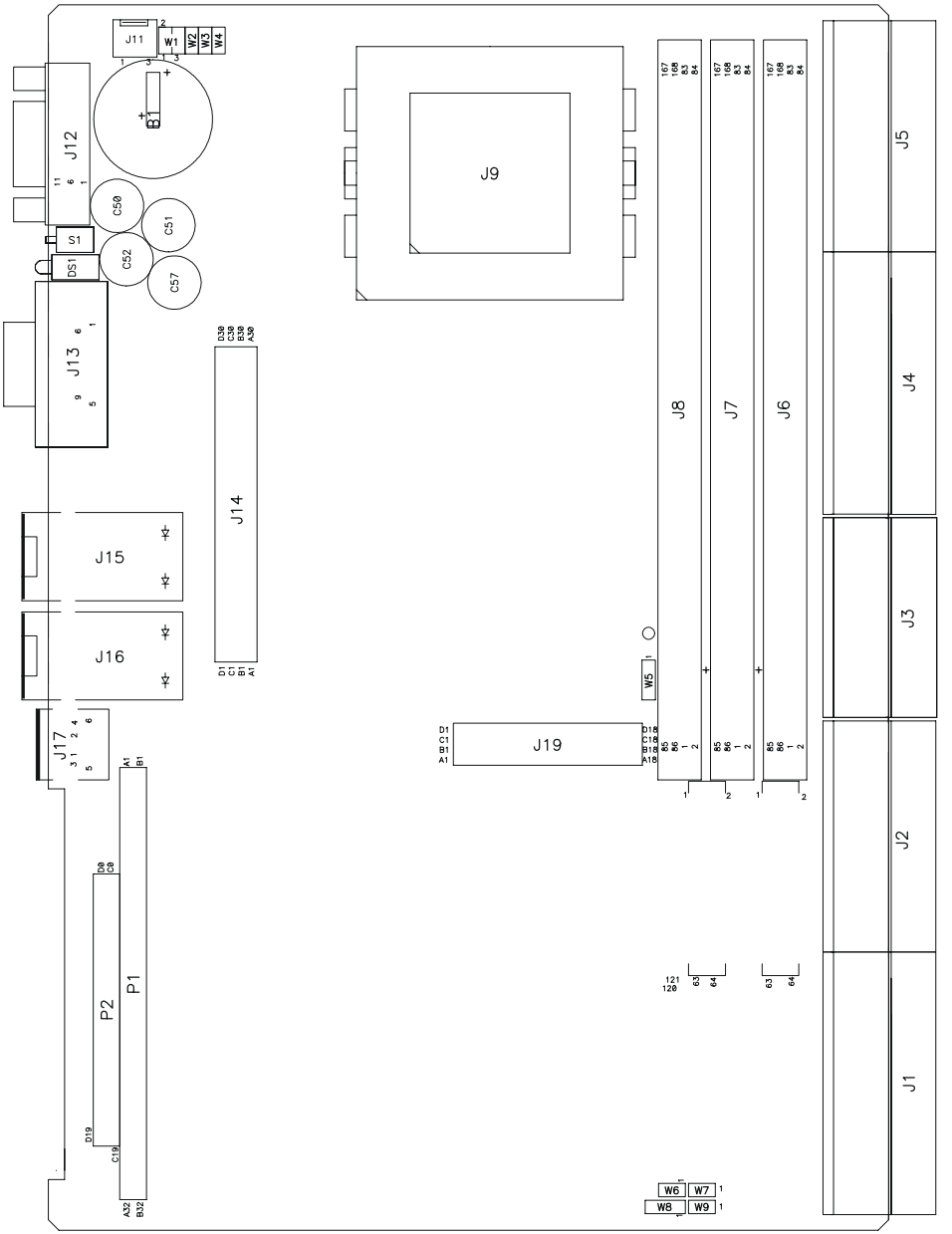
D.6 ASSEMBLY BOTTOM DIAGRAM - CPCI-CXS



D.7 MOUNTING HOLES - cPCI-CXS



D.8 CONNECTOR C.S. - cPCI-CXS



E. Connector Pinouts

E.1 cPCI-MXS and cPCI-CXS Connectors and Headers

MXS	CXS	Connector J14
P1	J1	CPCI Bus Connector
P2	J2	CPCI Bus Connector
P3	J3	CPCI I/O Connector
P4	J4	CPCI I/O Connector
P5	J5	CPCI I/O Connector
J1	J19	Mezzanine Storage Connector
J3	J11	Fan Header
J4	J15	Ethernet 1 Connector (Front panel configuration only)
J5	J16	Ethernet 2 Connector (Front panel configuration only)
J8	J12	CRT VGA Connector (Front panel configuration only)
J10	J13	Serial Port 1 – RS-232 (Front panel configuration only)
J14	J14	Mezzanine PCI Connector
J21	J20	PCI Mezzanine Card (PMC)
J50	J17	Keyboard/Mouse Connector
J60	J18	CompactFLASH Disk Connector
B1	B1	CMOS Battery Backup connector

NOTE P1-P5 correspond to PICMG's definition of J1-J5

E.2 P1/P2 (MXS) J1/J2 (CXS) cPCI BUS CONNECTORS

	ROW "A"			ROW "B"			ROW "C"		
	#	Ref.	SIGNAL	#	Ref.	SIGNAL	#	Ref.	SIGNAL
	1	A1	+5V	1	B1	-12V	1	C1	/TRST
	2	A2	TCK	2	B2	+5V	2	C2	TMS
	3	A3	/INTA	3	B3	/INTB	3	C3	/INTC
	4	A4	N.C.	4	B4	GND	4	C4	VI/O
	5	A5	N.C.	5	B5	N.C.	5	C5	/RST
	6	A6	/REQ0	6	B6	GND	6	C6	+3.3V
	7	A7	AD30	7	B7	AD29	7	C7	AD28
	8	A8	AD26	8	B8	GND	8	C8	VI/O
	9	A9	/CBE3	9	B9	N.C.	9	C9	AD23
	10	A10	AD21	10	B10	GND	10	C10	+3.3V
	11	A11	AD18	11	B11	AD17	11	C11	AD16
J1	15	A15	+3.3V	15	B15	/FRAME	15	C15	/IRDY
	16	A16	/DEVSEL	16	B16	GND	16	C16	VI/O
	17	A17	+3.3V	17	B17	SDONE	17	C17	/SBO
	18	A18	/SERR	18	B18	GND	18	C18	+3.3V
	19	A19	+3.3V	19	B19	AD15	19	C19	AD14
	20	A20	AD12	20	B20	GND	20	C20	VI/O
	21	A21	+3.3V	21	B21	AD9	21	C21	AD8
	22	A22	AD7	22	B22	GND	22	C22	+3.3V
	23	A23	+3.3V	23	B23	AD4	23	C23	AD3
	24	A24	AD1	24	B24	+5V	24	C24	VI/O
	25	A25	+5V	25	B25	/REQ64	25	C25	/PME
--------	----	-----	----------	----	-----	----------	----	-----	----------
	26	A1	CLK1	26	B1	GND	26	C1	/REQ1
	27	A2	CLK2	27	B2	CLK3	27	C2	/SYSEN
	28	A3	CLK4	28	B3	GND	28	C3	/GNT3
	29	A4	VI/O	29	B4	N.C.	29	C4	N.C.
	30	A5	N.C.	30	B5	GND	30	C5	VI/O
	31	A6	N.C.	31	B6	N.C.	31	C6	N.C.
	32	A7	N.C.	32	B7	GND	32	C7	VI/O
	33	A8	N.C.	33	B8	N.C.	33	C8	N.C.
	34	A9	N.C.	34	B9	GND	34	C9	VI/O
	35	A10	N.C.	35	B10	N.C.	35	C10	N.C.
J2	36	A11	N.C.	36	B11	GND	36	C11	VI/O
	37	A12	N.C.	37	B12	N.C.	37	C12	N.C.
	38	A13	N.C.	38	B13	GND	38	C13	VI/O
	39	A14	N.C.	39	B14	N.C.	39	C14	N.C.
	40	A15	N.C.	40	B15	GND	40	C15	/FAL
	41	A16	N.C.	41	B16	N.C.	41	C16	/DEG
	42	A17	N.C.	42	B17	GND	42	C17	/PRST
	43	A18	N.C.	43	B18	N.C.	43	C18	N.C.
	44	A19	N.C.	44	B19	GND	44	C19	N.C.
	45	A20	CLK5	45	B20	GND	45	C20	N.C.
	46	A21	CLK6	46	B21	GND	46	C21	N.C.
	47	A22	N.C.	47	B22	N.C.	47	C22	N.C.

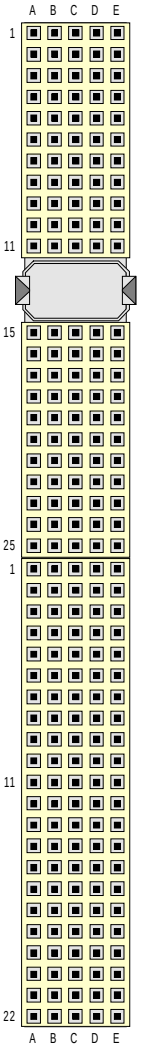
NOTE P1-P2 correspond to PICMG's definition of J1-J2

P1/P2 (MXS), J1/J2 (CXS) – CPCI Bus Connectors (continued)

	ROW "D"			ROW "E"		
	#	Ref.	SIGNAL	#	Ref.	SIGNAL
	1	D1	+12V	1	E1	+5V
	2	D2	TDO	2	E2	TDI
	3	D3	+5V	3	E3	/INTD
	4	D4	IRQ14	4	E4	IRQ15
	5	D5	GND	5	E5	/GNT0
	6	D6	CLK0	6	E6	AD31
	7	D7	GND	7	E7	AD27
	8	D8	AD25	8	E8	AD24
	9	D9	GND	9	E9	AD22
	10	D10	AD20	10	E10	AD19
	11	D11	GND	11	E11	/C/BE2
J1	15	D15	GND	15	E15	/TRDY
	16	D16	/STOP	16	E16	/LOCK
	17	D17	GND	17	E17	/PERR
	18	D18	PAR	18	E18	/CBE1
	19	D19	GND	19	E19	AD13
	20	D20	AD11	20	E20	AD10
	21	D21	N.C.	21	E21	/CBE0
	22	D22	AD6	22	E22	AD5
	23	D23	+5V	23	E23	AD2
	24	D24	AD0	24	E24	AD0
	25	D25	+3.3V	25	E25	+5V
---	---	---	---	---	---	---
	26	D1	/GNT1	26	E1	/REQ2
	27	D2	/GNT2	27	E2	/REQ3
	28	D3	/REQ4	28	E3	/GNT4
	29	D4	GND	29	E4	N.C.
	30	D5	N.C.	30	E5	N.C.
	31	D6	GND	31	E6	N.C.
	32	D7	N.C.	32	E7	N.C.
	33	D8	GND	33	E8	N.C.
	34	D9	N.C.	34	E9	N.C.
	35	D10	GND	35	E10	N.C.
J2	36	D11	N.C.	36	E11	N.C.
	37	D12	GND	37	E12	N.C.
	38	D13	N.C.	38	E13	N.C.
	39	D14	GND	39	E14	N.C.
	40	D15	/REQ5	40	E15	/GNT5
	41	D16	GND	41	E16	N.C.
	42	D17	/REQ6	42	E17	/GNT6
	43	D18	GND	43	E18	N.C.
	44	D19	N.C.	44	E19	N.C.
	45	D20	GND	45	E20	N.C.
	46	D21	N.C.	46	E21	N.C.
	47	D22	N.C.	47	E22	N.C.

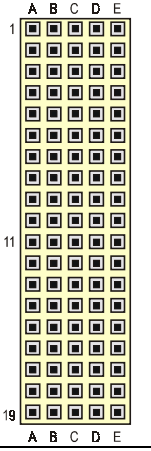
PINOUT

(Top View)



E.3 P3 (MXS), J3 (CXS) – CPCI I/O CONNECTORS

	ROW "A"			ROW "B"			ROW "C"		
	#	Ref.	SIGNAL	#	Ref.	SIGNAL	#	Ref.	SIGNAL
J3	1	A1	VP-OUT	1	B1	ZVPCLK	1	C1	VP-IN
	2	A2	GND	2	B2	VSCL2	2	C2	GND
	3	A3	VP5	3	B3	+5V	3	C3	VP6
	4	A4	VSDA2	4	B4	VP3	4	C4	/VP-HSYNC
	5	A5	VP0	5	B5	GND	5	C5	VP1
	6	A6	SPEEPLED0	6	B6	LINKLED-0	6	C6	ACTLED0
	7	A7	ACTLED1	7	B7	SD7	7	C7	SD6
	8	A8	GND	8	B8	+5V	8	C8	+5V
	9	A9	ETX+1	9	B9	ETX-1	9	C9	ERX+1
	10	A10	GND	10	B10	/WR 80	10	C10	SD1
	11	A11	/DCD4	11	B11	GND	11	C11	RXD4
	12	A12	/RTS4	12	B12	/CTS4	12	C12	/RI4
	13	A13	/JCD3	13	B13	+5V	13	C13	RXD3
	14	A14	/RTS3	14	B14	/CTS3	14	C14	/RI3
	15	A15	/S2BDSEL	15	B15	/S3BDSEL.	15	C15	S3PCIRST
	16	A16	/S2HEALTHY	16	B16	/S3HEALTHY	16	C16	N.C.
	17	A17	/S2PCIRST	17	B17	IRQ11	17	C17	IRQ9
	18	A18	IRQ7	18	B18	/S-IDE-ACT	18	C18	/HD_ACT
	19	A19	/PWRBT	19	B19	EXT-SMI	19	C19	PX4-NMI

	ROW "D"			ROW "E"			PINOUT (Top View)
	#	Ref.	SIGNAL	#	Ref.	SIGNAL	
J3	1	D1	VACTI	1	E1	GND	
	2	D2	VP-VSYNC	2	E2	GND	
	3	D3	GND	3	E3	VP7	
	4	D4	VP4	4	E4	/EN-CAM	
	5	D5	GND	5	E5	VP2	
	6	D6	LINKLED-1	6	E6	SPEEDLED-1	
	7	D7	SD5	7	E7	Reserved	
	8	D8	SD3	8	E8	Reserved	
	9	D9	ERX-1	9	E9	GND	
	10	D10	+12V	10	E10	Reserved	
	11	D11	/DSR4	11	E11	TXD4	
	12	D12	+5V	12	E12	/DTR4	
	13	D13	/DSR3	13	E13	TXD3	
	14	D14	GND	14	E14	/DTR3	
	15	D15	SD0	15	E15	S4BDSEL	
	16	D16	N.C.	16	E16	N.C.	
	17	D17	/S4HEALTHY	17	E17	/S4PCIRST	
	18	D18	IRRX-2	18	E18	IRTX-2	
	19	D19	/S5BDSEL	19	E19	PWROK-33	

J3

NOTE P3 correspond to PICMG's definition of J3

E.4 P4/P5 (MXS), J4/J4 (CXS) - CPCI I/O CONNECTORS

	ROW "A"			ROW "B"			ROW "C"		
	#	Ref.	SIGNAL	#	Ref.	SIGNAL	#	Ref.	SIGNAL
	1	A1	I2C-CLK	1	B1	I2C-DATA	1	C1	LID
	2	A2	SM-BYPASS	2	B2	/CD11	2	C2	/CD10
	3	A3	/SIO	3	B3	/SREQ	3	C3	/SCD
	4	A4	/SRST	4	B4	/SACK	4	C4	/SBSY
	5	A5	GND	5	B5	/WIDEPS	5	C5	TERMPWR
	6	A6	GND	6	B6	/SDPL	6	C6	/SCD7
	7	A7	/SCD4	7	B7	/SCD3	7	C7	/SCD2
	8	A8	/SDPH	8	B8	/SCD15	8	C8	/SCD14
	9	A9	GND	9	B9	GND	9	C9	S5HEALTHY
	10	A10	VSCL	10	B10	HSYNC	10	C10	VSYNC
	11	A11	BLUE	11	B11	GND	11	C11	S6BDSEL
J4	15	A15	GND	15	B15	+5V	15	C15	+5V
	16	A16	TX+0	16	B16	TX-0	16	C16	ERX+0
	17	A17	/BRSTDRV	17	B17	GND	17	C17	SDD7
	18	A18	SDD9	18	B18	SDD5	18	C18	SDD10
	19	A19	SDD3	19	B19	SDD12	19	C19	SDD2
	20	A20	SDD14	20	B20	SDD0	20	C20	SDD15
	21	A21	SDREQ	21	B21	GND	21	C21	/SDIOW
	22	A22	GND	22	B22	SIORDY	22	C22	S7HEALTHY
	23	A23	/SIOCS16	23	B23	SDA1	23	C23	GND
	24	A24	/SCS1	24	B24	/SCS3	24	C24	SEC-PD1
	25	A25	S7PCIRST	25	B25	S8BDSEL	25	C25	S8HEALTHY
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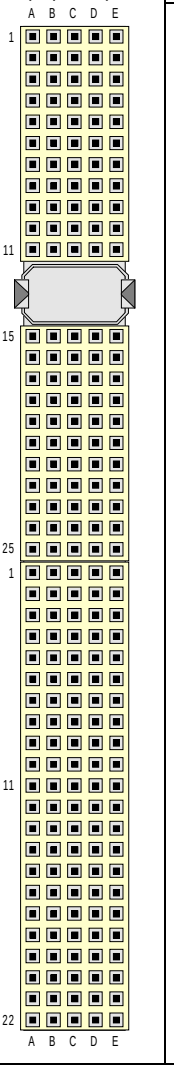
	26	A1	/BRSTDRV	26	B1	/BRSTDRV	26	C1	PDD7
	27	A2	PDD9	27	B2	PDD5	27	C2	PDD10
	28	A3	PDD3	28	B3	PDD12	28	C3	PDD2
	29	A4	PDD14	29	B4	PDD0	29	C4	GND
	30	A5	PDREQ	30	B5	PIORDY	30	C5	/PDIOW
	31	A6	/IO16	31	B6	GND	31	C6	/PDIAG
	32	A7	PCS1	32	B7	/PCS3	32	C7	PDA1
	33	A8	/FD-DRVEN1	33	B8	/FD-INDEX	33	C8	/FD-MTR0
	34	A9	/FD-MTR1	34	B9	/FD-DIR	34	C9	/FD-STEP
	35	A10	/FD-TRK1	35	B10	/FD-WRTPRT	35	C10	/FD-RDATA
J5	36	A11	/DCD2	36	B11	GND	36	C11	RXD2
	37	A12	/RTS2	37	B12	/CTS2	37	C12	/RI2
	38	A13	/DCD1	38	B13	+5V	38	C13	RXD1
	39	A14	/RTS1	39	B14	/CTS1	39	C14	/RI1
	40	A15	SLCT	40	B15	PE	40	C15	BUSY
	41	A16	PD6	41	B16	PD5	41	C16	PD4
	42	A17	PD2	42	B17	/INIT	42	C17	PD1
	43	A18	ALF	43	B18	USBD1+	43	C18	USBD1-
	44	A19	/STB	44	B19	GND	44	C19	USBV1
	45	A20	+5V	45	B20	/SMBDATA	45	C20	/SMBALERT
	46	A21	KDATA	46	B21	KCLK	46	C21	VCC-KBD
	47	A22	/PRST	47	B22	GND	47	C22	/DIAG-OC

NOTE P4-P5 correspond to PICMG's definition of J4-J5

E.5 P4/P5 (MXS), J4/J5 (CXS) (CONTINUED)

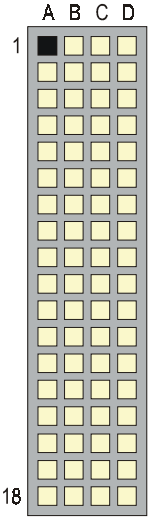
	ROW "D"			ROW "E"			PINOUT
	#	Ref.	SIGNAL	#	Ref.	SIGNAL	(Top View)
	1	D1	/EXT-FAN0-FAIL	1	E1	/EXT-FAN1-FAIL	
	2	D2	SD9	2	E2	/SCD8	
	3	D3	/SSEL	3	E3	/SMSG	
	4	D4	GND	4	E4	/SATN	
	5	D5	TERMPWR	5	E5	GND	
	6	D6	/SDC6	6	E6	/SCD5	
	7	D7	/SCD1	7	E7	/SCD0	
	8	D8	/SCD13	8	E8	/SCD12	
	9	D9	VSDA	9	E9	S5PCIRST	
	10	D10	RED	10	E10	GREEN	
	11	D11	GND	11	E11	GND	
J4	15	D15	S6HEALTHY	15	E15	/S6PCIRST	J4
	16	D16	ERX-0	16	E16	GND	
	17	D17	SDD8	17	E17	SDD6	
	18	D18	SDD4	18	E18	SDD11	
	19	D19	SDD13	19	E19	SDD1	
	20	D20	GND	20	E20	S7BDSEL	
	21	D21	GND	21	E21	/SDIOR	
	22	D22	/SDDACK	22	E22	IRQ15	
	23	D23	SDA0	23	E23	SDA2	
	24	D24	GND	24	E24	/FAL1	
	25	D25	S8PCIRST	25	E25	+5V	
--------	-----	-----	----------	-----	-----	----------	--------
	26	D1	PDD8	26	E1	PDD6	
	27	D2	PDD4	27	E2	PDD11	
	28	D3	PDD13	28	E3	PDD1	
	29	D4	PDD15	29	E4	IRQ14	
	30	D5	/PDDACK	30	E5	/PDIOR	
	31	D6	PDA0	31	E6	PDA2	
	32	D7	PRI-PD1	32	E7	/FD-DRVEN0	
	33	D8	/FD-DS1	33	E8	/FD-DS0	
	34	D9	/FD-WDATA	34	E9	/FD-WGATE	
	35	D10	/FD-HDSEL	35	E10	/FD-DSKCHG	
J5	36	D11	/DSR2	36	E11	TXD2	J5
	37	D12	+5V	37	E12	/DTR2	
	38	D13	/DSR1	38	E13	TXD1	
	39	D14	GND	39	E14	/DTR1	
	40	D15	/ACK	40	E15	PD7	
	41	D16	PD3	41	E16	/SLCTIN	
	42	D17	/ERR	42	E17	PD0	
	43	D18	GND	43	E18	USBV0	
	44	D19	USBD0+	44	E19	USBD0-	
	45	D20	GND	45	E20	SMBCLK	
	46	D21	MDATA	46	E21	MCLK	
	47	D22	+5V	47	E22	SPK-OUT	



E.6 J1(MXS) J19 (CXS) – MEZZANINE STORAGE CONNECTOR

	A	B	C	D	
1	VCC	VCC	VCC	VCC	1
2	VCC	VCC	VCC	PDD0	2
3	MCLK	MDATA	PDD1	PDD2	3
4	KBDAT	KBCLK	PDD3	PDD4	4
5	VCC-KBDF	GND	PDD5	PDD6	5
6	GND	GND	PDD7	PDD8	6
7	GND	GND	PDD9	PDD10	7
8	GND	GND	PDD11	PDD12	8
9	GND	GND	PDD13	PDD14	9
10	FD-DS1#	FD-DRVEN0#	PDD15	BRSTDRV#	10
11	FD-DRVEN1#	FD-MTR1#	PDIOW#	PDREQ	11
12	FD-INDEX#	FD-DS0#	PIORDY0	PDIOR#	12
13	FD-DSKCHG#	FDET	IRQ14	PDDACK#	13
14	FD-MTR0#	FD-DIR#	PDA0	PDA1	14
15	FD-STEP#	FD-WDATA#	PDA2	GND	15
16	FD-GATE#	FD-TRK0#	HD-ACT#	PCS1#	16
17	FD-WRTPTR#	FD-RDATA#	PCS3#	PDIAG#	17
18	FD-HSEL#	+12V	IOCS16#	+12V	18

Top View

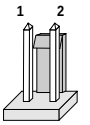


Active Low Signal

E.7 J3 (MXS) J11(CXS) – FAN

Pin #	Signal
1	+12V DC
2	GND

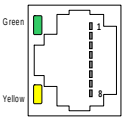
Front View



E.8 J4/J5 (MXS), J15/J16 (CXS) ETHERNET 1 AND 2 CONNECTOR

Signal	
TX+	1
TX-	2
RX+	3
Not Connected	4
Not Connected	5
RX-	6
Not Connected	7
Not Connected	8

Top View



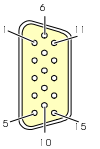
E.9 J8 (MXS), J12 (CXS) - CRT VGA CONNECTORS

Signal	
RED	1
GREEN	2
BLUE	3
Not Connected	4
GND	5

Signal	
Analog GND	6
Analog GND	7
Analog GND	8
Not Connected	9
GND	10

Signal	
Not Connected	11
Not Connected	12
HSYNC	13
VSYNC	14
Not Connected	15

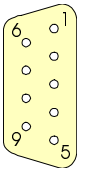
Top View



E.10 J10 (MXS), J13 (CXS) – SERIAL PORT 1 - RS-232

Pin Number	Signal Flow	Signal
DSR 1	I	6
RTS1	O	7
CTS 1	I	8
RI 1	-	9

Top View

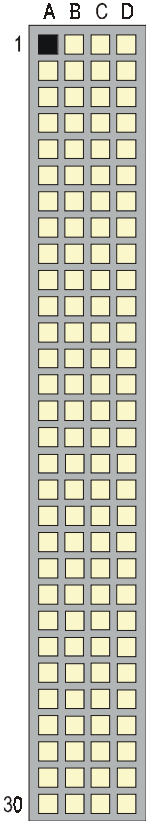


Pin Number	Signal Flow	Signal
1	I	DCD 1
2	I	RXD 1
3	I	TXD 1
4	O	DTR 1
5	O	GND 1

E.11 J14 (MXS AND CXS) – MEZZANINE PCI CONNECTOR

	A	B	C	D	
1	5V_KEY	Reserved	+5V	AD00	1
2	VI/O (5V)	AD02	AD01	+5V	2
3	AD05	GND	AD04	AD03	3
4	C/BE0#	AD07	GND	AD06	4
5	GND	AD09	AD08	GND	5
6	AD11	VI/O (5V)	AD10	MM66EN	6
7	AD14	AD13	GND	AD12	7
8	+3.3V	C/BE1#	AD15	+3.3V	8
9	SERR#	GND	SB0#	PAR	9
10	GND	PERR#	+3.3V	SDONE	10
11	STOP#	+3.3V	LOCK#	GND	11
12	+3.3V	TRDY#	GND	DEVSEL#	12
13	FRAME#	GND	IRDY#	+3.3V	13
14	GND	AD16	+3.3V	C/BE2#	14
15	AD18	+3.3V	AD17	GND	15
16	AD21	AD20	GND	AD19	16
17	+3.3V	AD23	AD22	+3.3V	17
18	IDSEL0	GND	IDSEL1	IDSEL2	18
19	AD24	C/BE3#	VI/O (5V)	IDSEL3	19
20	GND	AD26	AD25	GND	20
21	AD29	+5V	AD28	AD27	21
22	+5V	AD30	GND	AD31	22
23	REQ0#	GND	REQ1#	VI/O (5V)	23
24	GND	REQ2#	+5V	GNT0#	24
25	GNT1#	VI/O (3V)	GNT2#	GND	25
26	+5V	CLK0	GND	CLK1	26
27	CLK	+5V	CLK3	GND	27
28	GND	INTD#	+5V	RST#	28
29	+12V	INTA#	INTB#	INTC#	29
30	-12V	Reserved	Reserved	3.3V_KEY	30

Top View

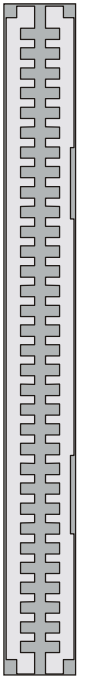


Active Low Signal

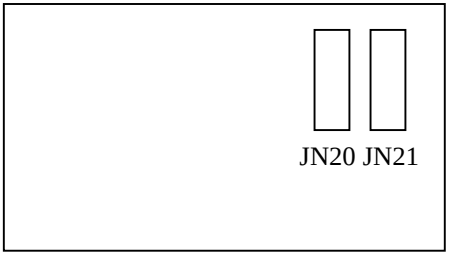
E.12 J20 PMC CONNECTOR

Pin Number	Signal
1	Not Connected
3	GND
5	INTB#
7	BUSMODE1#
9	INTD#
11	GND
13	PCLK-PMC
15	GND
17	REQ-PMC#
19	VCC
21	AD28
23	AD25
25	GND
27	AD22
29	AD19
31	VCC
33	FRAME#
35	GND
37	DEVSEL#
39	GND
41	PMC-SDONE#
43	PAR
45	VCC
47	AD12
49	AD9
51	GND
53	AD6
55	AD4
57	VCC
59	AD2
61	AD0
63	GND

Top View



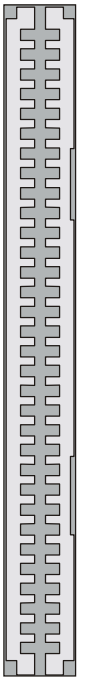
Pin Number	Signal
2	-12V
4	INTA#
6	INTC#
8	VCC
10	Not Connected
12	Not Connected
14	GND
16	GNT-PMC#
18	VCC
20	AD31
22	AD27
24	GND
26	C/BE3#
28	AD21
30	VCC
32	AD17
34	GND
36	IRDY#
38	VCC
40	LOCK#
42	PMC-SB0#
44	GND
46	AD15
48	AD11
50	VCC
52	C/BE0#
54	AD5
56	GND
58	AD3
60	AD1
62	VCC
64	Not Connected



E.13 J21 PMC CONNECTOR

Pin Number	Signal
1	+12V
3	Not Connected
5	Not Connected
7	GND
9	Not Connected
11	BUSMODE2
13	PCI RST
15	VCC
17	Not Connected
19	AD30
21	GND
23	AD24
25	IDSEL_PMC
27	VCC
29	AD18
31	AD16
33	GND
35	TRDY
37	GND
39	PERR
41	VCC
43	C/BE1
45	AD14
47	GND
49	AD8
51	AD7
53	VCC
55	Not Connected
57	Not Connected
59	GND
61	Not Connected
63	GND

Top View

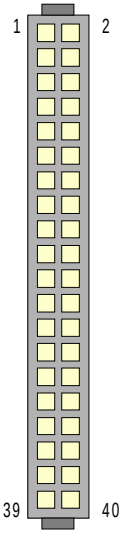


Pin Number	Signal
2	Not Connected
4	Not Connected
6	GND
8	Not Connected
10	Not Connected
12	VCC
14	BUSMODE3
16	BUSMODE4
18	GND
20	AD29
22	AD26
24	VCC
26	AD23
28	AD20
30	GND
32	C/BE2
34	Not Connected
36	VCC
38	STOP
40	GND
42	SERR
44	GND
46	AD13
48	AD10
50	VCC
52	Not Connected
54	Not Connected
56	GND
58	Not Connected
60	Not Connected
62	VCC
64	Not Connected

E.14 J60(MXS), J18 (CXS) - CompactFlash Disk Connector

Signal	Pin Number
D11	1
D12	3
D13	5
D14	7
D15	9
CS3#	11
Not Connected	13
Not Connected	15
PDIAG#	17
RIRQ14	19
VCC	21
GND	23
BRSTDRV#	25
To W5 jumper	27
A1	29
A0	31
D0	33
D1	35
D2	37
IOCS16#	39

Top View

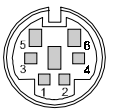


Pin Number	Signal
2	GND
4	D3
6	D4
8	D5
10	D6
12	D7
14	RPCS1#
16	IOR#
18	IOW#
20	VCC
22	VCC
24	GND
26	GND
28	A2
30	CFLASH-ACT#
32	Not Connected
34	D8
36	D9
38	D10
40	GND

E.15 J50 (MXS), J17 (CXS) - PS/2 Mouse Connector

Signal	
KDATA	1
MDATA	2
GND	3
5V Fused	4
KBCLK	5
MCLK	6

Front View



E.16 B1 (MXS, CXS) Battery Header

Signal	
Battery (+)	1
Battery (-)	2

Front View

F. BIOS SETUP ERROR CODES

F.1 POST BEEP

POST beep codes are defined in the BIOS to provide low level tone indication when an error occurs during the BIOS initialization.

Beep codes consist of a combination of long and short beeps. They are described as follows:

Beep Codes

Post code	Beep Code	Description
41	**-*	Enterring the boot block recovery code (i.e. Main BIOS checksum error)
22	*-*-*	Error when getting the boot block flash ID code
33	*-*-*-*	Error when erasing the boot block flash
44	*-*-*-*-*	Error when programming the boot block flash
55	*-*	Success of the boot block recovery code. The board is ready to be manually reset.

Legend * = 1 Short beep code, ** = 1 Long beep code, - = Silence

F.2 POST MESSAGES

During the Power On Self Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

"PRESS F1 TO CONTINUE, DEL TO ENTER SETUP".

F.3 ERROR MESSAGES

One or more of the following messages may be displayed if the BIOS detects an error during the POST. This list includes messages for both the ISA and EISA BIOS.

CMOS BATTERY HAS FAILED

1. If it's the first boot, check for the onboard battery jumper (jumper W4 for both the cPCI-MXS and cPCI-CXS). The board is shipped with W4 jumper set to OFF (onboard battery disconnected). This jumper must be shorted (ON) for proper battery operation.
2. CMOS battery is no longer functional. It should be replaced.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This indicates that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Floppy Drive A and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause BIOS to ignore the missing keyboard and continue the boot.

OFFENDING SEGMENT

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a Non-maskable Interrupt condition during boot, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

F.4 POST CODES

POST #	Designation	Description	
01	BOOT BLOCK	Boot Block in EMERGENCY : Clear Base Memory Area.	
03	Initialize Chips	1. Clear CMOS shutdown byte. 2. Initialize EISA extended registers. (Not for us since we don't have EISA bus.)	
04	Test Memory Refresh Toggle	RAM must be periodically refreshed in order to keep the memory from decaying.	
05	Blank Video, Initialize Keyboard	1. Clear CMOS reset status byte. 2. Early Keyboard initialization.	Boot Block in EMERGENCY: Initialize Keyboard Controller.
06	EPROM Checksum	1. Test F000h segment shadow readable and writeable for POST access correct. If not, show POST FE and beep continuously… 2. Autodetect Flash EPROM.	
07	Test CMOS Interface and Battery Status	1. Install the Teknor segment. 2. Verifies CMOS is working correctly (walking bit test). 3. Restore CMOS from Flash if option is enabled. 4. Check for OVERRIDE KEY (INSERT key).	
08	Program Chipset default	Program Chipset default (show POST BEh).	
09	Early Cache Initialization	1. Check for Intel's and/or Cyrix CPU. 2. Early Cache Initialization when cache is separate from chipset. 3. Turn off Gate A20.	
0A	Setup Interrupt Vector Table	1. Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize int. 00h-1Fh according to INT_TBL. 2. Early Power Management Initialization.	
0B	Test CMOS RAM Checksum	1. Verify time and date for valid values. 2. If Override enabled, check for Override key. If Override key pressed, Kill CMOS checksum. 3. Check CMOS Battery (useless if save CMOS in FLASH enabled since it's already done). 4. Verify Checksum, if bad, load defaults. 5. Copy CMOS in the stack. 6. Clear CMOS Alarm date. 7. Clear HD if Hidden. 8. Clear Floppy "B" if only one drive. 9. Detect for a Math Co-processor. 10. Set Fast Gate A20 Flag in CMOS. 11. If "B" drive only is set the 2 Drive are set… 12. Program Chipset for early Power Management. 13. P6 Bios Update (if applicable). *14. Kill Onboard PnP IO.* *15. PnP Early Initialization.* *16. PnP System Resource:* *1. Get ESCD.* *2. Create default SYSTEM_MAP.* *3. Decode/Record ISA ESCD resources.* *4. Record I/O port for PnP operation.* 17. Chipset Early Shadow.	

POST #	Designation	Description	
0C	Initialize Keyboard	1. Open Xilinx I/O Port location to x90h (X=1,2 or 3) inside the chipset (if necessary). 2. Disable (if necessary). Thermal Management. 3. Disable (if necessary) Ethernet Chip.Set IDE Detect counter to 0. 4. Set CD-ROM found variable to 0. 5. Initialize zone 40:0h for the keyboard buffer.	Boot Block 1st : Verify BIOS checksum. Boot Block in EMERGENCY 2nd : Init. vector 00h through 77h.
0D	Initialize Video Interface & Chipset	*1. On M1 set the cache for the memory installed.* *2. On PCI, do a PCI ROM init.* 3. On P6, Init. Apic. 4. Init. Chipset. 5. Turn ON CPU Cache. 6. Set Maximum Speed. 7. Measure CPU Clock Speed. 8. Restore Speed. 9. Turn Off CPU Cache. 10. Early Video Shadow. 11. Read CMOS location 14h to find out type of video to use. Detect and initialize Video Adapter. 12. Init. T380 if necessary.	Boot Block in EMERGENCY: Try to init. Video Card…
0E	Test Video Memory	1. If CGA or MONO, test video memory. 2. Beep the speaker. 3. Show the LOGO. 4. Install VT100 driver if necessary. 5. Write sign-on message to screen. 6. Write Copyright message to screen. 7. Write Evaluation message to screen. 8. Show CPU type and speed.	
0F	Test DMA Controller 0	Test DMA Controller 0.	
10	Test DMA Controller 1	Test DMA Controller 1.	
11	Test DMA Page Registers	Test DMA Page Registers.	
12	Reserved	Reserved for 8254 Counter 0 - Not implemented.	
13	Reserved	Reserved for 8254 Counter 1 - Not implemented.	
14	Test Timer Counter 2	Test 8254 Timer 0 Counter 2.	
15	PIC Test 8259-1 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	
16	PIC Test 8259-2 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	

POST #	Designation	Description
17	Test Struck 8259's Interrupt Bits	Nothing
18	Test 8259 Interrupt functionality	Force an interrupt and verify that the interrupt occurred (IRQ 0 - clock int. 8h).
19	Test Struck NMI Bits (Parity/ IO check)	Nothing.
1A-1E	Reserved	Reserved
1F	Set EISA Mode	If EISA non-volatile memory checksum is good, execute EISA initialization. If no, execute ISA test and clear EISA mode flag. Test EISA Configuration Memory integrity (checksum & communication interface).
20-2F	Enable Slots 0-15	Initialize slot 0 (System Board) to slot 15.
30	Size Base & Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB.
31	Test Base & Extended Memory	1. Test base memory from 256K to 640K and extended memory above 1MB using various patterns. 2. The last test is filling memory with 0's. 3. On a quick memory test or if user press the ESC key while testing memory, only the last test is performed.
32	Test EISA Extended Memory	If EISA Mode flag is set, then test EISA memory found in slots Initialization. NOTE 1: This will be skipped in ISA mode. NOTE 2: This POST also Detect & Report I/O PORTS and also Init. Super IO.
33-3C	Reserved	Reserved
3C	Setup Enable	
3D	Initialize & Install PS/2 Mouse	Detect if mouse is present. Initialize mouse. Install interrupt vector.
3E	Setup Cache Controller	Initialize cache controller.
3F-40	Reserved	Reserved
41	Initialize Floppy Drive & Controller	1. Verify if we should enter setup. If so, enter setup. 2. Initialize floppy disk drive controller and any drive. Boot Block in EMERGENCY: Scan for Floppy for emergency disk…
42	Initialize Hard Drive & Controller	Initialize hard drive controller and any drive. (Call HD_INSTALL).
43	Detect & Initialize Serial/Parallel/Joystick ports	Initialize any serial, parallel and game ports.
44	Reserved	Reserved
45	Detect & Initialize Math Coprocessor	Initialize Math Coprocessor.
46	Reserved	Reserved
47	Set Speed for Boot	Set Speed for Boot.
48-4C	Reserved	Reserved
4D	Init. PC-Speaker to LINE OUT	Enable access to PC-Speaker to LINE OUT and Enable/Disable it. (T934).
4E	Manufacturing POST Loop or display Messages	1. Reboot if Manufacturing POST Loop pin is set. 2. Otherwise display any messages (i.e., any non-fatal errors that were detected during POST). 3. Enter SETUP if needed.
4F	Security Check	*Ask password security if needed.*
50	Write CMOS	Write all CMOS values back to CMOS-RAM and clear screen.

POST #	Designation	Description	
51	Pre-Boot Enable	1. Enable Parity checker. 2. Enable NMI. 3. Enable cache before boot.	
52	Initialize Option (ROM scan)	1. Call POST 81 2. Initialize any ROMs present from C8000h to DBFFFh. Disable POST code from segment E0000h. 3. Initialize any ROMs present from DC000h to E0800h. NOTE: When FSCAN option is enabled, will initialize from C8000h to F7FFFh.	
53	Initialize Time Value	Initialize Time value in 40h: BIOS area.	
54-5F	Reserved	Reserved	
60		Store boot partition of head & cylinder.	
61	Final Init	*For last µs detail before boot.*	
62	Num Lock ON	Put Num Lock ON and Daylight Saving.	
63	Boot Attempt	1. Call POST 82. 2. Set Low stack. 3. Boot via int 19h.	
64-7F	Reserved	Reserved	
80	Teknor Segment Move 1	Install the Teknor segment from Flash to DC00:0h.	
81	Teknor Segment Move 2	Install the Teknor segment from DC00:0h to 7000:0h.	
82	Teknor Segment Move 3	Install the Teknor segment from 7000:0h to EC00:0h.	
83	Check & Program CPLD	Check & Program CPLD for valid UserCode & IDCode.	
84	Teknor CRC Check	Check if Teknor block have a valid CRC. If not, the Emergency procedure is launched.	
85-AF	Reserved	Reserved	
B0	Spurious	If interrupt occurs in protected mode.	
B1	Unclaimed NMI	If unmasked NMI occurs, display: Press F1 to disable NMI, F2 reboot.	
B2-BD	Reserved	Reserved	
BE	Early Prog Chipset Def.	Going to early program chipset to default values (called from POST_8s).	
BF	Program Chip Set	Called early at POST 0Dh to program chipset from CT-TABLE.	
C0	Turn ON/OFF Cache	OEM Specific - Cache control.	Boot Block: First POST.
C1	Memory presence	OEM Specific - Test to size on-board memory test.	Boot Block: Search for Boot Block Signature "*BBSS*".
C2	Early Memory Initialization	OEM Specific - Board Initialization.	
C3	Extended Memory Initialization	OEM Specific - Turn ON extended memory DRAM select.	Boot Block: Expand compressed BIOS
C4	Special Display Switch Handling	OEM Specific - Display/Video switch handling so that display switch errors never occur.	
C5	Early Shadow	OEM Specific - Early Shadow enable for fast boot.	Boot Block: Early Shadow System BIOS.
C6	Cache Programming	OEM Specific - Routine for programming which region are cacheable.	Boot Block: Cache Sizing
C7	Reserved	Reserved	
C8	Special Speed Switching	OEM Specific - Routine to handle speed switching.	
C9	Special Shadow Handling	OEM Specific - Normal Shadow routine.	

POST #	Designation	Description
CA	Very Early Initialization	OEM Specific – Initialize hardware before any other hardware initialization.
CB-CF	Reserved	Reserved
D0	Power Management Full speed	Trying to go back or into full speed mode.
D1	Power Management -- Doze mode	Trying to go or in Doze mode.
D2	Power Management --Sleep mode	Trying to go or in Sleep mode.
D3	Power Management – Suspend mode	Trying to go or in Suspend mode.
D4-DF	Debug	Available POST codes for use by source code customers during development.
E0	Reserved	Reserved
E1-EE	Setup Page	Page 1 to Page 14
EF	Shadow Error	In POST 6 to signal a Shadow Error.
F0-FE	Reserved	Reserved
FF	Boot	The system is now booted or waiting for an OS.

G. EMERGENCY PROCEDURE

Follow this procedure only in case of emergency such as a critical error occurred during the Boot Block Flash BIOS update (when using UBIOS utility program or if you meet one of the following symptoms at anytime:

1. No POST code on a power up (when using a POST card).
2. System stops at POST 41(when using a POST card) and associated beep code is generated (Refer to Section E.1).
3. Board does not boot, even after usual hardware and connection verifications.

G.1 HOW TO RUN EMERGENCY PROCEDURE

To run an EMERGENCY PROCEDURE, proceed as follows:

1. Remove battery jumper.
2. Disable the Power Fail Detection function.
3. Connected a 1.44MB floppy drive (drive A) to the board, and insert the EMERGENCY diskette, that you previously created, in it.
4. Power on the board. (Note that no VGA is present during this procedure.)
5. Boot block flash update will be completed when the POST code 55 is displayed (when using a POST card) or the associated beep code sounds (indicated in Section E-5).
6. After the procedure is successfully completed, power down the board, install your battery and Power Fail Detection jumpers.

   The boot block flash BIOS should be correctly programmed and the system should run properly.

NOTE See section F.2 Generate a Emergency Floppy Diskette.

G.2 GENERATE AN EMERGENCY FLOPPY DISKETTE :

Use a system that has a 1.44 Mbytes floppy drive A.

1. Insert the Teknor Emergency Diskette in drive A:
2. Copy the two files WDISK.COM and EMERDISK.TEK from drive A: to your hard drive (those files are available in your Teknor diskette package).
3. Remove the Teknor Emergency diskette and insert a DOS formatted floppy diskette in drive A:.
4. At the DOS prompt of your hard drive (same path of the two files WDISK.COM and EMERDISK.TEK), type WDISK EMERDISK.TEK then press Enter key.
5. The program may display one of the following messages:

   "Emergency Code transferred"

   The emergency diskette has been successfully created. Take the appropriate actions and restart from the step 4) when you see the following messages.

   "Write to disk failure!"

   Verify if your floppy diskette is write-protected.

   "The file to program in flash was not found"

   Be sure that EMERDISK.TEK file is in your current path.

   "Unable to read the binary file" or "Unable to close the opened file"

   Possible floppy diskette corruption or bad data transfer between floppy disk and host system.

   "Unable to allocate a memory block of 256 Kbytes"

   Not enough memory to run the WDISK program.

H. GETTING HELP

At Teknor, we take great pride in our customer's successes. We strongly believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, you may contact our Technical Support department at:

CANADIAN HEADQUARTERS
Tel. (450) 437-5682
Fax: (450) 437-8053

If you have any questions about Teknor, our products or services, you may reach us at the above numbers or by writing to :

Teknor Applicom inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

LIMITED WARRANTY

TEKNOR APPLICOM INC, ("The seller") warrants its boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts, which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

Returning Defective Merchandise

If your Teknor product malfunctions, please do the following before returning any merchandise:

1) Call our Technical Support department in Canada at (450) 437-5682. Make certain you have the following at hand:

   - The Teknor Invoice number
   - Your purchase order number
   - The serial number of the defective board.

2) Give the serial number found on the back of the board and explain the nature of your problem to a service technician.

3) If the problem cannot be solved over the telephone, the technician will further instruct you on the return procedure.

4) Prior to returning any merchandise, make certain you receive an RMA number from Teknor's Technical Support and clearly mark this number on the outside of the package you are returning. To request a number, follow these steps:

   - Make a copy of the request form on the following page.
   - Fill out the form and be as specific as you can about the board's problem.
   - Fax it to us.

5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.

6) When returning a Teknor board:

   i) Make certain that the board is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.

   ii) Ship prepaid to (but not insured, since incoming units are insured by Teknor):

Teknor Applicom inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

RETURN TO MANUFACTURER AUTHORIZATION REQUEST

Contact Name : _____

Company Name : _____

Street Address : _____

City : _____ Province/State: _____

Country : _____ Postal/Zip Code: _____

Phone Number : _____ Extension : _____

Fax Number : _____

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

Fax this form to Teknor's Technical Support Department in Canada at (450) 437-8053