E²Brain™ Module Specification

Specification for

Embedded Electronic Brains

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Kontron Modular Computers GmbH
Sudetenstraße 7
87600 Kaufbeuren
Germany

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Kontron Modular Computers GmbH
Sudetenstraße 7
D-87600 Kaufbeuren Germany

Tel: +49 (0) 800-SALESKONTRON
Internet: www.kontron.com

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E²Brain™ Module Specification

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1. Introduction

1.1 Objective

The objective of this specification is to provide a basic definition of the physical, mechanical and electrical qualities of Embedded Electronic Brain (E²Brain™) modules as envisioned by Kontron Modular Computers for usage in industrial, scientific, and commercial data processing and process control applications.

1.2 Scope

The scope of this specification is restricted to the definition of E²Brain™ modules and the manner in which they interface with module external entities. For information concerning industry standards which apply to this specification, refer to the appropriate standards documentation.

This specification does not extend to any requirements for compliance with ESD, EMC, or equipment or personnel safety regulations. For such compliance requirements, refer to appropriate regulation documentation.

1.3 Related Publications

The following is a list of reference publications for usage with this specification:

- PCI Local Bus Specification, 2.2, December 18,1998; PCI Special Interest Group
- PICMG® 2.0 R3.0 10/1/99, CompactPCI® Core Specification; PCI Industrial Manufacturers Group (PICMG®)

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2. The E²Brain™ Concept

2.1 Overview

The E²Brain™ concept is a highly flexible approach to providing application developers with the ability to concentrate on the definition of application requirements without having to continuously factor in potential restrictions concerning available data processing and communications functionality.

More specific, data processing and communications requirements become a function of the application and not vice versa. This is possible through the implementation of the E²Brain™ concept. Unlike other approaches to providing application solutions, the E²Brain™ concept concentrates on the most essential aspects of providing data processing and communications without attempting to provide in one entity a complete, self-contained, computer system.

The E²Brain™ specification first of all defines a PCB module with a form factor of 115 x 75 x nn (L x W x H) millimeters where H is (within a specific range) a function of the application. For interfacing with applications, the specification calls for up to four connectors which provide not only interfacing capability for current industry standards but also for future standards or application specific requirements. The type, location, and usage of these connectors is also defined in the specification so as to guarantee standardized compatibility. The specification is open as to the data processing and communications functionality to be implemented which is by definition a function of the application requirements. In addition, the specification envisions considerations for thermal energy dissipation through the implementation of what are to be known as BrainCAP™s (E²Brain™ Cooling Assembly, Protector) which can range from heat spreaders to highly sophisticated heat sink cooling designs.

The key features of the E²Brain™ concept are:

- Very compact and robust form factor
- Independent of CPU architecture
- Scalable, flexible, and open system interface
- PCI Master and Agent Mode
- PCI-64 and PCI-X capability
- Versatile and very powerful communications interfaces
- Complete thermal design concept

2.2 E²Brain™ Functionality

E²Brain™ (Embedded Electronic Brain) is a new platform architecture for advanced computer modules. The E²Brain™ specification defines a mechanical form factor and a comprehensive set of functional interfaces which provide a maximum of flexibility regarding its usage in network and communications equipment as well as in medical electronics or industrial control units. E²Brain™ modules provide complete computer cores integrating a high-performance CPU, system memory and - typical for E²Brain™ - advanced communications controllers. E²Brain™ modules are plugged on customized backplanes or standardized carrier boards which themselves provide the physical interfaces (PHYs) and connectors, power, and additional IO controllers. By using E²Brain™ modules the system developer is relieved of the task of designing computers, and, instead, they permit him to concentrate on the specific product development.

E²Brain™ is a computer platform dedicated not just to one architecture like the PC and Windows architecture, but it is open for all architectures including PowerPC, ARM, SH, x86, and others. E²Brain™ modules are very suitable for “deeply” embedded applications requiring flexible computing power combined with versatile and high-performance communications power.

Therefore, E²Brain™ defines up to four high speed serial ports operating in synchronous, asynchronous, or TDM modes, up to three LAN ports (10/100/1000 MBits/s), and defines also (G)MII and UTOPIA ports for connecting PHYs to optical carrier based networks. Two CAN ports are part of the E²Brain™ specification as well.

On the system side, E²Brain™ modules interface with additional peripheral controllers on the carrier via LPC or typically via PCI acting as a PCI system controller. E²Brain™ modules can also be operated as a peripheral device utilizing the E²Brain™ specification for PCI agent mode. PCI on E²Brain™ is scalable from 32-bit/33MHz over 64-bit up to PCI-X. E²Brain™ is already prepared beyond PCI to support the coming switch-matrix based high speed interconnects such as parallel RapidIO. High speed serial interconnects such as PCI-Express and serial RapidIO will be dealt with in future releases of the E²Brain™ Module Specification.

Although typical E²Brain™ modules dissipate power in the range of two to three watts, they are part of a well thought-out thermal design concept which considers the thermal aspects right from the beginning. By utilizing BrainCAPs, cooling, mechanical stabilization, and EMC compliance are combined in a single concept to satisfy almost any application requirement.

2.3 Basic Architecture

The following figure illustrates the basic functional architecture of E²Brain™ modules. Common to all E²Brain™ modules are the data processing and communications core and the system and communications interfaces.

The application requirements determine the functionality required of the E²Brain™ module core which in turn mandates the functionality to be provided by the system and communications interfaces. Both of these interfaces are comprised of a base set and an extended set of functional features.

The system interface to the application is accomplished through connectors Pn1 and Pn2. Connector Pn1 provides the base set of system interfacing and Pn2 the extended set. If the application does not require extended system interfacing, it is not necessary to populate connector Pn2. The same analogy applies to the communications interfacing whereby connector Pn3 provides the base set of communications interfacing and Pn4 the extended set. Pn4 is not required to be populated if there is not an application requirement for it. This concept together with a corresponding core provides a maximum of scalability and flexibility to satisfy the most demanding of applications.

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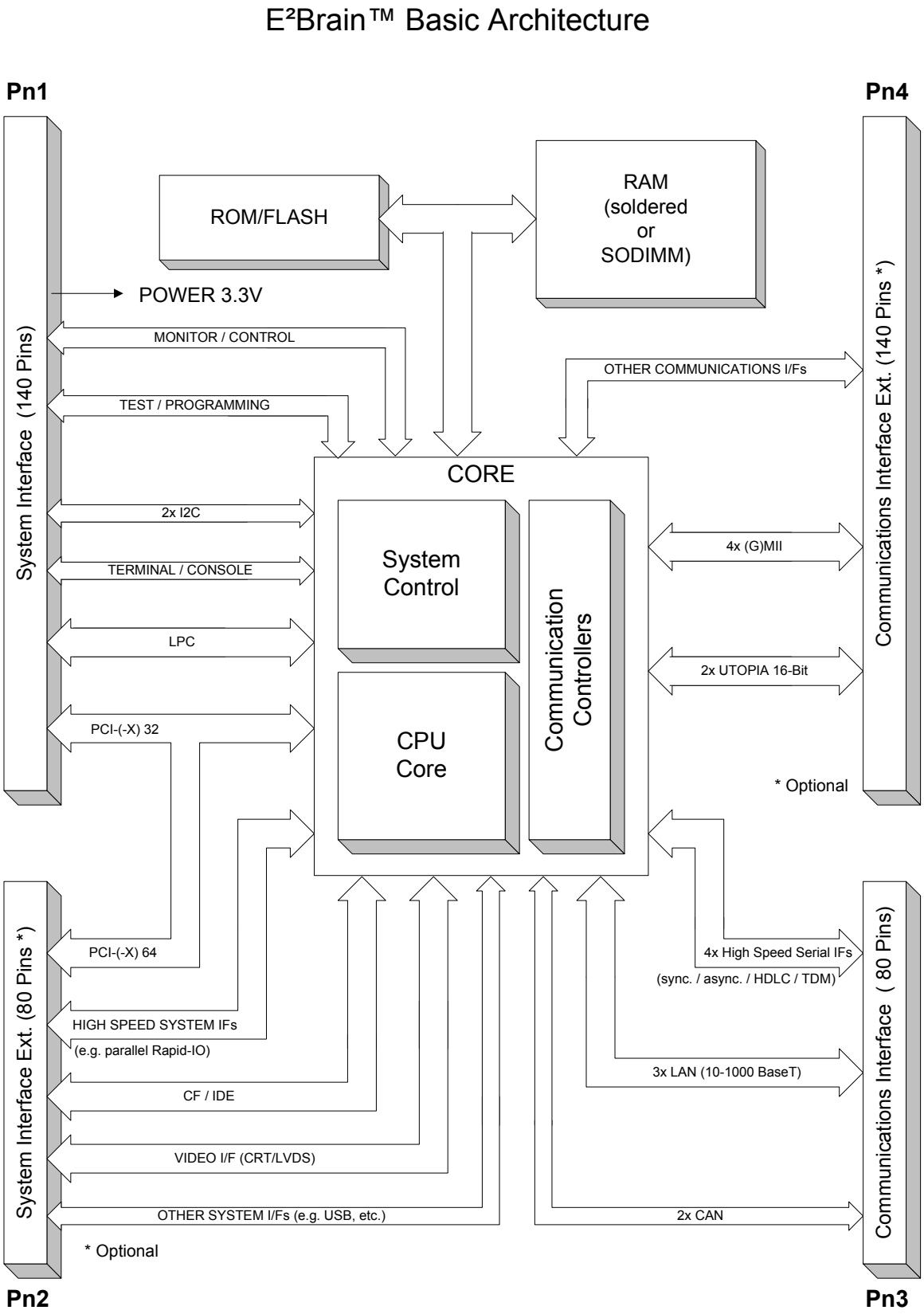
Figure 1: E²Brain™ Basic Architecture

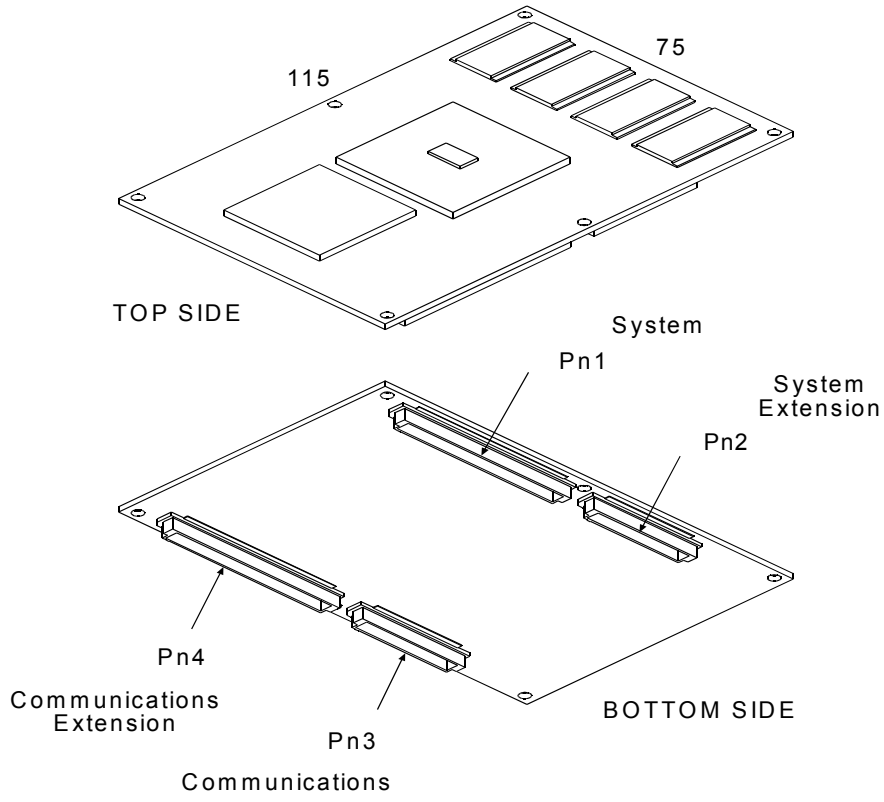


2.4 E²Brain™ Modules

E²Brain™ modules occupy an area of 75 by 115 millimeters and have a variable stacking height from 5.0 to 11.0 millimeters. Total height of an E²Brain™ module is a function of the application requirements which may call for a minimum of height or, depending on application requirements, can be extended to accommodate a wide variety of thermal design solutions.

The E²Brain™ specification foresees the use of up to four application interfacing connectors with a total 440 contacts. Located on the bottom side of module, there is at least one system and one communications interfacing connector required. To support extended requirements, additional system and communications connectors may be added. Different stacking heights between E²Brain™ module and carrier are supported through the use of appropriate connectors on the carrier board or by appropriate connectors on the E²Brain™ modules.

Figure 2: E²Brain™ Module Form Factor



2.5 E²Brain™ Carrier Boards

The carrier board or custom backplane on which the E²Brain™ module is mounted provides the power supply, the necessary PHYs and cable connectors, and, optionally, additional IO controllers. Exceptions are carrier boards where an E²Brain™ module is used as a peripheral. In this case the carrier board would house the system master CPU. An example would be a CompactPCI System Controller Board with an E²Brain™ site or a industrial PC motherboard with an E²Brain™ on the PC Card. Another constellation could be a carrier where more than one E²Brain™ site is available. In this case, one E²Brain™ could act as the system controller whereas the others would operate as peripherals. The following figures illustrate these possibilites.

Figure 3: Custom Backplane Board

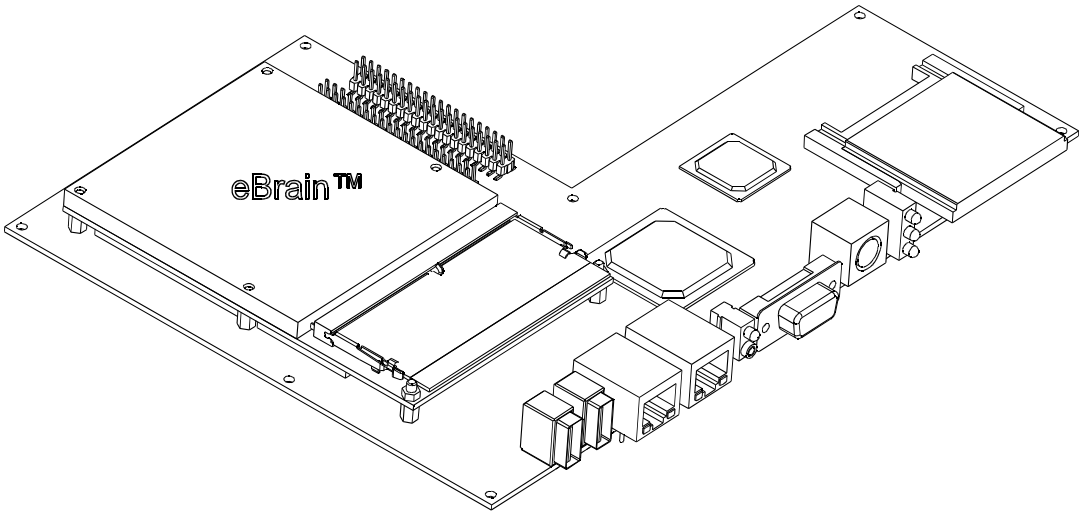


Figure 4: Standardized 6U Carrier Board for Up to Three E²Brain™ Modules

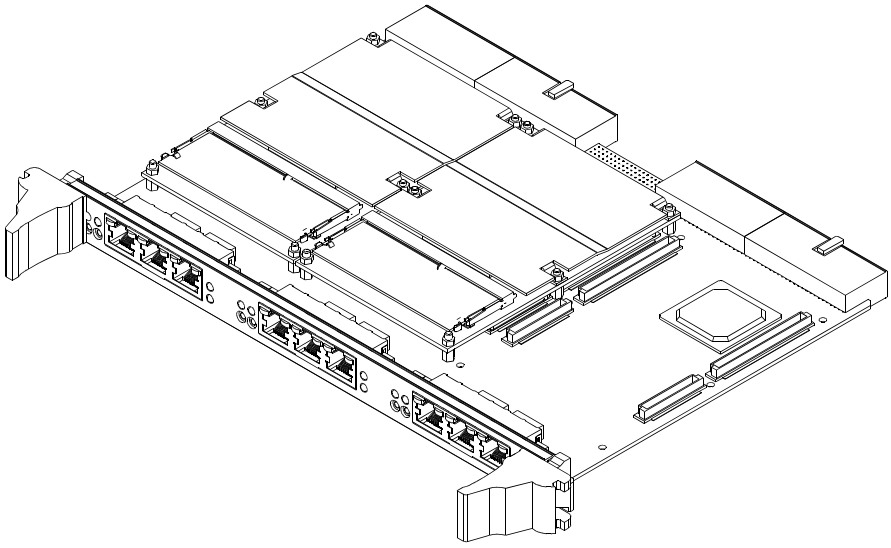
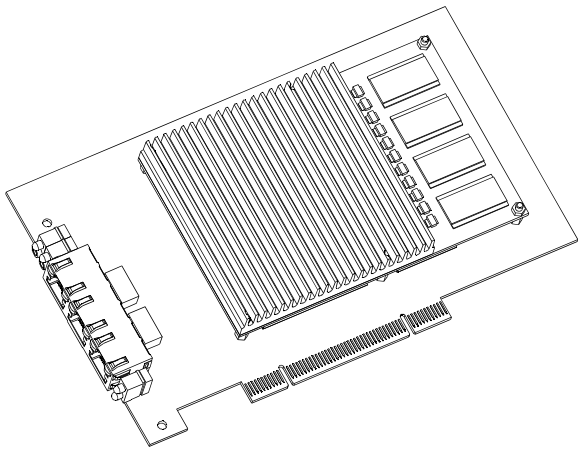


Figure 5: PC PCI Carrier Board with Passive Heatsink Cooling Solution



2.6 Applications

“Take what fits best, don’t pay for more.”

Due to the versatility and flexibility of the E²Brain™ family concept, the modules are best suited for any kind of embedded application where comprehensive and high performance computing and communications functionality is required. Different CPU architectures, scalable performance and connectivity allow the user to tailor the computing core exactly to the needs of the application.

The E²Brain™ modules can be basically divided in two groups:

- Communications engines
- Advanced computing cores

Communications engines are dedicated to applications with enhanced requirements in terms of connectivity and availability of communications specific interfaces such as:

- Serial ports: fast synchronous, asynchronous, or TDM modes
- ATM and UTOPIA
- Multiple Ethernet interfaces

These kind of modules are a perfect core for subsystem controllers in the Telecom infrastructure like PBXs (Private Branch Exchange) and small to medium size telephony systems as well as to any kind of Telecom or Datacom gateways, routers, bridges, and switches in commercial and industrial application areas.

Advanced computing cores provide an excellent combination of computing power with a comprehensive set of interfaces like serial and Ethernet ports. Perfectly fitted for use in real time control units for industrial and medical applications or test and measurement equipment. Deeply embedded, the advanced computing cores also power enterprise grade office equipment, mobile test stations in the automotive industry, and all kinds of intelligent user terminals.

Common to both principle types of modules is the excellent performance to power consumption ratio. Together with the well thought-out thermal design concept “BrainCAP” the E²Brain™ module family is perfectly qualified for use in deeply embedded and mobile applications with power consumption and heat dissipation constraints.

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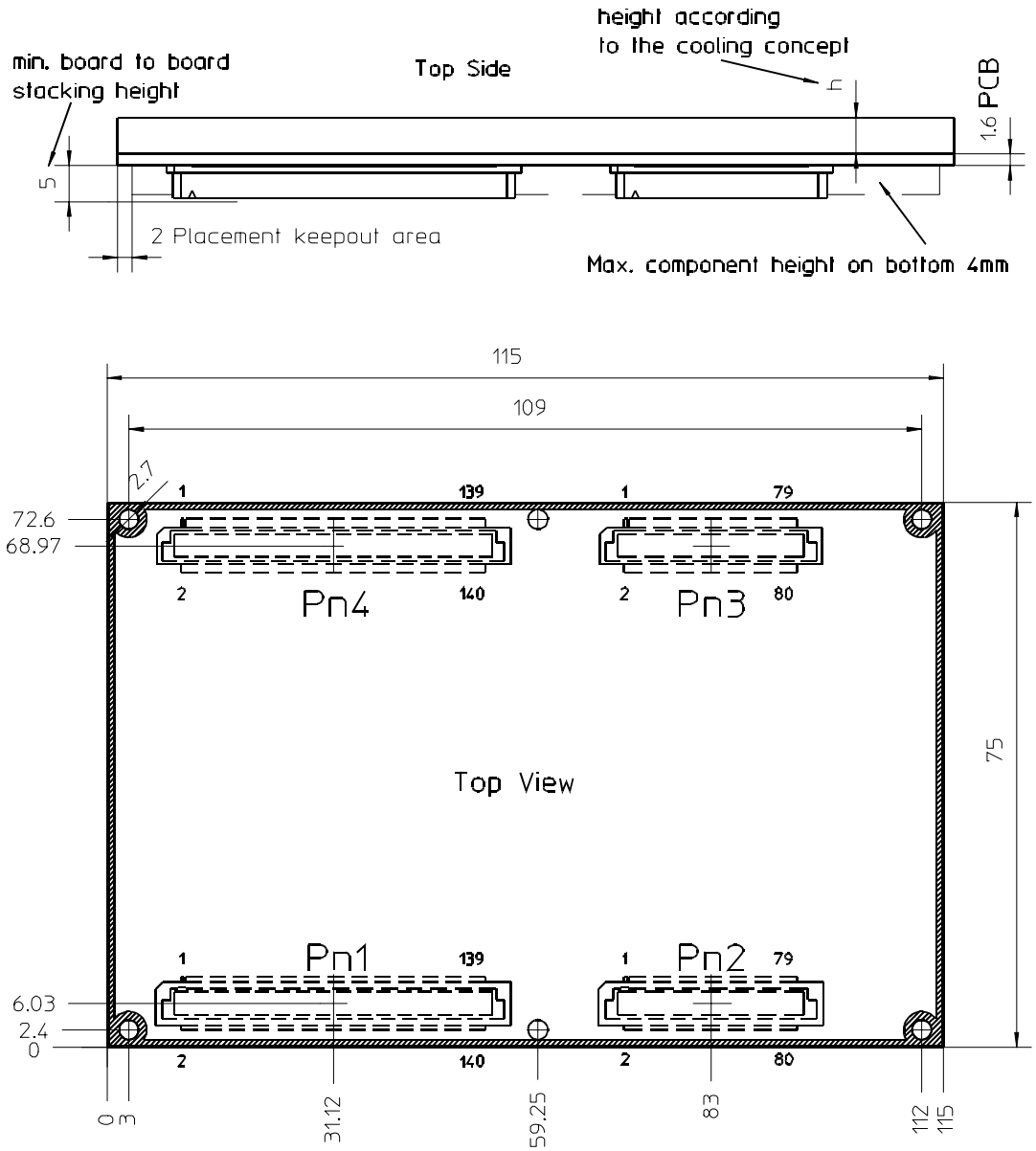
3. Mechanical Characteristics

3.1 Module Dimensions

The following figure illustrates the basic E²Brain™ module layout and corresponding dimensions.

Figure 6: E²Brain™ Module Dimensions



3.2 Board-to-Board Connections

Different system constraints may demand different stacking heights between a carrier board and an E²Brain™ module. For example, limited height within the chassis could require a lowest possible profile of the E²Brain™ carrier board package whereas component placement on the carrier board in the area below the E²Brain™ module could demand a higher stacking height.

Stacking heights can range from 5 mm to 16 mm. Different stacking heights can be achieved by selecting appropriate mating connectors for both the E²Brain™ module and the carrier board. Standard connectors on the E²Brain™ module are HIROSE FX8C-80P-SV and FX8C-140P-SV.

The following table shows the various stacking heights for the available mating connectors and the corresponding maximum component heights for the carrier board below the E²Brain™ module. The maximum component height for E²Brain™ modules on the connector side of the module is defined to be 2.0 millimeters. When components are placed between the E²Brain™ module and the carrier, thermal design requirements must be taken into consideration.

Table 1: Module Stacking and Component Heights

	CONNECTOR CARRIER FX8C-nnnS-SV		CONNECTOR CARRIER FX8C-nnnS-SV5	
CONNECTOR E²Brain™ Module	STACKING HEIGHT	CARRIER COMPONENT HEIGHT	STACKING HEIGHT	CARRIER COMPONENT HEIGHT
FX8C-nnnP-SV	5 mm	3 mm	10 mm	8 mm
FX8C-nnnP-SV1	6 mm	4 mm	11 mm	9 mm
FX8C-nnnP-SV2	7 mm	5 mm	12 mm	10 mm
FX8C-nnnP-SV4	9 mm	7 mm	14 mm	12 mm
FX8C-nnnP-SV6	11 mm	9 mm	16 mm	14 mm

3.3 Thermal Concept

For reliable operation and a long lifetime of computer boards in general, it is important to keep the operating temperatures of components as low as possible. Depending on the amount of thermal energy the components dissipate and the environmental conditions there are different approaches to meet that necessity. In general, thermal management can range from natural air convection, heatsinks combined with and without forced airflow, up to heatpipes or peltier elements. The simple theory behind this is summarized in the following.

Like the ohmic resistance “R” defined as “voltage divided by current”, there is a thermal resistance “R_{th}” defined as “delta Temperature divided by Power loss”. Its unit is “Kelvin per Watt” [K/W].

In reverse, with a known thermal resistance the temperature rise at a maximum power loss can be calculated as follows:

$$\Delta T = P * R_{th}$$

Example:

A CPU has a thermal resistance of R_{th} = 20 K/W for convection cooling with a good thermal PCB layout. With its maximum Power dissipation of 2.5 Watt the case heats up by:

$$\Delta T=P * R_{th} =2.5\ W * 20\ K/W = 50\ degrees\ K$$

Based on a given maximum case temperature of T_{jmax} = 105°C, the maximum ambient temperature of the processor would be 55°C (no heatsink, no forced airflow).

By adding a passive heatsink with an given value of 12 K/W the total thermal resistance is:

$$R_{thtot} = 1/(1/R_{th} + 1/R_{thhs}) = 1/(1/20 +1/12) = 7.5\ K/W$$

$$\rightarrow \Delta T=P * R_{th} = 2.5\ W * 7.5\ K/W = 18.75\ degrees\ K$$

Thus, with the given heatsink the maximum ambient temperature now would be 86 °C.

By adding forced airflow this value can be further improved. With a given airflow of 1m/s an additional factor of proportion has to be considered.

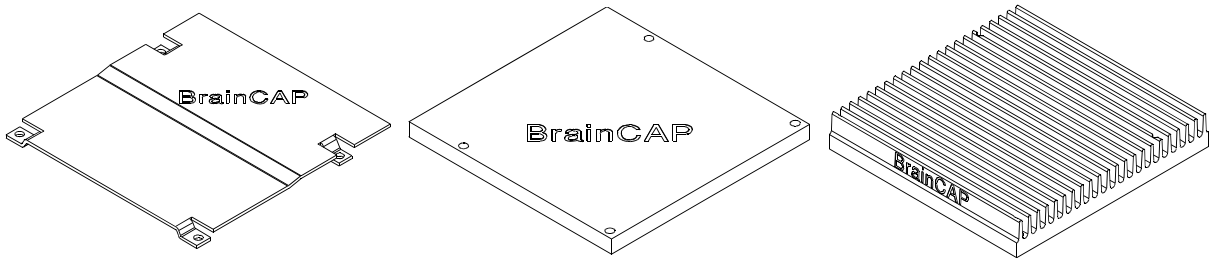
$$R_{thtot} = R_{th} * a = 7.5\ K/W * 0.6 = 4.5\ K/W$$

$$\rightarrow \Delta T=P * R_{th} = 2.5\ W * 4.5\ K/W = 11.25\ degrees\ K$$

Thus, with the additional forced airflow, the maximum ambient operating temperature now would be 93.7 °C.

Even if low power E²Brain™ modules don't require additional cooling measures, the thermal aspect is taken into consideration by specification. E²Brain™ concentrates on passive cooling which means "no fans on the module". Moreover, E²Brain™ prefers module cooling instead of component cooling. Therefore, the thermal concept provides BrainCAPs with standardized mechanical profiles and mounting. BrainCAPs are module heatsinks individually designed and tuned for a given specific module. BrainCAPs combine cooling with mechanical stabilization and EMI protection by its design.

Figure 7: Examples of BrainCAPS



Sheet Metal Heat Spreader | **Massive Aluminum Heatsink** | **Heatsink with Cooling Fins**

For applications where the chassis itself serves as the heatsink or the cooling device is mounted on the carrier, a heat spreader may be the preferred solution.

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4. Electrical Characteristics

By design the application interfacing to E²Brain™ modules is accomplished through the use of up to four discrete electrical connectors. These special, high density, low profile electrical connectors make a total of 440 signal paths available which are capable of satisfying even the most demanding of application requirements.

E²Brain™ modules are design to support four interface connectors. The standard configuration supports primary application system and communications interfacing with two connectors. Furthermore, the E²Brain™ specification makes provisions for application defined use of signal paths depending on the CPU architecture design. This feature of E²Brain™ modules offers a very wide range of scalability as well as flexibility to system designers.

The E²Brain™ specification defines the following connectors based on their designated interfacing functionality:

System:

- Pn1: System Interface
- Pn2: System Interface Extension

Communications:

- Pn3: Communications Interface
- Pn4: Communications Interface Extension

Pn1 and Pn3 are the standard interfacing connectors of E²Brain™ modules and provide the basic interfacing required for E²Brain™ operation. Pn2 and Pn4 are interfacing connectors which extend E²Brain™ functionality.

The System Interface and the System Interface Extension are specified primarily to provide discrete interfacing of system type I/O devices, whereas the Communications Interface and the Communications Interface Extension are specified to provide more general purpose type interfacing either directly to a network or to remote system I/O type devices.

The following chapters describe each of these interfaces and provide detailed information concerning their physical and electrical characteristics as well their usage.

4.1 System Interface

As the name implies, this interface provides the basic application connection functionality required to integrate E²Brain™ modules either as a high performance core or as a dedicated, special purpose subsystem within comprehensive data processing and handling systems which are suitable for practically any type of application requirements.

The System Interface is realized using a 140-pin, HIROSE FX8C-140P-SV connector designated as Pn1. The following table provides an overview of the signal types and a brief description of the interfacing realized on this connector. The ensuing chapters provide more detailed information concerning the signal specification for this interface.

Table 2: System Interface (Pn1) Signal Types

SIGNAL TYPE	DESCRIPTION
POWER	E²Brain™ module input power, grounds, battery backup power, PCI signaling voltage V(I/O)
MONITOR AND CONTROL (MC)	Monitor signals for LEDs and PCI operation. Control signals for E²Brain™ module operation
TEST AND PROGRAMMING (TP)	JTAG and DEBUG signals. System programming signals
TERMINAL AND CONSOLE (TC)	Two 2-wire serial interfaces: RxD1/TxD1: Used by the boot loader during startup as a terminal interface; once the system has been booted, is available as general purpose serial interface (Terminal) RxD2/TxD2: general purpose serial interface (Console)
I2C	One I2C standard interface for low speed, serial, inter-chip communications
LPC	One LPC standard interface for (GP)IOs and simple memory interfacing
PCI	One PCI (-X) standard interface for PCI-bus interfacing

4.1.1 Pn1 Connector Pinout

Because the E²Brain™ specification defines signal interfacing which is at the physical component level, the actual electrical characteristics of signals are for the most part different from those which are specified using accepted industry standards which apply more to unit-to-unit level signals. Only in those cases where the industry standard for such signals is at the physical component level are the characteristics of the signals specified compliant with the standard indicated, for example: PCI compliant signals.

The following table provides signal pinouts along with information concerning signal characteristics for connector Pn1 of E²Brain™ modules.

Table 3: Pinout of Pn1 Connector

SIGNAL	DIR	SIGNAL GROUP	PIN	PIN	SIGNAL	DIR	SIGNAL GROUP
GND	I	POWER	1	2	AUX-Power	I	POWER
SDA	I/O	I2C	3	4	SCL	I/O	I2C
MC6	O	M/C	5	6	+3.3V	I	POWER
MC0	I	M/C	7	8	MC7	O	M/C
MC2	I	M/C	9	10	MC1	I	M/C
+3.3V	I	POWER	11	12	GND	I	POWER
MC3	I	M/C	13	14	MC11	O	M/C
MC4	I	M/C	15	16	MC5	I	M/C
MC9	O	M/C	17	18	MC8	I	M/C
GND	I	POWER	19	20	MC10	O	M/C
LPCCLK	O	LPC	21	22	RESERVED		RESERVED
LAD0	I/O	LPC	23	24	LAD1	I/O	LPC
LAD2	I/O	LPC	25	26	+3.3V	I	POWER
LFRAME#	O	LPC	27	28	GND	I	POWER
SERIRQ#	I/O	LPC	29	30	LAD3	I/O	LPC
TxD1	O	T/C	31	32	RESERVED		LPC
+3.3V	I	POWER	33	34	TxD2	O	T/C
GND	I	POWER	35	36	RxD2	I	T/C
RxD1	I	T/C	37	38	QUACK/VFLS0	O	T/P
EMU_VCC	I	T/P	39	40	COP-HRST/HRESET	I	T/P
CKSTP_OUT/VFLS1	O	T/P	41	42	GND	I	POWER
COP-SRST/SRESET	O	T/P	43	44	TMS	I	T/P
TRST	I	T/P	45	46	+3.3V	I	POWER
TCK	I	T/P	47	48	TDO	O	T/P
RESERVED		RESERVED	49	50	TDI	I	T/P
GND	I	POWER	51	52	RESERVED		RESERVED
PCI-CLK-OUT-0	O	PCI	53	54	V(I/O)	I	POWER
+3.3V	I	POWER	55	56	PCI-CLK-IN	I	PCI
PCI-CLK-OUT-1	O	PCI	57	58	GND	I	I
PCI-RST#	I/O	PCI	59	60	PCI-CLK-OUT-2	O	PCI
INTA#	I	PCI	61	62	INTC#	I	PCI
INTB#	I	PCI	63	64	GNT#0	I/O	PCI-MASTER
INTD#	I	PCI	65	66	+3.3V	I	POWER
GND	I	POWER	67	68	GNT#1	O	PCI-MASTER
AD31	I/O	PCI	69	70	GNT#2	O	PCI-MASTER

Table 3: Pinout of Pn1 Connector

SIGNAL	DIR	SIGNAL GROUP	PIN	PIN	SIGNAL	DIR	SIGNAL GROUP
AD29	I/O	PCI	71	72	REQ#0	I/O	PCI-MASTER
AD27	I/O	PCI	73	74	REQ#1	I	PCI-MASTER
+3.3V	I	POWER	75	76	GND	I	POWER
AD25	I/O	PCI	77	78	REQ#2	I	PCI-MASTER
C/BE3#	I/O	PCI	79	80	AD30	I/O	PCI
AD23	I/O	PCI	81	82	AD28	I/O	PCI
GND	I	POWER	83	84	AD26	I/O	PCI
AD21	I/O	PCI	85	86	AD24	I/O	PCI
V(I/O)	I	POWER	87	88	+3.3V	I	POWER
AD19	I/O	PCI	89	90	IDSEL	I/O	PCI
AD17	I/O	PCI	91	92	GND	I	POWER
C/BE2#	I/O	PCI	93	94	AD22	I/O	PCI
+3.3V	I	POWER	95	96	AD20	I/O	PCI
IRDY#	I/O	PCI	97	98	AD18	I/O	PCI
DEVSEL#	I/O	PCI	99	100	AD16	I/O	PCI
GND	I	POWER	101	102	FRAME#	I/O	PCI
PCI-X-CAP	I/O	PCI	103	104	GND	I	POWER
LOCK#	I/O	PCI	105	106	TRDY#	I/O	PCI
PERR#	I/O	PCI	107	108	STOP#	I/O	PCI
SERR#	I/O	PCI	109	110	+3.3V	I	POWER
GND	I	POWER	111	112	PAR	I/O	PCI
C/BE1#	I/O	PCI	113	114	AD15	I/O	PCI
AD14	I/O	PCI	115	116	V(I/O)	I	POWER
AD12	I/O	PCI	117	118	AD13	I/O	PCI
AD10	I/O	PCI	119	120	AD11	I/O	PCI
+3.3V	I	POWER	121	122	AD9	I/O	PCI
M66EN	I/O	PCI	123	124	GND	I	POWER
AD8	I/O	PCI	125	126	C/BE0#	I/O	PCI
AD7	I/O	PCI	127	128	AD6	I/O	PCI
AD5	I/O	PCI	129	130	+3.3V	I	POWER
GND	I	POWER	131	132	AD4	I/O	PCI
AD3	I/O	PCI	133	134	AD2	I/O	PCI
AD1	I/O	PCI	135	136	AD0	I/O	PCI
ACK64#	I/O	PCI	137	138	REQ64#	I/O	PCI
+3.3V	I	POWER	139	140	GND	I	POWER

4.1.2 Power Interface

For E²Brain™ modules, a single power supply voltage of 3.3 VDC is specified. If additional voltages are required, for example Vcore, they are generated onboard from the 3.3V supply. The detailed power supply requirements for any give module (e.g. maximum power dissipation) are specified within the corresponding product documentation. The following table summarizes the power specifications.

Table 4: E²Brain™ Power Interface Requirements

VOLTAGE	DESCRIPTION
+ 3.3 VDC	Input voltage tolerance: +5% to -3% Supply voltage ripple: 100 mV peak-to-peak; 0 to 20 MHz
GND	Ground voltage reference input
AUX-Power	Optional auxiliary power input for battery backup of CMOS memory devices
V(I/O)	PCI signalling voltage selection. Requires 5V if a connected PCI device on carrier is a 5V only PCI device, otherwise 3.3V.

4.1.3 Monitor and Control Interface

This interface is comprised of a set of twelve IO signals which can be used to facilitate system integration. Their usage is at the discretion of the system designer and is basically “general purpose”. But, however, specific E²Brain™ modules may pre-define MC functions and dedicate them in hardware and firmware to functions such as reset or abort buttons, etc.

The following table provides a listing of Monitor and Control signals along with a brief description.

Table 5: Monitor and Control Interface Signal Description

SIGNAL	DESCRIPTION
MC0	Input, reset in (i.e. debounced reset button)
MC1	Input, non-maskable interrupt request (i.e. debounced abort button)
MC2	Input, maskable interrupt capable (i.e. DEG, power supply derating)
MC3	Input, maskable interrupt capable (i.e. FAL, power supply failure)
MC4	Input, maskable interrupt capable (i.e. Power Down Request)
MC5	Input in PCI Master Mode, Output OC in PCI Agent Mode (i.e. ENUM)
MC6	Output, 5 mA sink cap. (i.e. green RUN or general purpose LED)
MC7	Output, 5 mA sink cap. (i.e. red FAIL LED)
MC8	Input, (i.e. AGENT in PCI AGENT Mode)
MC9	Output, OC (i.e. HEALTHY in PCI AGENT Mode)
MC10	Output, OC (i.e. IREADY in PCI AGENT Mode)
MC11	Output, 5 mA sink cap. (i.e. Power Down Ack or LED)

4.1.4 Test and Programming Interface

The Test and Programming interface supports JTAG/DEBUG and ISP operations. This interface can be used for connecting hardware emulators and debuggers (e.g. BDM, COP, …), and for “in system programming” (ISP) of programmable hardware as well as in system testing (JTAG). It is comprised of a set of ten signals whereby some are common to all three interfaces and some are dedicated to only one.

The following table provides a listing of the Test and Programming interface signals and a brief description.

Table 6: Test and Programming Interface Signal Description

SIGNAL	DESCRIPTION
TCK	Test Clock in for JTAG/ISP and emulator/debugger
TDI	Test Data In for JTAG/ISP and emulator/debugger
TDO	Test Data Out JTAG/ISP and emulator/debugger
TMS	Test Mode Select, input for JTAG/ISP and emulator/debugger
TRST	Test Reset, input for JTAG/ISP and emulator/debugger
COP_HRST	Hard Reset, emulator/debugger hard reset In/Out
COP_SRST	Soft Reset, emulator/debugger soft reset In/Out
CKSTP_IN_/QACK/VFLS0	Status signal for BDM/COP emulator
CKSTP_OUT/VFLS1	Status signal for BDM/COP emulator
EMU_VCC	Reference Voltage of the JTAG/DEBUG core

4.1.5 Terminal and Console Interface

The E²Brain™ specification defines two serial interfaces for supporting a terminal port and a low speed communications interface for firmware updating. These interfaces are two signals wide and provide the standard UART protocol with XON/XOFF handshake protocol.

The following table provides a listing of the Terminal and Console interface signals and a brief description.

Table 7: Terminal and Console Interface Signal Description

SIGNAL	DESCRIPTION
TxD1, TxD2	Serial Transmit Data outputs, channel 1 and 2
RxD1, RxD2	Serial Receive Data signal inputs, channel 1 and 2

Note...

The corresponding serial signals on the E²Brain™ are TTL logic level signals.

4.1.6 I2C Interface

The E²Brain™ specification defines one I2C serial interfaces for supporting direct interfacing of E²Brain™ modules to carrier board devices. This interface is two signals wide.

The following table provides a listing of the I2C interface signals and a brief description.

Table 8: I2C Interface Signal Description

SIGNAL	DESCRIPTION
SCL	Serial Clock Line
SDA	Serial Data line

4.1.7 LPC Interface

The E²Brain™ specification defines one Low Pin Count (LPC) interface for supporting simple IOs, simple static memory devices, and IO controllers.

E²Brain™ provides therefore a 10-pin LPC interface according to Intel's Low Pin Count Interface Specification. Revision 1.0. In the case of PC (x-86) compatible E²Brain™ modules, the full LPC feature set can be implemented for example to connect Super IO or audio devices directly. In the case of non-x86 based E²Brain™ modules, just a useful subset of LPC functionality can be implemented by E²Brain™. The common denominator is the implementation of generic Memory Read/Write and IO Read/Write cycle types. Dedicated IRQs are provided by SERIRQ (serial IRQ).

In any case, the LPC interface on E²Brain™ modules peripheral devices to be connected in a very simple way either by directly interfacing their integrated LPC port or by translating the multiplexed LPC protocol into a very common static "SRAM-like" interface by programmable logic in front of the peripheral.

The following table provides a listing of the LPC interface signals and a brief description.

Table 9: LPC Interface Signal Description

SIGNAL	DESCRIPTION
LAD[0:3]	Multiplexed Command, Address, and Data lines
LFRAME#	Indicates start of a new cycle, termination of broken cycle
LRESET#	Same as PCI Reset
LPCCLK	33 MHz clock
SERIRQ	Serialized IRQ, optional for peripherals that need interrupt
LDRQ#	Encoded DMA/Bus Master Request, optional for peripherals

4.1.8 PCI Interface

In contrast to all other PCI based modules, E²Brain™ specifies both a PCI system controller mode and, optionally, a PCI agent mode. PCI agent mode can be selected by setting a static signal on the carrier board.

In system controller mode an E²Brain™ operates as the host, initializing and controlling up three PCI devices on the carrier, whereas, in the agent mode, the E²Brain™ itself operates as a PCI target. Thus, even more E²Brain™ modules can be combined to build one larger scalable PCI system. In this case one E²Brain™ is the PCI system controller and the others are intelligent subsystems working as PCI targets (agents).

The E²Brain™ specification defines a 32-bit PCI bus on Pn1. PCI and PCI-X bus speed (33/66/100/133) is determined by the module and is not limited by the E²Brain™ specification. PCI-X capability is indicated by a dedicated signal. The following table identifies the E²Brain™ PCI / PCI-X bus signals and provides a short description of each signal.

Table 10: PCI Interface Signal Description

SIGNAL	DESCRIPTION
AD [0:31]	PCI multiplexed address and data bus
INT [A, B, C, D]#	PCI interrupt requests
C/BE [0:3]#	PCI multiplexed bus command and byte enable
IRDY#	Initiator Ready indicates the current bus master is ready to complete the current data phase.
TRDY#	Target Ready indicates the selected device is ready to complete the current data phase.
PCI-RST#	PCI Reset signal
PCI-CLK-OUT- [0:2]	PCI clock Outputs for up to 3 external bus mastering PCI devices. All PCI signals except PCI_RST#, and INT [A, B, C, D] # are sampled on the rising edge. (Consider routing guidelines for the carrier board)
FRAME#	Indicate the beginning and duration of a PCI access.
STOP#	Indicates the target is requesting the master to stop the current transaction
DEVSEL#	Device select generated by the target when cycle refers to its own address.
REQ [0:2]#	PCI Arbiter requests
GNT [0:2]#	PCI Arbiter grants
PAR	Calculated/Checked Parity
PERR#	Parity Error
LOCK#	PCI Lock resource signal
SERR#	System Error
REQ64#	PCI request for a 64-bit access
ACK64#	PCI grant for a 64-bit access
PCI-CLK-IN	PCI clock input, used in agent mode
PCI-X	PCI-X Capability logic output, used in agent mode, 0 -> PCI-X capable
AGENT (MC8)	PCI-agent mode logic input, 0 -> PCI agent mode, 1 -> system controller

4.1.8.1 PCI Bus IDSEL Mapping and IRQ Routing

This specification recommends that the standard PCI enumeration and interrupt routing be in accordance with the following table.

Table 11: PCI Bus IDSEL Mapping and IRQ Routing

E²Brain™ PCI Device	PCI Device #	IDSEL (AD-line)	PCI Interrupt
E²Brain™ internal device	0	AD16	INTA
E²Brain™ internal device	1	AD17	INTB
E²Brain™ internal device	2	AD18	INTC
E²Brain™ internal device	3	AD19	INTD
E²Brain™ internal device	4	AD20	INTA
E²Brain™ internal device	5	AD21	INTB
reserved	6	AD22	INTC
reserved	7	AD23	INTD
reserved	8	AD24	INTA
reserved	9	AD25	INTB
E²Brain™ external device	10	AD26	INTC
E²Brain™ external device	11	AD27	INTD
E²Brain™ external device	12	AD28	INTA
reserved	13	AD29	INTB
reserved	14	AD30	INTC
reserved	15	AD31	INTD

4.1.8.2 Clock Distribution

Besides the onboard PCI clocks, E²Brain™ modules supply also the PCI clocks for external PCI devices. Due to the PCI specification there is a maximum allowed clock skew for all PCI devices. There are different values defined for the various PCI speeds:

- 33 MHz PCI: 2.0 ns max. clock skew
- 66 MHz PCI: 1.0 ns max. clock skew
- 133 MHz PCI-X: 0.5 ns max. clock skew

Since the actual clock skew is a function of the specific PCB design, clock skew must be taken into consideration by the complete system: E²Brain™ and carrier board. Therefore, E²Brain™ modules specify their onboard PCI clock delay and thus giving the resulting time budget for clock delay on the carrier board.

Example:

A typical E²Brain™ multilayer PCB based on FR4 has a signal delay of 180 ps per inch. The aligned onboard PCI trace lengths for internal PCI clocks would be 4 inches. The aligned onboard clock trace lengths for the external PCI clocks would be 2 inches.

- Onboard clock delays:

internal PCI clocks:	180*4 = 720 ps
onboard external PCI clocks:	200*2 = 360 ps

- Maximum trace length on carrier board (180ps/inch):

33 MHz PCI:	(2000+720-360)/180	=	13.1 in
66 MHz PCI:	(1000+720-360)/180	=	7.5 in
PCI-X:	(500+720-360)/180	=	4.7 in

4.2 System Interface Extension

The system Interface Extension Connector, Pn2, is used to provide CPU architecture specific system Interfaces. This can be either an extension for data path width or additional system interfaces.

In this section, the first two pinouts for the System Extension connector are introduced. The first connector pinout is used for expanding the PCI data path to 64-bit and the second pinout for providing CompactFlash connectivity.

4.2.1 PCI-64 Extension

This possibility for using the System Extension Connector, Pn2, provides a 64-bit PCI data-path to enhance the PCI bandwidth.

For this purpose the following signal groups are specified:

AD[32:63] PCI multiplexed address and data bus – extension to 64-bit

C/BE[4:7]# PCI multiplexed bus command and byte enable

PAR64# Parity Signal for 64-bit PCI extension

The following table provides pinout information for Pn2 for the PCI-64 extension.

Table 12: Pn2 Connector Pinout for PCI-64 Extension

SIGNAL	PIN	PIN	SIGNAL
GND	1	2	CBE7#
CBE6#	3	4	CBE5#
CBE4#	5	6	+3.3V
+3.3V	7	8	AD63
AD62	9	10	AD61
AD60	11	12	GND
GND	13	14	AD59
AD57	15	16	AD58
AD54	17	18	+3.3V
GND	19	20	AD56
AD52	21	22	AD55
AD50	23	24	GND
GND	25	26	AD53
AD48	27	28	AD51
AD46	29	30	GND
+3.3V	31	32	AD49
AD44	33	34	AD47
AD42	35	36	+3.3V
GND	37	38	AD45
AD40	39	40	AD43

SIGNAL	PIN	PIN	SIGNAL
AD38	41	42	GND
V(I/O)	43	44	AD41
AD36	45	46	AD39
AD34	47	48	GND
+3.3V	49	50	AD37
AD32	51	52	AD35
PAR64	53	54	GND
GND	55	56	AD33
	57	58	
	59	60	+3.3V
GND	61	62	
	63	64	
	65	66	GND
	67	68	
	69	70	
+3.3V	71	72	
	73	74	
	75	76	GND
	77	78	
	79	80	

4.2.2 CF/IDE, AC97, Graphic, and USB Options

Another usage of the Pn2 connector is to provide connectivity for typical system-on-chip interfaces like a CompactFlash/IDE interface, sound, graphic, and USB interfaces.

The recommended pinout can be divided into the following groups.

CF/IDE:

CF-CD1#	Compact Flash Card detection
CF-D[0:15]	Compact Flash / IDE data bus – 16-bit wide
CF-CS[0:1]#	Compact Flash / IDE chip select
CF-RD#	Compact Flash / IDE IO read strobe
CF-WR#	Compact Flash / IDE IO write strobe
CF-RST#	Compact Flash / IDE reset, active low
CF-INTRQ	Compact Flash / IDE interrupt request, active high
CF-IORDY	Compact Flash / IDE IO ready
CF-A[0:2]	Compact Flash / IDE address lines
CF-DASP#	Compact Flash / IDE Disk Active/Slave Present signal
CF-PDIAG#	Compact Flash / IDE Pass Diagnostic signal
CF-CS16#	Compact Flash / IDE word data transfer cycle signal, low active
CF-CD2#/ATA-CSEL#	Multiplexed: Compact Flash Card Detection signal / IDE: Cable select signal
ATA-DMARQ	IDE/ATA DMA request signal. Please refer to the ATA specification for more detail.
ATA-DMACK#	IDE/ATA DMA acknowledge signal. Please refer to the ATA specification for more detail.

Note:

The CompactFlash interface is realized as a true IDE interface. The PC CARD Memory Mode and the PC Card I/O Mode of the CompactFlash Specification are not supported.

In addition, the pinout for the CompactFlash / IDE Signals has been optimized for routing to a CompactFlash socket. The usage of these signals for IDE requires crossing of the signal lines.

Sound IF - AC97 Link:

AC97-Bit-Clk	Serial data Clock (12.288MHz)
AC97-SYNC	Fixed rate sample sync (48kHz)
AC97-SDATA_IN	Serial data in
AC97-SDATA_OUT	Serial data out

Graphic IFs:

Currently there are three different sets of pinouts defined for connecting the most often used graphic interfaces: CRT, Digital Flatpanel Port (DFP or simple LVDS) and Digital Visual Interface (DVI).

The DFP and the DVI interfaces use the same technology. They both use time multiplexing of the parallel color information: pixel clock and the sync impulses onto low voltage differential pairs. This technology is used to reduce the pin count of the digital display data.

For more information regarding multiplexing refer to appropriate documentation provided by National Semiconductor, Texas Instruments, the Digital Flat Panel Port (DFP) Specification, or the Digital Visual Interface (DVI) Specification.

DDC:

DDC-CLK	VESA DDC-Clock signal (Display Information)
DDC-DATA	VESA DDC-Data signal (Display Information)

The Display Data Channel (DDC) is a two wire interface between the graphics controller and the display, and it is used for display capability detection.

CRT:

CRT-R	CRT Red signal (analog): Red color information signal, terminated with 75 ohms
CRT-G	CRT Green signal (analog): Green color information signal, terminated with 75 ohms
CRT-B	CRT Blue signal (analog): Blue color information signal, terminated with 75 ohms
CRT-HSYNC	CRT horizontal synchronization pulse
CRT-VSYNC	CRT vertical synchronization pulse

If analog CRT signals are implemented, all required termination components must be realized on the E²Brain board.

LVDS:

LVDS-TxOut0+/-	LVDS differential pair 0
LVDS-TxOut1+/-	LVDS differential pair 1
LVDS-TxOut2+/-	LVDS differential pair 2
LVDS-TxClk+/-	LVDS differential pair clock line

DVI:

DVI-TxOut0+/-	DVI differential pair 0
DVI-TxOut1+/-	DVI differential pair 1
DVI-TxOut2+/-	DVI differential pair 2
DVI-TxOut2+/-	DVI differential pair 2

USB:

USB1+/-	Universal Serial Bus Port 1. These are the serial data pairs for the USB Port 1.
USB2+/-	Universal Serial Bus Port 2. These are the serial data pairs for the USB Port 2.
USB_OC	Over current condition indicator for host ports
USB_PO	Power ON/OFF control for host ports

The connector pinout described here defines two pairs of USB signals by meaning two USB Interfaces are fixed. The termination components of the USB signals are integrated on the E²Brain board.

The USB data signals should be routed as differential pairs.

The following table demonstrates the pinouts for the various configuration options as indicated above.

Table 13: Pn2 Connector Pinout for CF/IDE Options

CF + AC97 + USB			PIN	PIN	CF + AC97 + USB		
LVDS	DVI	CRT			CRT	DVI	LVDS
GND	GND	GND	1	2	CF_CD1#	CF_CD1#	CF_CD1#
CF_D3	CF_D3	CF_D3	3	4	CF_D11	CF_D11	CF_D11
CF_D4	CF_D4	CF_D4	5	6	+3.3V	+3.3V	+3.3V
+3.3V	+3.3V	+3.3V	7	8	CF_D12	CF_D12	CF_D12
CF_D5	CF_D5	CF_D5	9	10	CF_D13	CF_D13	CF_D13
CF_D6	CF_D6	CF_D6	11	12	GND	GND	GND
GND	GND	GND	13	14	CF_D14	CF_D14	CF_D14
CF_D7	CF_D7	CF_D7	15	16	CF_D15	CF_D15	CF_D15
CF_CS0#	CF_CS0#	CF_CS0#	17	18	+3.3V	+3.3V	+3.3V
GND	GND	GND	19	20	CF_CS1#	CF_CS1#	CF_CS1#
CF_RD#	CF_RD#	CF_RD#	21	22	CF_WR#	CF_WR#	CF_WR#
CF_INTRQ	CF_INTRQ	CF_INTRQ	23	24	GND	GND	GND
GND	GND	GND	25	26	CF_RST#	CF_RST#	CF_RST#
CF_IORDY	CF_IORDY	CF_IORDY	27	28	CF_A2	CF_A2	CF_A2
CF_A1	CF_A1	CF_A1	29	30	GND	GND	GND
+3.3V	+3.3V	+3.3V	31	32	CF_A0	CF_A0	CF_A0
CF_DASP#	CF_DASP#	CF_DASP#	33	34	CF_D0	CF_D0	CF_D0
CF_PDIAG#	CF_PDIAG#	CF_PDIAG#	35	36	+3.3V	+3.3V	+3.3V
GND	GND	GND	37	38	CF_D1	CF_D1	CF_D1
CF_D8	CF_D8	CF_D8	39	40	CF_D2	CF_D2	CF_D2
CF_D9	CF_D9	CF_D9	41	42	GND	GND	GND
V(I/O)	V(I/O)	V(I/O)	43	44	CF_CS16#	CF_CS16#	CF_CS16#
CF_D10	CF_D10	CF_D10	45	46	CF_CD2#/ATA-CSEL#	CF_CD2#/ATA-CSEL#	CF_CD2#/ATA-CSEL#
ATA_DMARQ	ATA_DMARQ	ATA_DMARQ	47	48	GND	GND	GND
+3.3V	+3.3V	+3.3V	49	50	ATA_DMACK#	ATA_DMACK#	ATA_DMACK#
AC97-BIT_CLK	AC97-BIT_CLK	AC97-BIT_CLK	51	52	AC97-SYNC	AC97-SYNC	AC97-SYNC
AC97-SDATA_IN	AC97-SDATA_IN	AC97-SDATA_IN	53	54	GND	GND	GND
GND	GND	GND	55	56	AC97-SDATA_OUT	AC97-SDATA_OUT	AC97-SDATA_OUT
		USB_OC	57	58			
		USB_PO	59	60	+3.3V	+3.3V	+3.3V
GND	GND	GND	61	62	DDC-Clk	DDC-Clk	DDC-Clk
LVDS TxOut0+	DVI-TxOUT0+	CRT-R	63	64	DDC-DATA	DDC-DATA	DDC-DATA
LVDS TxOut0-	DVI-TxOUT0-	CRT-G	65	66	GND	GND	GND
LVDS TxOut1+	DVI-TxOUT1+	CRT-B	67	68		DVI-TxCLK+	LVDS TxCLK+
LVDS TxOut1-	DVI-TxOUT1-	CRT-VSYN	69	70		DVI-TXCLK-	LVDS TxCLK-
+3.3V	+3.3V	+3.3V	71	72		Disp. ENAVDD	Disp. ENAVDD
LVDS TxOut2+	DVI-TxOUT2+	CRT-HSYN	73	74		Disp. ENABKL	Disp. ENABKL
LVDS TxOut2-	DVI-TxOUT2-		75	76	GND	GND	GND
USB1+	USB1+	USB1+	77	78	USB2+	USB2+	USB2+
USB1-	USB1-	USB1-	79	80	USB2-	USB2-	USB2-

4.2.3 High Bandwidth System Bus Options

Other pin layouts which define signal assignments for future high bandwidth busses like RapidIO, PCI-Express, etc. will be defined in the future and added to this document.

4.3 Communications Interface

The Communications Interface covers all interfaces which are provided by E²Brain™ modules as IO functions and makes them available to the carrier and for the system. This includes GND lines as well as signals for the different communications standards like HDLC, Ethernet, E1/T1, UTOPIA, CAN, etc..

The Communications Interface is comprised of two connectors: Pn3 with 80 pins and Pn4 for various optional COM Extensions with 140 pins. Pn4 is available only if there is an application requirement for it.

The signals on Pn3 are functionally grouped into:

- GND
- Serial
- TDM
- CAN
- Giga or Fast Ethernet with the respective LED signals

The signals on Pn4 are functionally grouped into:

- UTOPIA
- (G)MII
- R(G)MII

Note...

As different interfaces can be defined using the same pins, it depends on the actual configuration of the E²Brain™ module as to which function(s) are in fact available to the carrier board.

4.3.1 P3 Connector Pinout

The following table provides pinout information for three possible configuration variants for the Pn3 connector.

Table 14: Pinout of the Communications Interface Connector Pn3

VARIANT 1	VARIANT 2	VARIANT3	PINS		VARIANT 3	VARIANT 2	VARIANT 1
GND	GND	GND	1	2	GND	GND	GND
SER1_DSR	SCC1_TCLK/DSR	SCC1_TCLK/DSR	3	4	SCC1_RCLK/RI	SCC1_RCLK/RI	SER1_RI
SER1_RTS	SCC1_RTS	SCC1_RTS	5	6	SCC1_CTS	SCC1_CTS	SER1_CTS
SER1_TXD	SCC1_TXD	SCC1_TXD	7	8	SCC1_RXD	SCC1_RXD	SER1_RXD
SER1_DTR	SCC1_DTR	SCC1_DTR	9	10	SCC1_CD	SCC1_CD	SER1_CD
GND	GND	GND	11	12	SCC2_RCLK/RI	SCC2_RCLK/RI	SER2_RI
SER2_DSR	SCC2_TCLK/DSR	SCC2_TCLK/DSR	13	14	SCC2_CTS	SCC2_CTS	SER2_CTS
SER2_RTS	SCC2_RTS	SCC2_RTS	15	16	SCC2_RXD	SCC2_RXD	SER2_RXD
SER2_TXD	SCC2_TXD	SCC2_TXD	17	18	SCC2_CD	SCC2_CD	SER2_CD
SER2_DTR	SCC2_DTR	SCC2_DTR	19	20	TDMb_L1RCLK	SCC3_RCLK/RI	SER3_RI
SER3_DSR	SCC3_TCLK/DSR		21	22	GND	GND	GND
SER3_RTS	SCC3_RTS	TDMb_L1RQ	23	24	TDMb_L1TSYNC	SCC3_CTS	SER3_CTS
SER3_TXD	SCC3_TXD	TDMb_L1RXD	25	26	TDMb_L1TXD	SCC3_RXD	SER3_RXD
SER3_DTR	SCC3_DTR		27	28	TDMb_L1RSYNC	SCC3_CD	SER3_CD
SER4_DSR	SCC4_TCLK/DSR	SCC4_TCLK/DSR	29	30	TDMb_L1TCLK	SCC4_RCLK/RI	SER4_RI
SER4_RTS	SCC4_RTS	SCC4_RTS	31	32	SCC4_CTS	SCC4_CTS	SER4_CTS
SER4_TXD	SCC4_TXD	SCC4_TXD	33	34	SCC4_RXD	SCC4_RXD	SER4_RXD
SER4_DTR	SCC4_DTR	SCC4_DTR	35	36	SCC4_CD	SCC4_CD	SER4_CD
CAN2_TXD0	TDMa_L1TCLK	TDMa_L1TCLK	37	38	TDMa_L1CLKO	TDMa_L1CLKO	CAN2_RXD0
CAN2_TXD1	TDMa_L1TSYNC	TDMa_L1TSYNC	39	40	TDMa_L1RCLK	TDMa_L1RCLK	CAN2_RXD1
CAN1_TXD0	TDMa_L1TXD	TDMa_L1TXD	41	42	TDMa_L1RSYNC	TDMa_L1RSYNC	CAN1_RXD0
CAN1_TXD1	TDMa_L1RQ	TDMa_L1RQ	43	44	TDMa_L1RXD	TDMa_L1RXD	CAN1_RXD1
GND	GND	GND	45	46	GND	GND	GND
reserved	ETH3_ACT_LED		47	48		ETH3_LINK_LED	
ETH2_LINK_LED	ETH2_LINK_LED		49	50		ETH3_SPEED_LED	ETH2_1000_LED
ETH2_ACT_LED	ETH2_ACT_LED		51	52		ETH2_SPEED_LED	ETH2_100_LED
ETH2_SD	ETH2_SD		53	54	GND	GND	GND
ETH2_BIDC-	ETH3_T-		55	56		ETH3_R-	ETH2_BIDD-
ETH2_BIDC+	ETH3_T+		57	58		ETH3_R+	ETH2_BIDD+
ETH2_T-/BIDA-	ETH2_T-		59	60		ETH2_R-	ETH2_R-/BIDB-
ETH2_T+/BIDA+	ETH2_T+		61	62		ETH2_R+	ETH2_R+/BIDB+
2,5V	2,5V		63	64		2,5V	2,5V
ETH1_BIDC-	ETH1_BIDC-		65	66		ETH1_BIDD-	ETH1_BIDD-
ETH1_BIDC+	ETH1_BIDC+		67	68		ETH1_BIDD+	ETH1_BIDD+
ETH1_T-/BIDA-	ETH1_T-/BIDA-		69	70		ETH1_R-/BIDB-	ETH1_R-/BIDB-
ETH1_T+/BIDA+	ETH1_T+/BIDA+		71	72		ETH1_R+/BIDB+	ETH1_R+/BIDB+
GND	GND	GND	73	74		ETH1_SD	ETH1_SD
ETH1_LINK_LED	ETH1_LINK_LED		75	76		ETH1_1000_LED	ETH1_1000_LED
ETH1_ACT_LED	ETH1_ACT_LED		77	78		ETH1_100_LED	ETH1_100_LED
GND	GND	GND	79	80	GND	GND	GND

4.3.2 Ethernet Ports

The E²Brain™ modules provide up to three Ethernet ports whose signals are already at copper Ethernet transmission voltage levels (physical levels) for CAT5 cabling. So the carrier board needs to add only the galvanic isolation (magnetics) function and the appropriate transmission connector type.

Two of the three Ethernet ports are already prepared for Gigabit Ethernet transmission. A 2.5V power supply is also defined for applications where 2.5V is required for the magnetics devices.

Additionally, for monitoring and control purposes, LED functionality is provided to indicate activity, link, and speed status information for the respective ports.

Table 15: Ethernet Port Signal Type and Description

SIGNAL	DESCRIPTION
ETHn_T+/BIDA+	Transmit pair in 10BaseT/100BaseTX configuration
ETHn_T-/BIDA-	Channel A pair of Media Dependent Interface in 1000BaseT configuration
ETHn_R+/BIDB+	Receive pair in 10BaseT/100BaseTX configuration
ETHn_R-/BIDB-	Channel B pair of Media Dependent Interface in 1000BaseT configuration
ETHn_BIDC+	Channel C pair of Media Dependent Interface in 1000BaseT configuration
ETHn_BIDC-	
ETHn_BIDD+	Channel D pair of Media Dependent Interface in 1000BaseT configuration
ETHn_BIDD-	
2.5V	2.5V for magnetics transformer center tap

4.3.3 Synchronous/Asynchronous Serial Ports

Up to four, full modem, serial ports are available on the standard populated Pn3 connector. Eight signals per port are provided to realize either synchronous or asynchronous high speed serial links interfaced using dedicated Controlling/Handshaking. Therefore, all serial communications standards like RS232, RS422, RS485, HDLC, etc. are supported.

Table 16: Serial Port Signal Type and Description

SIGNAL	DESCRIPTION
SERn_TXD	Transmit data output
SERn_RXD	Receive data input
SERn_RTS/TXFRAME	Request to send output; transmit frame signal for synchronous transmission
SERn_CTS/RXFRAME	Clear to send input; receive frame signal for synchronous transmission
SERn_DTR	Data terminal ready output
SERn_CD	Carrier detect input
SERn_TCLK/DSR	Transmit clock for synchronous transmissions/Data set ready input
SERn_RCLK/RI	Receive clock for synchronous transmissions/Ring indicator input

Note...

All signals are available and supplied at TTL levels. Further signal conditioning via appropriate transceivers on the carrier board is required to support the respective communications standards.

4.3.4 TDM Ports

For special communications configurations, up to two Time Division Multiplexed (TDM) ports are supplied by the E²Brain™ modules. For example, E1/T1 or ISDN configurations are realizable over these ports. The eight signals to/from the E²Brain™ modules are all in TTL level and require additional signal conditioning by the carrier board depending on the physical needs of the chosen transmission standard.

Table 17: TDM Port Signal Type and Description

SIGNAL	DESCRIPTION
TDMa_L1TXD	Transmit data output
TDMa_L1RXD	Receive data input
TDMa_L1CLKO	Clock output from the serial TDM interface
TDMa_L1RQ	Request channel input signal
TDMa_L1TSYNC	Transmit sync input
TDMa_L1RSYNC	Receive sync input
TDMa_L1TCLK	Transmit clock for the serial TDM interface
TDMa_L1RCLK	Receive clock for the serial TDM interface

4.3.5 CAN Ports

To provide field bus support, there are pins available to implement two CAN bus ports on the Pn3 interface. The signals provided are at TTL voltage levels and must be adapted to the CAN bus levels through the use of appropriate CAN transceivers on the carrier board.

Table 18: CAN Port Signal Type and Description

SIGNAL	DESCRIPTION
CANn_TXD0	Transmit data output driver 0
CANn_RXD0	Receive data input channel 0
CANn_TXD1	Transmit data output driver 1
CANn_RXD1	Receive data input channel 1

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4.4 Communications Extension Interface

The Communications Extension Interface with 140 pins on an optionally populated connector is designed to provide further possibility for routing IO signals between the E²Brain™ modules and the carrier/external system. The Pn4 connector is designed for special interfaces which are in general not in standard use interfaces, but can be very useful or important for various applications.

The signals on Pn4 are functionally grouped into:

- (G)MII
- R(G)MII
- UTOPIA

Note...

Most pins on this connector are not specifically reserved for only one of the above mentioned interfaces. This means that it may not be possible to use all interfaces at the same time.

4.4.1 P4 Connector Pinout

The following table provides pinout information for three possible variant configurations of the Pn4 connector.

Table 19: Pinout of the Communications Interface Connector Pn4

VARIANT 1	VARIANT 2	VARIANT 3			VARIANT 3	VARIANT 2	VARIANT 1
GND	GND	GND	1	2	GND	GND	GND
UTP2_TXD1/RXD1	UTP2_TXD1/RXD1	GMII4_TXD6	3	4	GMII4_TXD7	UTP2_TXD0/RXD0	UTP2_TXD0/RXD0
UTP2_TXD3/RXD3	UTP2_TXD3/RXD3	GMII4_TXD4	5	6	GMII4_TXD5	UTP2_TXD2/RXD2	UTP2_TXD2/RXD2
UTP2_TXD5/RXD5	UTP2_TXD5/RXD5	(G)MII4_TXD2	7	8	(G)MII4_TXD3	UTP2_TXD4/RXD4	UTP2_TXD4/RXD4
UTP2_TXD7/RXD7	UTP2_TXD7/RXD7	(G)MII4_TXD0	9	10	(G)MII4_TXD1	UTP2_TXD6/RXD6	UTP2_TXD6/RXD6
GND	GND	GND	11	12	GND	GND	GND
UTP2_RXD7	UTP2_RXD7	(G)MII4_RXD0	13	14	(G)MII4_RXD1	UTP2_RXD6	UTP2_RXD6
UTP2_RXD5	UTP2_RXD5	(G)MII4_RXD2	15	16	(G)MII4_RXD3	UTP2_RXD4	UTP2_RXD4
UTP2_RXD3	UTP2_RXD3	GMII4_RXD4	17	18	GMII4_RXD5	UTP2_RXD2	UTP2_RXD2
UTP2_RXD1	UTP2_RXD1	GMII4_RXD6	19	20	GMII4_RXD7	UTP2_RXD0	UTP2_RXD0
UTP2_TxAddr4	UTP2_TxAddr4	RESERVED	21	22	GND	GND	GND
UTP2_TxAddr3	UTP2_TxAddr3	(G)MII4_COL	23	24	(G)MII4_CRS	UTP2_RxAddr4	UTP2_RxAddr4
UTP2_TxAddr2	UTP2_TxAddr2	(G)MII4_TX_ER	25	26	(G)MII4_TX_EN	UTP2_RxAddr3	UTP2_RxAddr3
UTP2_TxAddr1	UTP2_TxAddr1	(G)MII4_RX_DV	27	28	(G)MII4_RX_ER	UTP2_RxAddr2	UTP2_RxAddr2
UTP2_TxAddr0	UTP2_TxAddr0	GMII4_GTX_CLK	29	30	RESERVED	UTP2_RxAddr1	UTP2_RxAddr1
RESERVED	TX_EN-A	MDIO4	31	32	(G)MII4_RxClk	UTP2_RxAddr0	UTP2_RxAddr0
RESERVED	GTX-CLK-A	MDClk4	33	34	GND	GND	GND
GND	GND	GND	35	36	(G)MII4_TxClk	RX_CLK-A	RESERVED
UTP2_TXD9/RXD9	TXD1-A	GMII3_TXD6	37	38	GMII3_TXD7	TXD0-A	UTP2_TXD8/RXD8
UTP2_TXD11/ RXD11	TXD3-A	GMII3_TXD4	39	40	GMII3_TXD5	TXD2-A	UTP2_TXD10/ RXD10
UTP2_TXD13/ RXD13	RX_DV-A	(G)MII3_TXD2	41	42	(G)MII3_TXD3	RXD0-A	UTP2_TXD12/ RXD12
UTP2_TXD15/ RXD15	RXD1-A	(G)MII3_TXD0	43	44	(G)MII3_TXD1	RXD2-A	UTP2_TXD14/ RXD14
GND	GND	GND	45	46	GND	GND	GND
UTP2_RXD15	RXD3-A	(G)MII3_RXD0	47	48	(G)MII3_RXD1	GTX-CLK-B	UTP2_RXD14
UTP2_RXD13	TXD0-B	(G)MII3_RXD2	49	50	(G)MII3_RXD3	TX_EN-B	UTP2_RXD12
UTP2_RXD11	TXD2-B	GMII3_RXD4	51	52	GMII3_RXD5	TXD1-B	UTP2_RXD10
UTP2_RXD9	TXD3-B	GMII3_RXD6	53	54	GMII3_RXD7	RX_CLK-B	UTP2_RXD8
RESERVED	RESERVED	RESERVED	55	56	GND	GND	GND
UTP2_TxEnb	UTP2_TxEnb	(G)MII3_COL	57	58	(G)MII3_CRS	UTP2_TxClav	UTP2_TxClav
UTP2_TxSOC/ RxSOC	UTP2_TxSOC/ RxSOC	(G)MII3_TX_ER	59	60	(G)MII3_TX_EN	UTP2_RxEnb	UTP2_RxEnb
UTP2_RxSOC	UTP2_RxSOC	(G)MII3_RX_DV	61	62	(G)MII3_RX_ER	UTP2_RxClav	UTP2_RxClav
RESERVED	RX_DV-B	MDIO3	63	64	(G)MII3_RxClk	UTP2_RxCLK	UTP2_RxCLK
RESERVED	RXD0-B	GMII3_GTX_CLK	65	66	GND	GND	GND
RESERVED	RXD1-B	MDClk3	67	68	(G)MII3_TxClk	UTP2_TxCLK/ RxCLK	UTP2_TxCLK/ RxCLK
GND	GND	GND	69	70	RESERVED	UTP2_RxPrty	UTP2_RxPrty

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Table 19: Pinout of the Communications Interface Connector Pn4

VARIANT 1	VARIANT 2	VARIANT 3			VARIANT 3	VARIANT 2	VARIANT 1
RESERVED	RXD2-B	GMII2_GTX_CLK	71	72	GMII2_125CLK	UTP2_TxPrty	UTP2_TxPrty
RESERVED	RXD3-B	RESERVED	73	74	RESERVED	RESERVED	RESERVED
RESERVED	RESERVED	GMII1_125CLK	75	76	GMII2_TXD7	UTP1_TXD0/RXD0	UTP1_TXD0/RXD0
RESERVED	RESERVED	RESERVED	77	78	GMII2_TXD5	UTP1_TXD2/RXD2	UTP1_TXD2/RXD2
UTP1_TXD1/RXD1	UTP1_TXD1/RXD1	GMII2_TXD6	79	80	GND	GND	GND
GND	GND	GND	81	82	(G)MII2_TXD3	UTP1_TXD4/RXD4	UTP1_TXD4/RXD4
UTP1_TXD3/RXD3	UTP1_TXD3/RXD3	GMII2_TXD4	83	84	(G)MII2_TXD1	UTP1_TXD6/RXD6	UTP1_TXD6/RXD6
UTP1_TXD5/RXD5	UTP1_TXD5/RXD5	(G)MII2_TXD2	85	86	(G)MII2_RXD1	UTP1_RXD6	UTP1_RXD6
UTP1_TXD7/RXD7	UTP1_TXD7/RXD7	(G)MII2_TXD0	87	88	(G)MII2_RXD3	UTP1_RXD4	UTP1_RXD4
UTP1_RXD7	UTP1_RXD7	(G)MII2_RXD0	89	90	GND	GND	GND
UTP1_RXD5	UTP1_RXD5	(G)MII2_RXD2	91	92	GMII2_RXD5	UTP1_RXD2	UTP1_RXD2
UTP1_RXD3	UTP1_RXD3	GMII2_RXD4	93	94	GMII2_RXD7	UTP1_RXD0	UTP1_RXD0
UTP1_RXD1	UTP1_RXD1	GMII2_RXD6	95	96	(G)MII2_CRS	UTP1_RxAddr4	UTP1_RxAddr4
UTP1_TxAddr4	UTP1_TxAddr4	(G)MII2_COL	97	98	(G)MII2_TX_EN	UTP1_RxAddr3	UTP1_RxAddr3
UTP1_TxAddr3	UTP1_TxAddr3	(G)MII2_TX_ER	99	100	(G)MII2_RxClk	UTP1_RxAddr2	UTP1_RxAddr2
UTP1_TxAddr2	UTP1_TxAddr2	(G)MII2_RX_DV	101	102	GND	GND	GND
UTP1_TxAddr1	UTP1_TxAddr1	MDIO2	103	104	(G)MII2_TxClk	UTP1_RxAddr1	UTP1_RxAddr1
GND	GND	GND	105	106	(G)MII2_RX_ER	UTP1_RxAddr0	UTP1_RxAddr0
UTP1_TxAddr0	UTP1_TxAddr0	MDClk2	107	108	GMII1_TXD7	UTP1_TXD8/RXD8	UTP1_TXD8/RXD8
UTP1_TXD9/RXD9	UTP1_TXD9/RXD9	GMII1_TXD6	109	110	GMII1_TXD5	UTP1_TXD10/ RXD10	UTP1_TXD10/ RXD10
UTP1_TXD11/ RXD11	UTP1_TXD11/ RXD11	GMII1_TXD4	111	112	(G)MII1_TXD3	UTP1_TXD12/ RXD12	UTP1_TXD12/ RXD12
UTP1_TXD13/ RXD13	UTP1_TXD13/ RXD13	(G)MII1_TXD2	113	114	GND	GND	GND
GND	GND	GND	115	116	(G)MII1_TXD1	UTP1_TXD14/ RXD14	UTP1_TXD14/ RXD14
UTP1_TXD15/ RXD15	UTP1_TXD15/ RXD15	(G)MII1_TXD0	117	118	(G)MII1_RXD1	UTP1_RXD14	UTP1_RXD14
UTP1_RXD15	UTP1_RXD15	(G)MII1_RXD0	119	120	(G)MII1_RXD3	UTP1_RXD12	UTP1_RXD12
UTP1_RXD13	UTP1_RXD13	(G)MII1_RXD2	121	122	GMII1_RXD5	UTP1_RXD10	UTP1_RXD10
UTP1_RXD11	UTP1_RXD11	GMII1_RXD4	123	124	GND	GND	GND
UTP1_RXD9	UTP1_RXD9	GMII1_RXD6	125	126	GMII1_RXD7	UTP1_RXD8	UTP1_RXD8
RESERVED	RESERVED	(G)MII1_COL	127	128	(G)MII1_CRS	UTP1_TxClav	UTP1_TxClav
UTP1_TxEnb	UTP1_TxEnb	(G)MII1_TX_ER	129	130	(G)MII1_TX_EN	UTP1 RxEnb	UTP1 RxEnb
UTP1_TxSOC/ RxSOC	UTP1_TxSOC/ RxSOC	(G)MII1_RX_DV	131	132	(G)MII1_RX_ER	UTP1_RxClav	UTP1_RxClav
UTP1_RxSOC	UTP1_RxSOC	MDIO1	133	134	(G)MII1_RxClk	UTP1_RxCLK	UTP1_RxCLK
UTP1_RxPrty	UTP1_RxPrty	GMII1_GTX_CLK	135	136	GND	GND	GND
UTP1_TxPrty	UTP1_TxPrty	MDClk1	137	138	(G)MII1_TxClk	UTP1_TxCLK/ RxCLK	UTP1_TxCLK/ RxCLK
GND	GND	GND	139	140	GND	GND	GND

4.4.2 (G)MII I/F Option

The Media Independent (MII) Interface provides all signals from a Media Access Controller (MAC). These means that these signals will be supplied at TTL levels and can be further processed on the carrier board for example, for Ethernet copper or fiber transmission. Because the physical adaptation to a transmission medium/protocol is made on the carrier, the MACs on the E²Brain™ modules can be used very flexibly and in any kind of application system supporting/processing MII.

Even Gigabit speeds are supported which are indicated by the pins with (G)MII labeling.

Table 20: (G)MII Signal Type and Description

SIGNAL	DESCRIPTION
(G)MIIn_TXD[0...3]	Transmit data output for MII and GMII
(G)MIIn_RXD[0...3]	Receive data input for MII and GMII
GMIIn_TXD[4...7]	Transmit data output for GMII
GMIIn_RXD[4...7]	Receive data input for GMII
(G)MIIn_TX_EN	Transmit enable output
(G)MIIn_TX_ER	Transmit coding error output
(G)MIIn_TX_CLK	Transmit clock input
(G)MIIn_RX_ER	Receive error input
(G)MIIn_RX_DV	Receive data valid input
(G)MIIn_RX_CLK	Receive clock input
(G)MIIn_COL	Collision detected input
(G)MIIn_CRS	Carrier sense input
MDIOn	Management data input and output for Ethernet PHYs
MDCIkn	Management data clock output for Ethernet PHYs
GMIIn_GTX_CLK	Transmit clock input
GMIIn_125CLK	Gigabit transmit clock input

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4.4.3 RGMII I/F Option

Similar to the (G)MII interface option described under 4.4.2 is the RGMII interface which stands for Reduced Gigabit Media Independent Interface.

With 12 pins per port compared to 24 pins per port in Gigabit “normal” MII configuration it requires only half the number of signals of the GMII interface.

Table 21: RMII Signal Type and Description

SIGNAL	DESCRIPTION
RGMIIn_TXD[0...3]	Transmit data output for RGMII
RGMIIn_RXD[0...3]	Receive data input for RGMII
RGMIIn_Tx_EN	Transmit enable output
RGMIIn_Tx_CLK	Transmit clock input
RGMIIn_Rx_DV	Receive data valid input
RGMIIn_Rx_CLK	Receive clock input

4.4.4 UTOPIA I/F Option

The E²Brain™ concept supports via the optional Pn4 connector also the ATM protocol realized over UTOPIA or UTOPIA II interfaces. The UTOPIA interfaces can either be realized 8 or 16-bit wide depending on the processor and pin count resources used on the E²Brain™ module.

The UTOPIA connector interface on the E²Brain™ modules are designed to support full duplex on both sides: the master (ATM) side and the slave (PHY) side. Also Multi-PHY operation in the so called multiplexed polling mode is supported. One master can in this case address up to 31 PHY devices.

All signals from/to the E²Brain™ modules are in TTL level and must be transformed to UTOPIA levels with appropriate PHYs on the carrier board.

Table 22: UTOPIA Signal Type and Description

SIGNAL	DESCRIPTION
UTPn_TXD[0...7]	Transmit data output for 8 and 16-bit UTOPIA
UTPn_RXD[0...7]	Receive data input for 8 and 16-bit UTOPIA
UTPn_TXD[8...15]	Transmit data output for 16-bit UTOPIA
UTPn_RXD[8...15]	Receive data input for 16-bit UTOPIA
UTPn_TxEnb#	Transmit enable output signal
UTPn_TxClav	Transmit cell available input signal
UTPn_TxSOC	Transmit start of cell output signal
UTPn_TxCLK	Transmit clock output signal
UTPn_TxPrty	Transmit parity output signal
UTPn_RxEnb#	Receive enable output signal
UTPn_RxClav	Receive cell available input signal
UTPn_RxSOC	Receive start of cell input signal
UTPn_RxCLK	Receive clock input signal
UTPn_RxPrty	Receive parity input signal
UTPn_TxAddr[0...4]	Transmit address output signals
UTPn_RxAddr[0...4]	Receive address output signals