EBC3

E²Brain Module Carrier for the EB8347 CPU

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User Guide

kontron

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Please refer also to the section “High Voltage Safety Instructions” on the following page.

ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.

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High Voltage Safety Instructions

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Special Handling and Unpacking Instructions

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Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

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In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

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Chapter 1

Introduction

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1. Introduction

The E²Brain™ module described in this guide is designed to Kontron's "E²Brain™ Module Specification", revision 01. Section 1.1 provides general information regarding this specification and the system environment as envisioned for E²Brain™ modules. For more detailed information regarding the "E²Brain™ Module Specification", please contact Kontron.

The remaining sub-sections of the Introduction provide more specific details of the EBC3 E²Brain™ module itself to familiarize the user with this product as a whole.

1.1 The E²Brain™ Concept

The E²Brain™ concept is a highly flexible approach to providing application developers with the ability to concentrate on the definition of application requirements without having to continuously factor in potential restrictions concerning available data processing and communications functionality.

More specific, data processing and communications requirements become a function of the application and not vice versa. This is possible through the implementation of the E²Brain™ concept. Unlike other approaches to providing application solutions, the E²Brain™ concept concentrates on the most essential aspects of providing data processing and communications without attempting to provide in one entity a complete, self-contained computer system.

The E²Brain™ specification first of all defines a PCB module with a form factor of 115 x 75 x 11.6 millimeters. For interfacing with applications, the specification calls for up to four connectors which provide not only interfacing capability for current industry standards but also for future standards or application specific requirements. The type, location, and usage of these connectors is also defined in the specification so as to guarantee standardized compatibility. The specification is open as to the data processing and communications functionality to be implemented which is by definition a function of the application requirements. In addition, the specification envisions considerations for thermal energy dissipation through the implementation of what are known as BrainCAP™s (E²Brain™ **C**ooling **A**ssembly, **P**rotector) which can range from heat spreaders to highly sophisticated heat sink cooling designs.

The key features of the E²Brain™ concept are:

- very compact and robust form factor
- independent of CPU architecture
- scalable, flexible, and open system interface
- PCI Master and Agent Mode
- PCI-64 and PCI-X capability
- versatile and very powerful communications interfaces
- complete thermal design concept

1.1.1 E²Brain™ Functionality

E²Brain™ (Embedded Electronic Brain) is a new platform architecture for advanced computer modules. The E²Brain™ specification defines a very compact mechanical form factor and a comprehensive set of functional interfaces which can be adapted to a wide variety of applications. E²Brain™ modules provide complete computer cores integrating a high-performance CPU, system memory and - typical for E²Brain™ - advanced communications controllers. E²Brain™ modules are plugged into customized backplanes or standardized carrier boards which themselves provide the physical interfaces (PHYs) and connectors, power, and addition-

al IO controllers. Through the use of E²Brain™ modules the system developer is relieved of the task of designing computers, and, instead, they permit him to concentrate on the specific product development.

E²Brain™ is a computer platform dedicated not just to one architecture like the PC and Windows architecture, but it is open for all architectures including PowerPC, ARM, SH, x86, and others. E²Brain™ modules are very suitable for “deeply” embedded applications requiring flexible computing power combined with versatile and high-performance communications power.

Although typical E²Brain™ modules are designed to be low power consumption devices, they are part of a well thought out thermal design concept which considers the thermal aspects right from the beginning. Where higher power consumption is unavoidable, E²Brain™ modules are fitted with appropriate BrainCAP™s. By utilizing BrainCAP™s, cooling, mechanical stabilization, and EMI protection are combined in a single concept to satisfy almost any application requirement.

1.1.2 Basic Architecture

The following figure illustrates the basic functional architecture of E²Brain™ modules. Common to all E²Brain™ modules are the data processing and communications core and the system and communications interfaces.

The application requirements determine the functionality required of the E²Brain™ module core which in turn mandates the functionality to be provided by the system and communications interfaces. Both of these interfaces are comprised of a base set and an extended set of functional features.

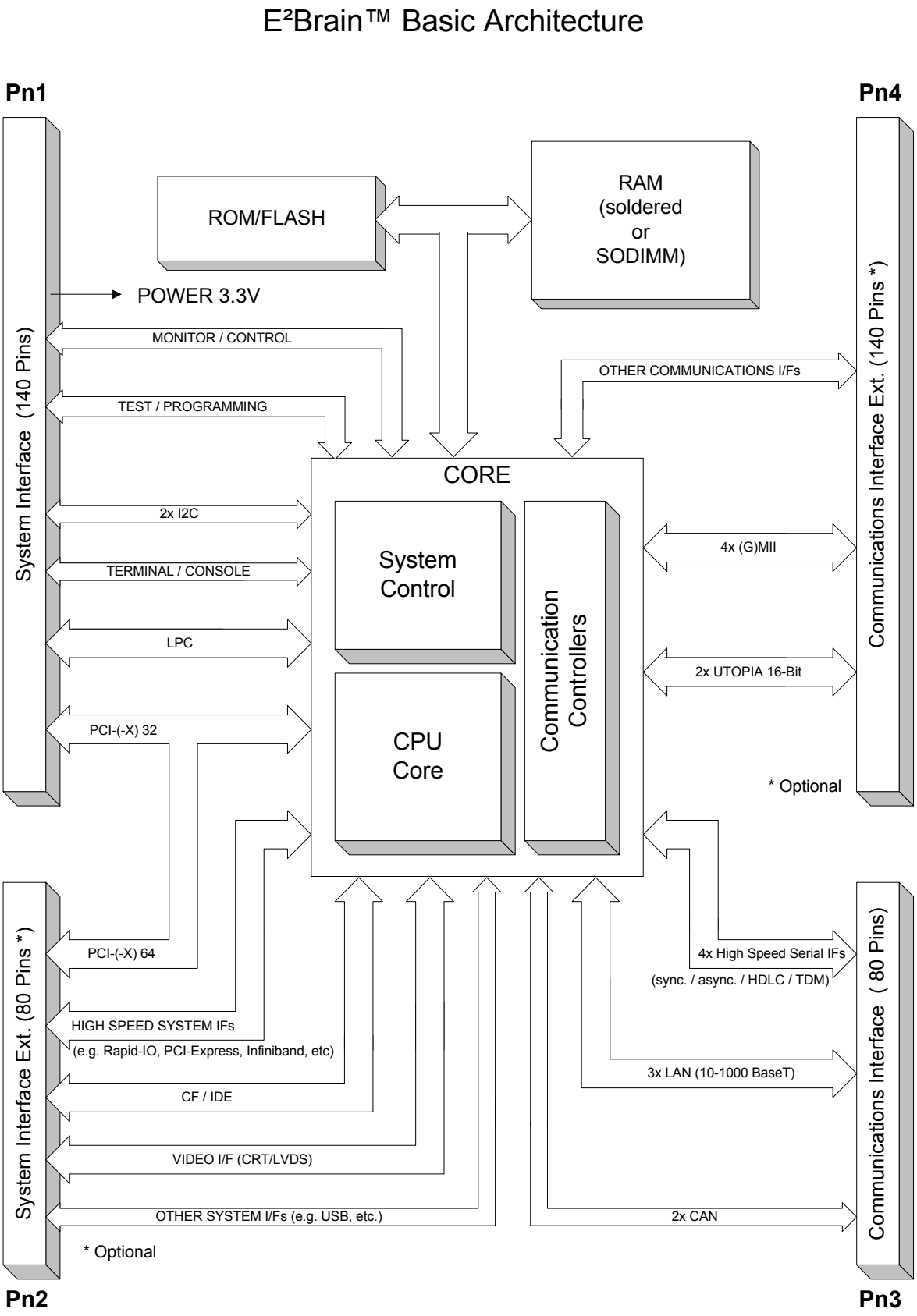
The system interface to the application is accomplished through connectors Pn1 and Pn2. Connector Pn1 provides the base set of system interfacing and Pn2 the extended set. If the application does not require extended system interfacing, it is not necessary to populate connector Pn2. The same analogy applies to the communications interfacing whereby connector Pn3 provides the base set of communications interfacing and Pn4 the extended set. Pn4 is not required to be populated if there is not an application requirement for it. This concept together with a corresponding core provides a maximum of scalability and flexibility to satisfy the most demanding of applications.

1.1.3 E²Brain™ System Environment

The E²Brain™ module form factor and mechanical and electrical interfacing are so conceived as to allow the use of E²Brain™ modules in practically any kind of system environment. These mezzanine modules can easily be integrated on most standardized carrier boards (VME, CompactPCI, PC PCI, etc.) as well as any other conceivable type of carrier board capable of providing the required mechanical and electrical infrastructure.

In addition to this infrastructure, thermal energy dissipation requirements must be taken into consideration when implementing applications using E²Brain™ modules. The E²Brain™ concept basically calls for modules to provide their own thermal energy dissipation. It may, however, be necessary to add additional thermal energy dissipation capability depending on the overall system environment. To satisfy such requirements, E²Brain™ modules may be equipped with specially designed cooling devices that are adapted to the specific system environment.

Figure 1-1: E²Brain™ Basic Architecture



1.2 EBC3 System Overview

The EBC3 is a special purpose E²Brain™ module carrier board which is designed to provide customers with a platform for the development of their own applications based on Kontron's EB8347 high performance processor module. This carrier board takes advantage of an extensive range of the many features offered by this module thus allowing developers to become familiar with their capabilities without having to first invest time and engineering resources in the development of an operational test environment.

In addition to supporting application development for the E²Brain™ modules themselves, the EBC3 can also be used as a model for the development of application specific carrier boards.

Designed as part of an overall system development kit, the EBC3 provides a comprehensive set of industry standard interfacing as well as test and programming interfaces. Coupled with EB8347 E²Brain™ module, board support package (BSP), and operating system it is an ideal starting basis for rapid efficient system application design and integration.

1.3 Product Overview

The EBC3 E²Brain™ carrier board is a part of an innovative concept to provide system integrators with a complete range of off-the-shelf as well as custom embedded computer cores for the most demanding of applications.

This carrier board which supports only the EB8347 E²Brain™ module as its computer core provides a comprehensive set of standard computer functionality coupled with industry standard system and communications I/O capability.

The following table provides a quick overview of the EBC3 board.

Table 1-1: EBC3 Product Overview

EBC3 FEATURES	DESCRIPTION
Product Type	E²Brain™ module carrier board: • Core Processor type supported: • EB8347 • Form factor: 244 mm x 244 mm (micro ATX) • Complies with the E²Brain™ specification
I/O Interfaces	System: • I²C bus • LPC bus • PCI-bus • Serial: terminal and console • USB • CompactFlash (Local Bus Data) • Digital I/O • EEPROM • LPC Flash • Audio (AC97) • CRT • SPI
I/O Interfaces	Communications: • Serial: high speed UART • Giga Ethernet (Three Speed: 10 / 100 / 1000 Mbps) • TMDS • TTL flat panel • Zoom video • PWM • GPIO / Local Bus Address
Other	Test and Programming: • EB8347 JTAG/DEBUG • EBC3 logic

Table 1-1: EBC3 Product Overview

EBC3 FEATURES	DESCRIPTION
Other	Monitor and Control: • Seven segment LED displays • Signal inputs and outputs • LEDs • Switches • Jumpers

1.4 Board Overview

1.4.1 Board Introduction

The EBC3 is a custom simplified application interface (SAI) for EB8347 high performance mezzanine computer module. It provides physical accommodations for mounting one E²Brain™ module and a comprehensive set of interfaces for application development.

1.4.2 Board Specific Information

Major board components of the EBC3 E²Brain™ SAI board are:

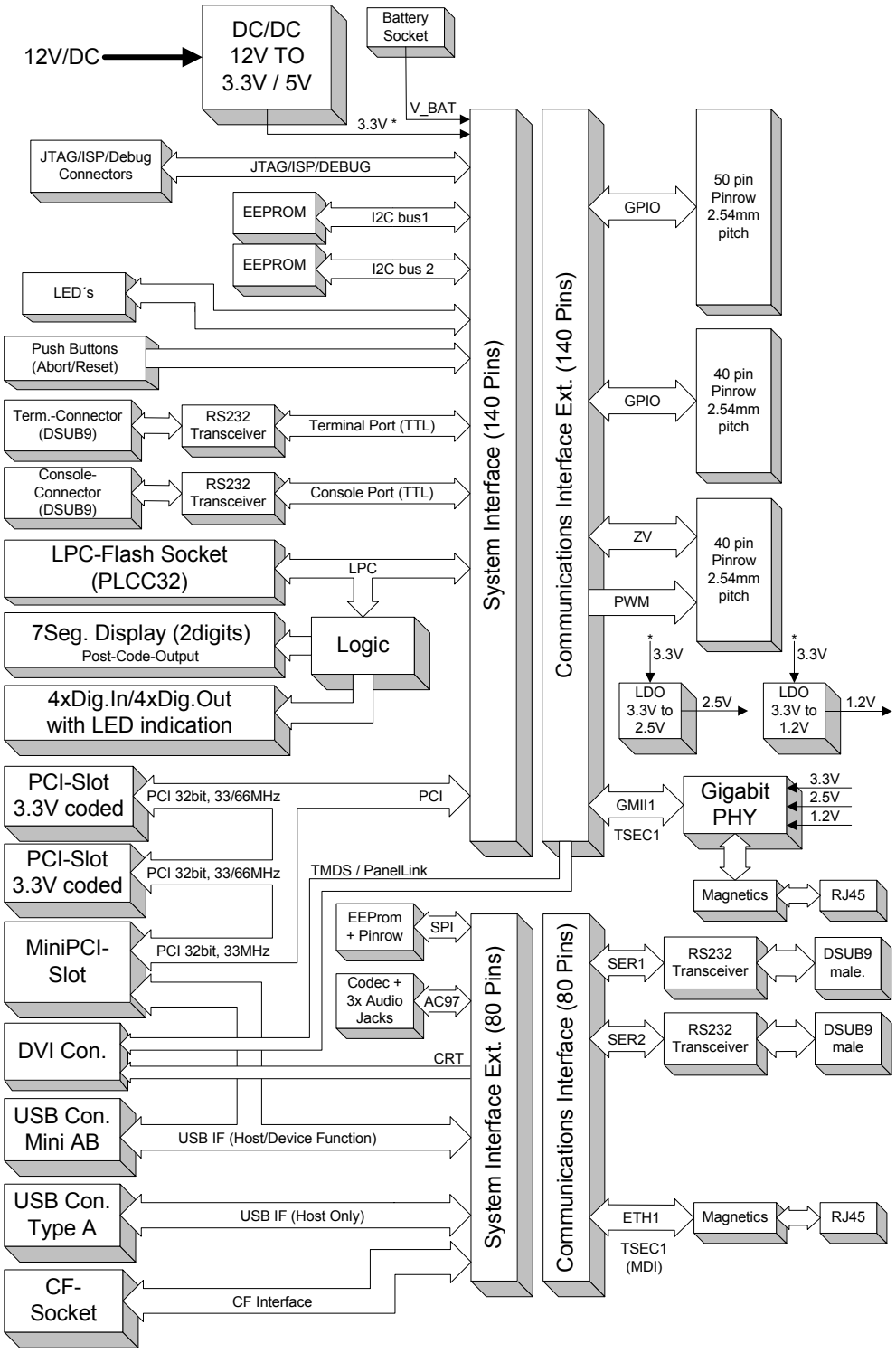
- Logic controller for digital IO and POST code display
- Two I2C EEPROMs (one for each I2C bus)
- Computer core interface: two system connectors and two communications connectors
- PCI interface (two PCI slots and one MiniPCI slot)
- Low Pin Count (LPC) interface
- I²C interfaces (to EEPROMs only)
- High speed serial interfaces:
  - Two RS232 with RTS/CTS handshaking
  - Two RS232 only (no hardware handshaking)
- Two Giga Ethernet interfaces (Three Speed Ethernet)
- Two USB interfaces
- Four digital input interfaces and four digital output interfaces (non-opto-isolated)
- LPC Flash interface (PLCC32)
- CompactFlash interface (Type I/II, Hitachi Microdrive)
- GPIO / Local Bus Address interface
- TTL flat panel interface with extensions
- Audio (AC97) intefaces (MIC, LINE IN, LINE OUT)
- DVI interface (TMDS, CRT)
- Zoom Video / PWM interface
- One debugging interface
- One programming interface
- Monitor and control interfaces
  - Two, seven segment LED displays
  - Eighteen single LEDs
  - Various jumpers
  - Two push button switches
  - One eight pole DIP switch
- DC/DC power supply

1.5 Board Diagrams

The following sections provide diagrams along with additional information concerning board functionality and component layout.

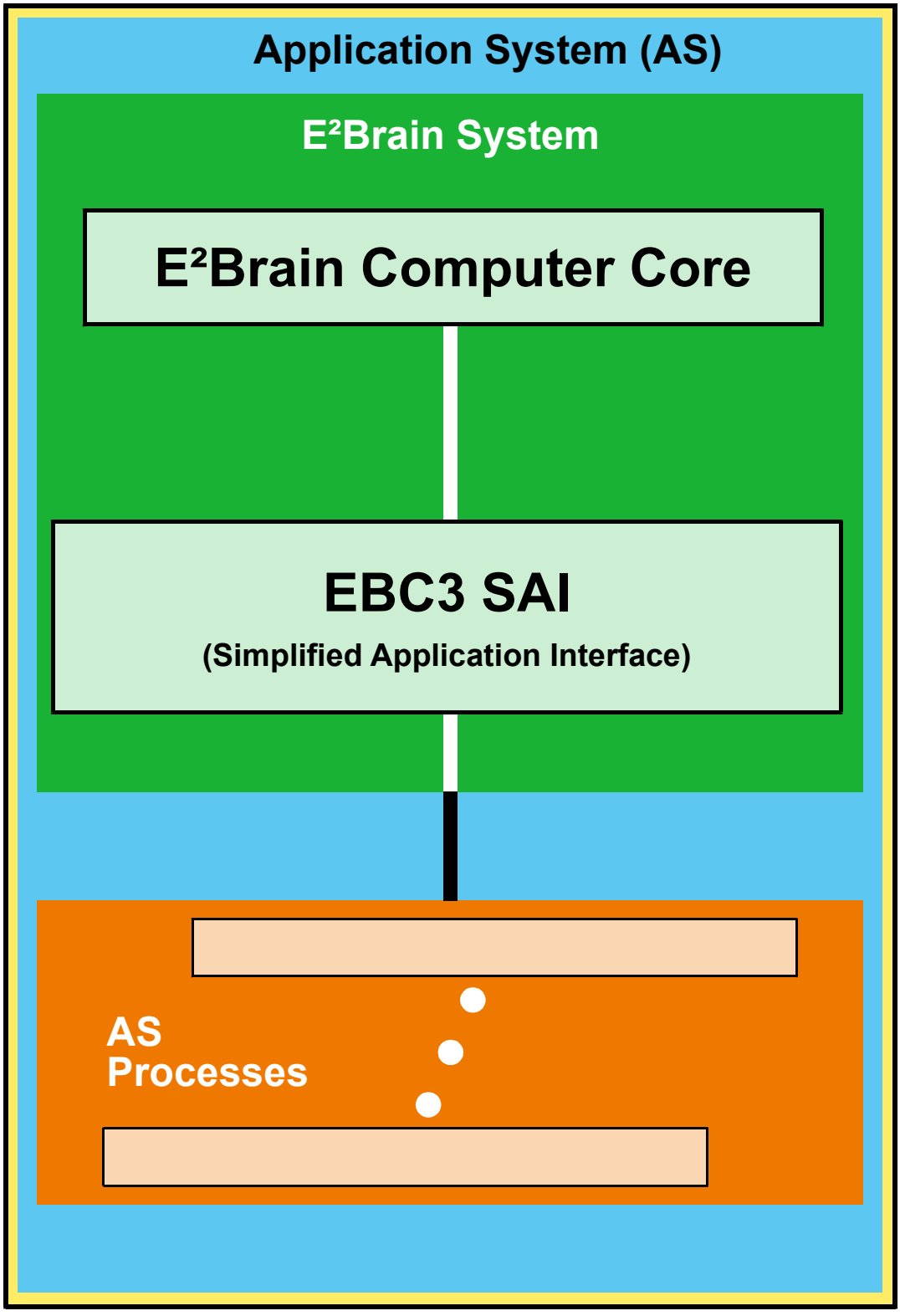
1.5.1 Board Architecture

Figure 1-2: EBC3 Basic Architecture



1.5.2 Application System Interfacing

Figure 1-3: EBC3 Application System Interfacing Diagram



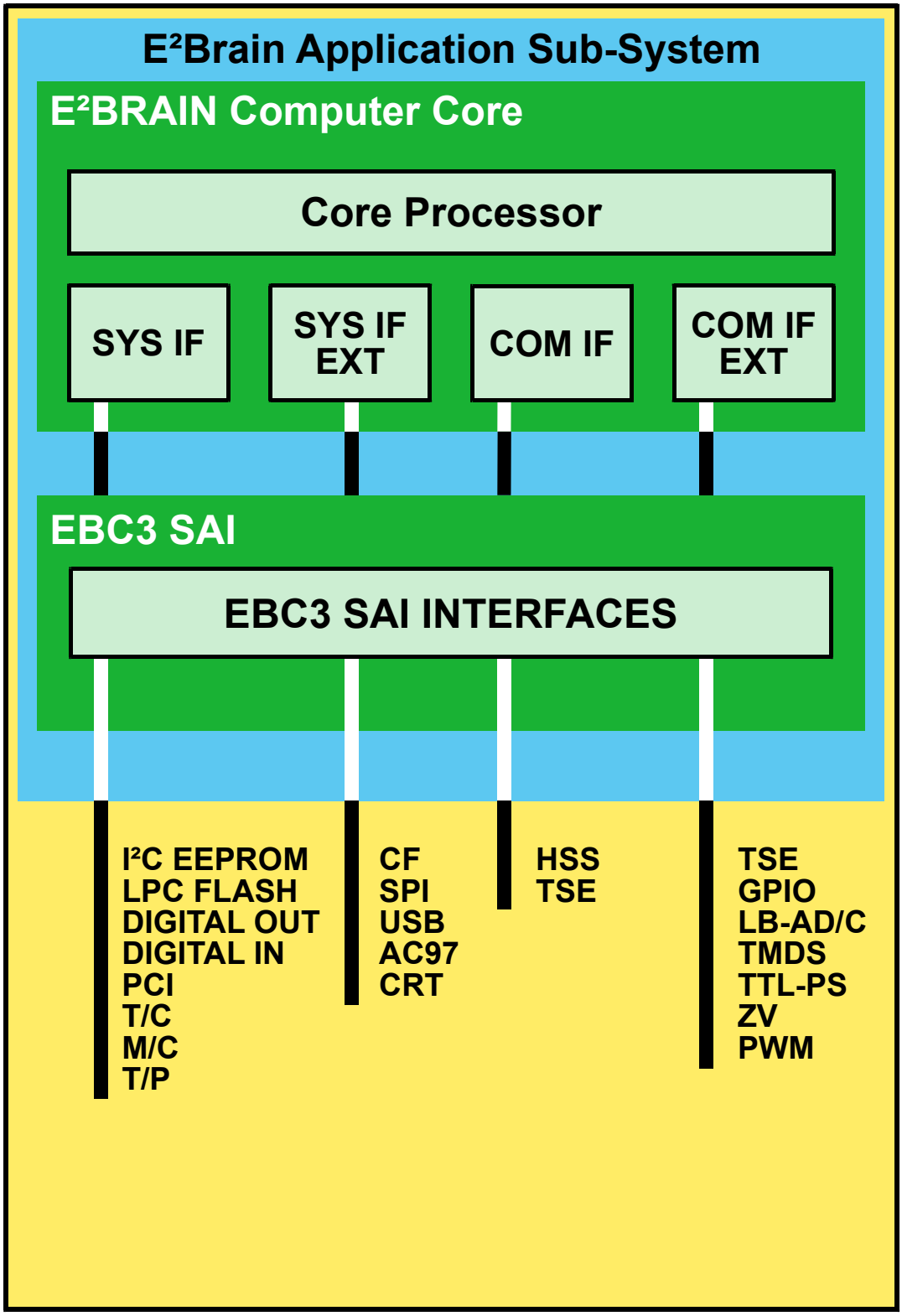
1.5.3 System Level Interfacing

An E²Brain™ application sub-system is comprised of an E²Brain™ computer core and a simplified application interface (SAI). In this case, the EBC3 is the SAI, whereby its application functionality is to support E²Brain™ solutions development. The interfaces available on the EBC3 are representative of typical E²Brain™ application requirements and are best suited for application development. The following figure demonstrates the basic interfacing relationship of the E²Brain™ module to the EBC3 SAI. The following table provides a legend for Figure 3.

Table 1-2: Legend for Figure 3

ITEM	DESCRIPTION
AC97	Audio interfaces
CF (LB-DATA)	CompactFlash (Local bus data) interface
CRT	CRT display interface (analog via DVI connector)
DIGITAL IN	Digital input interfaces
DIGITAL OUT	Digital output interfaces
GPIO / LB-AD/C	General purpose input / output interfaces or local bus address and control interfaces
HSS	High speed serial interfaces
I²C EEPROM	I²C interfaces EEPROMs are installed for application development usage
Local Bus	Expansion bus
LPC Flash	Low Pin Count Flash Supports PLCC32 socket.
M/C	Monitor / Control interfaces
PCI	PCI interfaces Two standard PCI connectors plus one mini-PCI connector
PWM	Pulse width modulated signal interface (flat panel brightness control)
SPI	Serial peripheral interface
T/C	Terminal / Console interfaces Serial interface for terminal/console type operations (RS232)
T/P	Test / Programming interfaces JTAG / DEBUG and programming
TMDS	Transition Minimized Differential Signal interface (DVI)
TSE	Three Speed Ethernet interfaces
TTL-PS	TTL flat panel signal interface
USB	Universal serial bus interfaces
ZV	Zoom video interface

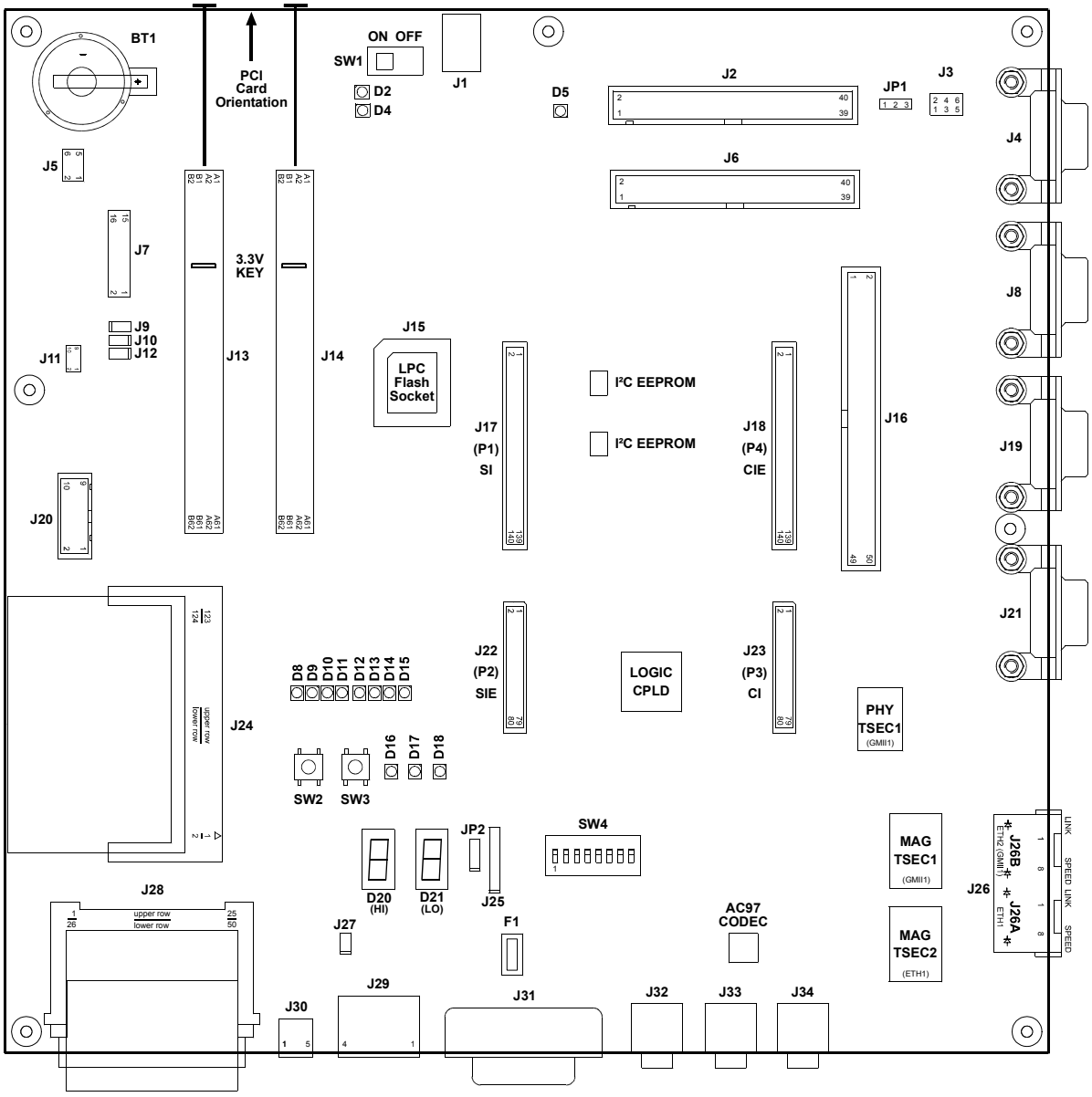
Figure 1-4: EBC3 System Level Interfacing Diagram



1.5.4 Board Layout

The following figures illustrate the positioning of the interfaces and monitor and control elements on the EBC3 carrier board. The accompanying table provides an ordered listing of these items along with a short description. For further information refer to section 2.

Figure 1-5: EBC3 Board (Front View)



WARNING!

The J13 and J14 connectors are 3.3V coded. Only 3.3V or universally coded cards may be used with this connector. Do not attempt to install 5V coded cards as this will result in damage to the PCI card, the EBC3, or the E²Brain™ module itself.

The EBC3 is configured for 3.3V V(I/O) operation which supports the EB8347 module. The EBC3 is not configurable for 5V V(I/O).

Figure 1-6: EBC3 Board Layout

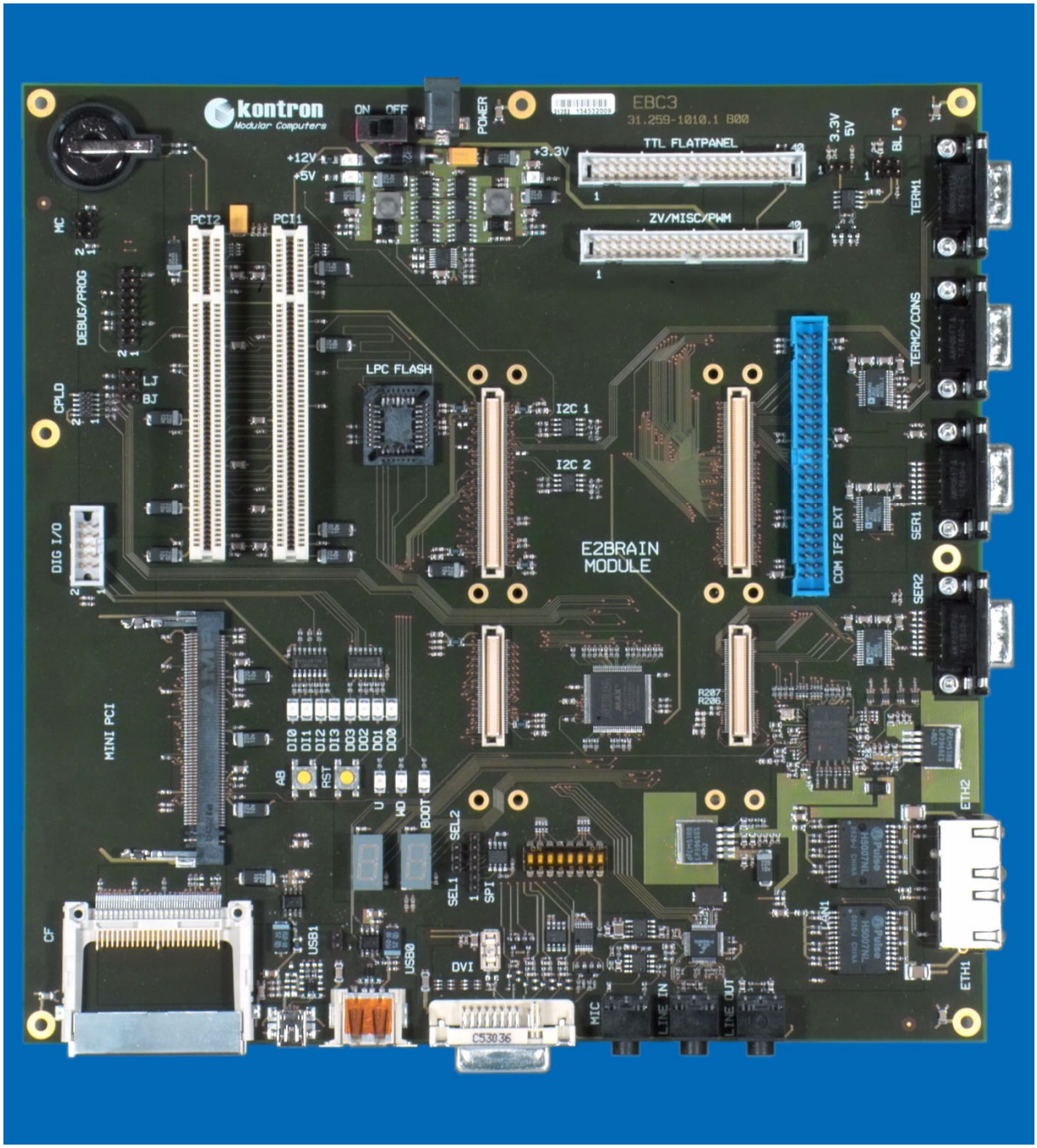


Table 1-3: EBC3 Interfaces and MC Elements

IF / MCE	ALIAS	DESCRIPTION
BT1		Backup battery for RTC, SRAM, etc.
D2	12V	LED, green, indicates 12V input power is applied
D4	5V	LED, green, indicates 5V power is applied
D5	3.3V	LED, green, indicates 3.3V power is applied
D8	DIN0	LED, green, indicates DIN(0) signal is asserted
D9	DIN1	LED, green, indicates DIN(1) signal is asserted
D10	DIN2	LED, green, indicates DIN(2) signal is asserted
D11	DIN3	LED, green, indicates DIN(3) signal is asserted
D12	DOUT3	LED, yellow, indicates DOUT(3) signal is asserted
D13	DOUT2	LED, yellow, indicates DOUT(2) signal is asserted
D14	DOUT1	LED, yellow, indicates DOUT(1) signal is asserted
D15	DOUT0	LED, yellow, indicates DOUT(0) signal is asserted
D16	GPIO	LED, red, general purpose IO signal, when on signal is asserted (MC11)
D17	WDOG	LED, yellow, indication is a function of the E²Brain™ module Watchdog logic(MC7)
D18	BOOT	LED, green, indication is a function of the NetBootLoader during system booting, is available to the application after booting is completed (MC6)
D20	POST_HI	LED, seven segment, hexadecimal display, higher nibble of byte, used for indicating POST codes or application after system is booted
D21	POST_LO	LED, seven segment, hexadecimal display, lowerer nibble of byte, used for indicating POST codes or application after system is booted
J1	+12Supply	Connector, +12V main input power supply
J2	TTL-FP	Connector, TTL signal interface for flat panel display
J3	FP-BL	Flat panel backlight power (SM501_BIAS)
J4	TERM	Connector, serial interface for terminal operations
J5	M/C	Connector, external access to monitor and control signal lines
J6	ZV/PWM/ MISC	Connector, zoom video port, PWM interface, power, and various control signals of the SM501 chip
J7	TP1	Connector, test and programming interface
J8	CONS	Connector, serial interface for console operations
J9	INT2	Jumper, test interface, interrupt input source, active low
J10	INT1	Jumper, test interface, interrupt input source, active high
J11	TP2	Connector, programming interface for the EBC3 logic CPLD
J12	F/LPCB	Jumper, selects boot code source: open = boot from E²Brain™ module Flash (default); set = boot from EBC3 LPC Flash

Table 1-3: EBC3 Interfaces and MC Elements

IF / MCE	ALIAS	DESCRIPTION
J13	PCI_SLOT2	Connector, PCI interface, standard 32-bit, 3.3V V(I/O), slot number 2, 33/66 MHz
J14	PCI_SLOT1	Connector, PCI interface, standard 32-bit, 3.3V V(I/O), slot number 1, 33/66 MHz
J15	LPCFLASH	Socket, Flash interface, PLCC, 32-pin, for LPC boot Flash
J16	CIE_EX	Connector, Local bus and DIO interfacing for EB8347
J17 (P1)	SI	Connector, system interfacing to the E²Brain™ module, System Interface - SI
J18 (P4)	CIE	Connector, communications interfacing extension to the E²Brain™ module, Communications Interface Extension - CIE
J19	SER1	Connector, high speed serial interface 1
J20	DIO	Connector, general purpose digital input (4) and output (4) interfacing
J21	SER2	Connector, high speed serial interface 2
J22 (P2)	SIE	Connector, system interfacing extension to the E²Brain™ module, System Interface Extension - SIE
J23 (P3)	CI	Connector, communications interfacing to the E²Brain™ module, Communications Interface - CI
J24	PCI_MINI	Connector, PCI interface, 32-bit, Mini PCI, 33 MHz
J25	SPI	Connector, SPI signal interface
J26B, J26A	TSE[1, 2]	Connector, dual RJ45, three speed Ethernet interface, right connector (J26B) is TSE1, left connector (J26A) is TSE2 (as seen from front of connector - LEDs visible)
J27	-	Reserved
J28	CF_SOCKET	Connector, CompactFlash interface, Type I and II
J29	USB1	Connector, USB interface, USB 2.0, type A
J30	USB2	Connector, USB interface, USB 2.0, type mini AB
J31	DVI	Connector, DVI interface for TFT flat panel displays
J32	MIC	Connector, audio microphone input to AC97 codec
J33	LINE IN	Connector, audio line input to AC97 codec
J34	LINE OUT	Connector, audio line output to AC97 codec
JP1	VDDSAVE	Jumper, VDDSAVE supply voltage select: 3.3V, 5V, or no voltage
JP2	SPI SELECT	Connector, SPI device select interface for an EEPROM, the CPU, an external device (JP2 is a connector and not a jumper.)
SW1	PWR ON/OFF	Power on/off switch
SW2	ABORT	Switch, when closed asserts the abort signal MC1
SW3	RESET	Switch, when closed asserts the reset signal MC0
SW4	<tbd>	<tbd>

1.6 Technical Specifications

Table 1-4: EBC3 Main Specifications

	DESIGNATOR	TYPE	SPECIFICATIONS
Mezzanine Module	EB8347		High Performance PowerPC™ Processor E²Brain™ Module based on the Freescale Integrated Processor PowerPC MPC8347(E)
Onboard Controller	Logic Controller		CPLD controller, Altera EPM3128, for digital I/O and seven segment LED display, LPC-bus interface
Embedded Module Interfaces	J17 (P1)	System Interface (SI)	E²Brain™ System Interface, 140-pin HIROSE connector
	J22 (P2)	System Interface Extension (SIE)	E²Brain™ System Interface Extension, 80-pin HIROSE connector
	J23 (P3)	Communications Interface (CI)	E²Brain™ Communications Interface, 80-pin HIROSE connector
	J18 (P4)	Communications Interface Extension (CIE)	E²Brain™ Communications Interface Extension, 140-pin HIROSE connector
System Interfaces	PCI INTERFACES		
	J17 (P1) (internal)	PCI-bus	Standard PCI bus, 32-bit, 33/66 MHz
	J13	PCI Slot 2	Single standard PCI expansion slot interface, 124-pin connector
	J14	PCI Slot 1	Single standard PCI expansion slot interface, 124-pin connector
	J24	Mini PCI	Mini PCI expansion interface, 124-pin connector
	LPC INTERFACES		
	J17 (P1) (internal)	LPC-bus	Standard LPC-bus, but no DMA support
	J15	PLCC32 socket	32-pin PLCC socket, supports LPC Flash for system booting, jumper configurable
	I²C INTERFACES		
	J17 (P1) (internal)	I²C-bus	Two standard I²C-bus interfaces On each interface only one device is connected, an EEPROM, which is provided for application development of I²C functionality. No other interfacing is possible.

Table 1-4: EBC3 Main Specifications (Continued)

	DESIGNATOR	TYPE	SPECIFICATIONS
System Interfaces	COMPACTFLASH INTERFACES		
	J22 (P2) (internal)	CompactFlash	CompactFlash interface routed from J22 (P2) to J28 to allow for direct interfacing between the E²Brain™ module and a CompactFlash
	J28	CompactFlash	Standard CompactFlash device interface, 50-pin, male, dual pinrow, shrouded connector
	TERMINAL / CONSOLE INTERFACES		
	J4	RS232	TERM, terminal serial port (no HW handshake), 9-pin, male, D-Sub connector
	J8	RS232	CONS, console serial port (no HW handshake), 9-pin, male, D-Sub connector
	USB INTERFACES		
	J29	USB 2.0	USB1, host port, type A receptacle connector
	J30	USB 2.0	USB2, device port, mini USB, type AB receptacle connector
	SPI INTERFACES		
	JP2	SPI device select	Special SPI device selection interface: 3-pin connector for up to three devices
	J25	SPI bus	Standard SPI interface with one device select line on 6-pin single row connector
	CRT INTERFACE		
	J31	CRT analog	CRT analog display interface (RGB plus H and V sync) routed to standard DVI connector
	AUDIO INTERFACES		
	J32	MIC	AC97 Codec microphone input interface on 3.5 mm stereo audio jack
	J33	LINE IN	AC97 Codec LINE IN input interface on 3.5 mm stereo audio jack
	J34	LINE OUT	AC97 Codec LINE OUT output interface on 3.5 mm stereo audio jack
	DIGITAL INPUT AND OUTPUT (DIO) INTERFACES		
	J21	Digital Input / Output	Four channels of digital input and four channels of digital output non-opto-isolated signals on 10-pin, male, shrouded, dual pinrow connector (DI 0, 1, 2, 3 and DO 0, 1, 2, 3)

Table 1-4: EBC3 Main Specifications (Continued)

	DESIGNATOR	TYPE	SPECIFICATIONS
Communications Interfaces	HIGH SPEED SERIAL INTERFACES		
	J19	RS232	SER1, configurable serial port, 9-pin, male, D-Sub connector
	J21	RS232	SER2, configurable serial port, 9-pin, male, D-Sub connector
	ETHERNET INTERFACES		
	J26A/B	Gigabit Ethernet (TSE)	Two three speed Ethernet interfaces, 10 / 100 / 1000 Mbit, dual RJ45 connector, TSE1 is routed to right connector, auto-negotiation
	OTHER INTERFACES		
	J2	TTL flat panel	TTL signals for the direct connection of an 18-bit/color TFT flat panel display
	J6	ZV/PWM/MISC	Zoom video port, least significant color pins for display connection, three PWM output pins
	J16	GPIO	General purpose interface, supports EB8347 DIO and Local bus address and control signals, shrouded, 50-pin, male, dual pinrow connector
	J31	TMDS (DVI)	Standard DVI interface for TFT displays
Monitor and Control (M/C) Interfaces	SWITCH INTERFACES		
	SW1	Switch	Board power on/off switch
	SW2	Switch	Abort switch, generates abort input (interrupt request)
	SW3	Switch	Reset switch, generates reset input
	SW4	Switch	<tbd>
	LED INTERFACES		
	D2	LED	Indicates 12V input power is applied
	D4	LED	Indicates 5V power is applied
	D5	LED	Indicates 3.3V power is applied
	D8	LED	Indicates DIN(0) signal is asserted
	D9	LED	Indicates DIN(1) signal is asserted
	D10	LED	Indicates DIN(2) signal is asserted
	D11	LED	Indicates DIN(3) signal is asserted
	D12	LED	Indicates DOUT(3) signal is asserted
	D13	LED	Indicates DOUT(2) signal is asserted
	D14	LED	Indicates DOUT(1) signal is asserted

Table 1-4: EBC3 Main Specifications (Continued)

	DESIGNATOR	TYPE	SPECIFICATIONS
Monitor and Control (M/C) Interfaces	D15	LED	Indicates DOUT(0) signal is asserted
	D16	LED	General purpose IO signal, when on signal is asserted (MC11)
	D17	LED	Indication is a function of the E²Brain™ module Watchdog logic(MC7)
	D18	LED	Indication is a function of the NetBootLoader during system booting, is available to the application after booting is completed (MC6)
	D20	LED	Seven segment, hexadecimal display, higher nibble of byte, used for indicating POST codes or application after system is booted
	D21	LED	Seven segment, hexadecimal display, lowerer nibble of byte, used for indicating POST codes or application after system is booted
	TSE1_LINK	LED	TSE channel 1 link indicator, green, integrated in J26B
	TSE1_SPEED	LED	TSE channel 1 link speed indicator, green/yellow, integrated in J26B
	TSE2_LINK	LED	TSE channel 2 link indicator, green, integrated in J26A
	TSE2_SPEED	LED	TSE channel 2 link speed indicator, green/yellow, integrated in J26A
	SIGNAL INTERFACES ON J5		
	MC2	M/C	Specific use of these signals is function of application and E²Brain™ module employed J5 is a 6-pin, male, dual pinrow header connector
	MC3	M/C	
	MC5	M/C	
	MC9	M/C	
	MC10	M/C	
	GND	Ground	
	J7	JTAG / DEBUG	EB8347 T / P interface, 16-pin, male, dual pinrow header connector
	J11	JTAG	EBC3 logic programming interface, 10-pin, male, dual pinrow, miniature header connector

Table 1-4: EBC3 Main Specifications (Continued)

	DESIGNATOR	TYPE	SPECIFICATIONS
Power Interfaces	J1	+ 12 V	Main input power interface to EBC3 board, 2-pin female receptacle
	J3	+ 3.3V or +5V	When SM501_BIAS asserted, supplies either +3.3V or +5V for flat panel backlight operation
	J17 (P1)	+ 3.3 V, V(IO)	Input power interface to E²Brain™ module, 140-pin HIROSE connector
	J22 (P2)	+ 3.3 V, V(IO)	Input power interface to E²Brain™ module, 80-pin HIROSE connector
	Battery socket (BT1)	AUX Power	Battery input power interface to E²Brain™ modules for power backup of RTC and SRAM memory devices Battery voltage range: 2.8 to 3.6 volts
	DC / DC	Power converter (onboard)	+ 12 V DC to + 3.3 V DC and + 5 V DC converter, distribution of power to EBC3 board and board connectors
General	Mechanical		Conforms with Kontron Modular Computers' "E²Brain™ Module Specification"
	Electrical		Main board input power voltage: + 12 V DC Onboard voltages: + 3.3 V DC + 5 V DC + 12 V DC + 2.5 V DC (for ETH PHY) + 1.25 V DC (for ETH PHY)
	Power Consumption		Output rating of the onboard DC / DC converter is 30 W
	Temperature Range		Operational: 0ºC to +55ºC Standard Storage: -55ºC to +125ºC
	Humidity		93% relative humidity at 40°C non-condensing
	Dimensions		244 mm x 244 mm, micro ATX
	Board Weight		Approximately 275 g (without E²Brain™ module installed)

1.7 Applied Standard

The Kontron module EBC3 complies with the requirements of the following standard:

Table 1-5: Applied Standard

	TYPE	STANDARD
CE	Electrical Safety	EN60950-1 Note: The EBC3 is specified I/O only for: SELV and EVL. It is **NOT SPECIFIED** for “Hazardous”

1.8 Related Publications

Table 1-6: Related Publications

	ISSUED BY	DOCUMENT
PCI	PCI-SIG	PCI Local Bus Specification, R.2.2
LPC	Intel®	Intel® Low Pin Count (LPC) Interface Specification, Rev. 1.1
I²C	Philips	I2C-BUS SPECIFICATION, Rev. 2.1
E²Brain	Kontron Modular Computers	E²Brain™ Module Specification, Rev. 01
USB	USB Implementers Forum, Inc.	Universal Serial Bus Revision 2.0 specification
AC97	Intel®	AC97 codec specification, version 2.1
DVI	DDWG	Digital Visual Interface, rev. 1.0

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Chapter 2

Functional Description

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2. Functional Description

The following chapters present more detailed, board level information about the EBC3 E²Brain™ SAI (Simplified Application Interface) whereby the board components and their basic functionality are discussed in general.

2.1 General Information

The EBC3 is comprised basically of the following:

- E²Brain embedded module interfaces
  - System Interface
  - System Interface Extension
  - Communications Interface
  - Communications Interface Extension
- Board system interfaces:
  - PCI expansion slots, Mini PCI socket
  - I²C bus
  - LPC interface
  - Terminal and Console (T/C) serial interfacing
  - Monitor and Control (M/C) interfacing
  - Test and Programming (T/P) interfacing
  - CompactFlash (CF) interface
  - Digital input and output interfacing
  - USB interfacing
  - LPC Boot Flash
  - SPI
  - Multimedia interfacing (graphics and audio)
  - DC/DC power supply
- Board communications interfaces:
  - High Speed Serial (HSS) communications
  - Gigabit Ethernet (TSE)

2.1.1 Embedded Module Interfaces

The EBC3 E²Brain™ SAI is supplied with a comprehensive set of embedded module interfacing capabilities. The standard set of system interfaces is routed through the System Interface connector J17 (P1). An extended set of system interfacing is routed through the System Interface Extension connector J22 (P2). The standard set of communications interfaces is routed through the Communications Interface connector J23 (P3). In addition, the EBC3 is provided with the Communications Interface Extension connector J18 (P4).

The System Interface connector J17 (P1) provides interfacing for the following:

- PCI bus
- LPC bus
- I²C bus (two separate busses)
- Terminal and Console (T/C) serial interfacing (TERM and CONS)
- Monitor and Control (M/C) interfacing
- Test and Programming (T/P) interfacing

The System Interface Extension connector J22 (P2) provides interfacing for the following:

- CompactFlash (CF) interface
- SPI interface
- CRT analog interface
- Audio (AC97) interfacing
- USB interfacing

The Communications Interface connector J23 (P3) provides interfacing for the following:

- High Speed Serial (HSS) interfacing (TTL level) (SER1, SER2)
- Gigabit Ethernet (MDI interface, Three Speed Ethernet)

The Communications Interface Extension connector J18 (P4) provides interfacing for the following:

- Giga Ethernet (GMII interface, Three Speed Ethernet)
- GPIO / Local bus address and control interfacing
- TMDS (DVI) interfacing
- TTL flat panel signal interfacing
- Zoom video interfacing
- PWM (brightness control interface)

2.1.2 Board System and Communications Interfaces

The EBC3 supports a very comprehensive sub-set of the E²Brain system and communications interfaces. Refer to the individual connector pinout descriptions for details.

2.2 Board-Level Interfacing Diagrams

The following five figures demonstrate the interfacing structure between the internal processing elements of the EBC3 and other major EBC3 components. The interfacing lines are shown in white where they are on board and in black for board external interfacing.

Legend for figures 8 through 12:

#	Interfacing without switching
(Jn)	Connector designator from E²Brain specification
(Pn)	Connector designator from E²Brain specification
AC97	Audio Control 97
BOOT	Boot LED
BT1	Backup battery interface
CI	Communications Interface
CIE	Communications Interface Extension
CODEC	Coder/decoder (audio)
CPLD	Complex programmable logic device
CRT	Cathode ray tube
DC/DC	DC to DC (converter)
DIN	Digital input indicator LED
DIO	Digital input and output
Dnn	LEDs 2, 4, 5, 8 ... 18, 20, 21
DOUT	Digital output indicator LED
ETH1	Ethernet 1
G/GY	Green and green/yellow LEDs
GMII1	Gigabit media independent interface 1
GPIO	General purpose input or output (LED)
HSS	High speed serial interfacing
I²C	Inter-Integrated Circuit
J26A	TSEC2 interface (left connector)
J26B	TSEC1 interface (right connector)
LB-AD	Local bus address interface
LB-DA	Local bus data interface
LDO	Low dropout linear regulator
LOGIC	Logic controller
LPC	Low pin count
M/C	Monitor and Control
MAG	Magnetics
MDI	Media dependent interface
nn	Connector number nn (Jnn)
PCI	Peripheral component interface
PHY	Ethernet PHY
PWM	Pulse width modulation
SAI	Simplified application interface
SERn	Serial interface n
SI	System Interface
SIE	System Interface Extension
SPI	Serial peripheral interface
SPI_SEL	SPI select signal
SWn	Switches 1, 2, 3, 4
T/C	Terminal/Console (serial interface)
T/P	Test and Programming
TMDS	Transition minimized differential signal (DVI)
TTL-PS	TTL panel signals
TXRX	Transceiver
USB	Universal serial bus
V(I/O)	PCI signalling voltage
V_BAT	Backup power input
WDOG	Watchdog (LED)
X	Interfacing with switching
ZV	Zoom video

Figure 2-1: EBC3 Board Level Interfacing (Sheet 1 of 5)

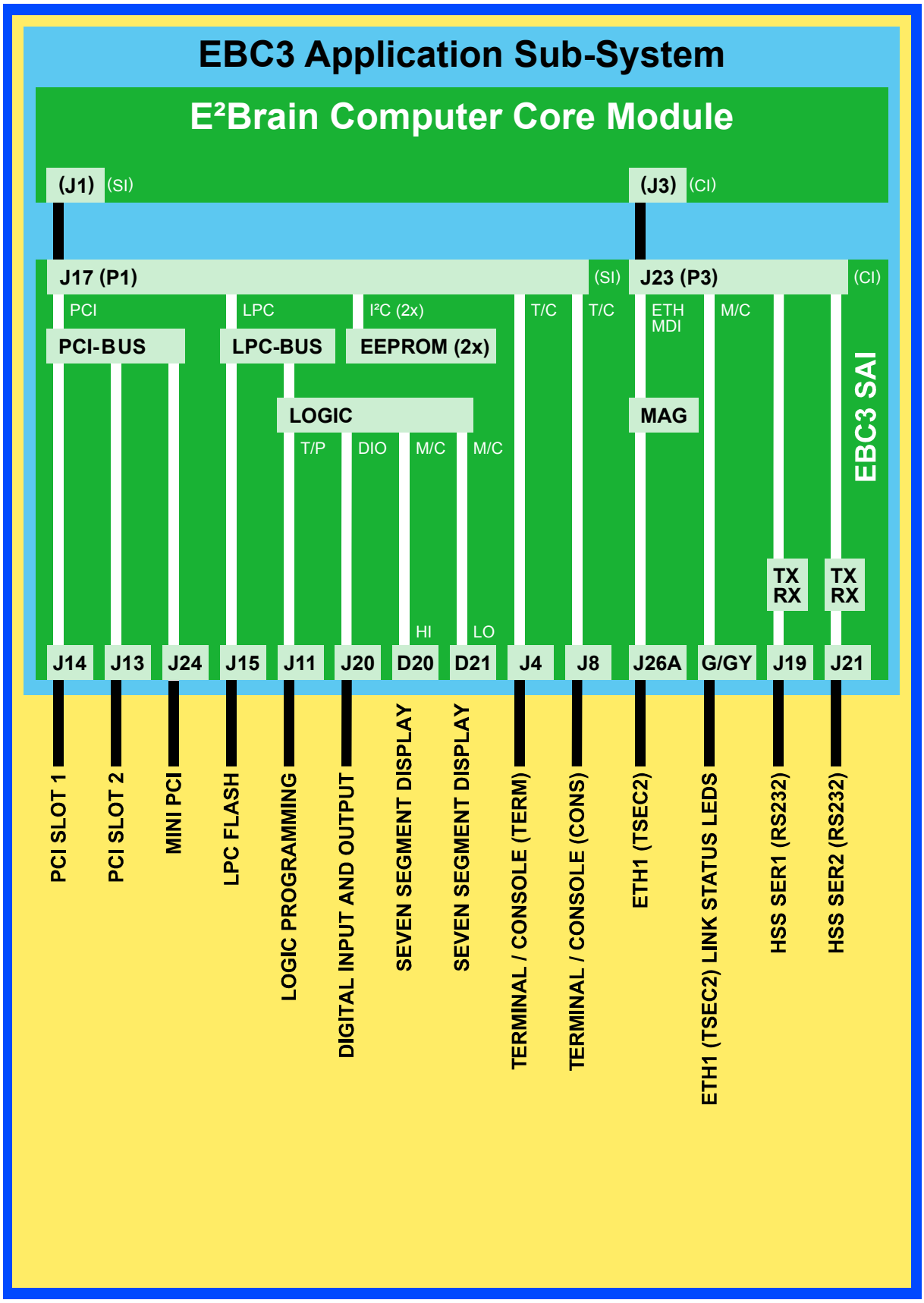


Figure 2-2: EBC3 Board Level Interfacing (Sheet 2 of 5)

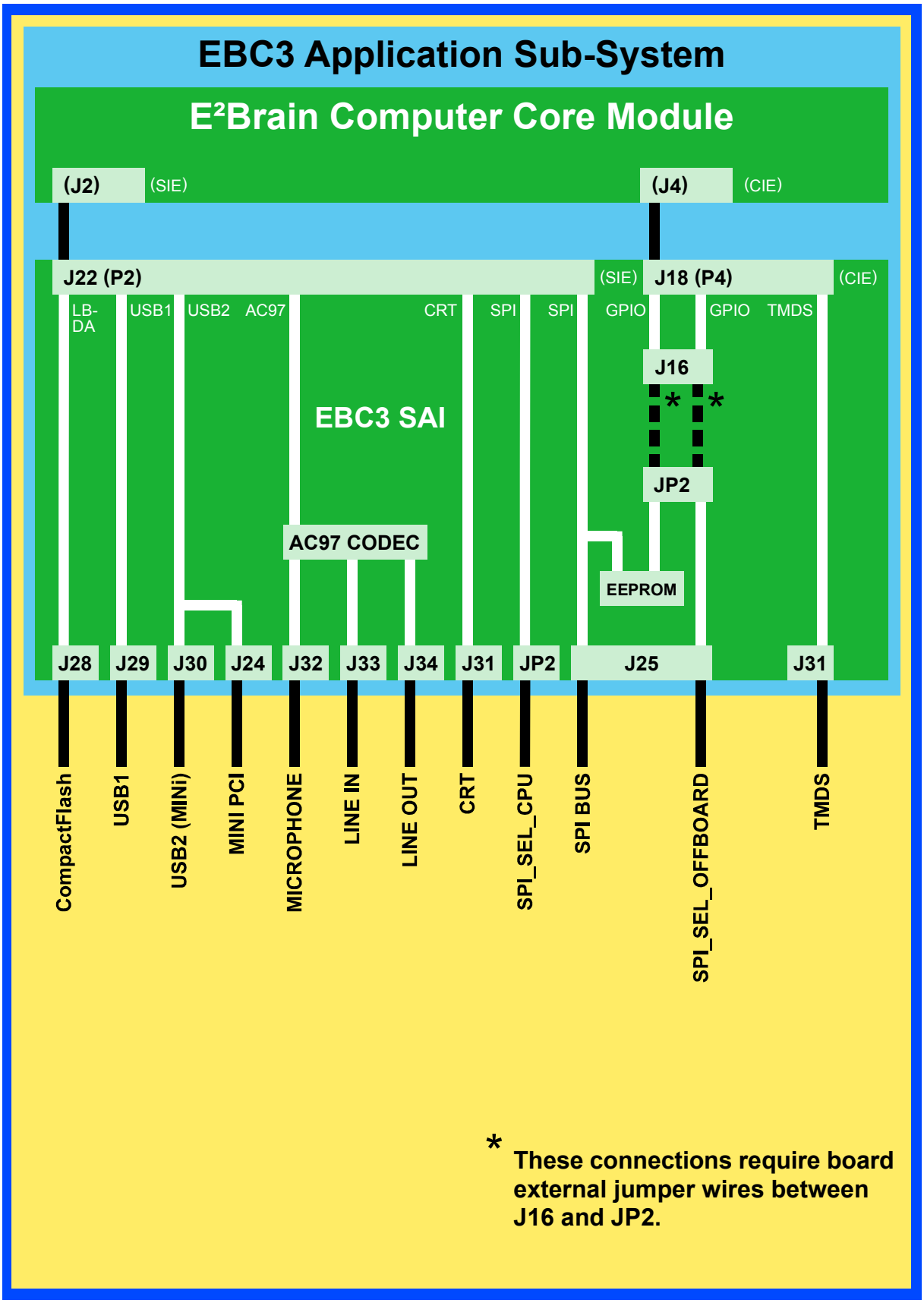


Figure 2-3: EBC3 Board Level Interfacing (Sheet 3 of 5)

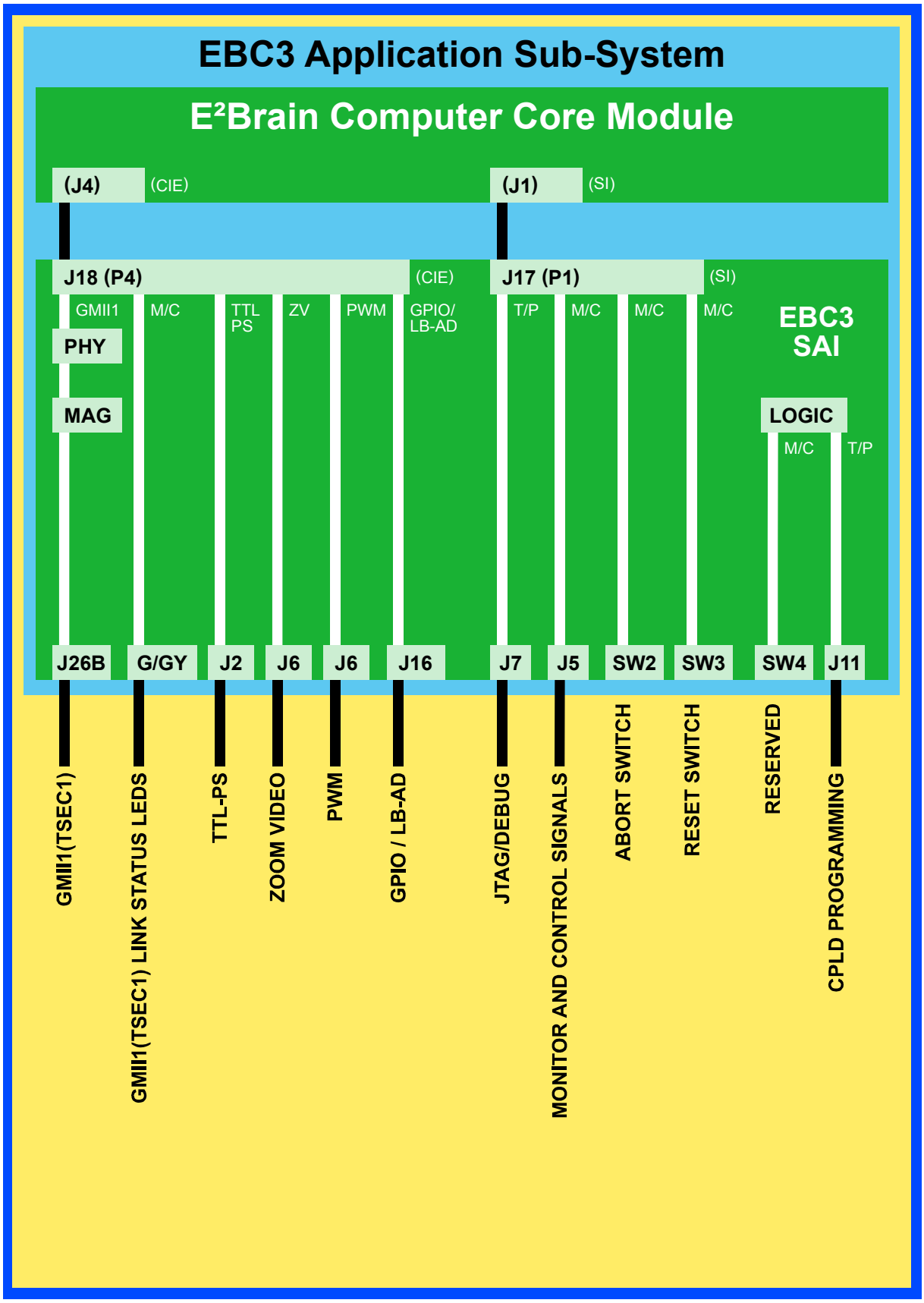


Figure 2-4: EBC3 Board Level Interfacing (Sheet 4 of 5)

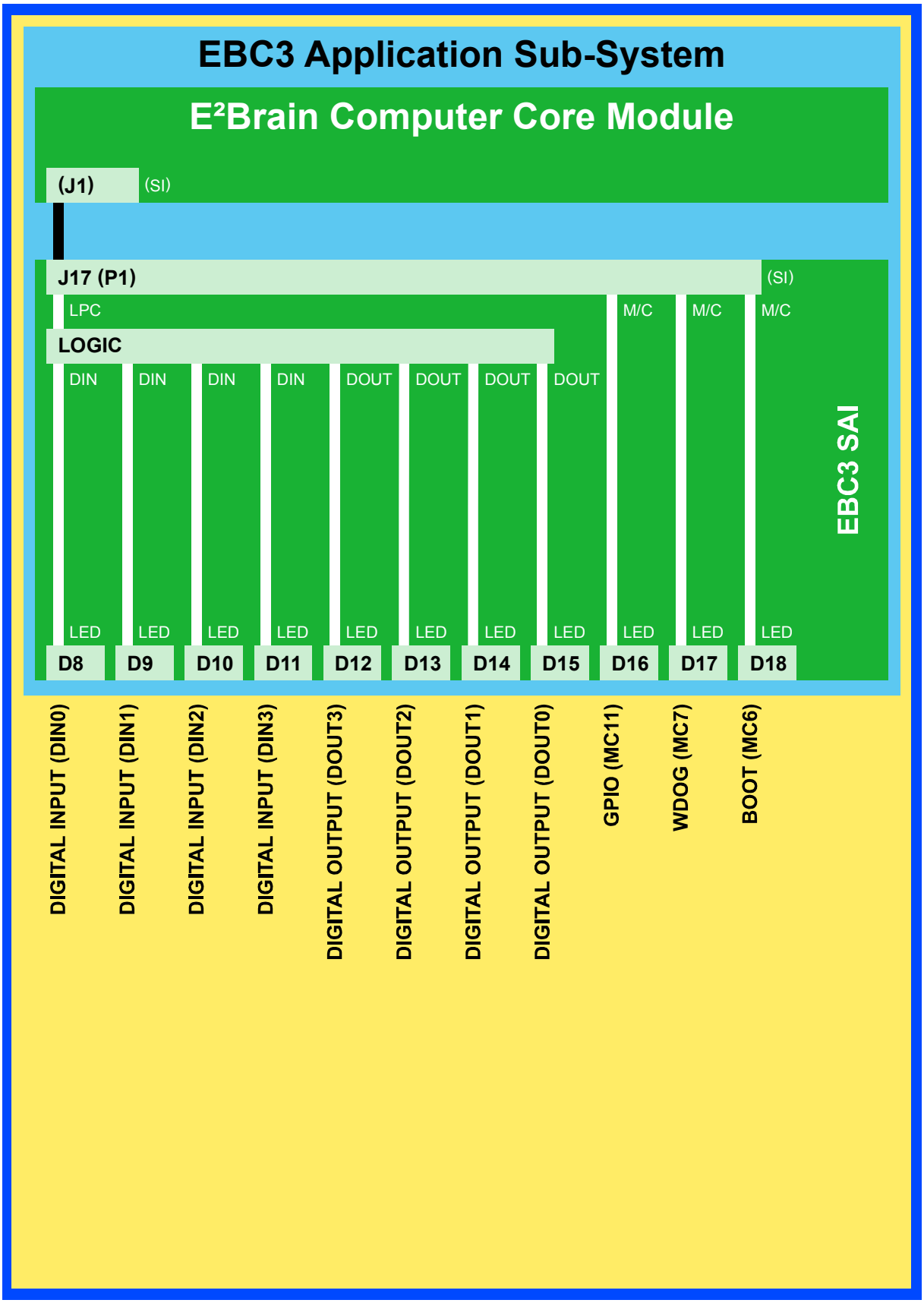
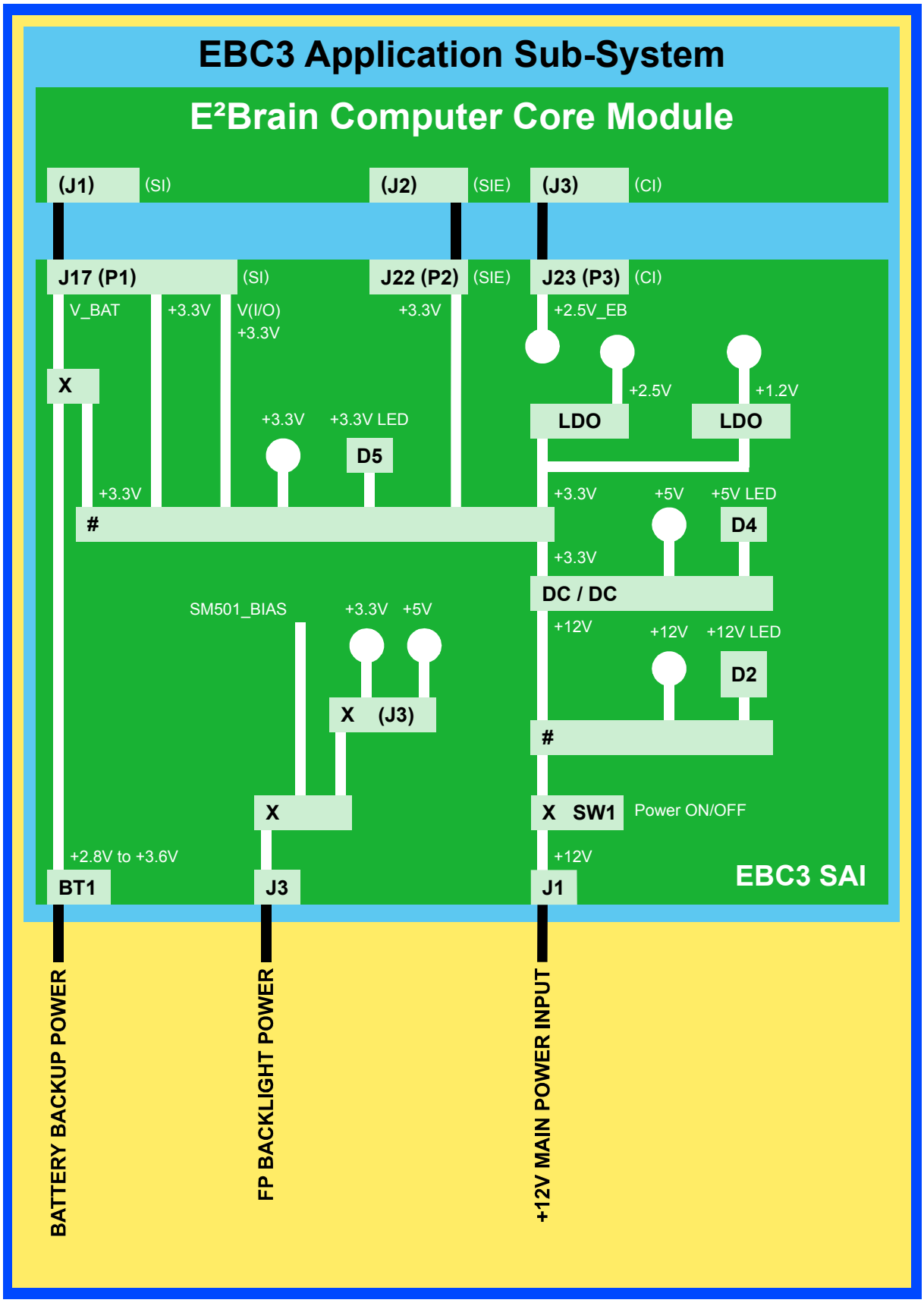


Figure 2-5: EBC3 Board Level Interfacing (Sheet 5 of 5)



2.3 Embedded Module Interfaces

As the name implies, these interfaces provide the basic interfacing functionality required for the realization of E²Brain™ applications using the EBC3 as the development platform.

2.3.1 Embedded Module System Interface

The System Interface is realized using a 140-pin, HIROSE FX8C-140S-SV connector designated as J17 (P1). The following table provides an overview of the signal types and a brief description of the interfacing realized on this connector. The ensuing sections provide more detailed information concerning the signal specification for this interface.

Table 2-1: System Interface J17 (P1) Signal Types

SIGNAL TYPE	DESCRIPTION
POWER	EBC3 E²Brain™ module input power, grounds, battery backup power, PCI signaling voltage V(I/O)
MONITOR AND CONTROL (M/C)	Monitor signals for LEDs and PCI operation. Control signals for E²Brain™ module operation
TEST AND PROGRAMMING (T/P)	JTAG, DEBUG, and system programming signals
TERMINAL AND CONSOLE (T/C)	Two serial interfaces: one for connecting a terminal and one for use as a console interface
I2C	Two I2C standard interfaces for low speed, serial, inter-chip communications
LPC	One LPC standard interface for (GP)IOs and simple memory interfacing
PCI	One PCI standard interface for PCI-bus interfacing

2.3.1.1 J17 (P1) Connector Pinout

The following table provides signal pinouts for connector J17 (P1).

Figure 2-6: J17 - System Interface Connector (SI)

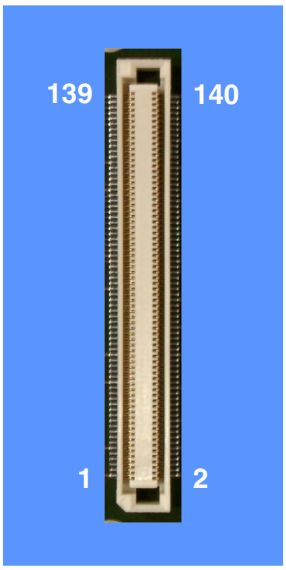


Table 7 Notes:

1. Emulator VCC: is used to provide the applicable IO voltage to the emulator probe
2. Back-up power for the SRAM and RTC
3. Used in AGENT mode
4. DIR: signal direction is as viewed from the E²Brain™module.

Table 2-2: Pinout of J19 (P1) Connector

SIGNAL	DIR	SIGNAL GROUP	PIN	PIN	SIGNAL GROUP	DIR	SIGNAL
GND	I	POWER	1	2	POWER	I	AUX-Power (2
SDA1	I/O	I2C	3	4	I2C	I/O	SCL1
MC6	O	M/C	5	6	POWER	I	+3.3V
MC0	I	M/C	7	8	M/C	O	MC7
MC2	I	M/C	9	10	M/C	I	MC1
+3.3V	I	POWER	11	12	POWER	I	GND
MC3	I	M/C	13	14	M/C	O	MC11
MC4	I	M/C	15	16	M/C	I	MC5
MC9	O	M/C	17	18	M/C	I	MC8
GND	I	POWER	19	20	M/C	I/O	MC10
LPCCLK	O	LPC	21	22	NC		
LAD0	I/O	LPC	23	24	LPC	I/O	LAD1
LAD2	I/O	LPC	25	26	POWER	I	+3.3V
LFRAME#	O	LPC	27	28	POWER	I	GND
SERIRQ#	I/O	LPC	29	30	LPC	I/O	LAD3
TxD1 (TERM)	O	T/C	31	32	NC		
+3.3V	I	POWER	33	34	T/C	O	TxD2 (CONS)
GND	I	POWER	35	36	T/C	I	RxD2 (CONS)
RxD1 (TERM)	I	T/C	37	38	T/P	I	CKSTP_IN
EMU_VCC (1	O	T/P	39	40	T/P	I	COP-HRST/HRESET
CKSTP_OUT	O	T/P	41	42	POWER	I	GND
COP-SRST/SRESET	I	T/P	43	44	T/P	I	TMS
TRST	I	T/P	45	46	POWER	I	+3.3V
TCK	I	T/P	47	48	T/P	O	TDO
SLC2	I/O	I2C	49	50	T/P	I	TDI
GND	I	POWER	51	52	I2C	I/O	SDA2
PCI-CLK-OUT-0	O	PCI	53	54	POWER	I	V(I/O) (3.3V)
+3.3V	I	POWER	55	56	PCI	I	PCI-CLK-IN (3
PCI-CLK-OUT-1	O	PCI	57	58	POWER	I	GND
PCI-RST#	I/O	PCI	59	60	PCI	O	PCI-CLK-OUT-2
INTA#	I/O	PCI	61	62	PCI	I	INTC#
INTB#	I	PCI	63	64	PCI	I/O	GNT#1
INTD#	I	PCI	65	66	POWER	I	+3.3V
GND	I	POWER	67	68	PCI-MASTER	O	GNT#2
AD31	I/O	PCI	69	70	PCI-MASTER	O	GNT#3

Table 2-2: Pinout of J19 (P1) Connector

SIGNAL	DIR	SIGNAL GROUP	PIN	PIN	SIGNAL GROUP	DIR	SIGNAL
AD29	I/O	PCI	71	72	PCI	I/O	REQ#1
AD27	I/O	PCI	73	74	PCI-MASTER	I	REQ#2
+3.3V	I	POWER	75	76	POWER	I	GND
AD25	I/O	PCI	77	78	PCI-MASTER	I	REQ#3
C/BE3#	I/O	PCI	79	80	PCI	I/O	AD30
AD23	I/O	PCI	81	82	PCI	I/O	AD28
GND	I	POWER	83	84	PCI	I/O	AD26
AD21	I/O	PCI	85	86	PCI	I/O	AD24
V(I/O) (3.3V)	I	POWER	87	88	POWER	I	+3.3V
AD19	I/O	PCI	89	90	PCI	I/O	IDSEL
AD17	I/O	PCI	91	92	POWER	I	GND
C/BE2#	I/O	PCI	93	94	PCI	I/O	AD22
+3.3V	I	POWER	95	96	PCI	I/O	AD20
IRDY#	I/O	PCI	97	98	PCI	I/O	AD18
DEVSEL#	I/O	PCI	99	100	PCI	I/O	AD16
GND	I	POWER	101	102	PCI	I/O	FRAME#
PCI-X-CAP	I/O	PCI	103	104	POWER	I	GND
LOCK#	I/O	PCI	105	106	PCI	I/O	TRDY#
PERR#	I/O	PCI	107	108	PCI	I/O	STOP#
SERR#	I/O	PCI	109	110	POWER	I	+3.3V
GND	I	POWER	111	112	PCI	I/O	PAR
C/BE1#	I/O	PCI	113	114	PCI	I/O	AD15
AD14	I/O	PCI	115	116	POWER	I	V(I/O) (3.3V)
AD12	I/O	PCI	117	118	PCI	I/O	AD13
AD10	I/O	PCI	119	120	PCI	I/O	AD11
+3.3V	I	POWER	121	122	PCI	I/O	AD9
M66EN	I/O	PCI	123	124	POWER	I	GND
AD8	I/O	PCI	125	126	PCI	I/O	C/BE0#
AD7	I/O	PCI	127	128	PCI	I/O	AD6
AD5	I/O	PCI	129	130	POWER	I	+3.3V
GND	I	POWER	131	132	PCI	I/O	AD4
AD3	I/O	PCI	133	134	PCI	I/O	AD2
AD1	I/O	PCI	135	136	PCI	I/O	AD0
ACK64#	I/O	PCI	137	138	PCI	I/O	REQ64#
+3.3V	I	POWER	139	140	POWER	I	GND

2.3.1.2 Power Interface

For the EBC3 E²Brain™ module, a single power supply voltage of 3.3 VDC is specified. The following table summarizes the power specifications.

Table 2-3: EBC3 Power Interface Requirements

VOLTAGE	DESCRIPTION
+ 3.3 VDC	Input voltage tolerance: +5% to -3% Supply voltage ripple: 100 mV peak-to-peak
GND	Ground voltage reference input
AUX-Power	Optional auxiliary power input for battery backup of RTC and/or SRAM devices
V(I/O)	PCI signalling voltage selection. The EBC3 only supports 3.3V PCI signalling.

2.3.1.3 Monitor and Control Interface

This interface is comprised of a set of twelve IO signals which can be used to facilitate system integration.

The following table provides a listing of Monitor and Control signals along with a brief description.

Table 2-4: Monitor and Control Interface Signal Description

SIGNAL	PIN	DESCRIPTION
MC0	7	Input (refer to the respective E²Brain™ module documentation for details)
MC1	10	Input (refer to the respective E²Brain™ module documentation for details)
MC2	9	Input (refer to the respective E²Brain™ module documentation for details)
MC3	13	Input (refer to the respective E²Brain™ module documentation for details)
MC4	15	Input (refer to the respective E²Brain™ module documentation for details)
MC5	16	Input (refer to the respective E²Brain™ module documentation for details)
MC6	5	Output (refer to the respective E²Brain™ module documentation for details)
MC7	8	Output (refer to the respective E²Brain™ module documentation for details)
MC8	18	Input (refer to the respective E²Brain™ module documentation for details)
MC9	17	Output (refer to the respective E²Brain™ module documentation for details)
MC10	20	Output (refer to the respective E²Brain™ module documentation for details)
MC11	14	Output (refer to the respective E²Brain™ module documentation for details)

2.3.1.4 Test and Programming Interface

The Test and Programming interface supports JTAG/DEBUG and ISP operations. This interface can be used for connecting hardware emulators and debuggers (COP), and for “in system programming” (ISP) of programmable hardware as well as in system testing (JTAG). It is comprised of a set of six signals whereby some are common to all three interfaces and some are dedicated to only one.

The following table provides a listing of the Test and Programming interface signals and a brief description.

Table 2-5: Test and Programming Interface Signal Description

SIGNAL	DESCRIPTION
TCK	Test Clock in for JTAG/ISP and emulator/debugger
TDI	Test Data In for JTAG/ISP and emulator/debugger
TDO	Test Data Out JTAG/ISP and emulator/debugger
TMS	Test Mode Select, input for JTAG/ISP and emulator/debugger
TRST	Test Reset, input for JTAG/ISP and emulator/debugger
COP_HRST/HRST	Hard Reset, emulator/debugger hard reset In
COP_SRST/SRESET	Soft Reset, emulator/debugger soft reset In
CKSTP_IN	Emulator/debugger specific signal
CKSTP_OUT	Emulator/debugger specific signal
EMU_VCC	Reference Voltage of the JTAG/DEBUG core

2.3.1.5 Terminal and Console Interface

The EBC3 provides two serial interfaces for supporting a terminal port and a low speed communications interface (console) for firmware updating. These interfaces are realized using the CPU on-chip dual UART, and as such provide only a two wire interface without hardware handshake signals.

The following table provides a listing of the Terminal and Console interface signals and a brief description.

Table 2-6: Terminal and Console Interface Signal Description

SIGNAL	DESCRIPTION
TxD1, TxD2 (TERM, CONS)	Serial Transmit Data outputs, channel 1 and 2
RxD1, RxD2 (TERM, CONS)	Serial Receive Data signal inputs, channel 1 and 2

2.3.1.6 I2C Interface

The EBC3 E²Brain™ module provides two I2C serial interfaces for supporting direct interfacing to the EBC3 carrier board devices. These interfaces are two signals wide and fully support the I2C specification.

The following table provides a listing of the I2C interface signals and a brief description.

Table 2-7: I2C Interface Signal Description

SIGNAL	DESCRIPTION
SCL1 / SLC2	Serial Clock lines, channels 1 and 2
SDA1 / SDA2	Serial Data lines, channels 1 and 2

2.3.1.7 LPC Interface

One Low Pin Count (LPC) interface for supporting simple IOs, simple static memory devices, and IO controllers is available to the EBC3.

The controller is completely integrated in the E²Brain™ module and offers an 8-bit data access port to devices which use LPC IO or memory access protocols. I/O and memory area are selected using different address spaces.

The I/O address space is 64 kByte in size, whereas the memory area offers 16 MByte address space. For respective address mapping, refer to the corresponding E²Brain™module documentation.

In addition, a serial IRQ controller is also implemented in the E²Brain™ module, controlling and collecting the serial LPC IRQs and converting and processing them to IRQs for the CPU. DMA, however, is not supported by this interface.

The following table provides a listing of the LPC interface signals and a brief description.

Table 2-8: LPC Interface Signal Description

SIGNAL	DESCRIPTION
LAD[0:3]	Multiplexed Command, Address, and Data lines
LFRAME#	Indicates start of a new cycle, termination of broken cycle
LPCCLK	33 MHz clock
SERIRQ	Serialized IRQ, optional for peripherals that need interrupt

2.3.1.8 PCI Interface

The EB8347 is available either as a system master variant or as a slave (Agent mode) variant. The EBC3, however, supports only system master mode operation.

In PCI Master mode (default by the EBC3), the E²Brain™ module operates as the host, initializing and controlling up three PCI devices on the EBC3.

The following table identifies the EBC3 PCI bus signals and provides a short description of each signal.

Table 2-9: PCI Interface Signal Description

SIGNAL	DESCRIPTION
AD [0:31]	PCI multiplexed address and data bus
INT [A, B, C, D]#	PCI interrupt requests
C/BE [0:3]#	PCI multiplexed bus command and byte enable
IRDY#	Initiator Ready indicates the current bus master is ready to complete the current data phase.
TRDY#	Target Ready indicates the selected device is ready to complete the current data phase.
PCI-RST#	PCI Reset signal, is also used for LPC devices
PCI-CLK-OUT-[1:3]	PCI clock Outputs for up to 3 external bus mastering PCI devices. All PCI signals except PCI_RST#, and INT [A, B, C, D] # are sampled on the rising edge. (Consider routing guidelines for Carrier board)
FRAME#	Indicate the beginning and duration of a PCI access.
STOP#	Indicates the target is requesting the master to stop the current transaction
DEVSEL#	Device select generated by the target when cycle refers to its own address.
REQ [1:3]#	PCI Arbiter requests
GNT [1:3]#	PCI Arbiter grants
PAR	Calculated/Checked Parity
PERR#	Parity Error
LOCK#	PCI Lock resource signal
SERR#	System Error
REQ64#	PCI request for a 64-bit access
ACK64#	PCI grant for a 64-bit access
PCI-CLK-IN	PCI clock input, used in agent mode
AGENT	PCI-agent mode logic input, 0 -> PCI agent mode, 1 -> system controller
M66EN	66 MHz enable
PCI-X-CAP	PCI-X capable

2.3.2 Embedded Module System Interface Extension

The System Interface Extension is realized using an 80-pin, HIROSE FX8C-80S-SV connector designated as J22 (P2), and it is used to provide CPU architecture specific system interfaces.

In the case of the EBC3, a CompactFlash interface, an SPI interface, an analog graphic (CRT) interface, an audio (AC97) interface, and two USB interfaces are available on the System Interface Extension.

The following sections provide further information concerning these interfaces.

Table 2-10: System Interface Extension J2 (Pn2) Signal Types

SIGNAL TYPE	DESCRIPTION
Power	EBC3 E²Brain™ module input power and grounds
Local bus	Supports up to 16-bit data IO for external devices such as CompactFlash in true IDE mode for example and is user configurable
SPI bus	Single Serial Peripheral Interface bus
USB	Dual USB 2.0 interface; one master/device and one master
CRT analog	Standard analog CRT display signals with H/V sync
AC97	AC97 sound interface
DDC bus (I²C)	Display Data Channel bus (I²C) for readout of LCD/TFT display information for display driver support

2.3.2.1 J22 (P2) Connector Pinout

The following figure and table provide pinout information for J22 (P2).

Figure 2-7: J22 - System Interface Extension Connector (SIE)

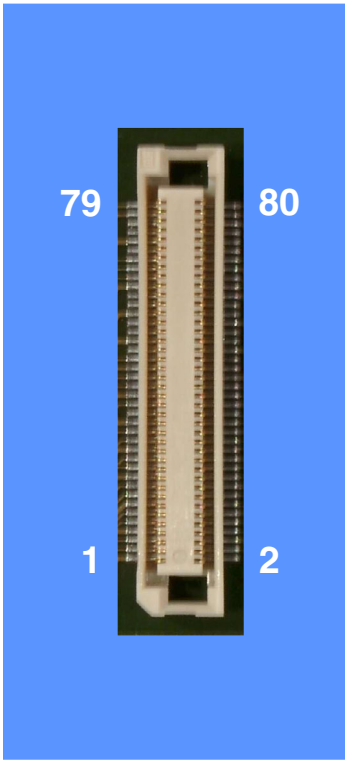


Table 2-11: Pinout of J22 (P2) Connector

SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL
GND	1	2	CF_CD1	CF_D9	41	42	GND
CF_D3	3	4	CF_D11	V(I/O) (3.3V)	43	44	CF_CS16
CF_D4	5	6	+3.3V	CF_D10	45	46	CF_CD2
+3.3V	7	8	CF_D12	ATA_ DMARQ	47	48	GND
CF_D5	9	10	CF_D13	+3.3V	49	50	CF/DMACK
CF_D6	11	12	GND	AC97 _BIT_CLK	51	52	AC97 _SYNC
GND	13	14	CF_D14	AC97_SDIN	53	54	GND
CF_D7	15	16	CF_D15	GND	55	56	AC97 _SDOUT
CF_CS0	17	18	+3.3V	USB_OC	57	58	AC97_RST#
GND	19	20	CF_CS1	USB1_PO	59	60	+3.3V
CF_RD	21	22	CF_WR	GND	61	62	Reserved
CF_INTRQ	23	24	GND	CRT_R	63	64	Reserved
GND	25	26	CF_RST	CRT_G	65	66	GND
CF_IORDY	27	28	CF_A2	CRT_B	67	68	SPI_MOSI
CF_A1	29	30	GND	CRT_VSYNC	69	70	SPI_MISO
+3.3V	31	32	CF_A0	+3.3V	71	72	SPI_SEL
CF_DASP	33	34	CF_D0	CRT _HSYNC	73	74	SPI_CLK
CF_PDIAG	35	36	+3.3V	USB2_PO	75	76	GND
GND	37	38	CF_D1	USB1+	77	78	USB2+
CF_D8	39	40	CF_D2	USB1-	79	80	USB2-

2.3.2.2 CompactFlash Interface

The following table provides a summary of the CompactFlash signals implemented on the System Interface Extension connector.

Table 2-12: CompactFlash Interface Signals

SIGNAL	DESCRIPTION
CF_D[15:0]	Compact Flash data bus – 16-bit wide
CF_CS[1:0]#	Compact Flash chip select
CF_RD#	Compact Flash IO read strobe
CF_WR#	Compact Flash IO write strobe
CF_RST#	Compact Flash reset, active low
CF_INTRQ	Compact Flash interrupt request, active high
CF_IORDY	Compact Flash IO ready
CF_A[2:0]	Compact Flash address lines

Note ...

The CompactFlash interface is realized as a true IDE interface (PIO mode). The PC CARD Memory Mode and the PC Card I/O Mode of the Compact Flash Specification are not supported.

In addition, the pinout for the Compact Flash signals have been optimized for routing to a CompactFlash socket.

2.3.2.3 AC97 Interface

The following table provides a summary of the AC97 signals implemented on the System Interface Extension connector.

Table 2-13: AC97 Interface Signals

SIGNAL	DESCRIPTION
AC97_BIT_CLK	Serial data clock (12.288MHz)
AC97_RST	Codec reset
AC97_SDATA_IN	Serial data in
AC97_SDATA_OUT	Serial data out
AC97_SYNC	Fixed rate sample sync (48kHz)

2.3.2.4 SPI Interface

The following table provides a summary of the SPI signals implemented on the System Interface Extension connector.

Table 2-14: SPI Interface Signals

SIGNAL	DESCRIPTION
SPI_CLK	Input/output serial clock
SPI_MISO	Master in, slave out
SPI_MOSI	Master out, slave in
SPI_SEL	SPI slave select (input)

2.3.2.5 CRT Interface

The following table provides a summary of the CRT signals implemented on the System Interface Extension connector.

Table 2-15: CRT Interface Signals

SIGNAL	DESCRIPTION
CRT_R	CRT red signal (analog): red color information signal
CRT_G	CRT green signal (analog): green color information signal
CRT_B	CRT blue signal (analog): blue color information signal
CRT_HSYNC	CRT horizontal synchronization pulse
CRT_VSYNC	CRT vertical synchronization pulse

2.3.2.6 USB Interface

The following table provides a summary of the USB signals implemented on the System Interface Extension connector.

Table 2-16: USB Interface Signals

SIGNAL	DESCRIPTION
USB_OC#	Over current condition indicator for Host ports (active low)
USB1_PO	Power ON control for Host port 1 (active high)
USB2_PO	Power ON control for Host port 2 (active high)
USB1-	Differential USB1 - (USB port 1, master only)
USB1+	Differential USB1 + (USB port 1, master only)
USB2-	Differential USB2 - (USB port 2), master or device)
USB2+	Differential USB2 + (USB port 2, master or device)

2.3.3 Embedded Module Communications Interface

The Communications Interface Connector J23 (Pn3), is used to provide a set of standard communications interfaces. In the case of the EBC3, there are two types of interfaces provided: two high speed serial interfaces and one Gigabit Ethernet interface.

Table 2-17: Communications Interface J23 (Pn3) Signal Types

SIGNAL TYPE	DESCRIPTION
High Speed Serial (HSS)	Two high speed serial interfaces (SER1, SER2)
Gigabit Ethernet	One Gigabit Ethernet 10/100/1000 Mbps interface

All of these interfaces are provided on the Communications Interface J23 (P3) connector (an 80-pin, HIROSE FX8C-80S-SV connector). The following figure and table provide pinout information for J23 (P3).

Figure 2-8: J23 - Communications Interface Connector (CI)

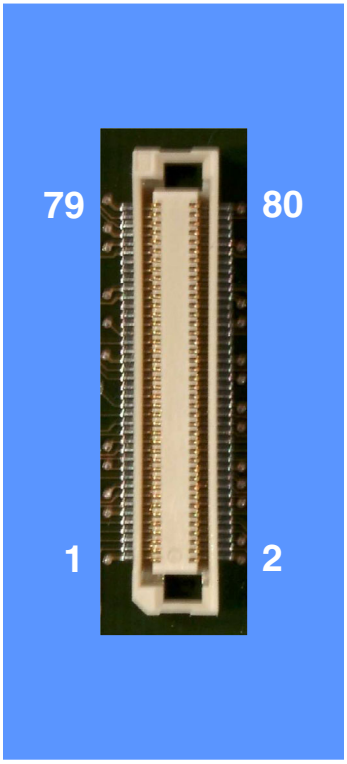


Table 2-18: Pinout of J23 (P3) Connector

SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL
GND	1	2	GND	NC	41	42	NC
RESERVED	3	4	RESERVED	NC	43	44	NC
SER1_RTS	5	6	SER1_CTS	GND	45	46	GND
SER1_TXD	7	8	SER1_RXD	NC	47	48	NC
RESERVED	9	10	RESERVED	NC	49	50	NC
GND	11	12	RESERVED	NC	51	52	NC
RESERVED	13	14	SER2_CTS	NC	53	54	GND
SER2_RTS	15	16	SER2_RXD	NC	55	56	NC
SER2_TXD	17	18	RESERVED	NC	57	58	NC
RESERVED	19	20	RESERVED	NC	59	60	NC
NC	21	22	GND	NC	61	62	NC
NC	23	24	NC	+2.5V	63	64	+2.5V
NC	25	26	NC	ETH1_BIDC-	65	66	ETH1_BIDD-
NC	27	28	NC	ETH1_BIDC+	67	68	ETH1_BIDD+
NC	29	30	NC	ETH1_T- / BIDA-	69	70	ETH1_R- / BIDB-
NC	31	32	NC	ETH1_T+ / BIDA+	71	72	ETH1_R+ / BIDB+
NC	33	34	NC	GND	73	74	ETH1_SD
NC	35	36	NC	ETH1_LINK _LED	75	76	ETH1_1000 _LED
NC	37	38	NC	ETH1_ACT_LED	77	78	ETH1_100_LED
NC	39	40	NC	GND	79	80	GND

2.3.3.1 High Speed Serial Interfaces

Two, four wire, serial ports (SER1 and SER2) are available on the EBC3

The following table provides a summary of the HSS signals implemented on the Communications Interface connector.

Table 2-19: High Speed Serial Interface Signal Type and Description

SIGNAL	DESCRIPTION
SERn_TXD	Transmit data output
SERn_RXD	Receive data input
SERn_RTS	Request to send output
SERn_CTS	Clear to send input

Note ...

If more serial interfaces are required, this can be accomplished through the utilization of appropriate GPIOs on the CIE_EX connector, J16, and additional circuitry external to the EBC3.

2.3.3.2 Gigabit Ethernet Interface

The EBC3 module provides one MDI Gigabit Ethernet interface (ETH1) on the J23 connector. A second GMII Gigabit Ethernet interface (GMII1) is available on the J18 connector.

Additionally, for monitoring and control purposes, LED functionality is provided to indicate activity, link, and speed status information for the respective ports.

Table 2-20: MDI Gigabit Ethernet Port Signal Type and Description

SIGNAL	DESCRIPTION
ETH1_T+ / BIDA+	Transmit pair in 10BaseT/100BaseTX configuration Channel A pair of Media Dependent Interface in 1000BaseT configuration
ETH1_T- / BIDA-	
ETH1_R+ / BIDB+	Receive pair in 10BaseT/100BaseTX configuration Channel B pair of Media Dependent Interface in 1000BaseT configuration
ETH1_R- / BIDB-	
ETH1_BIDC+	Channel C pair of Media Dependent Interface in 1000BaseT configuration
ETH1_BIDC-	
ETH1_BIDD+	Channel D pair of Media Dependent Interface in 1000BaseT configuration
ETH1_BIDD-	
2.5V	2.5V for magnetics transformer center tap
ETH1_LINK_LED	Indicates that link is present Steady on: link is present
ETH1_ACT_LED	Indicates that link is actively transmitting data Blinking: traffic on link
ETH1_100_LED	Indicates link speed Out: 10 Mb On: 100 Mb
ETH1_1000_LED	Indicates link speed Out: 10/100 Mb On: 1000 Mb

Note ...

On the EBC3 connector, J26A, the signal ETH1_ACT_LED is not available. Only the ETH1 Link and Speed information is provided.

2.3.4 Embedded Module Communications Interface Extension

The Communications Interface Extension is realized using a 140-pin, HIROSE FX8C-140S-SV connector designated as J18 (P4).

The following table provides an overview of the signal types and a brief description of the interfacing realized on this connector.

Table 2-21: Communications Interface Extension J18 (Pn4) Signal Type

SIGNAL TYPE	DESCRIPTION
GPIO(Address)	General Purpose Inputs and Outputs (Local bus addressing)
TMDS	Transition Minimized Differential Signal PanelLink DVI interface
ZV	Zoom Video port
PWM	Pulse Width Modulation flat panel, TFT or LCD, brightness control output
FP	TTL Flat Panel interface
TSEC1	Three Speed Ethernet Controller GMII interface (Gigabit Ethernet)

The following figure and table provide pinout information along with the signal direction for the J18 (P4) connector of the EBC3 SAI. The signal direction is as viewed from the E²Brain™ module.

Figure 2-9: J18 - Communications Interface Extension Connector (CIE)

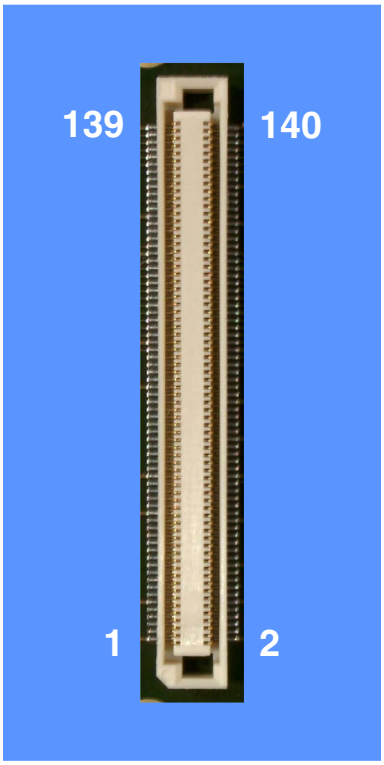


Table 2-22: Pinout of J18 (P4) Connector

SIGNAL	DIR	SIGNAL GROUP	PIN	PIN	SIGNAL GROUP	DIR	SIGNAL
GND	I	POWER	1	2	POWER	I	GND
GPIO25 (XCS1)	I/O	GPIO/LB-AD	3	4	GPIO/LB-AD	I/O	LCLK
GPIO23 (XA23)	I/O	GPIO/LB-AD	5	6	GPIO/LB-AD	I/O	GPIO22 (XA22)
GPIO21 (XA21)	I/O	GPIO/LB-AD	7	8	GPIO/LB-AD	I/O	GPIO20 (XA20)
GPIO19 (XA19)	I/O	GPIO/LB-AD	9	10	GPIO/LB-AD	I/O	GPIO18 (XA18
GND	I/O	POWER	11	12	POWER	I	GND
GPIO17 (XA17)	I/O	GPIO/LB-AD	13	14	GPIO/LB-AD	I/O	GPIO16 (XA16)
GPIO15 (XA15)	I/O	GPIO/LB-AD	15	16	GPIO/LB-AD	I/O	GPIO14 (XA14)
GPIO13 (XA13)	I/O	GPIO/LB-AD	17	18	GPIO/LB-AD	I/O	GPIO12 (XA12)
GPIO11 (XA11)	I/O	GPIO/LB-AD	19	20	GPIO/LB-AD	I/O	GPIO10 (XA10)
GPIO9 (XA9)	I/O	GPIO/LB-AD	21	22	POWER	I	GND
GPIO7 (XA7)	I/O	GPIO/LB-AD	23	24	GPIO/LB-AD	I/O	GPIO8 (XA8)
GPIO5 (XA5)	I/O	GPIO/LB-AD	25	26	GPIO/LB-AD	I/O	GPIO6 (XA6)
GPIO3 (XA3)	I/O	GPIO/LB-AD	27	28	GPIO/LB-AD	I/O	GPIO4 (XA4)
GPIO1 (XA1)	I/O	GPIO/LB-AD	29	30	GPIO/LB-AD	I/O	GPIO2 (XA2)
LGTA	I	GPIO/LB-AD	31	32	GPIO/LB-AD	I/O	GPIO0 (XA0)
NC	-	-	33	34	POWER	I	GND
GND	I	POWER	35	36	-	I	HTPLG
DVI_TXCLK-	O	TMDS	37	38	TMDS	O	DVI_TxOUT2-
DVI_TxCLK+	O	TMDS	39	40	TMDS	O	DVI_TxOUT2+
DVI_TxOUT1-	O	TMDS	41	42	TMDS	O	DVI_TxOUT0-
DVI_TxOUT1+	O	TMDS	43	44	TMDS	O	DVI_TxOUT0+
GND	I	POWER	45	46	POWER	I	GND
PWM0 (GPIO29)	O	PWM	47	48	PWM	O	PWM2 (GPIO31)
NC	-	-	49	50	PWM	O	PWM1 (GPIO30)
ZV15 (GPIO63)	I	ZOOM VIDEO	51	52	ZOOM VIDEO	I	ZV_CLK
ZV14 (GPIO62)	I	ZOOM VIDEO	53	54	ZOOM VIDEO	I	ZV_HREF
ZV7 (GPIO23)	I	ZOOM VIDEO	55	56	POWER	I	GND
ZV6 (GPIO22)	I	ZOOM VIDEO	57	58	ZOOM VIDEO	I	ZV_VSYNC
ZV5 (GPIO21)	I	ZOOM VIDEO	59	60	ZOOM VIDEO	I	ZV4 (GPIO20)
ZV3 (GPIO19)	I	ZOOM VIDEO	61	62	ZOOM VIDEO	I	ZV2 (GPIO18)
ZV1 (GPIO17)	I	ZOOM VIDEO	63	64	ZOOM VIDEO	I	ZV0 (GPIO16)
RESERVED	-	-	65	66	POWER	I	GND
NC	-	-	67	68	TTL-PS	O	FP23
GND	I	POWER	69	70	TTL-PS	O	FP22
SM501_BIAS	O	TTL-PS	71	72	TTL-PS	O	FP21

Table 2-22: Pinout of J18 (P4) Connector

SIGNAL	DIR	SIGNAL GROUP	PIN	PIN	SIGNAL GROUP	DIR	SIGNAL
FP_VDEN	O	TTL-PS	73	74	TTL-PS	O	FP20
NC	-	-	75	76	TTL-PS	O	FP19
FP_EN	-	TTL-PS	77	78	TTL-PS	O	FP18
FP17 (GPIO61)	O	TTL-PS	79	80	POWER	I	GND
GND	I	POWER	81	82	TTL-PS	O	FP16 (GPIO60)
FP15	O	TTL-PS	83	84	TTL-PS	O	FP14
FP13	O	TTL-PS	85	86	TTL-PS	O	FP12
FP11	O	TTL-PS	87	88	TTL-PS	O	FP10
FP9 (GPIO59)	O	TTL-PS	89	90	POWER	I	GND
FP7	O	TTL-PS	91	92	TTL-PS	O	FP8 (GPIO58)
FP5	O	TTL-PS	93	94	TTL-PS	O	FP6
FP3	O	TTL-PS	95	96	TTL-PS	O	FP4
FP1 (GPIO57)	O	TTL-PS	97	98	TTL-PS	O	FP2
FP_HSYNC	O	TTL-PS	99	100	TTL-PS	O	FP0 (GPIO56)
FP_VSYNC	O	TTL-PS	101	102	POWER	I	GND
FP_CLK	O	TTL-PS	103	104	TTL-PS	O	FP_DISP
GND	I	POWER	105	106	-	-	NC
NC	-	-	107	108	GMII1	O	TSEC1_TXD7
TSEC1_TXD6	O	GMII1	109	110	GMII1	O	TSEC1_TXD5
TSEC1_TXD4	O	GMII1	111	112	GMII1	O	TSEC1_TXD3
TSEC1_TXD2	O	GMII1	113	114	POWER	I	GND
GND	I	POWER	115	116	GMII1	O	TSEC1_TXD1
TSEC1_TXD0	O	GMII1	117	118	GMII1	I	TSEC1_RXD1
TSEC1_RXD0	I	GMII1	119	120	GMII1	I	TSEC1_RXD3
TSEC1_RXD2	I	GMII1	121	122	GMII1	I	TSEC1_RXD5
TSEC1_RXD4	I	GMII1	123	124	POWER	I	GND
TSEC1_RXD6	I	GMII1	125	126	GMII1	I	TSEC1_RXD7
TSEC1_COL	I	GMII1	127	128	GMII1	O	TSEC1_CRS
TSEC1_TX_ER	O	GMII1	129	130	GMII1	I	TSEC1_TX_EN
TSEC1_RX_DV	I	GMII1	131	132	GMII1	I	TSEC1_RX_ER
EC_MDIO1	I/O	PHY1_MANAGE	133	134	GMII1	I	TSEC1_RX_CLK
TSEC1_GTX_CLK	O	GMII1	135	136	POWER	I	GND
EC_MDC	O	PHY1_MANAGE	137	138	GMII1	O	TSEC1_TX_CLK
GND	I	POWER	139	140	POWER	I	GND

2.3.4.1 GPIO/Address Interfaces

The EBC3 module provides up to twenty-four GPIO signals or address lines depending on application requirements. These signals are user configurable and provide interfacing to carrier devices for monitor and control functions or data transfer to/from the EBC3 module.

Table 2-23: GPIO/Address Signal Type and Description

SIGNAL	I/O	DESCRIPTION
GPIO[23:0]	I/O	General purpose digital input/output signals (12 CPU IOs; 12 BPCC IOs)
XA[23:0]	O	Address signals, up to 24-bit
XCS1	O	Chip Select 1
LCLK	O	Local bus clock
LGTA	O	Local bus gate

2.3.4.2 TMDS DVI Interface

The EBC3 module provides all of the signals required for a complete TMDS PanelLink™ DVI interface. The electrical characteristics of these signals are low voltage differential and therefore care must be taken when connecting them to the DVI connector on the carrier board.

Table 2-24: TMDS DVI Signal Type and Description

SIGNAL	I/O	DESCRIPTION
DVI_TxCLK+/-	O	TMDS PanelLink clock channel
DVI_TxOUT0+/-	O	TMDS PanelLink output data channel 0 (differential signal)
DVI_TxOUT1+/-	O	TMDS PanelLink output data channel 1 differential signal)
DVI_TxOUT2+/-	O	TMDS PanelLink output data channel 2 (differential signal)
HTPLG	O	Hot plug signal

2.3.4.3 Zoom Video Interface

The EBC3 MMCC Zoom Video interface can interface with video decoders, such as NTSC/PAL decoders, MPEG-2 decoders, and JPEG codecs. The ZV interface supports resolutions up to 1280 x 1024 pixels. It directly accepts digitized RGB or YUV signals, but does not accept analog signals.

Table 2-25: Zoom Video Signal Type and Description

SIGNAL	I/O	DESCRIPTION
ZV[15:0] (GPIOnn)	I	Zoom video input signals (up to 16-bit) (the GPIOnn refers to GPIO signal pin of the MMCC).
ZV_CLK	I	Zoom video clock
ZV_HREF	I	Zoom horizontal reference
ZV_VSYNC	I	Zoom video vertical synchronization

2.3.4.4 Flat Panel Display Interface

The EBC3 module provides also TTL-level flat panel signals for connecting either a 16- or 24-bit pro pixel parallel TFT display. This interface includes the display control signals and the display power management signals which are all provided by the MMCC.

Table 2-26: Flat Panel Display Signal Type and Description

SIGNAL	I/O	DESCRIPTION
FP[23:0]	O	Flat panel display data
SM501_BIAS	O	On/off switching control signal for panel backlighting
FP_VDEN	O	Flat panel VDD enable
FP_EN	O	Flat panel enable
FP_HSYNC	O	Flat panel TFT horizontal sync
FP_VSYNC	O	Flat panel TFT vertical sync
FP_CLK	O	Flat panel pixel clock
FP_DISP	O	Flat panel display enable

2.3.4.5 PWM Interface

The EBC3 MMCC PWM interface serves to provide brightness control for flat panel diplays, TFT or LCD.

Table 2-27: Zoom Video Signal Type and Description

SIGNAL	I/O	DESCRIPTION
PWM[2:0] (GPIOnn)	I	Three independent pulse width modulation signals for flat panel display brightness control (the GPIOnn refers to GPIO signal pin of the MMCC).

2.3.4.6 Gigabit Ethernet Interface

The EB8347 module provides one GMII three speed Ethernet interface (GMII1 (TSEC1)) whose signals are already at TTL level. The EBC3 carrier board provides the PHY, galvanic isolation (magnetics) function, and the appropriate transmission connector type for Ethernet interfacing.

Table 2-28: Gigabit Ethernet Signal Type and Description

SIGNAL	I/O	DESCRIPTION
TSEC1_COL	I	Collision
TSEC1_CRS	I	Carrier sense
TSEC1_GTX_CLK	O	Transmit clock
EC_GTX_CLK125	I	Oscillator source for GMII
EC_MDC	O	Management clock
EC_MDIO	I/O	Management data
TSEC1_RX_CLK	I	Receive clock
TSEC1_RX_DV	I	Receive data valid
TSEC1_RXD[7:0]	I	Receive data bits 7:0
TSEC1_RX_ER	I	Receive error
TSEC1_TX_CLK	I	Transmit clock
TSEC1_TXD[7:0]	O	Transmit data bits 7:0
TSEC1_TX_EN	O	Transmit data valid
TSEC1_TX_ER	O	Transmit error
TSEC1_TX_ER	O	Transmit error

2.3.5 Monitor and Control (M/C)

Monitor and Control functions are divided essentially into Pre-operation and Operation. Pre-operation M/C deals with board configuration and system requirements. Operation M/C covers direct operational interfaces. For further information regarding Monitor and Control functions refer to chapters 2.3.4 and 4.

2.3.5.1 Pre-Operation M/C

Pre-operation M/C is a direct function of the application and the system requirements. These requirements dictate the EBC3 configuration as well as the overall system integration. Overall system integration and compliance with its requirements is beyond the scope of this manual.

2.3.5.2 Operation M/C

Operation M/C is primarily a function of the EBC3 driver software and the application. M/C signals are available, and, if implemented as part of the application, the operator as well as application software has access to these functions.

2.4 Board Interfaces

The following sections provide detailed information regarding the connector layout and pinout of the various board interfaces of the EBC3. The section ordering is by the connector designator.

2.4.1 J1 - 12V DC Power Input Connector

This connector is used for providing main input power to the EBC3 E²Brain™.

Figure 2-10: J1 - 12V DC Power Input Connector

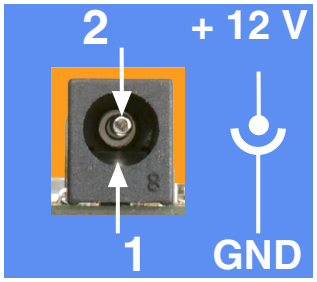


Table 2-29: Pinout of J1

PIN	DESCRIPTION
1	GND
2	+ 12 V DC

2.4.2 J2 - TTL Flat Panel Connector

This connector is used for providing interfacing for a TTL flat panel display, maximum 18-bit color resolution. It is a 40-pin, male, dual pinrow, shrouded connector.

Refer to section 2.4.30, JP1 VDDSAVE Jumper for selection of the VDDSAVE voltage.

Figure 2-11: J2 - TTL Flat Panel Connector

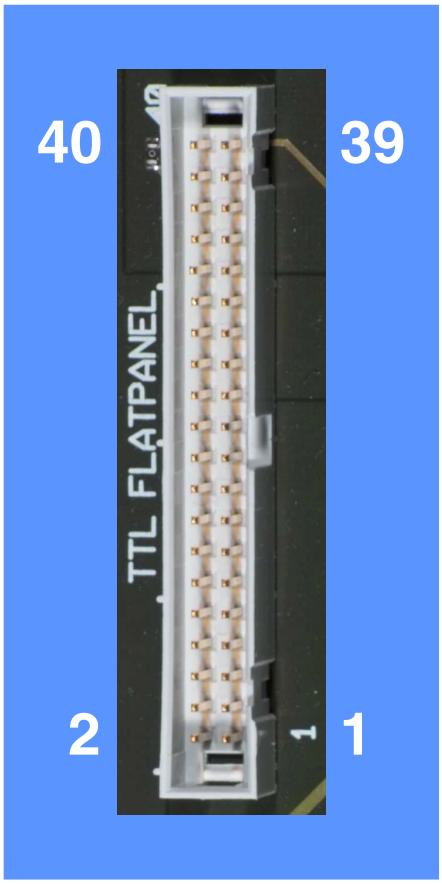


Table 2-30: Pinout of J2

SM501 SIGNAL	COLORS (18-BIT)	PIN	PIN	COLORS (18-BIT)	SM501 SIGNAL
GND	GND	1	2	SHFCLK	FPCLK
GND	GND	3	4	HSYNC	FP_HSYNC
FP_VSYNC	VSYNC	5	6	GND	GND
GND	GND	7	8	GND	GND
FP18	R2	9	10	R3	FP19
FP20	R4	11	12	GND	GND
FP21	R5	13	14	R6	FP22
FP23	R7	15	16	GND	GND
GND	GND	17	18	GND	GND
FP10	G2	19	20	G3	FP11
FP12	G4	21	22	GND	GND
FP13	G5	23	24	G6	FP14
FP15	G7	25	26	GND	GND
GND	GND	27	28	GND	GND
FP2	B2	29	30	B3	FP3
FP4	B4	31	32	GND	GND
FP5	B5	33	34	B6	FP6
FP7	B7	35	36	GND	GND
FP_DISP	DE	37	38	Scan dir select	VDDSAVE
VDDSAVE	VDDSAVE	39	40	VDDSAVE	VDDSAVE

2.4.3 J3 - Flat Panel Backlight Power Connector

This connector is used to provide input power for a flat panel backlight. The backlight input voltage is jumper selectable for either 3.3V or 5V and is turned on or off via a MOSFET controlled by the SM501_BIAS signal. The connector itself is a 6-pin, male, dual pinrow header connector.

Figure 2-12: J3 - FPBL Power Connector

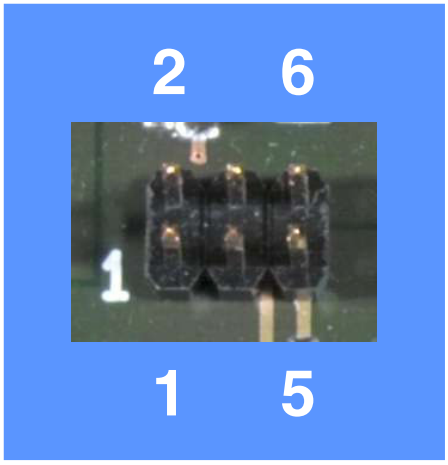


Table 2-31: Pinout of J3

PIN	SIGNAL	DESCRIPTION
1	3.3V	3.3 volt backlight input power (MOSFET supply voltage)
2	NC	Not connected
3	FP_BL_SUPPLY	Input voltage supply for MOSFET This voltage depends on source selected: jumpering of pins 1 and 3 of this connector supplies 3.3V; jumpering of pins 3 and 5 of this connector supplies 5V.
4	GND	Ground
5	5V	5 volt backlight input power (MOSFET supply voltage)
6	FP_BL_PWR	Flat panel backlight power input (drain of MOSFET) This is an output signal for supplying input power to a flat panel backlight. When signal SM501_BIAS is asserted, backlight power is turned on. Actual voltage supplied is a function of the jumpering of pins 1-3 or 3-5 (refer to description of pin 3 above).

2.4.4 J4 - TERM T/C Connector

This connector is used to provide serial terminal or console interfacing without hardware handshaking. This is a standard 9-pin, male, D-Sub connector.

Figure 2-13: J4 - TERM T/C Connector

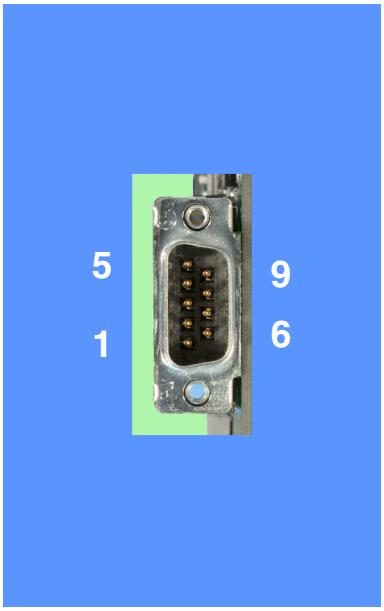


Table 2-32: Pinout of J4

PIN	SIGNAL	DESCRIPTION
1	NC	Not connected
2	RXD	Receive data
3	TXD	Transmit data
4	RS232+	RS232 positive voltage level
5	GND	Ground
6	NC	Not connected
7	RS232+	RS232 positive voltage level
8	NC	Not connected
9	NC	Not connected

2.4.5 J5 - Monitor and Control Signal Connector

This connector is used for providing selected monitor and control signal interfacing. It is a 6-pin, male, dual pinrow, header connector.

Figure 2-14: J5 - Monitor and Control Signal Connector

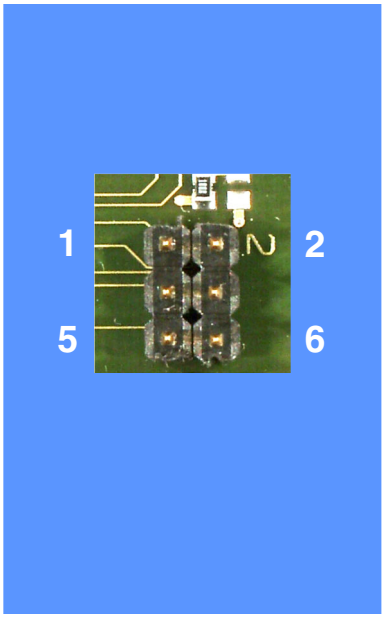


Table 2-33: Pinout of J5

PIN	SIGNAL	DESCRIPTION
1	MC5	Refer to the respective E²Brain™ module documentation for details
2	MC10	Refer to the respective E²Brain™ module documentation for details
3	MC2	Refer to the respective E²Brain™ module documentation for details
4	MC3	Refer to the respective E²Brain™ module documentation for details
5	MC9	Refer to the respective E²Brain™ module documentation for details
6	GND	Ground

2.4.6 J6 - ZV-PWM-MISC Signal Connector

This connector is used for providing interfacing for zoom video, TFT brightness control (PWM), and other control signals. It is a 40-pin, male, dual pinrow, shrouded connector.

Figure 2-15: J6 - ZV-PWM-MISC Connector

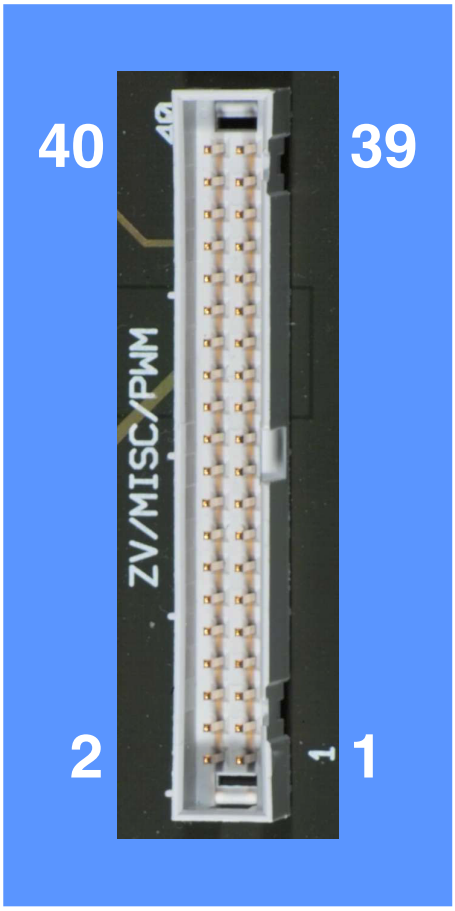


Table 2-34: Pinout of J6

SIGNAL	PIN	PIN	SIGNAL
GND	1	2	GND
ZV0	3	4	ZV1
ZV2	5	6	ZV3
ZV4	7	8	ZV5
ZV6	9	10	ZV7
3.3V	11	12	3.3V
FP0(B0) / GPIO56 / DCRT0 / ZV8	13	14	FP1(B1) / GPIO57 / DCRT1 / ZV9
FP8(G0) / GPIO58 / DCRT2 / ZV10	15	16	FP9(G1) / GPIO59 / DCRT3 / ZV11
FP16(R0) / GPIO60 / DCRT4 / ZV12	17	18	FP17(R1) / GPIO61 / DCRT5 / ZV13
GND	19	20	GND
ZV14 / DCRT6	21	22	ZV15 / DCRT7
ZV_VSYNC	23	24	ZV_HREF
ZV_CLK	25	26	12V
5V	27	28	5V
FP_EN (12V backlight)	29	30	SM501_BIAS (Backlight ON/OFF)
FP_VDEN / 3.3V/5V enable	31	32	SM501_GPIO55 / DCRT CLOCK)
VDDSAVE	33	34	VDDSAVE
PWM0	35	36	PWM1
PWM2	37	38	NC
GND	39	40	GND

2.4.7 J7 - DEBUG and Programming Connector

This connector is used for providing MPC8347 debugging interfacing. It is a 16-pin, male, dual pinrow, header connector. It can also be used to programm the CPLD on the EB8347 E²Brain™ module. Refer to the EB8347 E²Brain™ module manual for the JTAG configuration requirements.

Figure 2-16: J7 - Debug and Programming Connector

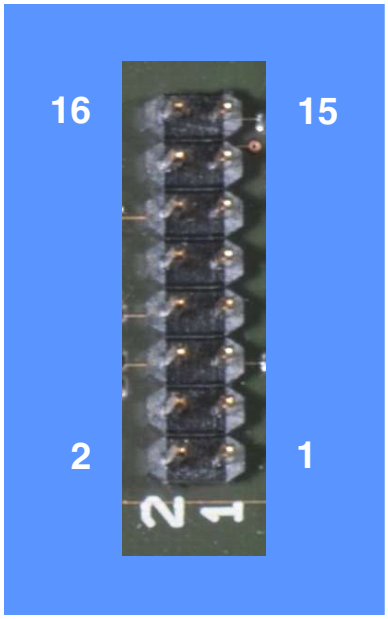


Table 2-35: Pinout of J7

PIN	SIGNAL
1	TDO
2	NC
3	TDI
4	TRST
5	Pull up 10 kΩ to +3.3V
6	TARGET_VCC
7	TCK
8	CHKSTP_IN
9	TMS
10	NC
11	SRST / HALT
12	GND
13	HRST
14	KEY (NC)
15	CHKSTP_OUT
16	GND

2.4.8 J8 - CONS T/C Connector

This connector is used to provide serial terminal or console interfacing without hardware handshaking. This is a standard 9-pin, male, D-Sub connector.

Figure 2-17: J8 - CONS T/C Connector

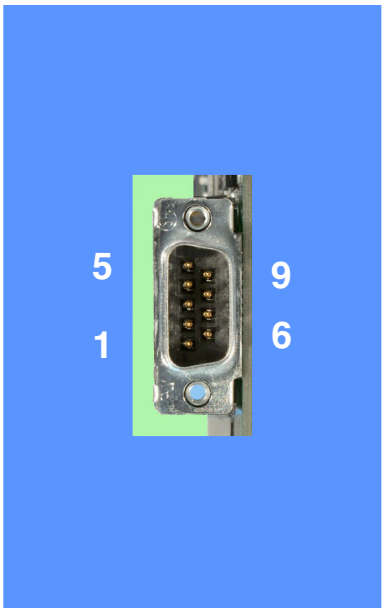


Table 2-36: Pinout of J8

PIN	SIGNAL	DESCRIPTION
1	NC	Not connected
2	RXD	Receive data
3	TXD	Transmit data
4	RS232+	RS232 positive voltage level
5	GND	Ground
6	NC	Not connected
7	RS232+	RS232 positive voltage level
8	NC	Not connected
9	NC	Not connected

2.4.9 J9 - INT2 T/P Interface

This jumper provides polarity control for SERIRQ testing. It is read in from and transferred inside the CPLD logic to the SERIRQ4 position of the SERIRQ signal. When set, the polarity is low, otherwise, it is high. This is a 2-pin, male, header connector.

2.4.10 J10 - INT1 T/P Interface

This jumper provides polarity control for SERIRQ testing. It is read in from and transferred inside the CPLD logic to the SERIRQ3 position of the SERIRQ signal. When set, the polarity is high, otherwise, it is low. This is a 2-pin, male, header connector.

2.4.11 J11 - Logic Programming Connector

This connector is used for providing a programming interface for the EBC3 logic controller. It is a 10-pin, male, dual pinrow, header connector.

Figure 2-18: J11 - Logic Programming Connector

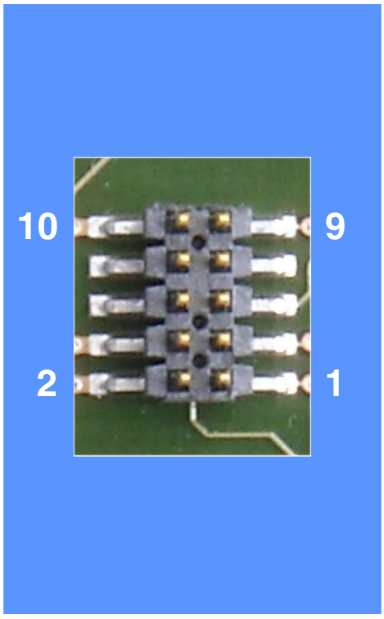


Table 2-37: Pinout of J11

PIN	SIGNAL
1	LTCK
2	GND
3	LTDO
4	+3.3V
5	LTMS
6	NC
7	NC
8	NC
9	LTDI
10	GND

2.4.12 J12 - F/LPCB Boot Select Interface

This jumper is used to select the source of the NetBootLoader boot software. When open, the source is the E²Brain™ module boot Flash. When set, the source is the EBC3 LPC Flash. This is a 2-pin, male, header connector.

2.4.13 J13 - PCI Expansion Slot 2 Connector

This connector is used for providing interfacing for one standard PC PCI board. J13 is a standard 124-pin, 3.3V coded, PC PCI expansion slot connector. Only universally or +3.3V coded PCI cards may used with this connector.

Figure 2-19: J13 - PCI Expansion Slot 2 Connector

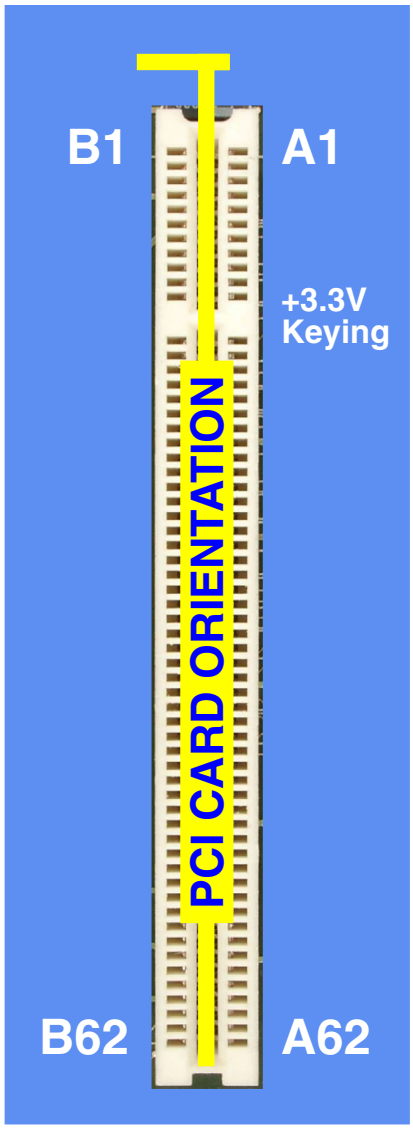


Table 2-38: Pinout of J13

SIGNAL	PIN	PIN	SIGNAL
RES	A1	B1	NC
+12V	A2	B2	RES
RES	A3	B3	GND
RES	A4	B4	NC
+5V	A5	B5	+5V
INTA#	A6	B6	+5V
INTC#	A7	B7	INTB#
+5V	A8	B8	INTD#
NC	A9	B9	NC
V(I/O)	A10	B10	NC
NC	A11	B11	NC
Key	A12	B12	Key
Key	A13	B13	Key
V_BAT	A14	B14	NC
RST#	A15	B15	GND
V(I/O)	A16	B16	CLK
GNT#	A17	B17	GND
GND	A18	B18	REQ#
NC	A19	B19	V(I/O)
AD30	A20	B20	AD31
+3.3V	A21	B21	AD29
AD28	A22	B22	GND
AD26	A23	B23	AD27
GND	A24	B24	AD25
AD24	A25	B25	+3.3V
IDSEL	A26	B26	C/BE3#
+3.3V	A27	B27	AD23
AD22	A28	B28	GND
AD20	A29	B29	AD21
GND	A30	B30	AD19
AD18	A31	B31	+3.3V

SIGNAL	PIN	PIN	SIGNAL
AD16	A32	B32	AD17
+3.3V	A33	B33	C/BE2#
FRAME#	A34	B34	GND
GND	A35	B35	IRDY#
TRDY#	A36	B36	+3.3V
GND	A37	B37	DEVSEL#
STOP#	A38	B38	GND
+3.3V	A39	B39	LOCK#
NC	A40	B40	PERR#
NC	A41	B41	+3.3V
GND	A42	B42	SERR#
PAR	A43	B43	+3.3V
AD15	A44	B44	C/BE1#
+3.3V	A45	B45	AD14
AD13	A46	B46	GND
AD11	A47	B47	AD12
GND	A48	B48	AD10
AD9	A49	B49	GND
GND	A50	B50	GND
GND	A51	B51	GND
C/BE0#	A52	B52	AD8
+3.3V	A53	B53	AD7
AD6	A54	B54	+3.3V
AD4	A55	B55	AD5
GND	A56	B56	AD3
AD2	A57	B57	GND
AD0	A58	B58	AD1
V(I/O)	A59	B59	V(I/O)
REQ64#	A60	B60	ACK64#
+5V	A61	B61	+5V
+5V	A62	B62	+5V

2.4.14 J14 - PCI Expansion Slot 1 Connector

This connector is used for providing interfacing for one standard PC PCI board. J14 is a standard 124-pin, 3.3V coded, PC PCI expansion slot connector. Only universally or +3.3V coded PCI cards may used with this connector.

Figure 2-20: J14 - PCI Expansion Slot 1 Connector

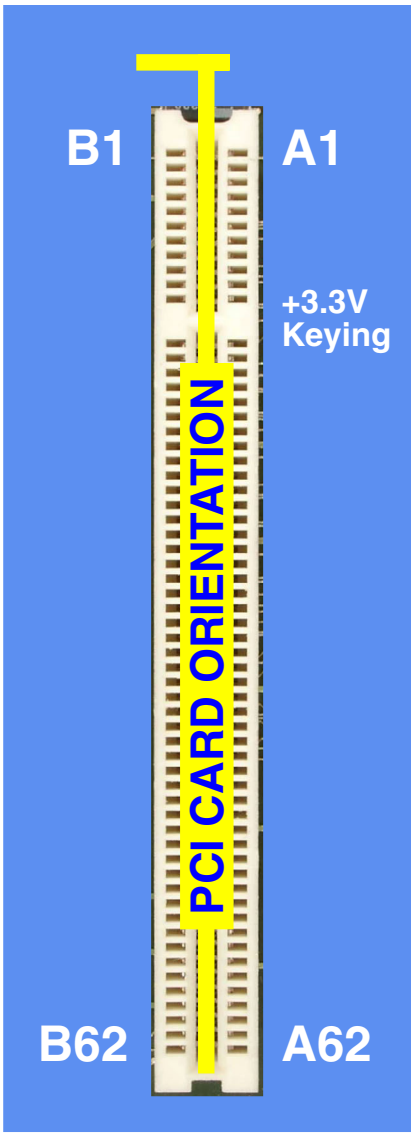


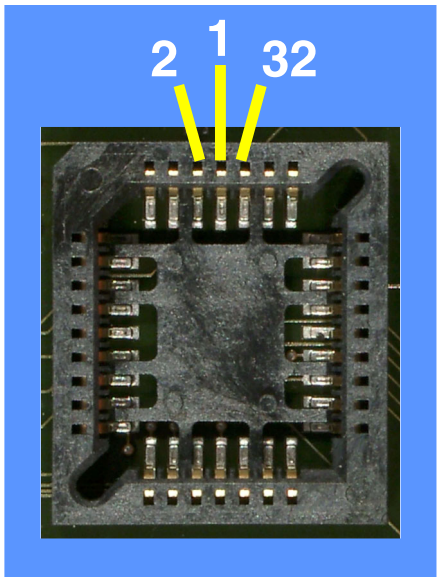
Table 2-39: Pinout of J14

SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL
RES	A1	B1	NC	AD16	A32	B32	AD17
+12V	A2	B2	RES	+3.3V	A33	B33	C/BE2#
RES	A3	B3	GND	FRAME#	A34	B34	GND
RES	A4	B4	NC	GND	A35	B35	IRDY#
+5V	A5	B5	+5V	TRDY#	A36	B36	+3.3V
INTA#	A6	B6	+5V	GND	A37	B37	DEVSEL#
INTC#	A7	B7	INTB#	STOP#	A38	B38	GND
+5V	A8	B8	INTD#	+3.3V	A39	B39	LOCK#
NC	A9	B9	NC	NC	A40	B40	PERR#
V(I/O)	A10	B10	NC	NC	A41	B41	+3.3V
NC	A11	B11	NC	GND	A42	B42	SERR#
Key	A12	B12	Key	PAR	A43	B43	+3.3V
Key	A13	B13	Key	AD15	A44	B44	C/BE1#
V_BAT	A14	B14	NC	+3.3V	A45	B45	AD14
RST#	A15	B15	GND	AD13	A46	B46	GND
V(I/O)	A16	B16	CLK	AD11	A47	B47	AD12
GNT#	A17	B17	GND	GND	A48	B48	AD10
GND	A18	B18	REQ#	AD9	A49	B49	GND
NC	A19	B19	V(I/O)	GND	A50	B50	GND
AD30	A20	B20	AD31	GND	A51	B51	GND
+3.3V	A21	B21	AD29	C/BE0#	A52	B52	AD8
AD28	A22	B22	GND	+3.3V	A53	B53	AD7
AD26	A23	B23	AD27	AD6	A54	B54	+3.3V
GND	A24	B24	AD25	AD4	A55	B55	AD5
AD24	A25	B25	+3.3V	GND	A56	B56	AD3
IDSEL	A26	B26	C/BE3#	AD2	A57	B57	GND
+3.3V	A27	B27	AD23	AD0	A58	B58	AD1
AD22	A28	B28	GND	V(I/O)	A59	B59	V(I/O)
AD20	A29	B29	AD21	REQ64#	A60	B60	ACK64#
GND	A30	B30	AD19	+5V	A61	B61	+5V
AD18	A31	B31	+3.3V	+5V	A62	B62	+5V

2.4.15 J15 - LPC Flash Socket

This PLCC socket connector is used to provide interfacing for one standard PLCC 32-pin Flash device. The EBC3 provides the capability of either booting from the onboard E²Brain™ module Flash or from the EBC3 onboard LPC Flash. The setting of the jumper J12 controls the selection of the source for the boot software.

Figure 2-21: J15 - LPC Flash Socket



2.4.16 J16 - CIE Extension Connector

This connector is used for providing interfacing for GPIO and Local Bus addressing signals for the EB8347 module. It is a 50-pin, male, dual pinrow, shrouded connector.

Figure 2-22: J16 - CIE Extension Connector

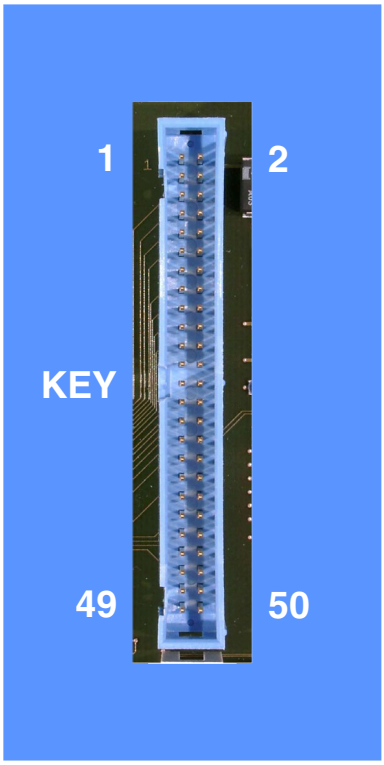


Table 2-40: Pinout of J16

SIGNAL	PIN	PIN	SIGNAL
3.3V	1	2	3.3V
LCS3	3	4	LCLK
GPIO23 (XA23)	5	6	GPIO22 (XA22)
GPIO21 (XA21)	7	8	GPIO20 (XA20)
GPIO19 (XA19)	9	10	GPIO18 (XA18
GND	11	12	GND
GPIO17 (XA17)	13	14	GPIO16 (XA16)
GPIO15 (XA15)	15	16	GPIO14 (XA14)
GPIO13 (XA13)	17	18	GPIO12 (XA12)
GPIO11 (XA11)	19	20	GPIO10 (XA10)
5V	21	22	5V
GPIO9 (XA9)	23	24	GPIO8 (XA8)
GPIO7 (XA7)	25	26	GPIO6 (XA6)
GPIO5 (XA5)	27	28	GPIO4 (XA4)
GPIO3 (XA3)	29	30	GPIO2 (XA2)
GPIO1 (XA1)	31	32	GPIO0 (XA0)
GND	33	34	GND
LGTA (LB hand-shake)	35	36	NC
3.3V	37	38	3.3V
NC	39	40	NC
NC	41	42	NC
GND	43	44	GND
NC	45	46	NC
NC	47	48	3.3V
5V	49	50	NC

2.4.17 J19 - SER1 HSS Connector

This connector is used to provide high speed RS232 four wire serial interfacing. This is a standard 9-pin, male, D-Sub connector.

Figure 2-23: J19 - SER1 HSS Connector

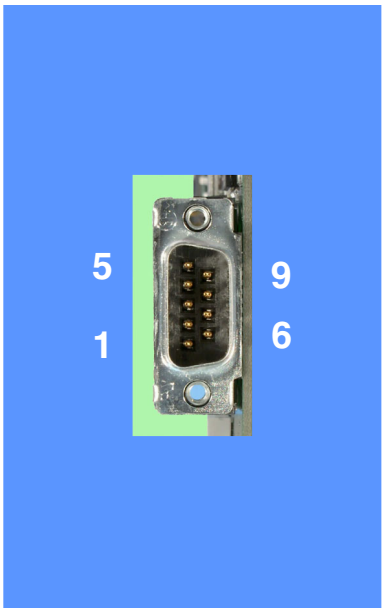


Table 2-41: Pinout of J19

PIN	RS232
1	Reserved
2	RXD
3	TXD
4	Reserved (This pin provides positive RS232 signal levels.)
5	GND
6	Reserved
7	RTS
8	CTS
9	Reserved

2.4.18 J20 - DIO Connector

This connector is used for providing four digital input and four digital output interfaces via the EBC3 logic controller. It is a 10-pin, male, dual pinrow, shrouded header connector.

Both the four inputs and the four outputs are defined as +3.3V TTL signalling GPIO, whereby the inputs accept 5V signal levels (up to a maximum of +5.5V DC). The digital outputs have a drive capacity of a maximum of 24mA, reduced to 12mA to guarantee the TTL output levels (0.4V Low and 2.4V High).

The digital general purpose I/O can be accessed via read/write cycles in the LPC IO-Space (offset address digital inputs: 0x00; offset address digital outputs: 0x01).

Figure 2-24: J20 - DIO Connector

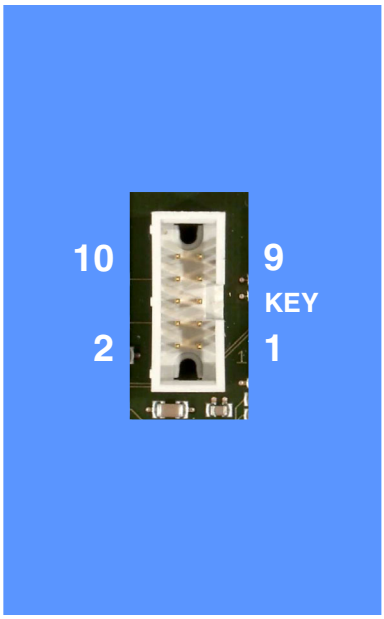


Table 2-42: Pinout of J20

PIN	SIGNAL
1	DO0
2	DI0
3	DO1
4	DI1
5	DO2
6	DI2
7	DO3
8	DI3
9	+3.3V
10	GND

2.4.19 J21 - SER2 HSS Connector

This connector is used to provide high speed RS232 full modem or RS422/RS485 serial interfacing. This is a standard 9-pin, male, D-Sub connector.

Figure 2-25: J21 - SER2 HSS Connector

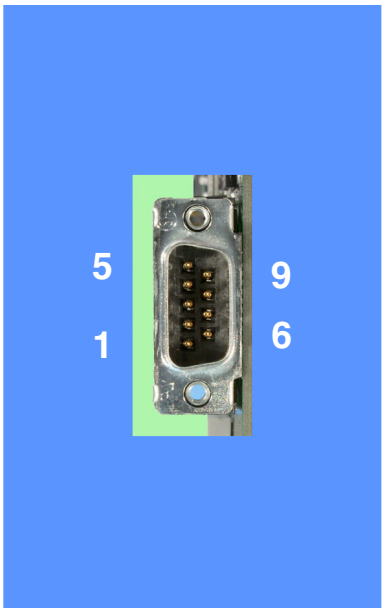


Table 2-43: Pinout of J21

PIN	RS232
1	Reserved
2	RXD
3	TXD
4	Reserved (This pin provides positive RS232 signal levels.)
5	GND
6	Reserved
7	RTS
8	CTS
9	Reserved

2.4.20 J24 - Mini PCI Connector

The EBC2 has one, 32-bit, 33 MHz, standard 124-pin Mini-PCI socket which accepts all type III Mini PCI boards. This interface supports a wide range of available Mini-PCI modules.

The Mini-PCI connector is a 124-pin card edge type connector that is similar to the SO-DIMM type. In the Mini-PCI specification this connecter is defined as “Type III”.

The maximum permitted height for the Mini PCI connector and the Mini PCI module is 8 mm.

Figure 2-26: J24 - Mini PCI Connector

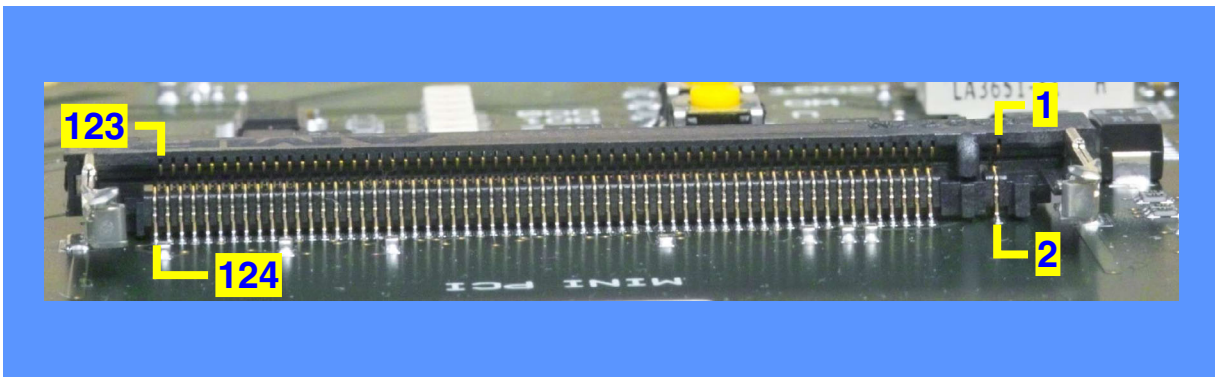


Table 2-44: Pinout of J24

SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL
NC	1	2	NC	3.3V	63	64	FRAME#
NC	3	4	NC	CLKRUN#	65	66	TRDY#
NC	5	6	NC	SERR#	67	68	STOP#
NC	7	8	NC	GND	69	70	3.3V
NC	9	10	NC	PERR#	71	72	DEVSEL#
NC	11	12	NC	C/BE[1]#	73	74	GND
NC	13	14	NC	AD[14]	75	76	AD[15]
NC	15	16	RESERVED	GND	77	78	AD[13]
INTB#	17	18	+5V	AD[12]	79	80	AD[11]
3.3V	19	20	INTA#	AD[10]	81	82	GND
RESERVED	21	22	RESERVED	GND	83	84	AD[09]
GND	23	24	3.3VAUX	AD[08]	85	86	C/BE[0]#
CLK	25	26	RST#	AD[07]	87	88	3.3V
GND	27	28	3.3V	3.3V	89	90	AD[06]
REQ#	29	30	GNT#	AD[05]	91	92	AD[04]
3.3V	31	32	GND	RESERVED	93	94	AD[02]
AD[31]	33	34	NC	AD[03]	95	96	AD[00]
AD[29]	35	36	RESERVED	+5V	97	98	NC
GND	37	38	AD[30]	AD[01]	99	100	NC
AD[27]	39	40	3.3V	GND	101	102	GND
AD[25]	41	42	AD[28]	NC	103	104	GND
NC	43	44	AD[26]	NC	105	106	NC
C/BE[3]#	45	46	AD[24]	NC	107	108	NC
AD[23]	47	48	IDSEL	NC	109	110	NC
GND	49	50	GND	NC	111	112	RESERVED
AD[21]	51	52	AD[22]	GND	113	114	GND
AD[19]	53	54	AD[20]	NC	115	116	NC
GND	55	56	PAR	GND	117	118	GND
AD[17]	57	58	AD[18]	GND	119	120	NC
C/BE[2]#	59	60	AD[16]	NC	121	122	RESERVED
IRDY#	61	62	GND	RESERVED	123	124	3.3VAUX

2.4.21 J25 - SPI Connector

This connector is used for providing a serial peripheral interface for external devices. It is a 6-pin, male, single pinrow, header connector.

Refer to section 2.4.31, JP2 SPI Select Connector for further information on the use on this connector.

Figure 2-27: J25 - SPI Connector

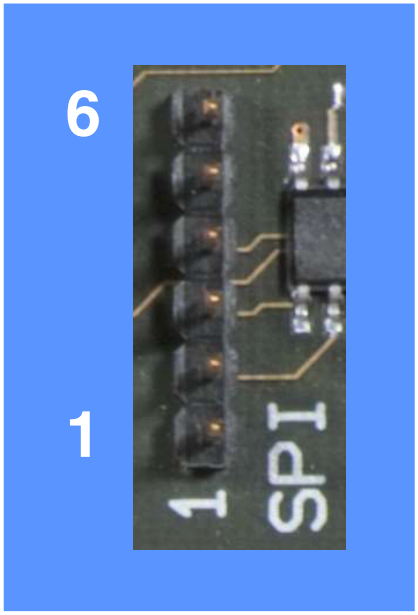


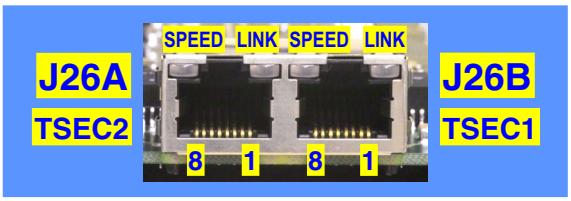
Table 2-45: Pinout of J25

PIN	SIGNAL
1	3.3V
2	SPI_CLK
3	SPI_MOSI
4	SPI_MISO
5	SPI_SEL
6	GND

2.4.22 J26 - Dual Gigabit Ethernet Connector

This connector provides interfacing for E²Brain™ modules which support the three speed Ethernet channels TSEC1 and TSEC2. This is a dual RJ45 connector with LEDs to indicate the status of the links.

Figure 2-28: J26 - Dual Gigabit Ethernet Connector



LED OPERATION:

LINK	OFF:	link not active
	GREEN:	link active
SPEED	OFF:	10 Mbps
	GREEN:	100 Mbps
	YELLOW:	1000 Mbps

Table 2-46: Pinouts of J26A and J26B Based on the Implementation

MDI / Standard Ethernet Cable						PIN	MDIX / Crossed Ethernet Cable					
10BASE-T		100BASE-TX		1000BASE-T			10BASE-T		100BASE-TX		1000BASE-T	
I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL		I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
O	TX+	O	TX+	I/O	BI_DA+	1	I	RX+	I	RX+	I/O	BI_DB+
O	TX-	O	TX-	I/O	BI_DA-	2	I	RX-	I	RX-	I/O	BI_DB-
I	RX+	I	RX+	I/O	BI_DB+	3	O	TX+	O	TX+	I/O	BI_DA+
-	-	-	-	I/O	BI_DC+	4	-	-	-	-	I/O	BI_DD+
-	-	-	-	I/O	BI_DC-	5	-	-	-	-	I/O	BI_DD-
I	RX-	I	RX-	I/O	BI_DB-	6	O	TX-	O	TX-	I/O	BI_DA-
-	-	-	-	I/O	BI_DD+	7	-	-	-	-	I/O	BI_DC+
-	-	-	-	I/O	BI_DD-	8	-	-	-	-	I/O	BI_DC-

Note ...

The Gigabit PHYs support automatic MDI/MDIX crossover at all speeds of operation. Therefore both standard as well as crossed Ethernet cables can be used with these interfaces.

2.4.23 J28 - CompactFLASH Type II Connector

This connector is used for providing interfacing for CompactFLASH Type II devices. The E²Brain™ modules that are supported by the EBC3 all provide a direct CF interface without a bridging device. It is a standard Type II CompactFLASH connector assembly with a 50-pin, male, dual pinrow connector.

Figure 2-29: J28 - CompactFlash Connector

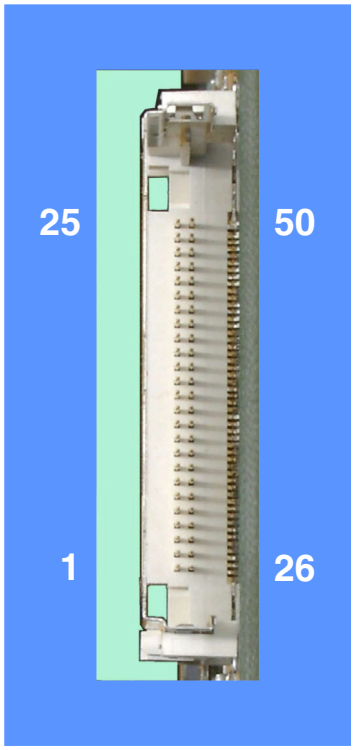


Table 2-47: Pinout of J28

SIGNAL	PIN	PIN	SIGNAL
GND	1	26	CF_CD1
CF_D3	2	27	CF_D11
CF_D4	3	28	CF_D12
CF_D5	4	29	CF_D13
CF_D6	5	30	CF_D14
CF_D7	6	31	CF_D15
CF_CS0	7	32	CF_CS1
GND	8	33	GND
GND	9	34	CF_RD
GND	10	35	CF_WR
GND	11	36	+3.3V
GND	12	37	CF_IRQ
+3.3V	13	38	+3.3V
GND	14	39	GND
GND	15	40	NC
GND	16	41	CF_RST
GND	17	42	CF_IORDY
CF_A2	18	43	CF_DMAREQ
CF_A1	19	44	CF_DMAACK
CF_A0	20	45	CF_DASP
CF_D0	21	46	CF_PDIAG
CF_D1	22	47	CF_D8
CF_D2	23	48	CF_D9
CF_CS16	24	49	CF_D10
CF_CD2	25	50	GND

2.4.24 J29 - USB1 Connector

This connector is used for providing a host USB 2.0 interface for E²Brain™ modules. It is a standard USB type A receptacle connector.

Figure 2-30: J29 - USB1 Connector

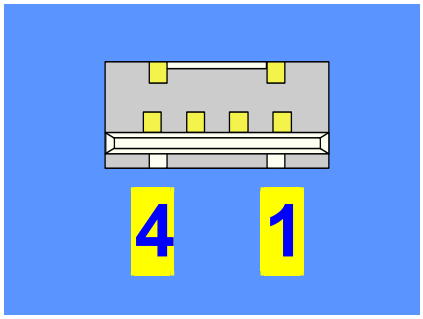


Table 2-48: Pinout of J29

PIN	SIGNAL
1	VCC
2	DATA-
3	DATA+
4	GND

2.4.25 J30 - USB2 Connector

This connector is used for providing a host or a device USB 2.0 interface for EB8347 E²Brain™ module. It is a standard USB type mini AB receptacle connector.

Figure 2-31: J30 - USB2 Connector

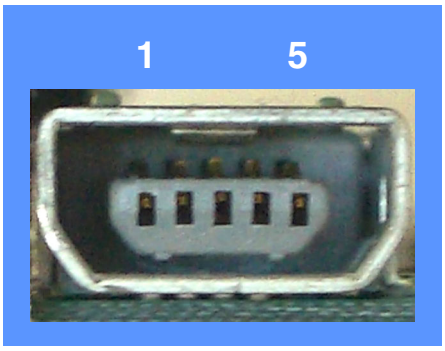


Table 2-49: Pinout of J30

PIN	SIGNAL
1	VCC
2	DATA-
3	DATA+
4	ID
5	GND

2.4.26 J31 - DVI Connector

This connector is used to provide a standard DVI interface for TFT displays. It is a 30-contact, female DVI compliant combined analog and digital receptacle connector.

Figure 2-32: J31 DVI Connector

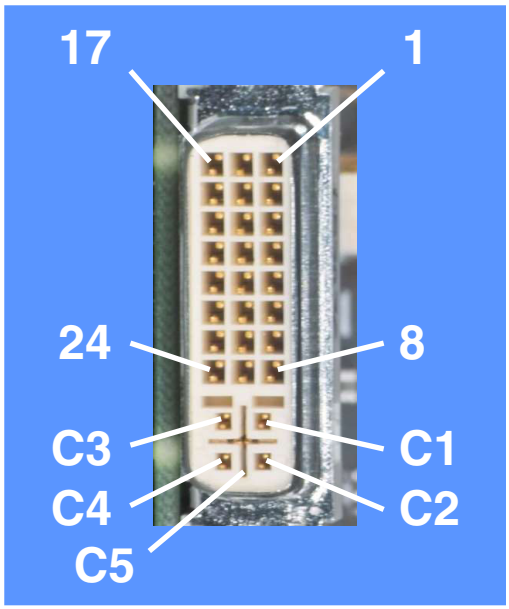


Table 2-50: Pinout of J31

SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN
DVI_TXOUT2-	1	DVI_TXOUT1-	9	DVI_TXOUT0-	17
DVI_TXOUT2+	2	DVI_TXOUT1+	10	DVI_TXOUT0+	18
GND	3	GND	11	GND	19
NC	4	NC	12	NC	20
NC	5	NC	13	NC	21
RESERVED	6	VCC_DVI	14	GND	22
RESERVED	7	GND	15	DVI_TXCLK+	23
CRT_VSYNC	8	NC	16	DVI_TXCLK-	24
CRT_R	C1	CRT_G	C2	CRT_B	C3
CRT_HSYNC	C4	GND	C5	GND	C5A

2.4.27 J32 - Microphone In (MIC) Audio Connector

The EBC3 provides a 3.5mm audio jack for connecting a stereo microphone to the AC97 Codec. The stereo signal is added together to provide a mono signal for the CS4299A Codec microphone input.

The following figures provide further connector and circuit connection information for J32.

Figure 2-33: J32 MIC Connector

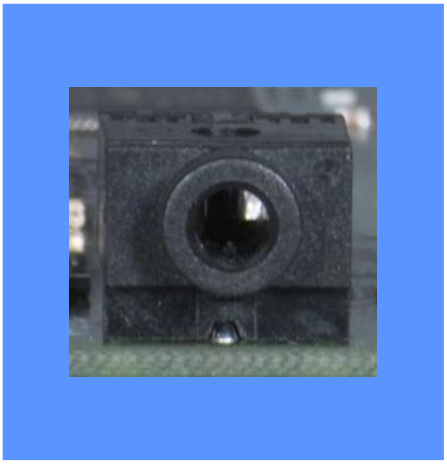
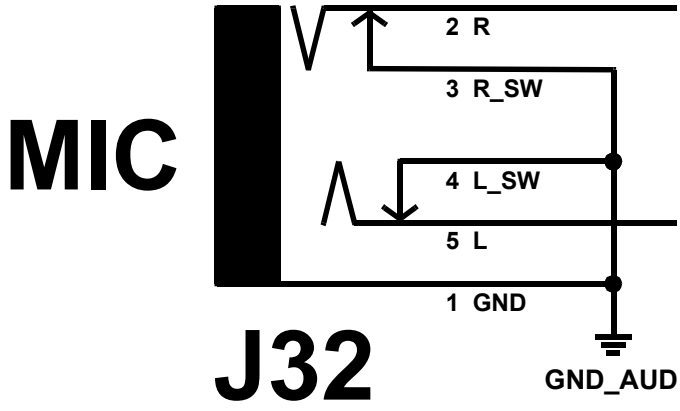


Figure 2-34: J32 MIC Circuit Connections



2.4.28 J33 - LINE IN Audio Connector

The EBC3 provides a 3.5mm audio jack to support a line level stereo input capabiliy. The signals are routed to the Line_In_R and Line_In_L inputs of the CS4299A.

The following figures provide further connector and circuit connection information for J33.

Figure 2-35: J33 LINE IN Connector

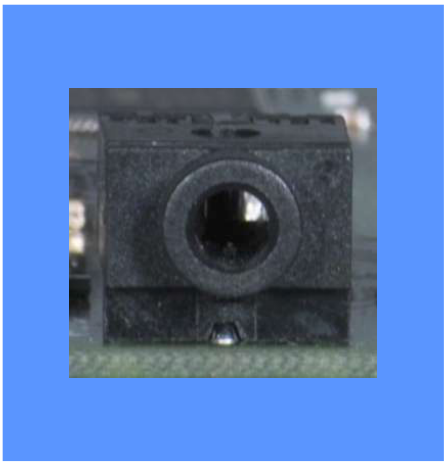
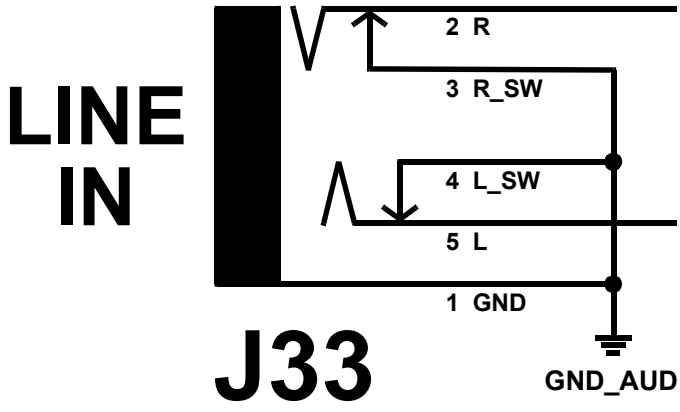


Figure 2-36: J33 LINE IN Circuit Connections



2.4.29 J34 - LINE OUT Audio Connector

The EBC3 provides a 3.5mm audio jack to support a line level stereo output audio signal. This signals are routed to the Line_Out_R and Line_Out_L outputs of the CS4299A.

The following figures provide further connector and circuit connection information for J33.

Figure 2-37: J34 LINE OUT Connector

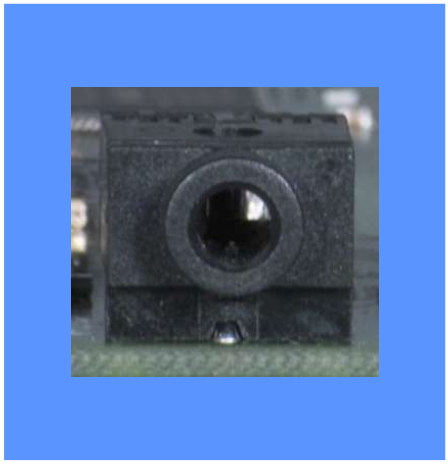
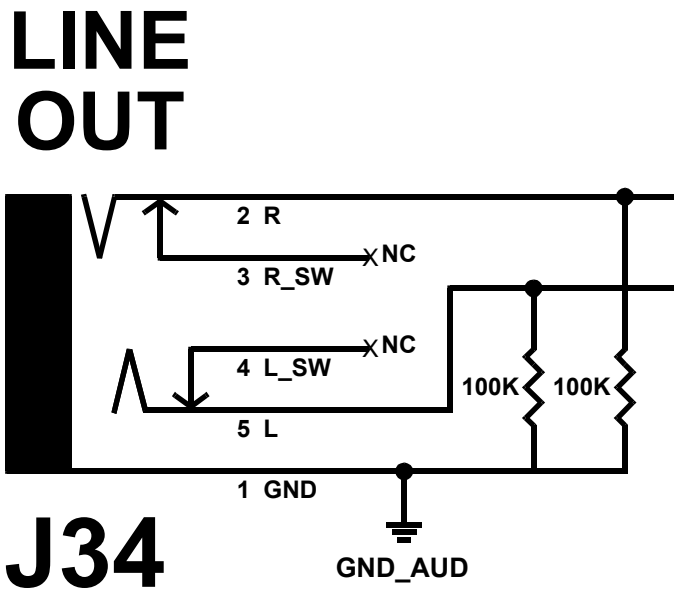


Figure 2-38: J34 LINE OUT Circuit Connections



2.4.30 JP1 - VDDSAVE Jumper

This jumper is used to select the input voltage supply for VDDSAVE which is supplied to the TTL flat panel connector, J2. It is a jumperable, 3-pin, male, single pinrow, header connector.

Jumpering pins 1 and 2 supplies +3.3V VDDSAVE. Jumpering pins 2 and 3 supplies +5V VDDSAVE.

Figure 2-39: JP1 - VDDSAVE Jumper

Table 2-51: Pinout of JP1

PIN	SIGNAL
1	+3.3V
2	VDDSAVE
3	+5V

2.4.31 JP2 - SPI Select Connector

JP2 is despite its naming is not a jumper, but rather a 3-pin connector. This connector is used to route various possible SPI_SEL signals to specific devices. It is a 3-pin, male, single pinrow, header connector.

Figure 2-40: JP2 - SPI Select Connector

Table 2-52: Pinout of JP2

PIN	SIGNAL	DESCRIPTION
1	SPI_SEL_EEPROM	Selects EBC3 onboard EEPROM
2	SPI_SEL_CPU	Selects E²Brain module CPU
3	SPI_SEL_OFFBOARD	Selects external SPI device

The SPI bus is a universal bus which requires dedicated device select signals for each device on the bus. The EB8347/EBC3 supplies the SPI bus, but only one device select signal (SPI_SEL) is provided as an input signal for the E²Brain module CPU as a slave device.

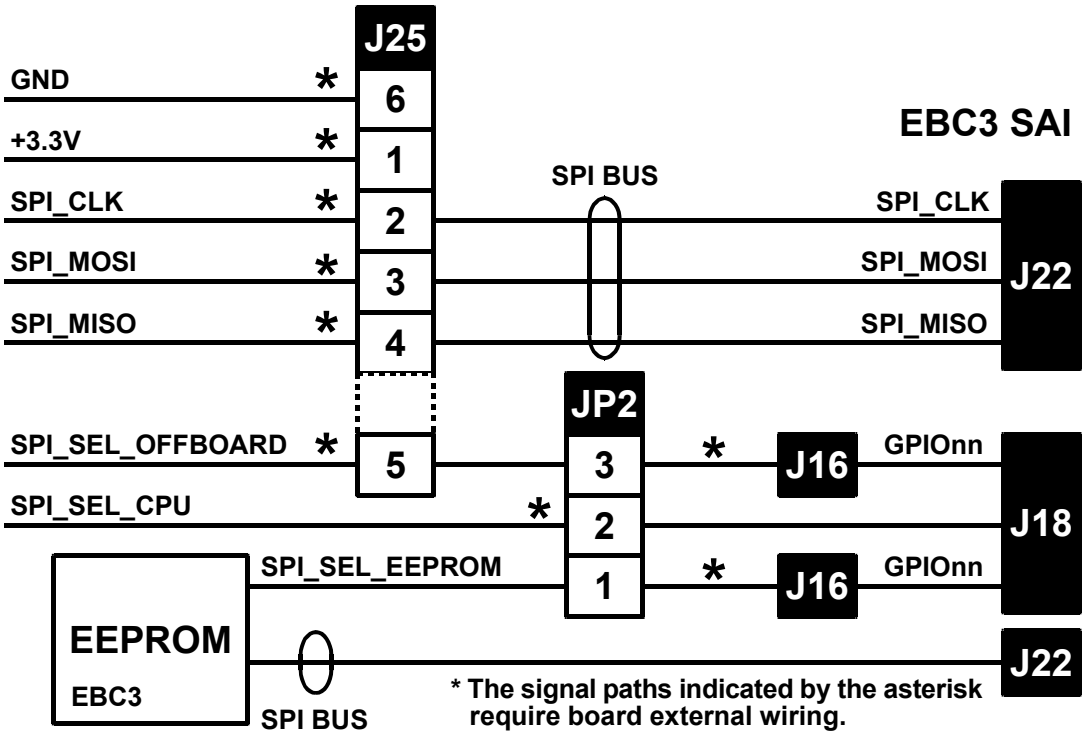
To select other devices on the SPI bus, there are several possibilites depending on the location of the device.

The optional SPI EEPROM on the EB8347 is selected via the BPCC logic.

The EBC3 onboard SPI EEPROM is selected via a user defined GPIO signal. To select an off-board SPI device, another user definable GPIO is required.

In conjunction with J16 and J25, the JP2 connector provides routing capability for these signals. The following figure demonstrates the routing configuration for SPI_SEL signals and the SPI bus.

Figure 2-41: SPI Selection Configuration



2.5 Monitor and Control Interfaces

The following sections provide detailed information regarding the monitor and control functions available on the EBC3.

2.5.1 Operational Status Indicators - LEDs

There are 16 operational status indicators available on the EBC3 for monitoring of the board operation. In addition to these indicators, each of the Ethernet connectors has two LEDs which provide link status information which has been described along with the connectors.The following table provides an overview of these indicators.

Table 2-53: EBC3 Operational Status Indicators (LEDs)

DES.	NAME	COLOR	DESCRIPTION
D2	12V	GREEN	When on is general indication that +12V supply is functioning
D4	5V	GREEN	When on is general indication that +5V supply is functioning
D5	3.3V	GREEN	When on is general indication that +3.3V supply is functioning
D8	DIN0	GREEN	Indicates DIN(0) signal is asserted
D9	DIN1	GREEN	Indicates DIN(1) signal is asserted
D10	DIN2	GREEN	Indicates DIN(2) signal is asserted
D11	DIN3	GREEN	Indicates DIN(3) signal is asserted
D12	DOUT3	YELLOW	Indicates DOUT(3) signal is asserted
D13	DOUT2	YELLOW	Indicates DOUT(2) signal is asserted
D14	DOUT1	YELLOW	Indicates DOUT(1) signal is asserted
D15	DOUT0	YELLOW	Indicates DOUT(0) signal is asserted
D16	GPIO	RED	General purpose indicator
D17	WDOG	YELLOW	Used to indicate the status of the E²Brain™ module watchdog Is a function of the application. If not used, remains off.
D18	BOOT	GREEN	General purpose indicator Used by bootloader to indicate boot status. After bootup is completed, is available for application use. At start of bootup, is flashing to indicate that bootup may be interrupted by pressing SW1. Refer to the corresponding E²Brain™ product documentation for further information.
D20	7SHN	RED	Seven segment LED, most significant nibble General purpose indicator for POST codes and application
D21	7SLN	RED	Seven segment LED, least significant nibble General purpose indicator for POST codes and application

2.5.2 Operator Switches - SW1, SW2, SW3, and SW4

There are four operator switches available on the EBC3 for interaction with the system. SW1 is the main power switch for the EBC3. SW3 can be used to invoke a system reset, and SW2 can be used to invoke a system abort. SW2 is used during the boot operation to cause the E²Brain™ module to abort the boot operation and allow command line inputs to the bootloader. Refer to the E²Brain™ module manual for further information.

SW4 is an eight pole DIP switch which is reserved for future use.

2.5.3 M / C Signals

In addition to the above mentioned interfaces, there are monitor and control signals available for application development and usage. Refer to sections 2.3.1.3, 2.4.5, and the E²Brain™ module product documentation for further information.

Chapter 3

Installation

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3. Installation

The EBC3 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board or injury to personnel.

3.1 Hardware Installation

The product described in this manual may only be mounted on an appropriate E²Brain™ carrier board which is specifically designed for this E²Brain™ module.

3.1.1 Safety Requirements

The module must be securely fastened to the carrier board using the mounting standoffs and screws provided with the module.

In addition the following electrical hazard precautions must be observed.

CAUTION, ELECTRIC SHOCK!

Ensure that the system main power is removed prior to installing or removing this board. Ensure that there are no other external voltages or signals being applied to this board or other boards within the system. Failure to comply with the above could endanger your life or health and may cause damage to this board or other system components including process-side signal conditioning equipment.

ESD Sensitive Device!

This Kontron board contains electrostatic sensitive devices. Please observe the following precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

Do not touch any on board components, connector pins, or board conductive circuits.

If working at an anti-static workbench with professional discharging equipment, ensure compliance with its usage when handling this product.

3.1.2 Installation Procedures

To install this EBC3 module proceed as follows:

1. Ensure that the handling and safety requirements indicated in chapter 3.1.1 are observed.

WARNING!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation. Please refer to chapters 4 for configuration information.

2. Ensure that the board is properly configured for operation before installing.

Note ...

Care must be taken when applying the procedures below to ensure that when the board is assembled along with the other application system components that it is not damaged through contact with the other components of the system.

3. Ensure that the associated E²Brain™ module is properly installed on the EBC3.

WARNING!

The EBC3 is designed for use only with E²Brain™ modules that comply with Kontron's E²Brain™ specification. Use of any other type of E²Brain™ module with the EBC3 will result in improper operation and possibly cause damage to the E²Brain™ module as well as the EBC3.

4. Assemble the EBC3 within the application system as required. See appropriate system documentation for assembly procedures.

3.1.3 Removal Procedures

To remove the EBC3 proceed as follows:

1. Ensure that the safety requirements indicated in chapter 3.1.1 are observed.

WARNING!

Care must be taken when applying the procedures below to ensure that when the board is removed it is not damaged through contact with other components in the system.

2. Disassemble the EBC3 within the application sub-system as required. See appropriate system documentation for disassembly procedures.
3. Dispose of the EBC3 as required observing applicable environmental regulations governing the handling and disposition of this type of product.

Chapter 4

Configuration

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4. Configuration

The following sections provide system integrators with detailed information for configuring the EBC3 module for operation

4.1 Jumper Settings

The EBC3 board has only one jumper, JP1, which is described in detail in section 2.

4.2 V(I/O) Configuration

The EBC3 is configured for +3.3V V(I/O) operation and cannot be configured for +5V. Only universally coded or +3.3V coded PCI cards may be used with this board. The PCI connectors J13 and J14 are +3.3V key coded. Refer to sections 2.4.13 and 2.4.14 for orientation information for PCI expansion boards.

4.3 LPC Address Mapping

The following table indicates the LPC address mapping for access to the digital input, digital output, and POST code data.

Table 4-1: LPC Address Mapping

REGISTER	LPC I/O ADDRESS OFFSET
DIN_DATA	0x0000 0000
DOUT_DATA	0x0000 0001
POST_CODE_DATA	0x0000 0080

The address map describes the offset location for the LPC I/O area. The LPC I/O address itself is a function of the corresponding E²Brain™ module.

4.4 PCI Bus IDSEL Mapping and IRQ Routing

The IRQ´s of the different PCI devices on the EBC3 must be distributed to the four PCI interrupts (INTA#, INTB#, INTC#, INTD#) of the E²Brain™ module. In the same manner, different PCI ADxx lines from the E²Brain™ module must be connected to the IDSEL input of the PCI devices on the EBC3.

The following table provides the realized routing on the EBC3 with the corresponding PCI device.

Table 4-2: IDSEL Mapping and IRQ Routing

EBC3 PCI DEVICE	EBC3 IDSEL ← ADXX E²Brain™ MODULE	PCI INTERRUPT E²Brain™ MODULE
PCI connector slot 1, J14	AD28	
INTA#		INTA#
INTB#		INTB#
INTC#		INTC#
INTD#		INTD#
PCI connector slot 2, J13	AD27	
INTA#		INTD#
INTB#		INTA#
INTC#		INTB#
INTD#		INTC#
Mini PCI slot, J24	AD26	
INTA#		INTC#
INTB#		INTD#

For further information concerning this subject, please contact Kontron Modular Computers.

4.5 EBC3 Register Description

The following sections provide register descriptions for the:

- Digital Input Data Register
- Digital Output Data Register
- POST Code Data Register

4.5.1 Digital Input Data Register

The digital input data register indicates the status of the respective input signals.

Address Offset: 0x0000 0000
Format: Byte
Access: Read
Value after reset: 0x00 (if inputs are left open)

Digital input channels 0 to 3 are active, channels 4 to 7 are not used.

Table 4-3: Digital Input Data Register

REGISTER NAME		Digital Input Data Register						ACCESS	
ADDRESS		0x0000 0000 (offset)						R	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		DIN_ DATA_7	DIN_ DATA_6	DIN_ DATA_5	DIN_ DATA_4	DIN_ DATA_3	DIN_ DATA_2	DIN_ DATA_1	DIN_ DATA_0
DEFAULT		0	0	0	0	0	0	0	0
0	DIN_ DATA_0	0	Input signal is low or open						
		1	Input signal is high						
1	DIN_ DATA_1	0	Input signal is low or open						
		1	Input signal is high						
2	DIN_ DATA_2	0	Input signal is low or open						
		1	Input signal is high						
3	DIN_ DATA_3	0	Input signal is low or open						
		1	Input signal is high						
4	DIN_ DATA_4	0	Channel not used						
		1							
5	DIN_ DATA_5	0	Channel not used						
		1							
6	DIN_ DATA_6	0	Channel not used						
		1							
7	DIN_ DATA_7	0	Channel not used						
		1							

4.5.2 Digital Output Data Register

The digital output data register controls the digital output port or indicates the status of the respective output signals in the case of a read access.

Address Offset: 0x0000 0001
Format: Byte
Access: Read and write
Value after reset: 0x00

The bits 0 to 3 set the outputs according to the programmed value and reflect the status of the respective digital output channel in the case of a read access. The bits 4 to 7 are reserved.

Table 4-4: Digital Output Data Register

REGISTER NAME		Digital Output Data Register						ACCESS	
ADDRESS		0x0000 0001 (offset)						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		DOUT_DATA_7	DOUT_DATA_6	DOUT_DATA_5	DOUT_DATA_4	DOUT_DATA_3	DOUT_DATA_2	DOUT_DATA_1	DOUT_DATA_0
DEFAULT		0	0	0	0	0	0	0	0
0	DOUT_DATA_0	0	TTL signal level 0						
		1	TTL signal level 1						
1	DOUT_DATA_1	0	TTL signal level 0						
		1	TTL signal level 1						
2	DOUT_DATA_2	0	TTL signal level 0						
		1	TTL signal level 1						
3	DOUT_DATA_3	0	TTL signal level 0						
		1	TTL signal level 1						
4	DOUT_DATA_4	0	Channel not used						
		1							
5	DOUT_DATA_5	0	Channel not used						
		1							
6	DOUT_DATA_6	0	Channel not used						
		1							
7	DOUT_DATA_7	0	Channel not used						
		1							

4.5.3 POST Code Data Register

The POST code data register is used to control the seven segment LED displays and to indicate the status of the respective display in the case of a read access.

Address Offset: 0x0000 0080
Format: Byte
Access: Read and write
Value after reset: 0x5F (indicates that the boot process has been completed)

LED D20 indicates the value of the higher nibble of the register, whereas, LED D21 indicates the value of the lower nibble of the register.

Table 4-5: POST Code Data Register

REGISTER NAME		POST Code Data Register						ACCESS	
ADDRESS		0x0000 0080 (offset)						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		POST_CODE_DATA_7	POST_CODE_DATA_6	POST_CODE_DATA_5	POST_CODE_DATA_4	POST_CODE_DATA_3	POST_CODE_DATA_2	POST_CODE_DATA_1	POST_CODE_DATA_0
DEFAULT		0	0	0	0	0	0	0	0
0	POST_CODE_DATA_0	0	Register lower nibble: display indicates in hexadecimal value: **BITS 3 2 1 0** **HEX** **DISPLAY: D21** 0 0 0 0 0x0 0 • • • 1 1 1 1 0xF F						
		1							
1	POST_CODE_DATA_1	0							
		1							
2	POST_CODE_DATA_2	0							
		1							
3	POST_CODE_DATA_3	0							
		1							
4	POST_CODE_DATA_4	0	Register higher nibble: display indicates in hexadecimal value: **BITS 7 6 5 4** **HEX** **DISPLAY: D20** 0 0 0 0 0x0 0 • • • 1 1 1 1 0xF F						
		1							
5	POST_CODE_DATA_5	0							
		1							
6	POST_CODE_DATA_6	0							
		1							
7	POST_CODE_DATA_7	0							
		1							

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