


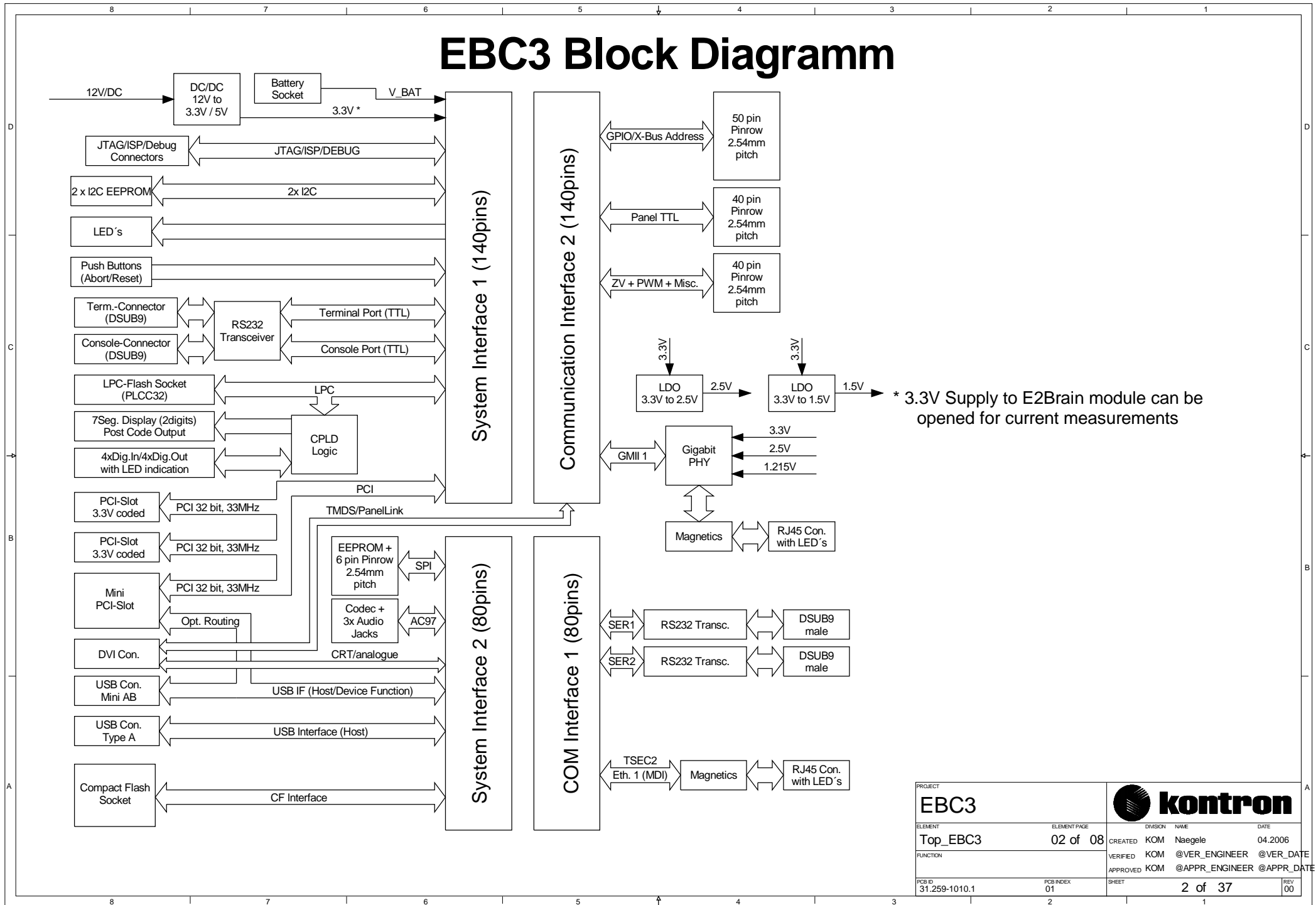
EBC3 E2Brain Carrier for E2Brain CPU module EB8347

Table of Contents

Cover Sheet	1	Panel Connectors	26
EBC3 Block Diagramm	2	USB Interface 0, 1	22 - 23
Diagram Clock Distribution	3	Audio (AC97 Codec)	24 - 25
Diagram Reset Structure	4	RS232 Terminal/Console Interface	26
Diagram Power Supply Structure	5	Serial Interfaces SER1 - SER2	27 - 30
Diagram Interrupt Structure	6	Digital Input/Output Interface	31
Resource Tables	7	LPC Flash Socket	32
Schematic TOP HIERARCHY	8	Compact Flash Socket	33
Hierarchy, Interface Connectors	9	CPLD Logic	34
System Interface1 Connector	10	JTAG Debugging and Programming Connectors	35
System Interface2 Connector	11	SPI	36
Communication IF1 Connector	12	Miscellaneous, Monitor and Control	37
Communication IF2 Connector	13	Power Supply	38 - 39
Hierarchy, PCI Connectors/Slots	14		
PCI Slot 1	15		
PCI Slot 2	16		
Mini PCI Extension	17		
Gigabit Ethernet PHY1	18 - 19		
Gigabit Magnetics, RJ45 Connectors	20		

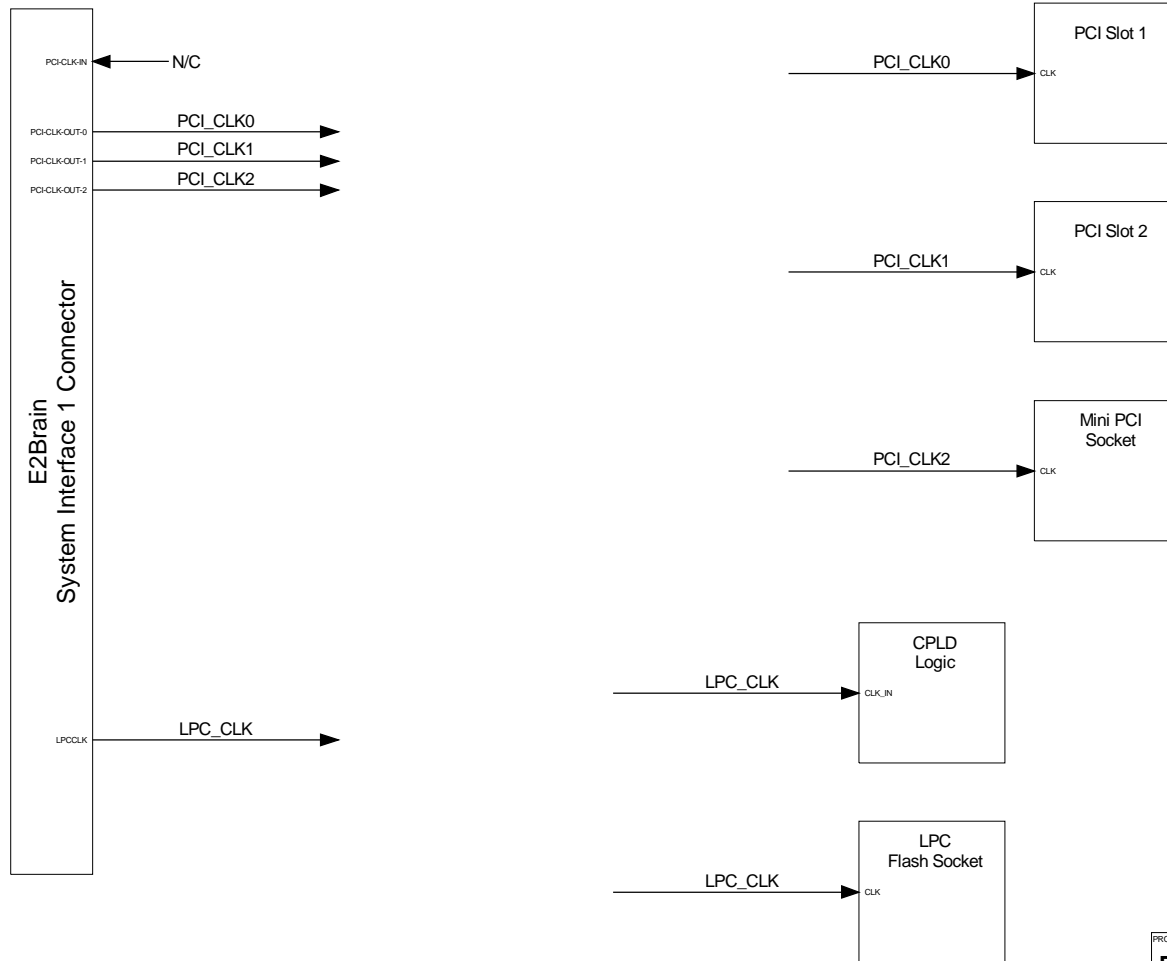
PROJECT EBC3			
ELEMENT Top_EBC3	ELEMENT PAGE 01 of 08	DIVISION KOM	NAME Naegele
		DATE 04.2006	
FUNCTION		VERIFIED KOM	@VER_ENGINEER @VER_DATE
		APPROVED KOM	@APPR_ENGINEER @APPR_DATE
PCB ID 31.259-1010.1	PCB INDEX 01	SHEET 1 of 37	REV 00


EBC3 Block Diagramm



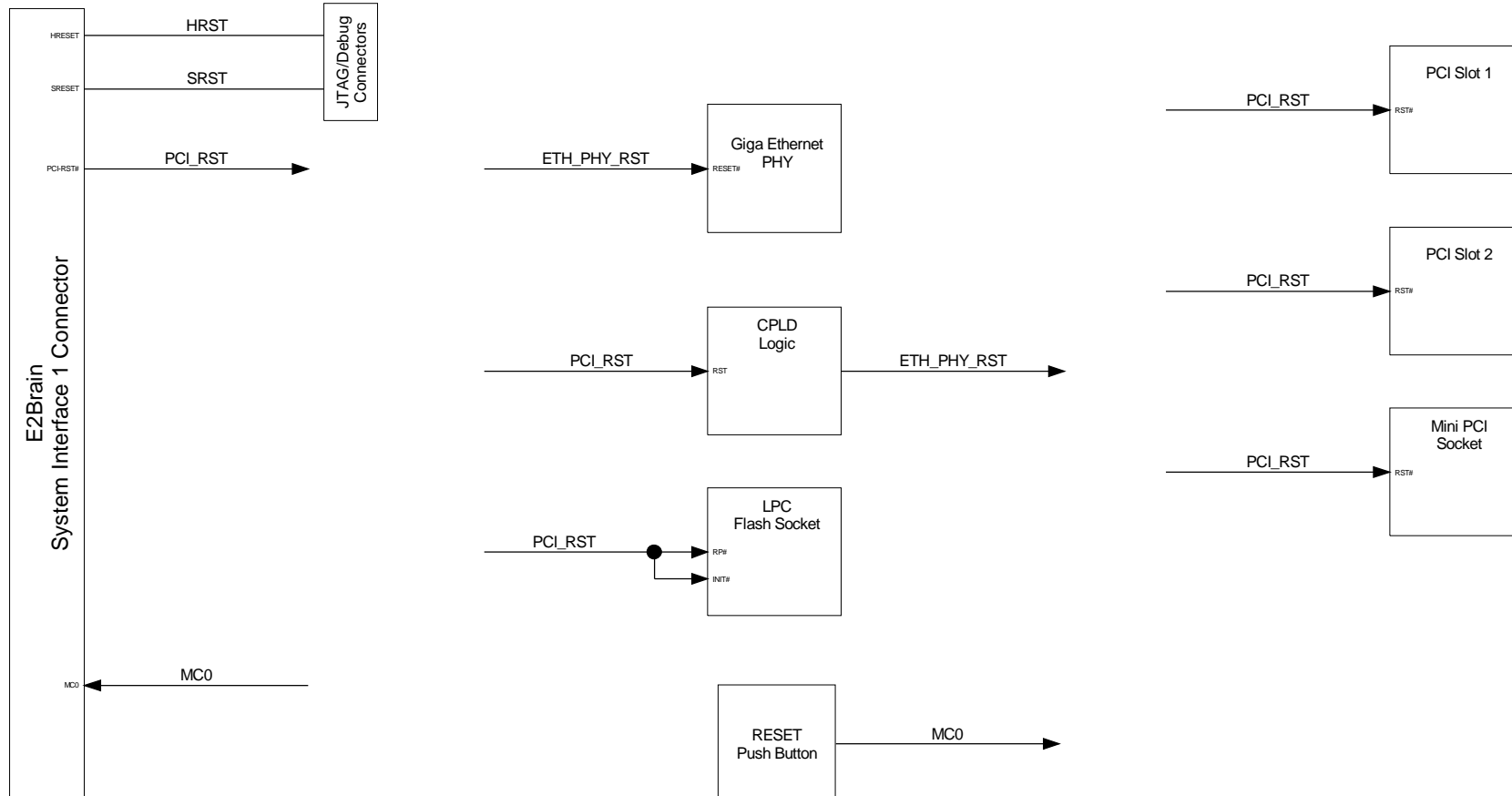
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PCB ID 31.259-1010.1		PCB INDEX 01	SHEET 2 of 37
		APPROVED KOM @APPR_ENGINEER	@APPR_DATE
		REV 00	

CLOCK DISTRIBUTION



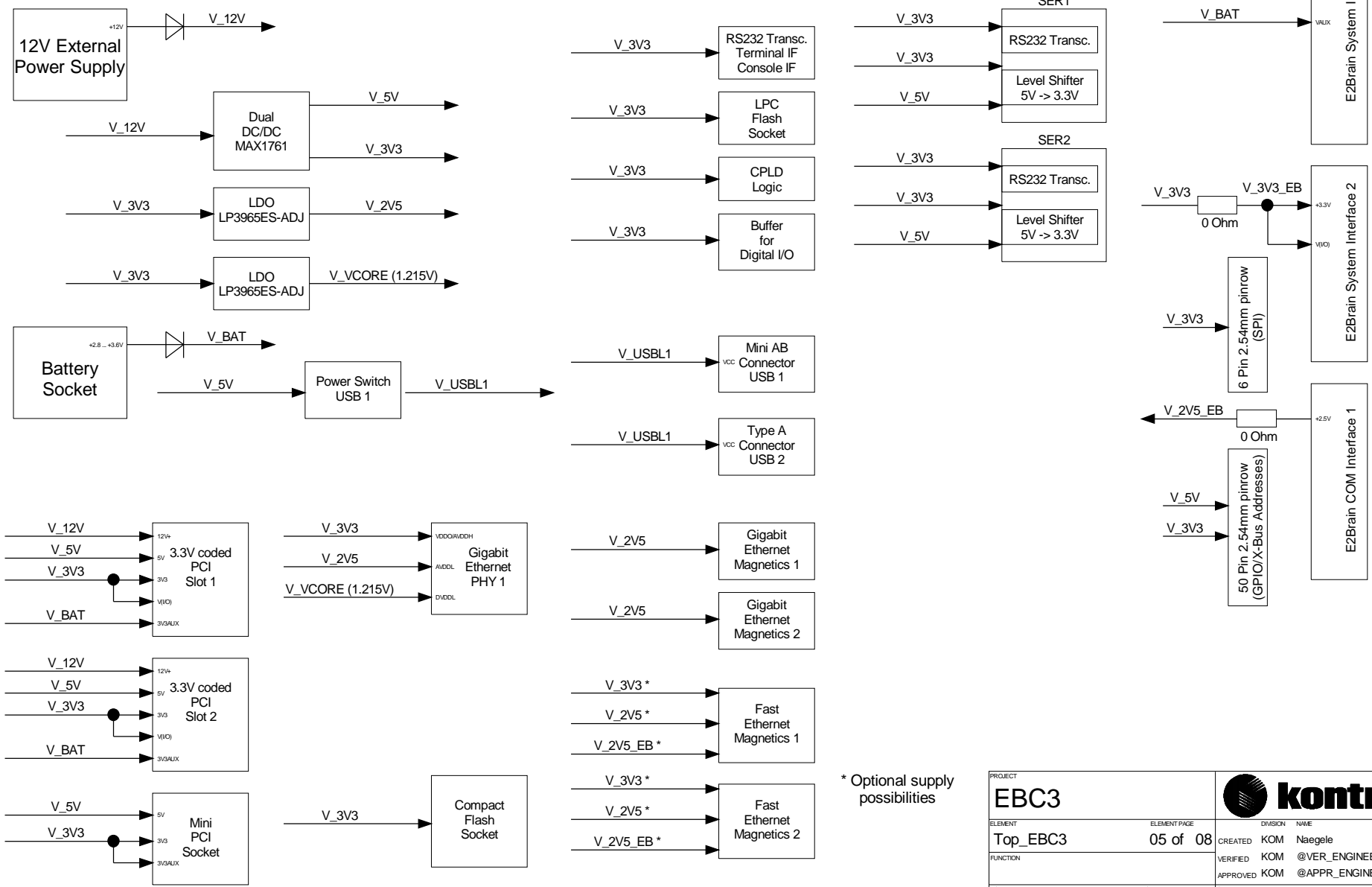
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		APPROVED KOM @APPR_ENGINEER	@APPR_DATE
PCB ID 31.259-1010.1	PCB INDEX 01	SHEET 3 of 37	REV 00

RESET STRUCTURE



PROJECT EBC3			
ELEMENT Top_EBC3	ELEMENT PAGE 04 of 08	DIVISION NAME KOM Naegele	DATE 04.2006
FUNCTION		VERIFIED KOM @VER_ENGINEER	@VER_DATE
		APPROVED KOM @APPR_ENGINEER	@APPR_DATE
PCB ID 31.259-1010.1	PCB INDEX 01	SHEET 4 of 37	REV 00

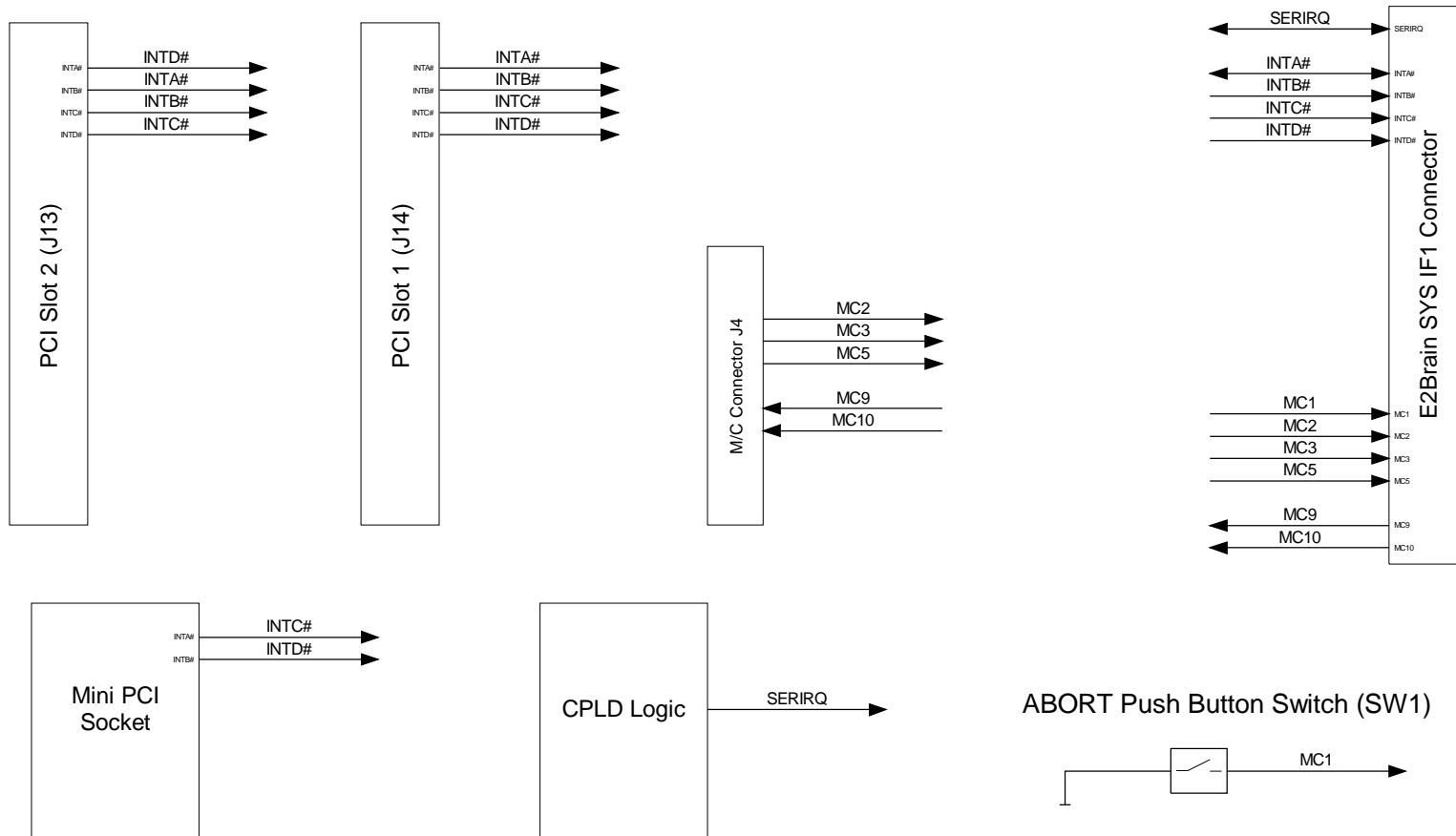
POWER SUPPLY STRUCTURE



* Optional supply possibilities

PROJECT EBC3			
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FUNCTION		DATE 04.2006	
PCB INDEX 31.259-1010.1		VERIFIED KOM	@VER_ENGINEER @VER_DATE
SHEET 01		APPROVED KOM	@APPR_ENGINEER @APPR_DATE
		SHEET 5 of 37	REV 00

INTERRUPT - STRUCTURE



PROJECT EBC3			
ELEMENT Top_EBC3	ELEMENT PAGE 06 of 08	DIVISION KOM	NAME Naegele
FUNCTION		DATE 04.2006	
PCB ID 31.259-1010.1		PCB INDEX 01	DATE @VER_DATE
SHEET 6 of 37		DATE @APPR_DATE	REV 00


Resource Tables

M/C Signal Routing

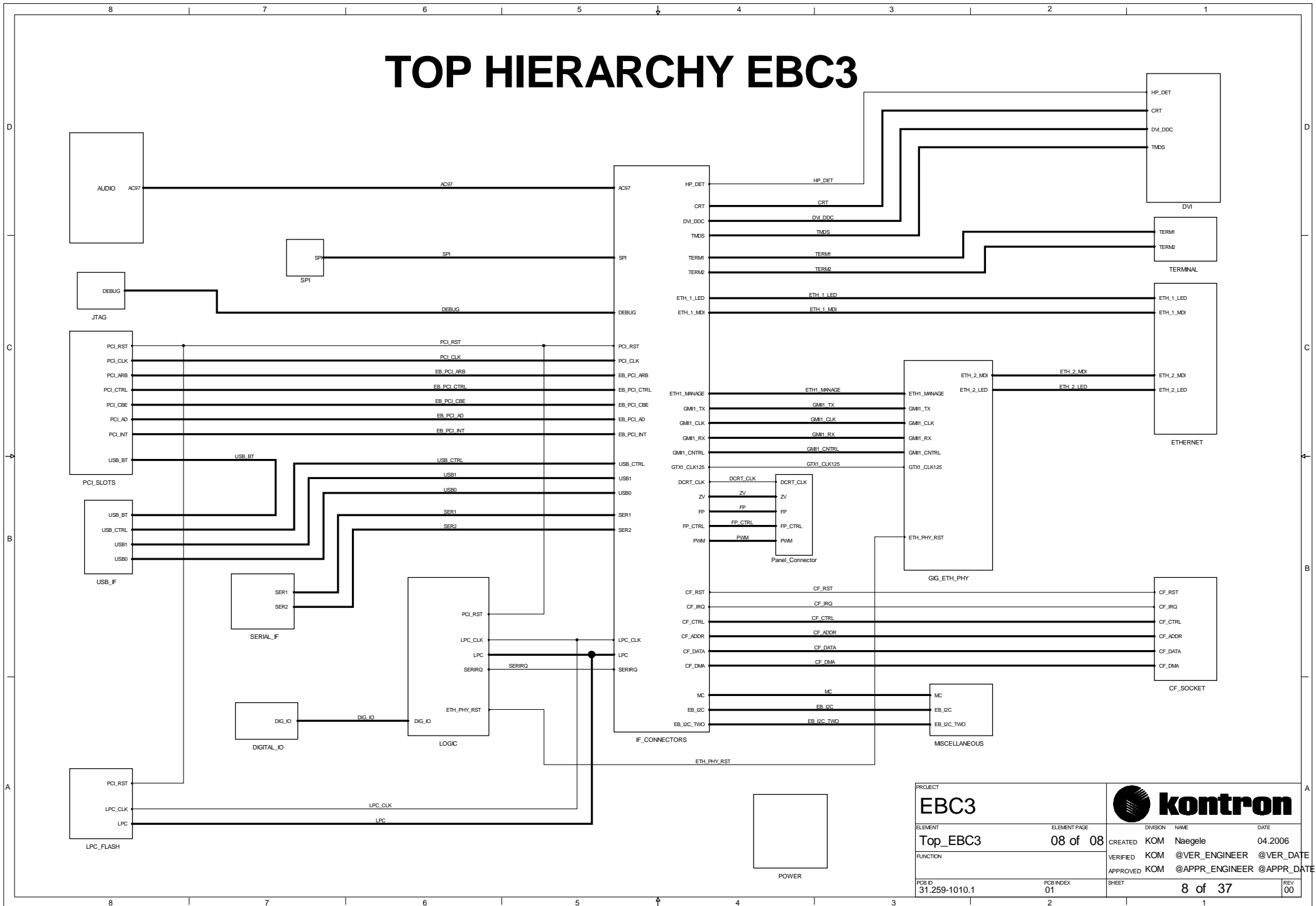
Signal	Function	E2Brain module	EBC3
MC0	RESET	Input for Reset	Output on Reset Push Button Switch
MC1	ABORT	Input for Abort	Output on Abort Push Button Switch
MC2	DEG	Input, maskable interrupt capable	Input available on J4 Pinrow
MC3	FAL	Input, maskable interrupt capable	Input available on J4 Pinrow
MC4	BOOT	Input for boot indication	Boot Jumper J12 output (open: Boot from E2Brain flash; set: Boot from LPC socket)
MC5	ENUM	Input, maskable interrupt capable	Input available on J4 Pinrow
MC6	LED1	Output: Boot LED/GP LED	Input for green PCB LED
MC7	LED2	Output: Watchdog LED	Input for yellow PCB LED
MC8	AGENT	Input for PCI Master or Agent Mode	Not mounted 00hm resistor for a PCI Master configuration of the E2Brain module
MC9	HEALTHY	Output signal	Output available on J4 Pinrow
MC10	IREADY	Output signal	Output available on J4 Pinrow
MC11	LED3	Output: GP LED	Input for red PCB LED

PCI Configuration

Device	IDSEL	REQ/GNT	Interrupt PCI Device	Interrupt E2Brain module
PCI Slot 1	AD28	0	INTA#	INTA#
			INTB#	INTB#
			INTC#	INTC#
			INTD#	INTD#
PCI Slot 2	AD27	1	INTA#	INTD#
			INTB#	INTA#
			INTC#	INTB#
			INTD#	INTC#
PCI Slot 2	AD26	2	INTA#	INTC#
			INTB#	INTD#

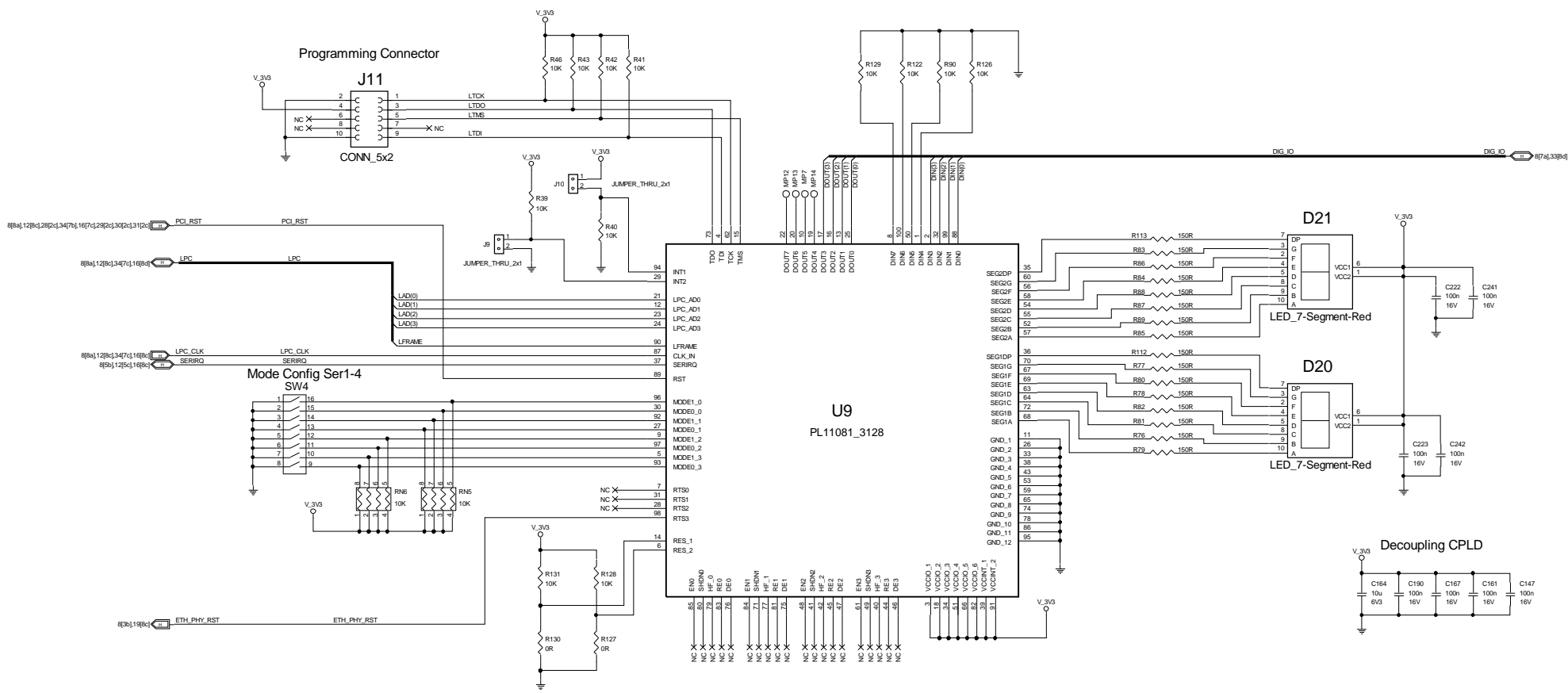
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PCB ID 31.259-1010.1	PCB INDEX 01	SHEET 7 of 37	REV 00


TOP HIERARCHY EBC3



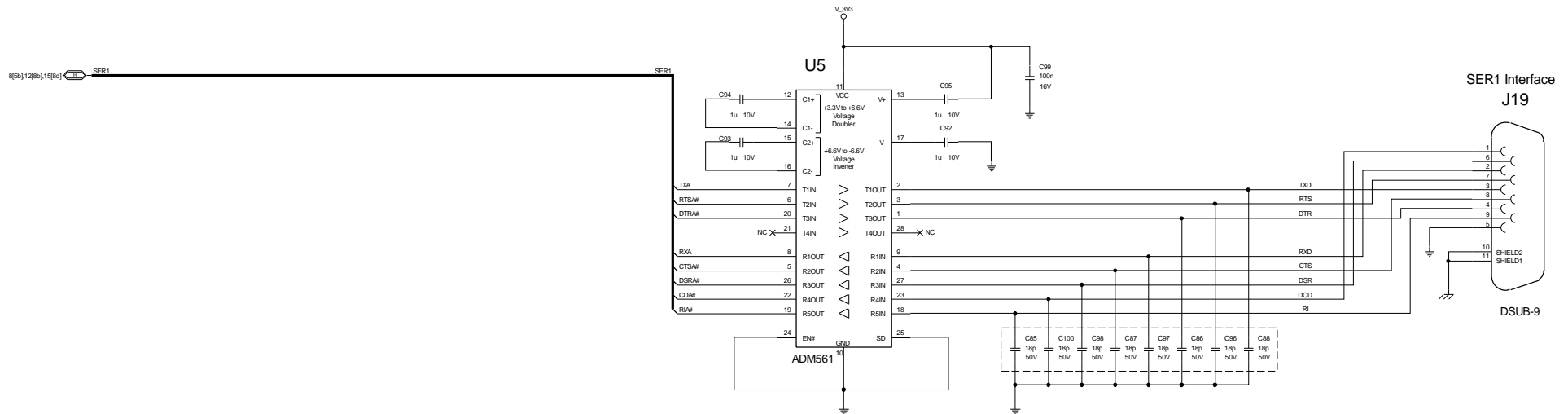
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PCB ID 31.259-1010.1		PCB INDEX 01	DATE @VER_DATE
SHEET 8 of 37		APPROVED @APPR_ENGINEER	DATE @APPR_DATE
		REV 00	


Onboard CPLD Logic



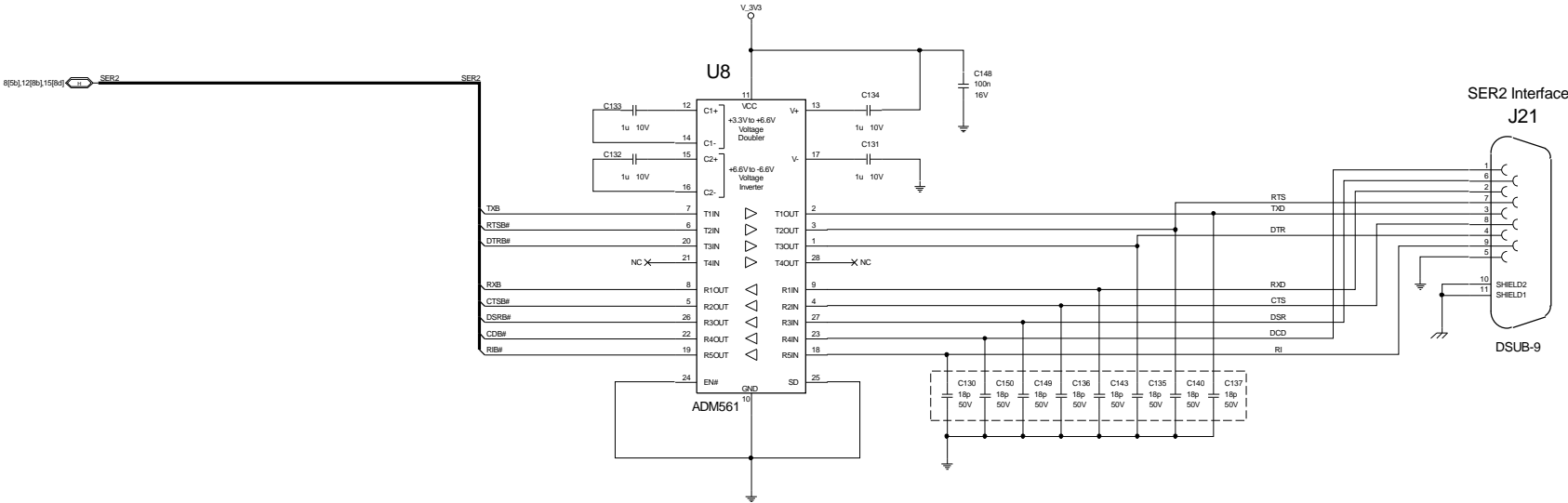
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ELEMENT LOGIC	ELEMENT PAGE 01 of 01	DIVISION KOM	NAME Naegele
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PCB ID 31.259-1010.1		PCB INDEX 01	APPROVED @APPR_ENGINEER
SHEET 9 of 37		REV 00	

RS232 Serial Interface SER1



PROJECT EBC3			
ELEMENT SERIAL_IF	ELEMENT PAGE 01 of 02	DIVISION KOM	NAME Naegele
FUNCTION		DATE 04.2006	VERIFIED KOM @VER_ENGINEER @VER_DATE
PCB ID 31.259-1010.1		PCB INDEX 01	APPROVED KOM @APPR_ENGINEER @APPR_DATE
SHEET 10 of 37		REV 00	

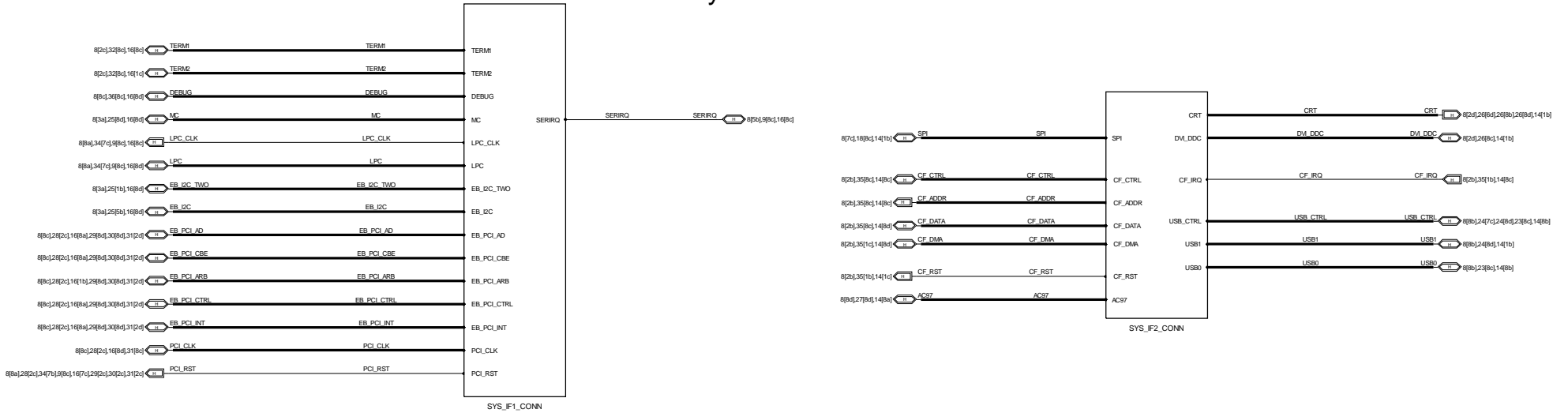
RS232 Serial Interface SER2



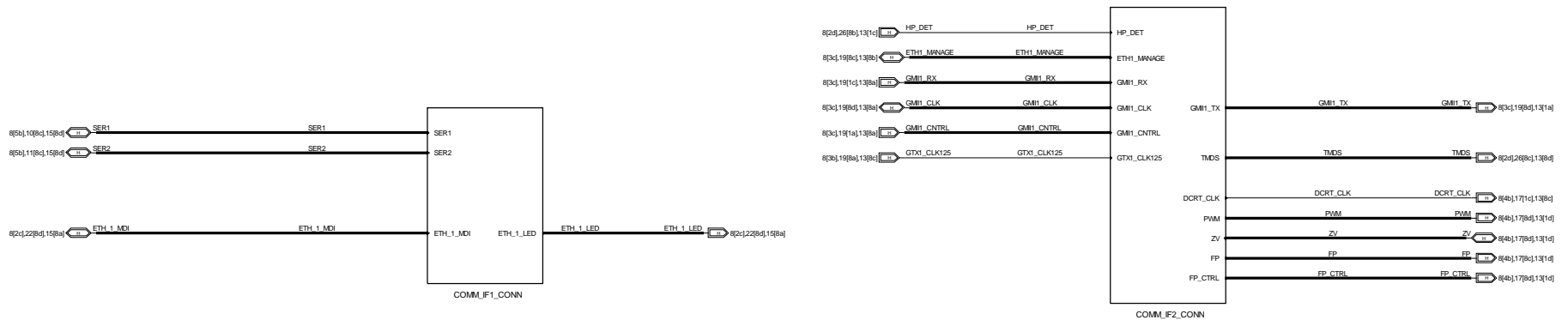
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ELEMENT SERIAL_IF	ELEMENT PAGE 02 of 02	DIVISION KOM	NAME Naegele
FUNCTION		DATE 04.2006	VERIFIED @VER_ENGINEER
PCB ID 31.259-1010.1		PCB INDEX 01	APPROVED @APPR_ENGINEER
SHEET 11 of 37		REV 00	

E2BRAIN INTERFACE CONNECTORS

System Interface

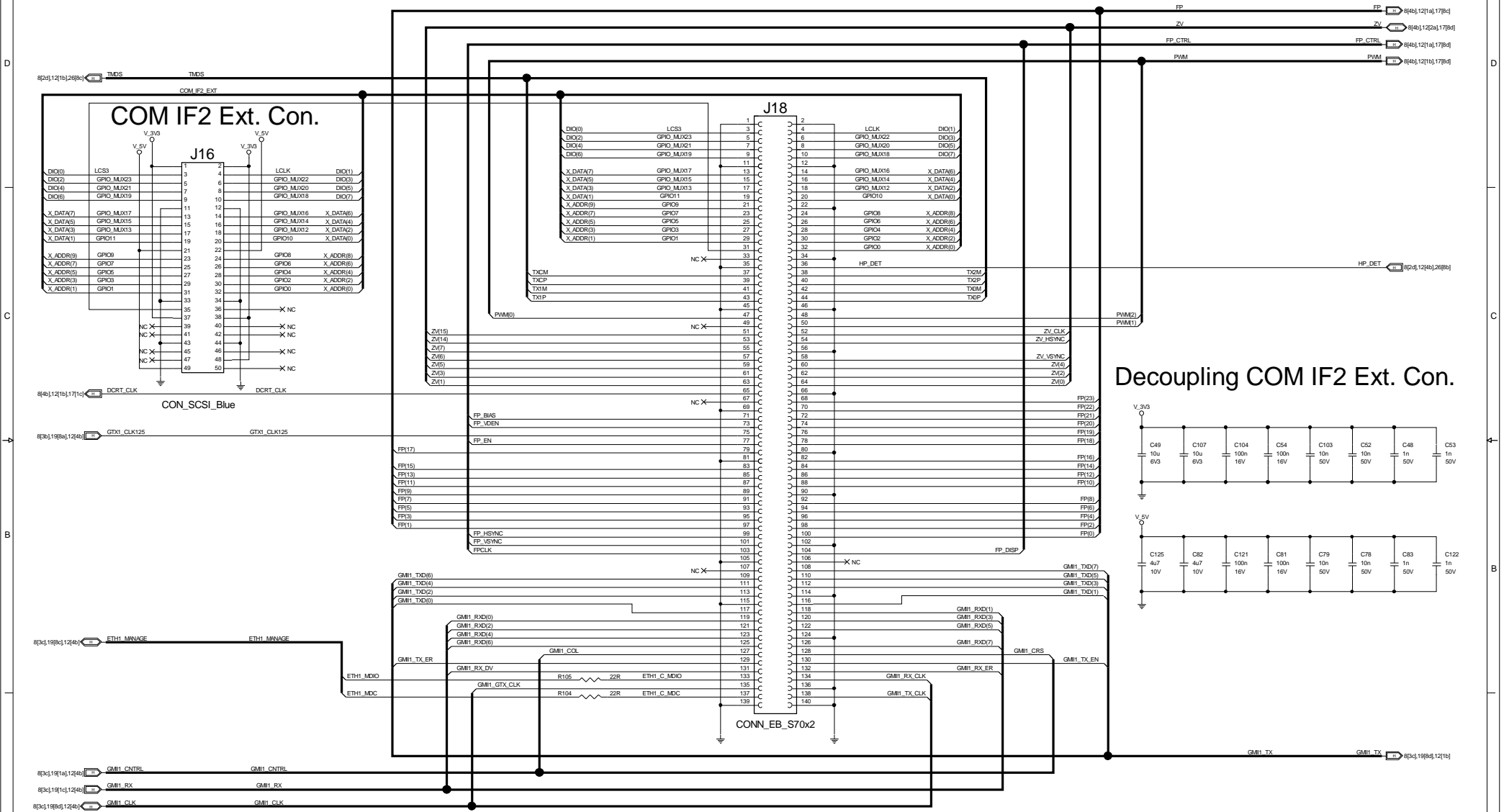


Communication Interface

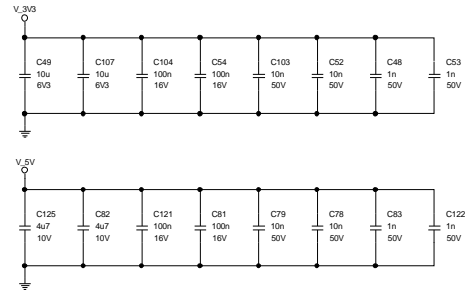



PROJECT EBC3			
ELEMENT IF_CONNECTORS	ELEMENT PAGE 01 of 01	DIVISION KOM	NAME Naegele
FUNCTION		DATE 04.2006	VERIFIED KOM @VER_ENGINEER @VER_DATE
PCB ID 31.259-1010.1		PCB INDEX 01	APPROVED KOM @APPR_ENGINEER @APPR_DATE
SHEET 12 of 37		REV 00	

Communication Interface 2 Connector

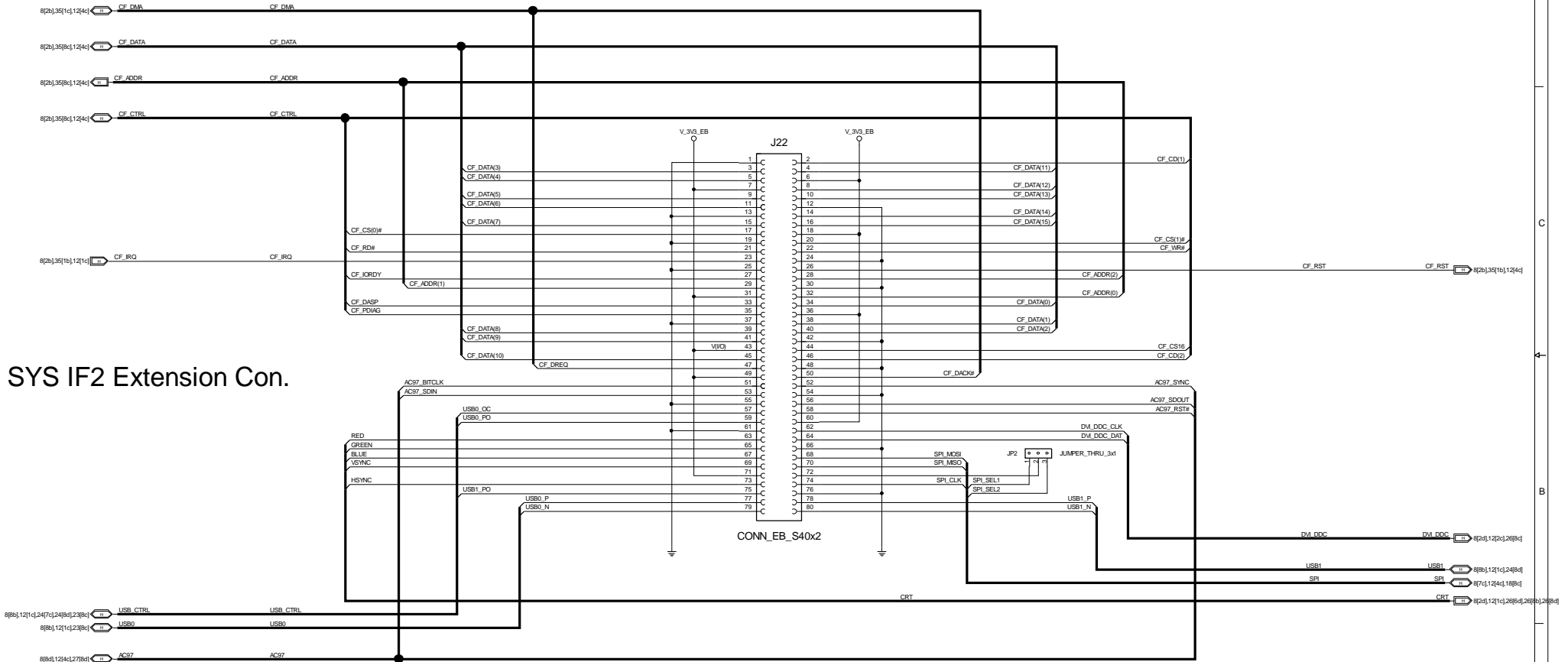


Decoupling COM IF2 Ext. Con.



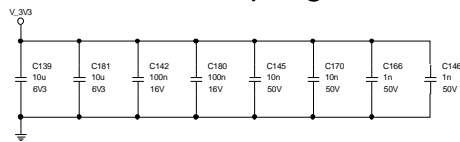
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FUNCTION		DATE 04.2006	VERIFIED KOM @VER_ENGINEER @VER_DATE
PCB ID 31.259-1010.1		PCB INDEX 01	APPROVED KOM @APPR_ENGINEER @APPR_DATE
SHEET 13 of 37		REV 00	

System Interface 2 Connector

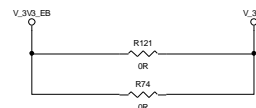


SYS IF2 Extension Con.

Decoupling



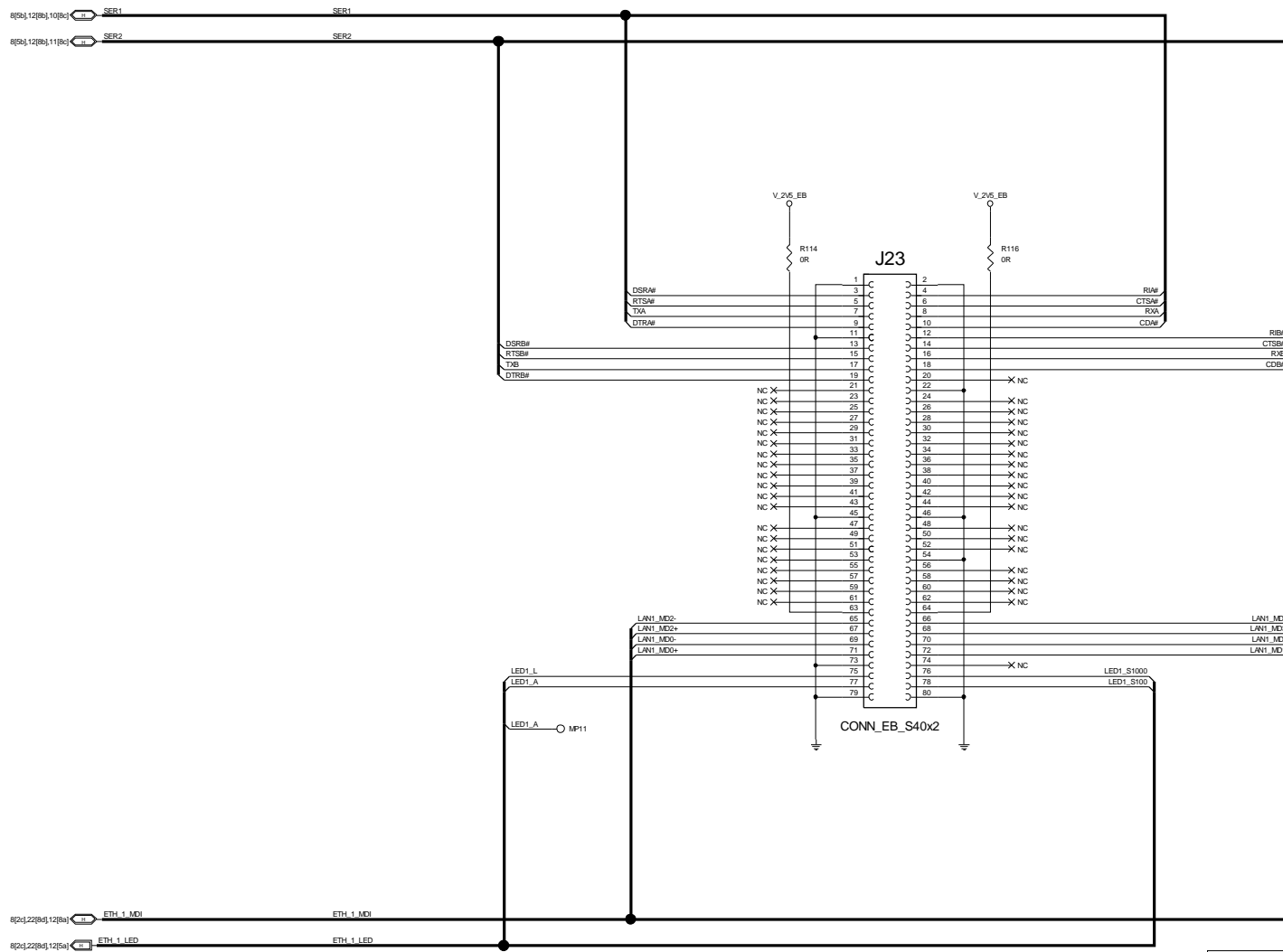
E2Brain Power Supply



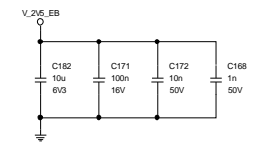
Separated (Open) for current measurement possibility


PROJECT EBC3			
ELEMENT SYS_IF2_CONN	ELEMENT PAGE 01 of 01	DIVISION KOM	NAME Naegele
FUNCTION		DATE 04.2006	VERIFIED KOM @VER_ENGINEER @VER_DATE
PCB ID 31.259-1010.1		PCB INDEX 01	APPROVED KOM @APPR_ENGINEER @APPR_DATE
SHEET 14 of 37		REV 00	

Communication Interface 1 Connector

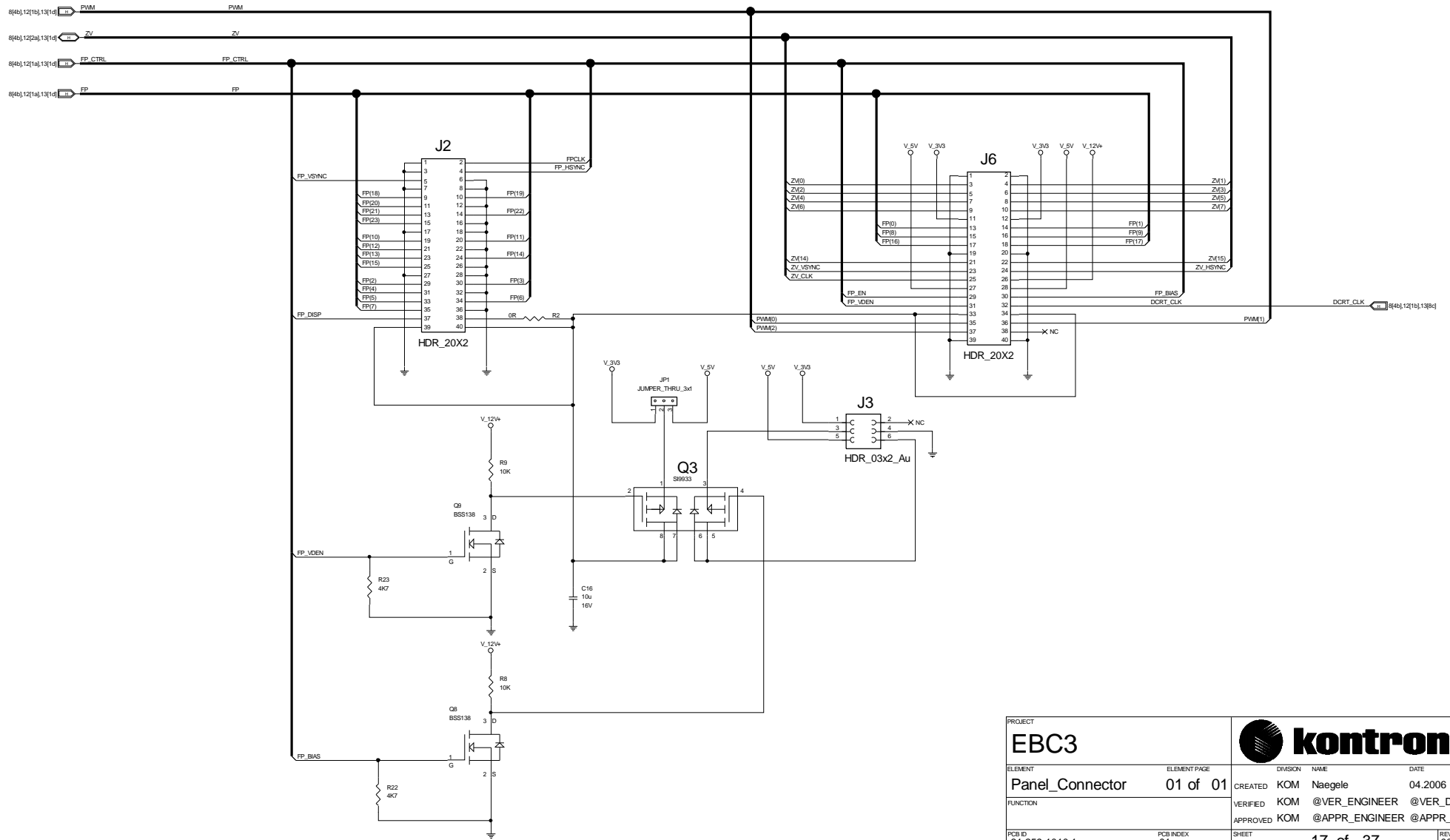


Decoupling 2.5V



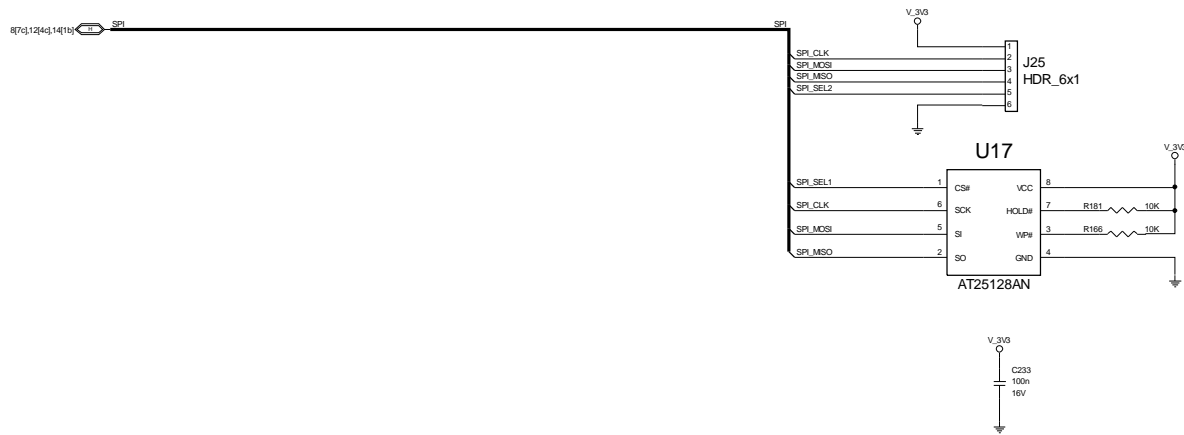
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SHEET 15 of 37		DATE @APPR_DATE	REV 00


Panel Connectors



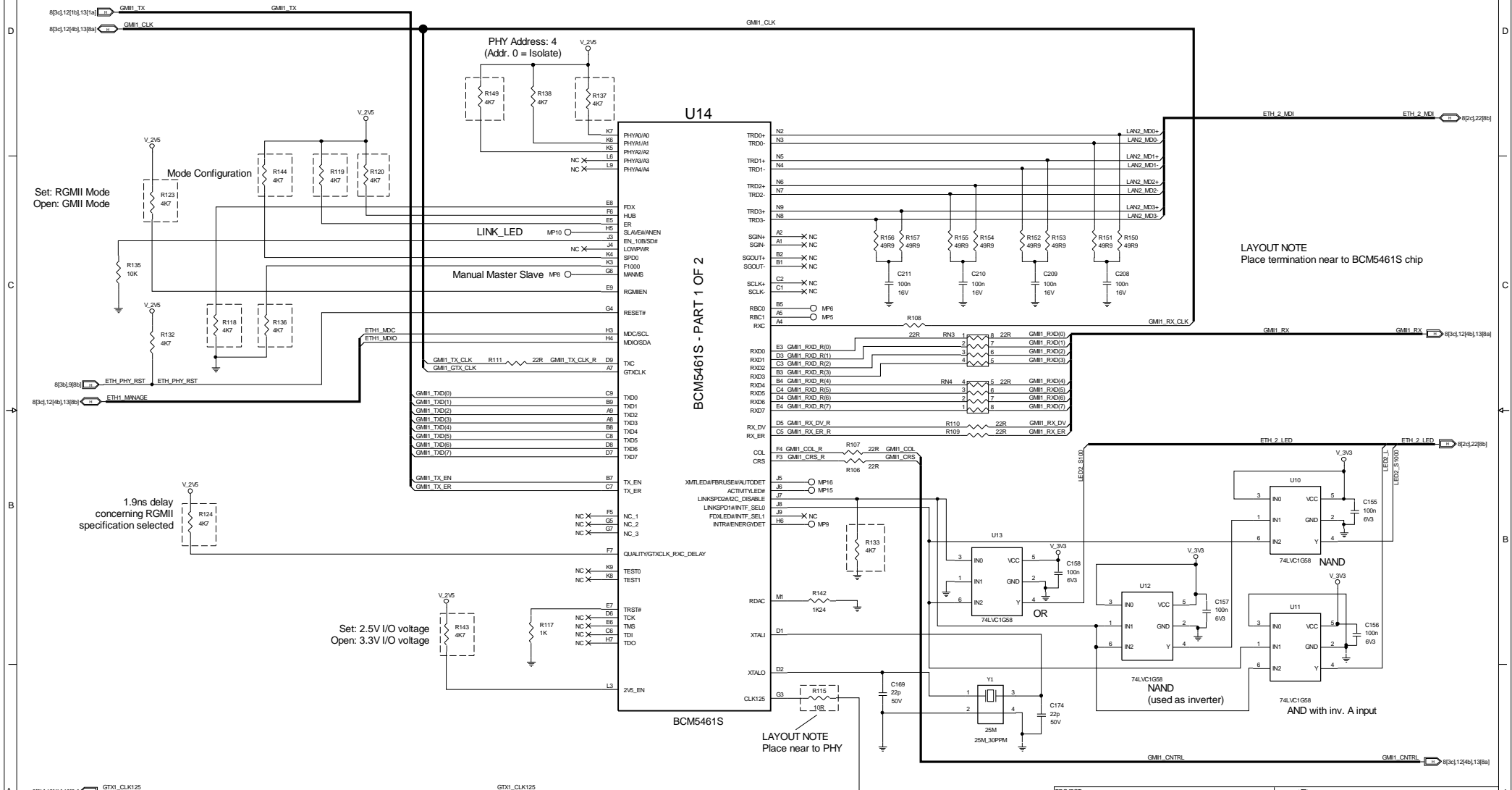
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PCB ID 31.259-1010.1		PCB INDEX 01	APPROVED KOM @APPR_ENGINEER @APPR_DATE
SHEET 17 of 37		REV 00	

SPI Components



PROJECT EBC3			
ELEMENT SPI	ELEMENT PAGE 01 of 01	DIVISION NAME KOM Naegele	DATE 04.2006
FUNCTION		VERIFIED KOM @VER_ENGINEER	@VER_DATE
PCB ID 31.259-1010.1		PCB INDEX 01	SHEET 18 of 37
		REV 00	

GIGABIT ETHERNET PHY1

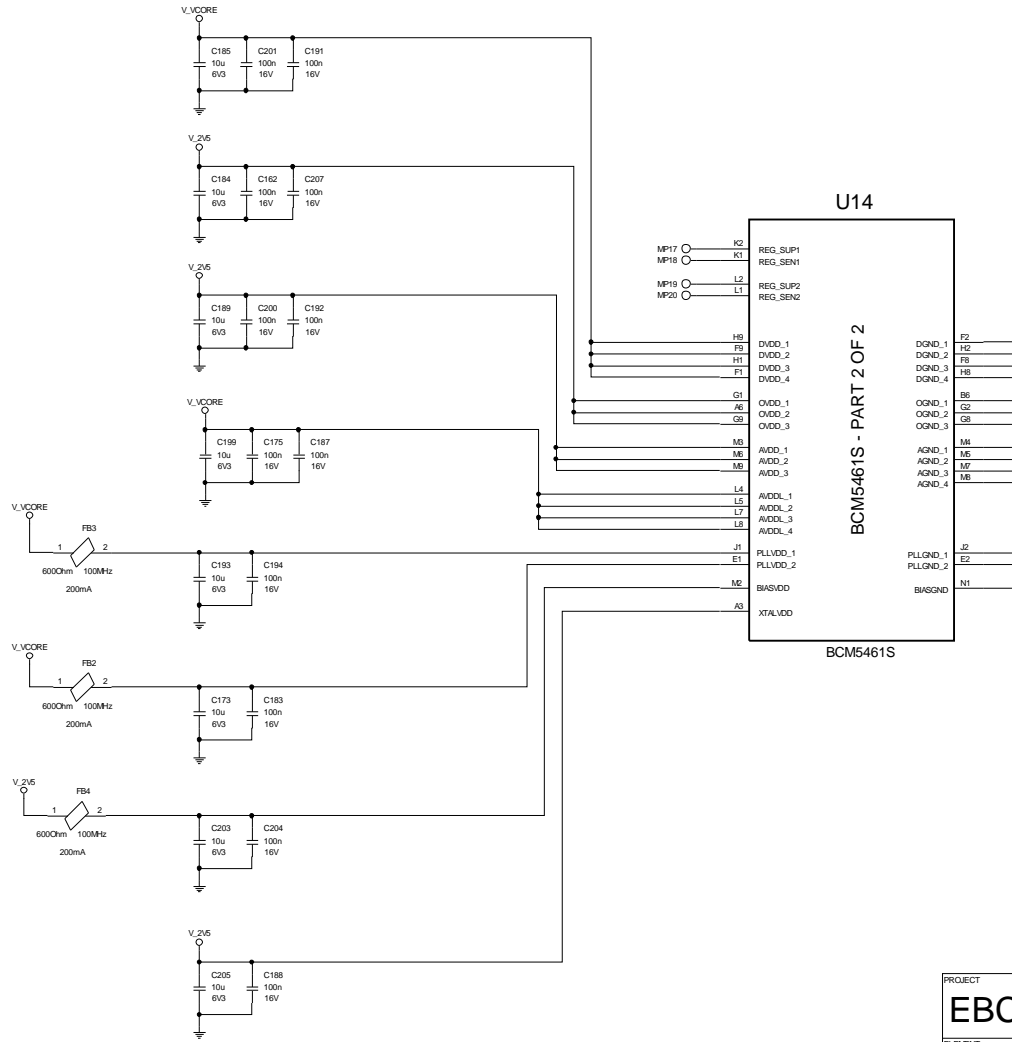


LAYOUT NOTE
Place termination near to BCM5461S chip

LAYOUT NOTE
Place crystal circuit near to BCM5461S chip.
The traces should be as short as possible
and approximately the same length.

PROJECT EBC3			
ELEMENT GIG_ETH_PHY	ELEMENT PAGE 01 of 03	DIVISION KOM	NAME Naegele
FUNCTION		DATE 04.2006	@VER_ENGINEER @VER_DATE
PCB ID 31.259-1010.1		PCB INDEX 01	SHEET 19 of 37
		REV 00	@APPR_ENGINEER @APPR_DATE

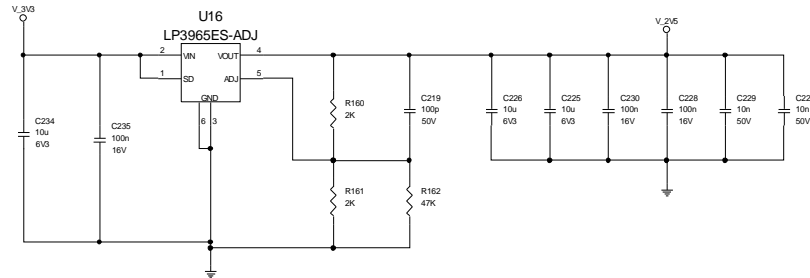
Gigabit PHY Power Supply



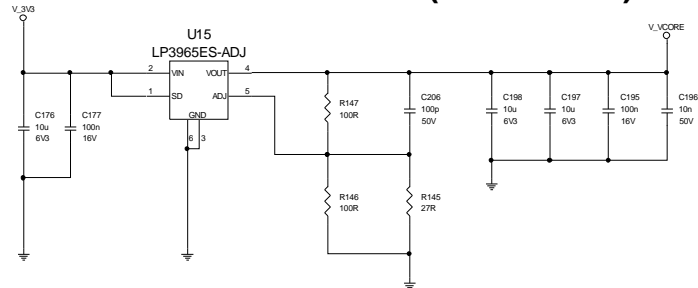
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SHEET 20 of 37		DATE @APPR_DATE	
REV 00		REV 00	

GIGABIT ETHERNET PHY1

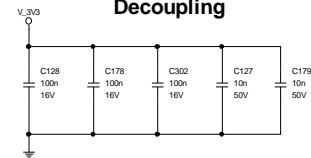
2.5V Generation



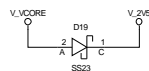
VCORE Generation (here 1.215V)



Decoupling



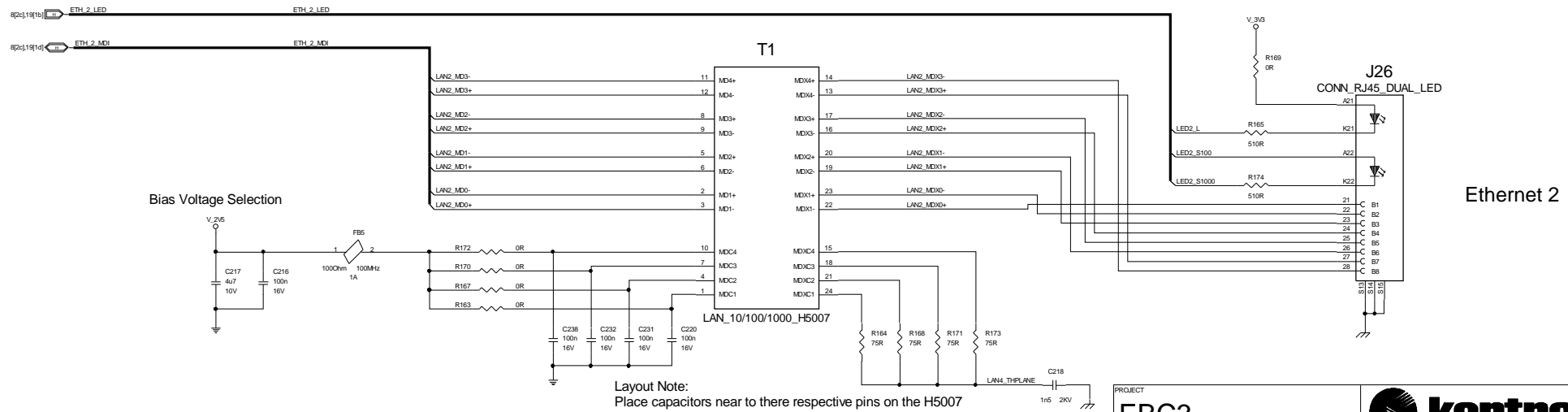
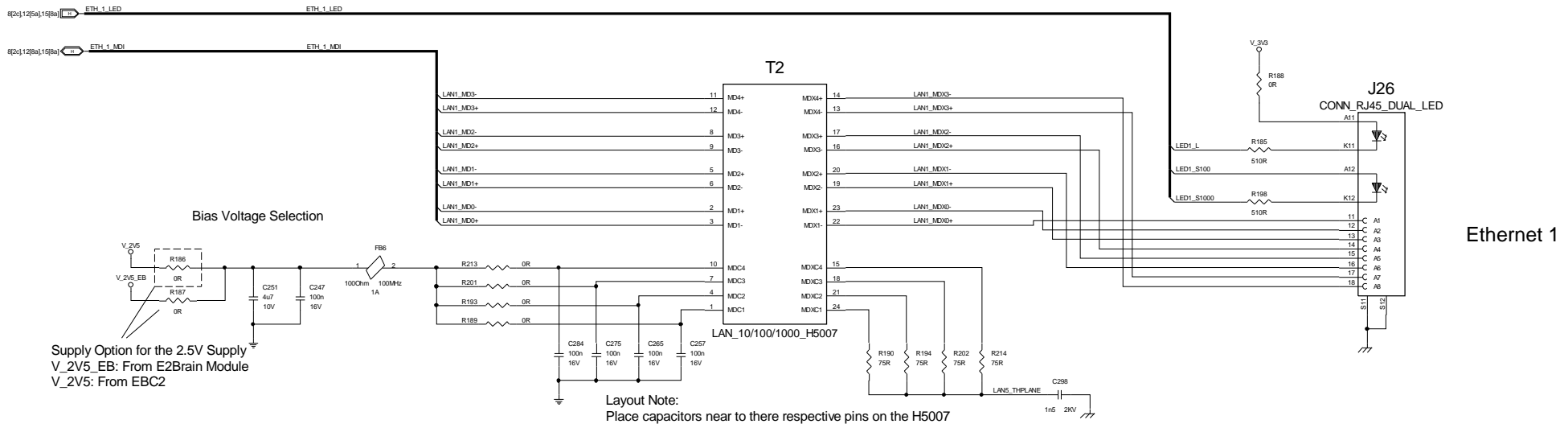
Voltage Tracking



1.5V must never be more than 0.5V greater than 2.5V

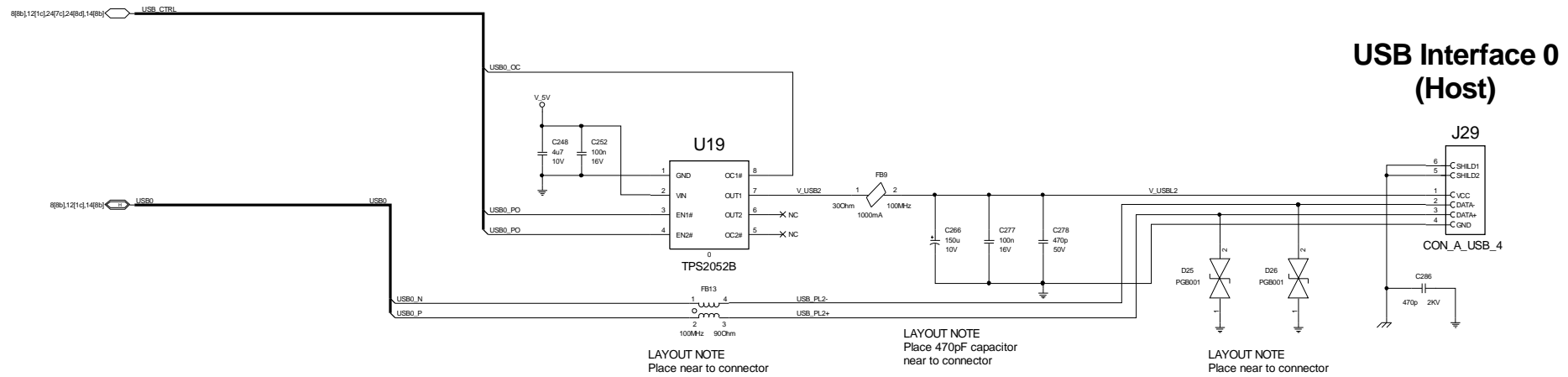
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VERIFIED KOM		@VER_ENGINEER @VER_DATE	
APPROVED KOM		@APPR_ENGINEER @APPR_DATE	
SHEET 21 of 37			

GIGABIT MAGNETICS, RJ45 CONNECTORS



PROJECT EBC3			
ELEMENT ETHERNET	ELEMENT PAGE 01 of 01	DIVISION KOM	NAME Naegele
FUNCTION		DATE 04.2006	VERIFIED @VER_ENGINEER
PCB ID 31.259-1010.1		PCB INDEX 01	APPROVED @APPR_ENGINEER
SHEET 22 of 37		DATE @APPR_DATE	
REV 00		REV 00	

USB Interface 0 Master



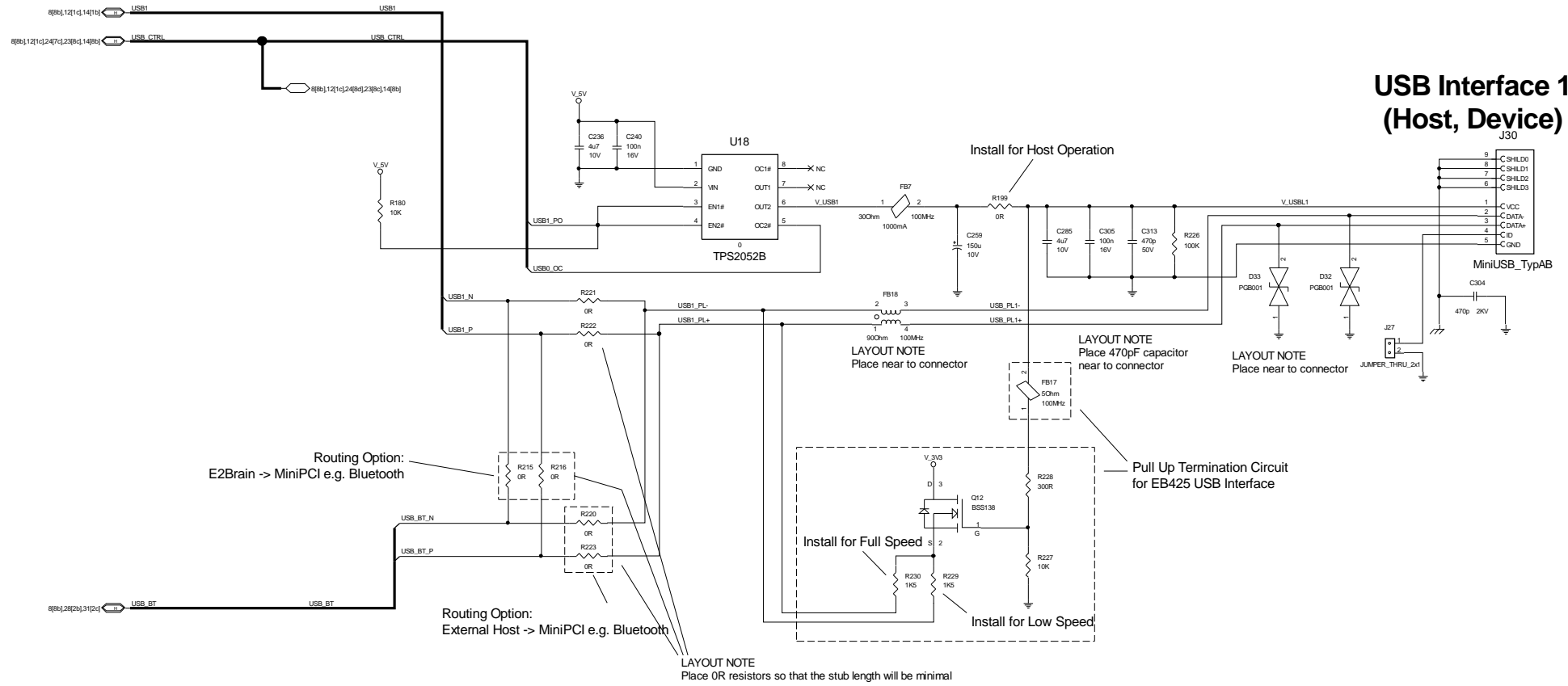
USB Interface 0 (Host)

Note:
Max. 500mA on USB Power Rail

PROJECT EBC3			
ELEMENT USB_IF	ELEMENT PAGE 01 of 02	DIVISION KOM	NAME Naegele
FUNCTION		DATE 04.2006	VERIFIED KOM
PCB ID 31.259-1010.1		PCB INDEX 01	DATE @VER_ENGINEER @VER_DATE
SHEET 23 of 37		DATE @APP_DATE	REV 00

USB Interface 1

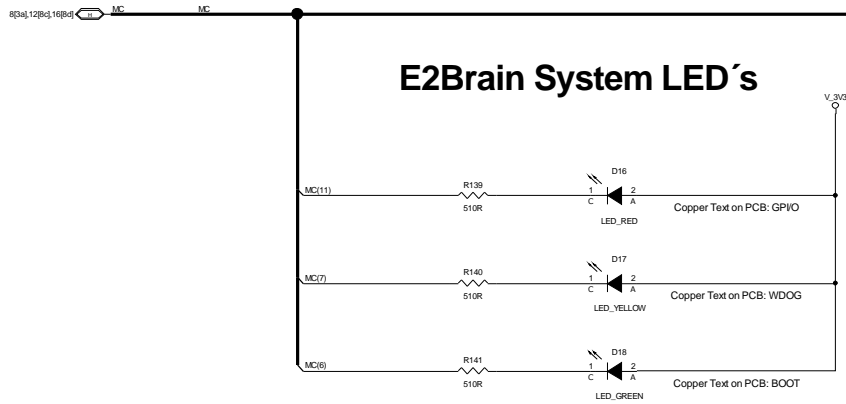
Host/Device



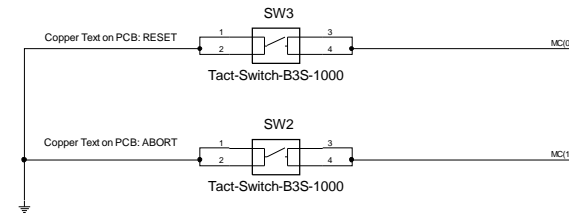
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ELEMENT USB_IF	ELEMENT PAGE 02 of 02	DIVISION KOM	NAME Naegele
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SHEET 24 of 37		REV 00	

Monitor and Control Utilities

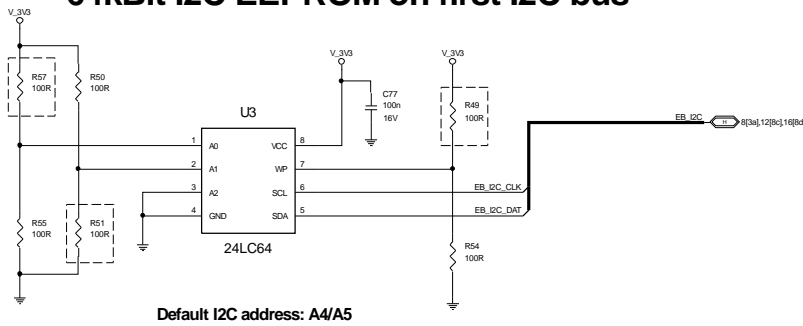
E2Brain System LED's



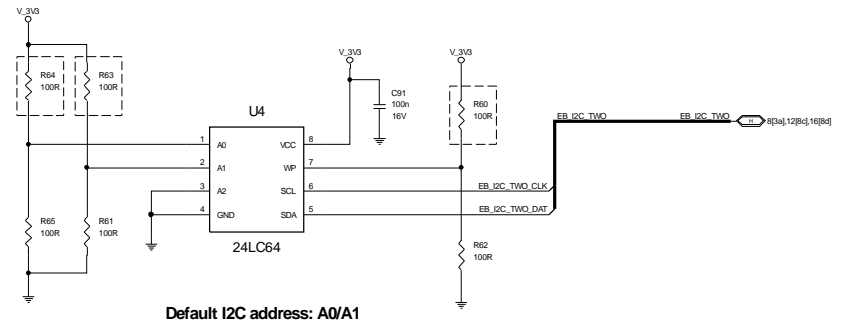
E2Brain System Switches



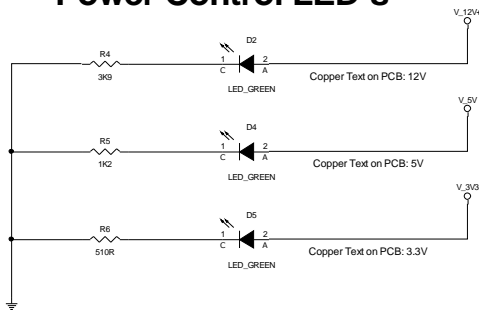
64kBit I2C EEPROM on first I2C bus



64kBit I2C EEPROM on second I2C Bus

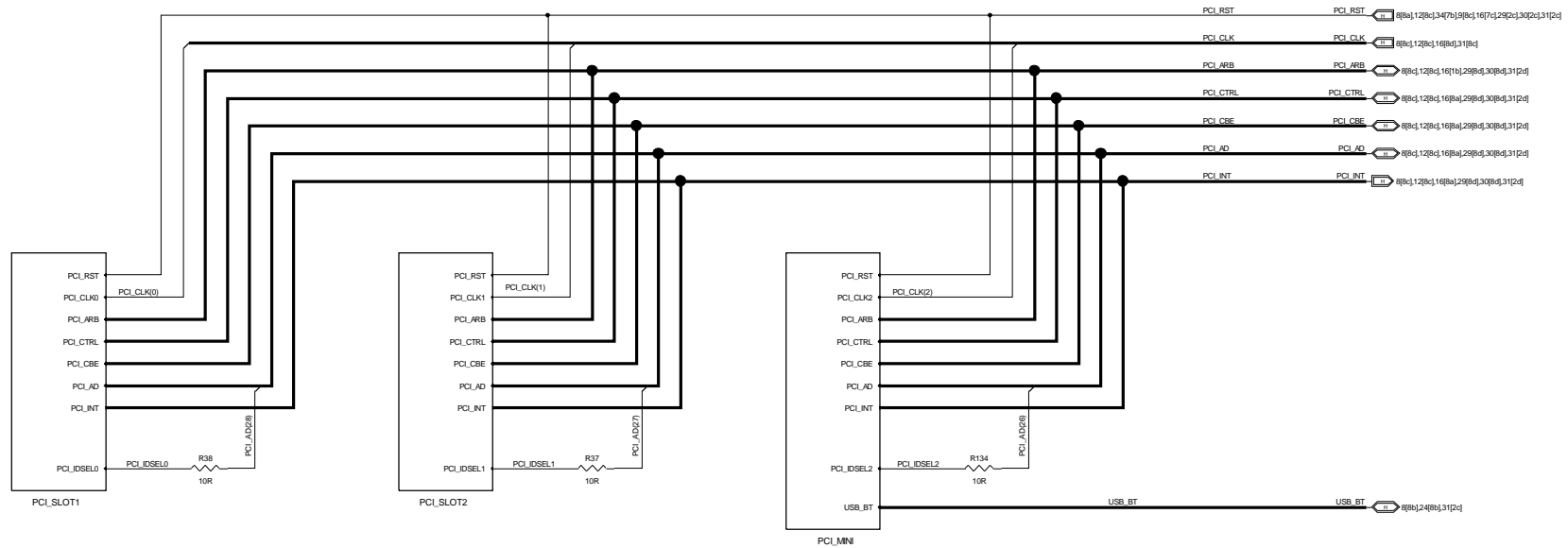


Power Control LED's



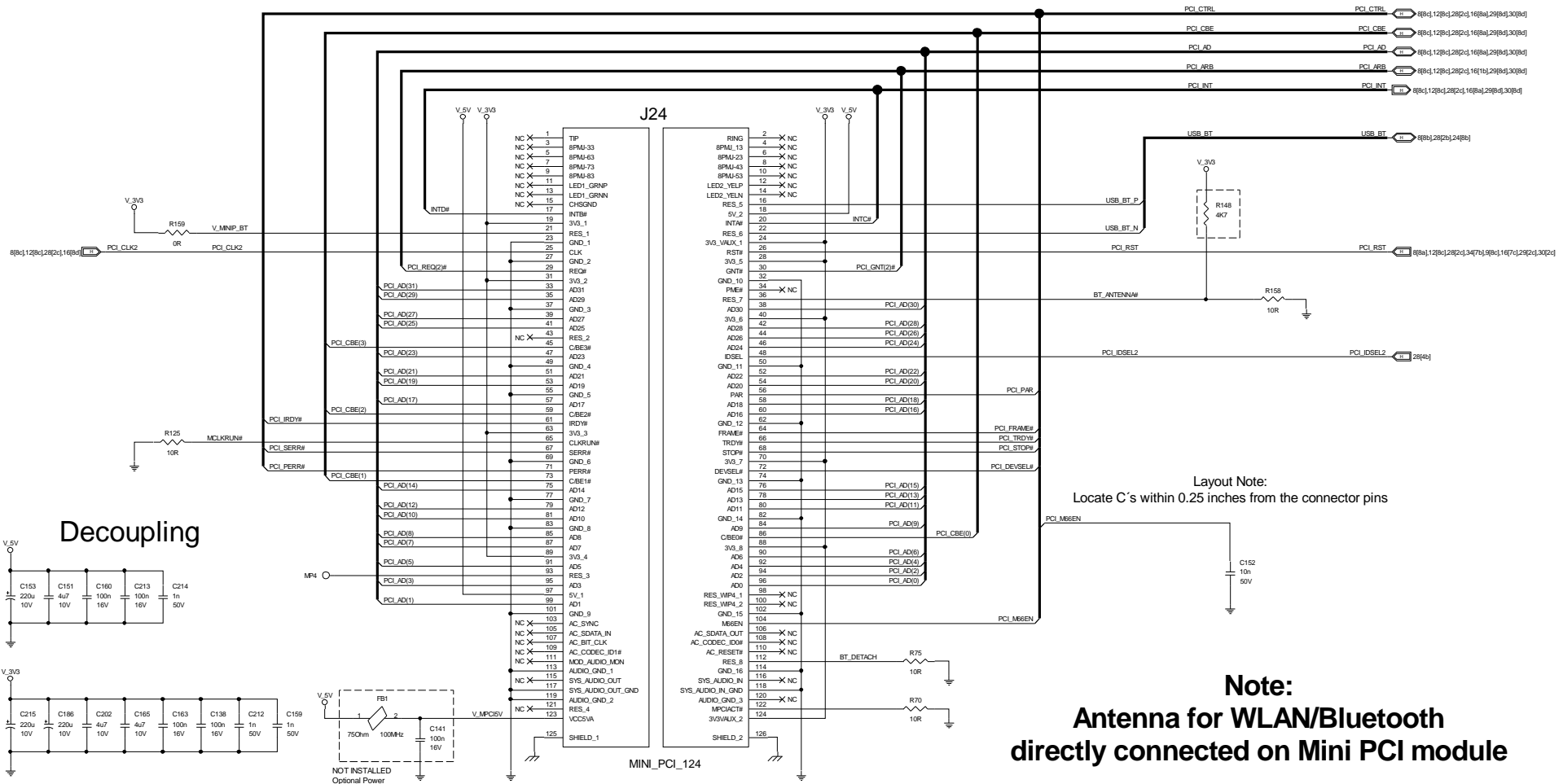
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ELEMENT MISCELLANEOUS	ELEMENT PAGE 01 of 01	DIVISION KOM	NAME Naegele
FUNCTION		DATE 04.2006	VERIFIED @VER_ENGINEER
PCB ID 31.259-1010.1		PCB INDEX 01	DATE @APPR_DATE
SHEET 25 of 37		REV 00	DATE @APPR_DATE

PCI CONNECTORS/SLOTS



PROJECT EBC3			
ELEMENT PCI_SLOTS	ELEMENT PAGE 01 of 01	DIVISION KOM	NAME Naegele
		DATE 04.2006	
FUNCTION		VERIFIED KOM	@VER_ENGINEER @VER_DATE
		APPROVED KOM	@APPR_ENGINEER @APPR_DATE
PCB ID 31.259-1010.1	PCB INDEX 01	SHEET 27 of 37	REV 00

MINI_PCI Extension



Layout Note:
Locate C's within 0.25 inches from the connector pins

Note:
Antenna for WLAN/Bluetooth
directly connected on Mini PCI module

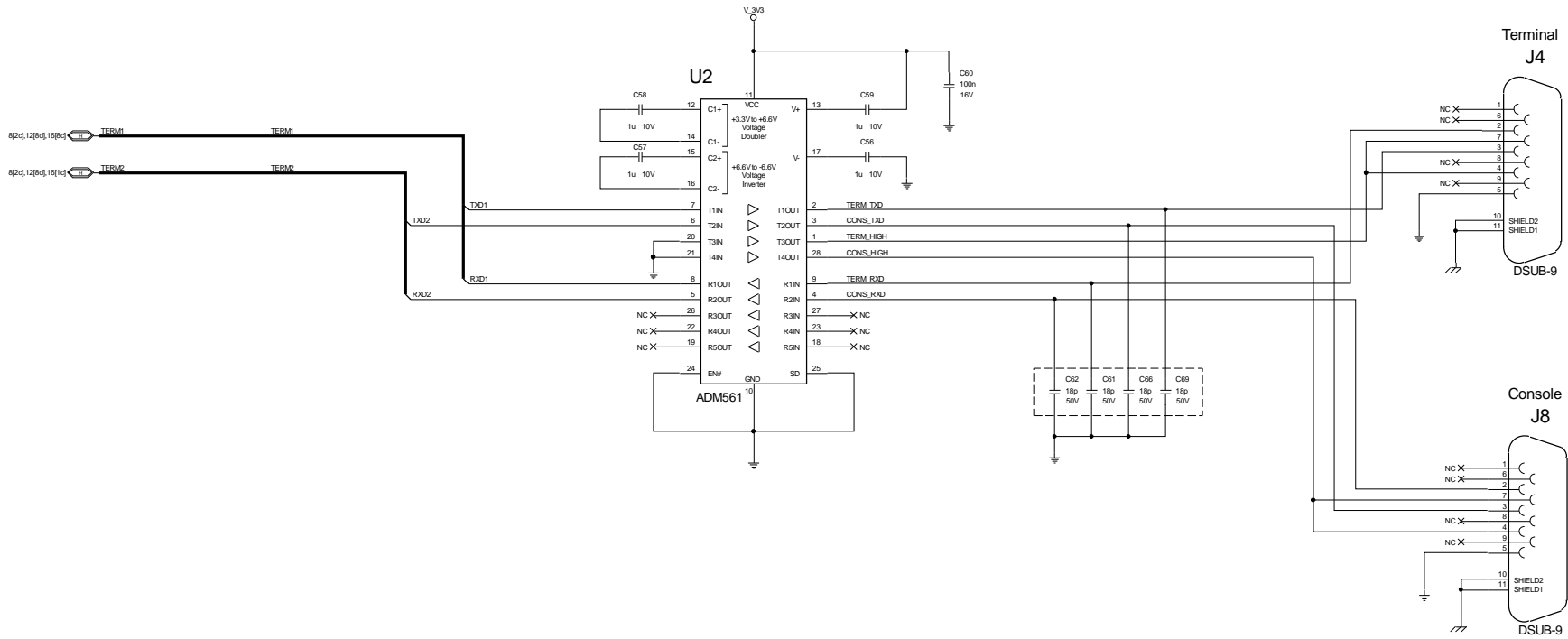
Bluetooth Option

MiniP No.	Name	Attr.	Description
43	Wakeup	Output	BT inform system to request a connection, H: BT wake up the system
36	Vcont1	Input	Antenna selection 1
21	VCC_BT	Input	DC power, DC 3.3V +/- 2%
16	D+	In/Out	USB D+
22	D-	In/Out	USB D-
112	Detach	Input	BT disconnection from system, H: Detach
93	RST	Input	Reset, H: reset.
121	Existence #	Out	BT module existence, L: existence

Note:
Mini-PCI locking metal spins
must be connected to GND

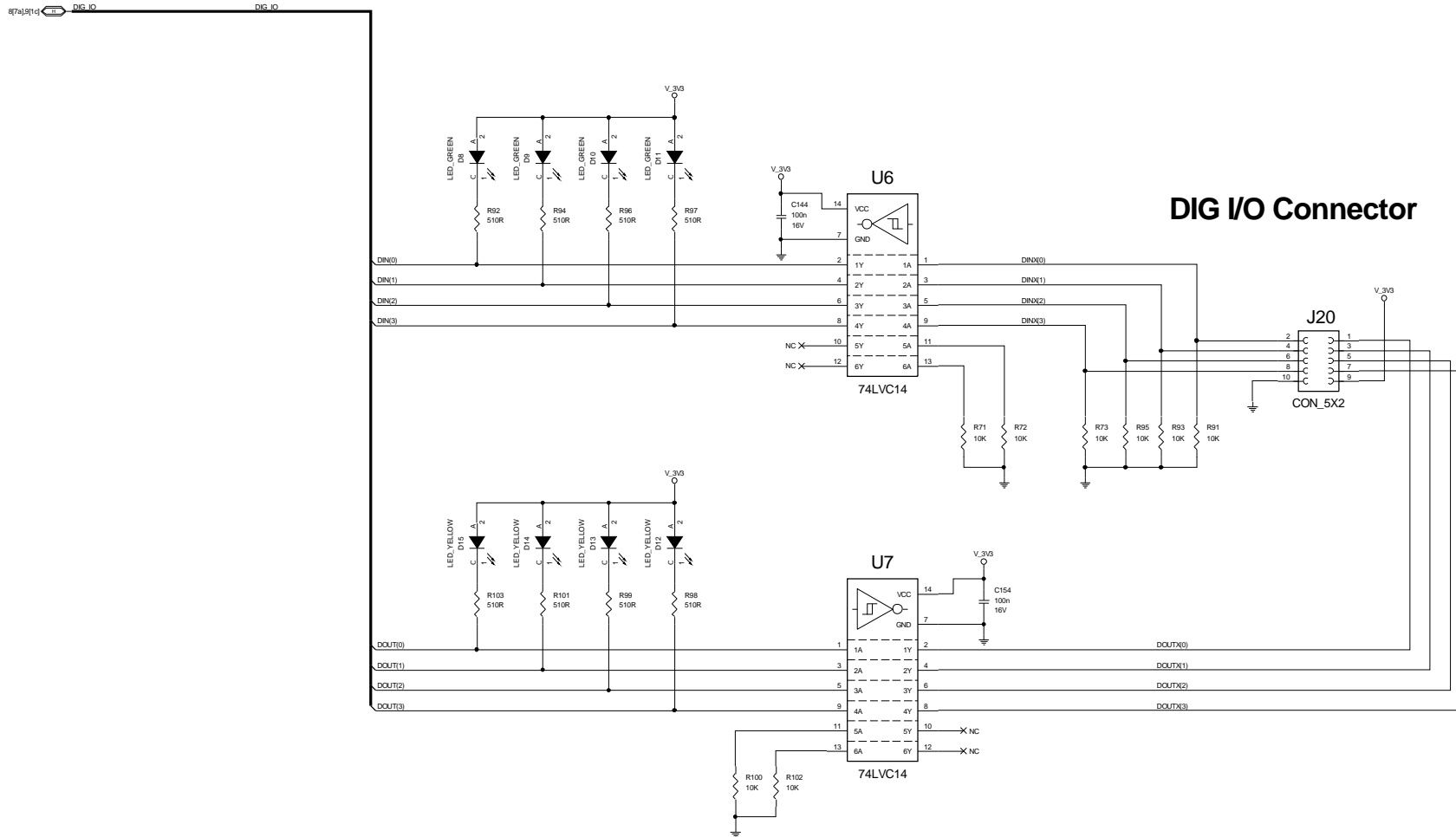
PROJECT EBC3			
ELEMENT PCI_MINI	ELEMENT PAGE 01 of 01	DIVISION KOM	NAME Naegele
FUNCTION MINI-PCI		DATE 04.2006	VERIFIED KOM @VER_ENGINEER @VER_DATE
PCB ID 31.259-1010.1	PCB INDEX 01	APPROVED KOM @APPR_ENGINEER @APPR_DATE	SHEET 30 of 37
		REV 00	

RS232 FRONT PANEL TERMINAL INTERFACES



PROJECT EBC3			
ELEMENT TERMINAL	ELEMENT PAGE 01 of 01	DIVISION KOM	NAME Naegele
FUNCTION		DATE 04.2006	VERIFIED KOM @VER_ENGINEER @VER_DATE
PCB ID 31.259-1010.1		PCB INDEX 01	APPROVED KOM @APPR_ENGINEER @APPR_DATE
SHEET 31 of 37		REV 00	

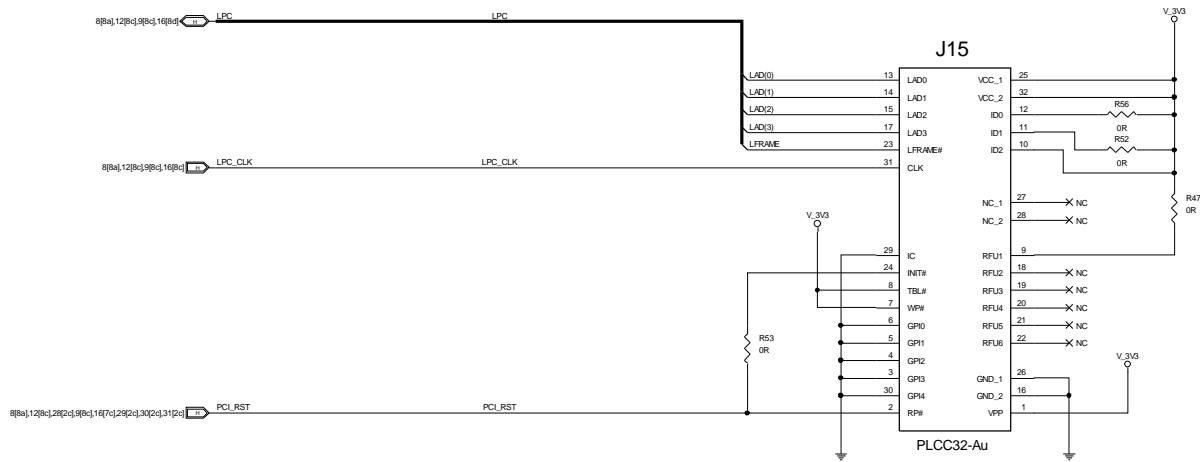
Digital Input/Output



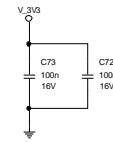
DIG I/O Connector

PROJECT EBC3			
ELEMENT DIGITAL_IO	ELEMENT PAGE 01 of 01	DIVISION KOM	NAME Naegele
FUNCTION		DATE 04.2006	VERIFIED KOM @APPR_ENGINEER @VER_DATE
PCB ID 31.259-1010.1		PCB INDEX 01	APPROVED KOM @APPR_ENGINEER @APPR_DATE
SHEET 32 of 37		REV 00	

LPC FLASH SOCKET

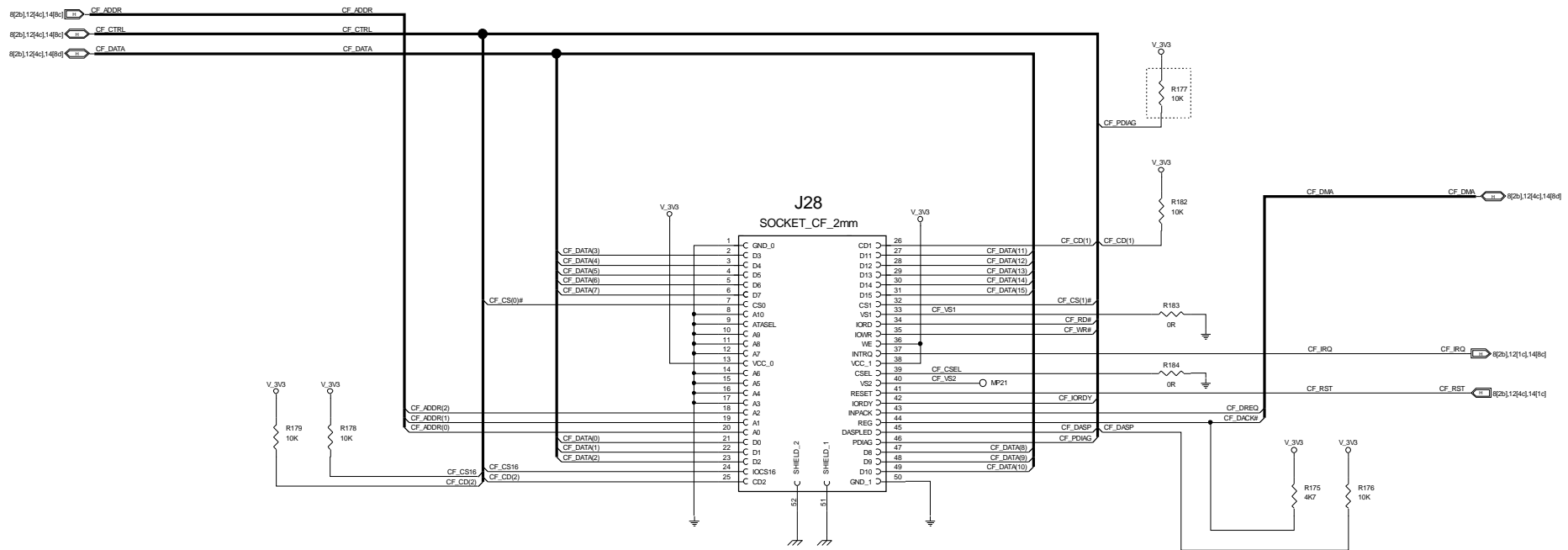


Decoupling



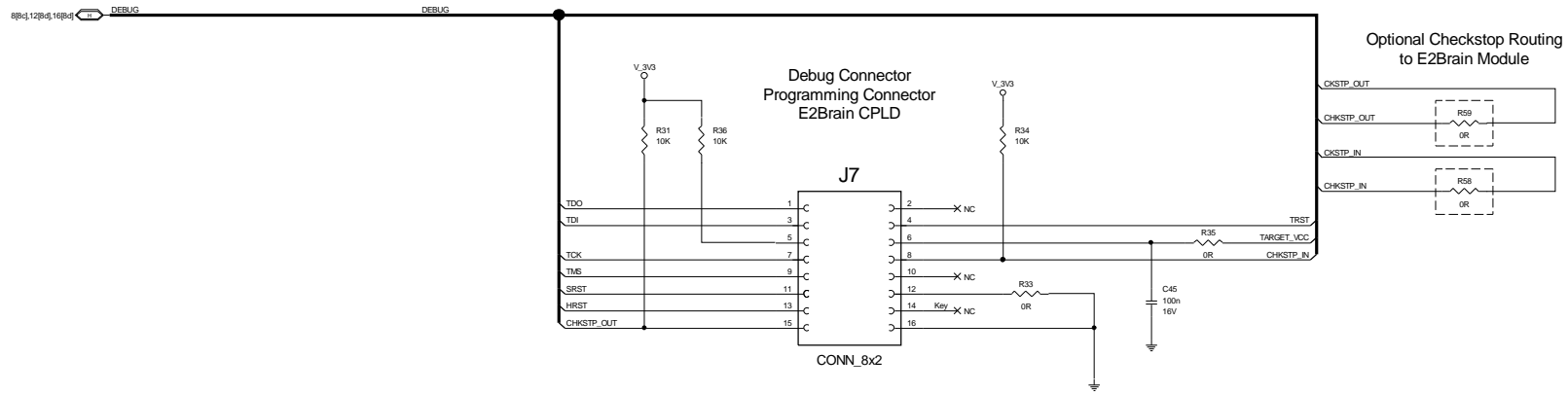
PROJECT EBC3			
ELEMENT LPC_FLASH	ELEMENT PAGE 01 of 01	DIVISION NAME KOM Naegele	DATE 04.2006
FUNCTION		VERIFIED KOM @VER_ENGINEER	@VER_DATE
PCB ID 31.259-1010.1		PCB INDEX 01	SHEET 33 of 37
		APPROVED KOM @APPR_ENGINEER	@APPR_DATE
		REV 00	


COMPACT FLASH SOCKET



PROJECT EBC3			
ELEMENT CF_SOCKET	ELEMENT PAGE 01 of 01	DIVISION NAME KOM Naegele	DATE 04.2006
FUNCTION		VERIFIED KOM @APPR_ENGINEER	@VER_DATE
PCB ID 31.259-1010.1		PCB INDEX 01	SHEET 34 of 37
			REV 00

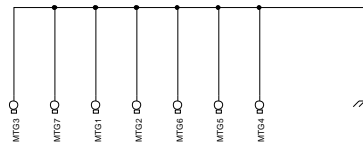
JTAG/DEBUGGING AND PROGRAMMING CONNECTOR



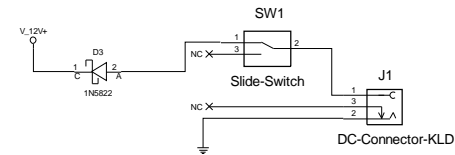
PROJECT EBC3			
ELEMENT JTAG	ELEMENT PAGE 01 of 01	DIVISION NAME KOM Naegele	DATE 04.2006
FUNCTION		VERIFIED KOM @VER_ENGINEER	@VER_DATE
PCB ID 31.259-1010.1		PCB INDEX 01	APPROVED KOM @APPR_ENGINEER
SHEET 35 of 37		REV 00	

Miscellany Power Supply

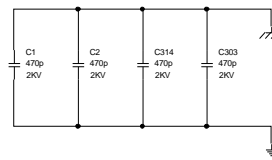
Mounting Holes



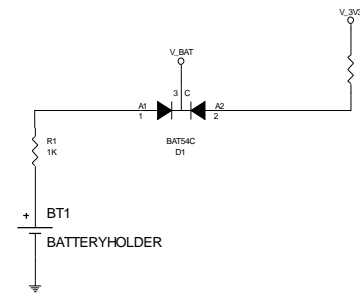
12V supply from external power supply



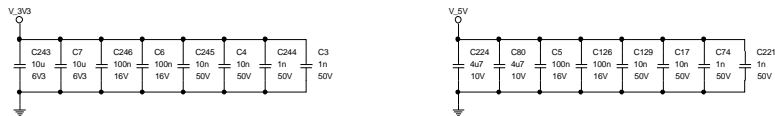
High Voltage GND/Shield Capacitors



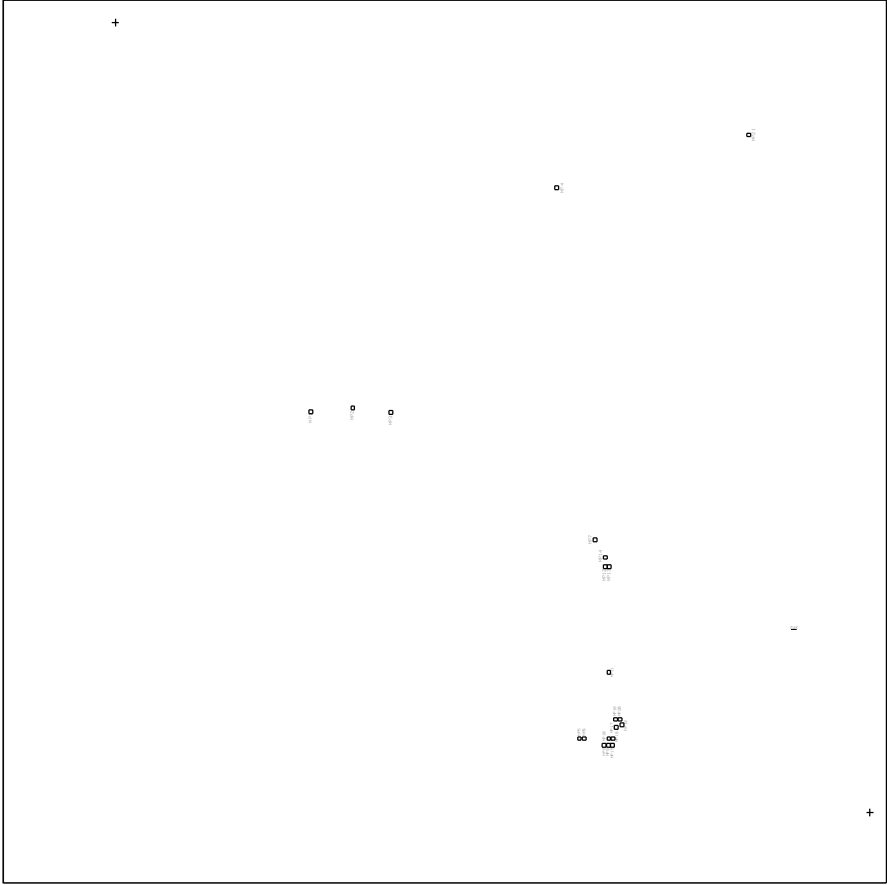
Backup supply options



Board Decoupling



PROJECT EBC3			
ELEMENT POWER	ELEMENT PAGE 02 of 02	DIVISION KOM	NAME Naegele
FUNCTION		DATE 04.2006	
PCB ID 31.259-1010.1		PCB INDEX 01	REV 00
SHEET 37 of 37			



EBC3 31.259-1010.1/01

