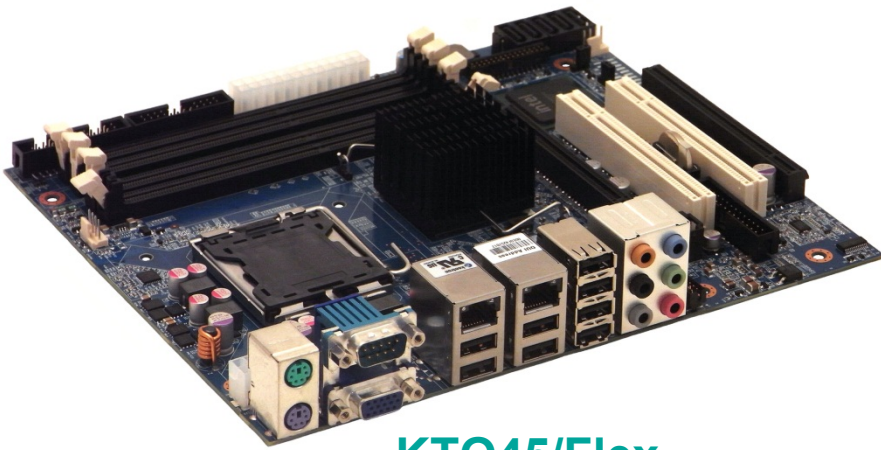
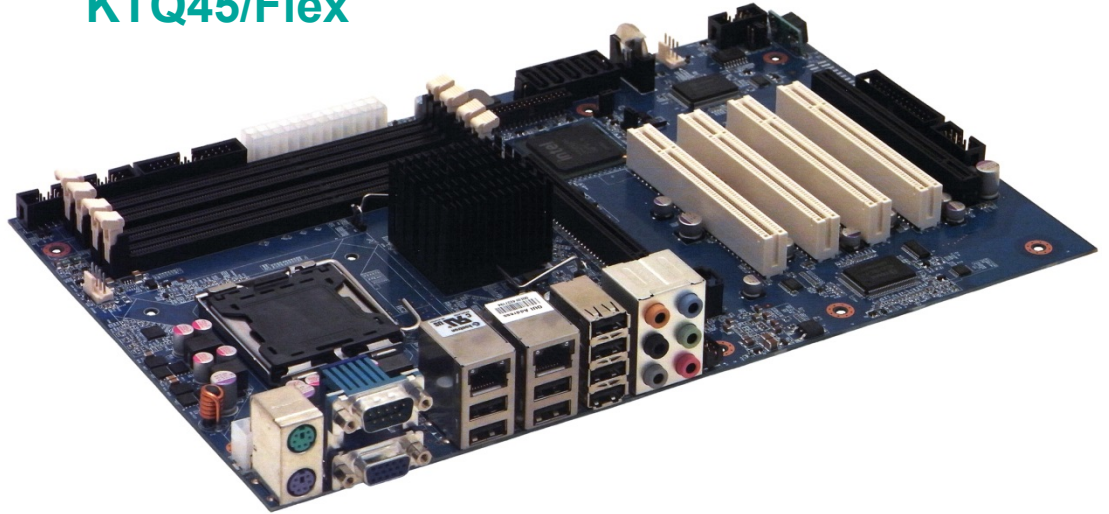


# » Kontron User's Guide «



**KTQ45/Flex**



**KTQ45/ATXE**

## **KTQ45 Users Guide**

KTD-00782-I

## Document revision history.

Rev.	Date	By	Comment
I	Oct. 31 <sup>st</sup> 2013	MLA	Added System Sensor position to pictures. Battery Type no. replaced. Added warning using PCIe Riser. Added more info on BIOS "USB Function". Added BIOS feature "Low RPM Fan Range".
H	July 14 <sup>th</sup> 2011	MLA	Corrected version of the Standard 60950-1. Page 71 correction. Added BIOS setting "C1E Support" and "Intel VT-d". New pictures.
G	Dec. 23 <sup>rd</sup> 2010	MLA	Corrected maximum RAM support. Note for using 820982 corrected. ADD2-CRT support added. Chapter 2.4 corrections. Added note for using both Onboard Graphics and PCIe card. Added note about using SATA converter.
F	Feb. 25 <sup>th</sup> 2010	MLA	Added note on Memory Remap Feature. ATX+12V pinning corrected. Chapter 2.5 updated. Other minor corrections.
E	Nov. 25 <sup>th</sup> 2009	JSE/MLA	Connector list corrected. CPU list correction. Table page 17 corrected. Page 36 (& 12), RS485 description & Note 1 changed.
D	Nov. 17 <sup>th</sup> 2009	MLA	Added/corrected info about ETHER1/ETHER2. RAM PN corrected.
C	Oct. 12 <sup>th</sup> 2009	MLA	Memory Map corrected. JP8 info on page 36 corrected. Added "mounting the board to chassis". PCIe x4 standard 1.1 added.
B	Sep. 22 <sup>nd</sup> 2009	MLA	On page 18: DDR2 corrected to DDR3. Other minor corrections. BIOS part updated and new layout.
A	Aug. 21 <sup>st</sup> 2009	MLA	Layout improvements. Minor additions.
0	July 9 <sup>th</sup> 2009	JSE/MLA	Initial release

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- CPU Board
  1. Type.
  2. Part Number (find PN on label)
  3. Serial Number if available (find SN on label)
- Configuration
  1. CPU Type, Clock speed
  2. DRAM Type and Size.
  3. BIOS Revision (Find the Version Info in the BIOS Setup).
  4. BIOS Settings different than *Default* Settings (Refer to the BIOS Setup Section).
- System
  1. O/S Make and Version.
  2. Driver Version numbers (Graphics, Network, and Audio).
  3. Attached Hardware: Harddisks, CD-rom, LCD Panels etc.

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## Introduction

This manual describes the KTQ45/Flex and KTQ45/ATXE boards made by KONTRON Technology A/S. The boards will also be denoted KTQ45 family if no differentiation is required.

The KTQ45 boards supports the Intel® Core™2 Quad processor Q9000 series, the Intel® Core™2 Duo processor E8000 and E7000 series with a maximum TDP of 95W. These processors belong to the Intel Yorkfield and Wolfdale families.

KTQ45 family differences	Format	PCI	RS232	RS485
KTQ45/Flex	Flex	2	2	0
KTQ45/ATXE	ATX	4	3	1

Use of this Users Guide implies a basic knowledge of PC-AT hard- and software. This manual is focused on describing the KTQ45 Board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in the following chapter before switching-on the power.

All configuration and setup of the CPU board is either done automatically or by the user in the CMOS setup menus. Except for the CMOS Clear jumper (JBAT1), ME Jumper (JBAT2), SPI jumper (JP6), Interface BIOS jumper (JP3 and JP5), RS485 mode selection jumper (KTQ45/ATXE only) (JP7&JP9).

# 1 Installation procedure

## 1.1 Installing the board

To get the board running, follow these steps. In some cases the board shipped from KONTRON Technology has DDR3 DRAM mounted. In this case Step 2 can be skipped.

### 1. Turn off the power supply

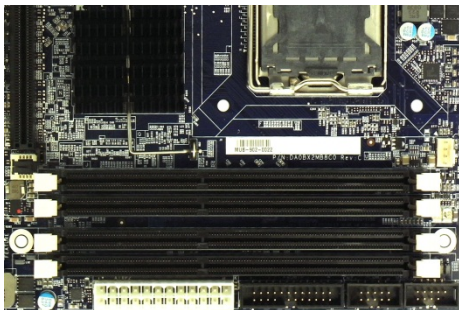


**Warning:** Turn off PSU (Power Supply Unit) completely (no mains power connected to the PSU) or leave the Power Connectors unconnected while configuring the board. Otherwise components (RAM, LAN cards etc.) might get damaged. Do not use PSU's without 3.3V monitoring watchdog, which is standard feature in ATX PSU's. Running the board without 3.3V connected will damage the board after a few minutes.

### 2. Insert the DDR3 DIMM 240pin DRAM module(s)

Be careful to push it in the slot(s) before locking the tabs. For a list of approved DDR3 DIMM modules contact your Distributor or FAE.

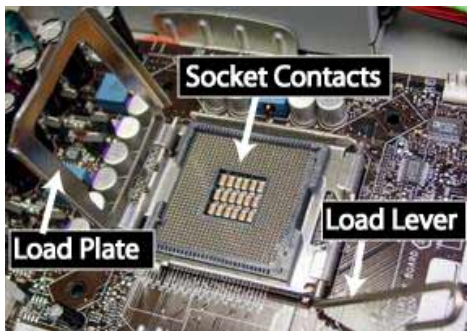
DDR3-800/1066 DIMM 240pin DRAM modules (PC3-6400/PC3-8500) are supported.



**NOTE:** Regardless of the Memory configuration used, DDR3 SLOT 1 (J1) must always be populated.

### 3. Install the processor

The CPU is keyed and will only mount in the CPU socket in one way. Use the handle to open/ close the CPU socket. The Intel® Core™2 Quad, Intel® Core™2 Duo in the LGA775 package are supported, refer to supported processor overview for details.



**Do NOT touch socket contacts**

#### Opening the socket:

Apply pressure to the corner with right hand thumb while opening/closing the load lever, otherwise lever can bounce back like a "mouse trap" and WILL cause bent contacts (when loaded)

1. Disengage Load Lever by depressing down and out on the hook to clear retention tab
2. Rotate Load Lever to fully open position at approximately 135°
3. Rotate Load Plate to fully open position at approximately 100°

#### Remove Socket Protective Cover

With left hand index finger and thumb to support the load plate edge, engage protective cover finger tab with right hand thumb and peel the cover from LGA775 Socket while pressing on center of protective cover to assist in removal.

Set protective cover aside. Always put cover back on if the processor is removed from the socket.



**IMPORTANT:** For return goods (RMA): warranty is void if returned without Protective cover.

**Visually inspect protective cover for damage**

If damage observed, replace the cover.

**Note:** After cover removal, make sure socket load plate and contacts are free of foreign material. Debris may be removed with compressed air.

**Note:** Removing protective cover after CPU insertion will compromise the ability to visually inspect socket.

**Processor Installation**

Locate Connection 1 indicator and the two orientation key notches.

Grasp the processor with thumb and index finger. (Grasp the edges without the orientation notches.)

The socket has cutouts for your fingers to fit into.

Carefully place the package into the socket body using a purely vertical motion. (Tilting the processor into place or shifting it into place on the socket can damage the sensitive socket contacts.)

CAUTION: Recommend not to use a Vacuum Pen for installation.

Verify that package is within the socket body and properly mated to the orientation keys

Close the socket by:

- A. Close the Load Plate
- B. While pressing down lightly on Load Plate, engage the Load Lever.
- C. Secure Load Lever with Load Plate tab under retention tab of Load Lever

**4. Cooler Installation**

Use heat paste or adhesive pads between CPU and cooler and connect the Fan electrically to the FAN\_CPU connector.

**5. Connecting Interfaces**

Insert all external cables for hard disk, keyboard etc. A CRT monitor must be connected in order to change CMOS settings. When using bootable SATA disk, then connect to SATA0 or SATA2 or select in BIOS "ATA/IDE Configuration" = Enhanced.

**6. Connect Power supply**

Connect power supply to the board by the ATX/ BXPWR and 4-pin ATX connectors. For board to operate connection of both the ATX/BTX and 4-pin ATX (12V) connectors are required.

**7. Turn on the power on the ATX/ BTX power supply****8. Power Button**

The PWRBTN\_IN must be toggled to start the Power supply; this is done by shorting pins 16 (PWRBTN\_IN) and pin 18 (GND) on the FRONTPL connector (see Connector description). A "normally open" switch can be connected via the FRONTPL connector.

**9. BIOS Setup**

Enter the BIOS setup by pressing the <Del> key during boot up.

Enter Exit Menu and Load Optimal Defaults.

Refer to the "BIOS Configuration / Setup" section of this manual for details on BIOS setup.

**Note:** To clear all CMOS settings, including Password protection, move the Clr-CMOS jumper (with/without power) for ~1 minute. This will also disable any Secure CMOS setup on the board. Alternatively, turn off power and remove the battery for 1 minute, but be careful to orientate the battery correctly when reinserted.

**10. Mounting the board to chassis**

**Warning:** When mounting the board to chassis etc. please notice that the board contains components on both sides of the PCB which can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.

When fixing the Motherboard on a chassis it is recommended using screws with integrated washer and having diameter of ~7mm.

**Note:** Do not use washers with teeth, as they can damage the PCB mounting hole / cause short circuit.

## 1.2 Requirement according to IEC60950

Users of KTQ45 family boards should take care when designing chassis interface connectors in order to fulfil the IEC60950 standard:

When an interface/connector has a VCC (or other power) pin, which is directly connected to a power plane like the VCC plane:

To protect the external power lines of the peripheral devices, the customer has to take care about:

- That the wires have suitable rating to withstand the maximum available power.
- That the enclosure of the peripheral device fulfils the fire protecting requirements of IEC60950.

### Lithium Battery precautions:

<p style="text-align: center;"><b>CAUTION!</b></p> <p>Danger of explosion if battery is incorrectly replaced.</p> <p>Replace only with same or equivalent type recommended by manufacturer.</p> <p>Dispose of used batteries according to the manufacturer's instructions.</p>	<p style="text-align: center;"><b>VORSICHT!</b></p> <p>Explosionsgefahr bei unsachgemäßem Austausch der Batterie.</p> <p>Ersatz nur durch den selben oder einen vom Hersteller empfohlenen gleichwertigen Typ.</p> <p>Entsorgung gebrauchter Batterien nach Angaben des Herstellers.</p>
<p style="text-align: center;"><b>ADVARSEL!</b></p> <p>Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering.</p> <p>Udskiftning må kun ske med batteri af samme fabrikat og type.</p> <p>Levér det brugte batteri tilbage til leverandøren.</p>	<p style="text-align: center;"><b>ADVARSEL</b></p> <p>Eksplosjonsfare ved feilaktig skifte av batteri.</p> <p>Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten.</p> <p>Brukte batterier kasseres i henhold til fabrikantens instruksjoner.</p>
<p style="text-align: center;"><b>VARNING</b></p> <p>Explosionsfara vid felaktigt batteribyte.</p> <p>Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren.</p> <p>Kassera använt batteri enligt fabrikantens instruktion.</p>	<p style="text-align: center;"><b>VAROITUS</b></p> <p>Paristo voi räjähtää, jos se on virheellisesti asennettu.</p> <p>Vaihda paristo ainoastaan laltevalmistajan suosittelemaan tyyppiin.</p> <p>Hävitä käytetty paristo valmistajan ohjeiden mukaisesti.</p>

## 2 System specification

### 2.1 Component main data

The table below summarizes the features of the KTQ45/Flex and KTQ45/ATXE embedded motherboards.

<b>Form factor</b>	KTQ45/Flex: Flex-ATX (190,5 millimetres by 228,6 millimetres) KTQ45/ATXE: Embedded-ATX (190,5 millimetres by 304,80millimeters)
<b>Processor</b>	<ul style="list-style-type: none"> <li>Support for Supports Intel® Core™2 Quad processor Q9000 series, Supports Intel® Core™2 Duo processor E8000 and E7000 in LGA775 package with up to 1333MHz system bus and 3/6/12MB internal cache.</li> <li>Support for Yorkfield (45 nanometre) and Wolfdale (45 nanometre) family processors.</li> </ul>
<b>Memory</b>	<ul style="list-style-type: none"> <li>4 pieces DDR3 DIMM 240pin DRAM sockets.</li> <li>Dual channel interleaved mode support.</li> <li>Support for DDR 800/1066MHz (PC3-6400/PC3-8500)</li> <li>Support system memory from 512MB and up to 16GB. Less than 4GB displayed in System Properties using 32bit OS. (Shared Video Memory/PCI resources is withdrawn).</li> <li>ECC not supported</li> </ul>
<b>Chipset</b>	Intel Q45+ICH10DO Chipset consisting of: <ul style="list-style-type: none"> <li>Intel® AC82Q45 Graphics Memory Controller Hub (GMCH)</li> <li>Intel® ICH10DO I/O Controller Hub</li> </ul>
<b>Security</b>	<ul style="list-style-type: none"> <li>Intel® Integrated TPM 1.2 support</li> </ul>
<b>Management</b>	<ul style="list-style-type: none"> <li>Intel® Active Management Technology (Intel® AMT) 5.0</li> </ul>
<b>Video</b>	<ul style="list-style-type: none"> <li>Intel® GMA 4500 graphics engine</li> <li>Dynamic Video Memory Technology (DVMT 5.0), allowing up to 384MB dynamically allocated Video Memory (System memory is allocated when it is needed).</li> <li>Analogue Display Support CRT, 350-MHz, 24 bit integrated RAMDAC with support for analogue monitors up to 2048 x 1536 @ 75 Hz</li> <li>Native Display port and DVI support. The digital ports are multiplexed on to the PEG interface using passive PEG card (Accessory).</li> <li>Serial Digital Video Out (SDVO) ports (2 channels) for additional CRT, LVDS panel, DVI, TV-Out and/or HDMI support via Advanced Digital Display 2 (ADD2) cards or Media Expansion Cards.</li> <li>Dual independent pipe support, Mirror and Dual independent display support Dual Monitor support with combinations of SDVO port devices and onboard CRT</li> </ul>
<b>Audio</b>	Audio, 7.1 Channel High Definition Audio Codec using the VIA 1708B codec <ul style="list-style-type: none"> <li>Line-out</li> <li>Line-in</li> <li>Surround output: SIDE, LFE, CEN, BACK and FRONT</li> <li>Microphone: MIC1</li> <li>CDROM in</li> <li>SPDIF Interface</li> <li>Onboard speaker</li> </ul>

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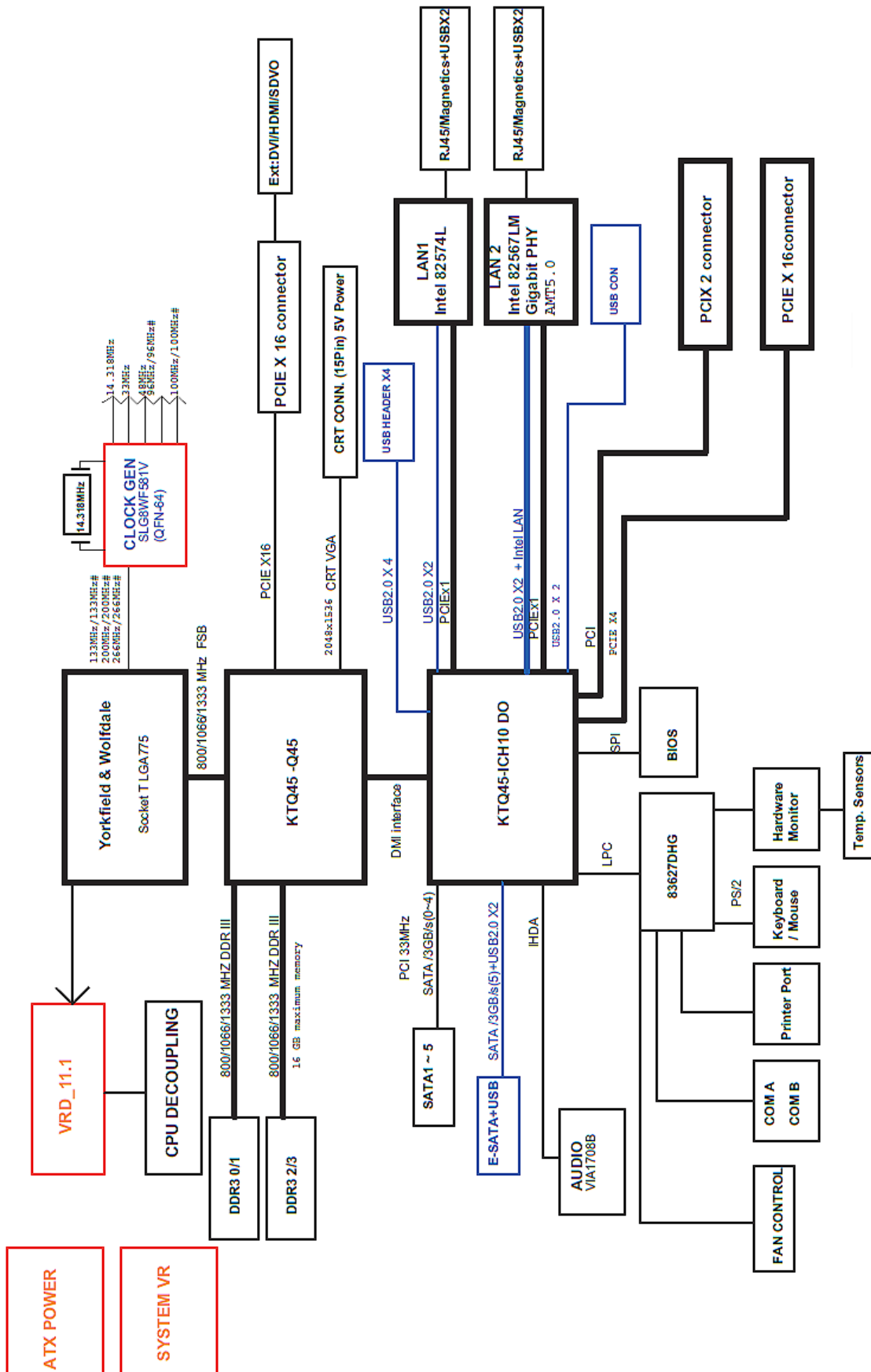
<b>I/O Control</b>	Winbond W83627DHG LPC Bus I/O Controller
<b>Peripheral interfaces</b>	<ul style="list-style-type: none"> <li>• Eight USB 2.0 ports on I/O area</li> <li>• Four USB 2.0 ports on internal pinrows</li> <li>• Two Serial ports (RS232) KTQ45/Flex, Four Serials ports 3x(RS323), 1x(RS485) (Galvanic isolated) with full duplex support on KTQ45/ATXE</li> <li>• One Parallel port, SPP/EPP/ECP</li> <li>• Five Serial ATA-300 IDE interfaces with RAID 0/1/5/10 support</li> <li>• PS/2 keyboard and mouse ports</li> </ul>
<b>LAN Support</b>	<ul style="list-style-type: none"> <li>• 1x 10/100/1000Mbps/s using NIC Intel® Boazman-LM WG82567LM (ETHER1) (connected to ICH10DO Integrated GbE MAC supporting AMT 5.0)</li> <li>• 1x 10/100/1000Mbps/s using NIC Intel® Hartwell 82574L (ETHER2)</li> <li>• PXE netboot supported. Wake On LAN (WOL) supported.</li> </ul>
<b>BIOS</b>	<ul style="list-style-type: none"> <li>• Kontron Technology / AMI BIOS (core version)</li> <li>• Support for Advanced Configuration and Power Interface (ACPI 3.0), Plug and Play <ul style="list-style-type: none"> <li>○ Suspend To Ram</li> <li>○ Suspend To Disk</li> <li>○ Intel Speed Step</li> </ul> </li> <li>• Secure CMOS/ OEM Setup Defaults</li> <li>• “Always On” BIOS power setting</li> <li>• RAID Support (RAID modes 0, 1, 5 and 10) (for Linux O/S only RAID 0 and 1)</li> </ul>
<b>Expansion Capabilities</b>	<ul style="list-style-type: none"> <li>• PCI Bus routed to PCI slot(s) (PCI Local Bus Specification Revision 2.3) <ul style="list-style-type: none"> <li>○ KTQ45/Flex: 2 slots PCI 2.3, 32 bits, 33 MHz, 5V compliant</li> <li>○ KTQ45/ATXE: 4 slots PCI 2.3, 32 bits, 33 MHz, 5V compliant</li> </ul> </li> <li>• PCI-Express bus routed to PCI Express slot(s) (PCI Express 2.0) <ul style="list-style-type: none"> <li>○ KTQ45/Flex and KTQ45/ATXE: <ul style="list-style-type: none"> <li>1 slot PCI-Express x16 (PCI Express 2.0)</li> <li>1 slot PCI-Express x4 (PCI Express 1.1)</li> </ul> </li> </ul> </li> <li>• SMBus routed to FEATURE, PCI slot, PCI Express</li> <li>• LPC Bus routed to TPM connector</li> <li>• DDC Bus routed to CRT connector</li> <li>• 8 x GPIOs (General Purpose I/Os) routed to FEATURE connector</li> </ul>
<b>Hardware Monitor Subsystem</b>	<ul style="list-style-type: none"> <li>• Smart Fan control system, support Thermal® and Speed® cruise for three onboard Fan control connectors: FAN_CPU, FAN_SYS and FEATURE</li> <li>• Three thermal inputs: CPU die temperature, System temperature and External temperature input routed to FEATURE connector. (Precision +/- 3°C)</li> <li>• Voltage monitoring</li> <li>• Intrusion detect input</li> <li>• SMI violations (BIOS) on HW monitor not supported. Supported by API (Windows).</li> </ul>
<b>Operating Systems Support</b>	<ul style="list-style-type: none"> <li>• WinXP</li> <li>• WinVista</li> <li>• Linux: Red Hat 5 U2, SuSe 10 SP2 (limitations may apply)</li> </ul>

(Continues)

<b>Environmental Conditions</b>	<p><b>Operating:</b> 0°C – 55°C operating temperature (forced cooling). It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within allowed temperature range. Note: KTQ45 operating temperature range is 0°C – 60°C (forced cooling) but CPU cooling limitations typically lowers the maximum temperature to 55°C.</p> <p>10% - 90% relative humidity (non-condensing)</p> <p><b>Storage:</b> -20°C – 70°C 5% - 95% relative humidity (non-condensing)</p> <p><b>Electro Static Discharge (ESD) / Radiated Emissions (EMI):</b> All Peripheral interfaces intended for connection to external equipment are ESD/ EMI protected. EN 61000-4-2:2000 ESD Immunity EN55022:1998 class B Generic Emission Standard.</p> <p><b>Safety:</b> IEC 60950-1: 2005, 2<sup>nd</sup> edition UL 60950-1 CSA C22.2 No. 60950-1 Product Category: Information Technology Equipment Including Electrical Business Equipment Product Category CCN: NWGQ2, NWGQ8 File number: E194252</p> <p><b>Theoretical MTBF:</b> 449.463 / 226.855 hours @ 40°C / 60°C for the KTQ45/Flex 352.559 / 174.306 hours @ 40°C / 60°C for the KTQ45/ATXE</p> <p><b>Restriction of Hazardous Substances (RoHS):</b> All boards in the KTQ45 family are RoHS compliant.</p> <p><b>Capacitor utilization:</b> No Tantalum capacitors on board Only Japanese brand Solid capacitors rated for 100degrees Celsius used on board</p>
<b>Battery</b>	<p>Exchangeable 3.0V Lithium battery for onboard Real Time Clock and CMOS RAM. Manufacturer Panasonic / Part-number CR-2032L/BN, CR2032N/BN or CR-2032L/BE. Approximate 4-5 years retention. Current draw is 5-6µA when PSU is disconnected.</p> <p><b>CAUTION: Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.</b></p>

## 2.2 System overview

The block diagram below shows the architecture and main components of the KTQ45 boards. The two key components on the board are the Intel® Q45 and Intel® ICH10DO Chipsets. Components shown shaded are optional depending on board type (KTQ45/Flex and ATXE) and variants of the board.



## 2.3 Processor Support Table

The KTQ45/Flex and ATXE are designed to support the following LGA775 processors:

**Intel® Core™ 2 Quad Processor**

**Intel® Core™ 2 Quad Mobile Processor**

**Intel® Core™ 2 Duo Processor**

**Intel® Pentium® Processor (2 cores)**

**Intel® Celeron®**

In the following list you will find all CPU's supported by the chipset in according to Intel but also other CPU's if successfully tested.

Embedded CPU's are indicated by **green** text.

Successfully tested CPU's are indicated by **highlighted** text.

Successfully tested embedded CPU's are indicated by **green and highlighted** text

Failed CPU's are indicated by **red** text.

Some of the processors in the list are distributed from Kontron, those CPU's are marked by an \* (asterisk) right after the CPU number. However please notice that this marking is only guide line and maybe not fully updated.

Processor Brand	Clock Speed [GHz]	Bus Speed [MHz]	Cache [MB]	CPU Number	sSpec no.	Thermal Guideline [Watt]
Intel® Core™2 Quad (Yorkfield)	<b>3.00</b>	<b>1333</b>	<b>12</b>	<b>Q9650 *</b>	<b>SLB8W</b>	<b>95</b>
	2.83	1333	12	Q9550		95
	<b>2.83</b>	<b>1333</b>	<b>12</b>	<b>Q9550S</b>		<b>86.5</b>
	2.66	1333	12	Q9450	SLAWR	95
	<b>2.66</b>	<b>1333</b>	<b>6</b>	<b>Q9400 *</b>	<b>SLB6B</b>	<b>95</b>
	2.66	1333	6	Q9400S		65
	2.50	1333	6	Q9300		95
	2.66	1333	4	Q8400		95
	2.66	1333	4	Q8400S		65
	2.50	1333	4	Q8300		95
	2.33	1333	4	Q8200		95
	2.33	1333	4	Q8200S		65
Intel® Core™2 Quad (Kentsfield)	2.66	1066	8	Q6700		105
	2.40	1066	8	Q6600		105
Intel® Core™ 2 Duo (Wolfdale)	3.33	1333	6	E8600		65
	3.16	1333	6	E8500		65
	3.00	1333	6	E8400	SLAPL	65
	<b>3.00</b>	<b>1333</b>	<b>6</b>	<b>E8400 *</b>	<b>SLB9J</b>	<b>65</b>
	2.83	1333	6	E8300		65
	2.66	1333	6	E8200		65
	2.66	1333	6	E8190		65
	3.06	1066	3	E7600		65
	2.93	1066	3	E7500		65
	<b>2.93</b>	<b>1066</b>	<b>2</b>	<b>E6500</b>	<b>SLGUM</b>	<b>65</b>
	<b>2.80</b>	<b>1066</b>	<b>3</b>	<b>E7400</b>	<b>SLGW3</b>	<b>65</b>
	2.80	1066	2	E6300	SLGU9	65
	2.70	800	2	E5400		65
	2.66	1066	3	E7300		65
	<b>2.60</b>	<b>800</b>	<b>2</b>	<b>E5300</b>	<b>SLGTL</b>	<b>65</b>
	2.50	800	2	E5200		65
2.53	1066	3	E7200		65	

(Continues)

Processor Brand	Clock Speed [GHz]	Bus Speed [MHz]	Cache [MB]	CPU Number	sSpec no.	Thermal Guideline [Watt]
Intel® Core™ 2 Duo (Conroe)	3.00	1333	4	E6850		65
	2.66	1333	4	E6750		65
	2.66	1333	4	E6700		65
	2.60	800	2	E4700		65
	2.40	1066	4	E6600		65
	2.33	1066	4	E6550		65
	2.33	1066	4	E6540		65
	2.13	1066	4	E6420		65
	2.13	1066	2	E6400 *	SLA97	65
	1.86	1066	4	E6320		65
	1.86	1066	2	E6300	SL9TA	65
	2.40	800	2	E4600		65
	2.20	800	2	E4500		65
	2.00	800	2	E4400		65
	1.80	800	2	E4300	SL9TB	65
	1.80	800	2	E4300 *	SLA99	65
Intel® Pentium® (2 Cores) (Conroe)	2.40	800	1	E2220		65
	2.20	800	1	E2200		65
	2.00	800	1	E2180		65
	1.80	800	1	E2160 *	SLA8Z	65
	1.60	800	1	E2140		65
Intel® Celeron® (Conroe)	2.40	800	0.5	E1600		65
	2.20	800	0.5	E1500 *	SLAQZ	65
	2.20	800	0.5	450		35
	2.00	800	0.5	440 *	SL9XL	35
	2.00	800	0.5	E1400		65
	1.80	800	0.5	430		35
	1.60	800	0.5	420		35
1.60	800	0.5	E1200		65	

## 2.4 System Memory support

The KTQ45 boards have four onboard DDR3 DIMM sockets and support the following memory features:

DDR3-800/1066 DIMM 240pin DRAM modules (PC3-6400/PC3-8500)

- 1.5V (only) 240-pin DDR3 SDRAM DIMMs with gold-plated contacts
- DDR3-800 (PC3-6400), DDR3-1066 (PC3-8500) SDRAM DIMMs
- DDR3-800/1066 DIMM with SPD timings supported
- Unbuffered, single-sided x8/x16 or double-sided x8/x16 DIMMs
- 16 GB (4 x 4GB) maximum total system memory using 64-bit OS. (Shared Video Memory is withdrawn).
- 4 GB maximum total system memory using 32-bit OS. ~3GB is displayed in System Properties. (Shared Video Memory is withdrawn).
- Minimum total system memory: 512 MB
- Non-ECC DIMMs
- Serial Presence Detect

The installed DDR3 SDRAM should support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read and configure the memory controller for optimal performance. If non-SPD memory is used, the BIOS will attempt to configure the memory settings, but performance and reliability may be impacted.

### Memory Operating Frequencies

Regardless of the DIMM type used, the memory frequency will either be equal to or less than the processor system bus frequency. For example, if DDR3 800 memory is used with an 800 MHz system bus frequency processor, the memory clock will operate at 400 MHz. The table below lists the resulting operating memory frequencies based on the combination of DIMMs and processors.

DIMM Type	Module name	Memory Data transfers [Mill/s]	Processor system bus frequency [MHz]	Resulting memory frequency [MHz]	clock	Peak transfer rate [MB/s]
DDR3 800	PC3-6400	800	800	400		6400
DDR3 800	PC3-6400	800	1066	400		6400
DDR3 800	PC3-6400	800	1333	400		6400
DDR3 1066	PC3-8500	1066	800	400		6400
DDR3 1066	PC3-8500	1066	1066	533		8533
DDR3 1066	PC3-8500	1066	1333	533		8533

**Notes:** Kontron offers the following memory modules:

- P/N 1028-6891, DDR3-RAM, **1GB**, 240p, 800MHZ, PC3-8500, DIMM
- P/N 1028-6892, DDR3-RAM, **2GB**, 240p, 800MHZ, PC3-8500, DIMM
- Faster RAM like PC3-10600 can be used but will run at lower speed.

### Memory Configurations

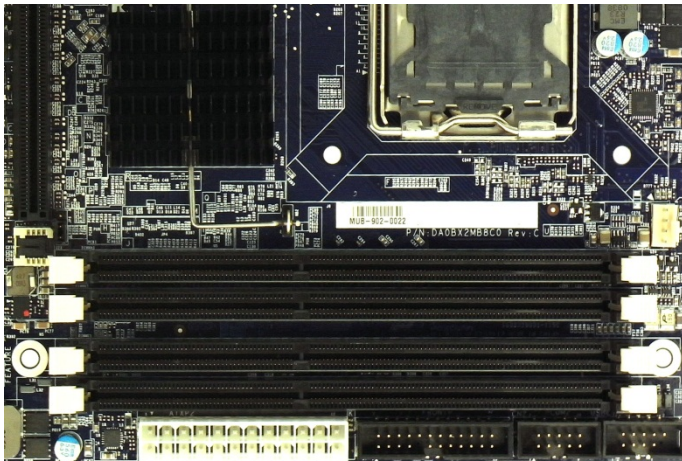
The KTQ45 boards support the following three types of memory organization:

1. Dual channel (Interleaved) mode. This mode offers the highest throughput. Dual channel mode is enabled when the installed memory capacities of both DIMM channels are equal. Technology and device width can vary from one channel to the other but the installed memory capacity for each channel must be equal. If different speed DIMMs are used between channels, the slowest memory timing will be used.

2. Single channel (Asymmetric) mode. This mode is equivalent to single channel bandwidth operation. This mode is used when only a single DIMM is installed or the memory capacities of channel A is bigger than of channel B. Technology and device width can vary from one channel to the other. If different speed DIMMs are used between channels, the slowest memory timing will be used.

3. Flex mode. This mode provides the most flexible performance characteristics and is used if both channels are populated and at the same time the memory capacities of channel A is smaller than of channel B.

Channel B will be divided into two parts. One part of channel B is used together with channel A and mapped to dual channel operation. The second part of channel B is mapped to single channel operation.



- ← Channel A, DDR3 DIMMA1 (SLOT 1)
- ← Channel A, DDR3 DIMMB1 (SLOT 2)
- ← Channel B, DDR3 DIMMC1 (SLOT 3)
- ← Channel B, DDR2 DIMMD1 (SLOT 4)

**Note:**

Regardless of the memory configuration Dual Channel, Single Channel or Flex, the DIMMA1 **must** always be populated. This is a requirement of the Intel® Management Engine.

The below tables shows examples of possible Memory slot configurations for the support of the various Memory modes.

Dual Channel Interleaved Mode Configurations			
Channel A		Channel B	
DDR3 DIMMA1 (SLOT 1)	DDR3 DIMMB1 (SLOT 2)	DDR3 DIMMC1 (SLOT 3)	DDR3 DIMMD1 (SLOT 4)
2 GB		2 GB	
1 GB	1 GB	2 GB	
1 GB	2 GB	1 GB	2 GB

In these examples the combined capacity of the two DIMMs in Channel A equals the combined capacity of the two DIMMs in Channel B.

Single Channel Asymmetric Mode Configurations			
Channel A		Channel B	
DDR3 DIMMA1 (SLOT 1)	DDR3 DIMMB1 (SLOT 2)	DDR3 DIMMC1 (SLOT 3)	DDR3 DIMMD1 (SLOT 4)
2 GB			
1 GB	2 GB	2 GB	

In these examples the combined capacity of the two DIMMs in Channel A does not equal the capacity of the DIMMs in Channel B.

Dual Channel Flex Mode Configurations			
Channel A		Channel B	
DDR3 DIMMA1 (SLOT 1)	DDR3 DIMMB1 (SLOT 2)	DDR3 DIMMC1 (SLOT 3)	DDR3 DIMMD1 (SLOT 4)
1 GB		2 GB	

The 1 GB DIMM in the Channel A, DIMM 0 socket and the lower 1 GB of the DIMM in the Channel B, DIMM 0 socket operate together in dual channel mode. The remaining (upper) 1 GB of the DIMM in Channel B operates in single channel mode.

## 2.5 KTQ45 Graphics Subsystem

The KTQ45 boards use the Intel Q45 chipset for the graphical control. This chipset contains two separate, mutually exclusive graphics options. Either the GMA 4500 graphics controller (contained within the AC82Q45 GMCH) is used, or a PCI Express x16 add-in card can be used. When a PCI Express x16 add-in card is installed, the GMA 4500 graphics controller is disabled.

### 2.5.1 Intel® GMA 4500

Features of the Intel GMA (Graphic Media Accelerator) 4500 graphics controller includes:

- High quality graphics engine supporting
  - DX10\* and OpenGL\* 2.0 compliant
  - Core frequency of 400 MHz
  - 1.6 GP/s pixel rate
  - High-Quality 3D Setup and Render Engine
  - High-Quality Texture Engine
  - 3D Graphics Rendering Enhancements
  - 2D Graphics
  - Video Overlay
  - Multiple Overlay Functionality
- Analogue Display (CRT)
  - 350 MHz Integrated 24-bit RAMDAC
  - Up to 2048x1536 @ 75 Hz refresh
  - Hardware Colour Cursor Support
  - DDC2B Compliant Interface
- Multiplexed PCIe x16, SDVO and TMDS.
  - PCIe x16 supports also PCIe Graphics card. Using PCIe Graphics card in combination with onboard graphics (VGA) is possible if BIOS setting *Initial Graphics Adaptor = IGD*. In this case onboard graphic will be Primary desktop and PCIe Graphics will be extended desktop. Note that PCIe Graphics driver shall be installed before the Intel Graphics driver
  - SDVO (Serial Digital Video Out) ports (2 channels single mode) for additional ADD2 (Advanced Digital Display 2) cards supporting second CRT monitor or Dual LVDS (Low Voltage Differential Signalling) panels or DVI (Digital Visual Interface) panels.
  - TMDS (Transition Minimized Differential Signalling) (2 channels) for additional, HDMI (High-Definition Multimedia Interface) support with HDCP (High-bandwidth Digital Content Protection) and HD Audio, DVI support, or DP (DisplayPort) support with 8/10 bit colours in WQXGA (2560x1600 pixels) and HDCP.
  - DVI, HDMI and DP support Hot-Plug.
  - 200 MHz dot clock on each 12-bit interface
  - Dual independent display options with digital display
- Dynamic Video Memory Technology (DVMT 5.0) support up to 352 MB



**Warning:** It is not recommended to use any PCIe Riser card in combination with PCIe Graphics card. Such combination does not comply with PCI Express 2.0 standard with the risk of generating instability.

## 2.5.2 DVMT 5.0 support

DVMT (Dynamic Video Memory Technology driven by OS driver) enables enhanced graphics and memory performance through highly efficient memory utilization. DVMT ensures the most efficient use of available system memory for maximum 2-D/3-D graphics performance. Up to 352 MB of system memory can be allocated to DVMT on systems that have 512 MB or more of total system memory installed. DVMT returns system memory back to the operating system when the additional system memory is no longer required by the graphics subsystem.

DVMT will always use a minimal fixed portion of system physical memory (as set in the BIOS Setup) for compatibility with legacy applications. An example of this would be when using VGA graphics under DOS. Once loaded, the operating system and graphics drivers allocate additional system memory to the graphics buffer as needed for performing graphics functions.

## 2.5.3 ADD2 card support

The KTQ45 board routes two multiplexed SDVO ports that are each capable of driving up to a 200 MHz pixel clock to the PCI Express x16 connector. The SDVO ports can be paired for a dual channel configuration to support up to a 400 MHz pixel clock. When an ADD2 (Advanced Digital Display) card is detected, the Intel GMA 4500 graphics controller is enabled and the PCI Express x16 connector is configured for SDVO mode. SDVO mode enables the SDVO ports to be accessed by the ADD2 card. An ADD2 card can either be configured to support simultaneous display with the primary VGA display or can be configured to support dual independent display as an extended desktop configuration with different colour depths and resolutions.

ADD2 cards can be designed to support the following configurations:

- TV-Out (composite video)
- TMDS for DVI 1.0
- LVDS
- Single device operating in dual channel mode
- VGA output
- HDTV output
- HDMI support (when used with the HD Audio Link)

Currently available Kontron ADD2 cards

- P/N 820953, ADD2-LVDS
- P/N 820950, ADD2-Dual LVDS
- P/N 820951, ADD2-Dual Internal DVI
- P/N 820952, ADD2-Dual DVI
- P/N 820954, ADD2-CRT

Please visit the Kontron website ([www.kontron.com](http://www.kontron.com)) for details.

## 2.5.4 PCIe Passive Graphic card support

The KTQ45 board routes two TMDS ports that are each capable of driving up to a 200 MHz pixel clock to the PCI Express x16 connector. When a TMDS card is detected, the Intel GMA 4500 graphics controller is enabled and the PCI Express x16 connector is configured for TMDS mode. A TMDS card can either be configured to support simultaneous display with the primary VGA display or can be configured to support dual independent display as an extended desktop configuration with different colour depths and resolutions.

PCIe Passive Graphic cards can be designed to support the following configurations:

- TMDS for DVI 1.0
- Display Port
- HDMI support

Currently available Kontron PCIe Passive Graphic cards:

- P/N 820977, KT-PCIe-DVI-HDMI-I, (HDMI, and DVI with TMDS option).

Please visit the Kontron website ([www.kontron.com](http://www.kontron.com)) for details.

## 2.6 Power Consumption

In order to ensure safe operation of the board, the ATX power supply must monitor the supply voltage and shut down if the supplies are out of range – refer to the hardware manual for actual power specification.

The KTQ45/Flex board is powered through the ATX connector and the additional 12V separate supply for CPU as specified in the ATX specification; besides this the power supplied to the board must be within the ATX specification.

The requirements to the supply voltages are as follows:

Supply	Min	Max	Note
VCC3.3	3.168V	3.432V	Should be $\pm 4\%$ for compliance with the ATX specification
VCC	4.75V	5.25V	Should be $\pm 5\%$ for compliance with the ATX specification. Should be minimum 5.00V measured at USB connectors in order to meet the requirements of USB standard.
+12V	11.4V	12.6V	Should be $\pm 5\%$ for compliance with the ATX specification
-12V	-13.2V	-10.8V	Should be $\pm 10\%$ for compliance with the ATX specification
-5V	-5.50V	-4.5V	Not required for the KTQ45 boards
5VSB	4.75V	5.25V	Should be $\pm 5\%$ for compliance with the ATX specification

### Static Power Consumption

The power consumption of the KTQ45/ATXu Board is measured under:

- 1- DOS, idle, mean
- 2- WindowsXP, Running 3DMARK 2001 & 2 x CPU BURN, mean
- 3- S1, mean
- 4- S3, mean
- 5- S4, mean

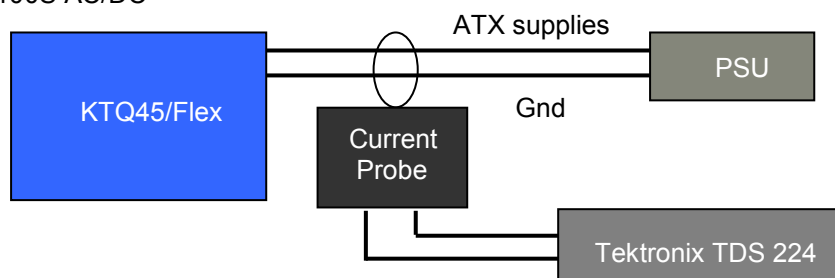
### Test system configuration

### Test system configuration

The following items were used in the test setup:

1. KTQ45/Flex board mounted w/ 3.00GHz (E8400) Core Duo & 1GB Samsung 1Rx8 PC3-10600U-09-00-A0 1,5V DDR3 Ram
2. 12V active cooler
3. PS/2 keyboard & mouse (Mouse: Genius Netscroll+ Keyboard:ACK-595)
4. CRT (Nokia 477Pro)
5. HD (Seagate Barracuda 7200.10 160 GB)
6. ATX PSU (OCZ-420ADJ)
7. Tektronix TDS 224, P6345 probes
8. Fluke Current Probe 80i-100S AC/DC

### Test setup



**Note:** The Power consumption of CRT, HD and Fan is not included.

DOS Idle, Mean, No external load		
Supply	Current draw	Power consumption
+12V	1.59A	19.08W
+5V	1.39A	6.95W
+3V3	1.28A	4.224W
-12V	-	0W
5VSB	-	0W
<b>Total</b>		<b>30.254W</b>

Windows XP, mean 3DMARK2001 (Game 1 – Car Chase test ) & 2 x CPUBURN		
Supply	Current draw	Power consumption
+12V	3.16A	37.92W
+5V	1.55A	7.75W
+3V3	2.8A	9.24W
-12V	0.00A	0W
5VSB	0.00A	0W
<b>Total</b>		<b>54.91W</b>

S1 Mode, Mean, No external load		
Supply	Current draw	Power consumption
+12V	0.76A	9.12W
+5V	1.11A	5.55W
+3V3	1.14A	3.762W
-12V	0.00A	0W
5VSB	0.00A	0W
<b>Total</b>		<b>18.432W</b>

S3 Mode, Mean, No external load		
Supply	Current draw	Power consumption
+12V	0.00A	0W
+5V	0.00A	0W
+3V3	0.00A	0W
-12V	0.00A	0W
5VSB	0.21A	1.05W
<b>Total</b>		<b>1.05W</b>

S4 Mode, Mean, No external load		
Supply	Current draw	Power consumption
+12V	0.00A	0W
+5V	0.00A	0W
+3V3	0.00A	0W
-12V	0.00A	0W
5VSB	0.21A	1.05W
<b>Total</b>		<b>1.05W</b>

### 3 Connector Definitions

The following sections provide pin definitions and detailed description of all on-board connectors.

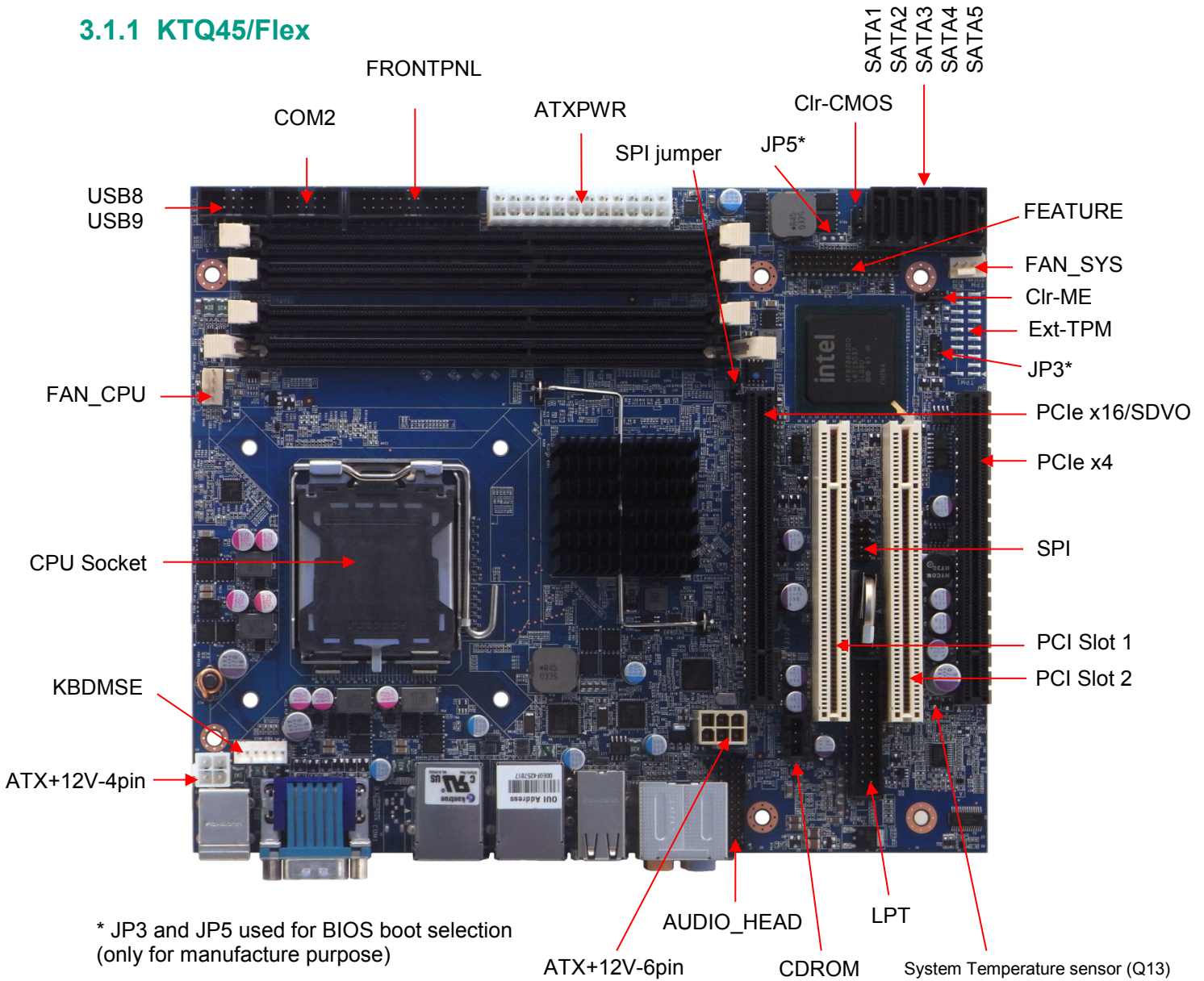
The connector definitions follow the following notation:

Column name	Description
Pin	Shows the pin-numbers in the connector. The graphical layout of the connector definition tables is made similar to the physical connectors.
Signal	The mnemonic name of the signal at the current pin. The notation "XX#" states that the signal "XX" is active low.
Type	AI: Analogue Input. AO: Analogue Output. I: Input, TTL compatible if nothing else stated. IO: Input / Output. TTL compatible if nothing else stated. IOT: Bi-directional tristate IO pin. IS: Schmitt-trigger input, TTL compatible. IOC: Input / open-collector Output, TTL compatible. NC: Pin not connected. O: Output, TTL compatible. OC: Output, open-collector or open-drain, TTL compatible. OT: Output with tri-state capability, TTL compatible. LVDS: Low Voltage Differential Signal. PWR: Power supply or ground reference pins.
	Ioh: Typical current in mA flowing out of an output pin through a grounded load, while the output voltage is > 2.4 V DC (if nothing else stated). Iol: Typical current in mA flowing into an output pin from a VCC connected load, while the output voltage is < 0.4 V DC (if nothing else stated).
Pull U/D	On-board pull-up or pull-down resistors on input pins or open-collector output pins.
Note	Special remarks concerning the signal.

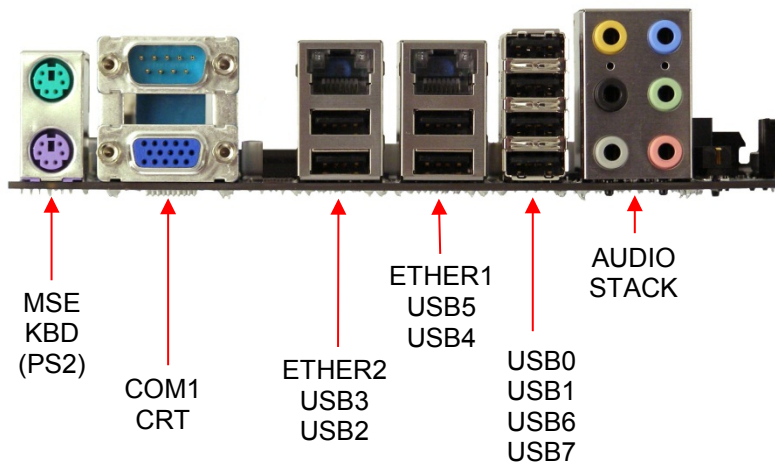
The abbreviation *TBD* is used for specifications which are not available yet or which are not sufficiently specified by the component vendors.

### 3.1 Connector layout

#### 3.1.1 KTQ45/Flex

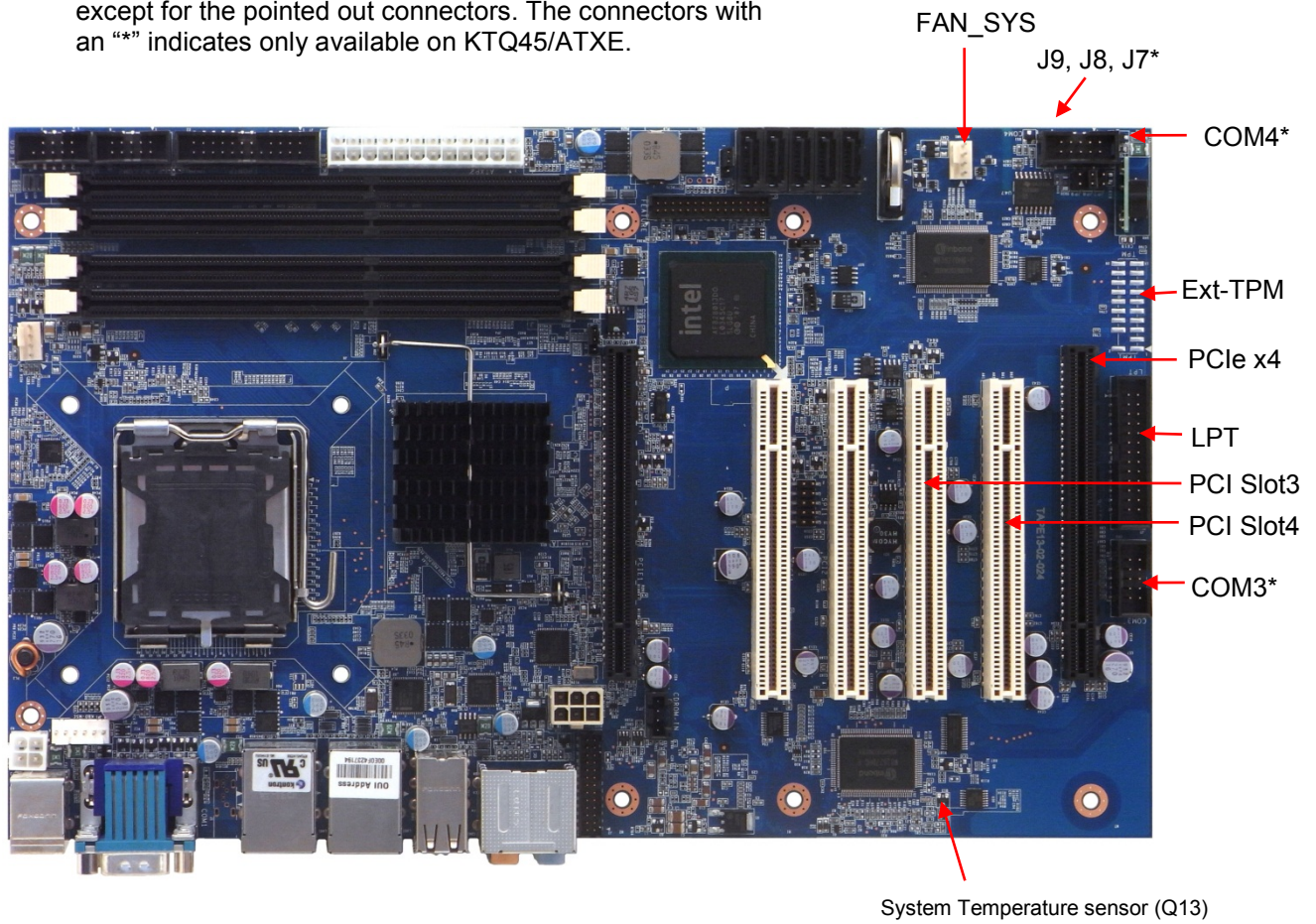


#### 3.1.2 KTQ45 - IO Bracket area



### 3.1.3 KTQ45/ATXE

Connectors are at the same location as on KTQ45/Flex, except for the pointed out connectors. The connectors with an "\*" indicates only available on KTQ45/ATXE.



## 3.2 Power Connector (ATXPWR)

The KTQ45 boards are designed to be supplied from a standard ATX or BTX power supply.

ATX/ BTX Power Connector:

Note	Type	Signal	PIN		Signal	Type	Note
	PWR	3V3	12	24	GND	PWR	
	PWR	+12V	11	23	5V	PWR	
	PWR	+12V	10	22	5V	PWR	
	PWR	SB5V	9	21	5V	PWR	
	I	P_OK	8	20	-5V	PWR	1
	PWR	GND	7	19	GND	PWR	
	PWR	5V	6	18	GND	PWR	
	PWR	GND	5	17	GND	PWR	
	PWR	5V	4	16	PS_ON#	OC	
	PWR	GND	3	15	GND	PWR	
	PWR	3V3	2	14	-12V	PWR	
	PWR	3V3	1	13	3V3	PWR	

**Note 1:** -5V supply is not used onboard.

Note: Use of BTX supply not required for operation, but may be required to drive high-power PCIe cards.

See chapter "Power Consumption" regarding input tolerances on 3.3V, 5V, SB5V, +12 and -12V (also refer to ATX specification version 2.2).

ATX+12V-6pin Power Connector (same net as +12V in ATX/BTX Power connector):

Note	Type	Signal	PIN		Signal	Type	Note
1	PWR	+12V	3	6	GND	PWR	
1	PWR	+12V	2	5	GND	PWR	
	PWR	+12V	1	4	GND	PWR	

ATX+12V-4pin Power Connector:

Note	Type	Signal	PIN		Signal	Type	Note
	PWR	GND	2	4	+12V	PWR	1
	PWR	GND	1	3	+12V	PWR	1

**Note 1:** Use of the 4-pin ATX+12V Power Connector is required for operation of the KTQ45 boards.

Signal	Description
P_OK	<p>P_OK is a power good signal and should be asserted high by the power supply to indicate that the +5VDC and +3.3VDC outputs are above the under voltage thresholds of the power supply. When this signal is asserted high, there should be sufficient energy stored by the converter to guarantee continuous power operation within specification. Conversely, when the output voltages fall below the under voltage threshold, or when mains power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, P_OK should be de-asserted to a low state. The recommended electrical and timing characteristics of the P_OK (PWR_OK) signal are provided in the <i>ATX12V Power Supply Design Guide</i>.</p> <p>It is strongly recommended to use an ATX or BTX supply with the KTQ45 boards, in order to implement the supervision of the 5V and 3V3 supplies. These supplies are not supervised onboard the KTQ45 boards.</p>
PS_ON#	Active low open drain signal from the board to the power supply to turn on the power supply outputs. Signal must be pulled high by the power supply.

### 3.3 Keyboard and Mouse connectors

Attachment of a keyboard or PS/2 mouse adapter can be done through the stacked PS/2 mouse and keyboard connector (MSE & KBD).

Both interfaces utilize open-drain signalling with on-board pull-up.

The PS/2 mouse and keyboard is supplied from SB5V when in standby mode in order to enable keyboard or mouse activity to bring the system out from power saving states. The supply is provided through a 1.1A resettable fuse.

#### 3.3.1 MINI-DIN Keyboard and Mouse Connector (KBD)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	-	NC	6	MSCLK	IOC	TBD	2K7	
	-	-	PWR	5V/SB5V	4	GND	PWR	-	-	
	-	-	-	NC	2	MSDAT	IOC	TBD	2K7	
	-	-	-	NC	6	KBDCLK	IOC	TBD	2K7	
	-	-	PWR	5V/SB5V	4	GND	PWR	-	-	
	-	-	-	NC	2	KBDDAT	IOC	TBD	2K7	

Signal Description – Keyboard & and mouse Connector (MSE & KBD), see below.

#### 3.3.2 Keyboard and Mouse pinrow Connector (KBDMSE)

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	KBDCLK	IOC	TBD	2K7	
2	KBDDAT	IOC	TBD	2K7	
3	MSCLK	IOC	TBD	2K7	
4	MSDAT	IOC	TBD	2K7	
5	5V/SB5V	PWR	-	-	
6	GND	PWR	-	-	

Signal Description – Keyboard & and mouse Connector (KBDMSE).

Signal	Description
MSCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MSDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.
KDBCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
KBDDAT	Bi-directional serial data line used to transfer data from or commands to the PC-AT keyboard.

### 3.4 Display connector

The KTQ45 board family provides onboard Analogue CRT interface. Additionally the KTQ45 boards provides support for ADD2 cards through the onboard PCI Express x16 connector, with extension capability for support of DVI, LVDS, VGA, HDMI/UDI, TV-Out, etc.

If a PCI Express x16 Graphics add-in card is used, the onboard Graphics controller (GMA 4500) is disabled.

#### 3.4.1 CRT Connector (CRT)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
					6	GND	PWR	-	-	
	/75R	*	A0	RED	1	11	NC	-	-	
					7	GND	PWR	-	-	
	/75R	*	A0	GREEN	2	12	DDCDAT	IO	TBD	2K2
					8	GND	PWR	-	-	
	/75R	*	A0	BLUE	3	13	HSYNC	O	TBD	
					9	5V	PWR	-	-	1
	-	-	-	NC	4	14	VSYNC	O	TBD	
					10	GND	PWR	-	-	
	-	-	PWR	GND	5	15	DDCCLK	IO	TBD	2K2

Signal Description - CRT Connector:

Pin	Signal	Description
1	RED	Analogue output carrying the red colour signal to the CRT. For 75 Ohm cable impedance.
2	GREEN	Analogue output carrying the green colour signal to the CRT. For 75 Ohm cable impedance.
3	BLUE	Analogue output carrying the blue colour signal to the CRT. For 75 Ohm cable impedance.
4	NC	No Connection
5-8	GND	
9	5V	This 5V supply is fused by a 1.1A resettable fuse.
10	GND	
11	NC	No Connection
12	DDCDAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
13	HSYNC	CRT horizontal synchronization output.
14	VSYNC	CRT vertical synchronization output.
15	DDCCLK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.

### 3.5 PCI-Express connectors

The KTQ45 board supports one 16-lane (x16) PCI Express port and one 4-lane PCI Express (x16) port.

**The 16-lane (x16) PCI Express 2.0** port can be used for external PCI Express graphics card. It is located nearest the CPU.

Supports PCI Express GEN1 frequency of 1.25 GHz (supports 2.5 Gbit/s in each direction, 500 MB/s totally). Maximum theoretical bandwidth using 16 lanes is 8 GB/s.

Supports PCI Express GEN2 frequency of 2.5 GHz (supports 5.0 Gbit/s in each direction, 1000 MB/s totally). Maximum theoretical bandwidth using 16 lanes is 16 GB/s.

The PCI Express (x16) interface is multiplexed with the SDVO ports.

**The 4-lane (x4) PCI Express 1.1** port is mechanically a x16 port and electrically a x4 port. It is located farthest away from CPU.

#### 3.5.1 PCI-Express x16/SDVO Connector (PCIe x16/SDVO)

Note	Type	Signal	PIN	Signal	Type	Note
		+12V	B1 A1	NC		
		+12V	B2 A2	+12V		
		+12V	B3 A3	+12V		
		GND	B4 A4	GND		
		SMB_CLK	B5 A5	NC		
		SMB_DATA	B6 A6	NC		
		GND	B7 A7	NC		
		+3V3	B8 A8	NC		
		NC	B9 A9	+3V3		
		SB3V3	B10 A10	+3V3		
		WAKE#	B11 A11	RST#		
		NC	B12 A12	GND		
		GND	B13 A13	PCIE_x16 CLK		
		PEG_TXP[15]/SDVOB_RED	B14 A14	PCIE_x16 CLK#		
		PEG_TXN[15]/SDVOB_RED#	B15 A15	GND		
		GND	B16 A16	PEG_RXP[15]/SDVO_TVCLKIN		
		SDVO_CTRLCLK	B17 A17	PEG_RXN[15] / SDVO_TVCLKIN#		
		GND	B18 A18	GND		
		PEG_TXP[14]/SDVOB_GREEN	B19 A19	NC		
		PEG_TXN[14]/SDVOB_GREEN#	B20 A20	GND		
		GND	B21 A21	PEG_RXP[14]/SDVOB_INT		
		GND	B22 A22	PEG_RXN[14]/SDVOB_INT#		
		PEG_TXP[13]/SDVOB_BLUE	B23 A23	GND		
		PEG_TXN[13]/SDVOB_BLUE#	B24 A24	GND		
		GND	B25 A25	PEG_RXP[13]/SDVO_FLDSTALL		
		GND	B26 A26	PEG_RXN[13]/SDVO_FLDSTALL#		
		PEG_TXP[12]/SDVOB_CLKP	B27 A27	GND		
		PEG_TXN[12]/SDVOB_CLKN	B28 A28	GND		
		GND	B29 A29	PEG_RXP[12]		
		NC	B30 A30	PEG_RXN[12]		
		SDVO_CTRLDATA	B31 A31	GND		
		GND	B32 A32	NC		
		PEG_TXP[11]/SDVOC_RED	B33 A33	NC		
		PEG_TXN[11]/SDVOC_RED#	B34 A34	GND		
		GND	B35 A35	PEG_RXP[11]		
		GND	B36 A36	PEG_RXN[11]		
		PEG_TXP[10]/SDVOC_GREEN	B37 A37	GND		
		PEG_TXN[10]/SDVOC_GREEN#	B38 A38	GND		
		GND	B39 A39	PEG_RXP[10]/SDVOC_INT		
		GND	B40 A40	PEG_RXN[10]/SDVOC_INT#		
		PEG_TXP[9]/SDVOC_BLUE	B41 A41	GND		
		PEG_TXN[9]/SDVOC_BLUE#	B42 A42	GND		
		GND	B43 A43	PEG_RXP[9]		
		GND	B44 A44	PEG_RXN[9]		
		PEG_TXP[8]/SDVOC_CLKN	B45 A45	GND		

	PEG_TXN[8]/SDVOC_CLKP	B46	A46	GND		
	GND	B47	A47	PEG_RXP[8]		
	PRSNT#2	B48	A48	PEG_RXN[8]		
	GND	B49	A49	GND		
	PEG_TXP[7]	B50	A50	NC		
	PEG_TXN[7]	B51	A51	GND		
	GND	B52	A52	PEG_RXP[7]		
	GND	B53	A53	PEG_RXN[7]		
	PEG_TXP[6]	B54	A54	GND		
	PEG_TXN[6]	B55	A55	GND		
	GND	B56	A56	PEG_RXP[6]		
	GND	B57	A57	PEG_RXN[6]		
	PEG_TXP[5]	B58	A58	GND		
	PEG_TXN[5]	B59	A59	GND		
	GND	B60	A60	PEG_RXP[5]		
	GND	B61	A61	PEG_RXN[5]		
	PEG_TXP[4]	B62	A62	GND		
	PEG_TXN[4]	B63	A63	GND		
	GND	B64	A64	PEG_RXP[4]		
	GND	B65	A65	PEG_RXN[4]		
	PEG_TXP[3]	B66	A66	GND		
	PEG_TXN[3]	B67	A67	GND		
	GND	B68	A68	PEG_RXP[3]		
	GND	B69	A69	PEG_RXN[3]		
	PEG_TXP[2]	B70	A70	GND		
	PEG_TXN[2]	B71	A71	GND		
	GND	B72	A72	PEG_RXP[2]		
	GND	B73	A73	PEG_RXN[2]		
	PEG_TXP[1]	B74	A74	GND		
	PEG_TXN[1]	B75	A75	GND		
	GND	B76	A76	PEG_RXP[1]		
	GND	B77	A77	PEG_RXN[1]		
	PEG_TXP[0]	B78	A78	GND		
	PEG_TXN[0]	B79	A79	GND		
	GND	B80	A80	PEG_RXP[0]		
	NC	B81	A81	PEG_RXN[0]		
	NC	B82	A82	GND		

### 3.5.2 PCI-Express x4 Connector (PCIe x4)

Note	Type	Signal	PIN	Signal	Type	Note
		+12V	B1 A1	NC		
		+12V	B2 A2	+12V		
		+12V	B3 A3	+12V		
		GND	B4 A4	GND		
		SMB_CLK	B5 A5	NC		
		SMB_DATA	B6 A6	NC		
		GND	B7 A7	NC		
		+3V3	B8 A8	NC		
		NC	B9 A9	+3V3		
		SB3V3	B10 A10	+3V3		
		WAKE#	B11 A11	RST#		
		NC	B12 A12	GND		
		GND	B13 A13	PCIe_x4 CLK		
		PCIe_TXP[1]	B14 A14	PCIe_x4 CLK#		
		PCIe_TXN[1]	B15 A15	GND		
		GND	B16 A16	PCIe_RXP[1]		
		NC	B17 A17	PCIe_RXN[1]		
		GND	B18 A18	GND		
		PCIe_TXP[2]	B19 A19	NC		
		PCIe_TXN[2]	B20 A20	GND		
		GND	B21 A21	PCIe_RXP[2]		
		GND	B22 A22	PCIe_RXN[2]		
		PCIe_TXP[3]	B23 A23	GND		
		PCIe_TXN[3]	B24 A24	GND		
		GND	B25 A25	PCIe_RXP[3]		
		GND	B26 A26	PCIe_RXN[3]		
		PCIe_TXP[4]	B27 A27	GND		
		PCIe_TXN[4]	B28 A28	GND		

	GND	B29	A29	PCIE_RXP[4]		
	NC	B30	A30	PCIE_RXN[4]		
	NC	B31	A31	GND		
	GND	B32	A32	NC		
	NC	B33	A33	NC		
	NC	B34	A34	GND		
	GND	B35	A35	NC		
	GND	B36	A36	NC		
	NC	B37	A37	GND		
	NC	B38	A38	GND		
	GND	B39	A39	NC		
	GND	B40	A40	NC		
	NC	B41	A41	GND		
	NC	B42	A42	GND		
	GND	B43	A43	NC		
	GND	B44	A44	NC		
	NC	B45	A45	GND		
	NC	B46	A46	GND		
	GND	B47	A47	NC		
	NC	B48	A48	NC		
	GND	B49	A49	GND		
	NC	B50	A50	NC		
	NC	B51	A51	GND		
	GND	B52	A52	NC		
	GND	B53	A53	NC		
	NC	B54	A54	GND		
	NC	B55	A55	GND		
	GND	B56	A56	NC		
	GND	B57	A57	NC		
	NC	B58	A58	GND		
	NC	B59	A59	GND		
	GND	B60	A60	NC		
	GND	B61	A61	NC		
	NC	B62	A62	GND		
	NC	B63	A63	GND		
	GND	B64	A64	NC		
	GND	B65	A65	NC		
	NC	B66	A66	GND		
	NC	B67	A67	GND		
	GND	B68	A68	NC		
	GND	B69	A69	NC		
	NC	B70	A70	GND		
	NC	B71	A71	GND		
	GND	B72	A72	NC		
	GND	B73	A73	NC		
	NC	B74	A74	GND		
	NC	B75	A75	GND		
	GND	B76	A76	NC		
	GND	B77	A77	NC		
	NC	B78	A78	GND		
	NC	B79	A79	GND		
	GND	B80	A80	NC		
	NC	B81	A81	NC		
	NC	B82	A82	GND		

### 3.6 Serial ATA Hard Disk interface

The KTQ45 boards have an integrated SATA Host controller that supports independent DMA operation on six ports and data transfer rates of up to 3.0Gb/s (300MB/s). The SATA controller supports AHCI mode and has integrated RAID functionality with support for RAID modes 0, 1, 5 and 10 (Linux O/S only support for RAID 0 and 1).

The board provides five Serial ATA (SATA) connectors which support one device per connector. The ICH10DO Serial ATA controller offers six independent Serial ATA ports with a theoretical maximum transfer rate of 3 Gbit/sec per port. One device can be installed on each port for a maximum of six Serial ATA devices. A point-to-point interface is used for host to device connections, unlike Parallel ATA IDE which supports a master/slave configuration and two devices per channel.

For compatibility, the underlying Serial ATA functionality is transparent to the operating system. The Serial ATA controller can operate in both legacy and native modes. In legacy mode, standard IDE I/O and IRQ resources are assigned (IRQ 14 and 15). In Native mode, standard PCI Conventional bus resource steering is used. Native mode is the preferred mode for configurations using the Windows XP and Windows Vista operating systems.

The KTQ45 supports the following RAID (Redundant Array of Independent Drives) levels:

- RAID 0 - data striping
- RAID 1 - data mirroring
- RAID 0+1 (or RAID 10) - data striping and mirroring
- RAID 5 - distributed parity

Limitations depending on Target Operating System apply.

**Note:** On the KTQ45 there is no parallel ATA or CF interface, but on the market it's possible to find different SATA converters to support CF etc.

In case CF card shall be used as hot plug device then it is recommended to use USB to CF adapter. (SATA to CF adapter doesn't support hot plug).

#### 3.6.1 SATA Hard Disk Connector (SATA1, SATA2, SATA3, SATA4, SATA5)

**SATA:**

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	GND	PWR	-	-	
2	SATA* TX+				
3	SATA* TX-				
4	GND	PWR	-	-	
5	SATA* RX-				
6	SATA* RX+				
7	GND	PWR	-	-	

The signals used for the primary Serial ATA hard disk interface are the following:

Signal	Description
SATA* RX+ SATA* RX-	Host transmitter differential signal pair
SATA* TX+ SATA* TX-	Host receiver differential signal pair

“\*” specifies 1, 2, 3, 4, 5 depending on SATA port.

### 3.7 Printer Port Connector (LPT)

The signal definition in standard printer port mode is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
	2K2	(24)/24	OC(O)	STB#	1 2	AFD#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD0	3 4	ERR#	I	-	2K2	
	2K2	24/24	IO	PD1	5 6	INIT#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD2	7 8	SLIN#	OC(O)	(24)/24	2K2	
	2K2	24/24	IO	PD3	9 10	GND	PWR	-	-	
	2K2	24/24	IO	PD4	11 12	GND	PWR	-	-	
	2K2	24/24	IO	PD5	13 14	GND	PWR	-	-	
	2K2	24/24	IO	PD6	15 16	GND	PWR	-	-	
	2K2	24/24	IO	PD7	17 18	GND	PWR	-	-	
	2K2	-	I	ACK#	19 20	GND	PWR	-	-	
	2K2	-	I	BUSY	21 22	GND	PWR	-	-	
	2K2	-	I	PE	23 24	GND	PWR	-	-	
	2K2	-	I	SLCT	25 26	GND	PWR	-	-	

The definition of the signals in standard Centronics mode (SPP) with a printer attached is as follows:

Signal	Description
PD7..0	Parallel data bus from PC board to printer. The data lines are able to operate in PS/2 compatible bi-directional mode.
SLIN#	Signal to select the printer sent from CPU board to printer.
SLCT	Signal from printer to indicate that the printer is selected.
STB#	This signal indicates to the printer that data at PD7..0 are valid.
BUSY	Signal from printer indicating that the printer cannot accept further data.
ACK#	Signal from printer indicating that the printer has received the data and is ready to accept further data.
INIT#	This active low output initializes (resets) the printer.
AFD#	This active low output causes the printer to add a line feed after each line printed.
ERR#	Signal from printer indicating that an error has been detected.
PE#	Signal from printer indicating that the printer is out of paper.

The printer port additionally supports operation in the EPP and ECP mode.

## 3.8 Serial Ports

Two RS232 serial ports are available on the KTQ45/Flex.

Three RS232 serial ports and one RS485 port are available on the KTQ45/ATXE.

The typical definition of the signals in the COM ports is as follows:

Signal	Description
TxD	Transmitted Data, sends serial data to the communications link. The signal is set to the marking state (-12V) on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Received Data, receives serial data from the communications link.
DTR	Data Terminal Ready, indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready, indicates that the modem or data set is ready to establish a communications link.
RTS	Request To Send, indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send, indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator, indicates that the modem has received a ringing signal from the telephone line.

The connector pinout for each operation mode is defined in the following sections.

### 3.8.1 COM1 Connectors

COM1 is RS232 port available in the IO Bracket area. The pinout of Serial ports Com1 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND	5					
					9	RI	I	-	/5K	
	-		O	DTR	4					
					8	CTS	I	-	/5K	
	-		O	TxD	3					
					7	RTS	O	-		
	/5K	-	I	RxD	2					
					6	DSR	I	-	/5K	
	/5K	-	I	DCD	1					

### 3.8.2 COM2 and COM3 Header Connectors

COM3 is only available on the KTQ45/ATXE.

The pinout of Serial ports COM2 and COM3 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
		-	I	DCD	1 2	DSR	I	-		
		-	I	RxD	3 4	RTS	O		-	
	-		O	TxD	5 6	CTS	I	-		
	-		O	DTR	7 8	RI	I	-		
	-	-	PWR	GND	9 10	5V	PWR	-	-	1

**Note 1:** The COM2 and COM3 5V supply is fused with individual 1.1A resettable fuses for each connector.

A DB9 adapter (ribbon cable) is available for connecting the COM ports to I/O front panel.

### 3.8.3 COM4 Header Connectors

COM4 is RS485 (galvanic isolated). COM4 is only available on the KTQ45/ATXE.

The pinout of Serial ports COM4 is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
3,5		-	I	RxD+	1 2	5V_iso	PWR	-	-	1
2,3,5		-	I	RxD -	3 4	5V_iso	PWR	-	-	
2,4,5	-		O	TxD-	5 6	GND_iso	PWR	-	-	
4,5	-		O	TxD+	7 8	GND_iso	PWR	-	-	
	-	-	PWR	GND_iso	9 10	GND_iso	PWR	-	-	

**Note 1:** The COM4 header 5V\_iso supply is fused with a 1.1A resettable fuse. The power source connected to this net is delivered by internally galvanic isolated PSU used to power onboard RS485 driver. The maximum allowed current to drawn on this net must not exceed 50mA if used.

**Warning:** Do not attempt to connect external power source to this net any attempt might damage the board.

**Note 2:** RTS signal control the output drivers.

**Note 3:** 120R termination resistor between signal RxD+ and RxD- is connected on the board.

**Note 4:** 120R termination resistor between signal TxD+ and TxD- is connected on the board.

**Note 5:** RxD and TxD pairs can be connected to each other for 2 wire / Half-Duplex transmission line. This can be configured on the board by adding Jumper JP7 and JP9. The transmitter termination resistor can be disabled by removing Jumper JP8.

If using Kontron PN 821016 or PN 821017 as DB9 adapter (ribbon cable) then the pinout is as follows:

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	GND_iso	5					
					9	GND_iso	PWR	-	-	
	-	-	O	TxD+	4					
					8	GND_iso	PWR	-	-	
	-	-	O	TxD-	3					
					7	5V_iso	PWR	-	-	
	-	-	I	RxD -	2					
					6	5V_iso	PWR	-	-	
	-	-	I	RxD+	1					

### 3.9 Ethernet Connectors

The KTQ45 boards supports 2 channels of 10/100/1000Mb Ethernet one based on Intel® Boazman-LM WG82567LM Gigabit PHY with AMT 5.0 support (ETHER1) and the other based on Intel® Hartwell 82574L PCI Express controller (ETHER2).

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100MB and Category 5E, 6 or 6E with 1Gb LAN networks.

The signals for the Ethernet ports are as follows:

Signal	Description
MDI[0]+ / MDI[0]-	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDI[1]+ / MDI[1]-	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDI[2]+ / MDI[2]-	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDI[3]+ / MDI[3]-	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.

**Note:** MDI = Media Dependent Interface.

#### 3.9.1 Ethernet Connectors 1 and 2 (ETHER1 and ETHER2)

Ethernet connector 1 (positioned to the right) is mounted together with USB Ports 4 and 5.

Ethernet connector 2 (positioned to the left) is mounted together with USB Ports 2 and 3.

The pinout of the RJ45 connector is as follows:

Signal	PIN	Type	Ioh/Iol	Note
MDI0+	1			
MDI0-	2			
MDI1+	3			
MDI2+	4			
MDI2-	5			
MDI1-	6			
MDI3+	7			
MDI3-	8			

**Note:** Do not use PCB silkscreen to identify the position of ETHER1/ETHER2. Silkscreen might indicate LAN1 and LAN2 in opposite order.

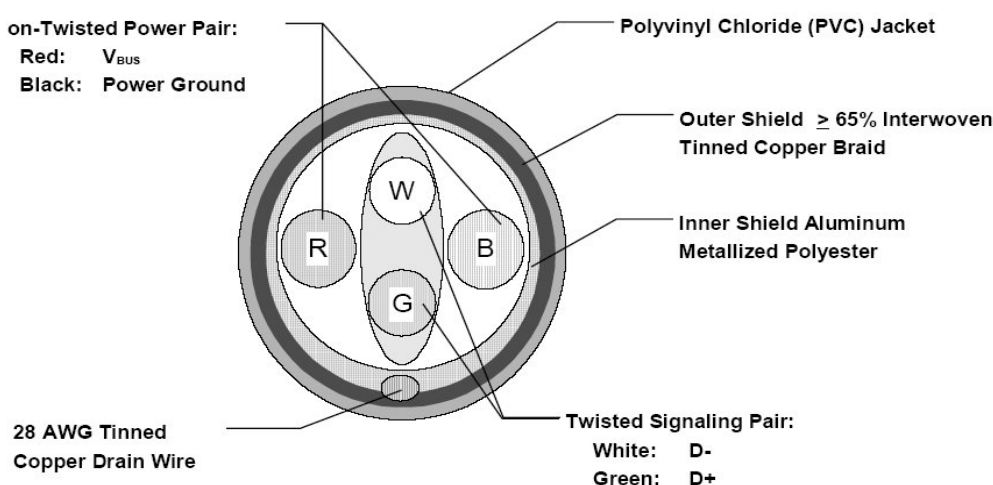
### 3.10 USB Connectors (USB)

The KTQ45 board contains two Enhanced Host Controller Interface (EHCI) host controllers that support USB 2.0 allowing data transfers up to 480Mb/s. The KTQ45 boards also contains Six Universal Host Controller Interface (UHCI Revision 1.1) controllers that support USB full-speed and low-speed signalling. The KTQ45 board supports a total of twelve USB 2.0 ports. All twelve ports are high-speed, full-speed, and low-speed capable and USB Legacy mode is supported.

Over-current detection on all twelve USB ports is supported.

USB Port 2 and 3 are supplied on the combined ETHER2, USB2, and USB3 connector.  
 USB Port 4 and 5 are supplied on the combined ETHER1, USB4, and USB5 connector.  
 USB Port 0, 1, 6 and 7 are supplied on the combined USB0, USB1, USB6, USB7 connector.  
 USB Port 8 and 9 are supplied on the USB8 USB9 on the internal USBC1 connector.  
 USB Ports 10 and 11 are supplied on the internal FRONTPNL connector; please refer to the FRONTPNL connector section for the pin-out.

**Note:** It is required to use only HiSpeed USB cable, specified in USB2.0 standard:



#### 3.10.1 USB Connector 2/3 (USB2/3)

USB Ports 2 and 3 are mounted together with ETHER2 Ethernet port.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	-	-	PWR	5V/SB5V	1 2 3 4	GND	PWR	-	-	
	/15K	0.25/2	IO	USB3-		USB3+	IO	0.25/2	/15K	
1	-	-	PWR	5V/SB5V	1 2 3 4	GND	PWR	-	-	
	/15K	0.25/2	IO	USB2-		USB2+	IO	0.25/2	/15K	

**Note 1:** In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB2+ USB2- USB3+ USB3-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external devices. SB5V is supplied during power down to allow wakeup on USB device activity. Protected by resettable 1.1A fuse covering both USB ports.

### 3.10.2 USB Connector 4/5 (USB4/5)

USB Ports 4 and 5 are mounted together with ETHER1 Ethernet port.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	-	-	PWR	5V/SB5V	1 2 3 4	GND	PWR	-	-	
	/15K	0.25/2	IO	USB5-		USB5+	IO	0.25/2	/15K	
1	-	-	PWR	5V/SB5V	1 2 3 4	GND	PWR	-	-	
	/15K	0.25/2	IO	USB4-		USB4+	IO	0.25/2	/15K	

**Note 1:** In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB4+ USB4- USB5+ USB5-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external devices. SB5V is supplied during power down to allow wakeup on USB device activity. Protected by resettable 1.1A fuse covering both USB ports.

### 3.10.3 USB Connector 0/1/6/7 (USB0/1/6/7)

USB Ports 0, 1, 6 and 7 are available on the combined USB0, USB1, USB6, USB7 connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	-	-	PWR	5V/SB5V	1 2 3 4	GND	PWR	-	-	
	/15K	0.25/2	IO	USB0-		USB0+	IO	0.25/2	/15K	
1	-	-	PWR	5V/SB5V	1 2 3 4	GND	PWR	-	-	
	/15K	0.25/2	IO	USB1-		USB1+	IO	0.25/2	/15K	
1	-	-	PWR	5V/SB5V	1 2 3 4	GND	PWR	-	-	
	/15K	0.25/2	IO	USB6-		USB6+	IO	0.25/2	/15K	
1	-	-	PWR	5V/SB5V	1 2 3 4	GND	PWR	-	-	
	/15K	0.25/2	IO	USB7-		USB7+	IO	0.25/2	/15K	

**Note 1:** In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB0+ USB0- USB1+ USB1- USB6+ USB6- USB7+ USB7-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Protected by resettable 1.1A fuses, one covering USB0 and USB1, and another covering USB6 and USB7.

### 3.10.4 USB Connector 8/9 (USB8/9)

USB Ports 8 and 9 are supplied on the internal USBC1 pinrow connector.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1		-	PWR	5V/SB5V	1 2	5V/SB5V	PWR	-		1
		-	IO	USB8-	3 4	USB9-	IO		-	
	-		IO	USB8+	5 6	USB9+	IO	-		
	-		PWR	GND	7 8	GND	PWR	-		
	-	-		KEY	9 10	NC		-	-	

**Note 1:** In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

Signal	Description
USB8+ USB8- USB9+ USB9-	Differential pair works as Data/Address/Command Bus.
5V/SB5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Protected by resettable 1.1A fuse covering both USB ports.

### 3.10.5 USB Connector 10/11 (USB10/11)

See Frontpanel Connector (FRONTPNL) description.

### 3.11 Audio Connectors

The onboard Audio circuit implements 7.1+2 Channel High Definition Audio with UAA (Universal Audio Architecture), featuring five 24-bit stereo DACs and three 20-bit stereo ADCs.

#### 3.11.1 Audio Speakers, Line-In, Line-Out and Microphone

Audio Speakers, Line-in, Line-out and Microphone are available in the stacked audio jack connector. Below is shown audio stack configuration when configured for 8-channel audio.

Note	Type	Signal			Signal	Type	Note
	OA	CEN-OUT	TIP RING SLEEVE	TIP RING SLEEVE	LINE1-IN-L	IA	
	OA	LFE-OUT			LINE1-IN-R	IA	
	PWR	GND			GND	PWR	
	OA	REAR-OUT-L	TIP RING SLEEVE	TIP RING SLEEVE	FRONT-OUT-L	OA	
	OA	REAR-OUT-R			FRONT-OUT-R	OA	
	PWR	GND			GND	PWR	
	OA	SIDE-OUT-L	TIP RING SLEEVE	TIP RING SLEEVE	MIC1-L	IA	
	OA	SIDE-OUT-R			MIC1-R	IA	
	PWR	GND			GND	PWR	

Signal	Description	Note
FRONT-OUT-L	Front Speakers (Speaker Out Left).	
FRONT-OUT-R	Front Speakers (Speaker Out Right).	
REAR-OUT-L	Rear Speakers (Surround Out Left).	
REAR-OUT-R	Rear Speakers (Surround Out Right).	
SIDE-OUT-L	Side speakers (Surround Out Left)	
SIDE-OUT-R	Side speakers (Surround Out Right)	
CEN-OUT	Center Speaker (Center Out channel).	
LFE-OUT	Subwoofer Speaker (Low Freq. Effect Out).	
MIC1	MIC Input 1	
LINE1-IN	Line in 1 signals	

Port	2-channel	4-channel	6-channel	8-channel
Light Blue	Line in	Line in	Line in	Line in
Lime	Line out	Front speaker out	Front speaker out	Front speaker out
Pink	Mic in	Mic in	Mic in	Mic in
Audio header	-	-	-	Side speaker out
Audio header	-	Rear speaker out	Rear speaker out	Rear speaker out
Audio header	-	-	Center/ Subwoofer	Center/ Subwoofer

### 3.11.2 CDROM Audio Input (CDROM)

CD-ROM audio input may be connected to this connector. It may also be used as a secondary line-in signal.

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	CD_Left	IA	-	-	1
2	CD_GND	IA	-	-	
3	CD_GND	IA	-	-	
4	CD_Right	IA	-	-	1

**Note 1:** The definition of which pins are use for the Left and Right channels is not a worldwide accepted standard. Some CDROM cable kits expect reverse pin order.

Signal	Description
CD_Left CD_Right	Left and right CD audio input lines or secondary Line-in.
CD_GND	Analogue GND for Left and Right CD. (This analogue GND is <b>not</b> shorted to the general digital GND on the board).

### 3.11.3 Audio Header (AUDIO\_HEAD)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
				LFE-OUT	1 2	CEN-OUT				
				AAGND	3 4	AAGND				
				FRONT-OUT-L	5 6	FRONT-OUT-R				
				AAGND	7 8	AAGND				
				REAR-OUT-L	9 10	REAR-OUT-R				
				SIDE-OUT-L	11 12	SIDE-OUT-R				
				AAGND	13 14	AAGND				
				MIC1-L	15 16	MIC1-R				
				AAGND	17 18	AAGND				
				LINE1-IN-L	19 20	LINE1-IN-R				
				NC	21 22	AAGND				
	-	-	PWR	GND	23 24	SPDIF-IN				
				SPDIF-OUT	25 26	GND	PWR	-	-	

Signal	Description	Note
FRONT-OUT-L	Front Speakers (Speaker Out Left).	
FRONT-OUT-R	Front Speakers (Speaker Out Right).	
REAR-OUT-L	Rear Speakers (Surround Out Left).	
REAR-OUT-R	Rear Speakers (Surround Out Right).	
SIDE-OUT-L	Side speakers (Surround Out Left)	
SIDE-OUT-R	Side speakers (Surround Out Right)	
CEN-OUT	Center Speaker (Center Out channel).	
LFE-OUT	Subwoofer Speaker (Low Freq. Effect Out).	
NC	No connection	
MIC1	MIC Input 1	
LINE1-IN	Line in 1 signals	
F-SPDIF-IN	S/PDIF Input	
F-SPDIF-OUT	S/PDIF Output	
AAGND	Audio Analogue ground	

### 3.12 Fan Connector (FAN\_CPU)

The **FAN\_CPU** is used for the connection of the FAN for the CPU.

The **FAN\_SYS** can be used to power, control and monitor a fan for chassis ventilation etc.

The 4pin header supports connection of 3-pin FAN, but it is recommended to use the 4-pin type for optimized FAN speed control. The 3- or 4-pin mode is set in the BIOS setup menu.

#### 4-pin Mode:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
1	CONTROL	O	-	-	
2	SENSE	I	-	4K7	
3	+12V	PWR	-	-	
4	GND	PWR	-	-	

Signal	Description
CONTROL	PWM signal for FAN speed control
SENSE	Tacho signal from the fan for supervision. The signals shall be generated by an open collector transistor or similar. Onboard is a pull-up resistor 4K7 to +12V. The signal has to be pulsed, typically twice per rotation.
12V	+12V supply for fan. A maximum of 2000mA can be supplied from this pin.
GND	Power Supply GND signal

#### 3-pin Mode:

PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
-					
2	SENSE	I	-	4K7	
3	+12V	PWR	-	-	
4	GND	PWR	-	-	

Signal	Description
SENSE	Tacho signal from the fan for supervision. The signals shall be generated by an open collector transistor or similar. Onboard is a pull-up resistor 4K7 to +12V. The signal has to be pulsed, typically twice per rotation.
12V	+12V supply for fan, can be turned on/off or modulated (PWM) by the chipset. A maximum of 2000mA can be supplied from this pin.
GND	Power Supply GND signal

### 3.13 Clear CMOS Jumper (Clr-CMOS /JBAT1)

The Clr-CMOS Jumper is used to clear the CMOS content.

Jumper in Clear CMOS position  (only for 1 minute)

Jumper normal position  <-- pin 1

SATA1 connector

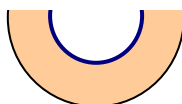
To clear all CMOS settings, including Password protection, move the Clr-CMOS jumper to pin 2-3 for 1 minute (Works with or without power connected to the system).

**WARNING:** Don't leave the jumper in Clear CMOS position, otherwise without power connected to the system the battery will fully depleted within a few weeks.

### 3.14 The Clear ME register Jumper (Clr-ME / JBAT2)

The Clr-ME Jumper (named JBAT2) is used to clear the manageability register. To clear the register both JBAT1 and JBAT2 should be in position 2&3 at the same time.

(Mounting hole in front of SATA connectors)



Jumper in normal position  <-- pin 1


Jumper in Clear ME Registers  (only for 1 minute)

**WARNING:** Don't leave the jumper in Clear CMOS position, otherwise without power connected to the system the battery will fully depleted within a few weeks.

### 3.15 The SPI Jumper (SPI-Jumper / JP6)

The SPI selection jumper is used to switch between onboard SPI and external SPI device.

**Note:** The SPI device holds the BIOS contents and should not be removed from its default position unless a pre-programmed SPI device is connected to the SPI1 connector.

Jumper in normal position  <-- pin 1

Jumper in Clear ME Registers 

(PCIe x16 / SDVO connectors)

### 3.16 Interface BIOS Jumpers (JP3 and JP5))

The Interface BIOS jumper (JP3 and JP5) are not to be removed from their default position, doing so will make the board non bootable. These jumpers are for manufacture purpose only.

JP3 shall be in position 1-2 (against PCI connectors)

JP5 shall be in position 1-2 (against SATA connectors)

### 3.17 TPM Connector (TPM)

This connector is unsupported.

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
	-	-	PWR	LPC CLK	1 2	GND				
	-	-	PWR	LPC FRAME#	3	KEY				
				LPC RST#	5 6	+5V				
				LPC AD3	7 8	LPC AD2				
				+3V3	9 10	LPC AD1				
				LPC AD0	11 12	GND				
				SMB_CLK	13 14	SMB_DATA				
				SB3V3	15 16	LPC SERIRQ				
				GND	17 18	CLKRUN#				
				SUS_STAT#	19 20	NC				

### 3.18 SPI Connector (SPI)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
				SPI_CLK	1 2	SB3V3	PWR	-	-	
	-	-	-	NC	3 4	BOOT0	IO		-	
	10K/			SPI_CS2#	5 6	BOOT1	IO	-		
	10K/			SPI_MOSI	7 8	MFG		-		
	10K/			SPI_MISO	9 10	GND	PWR	-	-	

### 3.19 Front Panel Connector (FRONTPNL)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
				USB10/11_5V	1 2	USB10/11_5V				
				USB1-	3 4	USB3-				
				USB1+	5 6	USB3+				
	-	-	PWR	GND	7 8	GND	PWR	-	-	
	-	-	-	NC	9 10	LINE2-IN-L	-	-	-	
	-	-	PWR	+5V	11 12	+5V	PWR	-	-	
			OC	HD_LED	13 14	SUS_LED				
	-	-	PWR	GND	15 16	PWRBTN_IN#				
				RSTIN#	17 18	GND	PWR	-	-	
				SB3V3	19 20	LINE2-IN-R	-	-	-	
				AGND	21 22	AGND				
				MIC2-L	23 24	MIC2-R				

Signal	Description
USB10/11_5V	5V supply for external devices. SB5V is supplied during powerdown to allow wakeup on USB device activity. Protected by resettable 1.1A fuse covering both USB ports.
USB1+ USB1-	Universal Serial Bus Port 1 Differentials: Bus Data/Address/Command Bus.
USB3+ USB3-	Universal Serial Bus Port 3 Differentials: Bus Data/Address/Command Bus.
+5V	Maximum load is 1A or 2A per pin if using IDC connector flat cable or crimp terminals respectively.
HD_LED	Hard Disk Activity LED (active low signal). Output is via 475Ω to OC.
SUS_LED	Suspend Mode LED (active high signal). Output is via 475Ω.
PWRBTN_IN#	Power Button In. Toggle this signal low to start the ATX / BTX PSU and boot the board.
RSTIN#	Reset Input. When pulled low for a minimum 16ms, the reset process will be initiated. The reset process continues even though the Reset Input is kept low.
LINE2-IN	Line in 2 signals
MIC2	MIC2-L and MIC2-R is second stereo microphone input.
SB3V3	Standby 3.3V voltage
AGND	Analogue Ground for Audio

**Note 1:** In order to meet the requirements of USB standard, the 5V input supply must be at least 5.00V.

### 3.20 Feature Connector (FEATURE)

Note	Pull U/D	Ioh/Iol	Type	Signal	PIN	Signal	Type	Ioh/Iol	Pull U/D	Note
2	2M/	-	I	INTRUDER#	1 2	GND	PWR	-	-	
				EXT_ISAIRQ#	3 4	EXT_SMI#	I		4K7	3
				PWR_OK	5 6	SB5V	PWR	-	-	
	-	-	PWR	SB3V3	7 8	EXT_BAT	PWR	-	-	
	-	-	PWR	+5V	9 10	GND	PWR	-	-	
1	4K7/	/12mA	IOT	GPIO0	11 12	GPIO1	IOT	/12mA	4K7/	1
1	4K7/	/12mA	IOT	GPIO2	13 14	GPIO3	IOT	/12mA	4K7/	1
1	4K7/	/12mA	IOT	GPIO4	15 16	GPIO5	IOT	/12mA	4K7/	1
1	4K7/	/12mA	IOT	GPIO6	17 18	GPIO7	IOT	/12mA	4K7/	1
	-	-	PWR	GND	19 20	FAN3OUT	O		4K7	3
				FAN3IN	21 22	+12V	PWR	-	-	
				TEMP3IN	23 24	VREF				
	-	-	PWR	GND	25 26	IRRX				
				IRTX	27 28	GND	PWR	-	-	
1	4K7/			SMBC	29 30	SMBD			4K7/	1

#### Notes:

1. Pull-up to +3V3Dual (+3V3 or SB3V3).
2. Pull-up to onboard Battery.
3. Pull-up to +3V3.

Signal	Description
INTRUDER#	INTRUDER, may be used to detect if the system case has been opened. This signal's status is readable, so it may be used like a GPI when the Intruder switch is not required.
EXT_ISAIRQ#	EXTERNAL ISA IRQ, (active low input) can activate standard AT-Bus IRQ-interrupt.
EXT_SMI#	External SMI, (active low input) signal can activate SMI interrupt.
PWR_OK	PoWeR OK, signal is high if no power failures are detected.
SB5V	StandBy +5V supply.
SB3V3	Max. load is 0.75A (1.5A < 1 sec.)
EXT_BAT	(EXTERNAL BATTERY) option for connecting + terminal of an external primary cell battery (2.5 - 4.0 V) (- terminal connected to GND etc. pin 10). The external battery is protected against charging and can be used with or without the onboard battery installed.
+5V	Max. load is 0.75A (1.5A < 1 sec.)
GPIO0..7	General Purpose Inputs / Output. These Signals may be controlled or monitored through the use of the KT-API-V2 (Application Programming Interface).
FAN3OUT	FAN 3 speed control OUTPUT. This 3.3V PWM signal can be used as Fan control voltage (0-3.3V DC in 128 steps) via a Fan Driver Circuit (not included) to program Fan voltage. For more info, see W83627 datasheet. Default PMW output is 127 (100% = 3.3V).
FAN3IN	FAN3 Input. 0V to +3V3 amplitude Fan 3 tachometer input.
+12V	Max. load is 0.75A (1.5A < 1 sec.)
TEMP3IN	Temperature sensor 3 input. (Recommended: Transistor 2N3904, having emitter connected to GND (pin 25), collector and basis shorted and connected to pin 23. Further a resistor 30K/1% shall be connected between pin 23 - 24. (Precision +/- 3°C).
VREF	Voltage REFERENCE, reference voltage to be used with TEMP3IN input.
IRRX	IR Receive input (IrDA 1.0, SIR up to 1.152K bps)
IRTX	IR Transmit output (IrDA 1.0, SIR up to 1.152K bps)
SMBC	SMBus Clock signal
SMBD	SMBus Data signal

### 3.21 PCI Slot Connector (PCI Slot)

Note	Type	Signal	Terminal S	Terminal C	Signal	Type	Note	
	PWR	-12V	F01	E01	TRST#	O		
	O	TCK	F02	E02	+12V	PWR		
	PWR	GND	F03	E03	TMS	O		
	I	TDO	F04	E04	TDI	O		
	PWR	+5V	F05	E05	+5V	PWR		
	PWR	+5V	F06	E06	INTA#	I		
	I	INTB#	F07	E07	INTC#	I		
	I	INTD#	F08	E08	+5V	PWR		
	I	REQ2#	F09	E09	CLKC	O		
	I	REQ3#	F10	E10	+5V (I/O)	PWR		
	OT	GNT2#	F11	E11	CLKD	O		
	PWR	GND	F12	E12	GND	PWR		
	PWR	GND	F13	E13	GND	PWR		
	O	CLKA	F14	E14	GNT3#	OT		
	PWR	GND	F15	E15	RST#	O		
	O	CLKB	F16	E16	+5V (I/O)	PWR		
	PWR	GND	F17	E17	GNT0#	OT		
	I	REQ0#	F18	E18	GND	PWR		
	PWR	+5V (I/O)	F19	E19	REQ1#	I		
	IOT	AD31	F20	E20	AD30	IOT		
	IOT	AD29	F21	E21	+3.3V	PWR		
	PWR	GND	F22	E22	AD28	IOT		
	IOT	AD27	F23	E23	AD26	IOT		
	IOT	AD25	F24	E24	GND	PWR		
	PWR	+3.3V	F25	E25	AD24	IOT		
	IOT	C/BE3#	F26	E26	GNT1#	OT		
	IOT	AD23	F27	E27	+3.3V	PWR		
	PWR	GND	F28	E28	AD22	IOT		
	IOT	AD21	F29	E29	AD20	IOT		
	IOT	AD19	F30	E30	GND	PWR		
	PWR	+3.3V	F31	E31	AD18	IOT		
	IOT	AD17	F32	E32	AD16	IOT		
	IOT	C/BE2#	F33	E33	+3.3V	PWR		
	PWR	GND	F34	E34	FRAME#	IOT		
	IOT	IRDY#	F35	E35	GND	PWR		
	PWR	+3.3V	F36	E36	TRDY#	IOT		
	IOT	DEVSEL#	F37	E37	GND	PWR		
	PWR	GND	F38	E38	STOP#	IOT		
	IOT	LOCK#	F39	E39	+3.3V	PWR		
	IOT	PERR#	F40	E40	SDONE	IO		
	PWR	+3.3V	F41	E41	SB0#	IO		
	IOC	SERR#	F42	E42	GND	PWR		
	PWR	+3.3V	F43	E43	PAR	IOT		
	IOT	C/BE1#	F44	E44	AD15	IOT		
	IOT	AD14	F45	E45	+3.3V	PWR		
	PWR	GND	F46	E46	AD13	IOT		
	IOT	AD12	F47	E47	AD11	IOT		
	IOT	AD10	F48	E48	GND	PWR		
	PWR	GND	F49	E49	AD09	IOT		
<b>SOLDER SIDE</b>					<b>COMPONENT SIDE</b>			
	IOT	AD08	F52	E52	C/BE0#	IOT		
	IOT	AD07	F53	E53	+3.3V	PWR		
	PWR	+3.3V	F54	E54	AD06	IOT		
	IOT	AD05	F55	E55	AD04	IOT		
	IOT	AD03	F56	E56	GND	PWR		
	PWR	GND	F57	E57	AD02	IOT		
	IOT	AD01	F58	E58	AD00	IOT		
	PWR	+5V (I/O)	F59	E59	+5V (I/O)	PWR		
	IOT	ACK64#	F60	E60	REQ64#	IOT		
	PWR	+5V	F61	E61	+5V	PWR		
	PWR	+5V	F62	E62	+5V	PWR		

### 3.21.1 Signal Description – PCI Slot Connector

SYSTEM PINS	
CLK	Clock provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals, except RST#, INTA#, INTB#, INTC#, and INTD#, are sampled on the rising edge of CLK and all other timing parameters are defined with respect to this edge. PCI operates at 33MHz.
RST#	Reset is used to bring PCI-specific registers, sequencers, and signals to a consistent state. What effect RST# has on a device beyond the PCI sequencer is beyond the scope of this specification, except for reset states of required PCI configuration registers. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be asynchronously tri-stated. SERR# (open drain) is floated. REQ# and GNT# must both be tri-stated (they cannot be driven low or high during reset). To prevent AD, C/BE#, and PAR signals from floating during reset, the central resource may drive these lines during reset (bus parking) but only to a logic low level—they may not be driven high. RST# may be asynchronous to CLK when asserted or deasserted. Although asynchronous, deassertion is guaranteed to be a clean, bounce-free edge. Except for configuration accesses, only devices that are required to boot the system will respond after reset.
ADDRESS AND DATA	
AD[31::00]	Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the clock cycle in which FRAME# is asserted. During the address phase AD[31::00] contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory, it is a DWORD address. During data phases AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb). Write data is stable and valid when IRDY# is asserted and read data is stable and valid when TRDY# is asserted. Data is transferred during those clocks where both IRDY# and TRDY# are asserted.
C/BE[3::0]#	Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE[3::0]# define the bus command. During the data phase C/BE[3::0]# are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE[0]# applies to byte 0 (lsb) and C/BE[3]# applies to byte 3 (msb).
PAR	Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. (PAR has the same timing as AD[31::00], but it is delayed by one clock.) The master drives PAR for address and write data phases; the target drives PAR for read data phases.
INTERFACE CONTROL PINS	
FRAME#	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase or has completed.
IRDY#	Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD[31::00]. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
TRDY#	Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	Stop indicates the current target is requesting the master to stop the current transaction.
LOCK#	Lock indicates an atomic operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked. A grant to start a transaction on PCI does not guarantee control of LOCK#. Control of LOCK# is obtained under its own protocol in conjunction with GNT#. It is possible for different agents to use PCI while a single master retains ownership of LOCK#. If a device implements Executable Memory, it should also implement LOCK# and guarantee complete access exclusion in that memory. A target of an access that supports LOCK# must provide exclusion to a minimum of 16 bytes (aligned). Host bridges that have system memory behind them should implement LOCK# as a target from the PCI bus point of view and optionally as a master.
IDSEL	Initialization Device Select is used as a chip select during configuration read and write transactions.
DEVSEL#	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

(Continues)

ARBITRATION PINS (BUS MASTERS ONLY)	
REQ#	Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ# which must be tri-stated while RST# is asserted.
GNT#	Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT# which must be ignored while RST# is asserted. While RST# is asserted, the arbiter must ignore all REQ# lines since they are tri-stated and do not contain a valid request. The arbiter can only perform arbitration after RST# is deasserted. A master must ignore its GNT# while RST# is asserted. REQ# and GNT# are tri-state signals due to power sequencing requirements when 3.3V or 5.0V only add-in boards are used with add-in boards that use a universal I/O buffer.
ERROR REPORTING PINS.	
The error reporting pins are required by all devices and maybe asserted when enabled	
PERR#	Parity Error is only for the reporting of data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the agent receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected. (If sequential data phases each have a data parity error, the PERR# signal will be asserted for more than a single clock.) PERR# must be driven high for one clock before being tri-stated as with all sustained tri-state signals. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed. An agent cannot report a PERR# until it has claimed the access by asserting DEVSEL# (for a target) and completed a data phase or is the master of the current transaction.
SERR#	System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required. SERR# is pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of SERR# is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of SERR# to the deasserted state is accomplished by a weak pullup (same value as used for s/t/s) which is provided by the system designer and not by the 51signaling agent or central resource. This pull-up may take two to three clock periods to fully restore SERR#. The agent that reports SERR#s to the operating system does so anytime SERR# is sampled asserted.
INTERRUPT PINS (OPTIONAL).	
Interrupts on PCI are optional and defined as "level sensitive," asserted low (negative true), using open drain output drivers. The assertion and deassertion of INTx# is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device deasserts its INTx# signal. PCI defines one interrupt line for a single function device and up to four interrupt lines for a multi-function device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning.	
INTA#	Interrupt A is used to request an interrupt.
INTB#	Interrupt B is used to request an interrupt and only has meaning on a multi-function device.
INTC#	Interrupt C is used to request an interrupt and only has meaning on a multi-function device.
INTD#	Interrupt D is used to request an interrupt and only has meaning on a multi-function device.

### 3.21.2 KTQ45 PCI IRQ & INT routing

Board type	Slot	IDSEL	INTA	INTB	INTC	INTD
KTQ45/Flex	1	AD16	INT_PIRQ#A	INT_PIRQ#B	INT_PIRQ#C	INT_PIRQ#D
	2	AD17	INT_PIRQ#B	INT_PIRQ#G	INT_PIRQ#H	INT_PIRQ#E
KTQ45/ATXE	1	AD16	INT_PIRQ#A	INT_PIRQ#B	INT_PIRQ#C	INT_PIRQ#D
	2	AD17	INT_PIRQ#B	INT_PIRQ#G	INT_PIRQ#H	INT_PIRQ#E
	3	AD18	INT_PIRQ#G	INT_PIRQ#H	INT_PIRQ#E	INT_PIRQ#F
	4	AD19	INT_PIRQ#H	INT_PIRQ#E	INT_PIRQ#F	INT_PIRQ#G

When using the 820982 "PCI Riser - Flex - 2slot w. arbiter" the lower slot has IDSEL / IRQs routed straight through and the top slot has the routing: IDSEL=AD30, INT\_PIRQ#F, INT\_PIRQ#G, INT\_PIRQ#H, INT\_PIRQ#E. 820982 PCI Riser shall be plugged into Slot #1.

## 4 Onboard connectors and Mating connectors

Connector	Onboard Connectors		Mating Connectors	
	Manufacturer	Type no.	Manufacturer	Type no.
FAN_CPU	Foxconn	HF2704E-M1	AMP	1375820-4 (4-pole)
FAN_SYS	AMP	1470947-1	AMP	1375820-3 (3-pole)
KBDMSE	Molex	22-23-2061	Molex	22-01-2065
CDROM	Foxconn	HF1104E	Molex	50-57-9404
	Molex	70543-0038		
SATA	Hon Hai	LD1807V-S52T	Molex	67489-8005
			Kontron	KT 821035 (cable kit)
ATXPWR	Molex	43045-1201	Molex	43025-1200
ATX+12V-4pin	Molex	22-23-2041	Molex	22-01-2046
ATX+12V-6pin	Molex	22-23-2041	Molex	22-01-2046
COM2, 3, 4	Wuerth	61201020621	Molex	90635-1103
			Kontron	KT 821016 (cable kit)
			Kontron	KT 821017 (cable kit)
USB8/9	Pinrex	512-90-10GBB2	Kontron	KT 821401 (cable kit)
USB10/11*	(FRONTPNL)	-	Kontron	KT 821401 (cable kit)
PRINTER	Foxconn	HL2213F	Molex	90635-1263
			Kontron	KT 821031 (cable kit)
AUDIO_HEAD	Molex	87831-2620	Molex	51110-2651
			Kontron	KT 821043 (cable kit)
FRONTPNL	Pinrex	512-90-24GBB3	Molex	90635-1243
			Kontron	KT 821042 (cable kit)
FEATURE	Molex	87831-3020	Molex	51110-3051
			Kontron	KT 821041 (cable kit)

\* USB10/USB11 is located in FRONTPNL connector. Depending on application the KT821401 can be used.

**Note:** Only one connector will be mentioned for each type of onboard connector even though several types with same fit, form and function are approved and could be used as alternative. Please also notice that standard connectors like DVI, PCIe, PCI, CF, Ethernet and USB are not included in the list.

## 5 System Resources

### 5.1 Memory Map

Address (hex)	Size	Description	
00000000	0009FFFF	655360	System board
000A0000	000BFFFF	131072	PCI-bus
000A0000	000BFFFF	131072	Intel(R) Q45/Q43 Express Chipset
000C0000	000CFFFF	65536	System board
000D0000	000DFFFF	65536	PCI-bus
000E0000	000FFFFF	131072	System board
00100000	CDDFFFFFFF	3452960768	System board
CDE00000	DFFFFFFF	304087040	PCI-bus
D0000000	DFFFFFFF	268435456	Intel(R) Q45/Q43 Express Chipset
E0000000	EFFFFFFF	268435456	Motherboard resources
F0000000	FED8FFFF	249102336	PCI-bus
FE400000	FE7FFFFF	4194304	Intel(R) Q45/Q43 Express Chipset
FEAC0000	FEADFFFF	131072	Intel(R) 82567LM-3 Gigabit Network Connection
FEAF0000	FEAF3FFF	16384	Microsoft UAA-bus driver for High Definition Audio
FEAF4000	FEAF43FF	1024	Intel(R) ICH10 Family USB Enhanced Host Controller - 3A6A
FEAF6000	FEAF63FF	1024	Intel(R) ICH10 Family USB Enhanced Host Controller - 3A6C
FEAF8000	FEAF8FFF	4096	Intel(R) 82567LM-3 Gigabit Network Connection
FEAFB800	FEAFB8FF	256	Intel(R) ICH10 Family SMBus Controller - 3A60
FEAFBC00	FEAFBC0F	16	Intel(R) Management Engine Interface
FEB00000	FEBFFFFFFF	1048576	Intel(R) ICH10 Family PCI Express Root Port 5 - 3A78
FEBDC000	FEBDFFFF	16384	Intel(R) 82574L Gigabit Network Connection
FEBE0000	FEBFFFFFFF	131072	Intel(R) 82574L Gigabit Network Connection
FEC00000	FEC0FFFF	4096	Motherboard resources
FED14000	FED19FFF	24576	System board
FED1C000	FED1FFFF	16384	Motherboard resources
FED20000	FED3FFFF	131072	Motherboard resources
FED40000	FED8FFFF	327680	Motherboard resources
FED90000	FED93FFF	16384	System board
FED90000	FFFFFFFF	19333120	System board
FEE00000	FEE0FFFF	4096	Motherboard resources
FFB00000	FFBFFFFFFF	1048576	Intel(R) 82802 Firmware-hub unit
FFC00000	FFEFFFFFFF	3145728	Motherboard resources
FFF00000	FFFFFFFF	1048576	Intel(R) 82802 Firmware-hub unit

## 5.2 PCI Devices

Bus #	Device #	Function #	Vendor ID	Device ID	Chip	Device Function
0	25	0	8086	10DE	82567LM-3	Gigabit Network Connection
2	0	0	8086	10D3	82574L	Gigabit Network Connection
0	30	0	8086	244E	82801JB ICH10	I/O Controller Hub 10
0	31	5	8086	3A06	82801JB ICH10	2-port SATA Controller
0	31	2	8086	3A00	82801JB ICH10	4-port SATA Controller
0	27	0	8086	3A6E	82801JB ICH10	High Definition Audio Controller
0	28	0	8086	3A70	82801JB ICH10	PCI Express Root Port 1
0	28	4	8086	3A78	82801JB ICH10	PCI Express Root Port 5
0	31	3	8086	3A60	82801JB ICH10	SMBus Controller
0	26	0	8086	3A67	82801JB ICH10	USB Universal Host Controller
0	26	1	8086	3A68	82801JB ICH10	USB Universal Host Controller
0	26	2	8086	3A69	82801JB ICH10	USB Universal Host Controller
0	29	0	8086	3A64	82801JB ICH10	USB Universal Host Controller
0	29	1	8086	3A65	82801JB ICH10	USB Universal Host Controller
0	29	2	8086	3A66	82801JB ICH10	USB Universal Host Controller
0	26	7	8086	3A6C	82801JB ICH10	USB2 Enhanced Host Controller
0	29	7	8086	3A6A	82801JB ICH10	USB2 Enhanced Host Controller
0	31	0	8086	3A14	82801JB ICH10	LPC Bridge
0	3	0	8086	2E14	Q45 Chipset	Host Embedded Controller Interface
0	2	0	8086	2E12	Q45 Chipset	Integrated Graphics 0
0	0	0	8086	2E10	Q45 Chipset	Memory Controller Hub



## 5.4 IO Map

Address range (hex)		Size	Description
0	000F	16	DMA-controller
0	0CF7	3320	PCI-bus
10	001F	16	Motherboard resources
20	21	2	Programmable interrupt controller
22	003F	30	Motherboard resources
40	43	4	System timer
44	005F	28	Motherboard resources
60	60	1	Standard keyboard
61	61	1	System Speaker
62	63	2	Motherboard resources
64	64	1	Standard keyboard
65	006F	11	Motherboard resources
70	71	2	System CMOS/Real time clock
72	007F	14	Motherboard resources
80	80	1	Motherboard resources
81	83	3	DMA-controller
84	86	3	Motherboard resources
87	87	1	DMA-controller
88	88	1	Motherboard resources
89	008B	3	DMA-controller
008C	008E	3	Motherboard resources
008F	008F	1	DMA-controller
90	009F	16	Motherboard resources
00A0	00A1	2	Programmable interrupt controller
00A2	00BF	30	Motherboard resources
00C0	00DF	32	DMA-controller
E0	00EF	16	Motherboard resources
00F0	00FF	16	Numerical Data Processor
170	177	8	Secondary IDE-channel
01F0	01F7	8	Primary IDE-channel
274	277	4	ISAPNP read data port
279	279	1	ISAPNP read data port
02F8	02FF	8	Communications port (COM2)
376	376	1	Secondary IDE-channel
378	037F	8	Printer Port (LPT1)
03B0	03BB	12	Intel(R) Q45/Q43 Express Chipset
03C0	03DF	32	Intel(R) Q45/Q43 Express Chipset
03F6	03F6	1	Primary IDE-channel
03F8	03FF	8	Communications port (COM1)
400	041F	32	Intel(R) ICH10 Family SMBus Controller - 3A60
04D0	04D1	2	Motherboard resources
500	057F	128	Motherboard resources
800	087F	128	Motherboard resources
0A00	0A0F	16	Motherboard resources
0A10	0A1F	16	Motherboard resources
0A79	0A79	1	ISAPNP read data port
0D00	FFFF	62208	PCI-bus
BC00	BC0F	16	Intel(R) ICH10 Family 2 port Serial ATA Storage Controller 2 - 3A06
C000	C00F	16	Intel(R) ICH10 Family 2 port Serial ATA Storage Controller 2 - 3A06
C080	C083	4	Intel(R) ICH10 Family 2 port Serial ATA Storage Controller 2 - 3A06
C400	C407	8	Intel(R) ICH10 Family 2 port Serial ATA Storage Controller 2 - 3A06
C480	C483	4	Intel(R) ICH10 Family 2 port Serial ATA Storage Controller 2 - 3A06
C800	C807	8	Intel(R) ICH10 Family 2 port Serial ATA Storage Controller 2 - 3A06
CC00	CC1F	32	Intel(R) ICH10 Family USB Universal Host Controller - 3A66
D000	D01F	32	Intel(R) ICH10 Family USB Universal Host Controller - 3A65
D080	D09F	32	Intel(R) ICH10 Family USB Universal Host Controller - 3A64
D400	D41F	32	Intel(R) ICH10 Family USB Universal Host Controller - 3A69
D480	D49F	32	Intel(R) ICH10 Family USB Universal Host Controller - 3A68
D800	D81F	32	Intel(R) ICH10 Family USB Universal Host Controller - 3A67
D880	D89F	32	Intel(R) 82567LM-3 Gigabit Network Connection
DC00	DC07	8	Intel(R) Q45/Q43 Express Chipset
E000	EEEE	4096	Intel(R) ICH10 Family PCI Express Root Port 5 - 3A78
EC00	EC1F	32	Intel(R) 82574L Gigabit Network Connection
FF90	FF9F	16	Intel(R) ICH10 Family 4 port Serial ATA Storage Controller 1 - 3A00
FFA0	FFAF	16	Intel(R) ICH10 Family 4 port Serial ATA Storage Controller 1 - 3A00

## 6 Overview of BIOS Features

This section details specific BIOS features for the KTQ45 board.  
The KTQ45 board is based on the AMI BIOS core version 8.10 with Kontron BIOS extensions.

### 6.1 System Management BIOS (SMBIOS/DMI)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components.

The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS.

The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT\*, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

### 6.2 Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support is Disabled in the BIOS Setup.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

### 6.3 BIOS Update

The BIOS can be updated using Kontron utility called bf.exe, which are available on the Kontron Web site. The utility supports DOS and Windows environment. Before updating the BIOS, AMT related restrictions must be followed. Do not attempts to ignore below steps as it might result in corrupted BIOS.

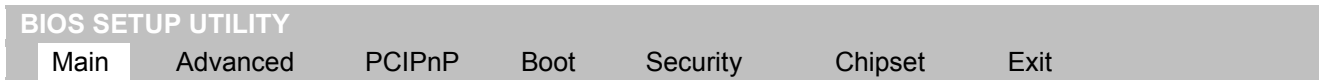
Before updating the BIOS below steps must be followed:

- Make sure that AMT technology is disabled under the menu: Advanced, Intel AMT Configuration, Intel AMT Support.
- Make sure not populate DIMM into SLOT 1 socket (DIMM socket closest to the CPU) The 3 remaining DIMM sockets can be freely used without restrictions.

# BIOS Configuration/Setup

## 6.4 Introduction

The BIOS Setup is used to view and configure BIOS settings for the KTQ45 board. The BIOS Setup is accessed by pressing the DEL key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The Menu bar looks like this:

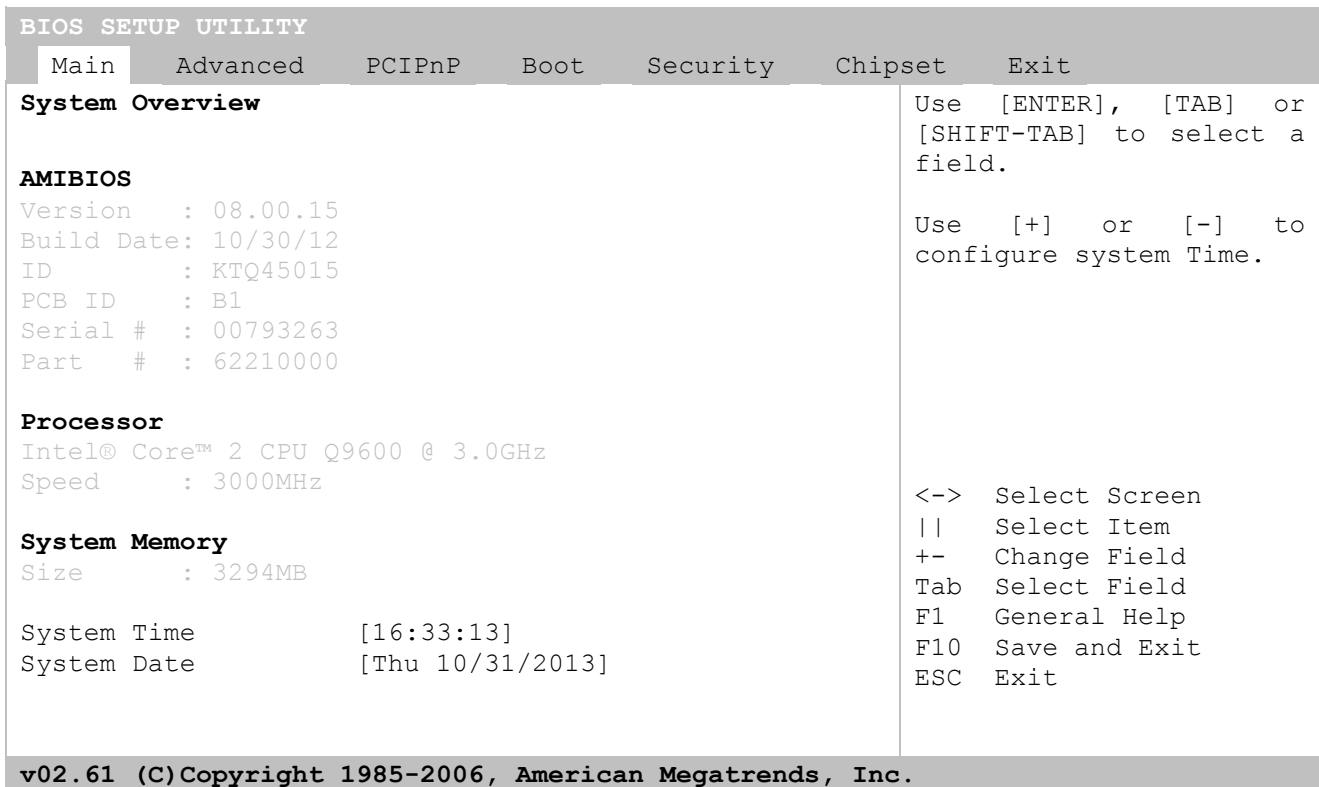


The available keys for the Menu screens are:

- Select Menu: <←> or <→>
- Select Item: <↑> or <↓>
- Select Field: <Tab>
- Change Field: <+> or <->
- Help: <F1>
- Save and Exit: <F10>
- Exits the Menu: <Esc>

Please note that in the following the different BIOS Features will be described as having some options. These options will be selected automatically when loading either Failsafe Defaults or Optimal Defaults. The Default options will be indicated by the option in **bold**, but please notice that when Failsafe Defaults are loaded a few of the options, marked with “\*”, are now the default option.

## 6.5 Main Menu



Feature	Options	Description
System Time	HH:MM:SS	Set the system time.
System Date	MM/DD/YYYY	Set the system date.

## 6.6 Advanced Menu

```

BIOS SETUP UTILITY
  Main   Advanced  PCIPnP  Boot   Security  Chipset  Exit
Advanced Settings
Warning: Setting wrong values in below sections
         may cause system to malfunction.

▶ CPU Configuration
▶ IDE Configuration
▶ LAN Configuration
▶ SuperIO Configuration
▶ Hardware Health Configuration
▶ Voltage Monitor
▶ ACPI Configuration
▶ Intel AMT Configuration
▶ Intel VT-d Configuration
▶ Remote Access Configuration
▶ Trusted Computing
▶ USB Configuration

Configure CPU.

<-      Select Screen
||      Select Item
Enter   Go to Sub Screen
F1      General Help
F10     Save and Exit
ESC     Exit

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```

### 6.6.1 Advanced settings – CPU Configuration

```

BIOS SETUP UTILITY
  Advanced
CPU Configure
Module Version: 3F.14
Disabled for WindowsXP

Manufacturer: Intel
Intel® Core™2 CPU           Q9650 @ 3.0Ghz
Frequency   : 3.00Ghz
FSB Speed   : 1332Mhz
Cache L1    : 128 KB
Cache L2    : 12288 KB
Ratio Actual Value:9

C1E Support           [Enabled]
Max CPUID Value Limit [Disabled]
Execute-Disable Bit Capability [Enabled]
Core Multi-Processing [Enabled]
PECI                  [Enabled]
Intel® SpeedStep™ tech [Enabled]
Intel® C-STATE tech   [Enabled]

<->  Select Screen
||   Select Item
+-   Change Option
F1   General Help
F10  Save and Exit
ESC  Exit

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```

Feature	Options	Description
C1E Support	Disabled <b>Enabled</b>	If disabled and if “Intel® C-STATE tech” is disabled then CPU always runs full speed.
Max CPUID Value Limit	<b>Disabled</b> Enabled	Disabled for WindowsXP
Execute-Disable Bit Capability	Disabled <b>Enabled</b>	When disabled, force the XD feature flag to always return 0.
Core Multi-Processing	Disabled <b>Enabled</b>	When disabled, disable one execution core of each CPU die.
PECI	Disabled <b>Enabled</b>	When enabled, enables Peci interface.
Intel® SpeedStep™ tech	Disabled* <b>Enabled</b>	Disabled: Disable GV3 Enabled: Enable GV3
Intel® C-STATE tech	Disabled* <b>Enabled</b>	CState enabled: CPU idle is set to C2 C3 C4 State

## 6.6.2 Advanced settings – IDE Configuration

```

BIOS SETUP UTILITY
  Advanced
IDE Configuration
  Mirrored IDER Configuration      [Disabled]
  Configure SATA#1 as             [SATA]

  ▶ Primary IDE Master           : [Hard Disk]
  ▶ Primary IDE Slave            : [Not Detected]
  ▶ Secondary IDE Master         : [Not Detected]
  ▶ Secondary IDE Slave          : [Not Detected]
  ▶ Third IDE Master             : [Not Detected]

  Hard Disk Write Protect         [Disabled]
  IDE Detect Time Out (Sec)      [35]

  Sata BIOS Extension            [Enabled]
  ▶ AHCI Configuration

Options
Disabled
Compatible
Enhanced

<-  Select Screen
|   Select Item
+-  change option
F1   General Help
F10  Save and Exit
ESC  Exit

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```

Feature	Options	Description
Configure SATA#1 as	<b>SATA</b> RAID AHCI	SATA RAID AHCI

Feature	Options	Description
Hard Disk Write Protect	<b>Disabled</b> Enabled	Disable/Enable device write protection. This will be effective only if device is accessed through BIOS
IDE Detect Time Out (Sec)	0 5 10 15 20 25 30 <b>35</b>	Select the timeout value for detecting ATA/ATAPI device(s)
Sata BIOS Extension	Disabled <b>Enabled</b>	Disabled Enabled

BIOS SETUP UTILITY

Advanced

**Primary IDE Master**

Select the type of devices connected to the system

Device :Hard Disk  
 Vendor :ST340014A  
 Size :40.0GB  
 LBA Mode :Supported  
 Block Mode :16Sectors  
 PIO Mode :4  
 Async DMA :MultiWord DMA-2  
 Ultra DMA :Ultra DMA-5  
 S.M.A.R.T. :Supported

---

Type [Auto]  
 LBA/Large Mode [Auto]  
 Block (Multi-Sector Transfer) [Auto]  
 PIO Mode [Auto]  
 DMA Mode [Auto]  
 S.M.A.R.T. [Auto]  
 32Bit Data Transfer [Enabled]

<- Select Screen  
 || Select Item  
 +- Change Option  
 F1 General Help  
 F10 Save and Exit  
 ESC Exit

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Feature	Options	Description
Type	Not Installed <b>Auto</b> CD/DVD ARMD	Select the type of device installed
LBA/Large Mode	Disabled <b>Auto</b>	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, and Sectors.
Block (Multi-Sector Transfer)	Disabled <b>Auto</b>	Select if the device should run in Block mode
PIO Mode	<b>Auto</b> 0 1 2 3 4	Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.
DMA Mode	<b>Auto</b> SWDMA0 SWDMA1 SWDMA2 MWDMA0 MWDMA1 MWDMA2 UDMA0 UDMA1 UDMA2 UDMA3 UDMA4 UDMA5 UDMA6	Selects the Ultra DMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode.  <b>Note: To use UDMA Mode 2, 3, 4, 5 and 6 with a device, the harddisk cable used MUST be UDMA66/100 cable (80-conductor cable).</b>
S.M.A.R.T.	<b>Auto</b> Disabled Enabled	Select if the Device should be monitoring itself (Self-Monitoring, Analysis and Reporting Technology System)
32Bit Data Transfer	Disabled* <b>Enabled</b>	Select if the Device should be using 32Bit data Transfer

BIOS SETUP UTILITY

Advanced

**AHCI Settings**

AHCI BIOS Support [Enabled]

- ▶ AHCI Port0 [Not Detected]
- ▶ AHCI Port1 [Not Detected]
- ▶ AHCI Port2 [Not Detected]
- ▶ AHCI Port3 [Not Detected]
- ▶ AHCI Port4 [Not Detected]

Enables for supporting

<- Select Screen  
 || Select Item  
 +- change option  
 F1 General Help  
 F10 Save and Exit  
 ESC Exit

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Feature	Options	Description
AHCI BIOS Support	Disabled <b>Enabled</b>	Enabled for Supporting

BIOS SETUP UTILITY

Advanced

**AHCI Port0**

Device :Hard Disk  
 Vendor :WDC WD800AAJS-00PSA0  
 SIZE :80GB

- ▶ SATA Port0 [AUTO]
- ▶ S.M.A.R.T [Enabled]

Select the type of device connected to the system.

<- Select Screen  
 || Select Item  
 +- change option  
 F1 General Help  
 F10 Save and Exit  
 ESC Exit

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Feature	Options	Description
SATA Port0	<b>Auto</b> Not Installed	Select the type of device connected to the system.
S.M.A.R.T	<b>Enabled</b> Disabled	S.M.A.R.T. stands for Self-Monitoring, Analysis and Reporting Technology.

### 6.6.3 Advanced settings – LAN Configuration

```

BIOS SETUP UTILITY
  Advanced
LAN Configuration
  Control of Ethernet
  Devices and PXE boot

ETH1 Configuration (Right)      [Enabled]
  MAC Address & Link status    : 00E0F41E24A4 +
ETH2 Configuration (Left)      [Enabled]
  MAC Address & Link status    : 00E0F41E24A5 -

<-  Select Screen
||   Select Item
+-   change option
F1   General Help
F10  Save and Exit
ESC  Exit

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```

Feature	Options	Description
ETH1 Configuration	Disabled <b>Enabled</b> With RPL/PXE boot	Disable/enable LAN or enabled with RPL/PXE boot

Feature	Options	Description
ETH2 Configuration	Disabled <b>Enabled</b> With RPL/PXE boot	Disable/enable LAN or enabled with RPL/PXE boot

**Notes:**

1. The “+” and “-” (to the right of the MAC address) indicates if link is established or not.
2. ETH1 (and only ETH1) can be used for AMT.

### 6.6.4 Advanced settings – Configure Win627DHG Super IO Chipset

BIOS SETUP UTILITY		
	Advanced	
<b>Configure Win627DHG Super IO Chipset</b>		Allows BIOS to Select Serial Port1 Base Addresses.
Serial Port1 Address	[3F8/IRQ4]	
Serial Port2 Address	[2F8/IRQ3]	
Serial Port2 Mode	[Normal]	
Parallel Port Address	[378]	
Parallel Port Mode	[Normal]	
Parallel Port IRQ	[IRQ7]	
Serial Port3 Address	[Disabled]	
RS485 Port Address	[Disabled]	
		<- Select Screen    Select Item +- change option F1 General Help F10 Save and Exit ESC Exit
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Feature	Options	Description
Serial Port1 Address	Disabled <b>3F8/IRQ4</b> 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3	Select the BASE I/O address and IRQ.  (The available options depend on the setup for the other Serial Ports).
Serial Port2 Address	Disabled 3F8/IRQ4 <b>2F8/IRQ3</b> 3E8/IRQ4 2E8/IRQ3	Select the BASE I/O address and IRQ.  (The available options depend on the setup for the other Serial Ports).
Serial Port2 Mode	<b>Normal</b> IrDA ASK IR	Select Mode for Serial Port2
If IrDA or ASK IR: IR Duplex Mode	Full Duplex <b>Half Duplex</b>	IrDA communication selection
Parallel Port Address	Disabled * <b>378</b> 278 3BC	Select the I/O address for the Parallel Port.
Parallel Port Mode	<b>Normal</b> Bi-Directional ECP EPP ECP & EEP	Select the mode of operation for the Parallel Port
If ECP Mode: ECP Mode DMA Channel	DMA0 DMA1 <b>DMA3</b>	Select a DMA channel in ECP mode of operation
If EPP mode: EPP Version	<b>1.9</b> 1.7	Select version of EPP in the EPP mode of operation
Parallel Port IRQ	IRQ5 <b>IRQ7</b>	Select a IRQ for the Parallel Port

(Continues)

Feature	Options	Description
Serial Port3 Address	<b>Disabled</b> 3F8 2F8 3E8 2E8	Allows BIOS to select Serial Port3 Base Addresses  (The available options depend on the setup for the other Serial Ports).
Serial Port3 IRQ	IRQ3 IRQ4 IRQ10 <b>IRQ11</b>	Allows BIOS to select Serial Port3 IRQ.  (The available options depend on the setup for the other Serial Ports).
RS485 Port Address	<b>Disabled</b> 3F8 2F8 3E8 2E8	Allows BIOS to select Serial Port4 Base Addresses  (The available options depend on the setup for the other Serial Ports).
RS485 Port IRQ	IRQ3 IRQ4 <b>IRQ10</b> IRQ11	Allows BIOS to select Serial Port4 IRQ.  (The available options depend on the setup for the other Serial Ports).

### 6.6.5 Advanced settings – Hardware Health Configuration

```

BIOS SETUP UTILITY
  Advanced
Hardware Health Configuration
System Temperature      :48°C/118°F
CPU Temperature        :56°C/132°F
VTIN Temperature       :N/A

SYS FAN Speed          :Fail
  Fan Cruise Control   [Disable]
  Fan Type              [4 Wire]
CPU FAN Speed          :2537 RPM
  Fan Cruise Control   [Thermal]
  Fan Setting           [45°C/113°F]
  Fan Type              [4 Wire]
AUXFAN Speed          :2164
  Fan Cruise Control   [Speed]
  Fan Setting           [2177 RPM]

Fan Step Time          [2]
Low RPM Fan Range     [Disabled]

Watchdog Function      [Disabled]
    
```

Disable = Full Speed

Thermal: Does regulate fan speed according to specified temperature

Speed: Does regulate according to specified RPM

<- Select Screen  
|| Select Item  
+- change option  
F1 General Help  
F10 Save and Exit  
ESC Exit

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Feature	Options	Description
Fan Cruise Control	<b>Disabled</b> Thermal Speed	Select how the Fan shall operate.  When set to Thermal, the Fan will start to run at the CPU die temperature set below.  When set to Speed, the Fan will run at the fixed speed set below.
Fan Settings	1406-5625 RPM 30°-60°C	The fan can operate in Thermal mode or in a fixed fan speed mode
Fan Type	<b>4 wire</b> 3 wire	Select the electrical interface for the fan:  3 Wire = PWM output to fan power line. RPM reading and speed regulation at lower speed might be poor.  4 Wire = 12VDC always PWM on control signal
Fan Step Time	0, 1, <b>2</b> , 3, 4, 5, 6, 7	Fan regulation delay. (0 is fast and 7 is slow)
Low RPM Fan Range	<b>Disabled</b> Enabled	Enabled: Down to 500 RPM is possible. Note that if Speed setting is used then set the speed to the double of the requested RPM.
Watchdog	<b>Disabled</b> 15 seconds 30 seconds 1 minute 2 minutes 5 minutes 10 minutes	To be serviced via API.

**Note:** The AUXFAN is available via Feature Connector.

## 6.6.6 Advanced settings – Voltage Monitor

```
BIOS SETUP UTILITY
  Advanced
Voltage Monitor

Requested Core CPU      :1.25000 V
CPU Vccp                :1.240 V

AVCC                    :3.248 V
3VCC                    :3.248 V
P12V                    :11.800 V
-12Vin                  :Good
P5V                     :5.016 V
DDR1V5                  :1.528 V
P1V5                    :1.544 V
VSB                     :3.264 V
VBAT                    :3.072 V

<-  Select Screen
||  Select Item
+-  change option
F1  General Help
F10 Save and Exit
ESC Exit

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```

### 6.6.7 Advanced settings – ACPI Settings

```

BIOS SETUP UTILITY
  Advanced
ACPI Settings
Suspend mode                [S3 (STR)]
Repost Video on S3 Resume   [No]
ACPI Version Features       [ACPI v1.0]

PS/2 Kbd/Mouse S4/S5 Wake   [Disabled]
Keyboard Wake Hotkey        [Any key]
USB Device Wakeup From S3/S4 [Enabled]

Select the ACPI state used for System Suspend.

<->   Select Screen
||     Select Item
+-     change option
F1     General Help
F10    Save and Exit
ESC    Exit

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```

Feature	Options	Description
Suspend mode	S1 (POS) <b>S3 (STR)</b>	Select the ACPI state used for System Suspend
Repost Video on S3 Resume	<b>No</b> Yes	Determines whether to invoke VGA BIOS post on S3/STR resume
ACPI Version Features	<b>ACPI v1.0</b> ACPI v2.0 ACPI v3.0	Enabled RSDP pointers to 64-bit Fixed System Description Table. Di ACPI version has some.
PS/2 Kbd/Mouse S4/S5 Wake	<b>Disabled</b> Enabled	Enabled: The System can also be waked from S4 or S5. Disabled: PS/2 Kbd or Mouse can still wake system from S3
Keyboard Wake Hotkey	<b>Any key</b> "Space" "Enter" "Sleep button"	Any key "Space" "Enter" "Sleep button"
USB Device Wakeup from S3/S4	Disabled <b>Enabled</b>	Enabled/Disable USB Device Wakeup From S3/S4.

### 6.6.8 Advanced settings – Intel AMT Configuration

```

BIOS SETUP UTILITY
  Advanced
Configuration Intel AMT Parameters
Intel AMT Support          [Enabled]
Force IDER                 [Disabled]
Force SOL                  [Disabled]
Unconfigure AMT/ME        [Disabled]
Active Remote Assistance   [Disabled]

Options
Disabled
Enabled

<->  Select Screen
||   Select Item
+-   change option
F1   General Help
F10  Save and Exit
ESC  Exit

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```

Feature	Options	Description
Intel AMT Support	<b>Disabled</b> Enabled	Disabled Enabled
Force IDER	<b>Disabled</b> IDER Pri. Master IDER Pri. Slave IDER Sec. Master IDER Pri. Slave	Disabled IDER Pri. Master IDER Pri. Slave IDER Sec. Master IDER Pri. Slave
Force SOL	<b>Disabled</b> Enabled	
Unconfigure AMT/ME	<b>Disabled</b> Enabled	Disabled Enabled

### 6.6.9 Advanced settings – Intel VT-d Configuration

```

BIOS SETUP UTILITY
  Advanced
Intel VT-d Configuration
Intel VT-d                [Disabled]
Options
Disabled
Enabled

<->  Select Screen
||   Select Item
+-   change option
F1   General Help
F10  Save and Exit
ESC  Exit

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```

Feature	Options	Description
Intel VT-d	<b>Disabled</b>	Disabled
	Enabled	Enabled

### 6.6.10 Advanced settings – Remote Access Configuration

```

BIOS SETUP UTILITY
  Advanced
Configure Remote Access type and parameters
Remote Access           [Enabled]
Serial port number      [COM1]
  Base Address, IRQ     [3F8h, 4]
Serial Port Mode        [115200 8,n,1]
Flow Control            [None]
Redirection After BIOS POST [Always]
Terminal Type           [ANSI]
VT-UTF8 Combo Key Support [Enabled]
Sredir Memory Display Delay [No Delay]

Select Remote Access type.

<-> Select Screen
||  Select Item
+-  change option
F1  General Help
F10 Save and Exit
ESC  Exit

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```

Feature	Options	Description
Remote Access	<b>Disabled</b> Enabled	When Enabled then a remote PC can via one of the serial ports behave like a TTY terminal, so that keyboard and monitor (in a terminal window) is emulated by the remote PC. As remote PC terminal program the Windows Hyperterminal can be used.
Serial port number	<b>COM1</b> COM2	Setup which comport that should be used for communication
Serial Port Mode	<b>115200 8 n 1</b> 57600 8 n 1 38400 8 n 1 19200 8 n 1 9600 8 n 1	Select the serial port speed
Flow Control	<b>None</b> Hardware Software	Select Flow Control for serial port
Redirection After BIOS POST	Disabled Boot Loader <b>Always</b>	How long shall the BIOS send the picture over the serial port
Terminal Type	<b>ANSI</b> VT100 VT-UTF8	Select the target terminal type
VT.UTF8 Combo Key Support	<b>Enabled</b> Disabled	Enable VT-UTF8 Combination Key Support for ANSI/VT100 terminals
Sredir Memory Display Delay	<b>No Delay</b> Delay 1 Sec Delay 2 Sec Delay 4 Sec	Gives the delay in seconds to display memory information

### 6.6.11 Advanced settings – Trusted Support

```

BIOS SETUP UTILITY
  Advanced
Trusted Computing
TCG/TPM Support                [Yes]
Execute TPM Command            [Don't change]
  TPM Enabled/Disabled Status  [No State]
  TPM Owner Status             [No State]

<->  Select Screen
||   Select Item
+-   change option
F1   General Help
F10  Save and Exit
ESC  Exit

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```

Feature	Options	Description
TCG/TPM Support	No Yes	Enables/Disable TPM TCG (TPM 1.1/1.2) Support.
Execute TPM Command	Don't change Disabled Enabled	Enable(Activate)/ Disable(Deactivate) Command to TPM

## 6.6.12 Advanced settings – USB Configuration

BIOS SETUP UTILITY	
Advanced	
<b>USB Configuration</b>  Module Version - 2.24.5-13.4  USB Devices Enabled : 1 Drive  Legacy USB Support                   [Enabled] USB 2.0 Controller Mode           [HiSpeed]  ▶ USB Mass Storage Device Configuration	Enables support for legacy USB. AUTO option disables if no USB Devices are connected.       <-> Select Screen    Select Item +- change option F1 General Help F10 Save and Exit ESC Exit
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Feature	Options	Description
Legacy USB Support	Disabled <b>Enabled</b> Auto	Support for legacy USB Keyboard
USB 2.0 Controller Mode	FullSpeed* <b>HiSpeed</b>	Configure the USB 2.0 controller in HiSpeed (480Mbps) or FullSpeed (12Mbps).  Note: This feature is not available when Failsafe Defaults are loaded, because USB2.0 controller is disabled as default.

## 6.6.13 Advanced settings – USB Mass Storage Device Configuration

BIOS SETUP UTILITY	
Advanced	
<b>USB Mass Storage Device Configuration</b>	
USB Mass Storage Reset Delay [20 Sec]	Number of seconds POST waits for the USB mass storage device after start unit command.
Device #1 JetFlash TS256MJF2L	
Emulation Type [Auto]	
	<-> Select Screen    Select Item +- change option F1 General Help F10 Save and Exit ESC Exit
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Feature	Options	Description
USB Mass Storage Reset Delay	10 Sec <b>20 Sec</b> 30 Sec 40 Sec	Number of seconds POST waits for the USB mass storage device after start unit command.
Emulation Type	<b>Auto</b> Floppy Forced FDD Hard Disk CDROM	If Auto, USB devices less than 530MB will be emulated as Floppy and remaining as hard drive. Forced FDD option can be used to force a HDD formatted drive to boot as FDD (Ex. ZIP drive).

## 6.7 PCIpnp Menu

```

BIOS SETUP UTILITY
Main  Advanced  PCIPnP  Boot  Security  Chipset  Exit
Advanced PCI/PnP Settings
Warning: Setting wrong values in below sections
          May cause system to malfunction.

Allocate IRQ to PCI VGA      [Yes]
Palette Snooping             [Disabled]

Yes: Assigns IRQ to PCI
VGA card if card
requests IRQ.
No: Does not assign IRQ
to PCI VGA card even if
card requests an IRQ

<->  Select Screen
||   Select Item
+-   change option
F1   General Help
F10  Save and Exit
ESC  Exit

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```

Feature	Options	Description
Allocate IRQ to PCI VGA	Yes No	Yes: Assigns IRQ to PCI VGA card if card requests IRQ. No: Does not assign IRQ to PCI VGA card even if card requests an IRQ
Palette Snooping	Disabled Enabled	Enabled: informs the PCI devices that an ISA graphics device is installed in the system so the card will function correctly.

## 6.8 Boot Menu

```
BIOS SETUP UTILITY
Main   Advanced   PCIPnP   Boot   Security   Chipset   Exit
Boot Settings
▶ Boot Settings Configuration
▶ Boot Device Priority

Configure Settings
during System Boot.

<->  Select Screen
||   Select Item
Enter Go to Sub Screen
F1   General Help
F10  Save and Exit
ESC  Exit

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```

### 6.8.1 Boot – Boot Settings Configuration

BIOS SETUP UTILITY

Boot

Boot Settings Configuration		Allows BIOS to skip certain tests while booting in order to decrease boot time.
Quick Boot	[Enabled]	<-> Select Screen    Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit
Quiet Boot	[Disabled]	
AddOn ROM Display Mode	[Force BIOS]	
Bootup Num-Lock	[On]	
PS/2 Mouse Support	[Auto]	
Wait for 'F1' If Error	[Enabled]	
Hit 'DEL' Message Display	[Enabled]	
Interrupt 19 Capture	[Disabled]	
Force boot Device	[Disabled]	

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Feature	Options	Description
Quick Boot	<b>Enabled</b> Disabled	Allows BIOS to skip certain tests while booting in order to decrease boot time.
Quiet Boot	<b>Disabled</b> Enabled Black Screen White Screen	Disabled: Displays normal POST messages. Enabled: Displays OEM Logo (no POST messages). Black Screen: No picture. White Screen: White picture.
AddOn ROM Display Mode	<b>Force BIOS</b> Keep current	Set display mode for Option ROM.
Bootup Num-Lock	Off <b>On</b>	Select Power-on state for numlock
PS/2 Mouse Support	Disabled Enabled <b>Auto</b>	Select support for PS/2 Mouse.
Wait for 'F1' If Error (see note)	Disabled <b>Enabled</b>	Wait for F1 key to be pressed if error occurs.
Hit 'DEL' Message Display	Disabled <b>Enabled</b>	Displays "Press DEL to run Setup" in POST.
Interrupt 19 Capture	<b>Disabled</b> Enabled	Enabled: Allows option ROMs to trap interrupt 19
Force boot Device	<b>Disabled</b> Primary IDE Master Primary IDE Slave Secondary IDE Master Secondary IDE Slave Third IDE Master Third IDE Slave 5 <sup>th</sup> IDE Master 6 <sup>th</sup> IDE Master RAID Any Harddrive (Above) Network	Overrides current boot setting. Device must be in the boot priority menu, though. If the device fails to boot, the system will NOT try other devices.

**Note:** List of errors:

<INS> Pressed  
 Timer Error  
 Interrupt Controller-1 error  
 Keyboard/Interface Error  
 Halt on Invalid Time/Date  
 NVRAM Bad

Primary Master Hard Disk Error  
 S.M.A.R.T HDD Error  
 Cache Memory Error  
 DMA Controller Error  
 Resource Conflict  
 Static Resource Conflict

PCI I/O conflict  
 PCI ROM conflict  
 PCI IRQ conflict  
 PCI IRQ routing table error

## 6.8.2 Boot – Boot Device Priority

BIOS SETUP UTILITY	
Boot	
<b>Boot Device Priority</b>	Specifies the boot sequence from the available devices.
1st Boot Device [ESS-ST380811AS]	A device enclosed in parenthesis has been disabled in the corresponding type menu.
	<-> Select Screen    Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit
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**Note:** When pressing <F11> while booting it is possible manually to select boot device.

## 6.9 Security Menu

```

BIOS SETUP UTILITY
  Main   Advanced  PCIPnP  Boot   Security  Chipset  Exit
-----
Security Settings
Supervisor Password :Not Installed
User Password       :Not Installed

Change Supervisor Password
Change User Password

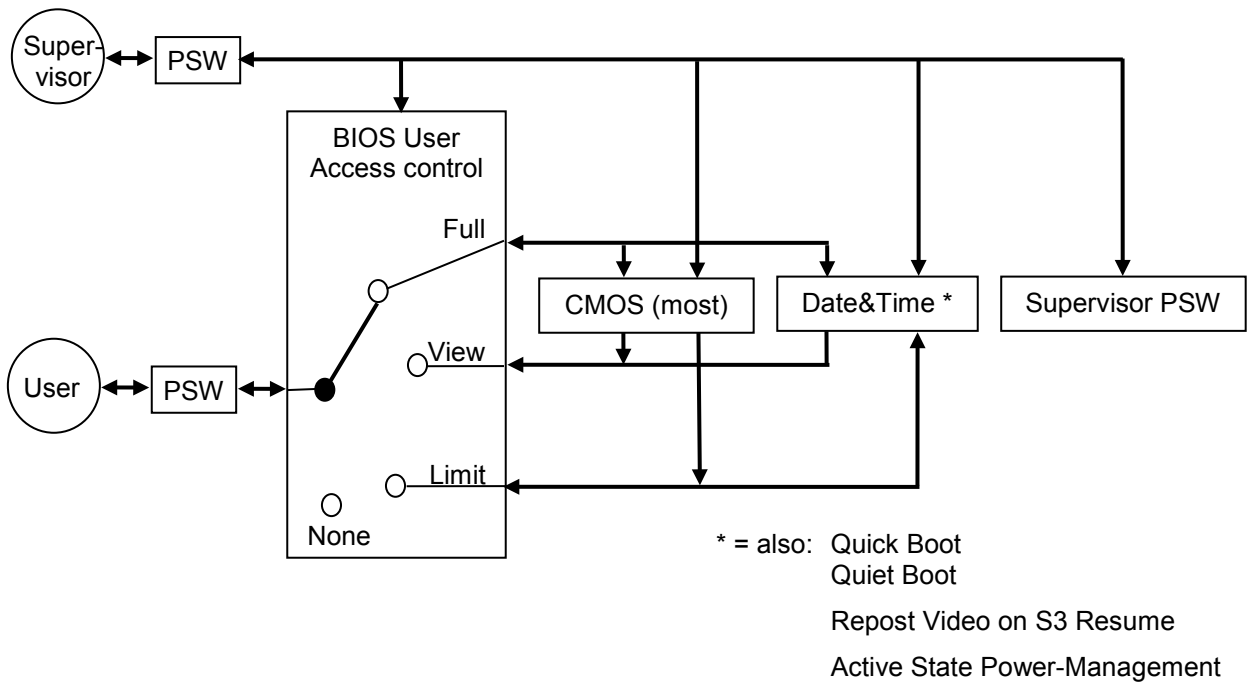
Install or Change the password.

<->  Select Screen
||   Select Item
Enter Go to Sub Screen
F1   General Help
F10  Save and Exit
ESC  Exit

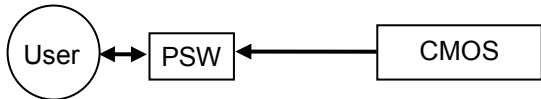
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```

Feature	Options	Description
Change Supervisor Password	Password	When not cleared the advanced Supervisor Password protection system is enabled (see below diagram). Hereafter setting can only be accessed when entering BIOS as Supervisor.
User Access Level	<b>Full Access</b> View Only Limited No Access	Only visible if Supervisor Password is installed. Full Access: User can change all BIOS settings. View Only: User can only read BIOS settings. Limited: User can only read settings except: Date & Time, Quick Boot, Quiet Boot, Repost Video on S3 Resume, Active State Power-Management and Remote Access. No Access: User cannot enter BIOS, but if Password Check = Always then User password will allow boot.
Change User Password	Password	Change the User Password
Password Check	<b>Setup</b> Always	Only visible if Password is installed. Setup: Protects only BIOS settings. Always: Protects both BIOS settings and Boot.

Supervisor Password protection (setup Supervisor before User)



User Password protection only (no Supervisor Password used)



## 6.10 Chipset Menu

```
BIOS SETUP UTILITY
Main   Advanced  PCIPnP  Boot   Security  Chipset  Exit
Advanced Chipset Settings
Warning: Setting wrong values in below sections
         may cause system to malfunction.

▶ North Bridge Configuration
▶ South Bridge Configuration
▶ ME Subsystem Configuration
▶ VE Subsystem Configuration
▶ Spread spectrum control

Configures North Bridge
features.

<->  Select Screen
||   Select Item
Enter Go to Sub Screen
F1   General Help
F10  Save and Exit
ESC  Exit

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```

## 6.10.1 Advanced Chipset Settings – North Bridge Chipset Configuration

BIOS SETUP UTILITY		Chipset
<b>North Bridge Chipset Configuration</b>		
Memory Remap Feature	[Disabled]	ENABLE: Allow remapping of overlapped PCI memory above the total physical memory.
PCI MMIO Allocation: 4GB to 4428MB		
Memory Hole	[Disabled]	Disable: Do not allow remapping of memory
Initial Graphics Adaptor	[PEG/PCI]	
IGD Graphics Mode Select	[Enabled, 32MB]	
PEG Port Configuration		
▶ Video Function Configuration		
		<-> Select Screen    Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit
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Feature	Options	Description
Memory Remap Feature (See note below)	<b>Disabled</b> Enabled	ENABLE: Allow remapping of overlapped PCI memory above the total physical memory.  Disable: Do not allow remapping of memory.
Memory Hole	<b>Disabled</b> 15MB-16MB	<b>Disabled</b> 15MB-16MB
Initial Graphics Adaptor	IGD PCI/IGD PCI/PEG PEG/IGD <b>PEG/PCI</b>	Select which graphics controller to use as the primary boot device.
IGD Graphics Mode Select	Disabled <b>Enabled, 32MB</b> Enabled, 64MB Enabled, 128MB	Select the amount of system memory used by the Integrated Graphic Device.

### Notes:

Memory Remap Feature should be Enabled when using 64bit OS and has effect if using more than 4GB of memory. If using 32bit OS and more than 3GB (max 4GB) then up to ½ GB might be lost if Memory Remap Feature is Enabled, so in general it is recommended to Disable the Memory Remap Feature when 32 bit OS is used.

Using PCIe Graphics card in combination with onboard graphics (VGA) is possible if BIOS setting *Initial Graphics Adaptor* = *IGD*. In this case onboard graphic will be Primary desktop and PCIe Graphics will be extended desktop. Note that PCIe Graphics driver shall be installed before the Intel Graphics driver.

## 6.10.2 Advanced Chipset ... – North Br. ... – Video Function Configuration

BIOS SETUP UTILITY		Chipset
<b>Video Function Configuration</b>		Options
DVMT Mode Select	[DVMT Mode]	Fixed Mode
DVMT/FIXED Memory	[256MB]	DVMT Mode
Flat Panel Type	[Type 3]	
Backlight Control Support	[VBIOS-Default]	
BIA Control	[VBIOS-Default]	
TV Standard	[VBIOS-Default]	
Spread Spectrum	[Disabled]	<-> Select Screen
Boot Display Preferences	[Auto]	Select Item
		Enter Go to Sub Screen
		F1 General Help
		F10 Save and Exit
		ESC Exit
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Feature	Options	Description
DVMT Mode Select	Fixed Mode <b>DVMT Mode</b>	Fixed Mode DVMT Mode
DVMT/FIXED Memory	128MB <b>256MB</b> Maximum DVMT	This setting is only
Flat Panel Type	Type 1, 2, <b>3</b> , 4 ...16	Type 1,2,3 to 16
Backlight Control Support	<b>VBIOS-Default</b> Both BLC & BIA Disabled BLC Enabled	VBIOS-Default Both BLC & BIA Disabled BLC Enabled.
BIA Control	<b>VBIOS-Default</b> BIA Disabled BIA Enabled at Level1 BIA Enabled at Level2 BIA Enabled at Level3 BIA Enabled at Level4 BIA Enabled at Level5	VBIOS-Default BIA Disabled BIA Enabled at Level1 BIA Enabled at Level2 BIA Enabled at Level3 BIA Enabled at Level4 BIA Enabled at Level5
TV Standard	<b>VBIOS-Default</b> NTSC PAL SECAM SMPTE240M ITU-R television SMPTE295M SMPTE296M EIA-770.2 EIA-770.3	VBIOS-Default NTSC PAL SECAM SMPTE240M ITU-R television SMPTE295M SMPTE296M EIA-770.2 EIA-770.3
Spread Spectrum	<b>Disabled</b> Enabled	Disabled Enabled
Boot Display Preferences	<b>Auto</b> PORT-0: CRT PORT-1: LVDS PORT-2: S/DVO-B PORT-2: S/DVO-C CRT + LVDS CRT + S/DVO-B CRT + S/DVO-C LVDS + S/DVO-B LVDS + S/DVO-C S/DVO-B + S/DVO-C Port-4: TV TV + CRT TV + LVDS TV + S/DVO-B TV + S/DVO-C	Auto PORT-0: CRT PORT-1: LVDS PORT-2: S/DVO-B PORT-2: S/DVO-C CRT + LVDS CRT + S/DVO-B CRT + S/DVO-C LVDS + S/DVO-B LVDS + S/DVO-C S/DVO-B + S/DVO-C Port-4: TV TV + CRT TV + LVDS TV + S/DVO-B TV + S/DVO-C

## 6.10.3 Advanced Chipset Settings – South Bridge Chipset Configuration

BIOS SETUP UTILITY		Chipset
<b>South Bridge Chipset Configuration</b>		Disabled
USB Functions	[8 USB Ports]	2 USB Ports
USB Port Configure	[6x6 USB Ports]	4 USB Ports
USB 2.0 Controller	[Enabled]	6 USB Ports
HDA Controller	[Enabled]	8 USB Ports
Audio Jack Sensing	[Auto]	10 USB Ports
SMBUS Controller	[Enabled]	12 USB Ports
Restore on AC Power Loss	[Power on]	<-> Select Screen
		Select Item
		Enter Go to Sub Screen
		F1 General Help
		F10 Save and Exit
		ESC Exit
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Feature	Options	Description
USB Functions	Disabled 2 USB Ports 4 USB Ports 6 USB Ports 8 USB Ports 10 USB Ports 12 USB Ports	Disabled 2 USB Ports (USB0/1 enabled) 4 USB Ports (USB0/1/2/3 enabled) 6 USB Ports (USB0/1/2/3/4/5 enabled) 8 USB Ports (USB0/1/2/3/4/5/10/11 enabled) 10 USB Ports (USB0/1/2/3/4/5//6/7/10/11 enabled) 12 USB Ports (all USB ports enabled)
USB Port Configure	<b>6x6 USB Ports</b> 8x4 USB Ports	<b>6x6 USB Ports</b> 8x4 USB Ports
USB 2.0 Controller	Disabled <b>Enabled</b>	If above function "USB Function" = 10 or 12 USB Ports then USB 2.0 Controller is always enabled
HDA Controller	Disabled <b>Enabled</b>	Disabled Enabled
Audio Jack Sensing	<b>Auto</b> Disabled	Auto: The insertion of audio jacks is auto determined. Disabled: Driver assumes that all jacks are inserted (useful when using Audio pinrow)
SMBUS Controller	<b>Enabled</b> Disabled	Disabled Enabled
Restore on AC Power Loss	Power Off <b>Power On</b> Last State	Power Off Power On Last State

### 6.10.4 Advanced Chipset Settings – ME Subsystem Configuration

```

BIOS SETUP UTILITY
Chipset
ME Subsystem Configuration
    Disabled
    Enabled
BootBlock HECI Message      [Enabled]
HECI Message                 [Enabled]
End of Post S5 HECI Message [Enabled]

ME HECI configuration
    ME-HECI      [Enabled]
    ME-IDER      [Disabled]
    ME-KT        [Disabled]

<->  Select Screen
||   Select Item
Enter Go to Sub Screen
F1   General Help
F10  Save and Exit
ESC  Exit

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```

Feature	Options	Description
BootBlock HECI Message	Disabled <b>Enabled</b>	<b>Disabled</b> Enabled
HECI Message	Disabled <b>Enabled</b>	<b>Disabled</b> Enabled
End of Post S5 HECI Message	Disabled <b>Enabled</b>	Disabled Enabled
ME HECI	Disabled <b>Enabled</b>	Disabled Enabled
ME-IDER	<b>Disabled</b> Enabled	Disabled Enabled
ME-KT	<b>Disabled</b> Enabled	Disabled Enabled

### 6.10.5 Advanced Chipset Settings – VE Subsystem Configuration

```

BIOS SETUP UTILITY
Chipset
VE Subsystem Configuration
VE-VECI [Disabled]
Unhide All Physical HC [Enabled]

Enabled/Disable VECI
Messaging

<-> Select Screen
|| Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit

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```

Feature	Options	Description
VE-VECI	<b>Disabled</b> Enabled	Disabled Enabled
Unhide All Physical HC	Disabled <b>Enabled</b>	Disabled Enabled

## 6.10.6 Advanced Chipset Settings – Spread Spectrum Control

```

BIOS SETUP UTILITY
Chipset
Clock Synthesizer Setting
Options
PLL1 spread [Disabled] Disabled
CLK & 27M_SS spread [Disabled] Enabled

<-> Select Screen
|| Select Item
Enter Go to Sub Screen
F1 General Help
F10 Save and Exit
ESC Exit

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```

Feature	Options	Description
PLL1 spread	<b>Disabled</b> Enabled	Disabled Enabled
CLK & 27M_SS spread	<b>Disabled</b> Enabled	Disabled Enabled

## 6.11 Exit Menu

BIOS SETUP UTILITY						
Main	Advanced	PCIPnP	Boot	Security	Chipset	Exit
<b>Exit Options</b>						Exit system setup after saving the changes.
Save Changes and Exit						F10 Key can be used for this operation.
Discard Changes and Exit						
Discard Changes						
Load Optimal Defaults						
Load Failsafe Defaults						
Halt on invalid Time/Date				[Disabled]		<-> Select Screen    Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit
Secure CMOS				[Disabled]		
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Feature	Options	Description
Save Changes and Exit	Ok Cancel	Exit system setup after saving the changes
Discard Changes and Exit	Ok Cancel	Exit system setup without saving any changes
Discard Changes	Ok Cancel	Discards changes done so far to any of the setup questions
Load Optimal Defaults	Ok Cancel	Load Optimal Default values for all the setup questions
Load Failsafe Defaults	Ok Cancel	Load Failsafe Default values for all the setup questions
Halt on invalid Time/Date	Enabled <b>Disabled</b>	Enabled: System halt if incorrect Date & Time.
Secure CMOS	Enabled <b>Disabled</b>	Enable will store current CMOS in non volatile ram. (For protection of CMOS data in case of battery failure etc.)

## 7 AMI BIOS Beep Codes

### Boot Block Beep Codes:

Number of Beeps	Description
1	Insert diskette in floppy drive A:
2	'AMIBOOT.ROM' file not found in root directory of diskette in A:
3	Base Memory error
4	Flash Programming successful
5	Floppy read error
6	Keyboard controller BAT command failed
7	No Flash EPROM detected
8	Floppy controller failure
9	Boot Block BIOS checksum error
10	Flash Erase error
11	Flash Program error
12	'AMIBOOT.ROM' file size error
13	BIOS ROM image mismatch (file layout does not match image present in flash device)

### POST BIOS Beep Codes:

Number of Beeps	Description
1	Memory refresh timer error.
2	Parity error in base memory (first 64KB block)
3	Base memory read/write test error
4	Motherboard timer not operational
5	Processor error
6	8042 Gate A20 test error (cannot switch to protected mode)
7	General exception error (processor exception interrupt error)
8	Display memory error (system video adapter)
9	AMIBIOS ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory test failed

### Troubleshooting POST BIOS Beep Codes:

Number of Beeps	Troubleshooting Action
1, 2 or 3	Reset the memory, or replace with known good modules.
4-7, 9-11	Fatal error indicating a serious problem with the system. Consult your system manufacturer. Before declaring the motherboard beyond "all hope", eliminate the possibility of interference due to a malfunctioning add-in card. Remove all expansion cards, except the video adapter. <ul style="list-style-type: none"> <li>• If beep codes are generated when all other expansion cards are absent, consult your system manufacturer's technical support.</li> <li>• If beep codes are not generated when all other expansion cards are absent, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem happens again. This will reveal the malfunctioning card.</li> </ul>
8	If the system video adapter is an add-in card, replace or reset the video adapter. If the video adapter is an integrated part of the system board, the board may be faulty.

## 8 OS Setup

Use the Setup.exe files for all relevant drivers. The drivers can be found on KTQ45 Driver CD or they can be downloaded from the homepage <http://www.kontron.com/>

## 9 Warranty

KONTRON Technology warrants its products to be free from defects in material and workmanship during the warranty period. If a product proves to be defective in material or workmanship during the warranty period, KONTRON Technology will, at its sole option, repair or replace the product with a similar product. Replacement Product or parts may include remanufactured or refurbished parts or components.

### The warranty does not cover:

1. Damage, deterioration or malfunction resulting from:
  - A. Accident, misuse, neglect, fire, water, lightning, or other acts of nature, unauthorized product modification, or failure to follow instructions supplied with the product.
  - B. Repair or attempted repair by anyone not authorized by KONTRON Technology.
  - C. Causes external to the product, such as electric power fluctuations or failure.
  - D. Normal wear and tear.
  - E. Any other causes which does not relate to a product defect.
2. Removal, installation, and set-up service charges.

### Exclusion of damages:

KONTRON TECHNOLOGY LIABILITY IS LIMITED TO THE COST OF REPAIR OR REPLACEMENT OF THE PRODUCT. KONTRON TECHNOLOGY SHALL NOT BE LIABLE FOR:

1. DAMAGE TO OTHER PROPERTY CAUSED BY ANY DEFECTS IN THE PRODUCT, DAMAGES BASED UPON INCONVENIENCE, LOSS OF USE OF THE PRODUCT, LOSS OF TIME, LOSS OF PROFITS, LOSS OF BUSINESS OPPORTUNITY, LOSS OF GOODWILL, INTERFERENCE WITH BUSINESS RELATIONSHIPS, OR OTHER COMMERCIAL LOSS, EVEN IF ADVISED OF THEIR POSSIBILITY OF SUCH DAMAGES.
2. ANY OTHER DAMAGES, WHETHER INCIDENTAL, CONSEQUENTIAL OR OTHERWISE.
3. ANY CLAIM AGAINST THE CUSTOMER BY ANY OTHER PARTY.