Modular Computers®

CP304

3U CompactPCI
Pentium® III Based CPU Board

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The product described in this manual is in compliance with all applied CE standards.

Revision History

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01	Initial Issue	00	Apr. 2002
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Imprint

Modular Computers®

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This manual was realized by: **TPD/Engineering, PEP Modular Computers GmbH**.

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Explanation of Symbols

CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section “Applied Standards” in this manual.

Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.

Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.

Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.

Note...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

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Your new *PEP* product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new *PEP* product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.

Caution, Electric Shock!

Before installing your new PEP product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks.

Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

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In order to maintain PEP's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by *PEP Modular Computers* and described in this manual or received from PEP Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please, consult the special handling and unpacking instruction on the previous page of this manual.

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If the customer's eligibility for warranty has not been voided, in the event of any claim, he may return the product at the earliest possible convenience to the original place of purchase, together with a copy of the original document of purchase, a full description of the application the product is used on and a description of the defect. Pack the product in such a way as to ensure safe transportation (see our safety instructions).

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Chapter 1

Introduction

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1. Introduction

1.1 System Overview

The CompactPCI board described in this manual operates with the PCI bus architecture to support additional I/O and memory-mapped devices as required by various industrial applications. For detailed information concerning the CompactPCI standard, please consult the complete Peripheral Component Interconnect (PCI) and CompactPCI Specifications. For further information regarding these standards and their use, visit the homepage of the *PCI Industrial Computer Manufacturers Group (PICMG)*.

Many system-relevant CompactPCI features that are specific to *PEP* Modular Computers CompactPCI systems may be found described in the *PEP* CompactPCI System Manual. Due to its size, this manual cannot be downloaded via the internet. Please refer to the section “Related Publications” at the end of this chapter for the relevant ordering information.

The CompactPCI System Manual includes the following information:

- Common information that is applicable to all system components, such as safety information, warranty conditions, standard connector pinouts etc.
- All the information necessary to combine PEP’s racks, boards, backplanes, power supply units and peripheral devices in a customized CompactPCI system, as well as configuration examples.
- Data on rack dimensions and configurations as well as information on mechanical and electrical rack characteristics.
- Information on the distinctive features of PEP CompactPCI boards, such as functionality, hotswap capability. In addition, an overview is given for all existing PEP CompactPCI boards with links to the relating datasheets.
- Generic information on the PEP CompactPCI backplanes, such as the slot assignment, PCB form factor, distinctive features, clocks, power supply connectors and signalling environment, as well as an overview of the PEP CompactPCI standard backplane family.
- Generic information on the PEP CompactPCI power supply units, such as the input/output characteristics, redundant operation and distinctive features, as well as an overview of the PEP CompactPCI standard power supply unit family.

1.2 PEP Single-Height CPU Boards

1.2.1 Intel® Pentium® III Processor Family for the PGA370 Socket

The CP304 is an advanced 32-bit / 33 MHz CompactPCI system controller board designed to utilize all Intel® Pentium® III processors in the FC-PGA and FC-PGA2 sockets and also future processors. The board is based on the Intel® 815-B0 and CICH Communications Controller Hub (CICH) chipset. The CP304 can be configured with processors ranging from the entry-level 566 MHz Celeron® through to the 1266 MHz Pentium III processor with 512 KB L2 cache (whose development names were “Tualatin” and “Pentium III-S”).

1.2.2 Ultra Low Voltage Intel Pentium III Processor Family

The CP303 is an advanced 64-bit / 33 MHz CompactPCI system controller board designed to utilize the Ultra Low Voltage Intel Pentium III (whose development names were “Tualatin” and “Processor-M™”). The board is based on the Intel 815-B0 chipset and can support CPU speeds of 800 MHz through 1200 MHz and host bus speeds up to 133 MHz.

1.2.3 Intel Mobile Pentium III Family

The CP302 is a high performance 64-bit/ 33 MHz CompactPCI system controller board designed to utilize the Intel Mobile Pentium III (whose development name was “Coppermine”). This board is based on the Intel 440BX AGP chipset and can support CPU speeds of 400 MHz through 700 MHz and host bus speeds up to 100 MHz.

The CP301 is a system controller which is identical to the CP302 in every respect except that it has a different 4HP front panel interface. The CP301 supports two COM ports and one Fast Ethernet connector on the 4HP interface. The USB and keyboard connector are not available on the 4HP version.

The CP302-PM is a peripheral master which is identical to the CP302 apart from having a different PCI/PCI (non-transparent) bridge at J1/J2. This makes possible the addition of further CP302-PM’s together with a system controller CPU on one CompactPCI bus, i.e. multiprocessing.

1.3 Board Overview

1.3.1 Board Introduction

The CP304 is designed around the Intel® Pentium® III processor for the FC-PGA and FC-PGA2 socket family and the Intel 815-B0 and CICH Communications Controller Hub (CICH) chipset. The board can be configured with processors ranging from the entry-level 566 MHz Celeron® through to the 1266 MHz Pentium III processor with up to 512 kB L2 cache and processor system bus speed up to 133 MHz.

The CP304 offers more features and expandability than other CompactPCI boards in its class.

The board comes with two onboard Ultra ATA/100 interfaces, up to two 10BASE-T/100BASE-TX Fast Ethernet ports, both integrated in the chipset (82559 style) and a built-in Intel 3D Graphics accelerator for enhanced graphics performance with either a VGA-CRT or a VGA-DVI interface.

The board supports one SODIMM socket for flexible memory upgrading up to 512 MB and also a 32-bit/33 MHz CompactPCI interface.

Designed for stability, the board fits into all applications situated in industrial environments making it a perfect core technology for long life applications.

Components have been selected from embedded technology programs and therefore assure long term availability.

The board is compatible with the Microsoft® Windows® 2000 and Windows® XP operating systems. However, the performance of CompactPCI can be tailored to suit real-time applications and operating systems such as Linux® or VxWorks®, which are instrumental to the success of CompactPCI in these market sectors.

1.3.2 Board-Specific Information

The CP304 is a CompactPCI Pentium® III processor based single-board computer specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

Some of the CP304's outstanding features are:

- Intel® Pentium® III socket 370 FC-PGA/FC-PGA2 microprocessor up to 1266 MHz
- Up to 512 kB L2 cache on-die, running at CPU speed
- 133 MHz processor system bus
- 82815-B0 GMCH and 82801 CICH chipset
- Up to 512 MB SDRAM memory
- Integrated 3D high performance VGA controller
- Analog and digital display support up to 1600 x 1200 x 8-bit
- Two Fast Ethernet interfaces
- Two EIDE Ultra ATA/100 interfaces
- Optional onboard CompactFlash type II socket or 2.5” hard disk
- Two USB 1.1 ports
- Compatible with CompactPCI Spec. Rev. 3.0
- 2 MB on-board flash (1 MB for BIOS and 1 MB for VxWorks®)
- Integrated Hardware Monitor
- Watchdog timer
- Two COM ports
- I/O extension connector (LPC)
- Several rear I/O configurations
- Jumperless board configuration
- Passive heatsink solution

1.4 Optional Modules

1.4.1 CP-RIO3-01 Rear I/O Module

Designed for use with a 32-bit rear I/O variant of the CP304 and a backplane with system slot rear I/O capability, this module provides rear I/O interfacing for the two standard RS232 serial interfaces and one of the two Fast Ethernet interfaces and also an EIDE port.

See Appendix A for more details.

1.4.2 CP-RIO3-02 Rear I/O Module

Designed for use with a 32-bit rear I/O variant of the CP304 and a backplane with system slot rear I/O capability, this module provides rear I/O interfacing for the two standard RS232 serial interfaces and two Fast Ethernet interfaces. This module does not support the baseboard EIDE port.

See Appendix B for more details.

1.5 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the CP304.

Table 1-1: System Relevant Information

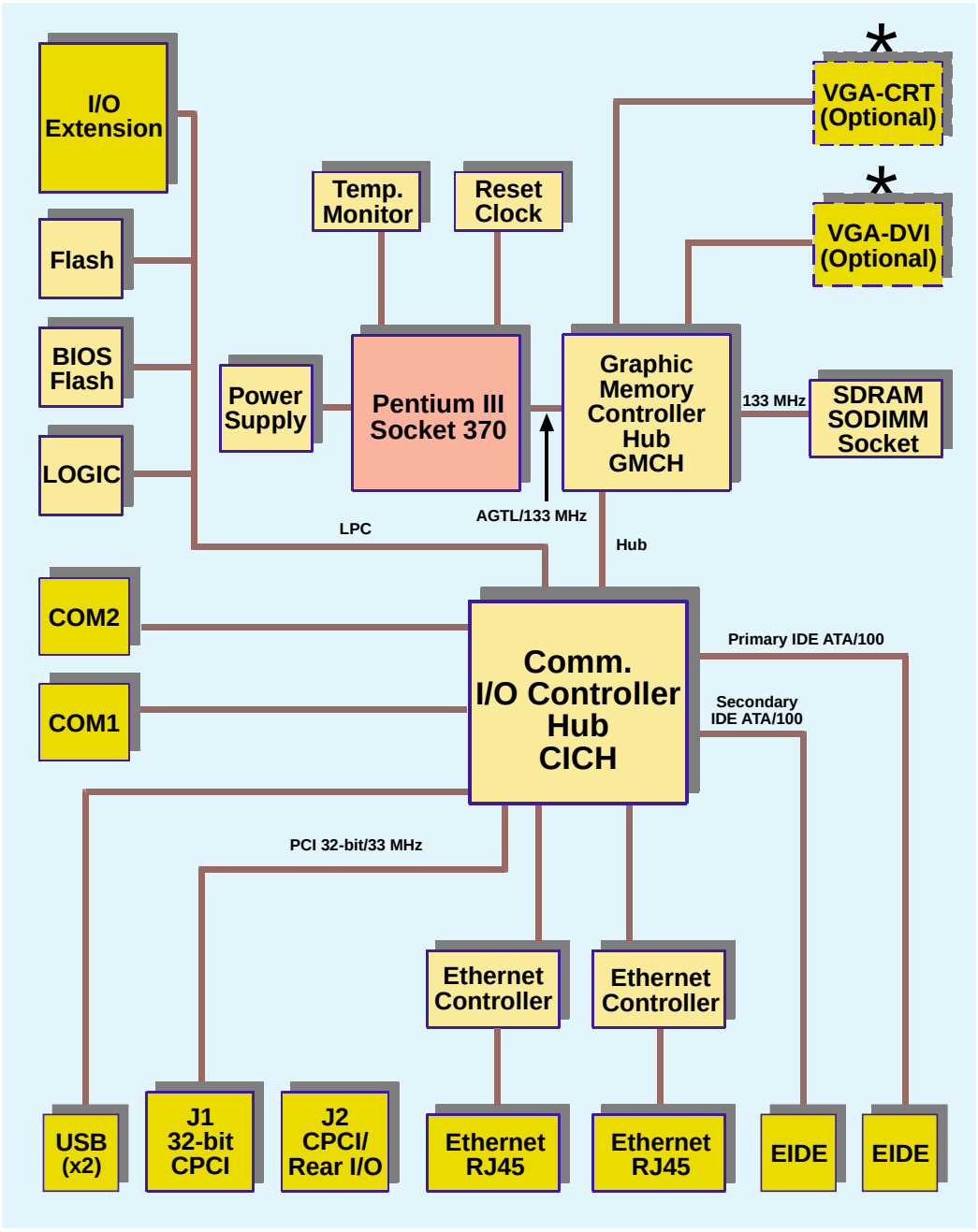
SUBJECT	INFORMATION
System Configuration	A CP304 system master board can support up to 7 peripheral boards with 32-bit and 33 MHz.
System Slot/Peripheral Slot Functionality	The CP304 can operate only as a system master board.
Board Location in the System	The CP304 board must be installed in a system slot of a CompactPCI backplane.
Hotswap Compatibility	The CP304 supports the addition or removal of other boards whilst in a powered-up state. Individual clocks for each slot and ENUM signal handling are in compliance with the PICMG 2.1 Hotswap specification.
Hardware Requirements	The CP304 can be installed in any CompactPCI 3U rack.
Operating Systems	The CP304 can operate under the following operating systems: Microsoft® Windows® 2000 and Windows® XP, Linux®, VxWorks® plus others

1.6 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

1.6.1 Functional Block Diagram

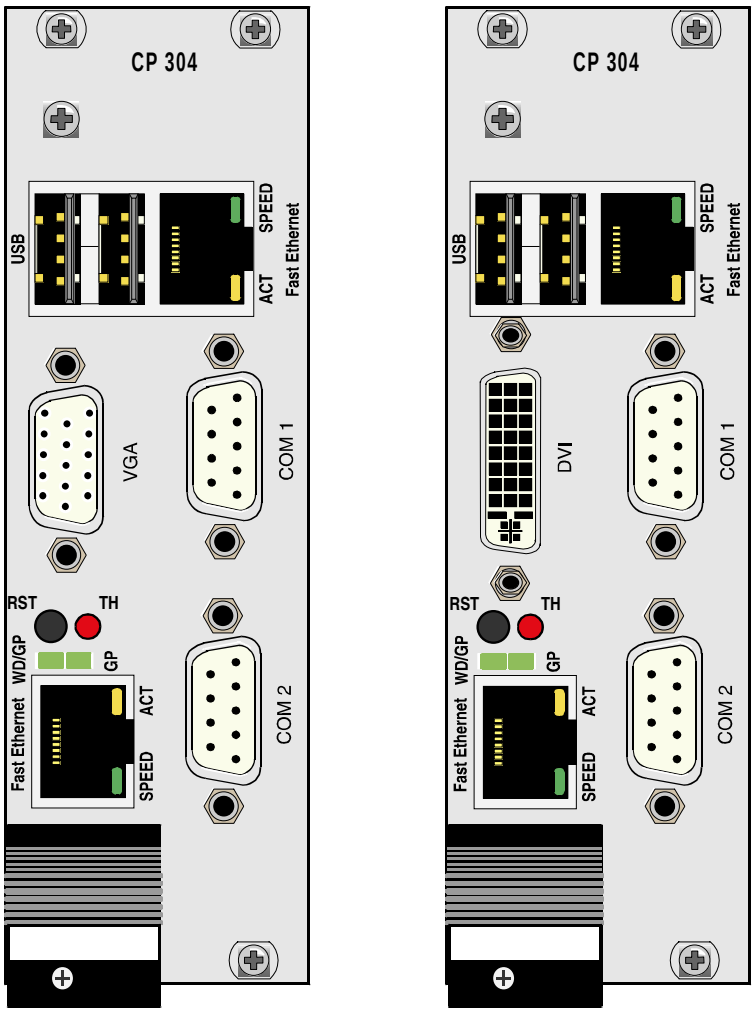
Figure 1-1: CP304 Functional Block Diagram



* either VGA-DVI or VGA-CRT port

1.6.2 Front Panels

Figure 1-2: CP304 8HP Front Panels



LEGEND:

Left CP304: 8HP VGA version

Right CP304: 8HP DVI version

General Purpose LED's

- WD/GP (green): Watchdog or General Purpose
- GP (green): General Purpose
- TH (red): Overtemperature Status

Integral Ethernet LED's

- ACT (yellow): Ethernet Link/Activity
- SPEED (green): Ethernet Speed

1.6.3 Board Layout

Figure 1-3: CP304 Board Layout (Front View)

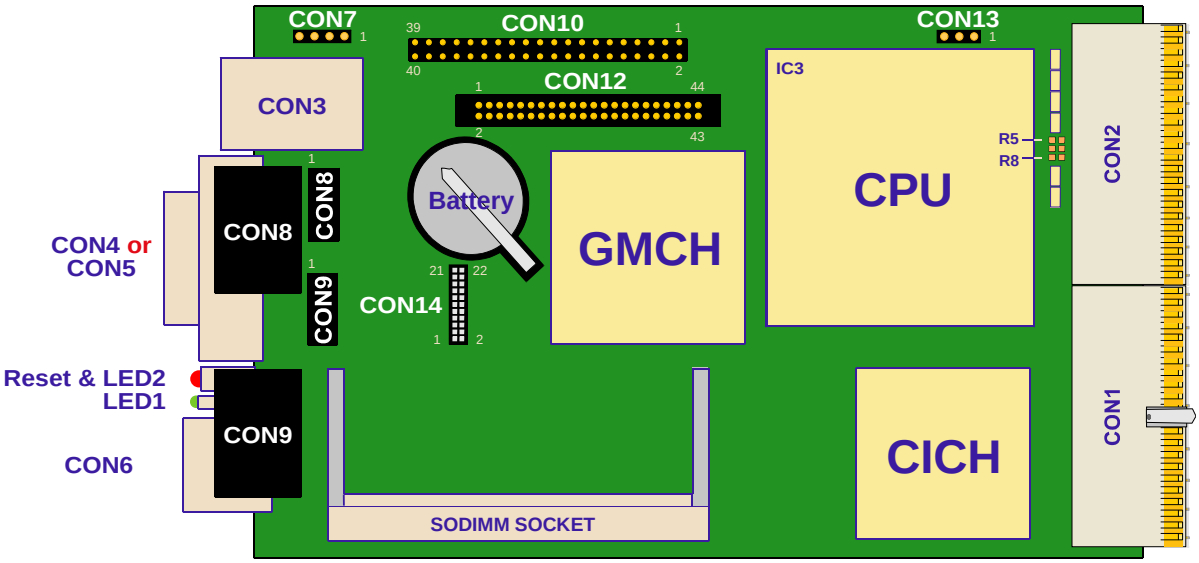
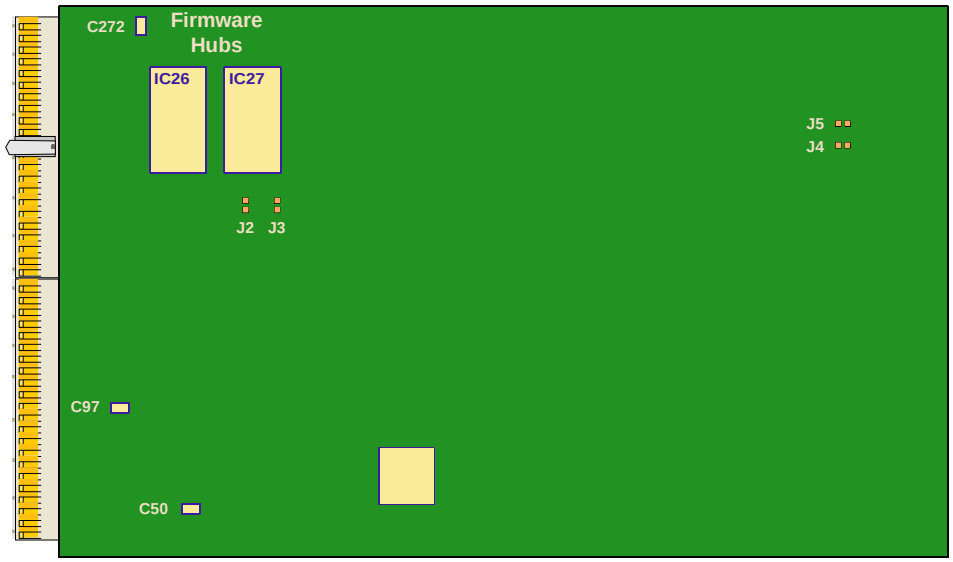


Figure 1-4: CP304 Board Layout (Reverse View)



1.7 Technical Specifications

Table 1-2: CP304 8HP Version Main Specifications

	CP304	Specifications
Processor and Memory	CPU	All Intel® PGA370 socket Pentium® III and Celeron® processor Pentium III up to 1000 MHz with 256 kB L2 on-die cache in 370 FC-PGA packaging Celeron up to 850 MHz with 128 kB L2 on-die cache in 370 FC-PGA packaging Pentium III up to 1266 MHz with 512 kB L2 on-die cache in 370 FC-PGA2 packaging Celeron up to 1200 MHz with 256 kB L2 on-die cache in 370 FC-PGA2 packaging
	Memory	Main Memory: up to 512 MB SDRAM via one SODIMM socket running at up to 133 MHz Cache structure: up to 512 kB L2 on-die full speed processor cache Flash Memory: 1 MB Flash for BIOS and 1 MB Flash extension Memory Extension: Optional CompactFlash socket type II (true IDE mode) EEPROM: Two 256 byte EEPROM's for storing CMOS data when operating without battery and two 256 byte EEPROM's for user purposes
Chipset	Intel® 815-B0 Graphics Memory Controller Hub Chipset	Support for a single Pentium III microprocessor 64-bit AGTL/AGTL+ based System Bus interface at 66/100/133 MHz 64-bit System Memory interface with optimized support for SDRAM at 133 MHz Integrated 2D and 3D Graphics Engines Integrated H/W Motion Compensation Engine Integrated 230 MHz DAC Integrated Digital Video Out Port AGP 1X/2X/4X Controller
	Intel® Communications I/O Controller Hub	PCI Rev. 2.2 compliant with support for 32-bit/33 MHz PCI operations Power management logic support Enhanced DMA controller, interrupt controller, and timer functions Integrated IDE controller Ultra ATA/100/66/33 USB host interface with one host controller; supports 2 USB ports Two Integrated LAN controllers (82559 style) System Management Bus (SMBus) compatible with most I^2C™ devices Low Pin Count (LPC) interface Firmware Hub (FWH) interface support Two UART's, 16C550 compatible

Table 1-2: CP304 8HP Version Main Specifications (cont'd)

	CP304	Specifications
External Interfaces	VGA interface	Built-in Intel 3D Graphics accelerator for enhanced graphics performance. Supports resolutions of up to 1600 x 1200 x 8-bit colors at a 75 Hz refresh rate or 1280 x 1024 x 24-bit true colors at an 85 Hz refresh rate. Hardware motion compensation for software MPEG2 and MPEG4 decoding. The graphics controller provides flexible allocation of video memory up to 6 MB. 15-pin D-sub VGA-CRT connector or 29-pin DVI-I connector with analog and digital signals.
	Fast Ethernet Interface	Dual channel ethernet integrated within the CICH (82559 style) Data rate: 10 & 100 MBit/s Ethernet: Full 802.2 & 802.3 IEEE compliance supporting 10Base-T and 100Base-TX. Cabling: Category 5 two-pair cabling
	USB Interface	The CICH contains one USB 1.1 UHCI compliant host controller with a data transfer rate of up to 12 Mbit/s. The host controller includes a root hub with two separate USB ports.
	Serial Ports	Two UART's, 16C550 compatible.
	CompactPCI Bus Interface	Compatible with CompactPCI Specification V 2.0, Rev. 3.0 32-bit/33 MHz master interface 3.3V/5.0V compatible (default configuration 5.0 V)
	Hotswap Compatible	The CP304 supports the addition or removal of other boards whilst in a powered-up state. Individual clocks for each slot and Enumeration signal handling are in compliance with the PICMG 2.1 Hotswap Specification.
	Rear I/O	When the rear I/O is enabled the CompactPCI interface is configured for 32-bit/33 MHz. The 32-bit CompactPCI bus has rear I/O capability. The following interfaces are routed to the rear I/O connector J2: COM1 and COM2 (TTL signaling), 2xUSB's, CRT VGA, 2xEthernets, EIDE port and general purpose signals.
General	Dimensions, Operating Temperatures, Weight	Dimensions: 100 mm x 160 mm Operating temp.: 0°C to +60°C Storage temp.: -55°C to +85°C Operating humidity: 0% to 95% non-condensing Weight: CP304 8HP with heatsink: 400 grams

Table 1-2: CP304 8HP Version Main Specifications (cont'd)

	CP304	Specifications
Interfaces	Front Panel Interfaces - 8HP VGA-CRT Version	VGA: 15-pin D-sub connector USB: two 4-pin connectors COM: two 9-pin D-sub connectors Ethernet: two RJ45 connectors Two LED's yellow: (integrated in Ethernet RJ45 jack): Ethernet Link/Activity Two LED's green: (integrated in Ethernet RJ45 jack): Ethernet Speed Two LED's green: Watchdog or General Purpose One LED red: Overtemperature Status Reset button, guarded
	Front Panel Interfaces - 8HP VGA-DVI Version	VGA: 29-pin DVI-I connector USB: two 4-pin connectors COM: two 9-pin D-sub connectors Ethernet: two RJ45 connectors Two LED's yellow: (integrated in Ethernet RJ45 jack): Ethernet Link/Activity Two LED's green: (integrated in Ethernet RJ45 jack): Ethernet Speed Two LED's green: Watchdog or General Purpose One LED red: Overtemperature Status Reset button, guarded
	Onboard interfaces	Two EIDE interfaces supporting Ultra ATA/100/66/33 for up to four devices (hard disks or CD-ROM's) on a 40-pin 2.54mm connector and a 44-pin 2.0mm connector. I/O extension connector
Hardware Monitoring	Thermal Management/ System Monitoring	Watchdog: software configurable watchdog generates IRQ, NMI or hardware reset. Hardware monitor: LM81 monitoring temperature, fan speed and all onboard voltages. Temperature monitor: MAX 1617 monitoring the CPU on-die and board temperature.
	Common Features	DC power monitors (3.3V and 5V) Battery socket and 3.0V lithium battery for RTC, suitable types: VARTA Type CR2025 PANASONIC BR2020

Table 1-2: CP304 8HP Version Main Specifications (cont'd)

	CP304	Specifications
Software	Software BIOS and Operating System Support	Award BIOS within 1 MB of Flash memory and having the following features: - Award Preboot Agent included; this allows BIOS updates and service functions without VGA or a local disk - LAN-boot capability for diskless systems - Boot from USB floppy and CD-ROM - BIOS boot support for USB keyboards - Software enable/disable function for the rear I/O, Ethernet and COM port configuration - Plug&Play capability - Dual BIOS support - The BIOS parameters are saved in the EEPROM - Board serial number within the EEPROM - PC Health Monitoring, which allows you to protect your system from problems even before they occur Operating systems supported: Linux®, VxWorks®, Windows®2000, Windows®XP, plus others

1.8 Software Support

Real-time operating systems such as VxWorks and others are supported. The standard PC features supported by the BIOS also allow for PC operating systems such as Linux®, MS-DOS®, Windows® 2000 and Windows® XP.

1.8.1 Windows® 2000, Windows® XP

The Microsoft® platforms Windows® 2000 and Windows® XP are rapidly gaining popularity as the solution for embedded application requirements, such as medical systems, industrial automation and, in network devices, routers and switches.

In addition to being a modern, powerful 32-bit operating system platform, Windows® provides a number of unique advantages not found in any other embedded operating system.

The familiar Windows® Win32® API, with its associated broad range of development tools and knowledge base, provides a broad base of development talent, tools, and expertise.

Windows® also offers comprehensive networking support and connectivity to non-embedded and enterprise information systems.

For systems with advanced operator interfaces, there is also the familiar Windows Graphical User Interface (GUI).

A major benefit of the Windows operating system in embedded applications is the ability to leverage existing off-the-shelf software components, either those in Windows itself or components from a wide range of third party developers.

Embedded system designers who create applications that maximize the use of existing components, and minimize the number of software components that must be written, will realize the lowest development costs and fastest time to market.

1.8.2 WindRiver®: VxWorks®, RTOS

Tornado was originally designed to solve the problems inherent in a cross-development environment, such as limited host-target communication, limited target resources, and poorly integrated tools. With Tornado® II, WindRiver® built upon the Tornado® framework, focusing developer time-to-productivity.

VxWorks®, the run-time component of the Tornado® II embedded development platform, is the most widely adopted real-time operating system (RTOS) in the embedded industry.

Tornado II also includes a comprehensive suite of core and optional cross-development tools and utilities and a full range of communications options for the target connection to the host.

The flexible VxWorks® RTOS comprises the core capabilities of the WindRiver microkernel along with advanced networking support, powerful file system and I/O management and C++ and other standard run-time support (more than 1800 powerful application program interfaces (HPIS)).

These core capabilities can be combined with add-on components available from WindRiver® Systems and PEP Modular Computers GmbH (e.g. VxWorks driver support for various PEP CompactPCI boards).

The VxWorks is designed for scalability, enabling developers to allocate scarce memory resources to their application, rather than to the operating system. From deeply embedded designs requiring a few kilobytes of memory, to complex high-end real-time systems where more operating system functions are needed, the developer may choose from over 100 different options to create hundreds of configurations. Individual modules may be used in development and omitted in production systems.

Furthermore, these individual subsystems are themselves scalable, allowing the developer to optimally configure VxWorks run-time software for the widest range of applications. Additionally, TCP, UDP, sockets, and standard Berkeley network services can all be scaled in or out of the networking stack as necessary.

These configuration options may be easily selected by means of the Tornado II project facility´s graphical interface.

1.8.3 Other Operating Systems

Contact *PEP* for information on other operating systems.

1.8.4 *PEP* Support

PEP is one of the few CompactPCI and VME vendors providing inhouse support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software manufacturers, *PEP* is able to produce and support BSP’s and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

Finally, customers possessing a maintenance agreement with *PEP* can be guaranteed hotline software support and are supplied with regular software updates. A dedicated website is also provided for online updates and release downloads.

1.9 Environmental Considerations

1.9.1 Absolute Maximum Electrical Ratings

Absolute Maximum Ratings indicate limits beyond which damage to the board may occur. Do not operate the CP304 at or beyond these maximum values.

Table 1-3: Voltage Limits

Supply Voltage	Maximum Permitted Value
3.3 V	+4.5 V
5 V	+5.5 V
+12 V	+14 V
-12 V	-14 V

1.9.2 DC Operating Characteristics

The following table sets out the voltage parameters within which the board is functional. The CP304 cannot be guaranteed to function if the board is not operated within the prescribed limits.

Table 1-4: Voltage Range

Supply Voltage	Limit
3.3 V	3.20 V min. to 3.47 V max.
5 V	4.85 V min. to 5.25 V max.
+12 V	11.4 V min. to 12.6 V max.
-12 V	-11.4 V min. to -12.6 V max.

1.9.3 Power Consumption

The goal of this description is to provide a method to calculate the power consumption for the CP304 base board and for additional configurations. The processor dissipates the majority of the thermal power.

The power consumption tables below list the voltage and current specifications for the CP304 board and the CP304 accessories. The values were measured using an 8-slot passive CompactPCI backplane with two power supplies, one for the CPU and the other for the hard disk. During measurement the power consumption of the backplane was ignored. The operating system used was Windows® 2000. All measurements were conducted at a temperature of 25°C. The measured values varied, because power consumption was dependent on processor activity.

Table 1-5: Power Consumption, Windows® 2000 IDLE Mode

	P III 1.4 GHz 256 MB	P III 1.26 GHz 256 MB	P III 1 GHz 256 MB	P III 866 MHz 256 MB	Celeron® 1.4 GHz 256 MB	Celeron 1.2 GHz 256 MB	Celeron 566 MHz 256 MB
Core Voltage	1.45 V	1.45 V	1.75 V	1.75 V	1.45 V	1.45 V	1.75 V
5 V	21.1 W	13.8 W	6.8 W	3.4 W	20.0 W	13.7 W	5.1 W
3.3 V	6.8 W	6.5 W	6.4 W	6.0 W	6.5 W	6.2 W	6.4 W
Total	27.9 W	20.3 W	13.2 W	9.4 W	26.5 W	19.9 W	11.5 W

Note...

The above values were measured with no application started and without keyboard.

Table 1-6: Power Consumption, Windows® 2000, 100% CPU usage (Game: 3D-Pinball)

	P III 1.4 GHz 256 MB	P III 1.26 GHz 256 MB	P III 1 GHz 256 MB	P III 866 MHz 256 MB	Celeron® 1.4 GHz 256 MB	Celeron 1.2 GHz 256 MB	Celeron 566 MHz 256 MB
Core Voltage	1.45 V	1.45 V	1.75 V	1.75 V	1.45 V	1.45 V	1.75 V
5 V	25.7 W	17.5 W	26 W	18.5 W	24.0 W	16.4 W	13.1 W
3.3 V	7.1 W	6.7 W	7 W	7 W	7.0 W	7 W	7 W
Total	32.8 W	24.2 W	33 W	25.5 W	31.0 W	23.4 W	20.1 W

Table 1-7: Power Consumption, Windows® 2000, 100% CPU usage (High Power Tool)

	P III 1.4 GHz 256 MB	P III 1.26 GHz 256 MB	P III 1 GHz 256 MB	P III 866 MHz 256 MB	Celeron® 1.4 GHz 256 MB	Celeron 1.2 GHz 256 MB	Celeron 566 MHz 256 MB
Core Voltage	1.45 V	1.45 V	1.75 V	1.75 V	1.45 V	1.45 V	1.75 V
5 V	31.4 W	22.8 W	34 W	25.5 W	29.9 W	22.2 W	16.6 W
3.3 V	6.9 W	6.6 W	6.5 W	6.1 W	6.5 W	6.2 W	6.4 W
Total	38.3 W	29.4 W	40.5 W	31.6 W	36.4 W	28.4 W	23.0 W

Note...

The above values are with Windows® 2000 running with 100% CPU usage, the INTEL HiPower tool started and without keyboard.

Analysis indicates that real applications do not reach the maximum possible power consumption of the HiPower tool, the maximum power consumption is 20 - 30% lower than the measured value.

Table 1-8: Power Consumption Table for CP304 Accessories

Module	Power 5V	Power 3.3V
Keyboard	100 mW	--

1.9.4 Temperature Range and Air Flow

These values are measured using typical applications running under Windows® 2000. In worst case situations, the values vary and the temperature range must be reduced. In all situations the maximum case temperature of the Pentium® III processor must be below the maximum temperature value. This temperature value can be measured with the onboard remote temperature sensor. To guarantee the maximum temperature, the BIOS supports a temperature control feature. In instances of overtemperature the hardware monitor will reduce the processor clock speed to reduce power consumption.

Figure 1-5: Temperature Range and Air Flow Chart for FC-PGA processors (Coppermine Core)

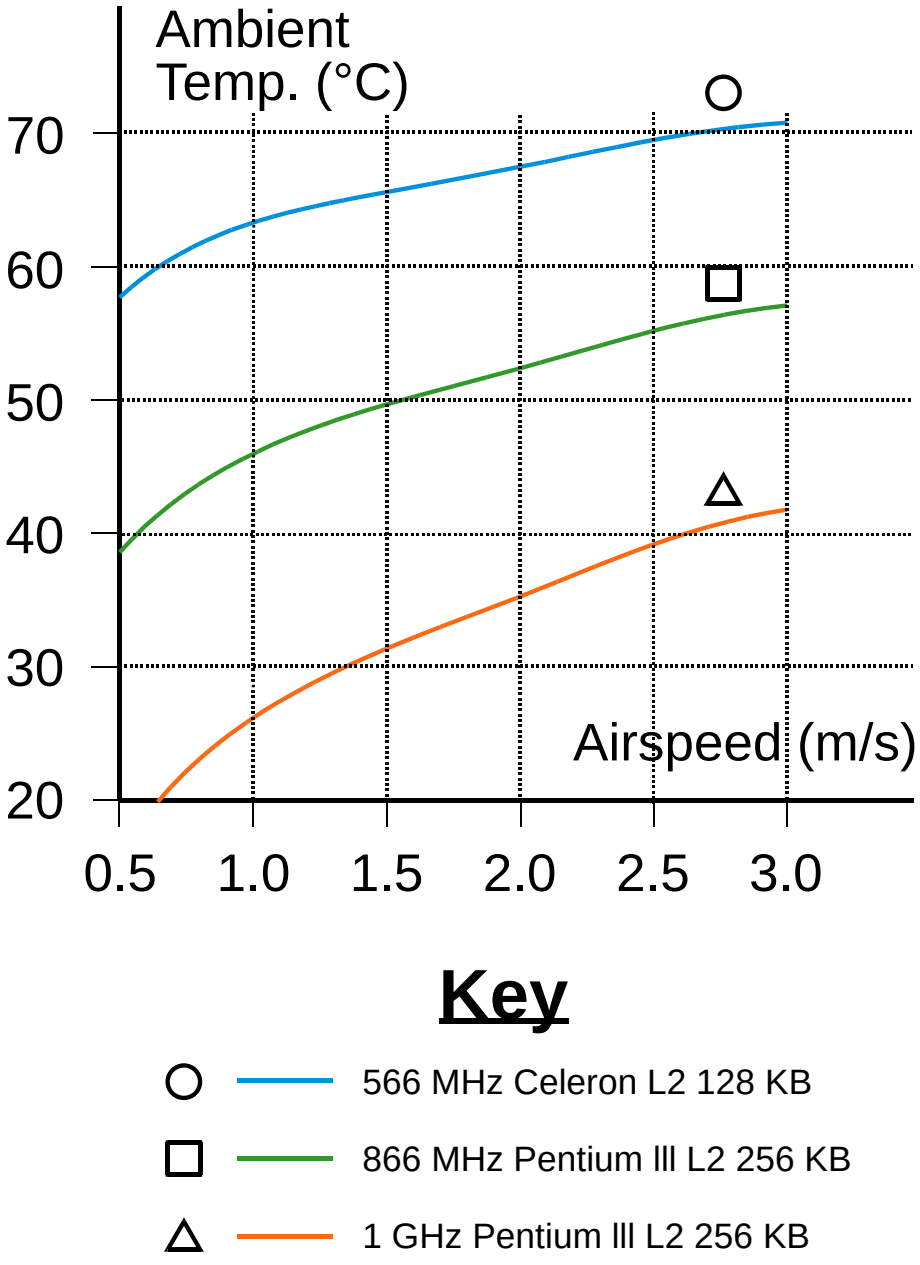
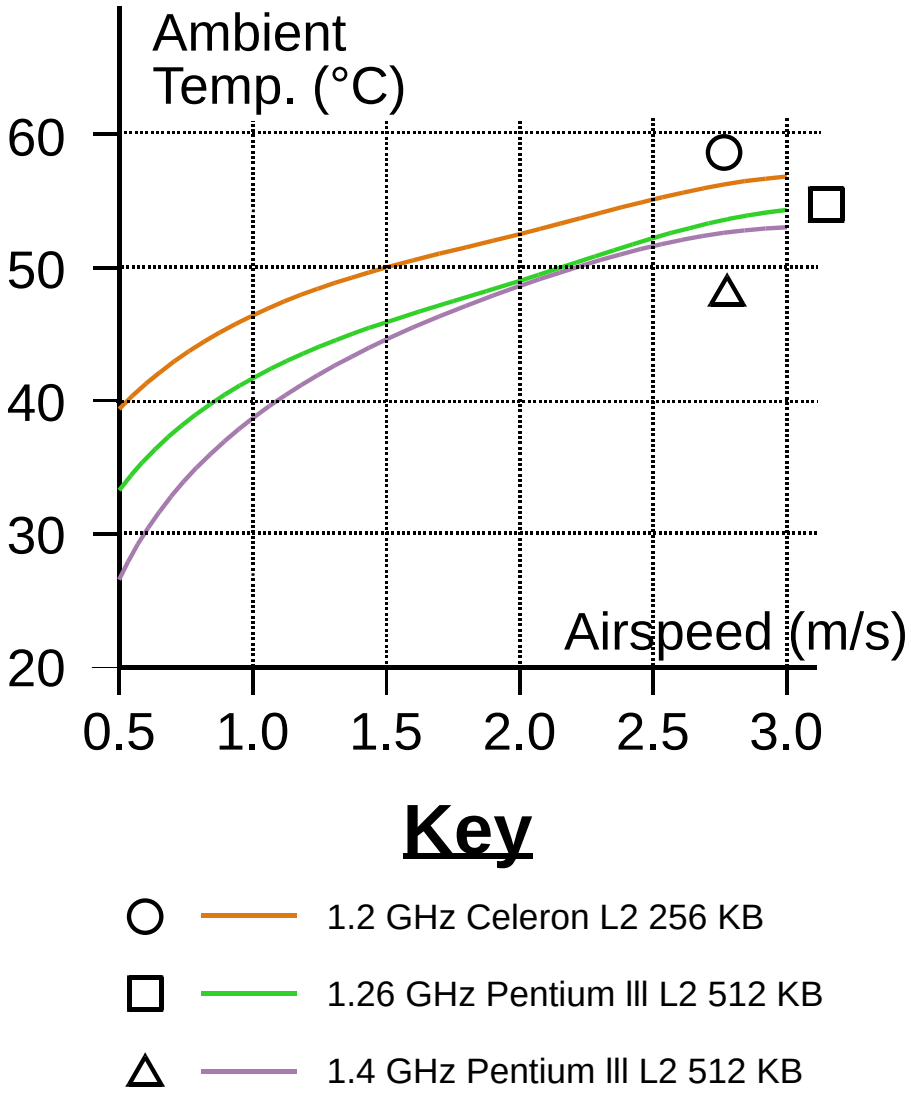


Figure 1-6: Temperature Range and Air Flow Chart for FC-PGA2 Processors (Tualatin Core)



Warning!

The temperature ranges detailed above assume that any appended hard disk is capable of operating at these temperatures. The user must ensure that any appended hard disk can function at the operating temperatures expected.

0 m/s air flow means standard convection cooling with the board in an upright position. An airflow of 1 - 1.2 m/s is a typical value for a standard *PEP* ASM 4 rack (3U CompactPCI rack with 1U cooling fans). For other racks or housings the available airflow will differ. The maximum ambient temperature must be recalculated and/or measured for such environments. For the calculation of the maximum ambient temperature the processor junction (case) temperature must never exceed the values indicated in the table below. The maximum heatsink temperature depends on the physical characteristics of the heatsink and thermal connection to the processor. To ensure that the heatsink temperature does not exceed its limits an airflow may be needed for a given ambient temperature. Heatsink temperature is measured at the top of the heatsink base, closest to the processor .

Table 1-9: Maximum CPU Temperature

	P III 1.4 GHz	P III 1.26 GHz	P III 1 GHz	P III 866 MHz	Celeron® 1.4 GHz	Celeron 1.2 GHz	Celeron 566 MHz
Maximum T-junction Temperature	--	--	70°C	80°C	--	--	90°C
T-junction Offset	--	--	3.8°C	3.4°C	--	--	2.6°C
Maximum Case Temperature	69°C	69°C	--	--	69°C	69°C	--

Warning!

It is the responsibility of the end user to ensure that the processor junction temperate never exceeds the maximum T-junction temperature in order to protect the board against overheating. Permanent overheating can damage the board.

If the temperature on the processor junction is greater than the maximum T-junction temperature, the maximum ambient temperature must be reduced or an external airflow must be provided by means of an additional fan.

Warning!

Due care should be exercised when handling the board due to the fact that the heatsink can get very hot. Do not touch the heatsink when changing the board.

Note...

The BIOS supports a temperature control function, If the temperature is too high, the sensors automatically reduce the CPU clock frequency, depending on the mode chosen in the BIOS setup.

1.9.5 Storage Temperatures

- Storage temperature without hard disk –55°C to +85°C
- Storage temperature with hard disk –40°C to +65°C
- Humidity non-condensing 0% to 95% at +40°C

1.10 Applied Standards

The *PEP Modular Computers'* CompactPCI systems comply with the requirements of the following standards:

Table 1-10: Applied Standards

COMPLIANCE	TYPE	STANDARD	Test Level (Ruggedized Version)
CE	Emission	EN50081-1	--
	Immission	EN50082-2	--
	Electrical Safety	EN60950	--
Mechanical	Mechanical Dimensions	IEEE 1101.10	--
Environmental Aspects	Vibration (Sinusoidal)	IEC68-2-6	2g/12-300Hz/10 acceleration / frequency range / test cycles
	Random Vibration (Broadband)	IEC68-2-64 (3U boards)	20-500Hz,0.1g²/500-2000Hz, 0.01g²/7g rms/3/30min frequency range1 / frequency range2 /acceleration / cycle / duration
	Permanent Shock	IEC68-2-29	15g/11ms/3000/1s peak acceleration / shock duration half sine / number of shocks / recovery time
	Single Shock	IEC68-2-27	30g/9ms/18/5s peak acceleration / shock duration / number of shocks / recovery time in seconds

1.11 Related Publications

The following publications contain information relating to this product.

Table 1-11: Related Publications

PRODUCT	PUBLICATION
CompactPCI Systems and Boards	CompactPCI Specification 2.0, Rev. 3.0
	Hotswap Specification PICMG 2.1
	PEP Modular Computers' CompactPCI System Manual, ID 19954
CompactFlash Cards	CF+ and CompactFlash Specification Revision 1.4

1.12 Trademarks

- CompactPCI is a trademark of the PCI industrial Computers Manufacturers Group
- Ethernet is a registered trademark of Xerox Corporation
- IEEE is a registered trademark of the Institute of Electrical and Electronics Engineers Inc.
- VxWorks is a registered trademark of WindRiver Systems Inc.
- Intel is a trademark of Intel Corporation
- Pentium III is a trademark of Intel Corporation
- Microsoft is a trademark of the Microsoft corporation
- Other trademarks are the property of their respective owners

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Chapter 2

Functional Description

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2. Functional Description

2.1 CPU, Memory and Chipset

2.1.1 CPU

The CP304 supports all Intel® Pentium® III and Celeron® processors in the FC-PGA and FC-PGA2 sockets. The Intel Pentium III microprocessors offer exceptional performance coupled with low power consumption. This processor is based on the same core as existing Intel processors. Key performance features include Internet Streaming SIMD instructions and a processor system bus speed of 133 MHz.

The processor includes a maximally integrated on-die 512 KB 8-way set associative level-two (L2) cache.

The L2 cache implements the Advanced Transfer Cache Architecture with a 256-bit wide bus. The processor also includes a 16 KB level one (L1) instruction cache and 16 KB L1 data cache. These cache arrays run at the full speed of the processor core. Memory is cacheable for 64 GB of addressable memory space, allowing significant headroom for desktop systems. The processor speed is automatically selected and the onboard voltage regulator is automatically programmed by the processor's VID pins to provide the required voltage. The CP304 is available with a variety of Intel processors as set out in the following table.

Table 2-1: Supported Intel® Processors on the CP304

Processor	Package	Technology	Speed	L2 Cache	Core Voltage	Processor Side Bus
Celeron®	FC-PGA	0.18u	566 MHz	128 kB	1.75 V	66 MHz
Celeron	FC-PGA2	0.13u	1200 MHz	256 kB	1.45 V	100 MHz
Pentium® III	FC-PGA	0.18u	866 MHz	256 kB	1.75 V	133 MHz
Pentium III	FC-PGA	0.18u	1000 MHz	256 kB	1.75 V	133 MHz
Pentium III	FC-PGA2	0.13u	1266 MHz	512 kB	1.45 V	133 MHz
Plus future Intel® Pentium III microprocessors with 133 MHz processor side bus						

Note...

Use only the processors listed above. Use of unsupported processors can damage the board, the processor, and the power supply. The PPGA Celeron® Processors are NOT supported.

2.1.2 Memory

The board supports a maximum of 512 MB. To enable the flexible updating of memory a SODIMM socket is provided. All installed memory will be automatically detected, so there is no need to set any jumpers. All PC/133 compliant SDRAM's on 144-pin SODIMM's are supported by the CP304 board.

All memory components and SODIMM's used with this board must comply with the following PC SDRAM specifications:

- PC SDRAM Specification PC133
- PC Serial Presence Detect Specification

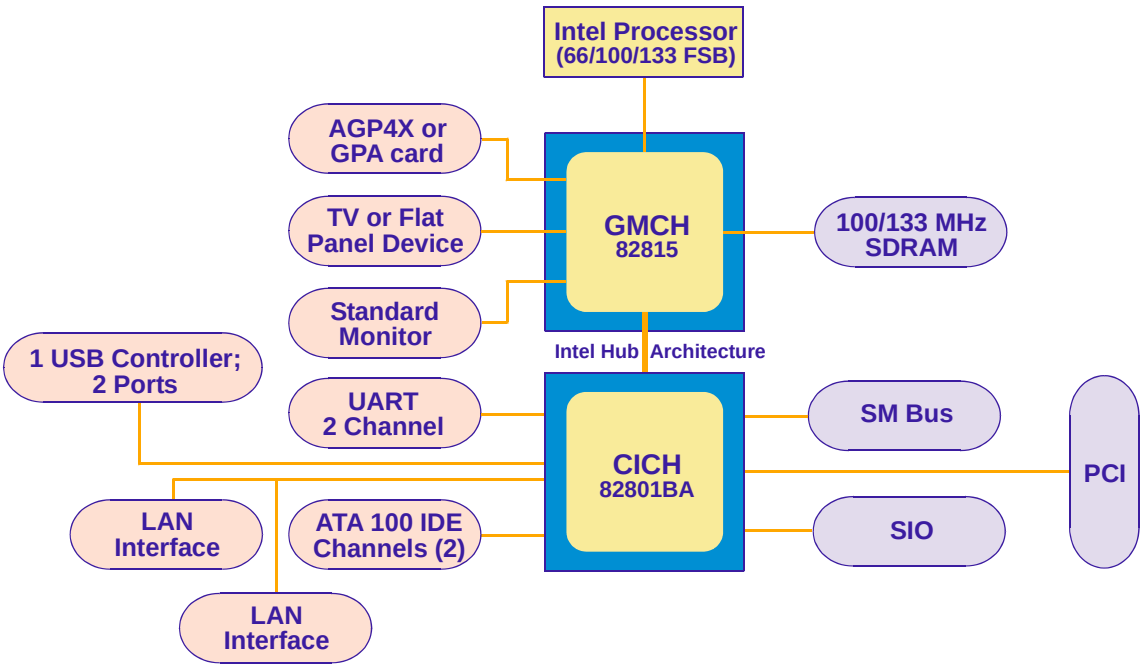
2.1.3 815-B0 Chipset Overview

The Intel® 815-B0 chipset consists of the following devices:

- 82815-B0 Graphics and Memory Controller Hub (GMCH) with Accelerated Hub Architecture (AHA) bus
- 82802 I/O Communication Controller Hub (CICH) with AHA bus
- 82802 Firmware Hub (FWH)

The GMCH provides the processor interface for the Pentium® III microprocessor, the memory bus, the AGP 4x bus in the case of an external graphics controller, and includes a high performance graphics accelerator. The CICH is a centralized controller for the boards' I/O peripherals, such as the PCI, USB, EIDE, LAN and UART ports. The Firmware Hub FWH provides the non-volatile storage of the BIOS.

Figure 2-1: 815-B0 Chipset Functional Block Diagram:



2.1.4 Graphics and Memory Controller Hub (815-B0)

The 815-B0 Graphics Memory Controller Hub (GMCH) is a highly integrated hub that provides the CPU interface (optimized for the Intel® Pentium® III microprocessor), the SDRAM system memory interface, a hub link interface to the CICH and an AGP interface for an external VGA controller or internal graphics.

2.1.4.1 Graphics and Memory Controller Hub Feature Set

Host Interface

The 815-B0 is optimized for Intel® Pentium® III microprocessors. The chipset supports a Processor Side Bus (PSB) frequency of 133 MHz using 1.25V AGTL signaling. Single-ended AGTL termination is supported for single processor configurations. It supports 32-bit host addressing for decoding up to 4 GB of memory address space.

System Memory Interface

The 815-B0 integrates a system memory SDRAM controller with a 64-bit wide interface without ECC. The chipset supports PC133 Single Data Rate (SDR) SDRAM for system memory.

AGP Interface

The 815-B0 supports 1.5V AGP 4x devices with a maximum data transfer of 1066 MB/s and sideband addressing. If the internal graphics controller is enabled the AGP port cannot be used. If an AGP card is installed in the system, the 815-B0 internal graphics will be disabled and the AGP controller will be enabled.

815-B0 Graphics Controller

The 815-B0 includes a highly integrated graphics accelerator and H/W Motion Compensation engines for software MPEG2 decoding, delivering high performance 2D and 3D video capabilities. The internal graphics controller provides interfaces to a standard progressive scan monitor, TV-Out device, and TMDS transmitter. These interfaces are only active when running in internal graphics mode.

2.1.5 Communications I/O Controller Hub (CICH)

The Communications I/O Controller Hub (CICH) is a highly integrated multifunctional I/O controller hub that provides the interface to the PCI bus and integrates many of the functions required in today's PC platforms. The CICH communicates with the host controller over a dedicated hub interface.

2.1.5.1 Communications I/O Controller Hub Feature Set

Feature Set:

- PCI 2.2 interface with eight IRQ inputs
- Bus Master EIDE controller: UltraDMA 100/66/33
- One USB controller with up to two USB 1.1 ports
- Hub interface to 815-B0
- FWH interface
- LPC interface
- Two integrated LAN controllers; 82559 style
- Two UART's; 16550 style
- RTC controller

2.1.6 Interrupts

Two enhanced 8259-style interrupt controllers provide a total of fifteen interrupt inputs with features which include level and edge-triggered inputs, fixed and rotating priorities and individual input masking. Interrupt sources include: counter/timers, serial I/O, RTC, keyboard/mouse, printer, floppy disk, EIDE interfaces and four interrupt sources on the CompactPCI backplane.

2.2 Peripherals

The following standard peripherals are available on the CP304 board:

2.2.1 Timer

- Real-Time Clock

  The ICH2 contains a MC146818A-compatible real-time clock with 256 bytes of battery-backed RAM.

  The real-time clock performs timekeeping functions and includes 256 bytes of general purpose battery-backed CMOS RAM. Features include an alarm function, programmable periodic interrupt and a 100-year calendar. All battery-backed CMOS RAM data remains stored in an additional EEPROM. This prevents data loss.

- Counter/Timer

  Three 8254-style counter/timers are included on the CP304 as defined for the PC/AT.

2.2.2 Watchdog Timer

A watchdog timer is provided, which forces either an IRQ5, NMI, or Reset condition (configurable in the watchdog register). The watchdog time can be programmed in 12 steps ranging from 125 msec up to 256 seconds. If the watchdog timer is enabled, it cannot be stopped.

2.2.3 Battery

The CP304 is provided with a 3.0V “coin cell” lithium battery for the RTC.

To replace the battery please proceed as follows:

- Turn off power
- Remove the battery
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. Suitable batteries include the VARTA CR2025 and
PANASONIC BR2020

Important notes concerning the battery appear on the next page

Important:

Care must be taken to ensure that the battery is correctly replaced.

The battery should be replaced only with an identical or equivalent type recommended by the manufacturer.

Dispose of used batteries according to the manufacturer's instructions.

The typical life expectancy of a 170 mAh battery (VARTA CR2025) is 5 - 6 years with an average on-time of 8 hours per working day at an operating temperature of 30°C. However, this typical value varies considerably because the life expectancy is dependent on the operating temperature and the standby time (shutdown time) of the system in which it operates.
To ensure that the lifetime of the battery has not been exceeded it is recommended to exchange the battery after 4 - 5 years.

2.2.4 Reset

The CP304 is automatically reset by a precision voltage monitoring circuit that detects a drop in voltage below the acceptable operating limit of 4.725 V for the 5 V line and below 3.0 V for the 3.3 V line, or in the event of a power failure of the DC/DC converter. Other reset sources include the watchdog timer and the local push-button switch. The CP304 responds to any of these sources by initializing local peripherals.

A reset will be generated by the following conditions:

- +5 V supply falls below 4.75 V
- +3.3 V supply falls below 3.0 V
- +1.8 V supply falls below 1.5 V
- Power failure of the DC/DC converter for the processor
- Pushbutton "RESET" pressed
- Watchdog overflow
- CompactPCI backplane PRST input

2.2.5 SMBus Devices

The CP304 provides a System Management Bus (SMBus) for access to several system monitoring and configuration functions. The SMBus consists of a two-wire I²C™ bus interface. The following table describes the function and address of every onboard SMBus device.

Table 2-2: SMBus Device Addresses

Device	SMBus Address
Temperature Sensor MAX1617	0011000Xb
Hardware Monitor LM81	0101100Xb
EEPROM	1010XXXXb

2.2.6 Thermal Management / System Monitoring

The LM81 can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds and temperatures; all of which are very important for the proper operation and stability of a high-end computer system. The LM81 provides an I²C™ serial bus interface.

The voltages of the onboard power supply, which are: +12 V, -12 V, +5 V, +3.3 V, +1.5 V, and the battery voltage are supervised. Two fan tachometer outputs can be measured using the LM81's FAN1 and FAN2 inputs.

The integrated MAX1617 temperature sensors monitor the CPU temperature and the ambient temperature around the CPU to make sure that the system is operating at a safe temperature level. If the temperature is too high, the sensors automatically reduce the CPU clock frequency, depending on the mode chosen in the BIOS set. Thermal management operations are controlled by the ICH2 hub and settings are available in the BIOS.

2.2.7 Serial EEPROM

A serial EEPROM is provided, organised into 4 blocks with 256 bytes per block (24LC08). This EEPROM is connected to the I²C™ bus provided by the ICH2.

Table 2-3: EEPROM Address Map

Address	Function
1010000xb	Reserved
1010001xb	Reserved
1010010xb	Reserved
1010011xb	Reserved
1010100xb	VxWorks® parameter
1010101xb	Free for user purposes
1010110xb	Free for user purposes
1010111xb	CMOS backup and board serial number

It is strongly recommended that users access only the two free EEPROM banks

2.2.8 FLASH Memory

There are three flash devices available as described below, one for the BIOS, one onboard flash and one CompactFlash socket.

2.2.8.1 BIOS FLASH (Firmware Hub)

For simple BIOS updating a standard onboard 1 MB Firmware Hub device in a 40-pin TSSOP package is used. The Firmware Hub (FWH) interface consists of a 5-signal communication interface which is used to control the operation of the device in a system environment. The buffers for this interface were designed to be PCI compliant. The FWH interface is equipped to operate at 33 MHz, synchronous with the PCI bus.

The FWH stores both the system BIOS and video BIOS. It can be updated as new versions of the BIOS become available. You may easily upgrade your BIOS using the AWARD *awdflash* utility .

2.2.8.2 User FLASH

For small flash extensions an additional 1 MB Firmware Hub flash memory is available. Due to the new chipset generation with the Low Pin Count interface the flash block is not mapped in the first 1 MB memory block as on the BX based CPU boards, instead it is mapped in the extended memory area, i.e. 0xFFF00000-0xFFF7FFFF.

2.2.8.3 Dual BIOS

Dual BIOS means that there are two chips for the BIOS on the CP304 board (BIOS Flash and the User Flash). One chip is intended to be a backup in case the other gets corrupted. These chips are soldered to the board.

If the primary BIOS is corrupted due to physical damage or a faulty flash upgrade, the solder jumper J2 must be set; the system will switch over to the secondary chip and boot with default settings.

Note...

The Dual BIOS feature cannot be used if the second Flash chip is used for VxWorks®

2.3 Board Interfaces

2.3.1 General Purpose LED Output

The CP304 provides two software programmable GP LED's. After a reset the default configuration for the two GP LED's is "Overtemperature" and "Watchdog status". The LED's can be configured via two onboard registers. For more information please see Chapter 4.

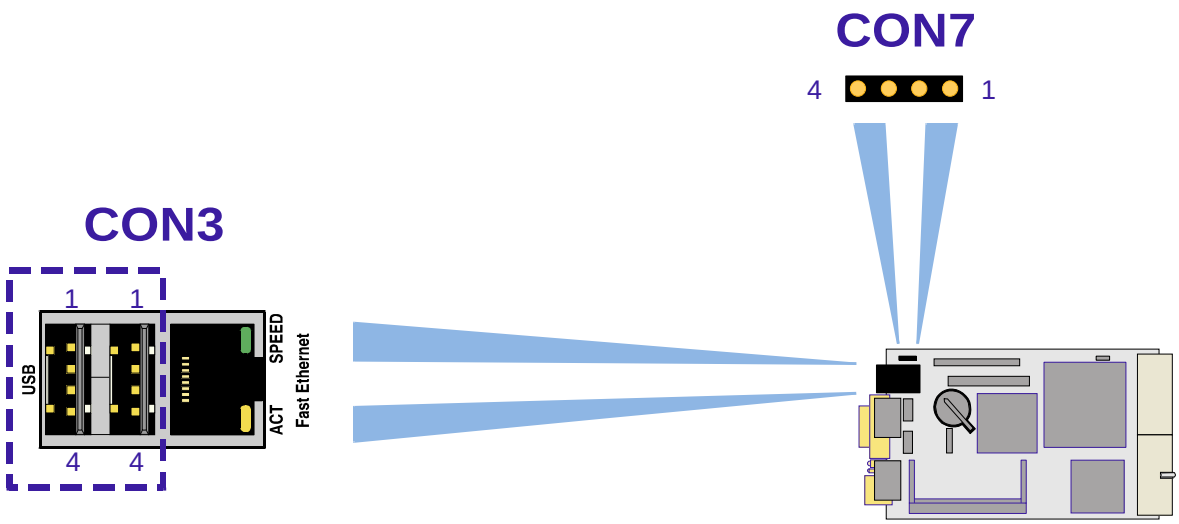
The LED control logic remains in the state until the next system reset.

2.3.2 USB Interfaces

There are three USB ports on the CP304 board, only two of which may be used at any one time, with the proviso given in the note below. Each USB port has a maximum transfer rate of 12 Mbit. One USB peripheral device may be connected to each port. To connect more than two USB devices an external hub is required.

The USB power supply is protected by a self resetable 500 mA fuse.

Figure 2-2: USB Connectors CON3 and CON7



2.3.2.1 USB Connectors CON3 and CON7 Pinouts

The CP304 has two USB interfaces implemented on a 4-pin connector with the following pinout:

Table 2-4: USB Connector CON3 (External Connection) Pinout

Pin Number	Signal	Function	In/Out
1	VCC	VCC signal	--
2	UV0-	Differential USB-	--
3	UV0+	Differential USB+	--
4	GND	GND signal	--

Table 2-5: USB Connector CON7 (Internal Connection) Pinout

Pin Number	Signal	Function	In/Out
1	VCC	VCC signal	--
2	UV0-	Differential USB-	--
3	UV0+	Differential USB+	--
4	GND	GND signal	--

Note...

The two USB connectors within CON3 and the USB connector CON7 cannot all be used at the same time. The USB connector within CON3, which is adjacent to the Fast Ethernet connector, is electrically identical to the USB connector CON7 and not separated and therefore cannot be used at the same time.

The USB power supply to each USB connector is protected with a fuse (500 mA) and all the signal lines are EMI-filtered.

2.3.3 Graphics Controller

The 815-B0 chipset includes a highly integrated graphics accelerator delivering high performance 2D and 3D video capabilities. The internal graphics controller provides interfaces to a standard progressive scan monitor or a DVI interface.

Integrated 2D/3D Graphics:

- 3-D hyperpipelined architecture
- Full 2-D hardware acceleration
- Intel® i815e D.V.M. Technology graphics core
- Integrated 230 Mhz DAC
- Resolution up to 1280 x 1024 with 16 M colors
- Integrated H/W Motion Compensation engines for software MPEG2 decode

2.3.3.1 Video Memory Usage

The 815-B0 chipset supports the new Dynamic Video Memory Technology (D.V.M.T.). This new technology ensures the most efficient use of all available memory for maximum 3D graphics performance. D.V.M.T. dynamically responds to application requirements, allocating display and texturing memory resources as required.

The operating system requires up to 1 MB of system memory to support legacy VGA. System properties will display up to 1MB less than physical system memory available to the operating system.

The graphics driver for the Intel® 815-B0 configuration will request up to 6 MB of memory from the OS to implement a maximum 1600 x 1200 screen resolution, 2 MB for a command buffer and 4 MB is required for Z-Buffering. When the 3D application is closed, the OS will reallocate system memory back for generic use.

2.3.3.2 Video Resolution

The GMCH supports a wide range of resolutions, color depths, and refresh rates via a programmable dot clock that has a maximum frequency of 230 MHz.

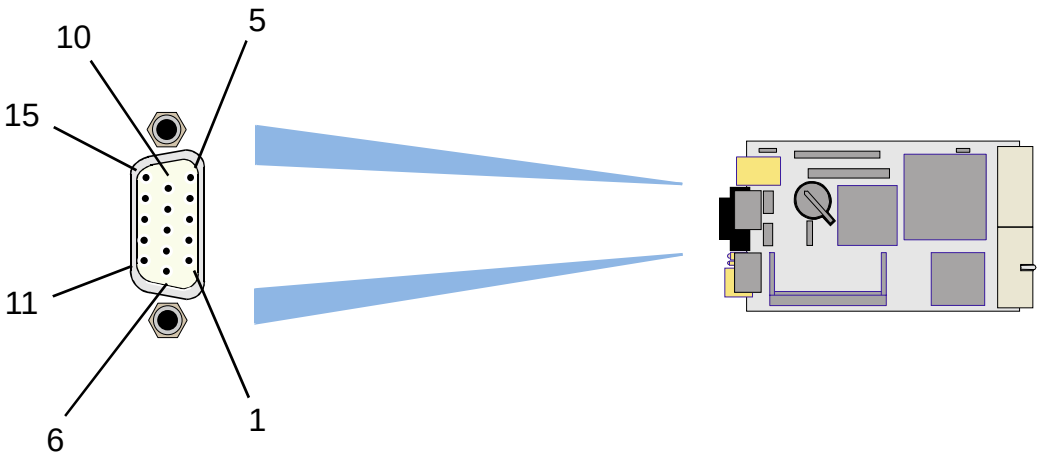
Table 2-6: Partial List of Display Modes Supported

Resolution	Bits per Pixel (frequency in Hz)		
	8-bit indexed	16-bit	24-bit
320x200	70	70	70
320x240	70	70	70
352x480	70	70	70
352x576	70	70	70
400x300	70	70	70
512x384	70	70	70
640x400	70	70	70
640x480	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
720x480	75,85	75,85	75,85
720x576	60,75,85	60,75,85	60,75,85
800x600	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
1024x768	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
1152x864	60,70,72,75,85	60,70,72,75,85	60,70,72,75,85
1280x720	60,75,85	60,75,85	60,75,85
1280x960	60,75,85	60,75,85	60,75,85
1280x1024	60,70,72,75,85	60,70,72,75,85	60,70,75,85
1600x900	60,75,85	60,75,85	--
1600x1200	60,70,72,75	--	--

2.3.3.3 CRT Interface and Connector CON4

(Version of board with VGA-CRT interface)

Figure 2-3: D-sub CRT Connector CON4



The 15-pin female connector CON4 is used to connect a CRT monitor to the CP304 board.

Table 2-7: CRT Connector CON4 Pinout

Pin Number	Signal	Function	In/Out
1	Red	Red video signal output	Out
2	Green	Green video signal output	Out
3	Blue	Blue video signal output	Out
13	Hsync	Horizontal sync.	TTL out
14	Vsync	Vertical sync.	TTL out
12	Sdata	I^2C™ data	In/Out
15	Sclk	I^2C™ clock	Out
9	VCC	Power +5V 200 mA, no fuse protection	Out
5,6,7,8,10	GND	Signal ground	--
4,11	Free	--	--

2.3.3.4 DVI-I Interface and Connector CON5

(Version of board with VGA-DVI interface)

The 29-pin DVI-I female connector CON5 is used to connect an analog or digital monitor to the CP304 board

Figure 2-4: DVI-I Interface Connector CON5

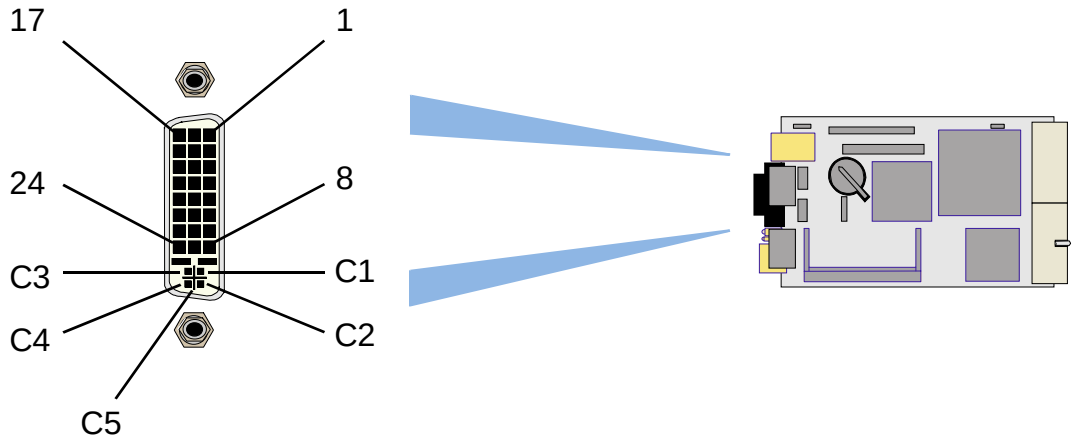


Table 2-8: DVI-I Connector CON5 Pinout

Pin Number	Signal	Function	In/Out
1	T.M.D.S Data 2-	T.M.D.S* Link -	Out
2	T.M.D.S Data 2+	T.M.D.S* Link +	Out
3	Data 2/4 Shield	Data 2/4 Shield	--
4	Free	--	--
5	Free	--	--
6	DDC Clock	I^2C™ Clock	Out
7	DDC Data	I^2C™ Data	In/Out
8	T.M.D.S Data 1-	T.M.D.S Link -	Out
9	T.M.D.S Data 1+	T.M.D.S Link +	Out
10	Data 1/3 Shield	Data 1/3 Shield	--
11	Free	--	--
12	Free	--	--
14	VCC	Power +5 V max. 1.5A	--
15	GND	Signal ground	--
16	Free	--	--
17	T.M.D.S Data 0-	T.M.D.S Link -	Out
18	T.M.D.S Data 0+	T.M.D.S Link +	Out
19	Data 0/5 Shield	Data 0/5 Shield	--
20	free	--	--
21	free	--	--
22	Clock Shield	Clock Shield	--
23	T.M.D.S Clock +	T.M.D.S Link +	Out
24	T.M.D.S Clock -	T.M.D.S Link -	Out
C1	Red	Red video signal output	Out
C2	Green	Green video signal output	Out
C3	Blue	Blue video signal output	Out
C4	Hsync	Horizontal sync. TTL out	Out
C5	Vsync	Vertical sync. TTL out	Out

* T.M.D.S. = Transition Minimized Differential Signaling

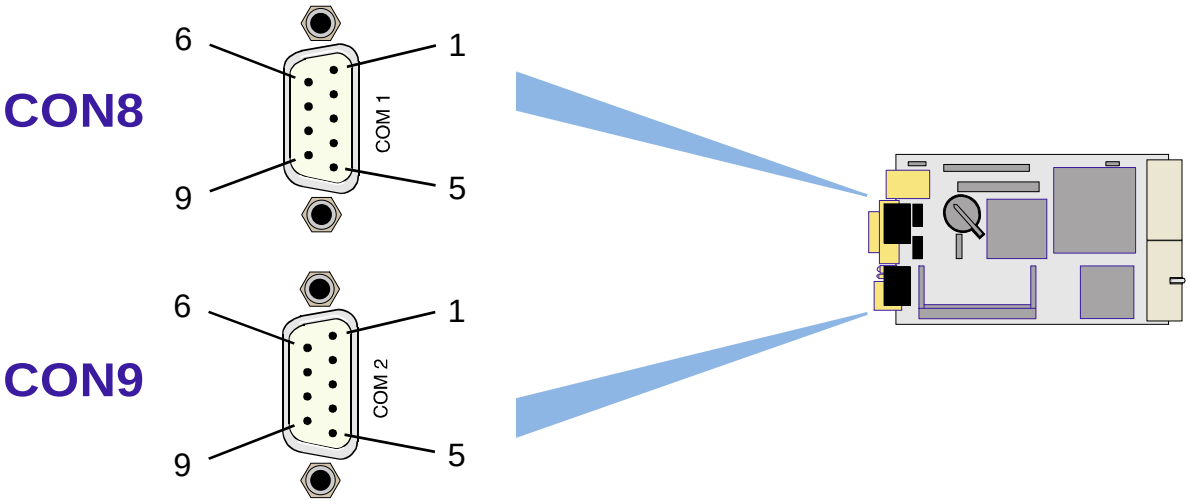
Note...

The CP304 is delivered configured either with the VGA-CRT or VGA-DVI interface and cannot subsequently be reconfigured.

2.3.4 Universal Serial Ports (UART)

2.3.4.1 Serial Port Interface COM1 and COM2

Figure 2-5: PC-Compatible D-sub Serial Connector CON8 (COM1) and CON9 (COM2)



A PC-compatible RS232 serial port is available with 5V charge-pump technology eliminating the need for a +12V and -12V supply. The COM port, which is fully compatible with the 16550 controller, includes a complete set of handshaking and modem control signals, maskable interrupt generation and data transfer of up to 460.8 kB/s.

The serial ports COM1 and COM2 can be enabled/disabled under software control. Selection can be made inside the BIOS or via the rear I/O configuration register. The standard software configuration is front I/O.

2.3.4.2 Serial Port Connector CON8 and CON9 Pinout

Table 2-9: Serial Port Connector CON8 (COM1) and CON9 (COM2) Pinout

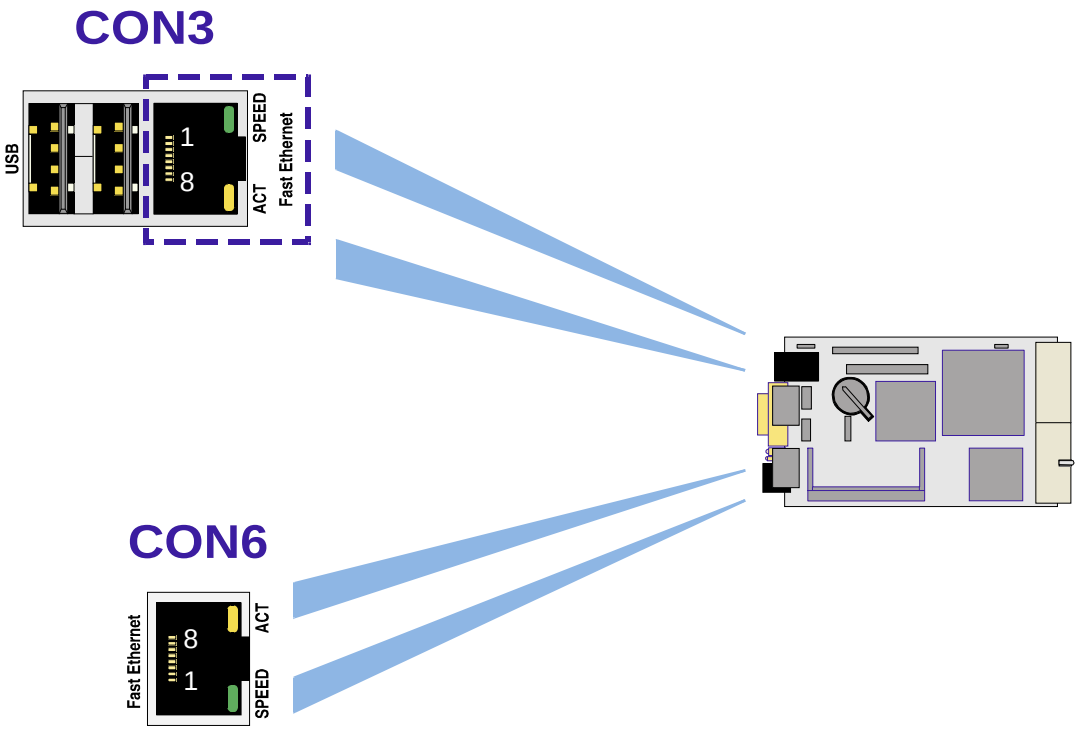
Pin Number	Signal	Function	In/Out
1	DCD	DCD Data carrier detect	In
2	RXD	RXD Receive data	In
3	TXD	TXD Transmit data	Out
4	DTR	DTR Data terminal ready	Out
5	GND	GND Signal ground	--
6	DSR	DSR Data send request	In
7	RTS	RTS Request to send	Out
8	CTS	CTS Clear to send	In
9	RIN	RI Ring indicator	In

2.3.5 Fast Ethernet

The CP304 board includes two 10BASE-T/100BASE-TX Ethernet ports integrated within the CICH chipset (82559 style). The controller contains two receive and transmit FIFO buffers that prevent data overruns or underruns while waiting for access to the PCI bus.

Two LED's monitor network conditions. The Boot from LAN feature is supported, for details please refer to section 5.5, BIOS Features Setup, in chapter 5, CMOS Setup.

Figure 2-6: Fast Ethernet Connectors CON3 and CON6



The Ethernet connectors are realized as RJ45 twisted-pair connectors. The interfaces provide automatic detection and switching between 10Base-T and 100Base-TX data transmission. The two Ethernet channels may be configured via the BIOS setting or the rear I/O Configuration Register for front I/O or rear I/O. The standard software configuration is front I/O.

Fast Ethernet connector pinouts appears on the following page

2.3.5.1 RJ45 Connectors CON3 and CON6 Pinout

The CON3 and CON6 connectors supply the 10Base-TX/100Base-TX interfaces to the Ethernet controller.

Table 2-10: RJ45 Connectors CON3 and CON6 Pinout

Pin Number	Signal	Function	In/Out
1	TX+	Transmit +	Out
2	TX-	Transmit -	Out
3	RX+	Receive +	In
4	NC	--	--
5	NC	--	--
6	RX-	Receive -	In
7	NC	--	--
8	NC	--	--

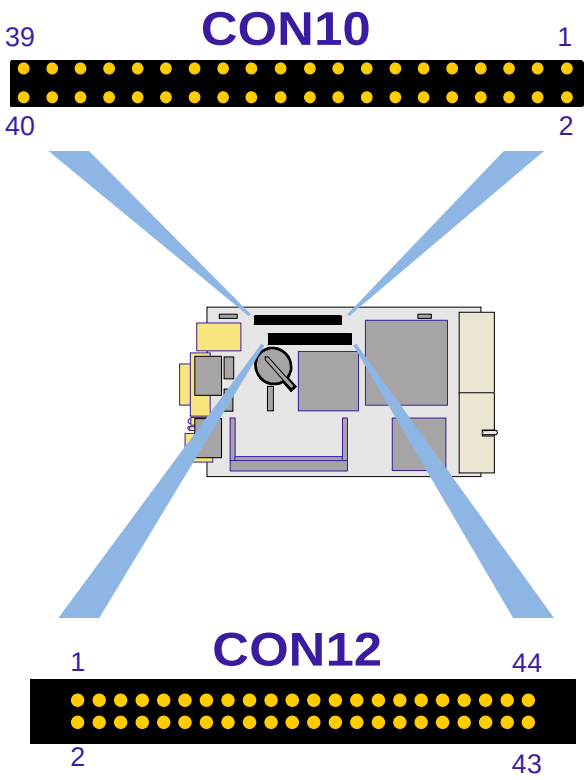
2.3.6 Ethernet LED Status

Yellow: ACT: This LED monitors network connection and activity. The LED lights up when network packets are sent or received through the RJ45 port. When this LED is not lit it means that either the computer is not sending or receiving network data or that the cable connection is faulty.

Green: SPEED: This LED lights up to indicate a successful 100Base-TX connection. When not lit the connection is operating at 10Base-T.

2.3.7 EIDE Interface

Figure 2-7: EIDE Interface Connectors CON10 and CON12



The EIDE interface supports the following modes:

- Programmed I/O (PIO): CPU controls data transfer.
- 8237-style DMA: DMA offloads the CPU, supporting transfer rates of up to 16 MB/sec
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec
- ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to Ultra DMA and is device driver compatible.
- ATA-100: DMA protocol on IDE bus allows host and target throttling. The ICH2 ATA-100 logic can achieve read transfer rates of up to 100 MB/sec and write transfer rates up to 88 MB/sec.

There are two independent EIDE ports available. The primary port is connected to the 44-pin, 2-row male connector. The secondary EIDE interface is a 40-pin, 2-row male connector AT standard interface for an EIDE hard disk.

Each EIDE interface provides support for two devices (one master and one slave) and togethor, therefore, support a maximum of 4 devices. All hard disks can be used in cylinder head sector (CHS) mode with the BIOS also supporting the logical block addressing (LBA) mode.

Note...

ATA-66 and ATA-100 are faster timings and require a specialized cable which has additional grounding wires to reduce reflections, noise, and inductive coupling. This cable will also support all legacy IDE drives.

The blue end of the ATA-100 cable must be connected to the motherboard, the gray connector to the UltraDMA /100 slave device and the black connector to the UltraDMA/100 master device.

EIDE connector pinout appears on the following page

2.3.7.1 Onboard EIDE Connector CON12 Pinout

A 2.5” hard disk or Flash disk may be mounted directly onto the CP304 module using the 44-pin connector CON12.

Table 2-11: Pinout of the AT 44-pin Connector

Pin Number	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	N/C	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--
25	IOR	I/O read	Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	N/C	--	--
33	A1	Address 1	Out
34	ATA66	Detect ATA66	In
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	LED	LED driving	In
40	GND	Ground signal	--
41	VCC	5V power	--
42	VCC	5V power	--
43	GND	Ground signal	--
44	N/C	--	--

2.3.7.2 CON10 (Secondary EIDE Interface) Pinout

The following table sets out the pinout of the CON10 connector, giving the corresponding signal names. The maximum length of cable that may be used is 35 cm.

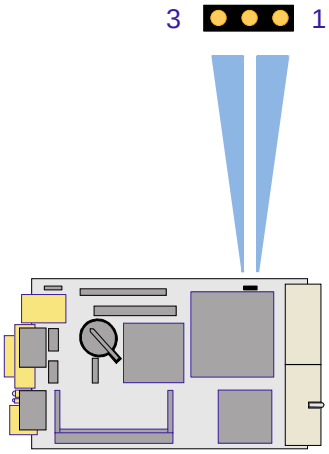
Table 2-12: CON10 (Secondary EIDE) Pinout

Pin Number	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	N/C	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--
25	IOR	I/O read	Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	N/C	--	--
33	A1	Address 1	Out
34	ATA66	Detect ATA66	In
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	LED	LED driving	In
40	GND	Ground signal	--

2.3.8 Fan Power Supply

A fan for CPU cooling may be connected via the power connector CON13.

Figure 2-8: Fan Power Supply Connector CON13



2.3.8.1 Fan Power Supply Connector CON13 Pinout

Table 2-13: Fan Power Supply Connector CON13 Pinout

Pin Number	Signal	Function	In/Out
1	GND	Signal Ground	--
2	+12V	Power	--
3	Sense input	Sense input	In

2.3.9 CompactPCI Bus Interface

The complete CompactPCI connector configuration comprises two connectors named J1 and J2

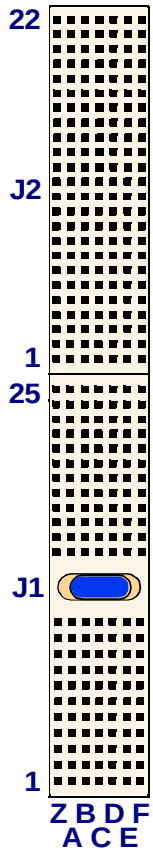
Their function is as follows:

- J1/J2: 32-bit CompactPCI interface with PCI bus signals, arbitration, clock and power
- J2 has optional rear I/O interface functionality.

The board is capable of driving up to seven CompactPCI slots, with individual arbitration and clock signals. In addition to standard CompactPCI system functionality, the CP304 also supports Hotswap capability which means that hotswappable boards can be removed from or installed in the system whilst it is running.

The CP304 is designed for a CompactPCI bus architecture. The CompactPCI standard is electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

Figure 2-9: CPCI Connectors J1/J2



2.3.9.1 CompactPCI Connector Keying

CompactPCI connectors support guide lugs to ensure a correct polarized mating. A proper mating is further assured by the use of color coded keys for 3.3V and 5V operation.

Color coded keys prevent inadvertent installation of a 5V peripheral board into a 3.3V slot. The CP304 board is a 5V version. Backplane connectors are always keyed according to the signaling (VIO) level. Coding key colors are defined as follows:

Table 2-14: Coding Key Colors

Signaling Voltage	Key Color
3.3V	Cadmium Yellow
5V	Brilliant Blue
Universal board (5V and 3.3V)	None

The default setting is indicated by italics.

CompactPCI connector pinouts appear on the following page.

2.3.9.2 CompactPCI Connectors CON1 and CON2 Pinouts

The CP304 is provided with two 2 mm x 2 mm pitch female CompactPCI bus connectors, J1 and J2.

Table 2-15: CompactPCI Bus Connector J1 (CON1) Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
25	5V	REQ64#	ENUM#	3.3V	5V	GND
24	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	3.3V	AD[9]	AD[8]	M66EN#	C/BE[0]#	GND
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	3.3V	IPMB SCL	IPMB SDA	GND	PERR#	GND
16	DEVSEL	GND	V(I/O)	STOP#	LOCK#	GND
15	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
12-14	Key Area					
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	C/BE[3]#	IDSEL (OPEN)	AD[23]	GND	AD[22]	GND
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	REQ0#	GND	3.3V	CLK0	AD[31]	GND
5	BRSVP1A5	BRSVP1B5	RST#	GND	GNT0	GND
4	IPMB PWR	GND	V(I/O)	INTP	INTS	GND
3	INTA#	INTB#	INTC#	5V	INTD#	GND
2	TCK	5V	TMS	TDO	TDI	GND
1	5V	-12V	TRST#	+12V	5V	GND

Table 2-16: 64-bit CompactPCI Bus Connector J2 (CON2) Pinout

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	RSV	RSV	RSV	GND
20	GND	CLK5	GND	RSV	GND	RSV	GND
19	GND	GND	GND	RSV	RSV	RSV	GND
18	GND	RSV	RSV	RSV	GND	RSV	GND
17	GND	RSV	GND	PRST#	REQ6#	GNT6#	GND
16	GND	RSV	RSV	DEG#	GND	RSV	GND
15	GND	RSV	GND	FAL#	REQ5#	GNT5#	GND
14	GND	NC	NC	NC	GND	NC	GND
13	GND	NC	GND	V(I/O)	NC	NC	GND
12	GND	NC	NC	NC	GND	NC	GND
11	GND	NC	GND	V(I/O)	NC	NC	GND
10	GND	NC	NC	NC	GND	NC	GND
9	GND	NC	GND	V(I/O)	NC	NC	GND
8	GND	NC	NC	NC	GND	NC	GND
7	GND	NC	GND	V(I/O)	NC	NC	GND
6	GND	NC	NC	NC	GND	NC	GND
5	GND	NC	GND	V(I/O)	NC	NC	GND
4	GND	V(I/O)	RSV	NC	GND	NC	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

2.3.10 Optional Rear I/O interface on CompactPCI Connector J2

The CP304 board provides optional rear I/O connectivity. Some standard PC interfaces are implemented and assigned to the front panel and to the rear connector J2.

When the rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus the rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the system rear I/O feature a special backplane is necessary. The CP304 with rear I/O is compatible with all standard CompactPCI passive backplanes with rear I/O support on the system slot.

The CP304 rear I/O provides the following interfaces (all signals are available on J2 only when the board is ordered for rear I/O functionality):

Rear I/O version

- 32-bit/33 MHz CompactPCI interface
- Two USB ports
- Two Ethernet ports without LED
- Two COM ports (TTL level)
- CRT VGA port
- EIDE port (primary)
- One fan control input
- One general purpose output
- Input for external backup battery

Note...

The pinouts for one of the ethernets and the USB, COM, EIDE and VGA ports are identical to the CP302 and CP303 pinouts.

2.3.10.1 Rear I/O Configuration Illustration

Figure 2-10: CP304 Rear I/O Configuration

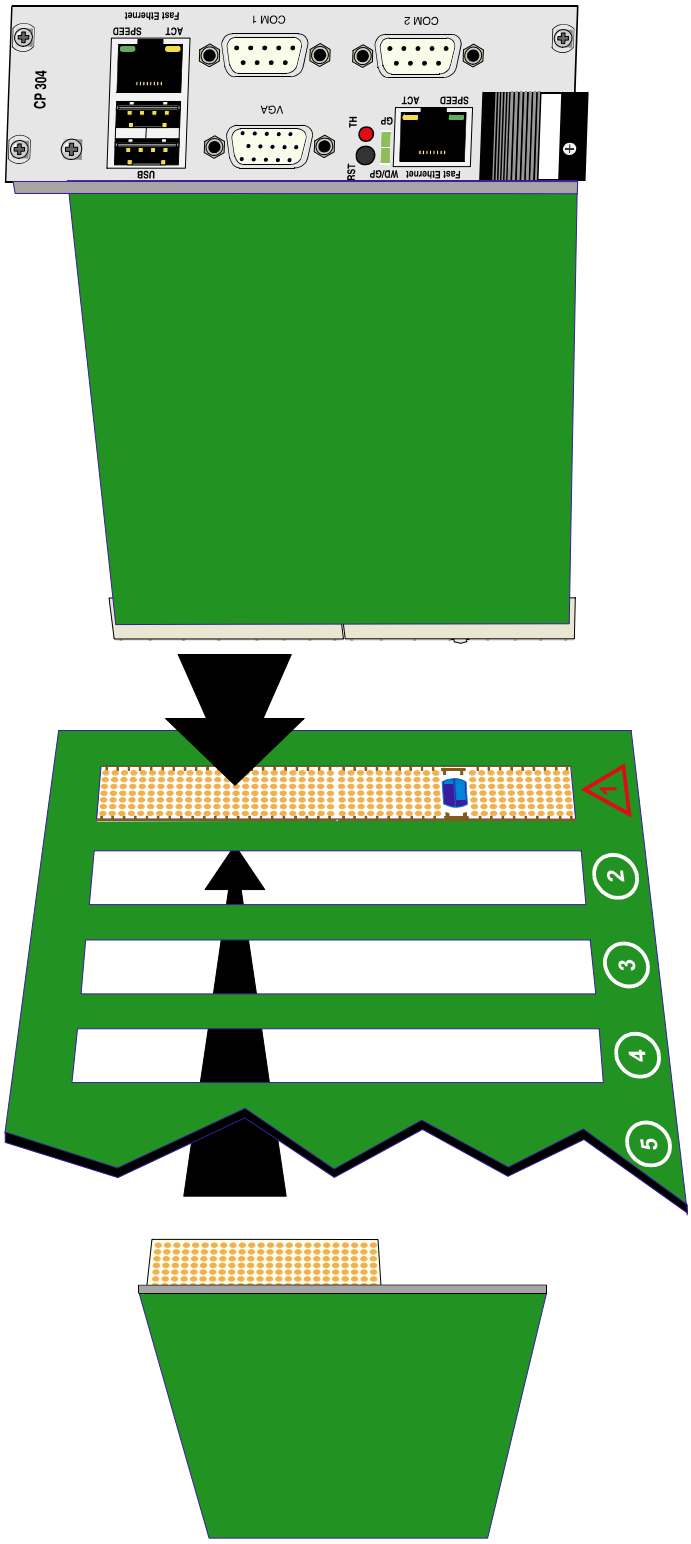


Table 2-17: Rear I/O CompactPCI Bus Connector J2 (CON2) Pinout

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	TDN1	RDN1	RDP1	GND
20	GND	CLK5	GND	TDP1	GND	VCC	GND
19	GND	GND	GND	RES	RES	+3.3V	GND
18	GND	RDN2	UV0-	UV3+	RTC Bat	+3.3V	GND
17	GND	RDP2	ROUT (GND)	PRST	REQ6	GNT6	GND
16	GND	TDN2	UV0+	DEG	GND	UV3-	GND
15	GND	TDP2	GOUT (GND)	FAL	REQ5	GNT5	GND
14	GND	2RIN	2DSR	2RTS	VSYNC (GND)	2CTS	GND
13	GND	2RXD	FANSENSE (GND)	BOUT (VIO) *NC*	2DTR	2DCD	GND
12	GND	1DSR	1RTS	1CTS	HSYNC (GND)	2TXD	GND
11	GND	1DTR	BOUT (GND) *Default Config.*	IDEDB9 (VIO) 4)	1DCD	1RIN	GND
10	GND	IDEDB8 4)	IDERST 4)	1TXD	IDEDB10 (GND) 4)	1RXD	GND
9	GND	IDEDB6 4)	IDEDB7 (GND) 4)	IDEDB4 (VIO) 4)	IDEDB5 4)	IDEDB11 4)	GND
8	GND	IDEDB3 4)	IDEDB12 4)	IDEDB2 4)	GND	IDEDB1	GND
7	GND	IDEDB14 4)	IDEDB0 (GND) 4)	IDEDB15 (VIO) 4)	IDEDRQB 4)	IDEIOWB	GND
6	GND	IDEIORB 4)	ICHRDYB 4)	IDACKB 4)	IDEDB13 (GND) 4)	IDEIRQB 4)	GND
5	GND	IDEAB1 4)	GND	IDAB0 (VIO) 4)	IDEAB2 4)	GPLED	GND
4	GND	VIO	VCC	IDECSB0 4)	GND	IDECSB1 4)	GND
3	GND	CLK4	GND	GNT3	REQ4	GNT4	GND
2	GND	CLK2	CLK3	SSYSEN	GNT2	REQ3	GND
1	GND	CLK1	GND	REQ1	GNT1	REQ2	GND

The CompactPCI connector signal description appears on the next page

Table 2-18: CompactPCI Connector Signal Descriptions

Signal Type	Description
Ethernet 1	
TDP1/TDN1	Transmit Differential Pair. (Between ethernet controller and magnetics)
RDP1/RDN1	Receive Differential Pair. (Between ethernet controller and magnetics)
Ethernet 2	
TDP2/TDN2	Transmit Differential Pair. (Between Ethernet controller and magnetics)
RDP2/RDN2	Receive Differential Pair. (Between Ethernet controller and magnetics)
USB ports	
USB1+/-	USB data differential data signals
USB3+/-	USB data differential data signals
Serial Port 1	
S1*	Serial port signals; TTL level
Serial Port 2	
S2*	Serial port signals; TTL level
CONTROL Signals	
FANSENSE	Schmitt Trigger fan tachometer inputs; TTL level
VGA CRT signals	
ROUT	Red signal
GOUT	Green signal
BOUT*	Blue signal
HSYNC	Horizontal Sync.
VSYNC	Vertical Sync.
EIDE Signals	
IDE*	EIDE signals
Reserved Signals	
RES	Reserved (leave open)

Note...

* this signal (BOUT) appears twice in the rear I/O CompactPCI bus connector J2 pinout in order to provide compatibility with the CP302. Pin number B11 refers to the CP304 and C13 refers to the CP302. The default configuration is CP304 (B11).

2.3.10.2 Rear I/O Configuration

In order to implement the system rear I/O feature, a system slot rear I/O backplane is necessary. This backplane must comply with the CompactPCI Specification PICMG 2.0 R3.0, October 1999.

Warning!

If the board is ordered as a non-rear I/O version the jumpers and resistors allocated for rear I/O must not be altered. The setting of the rear I/O jumpers and resistors **may result in damage to your board or system**.

To support the rear I/O feature a special backplane is necessary. Do not plug a rear I/O configured board in a non-system slot rear I/O backplane. This will damage the board.

Ethernet Interface

Ethernet signals are available on the front RJ45 connector and on the rear I/O interface.

The combination of both front and rear I/O is not supported. Both Fast Ethernet channels are decoupled, but enabled separately. It is not possible to operate both the rear and front I/O at the same time. Switching over from front to rear I/O or vice versa is effected under BIOS control without the need to plug/unplug Ethernet cables.

VGA Interface

The VGA signals are available on J2 when the board is ordered for rear I/O configuration. In this configuration both the front and rear I/O interfaces are active. The 75 ohm termination resistor for the red, green and blue video signals are equipped on the CP304.

Note...

Both VGA ports are electrically identical and not separated. Do not connect devices at both connectors (front I/O and rear I/O) at the same time. Doing so will result in poor signal quality.

For details of the VGA resistor settings, please refer to section 4.1.4 in chapter 4, Configuration.

EIDE Interface

Only one EIDE connector may be used at any one time through the same port; connecting both EIDE devices to the CP304 baseboard and the rear I/O module simultaneously will result in malfunction and data loss.

Serial Interface COM1 and COM2

The COM1 and COM2 ports can be used on either the front I/O or the rear I/O. If rear I/O configuration is enabled the driver for the COM1 or COM2 port can be disabled via the BIOS setting or the rear I/O configuration register.

USB Interfaces

There are two independent USB interfaces available, both ports are routed to the two 4-pin front I/O connectors. These ports may also be used on the rear I/O interface.

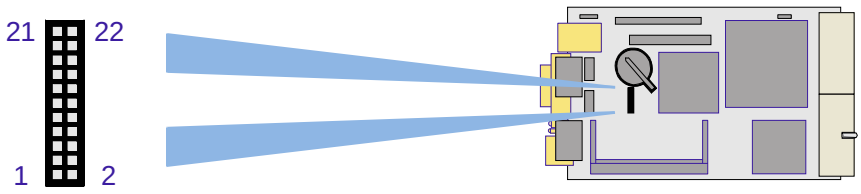
Note...

Do not connect devices at both connectors (on the front and rear I/O front panels) at the same time.

2.3.11 Extension Connector CON14

The I/O extension connector provides cost-effective, flexible configuration options. On the Intel® 815-B0 chipset platform, the Super I/O (SIO) component has migrated to the Low Pin Count (LPC) interface. To provide flexible configuration of additional low speed PC devices, e.g. Super I/O, IPMI or CAN controller, the LPC port is connected to the I/O extension connector. The I/O extension interface contains all the signals necessary to connect up to two LPC devices.

Figure 2-11: Extension Connector CON14



Chapter 3

Installation

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3. Installation

3.1 Board Installation

Warning!

Due care should be exercised when handling the board due to the fact that the heatsink can get very hot. Do not touch the heatsink when changing the board.

Caution!

If your board type is not specifically qualified as hotswap capable, please switch off the CompactPCI system before installing the board in a free CompactPCI slot. Failure to do so could endanger your life/health and may damage your board or system.

Note...

Certain CompactPCI boards require bus master and/or rear I/O capability. If you are in doubt whether such features are required for the board you intend to install, please check your specific board and/or system documentation to make sure that your system is provided with an appropriate free slot in which to insert the board.

ESD Equipment!

Your CompactPCI board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

Do not touch components, connector-pins or traces.

If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

Chapters 2 and 5 of this manual describe the hardware and software setup of the CP304 controller board, its CPU and the following related devices:

- serial port
- floppy disk interface
- EIDE device interface
- VGA
- USB
- Fast Ethernet

3.1.1 Placement of the CP304

The *PEP* CompactPCI system configuration is characterized by the fact that its system slot (slot “1”) is on the right end of the backplane, thus allowing for physical CPU growth (heat-sink, cooling fan etc.) associated with higher performance processors.

Important!

After having inserted your controller board, please make sure it has been fitted into the system slot.

3.1.2 EIDE Interfaces

The CP304 board is provided with two EIDE interfaces.

The EIDE interfaces allow installation of up to four devices (two master-slave pairs). If installed, the devices are automatically recognized by the BIOS at system “power on”.

3.1.2.1 Hard Disk Installation

To install a hard disk, it is necessary to perform the following operations in the given order:

1. Install the hardware;
2. Initialize the software necessary to run the chosen operating system.

Warning!

The incorrect connection of power or data cables may damage your hard disk unit and/or CP304 board.

Note...

ATA-66 and ATA-100 are faster timings and require a specialized cable which has additional grounding wires to reduce reflections, noise, and inductive coupling. This cable will also support all legacy IDE drives.

The blue end of the ATA-100 cable must connect to the motherboard the gray connector to the UltraDMA/100 slave device and the black connector to the UltraDMA/100 master device.

Some symptoms of incorrectly installed HDD’s are:

- Hard disk drives are not auto-detected: may be a Master / Slave problem or a bad IDE cable. Contact your vendor.
- Hard Disk Drive Fail message at bootup: may be a bad cable or lack of power going to the drive.
- No video on bootup: usually means the cable is on backwards.
- Hard drive lights are constantly on: usually means bad IDE cable or defective drives / motherboard. Try another HDD.
- Hard drives do not power up: check power cables and cabling. May also be a bad power supply or IDE drive.

3.1.3 USB Connectors

The CP304 supports all USB Plug&Play computer peripherals (e.g. keyboard, mouse, printer, etc.).

Note...

All USB devices can be attached or detached while the host or other peripherals are powered up.

3.1.4 Rear I/O Installation

Warning!

To support the rear I/O feature a special backplane is necessary. Do not plug a rear I/O configured board into a non-system slot rear I/O backplane. This will damage the board.

3.2 Software Installation

The installation of the Ethernet and all other on-board peripheral drivers is described in detail in the relevant Driver Kit files.

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Chapter 4

Configuration

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4. Configuration

4.1 Jumper Description

4.1.1 Dual BIOS Configuration

Dual BIOS means that there are two chips for the BIOS on the CP304 board (BIOS Flash and the User Flash). One chip is intended to provide a backup in the event that the other gets corrupted. These chips are soldered to the board.

If the primary BIOS is corrupted due to physical damage or a faulty flash upgrade, the solder jumper J2 should be set and the system switched over to the secondary chip and booted with default settings.

Table 4-1: Dual BIOS Configuration

J2	Description
Open	*Normal boot from the on-board BIOS*
Closed	Boot from the second BIOS chip

The default setting is indicated by italics

Note...

The Dual BIOS feature cannot be used if the second Flash chip is used for VxWorks.

4.1.2 Clearing BIOS CMOS Setup

If the system does not boot (due to, for example, the wrong BIOS configuration, or wrong password setting) the CMOS setting may be cleared using jumper J4.

Procedure for clearing CMOS setting:

The system is booted with the jumper in the new, closed position, then powered down again. The jumper is reset back to the normal position, then the system is rebooted.

Table 4-2: Clearing BIOS CMOS Setup

J4	Description
Open	*Normal boot using the CMOS settings*
Closed	Clear the CMOS settings and use the default values

The default setting is indicated by italics

4.1.3 Shorting Chassis GND (Shield) to Logic GND

The front panel and front panel connectors are isolated to the logic ground.

To enable the connection between the chassis GND and logic GND the capacitors must be exchanged with zero ohm resistors.

Table 4-3: Shorting Chassis GND (Shield) to Logic GND

CAPACITOR	SETTING	DESCRIPTION
C50, C97, C272	*Closed 470pF 2KV capacitors*	*Connectors are isolated to logic GND with three 470pF 2KV capacitors*
	Closed zero ohm resistors	Connectors are connected to logic GND and chassis GND

The default setting is indicated by italics.

4.1.4 Rear I/O VGA Configuration

These resistors are used to configure the rear I/O VGA port.

Table 4-4: Rear I/O VGA Configuration

R5	R8	Description
Open	Open	Rear I/O disabled
Closed	Open	Blue video signal matching CP302 rear I/O pinout
Open	Closed	Blue video signal matching CP303/CP304 rear I/O pinout
Closed	Closed	Not supported - these resistor settings will result in damage to the board

4.1.5 Reserved Jumpers

The following jumpers are reserved for future configurations:

J3 and J5

4.2 Interrupts

The CP304 board uses the standard AT IRQ routing (8259 controller).

This interrupt routing is the default, but can be modified via the BIOS.

Table 4-5: Interrupt Setting

IRQ	Priority	Standard Function
IRQ0	1	System timer
IRQ1	2	Keyboard controller
IRQ2	--	Input of the second IRQ controller (IRQ8-IRQ15)
IRQ3	11	Free - reserved for COM2
IRQ4	12	Free - reserved for COM1
IRQ5	13	Watchdog
IRQ6	14	Floppy Disk controller
IRQ7	15	Free - reserved for COM3 or COM4
IRQ8	3	System Real Time Clock
IRQ9	4	PCI or ACPI
IRQ10	5	PCI
IRQ11	6	PCI
IRQ12	7	PCI or PS/2 mouse
IRQ13	8	Coprocessor error
IRQ14	9	Primary hard disk
IRQ15	10	Secondary hard disk
NMI	--	Watchdog

4.3 On-board PCI Interrupt Routing

The CICH provides up to 8 PCI interrupt inputs. The table below describes the connection of these IRQ signals:

For more information please see the Intel® CICH datasheet.

Table 4-6: PCI Interrupt Routing

CICH IRQ Input	PCI Device	Function Internal CICH
PIRQA	CPCI IRQA	Free
PIRQB	Free	MODEM + SMBUS
PIRQC	Free	Free
PIRQD	Free	USB 1 controller
PIRQE	Free	CICH LAN1 controller IRQA
PIRQF	CPCI IRQB	CICH LAN2 controller IRQA
PIRQG	CPCI IRQC	Free
PIRQH	CPCI IRQD	Free

4.4 Memory Map

The CP304 board uses the standard AT ISA memory map.

4.4.1 Memory Map for the 1st Megabyte

The following table sets out the memory map for the first megabyte:

Table 4-7: Memory Map for the 1st Megabyte

Memory Range	Size	Function
0xE0000 – 0xFFFFF	128 k	BIOS implemented in FWH Reset vector 0xFFFF0
0xD0000 – 0xDFFFF	64 k	Free
0xCC000 – 0xCFFFF	16 k	Free
0xC0000 – 0xCBFFF	48 k	BIOS of the VGA card.
0xA0000 – 0xBFFFF	128 k	Normally used as video RAM as follows: CGA video : 0xB8000-0xBFFFF Monochrome video : 0xB0000-0xB7FFF EGA/VGA video : 0xA0000-0xAFFFF
0x000000 – 0x9FFFF	640 k	DOS reserved memory space

Note...

The 1 MB FLASH extension is mapped in the extended memory area e.g. 0xFFF00000–0xFFF7FFFF. The Flash address range can be configured by the CICH chip.

4.4.2 I/O Address Map

The following table sets out the memory map for the I/O memory:

Table 4-8: I/O Address Map

Address	Device
000,00F	DMA controller #1
020,021	Interrupt controller #1
022,02F	Reserved
040,043	Timer
060,063	Keyboard interface
070,071	RTC port
080,08F	DMA page register
0A0,0A	Interrupt controller #2
0C0,0DF	DMA controller #2
0E0,0EF	Reserved
0F0,0FF	Math coprocessor
170,17F	Hard disk secondary
1F0,1FF	Hard disk primary
278,27F	Parallel port LPT2
280	Watchdog trigger
282	Watchdog time
284	Watchdog, CPCI IRQ routing
286	I/O status
287	I/O configuration
288	Board version
289	Hardware index
28B	Logic index
28D	LED control
2E8,2EF	Serial port COM4
2F8,2FF	Serial port COM2
378,37F	Parallel printer port LPT1
3BC,3BF	Parallel printer port LPT3
3E8,3EF	Serial port COM3
3F0,3F7	Floppy Disk
3F8,3FF	Serial port COM1

Note...

The yellow (shaded on a printout) table cells indicate CP304-specific registers.

4.5 Special Registers Description

The following registers are special registers which the CP304 uses to watch the on-board hardware special features and the CompactPCI control signals.

Normally, only the system BIOS uses these registers, but they are documented here for application use as required.

Note...

Take care when modifying the contents of these registers as the system BIOS may be relying on the state of the bits under its control.

4.5.1 Watchdog

The CP304 has one watchdog timer. This timer is provided with a programmable timeout ranging from 125 msec to 256 sec. Failure to strobe the watchdog timer within a set time period results in a system reset, NMI or an interrupt. This can be configured via the register 0x284.

To enable the watchdog bit ”4” of the register 0x282 must be set. If the watchdog is enabled via bit ”4”, this bit cannot later be cleared.

With a write access to the register 0x280 the watchdog is retriggered. Once the watchdog is enabled, it must be continuously strobed within the terminal count period to avoid resetting the system hardware.

The watchdog can be configured in several modes, one of which is the dual stage configuration. If the NMI and the reset configuration bit are set (0x284 = 0x84) the watchdog has two stages. The first stage timeout generates an NMI interrupt. If the NMI handler does not reconfigure the watchdog, the watchdog switches to the second stage and generates a master reset after the configured timeout elapses.

4.5.2 Watchdog Trigger

A write access triggers the watchdog.

The I/O location for the watchdog trigger is 0x280.

4.5.3 Watchdog Time

Table 4-9: Watchdog Time

REGISTER NAME		WATCHDOG TIME						ACCESS	
ADDRESS		0x282						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	Res.	WDR	WDEN	WDT3	WDT2	WDT1	WDT0
DEFAULT		0	0	0	0	0	0	0	0

BIT	NAME	VAL	DESCRIPTION
0 1 2 3	WDT[3:0]		Timeout Period: Bits: 3 2 1 0 Setting: 0 0 0 0 = 0 = 000.125 sec 0 0 0 1 = 1 = 000.250 sec 0 0 1 0 = 2 = 000.500 sec 0 0 1 1 = 3 = 001 sec 0 1 0 0 = 4 = 002 sec 0 1 0 1 = 5 = 004 sec 0 1 1 0 = 6 = 008 sec 0 1 1 1 = 7 = 016 sec 1 0 0 0 = 8 = 032 sec 1 0 0 1 = 9 = 064 sec 1 0 1 0 = 10 = 128 sec 1 0 1 1 = 11 = 256 sec 1 1 0 0 = 12 = res. 1 1 0 1 = 13 = res. 1 1 1 0 = 14 = res. 1 1 1 1 = 15 = res.
4	WDEN	0	Watchdog timer disabled
		1	Watchdog timer enabled  ***Note...*** Once the watchdog timer is enabled it cannot be disabled except by resetting the system.
5	WDR	0	System reset (determines the reset event)
		1	Reset from Watchdog
6		0	Reserved
7		0	Reserved

4.5.4 CPCI and Watchdog Interrupt Configuration Register

The interrupt configuration register holds a series of bits defining the interrupt routing for the watchdog, the power control derate signal and the CompactPCI enumeration signal. If the watchdog timer fails, it can generate three independent hardware events: a reset, an NMI or an IRQ5 interrupt.

The enumeration signal is generated by a hotswap compatible board after insertion and prior to removal. The system uses this interrupt signal to force software to configure the new board. The derate signal indicates that the power supply is beginning to derate its power output.

Note...

To enable the dual stage watchdog the NMI and the reset bit must be set. At the first stage the watchdog generates an NMI and at the second stage the system will be reset.

Table 4-10: CompactPCI and Watchdog Interrupt Configuration Register

REGISTER NAME		Interrupt Configuration Register						ACCESS	
ADDRESS		0x284						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		WNMI	CFNMI	CFIRQ	CEIRQ	CDIRQ	WRST	WIRQ	Res.
DEFAULT		0	0	0	0	0	0	0	0
BIT	NAME	VAL	DESCRIPTION						
0		0	Reserved						
1	WIRQ	0	Disable Watchdog IRQ5 routing						
		1	Enable Watchdog IRQ5 routing						
2	WRST	0	Disable Watchdog hardware reset						
		1	Enable Watchdog hardware reset						
3	CDIRQ	0	Disable CPCI derate signal to IRQ5 routing						
		1	Enable CPCI derate signal to IRQ5 routing						
4	CEIRQ	0	Disable CPCI enum signal to IRQ5 routing						
		1	Enable CPCI enum signal to IRQ5 routing						
5	CFIRQ	0	Disable CPCI fail signal to IRQ5 routing						
		1	Enable CPCI fail signal to IRQ5 routing						
6	CFNMI	0	Disable CPCI fail signal to NMI routing						
		1	Enable CPCI fail signal to NMI routing						
7	WNMI	0	Disable Watchdog NMI routing						
		1	Enable Watchdog NMI routing						

4.5.5 I/O Status

This register describes the local and CompactPCI control signals. The watchdog status bit indicates the status of the watchdog timer. If the timer is not retriggered within the previously set time period, the bit is set to ”0” and the watchdog LED lights. The fail signal is an output of the power supply and indicates a power supply failure. For the description of the derate and enumeration signals please see the CompactPCI and Watchdog Configuration Register.

Table 4-11: I/O Status Register

REGISTER NAME		I/O Status Register						ACCESS	
ADDRESS		0x286						R	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		WST	Res.	Res.	Res.	CSLOT	CENUM	CFAIL	CDER
DEFAULT		1	0	0	0	0	0	0	0
BIT	NAME	VAL	DESCRIPTION						
0	CDER	0	Indicates power derating (CPCI DEG signal)						
		1	Power normal						
1	CFAIL	0	Indicates a power supply failure (CPCI FAIL signal)						
		1	Power normal						
2	CENUM	0	Indicates the insertion or removal of a hotswap system board (CPCI ENUM)						
		1	No hotswap event						
3	CSLOT	0	Indicates that the board is installed in a system slot						
		1	Indicates that the board is installed in a peripheral slot						
4		0	Reserved						
5		0	Reserved						
6		0	Reserved						
7	WST	0	Indicates that a Watchdog timeout has occurred						
		1	Indicates that no Watchdog timeout has occurred						

4.5.6 I/O Configuration Register

The I/O configuration register holds a series of bits defining the on-board configuration for the two COM ports and the general purpose LED's.

Table 4-12: I/O Configuration Register

REGISTER NAME		I/O Configuration Register						ACCESS	
ADDRESS		0x287						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	DBIOS	ELED2	ELED1	Ekey	Res.	Res.	Res.
DEFAULT		0	0	0	0	0	0	0	0
BIT	NAME	VAL	DESCRIPTION						
0		0	Reserved						
		1							
1		0	Reserved						
		1							
2		0	Reserved						
		1							
3	EKEY	0	Disable keyboard controller emulation						
		1	Enable keyboard controller emulation						
4	ELED1	0	Enable LED1 for watchdog						
		1	Enable LED1 for GP						
5	ELED2	0	Disable LED2						
		1	Enable LED2 for GP						
6	DBIOS	0	Default boot from 1st FWH						
		1	Boot from 2nd FWH						
7		0	Reserved						

4.5.7 Board Version

This register describes the hardware and the board version. The contents of this register are unique for each *PEP* CompactPCI board.

Table 4-13: Board ID Register

REGISTER NAME	Board Version						ACCESS	
ADDRESS	0x288						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	BID7	BID6	BID5	BID4	BID3	BID2	BID1	BID0
DEFAULT	0	1	0	1	0	0	0	1

4.5.8 Hardware Index

The hardware index will signal to the software when differences in the hardware require different handling by the software. It starts with the value “0” and will be incremented with each change in hardware as development continues.

Table 4-14: Hardware Index Register

REGISTER NAME	Hardware Index						ACCESS	
ADDRESS	0x289						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	HWI7	HWI6	HWI5	HWI4	HWI3	HWI2	HWI1	HWI0
DEFAULT	0	0	0	0	0	0	0	0

4.5.9 Logic Version

The logic version register may be used by software to identify the logic status of the board. It starts with the value “0” and will be incremented with each logic update.

Table 4-15: Logic Version Register

REGISTER NAME	Logic Version						ACCESS	
ADDRESS	0x28B						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	LR7	LR6	LR5	LR4	LR3	LR2	LR1	LR0
DEFAULT	0	0	0	0	0	0	0	0

4.5.10 LED Control

The LED's on the front panel can be switched on and off by setting the LED register.

Table 4-16: LED Control Register

REGISTER NAME		LED Control Register						ACCESS	
ADDRESS		0x28D						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		res.	res.	res.	res.	res.	res.	LED1	LED0
DEFAULT		0	0	0	0	0	0	0	0
BIT	NAME	VAL	DESCRIPTION						
0	LED0	0	LED off						
		1	LED on						
1	LED1	0	LED off						
		1	LED on						
2		0	Reserved						
3		0	Reserved						
4		0	Reserved						
5		0	Reserved						
6		0	Reserved						
7		0	Reserved						

4.6 On-board Chipset I/O Configuration

The CICH provides several general purpose I/O pins. The table below describes the connection of these I/O pins:

Table 4-17: On-board Chipset I/O Configuration

Number	Type	After Reset	Description
GPIO0	R	Input	Free
GPIO6	R	Input	Cable detection for primary EIDE port
GPIO7	R	Input	Cable detection for secondary EIDE port
GPI8	R	Input	Rear I/O status 1 = rear I/O module plugged in 0 = no rear I/O module plugged in
GPI12	R	Input	SMI input from hardware Monitor LM81
GPI13	R	Input	Free
GPO18	W	Output blinks	GPIO[18] blinks, by default, immediately after reset. Connected to logic
GPO19	W	Output High	Ethernet 1 interface 1 = front I/O interface 0 = rear I/O interface
GPO20	W	Output High	Ethernet 2 interface 1 = front I/O interface 0 = rear I/O interface
GPO21	W	Output High	COM1 R232 buffer for front I/O connector 1 = disable RS232 buffer 0 = enable RS232 buffer
GPO22	W	Output High	COM2 R232 buffer for front I/O connector 1 = disable RS232 buffer 0 = enable RS232 buffer
GPO23	W	Output Low	Reserved
GPIO24	RW	Input High	Solder Jumper for BIOS seeting 1 = normal 0 = clear CMOS RAM
GPIO25	RW	Input High	Reserved
GPIO27	RW	Input High	Ethernet 2 Link Status 1 = no link 0 = link
GPIO28	RW	Input High	Ethernet 1 Link Status 1 = no link 0 = link

Note...

For additional information please refer to the Intel® CICH datasheet.

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Chapter 5

CMOS

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5. CMOS

This chapter describes the Award BIOS Setup program, BIOS, version 6.00PG. The Setup program lets you modify basic system configuration settings.

5.1 Proprietary Notice

5.2 Introduction to Setup

This manual describes the Award BIOS Setup program. The Setup program lets you modify basic system configuration settings. The settings are then stored in a dedicated battery-backed memory, called CMOS RAM, that retains the information when the power is turned off.

A special feature of *PEP's* CompactPCI boards is that all Setup information is additionally saved in a non-volatile serial EEPROM. This feature provides the user with enhanced data security in comparison with a standard PC board, because setup data will not be lost should the battery fail.

The Award BIOS in your computer is a customized version of an industry-standard BIOS for IBM PC AT–compatible personal computers. It supports the Intel®x86 and compatible processors. The BIOS provides critical low-level support for the system central processing, memory, and I/O subsystems.

The Award BIOS has been customized by adding important, but nonstandard, features such as virus and password protection, power management, and detailed fine-tuning of the chipset controlling the system.

The rest of this manual is intended to guide you through the process of configuring your system using Setup.

Starting Setup

The Award BIOS is immediately activated when you first turn on the computer. The BIOS reads system configuration information in CMOS RAM and begins the process of checking out the system and configuring it through the Power-on Self Test (POST).

When these preliminaries are finished, the BIOS seeks an operating system on one of the data storage devices (hard drive, floppy drive, etc.). The BIOS launches the operating system and hands control of system operations to it.

During POST, you can start the Setup program in one of two ways:

- By pressing <Del> immediately after switching the system on, or
- By pressing the <Del> key or by simultaneously pressing <CTRL>, <ALT>, and <ESC> keys when the following message appears briefly at the bottom of the screen during POST:

Press DEL to enter SETUP

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the RESET button on the system case. You may also restart by simultaneously pressing <CTRL>, <ALT>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message appears and you are again asked to

Press F1 to continue, DEL to enter SETUP

Setup Keys

Use the keystrokes listed in the left column of the table below to make your selections or exit the current menu. The table below describes the functions of the keystrokes:

The following table describes how to navigate in Setup using the keyboard.

Table 5-1: Keyboard Commands

Key	Description
Up Arrow	Move to previous item
Down Arrow	Move to next item
Left Arrow	Move to the item to the left
Right Arrow	Move to the item to the right
Esc Key	Exit this menu. Main Menu: Quit without saving changes into CMOS RAM
PgUp Key	Increase the numeric value or make changes
PgDn Key	Decrease the numeric value or make changes
+ Key	Increase the numeric value or make changes
- Key	Decrease the numeric value or make changes
F1 Key	Brings up the General Help window that describes the legend keys
F5 Key	Select the Previous Value for the field
F6 Key	Load the Fail-Save Defaults for this page
F7 Key	Load the Optimized Defaults for this page
F10 Key	Save to CMOS and EXIT
Enter	Execute Command or Select sub menu

To display a sub-menu, use the arrow keys to move the cursor to the sub-menu you want. Then press <Enter>.

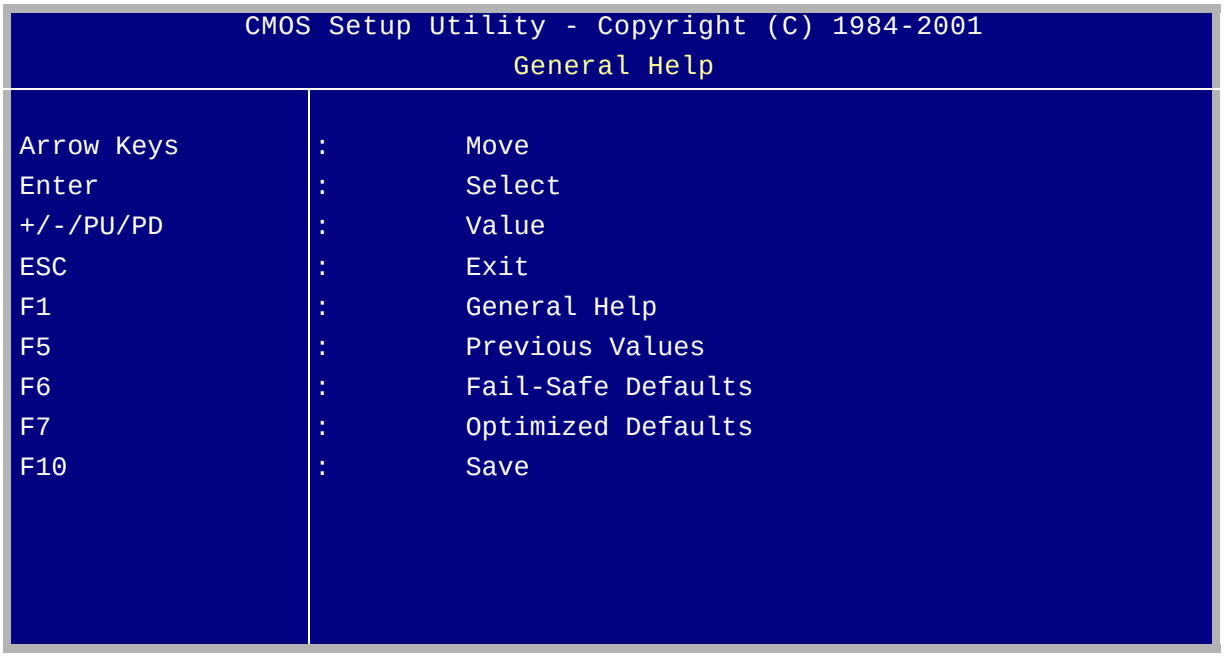
A pointer (>) indicates those entries which have sub-menus. Within the sub-menus, the variable fields may be changed directly if the desired values are known. Alternatively, a pop-up box may be opened by selecting the item using the arrow keys and then pressing return. The box offers a range of values from which a selection may be made.

Getting Help

The General Help Window

Press F1 and the General Help window pops up which describes the legend keys and their alternatives. To exit the Help Window press <Esc>.

Figure 5-1: General Help Window — Screen Display



The Field Help Window

The Item Help window on the right side of each menu displays the help text for the currently selected field. It updates as you move the cursor to each field.

In Case of Problems

You can restart by either using the ON/OFF switch, the RESET button or by pressing <CTRL>, <ALT> and <Delete> at the same time. The best advice is change only those settings that you thoroughly understand. In particular, do not change settings in the Chipset screen without good reason. The Chipset defaults have been carefully chosen by PEP Modular Computers for optimum performance and reliability. Even a seemingly small change to the Chipset setup may result in the system becoming unstable.

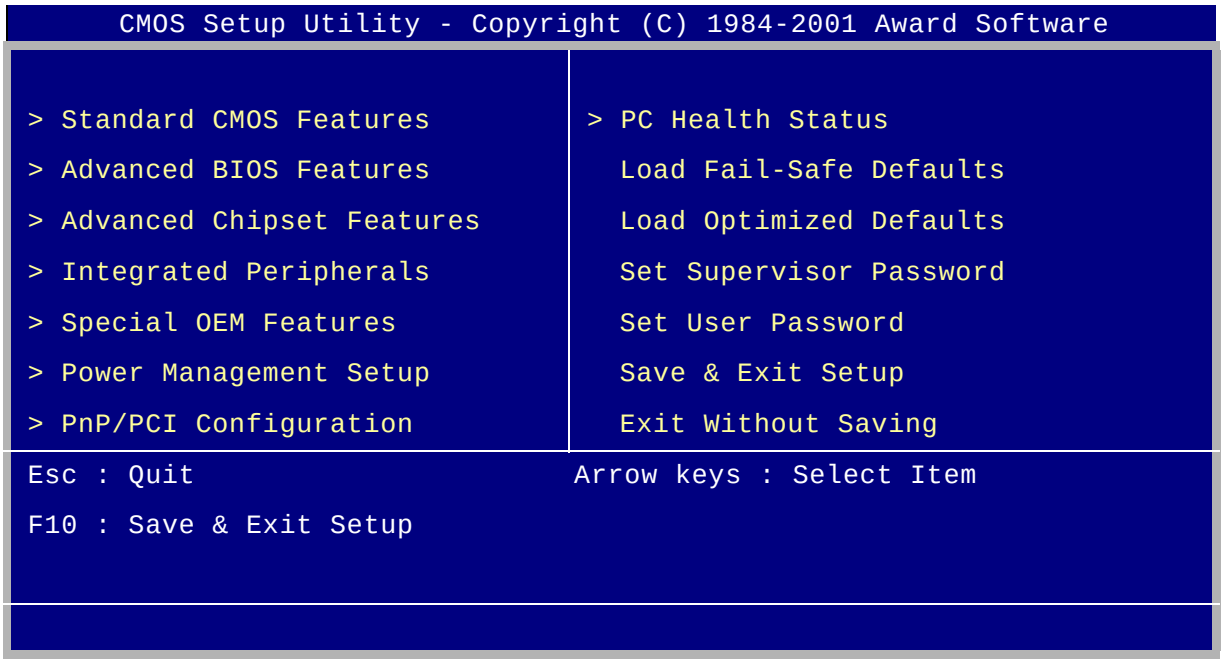
Setup Variations

Not all systems have the same Setup. While the basic look and function of the Setup program remains the same for all systems, the appearance of your Setup screens may differ from the screens shown here. Each system design and chipset combination require customized configurations. In addition, the final appearance of the Setup program depends on your system designer. Your system designer may decide that certain items should not be available for user configuration and remove them from the Setup program.

5.3 Main Setup Menu

When you enter the Award BIOS CMOS Setup Utility, a Main Menu, similar to the one shown below, appears on the screen. The Main Menu allows you to select from several Setup functions and two exit choices. Use the arrow keys to select items and press ↵ to accept and enter the sub-menu.

Figure 5-2: CMOS Setup Utility Main Menu — Screen Display



A brief description of each highlighted selection appears at the bottom of the screen.

Following is a brief summary of each Setup category.

Standard CMOS Setup

Options in the original PC AT-compatible BIOS.

Advanced BIOS Features

Award enhanced BIOS options.

Advanced Chipset Features

Options specific to your system chipset.

Integrated Peripherals

I/O subsystems, which are dependant on the integrated peripherals controller in your system.

Special OEM Features

PEP features specific to Award BIOS.

Power Management Setup

Advanced Power Management (APM) options.

PnP/PCI Configuration

PlugandPlay standard and PCI Local Bus configuration options.

PC Health Status

Information about the temperature and the voltage of the CPU.

Load Fail-Safe Defaults

BIOS defaults are factory settings for the most stable, minimal-performance system operations.

Load Optimized Defaults

Setup defaults are factory settings for optimal-performance system operations.

Set Supervisor/User Password

Change, set, or disable a password. In BIOS versions that allow separate user and supervisor passwords, only the supervisor password permits access to Setup. The user password generally allows only power-on access.

Save & Exit Setup

Save settings in non-volatile CMOS RAM and exit Setup.

Exit Without Save

Abandon all changes and exit Setup.

5.4 Standard CMOS Features

In the Standard CMOS menu you may set the system time and date, drive parameters, and select the type of errors that stop the BIOS POST.

Figure 5-3: Standard CMOS Setup Menu — Screen Display

```
      CMOS Setup Utility – Copyright (c)1984-2001 Award Software
                        Standard CMOS Features
```

Date (mm:dd:yy)	Thu, Aug 30 2001	Item Help
Time (hh:mm:ss)	13 : 27 : 29	
> IDE Primary Master	[None]	
> IDE Primary Slave	[None]	
> IDE Secondary Master	[None]	
> IDE Secondary Slave	[None]	
Halt On	[All , But Keyboard]	
Base Memory	xxxK	
Extended Memory	xxxxxxK	
Total Memory	xxxxxxK	

Date

Press the →or ←key to move to the desired field (month, date, year). Press the “PgUp” or “PgDn” key to change the setting, or type the desired value into the field. With these settings you set the system date. The weekday is set from the system.

Time

The time format is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Press the →or ←key to move to the desired field. Press the PgUp or PgDn key to change the setting, or type the desired value into the field. Using these settings you set the system time.

Hard Disks

The BIOS supports up to four EIDE drives. This section does not show information relating to other EIDE devices, such as a CD-ROM drive, or about other hard drive types, such as SCSI drives.

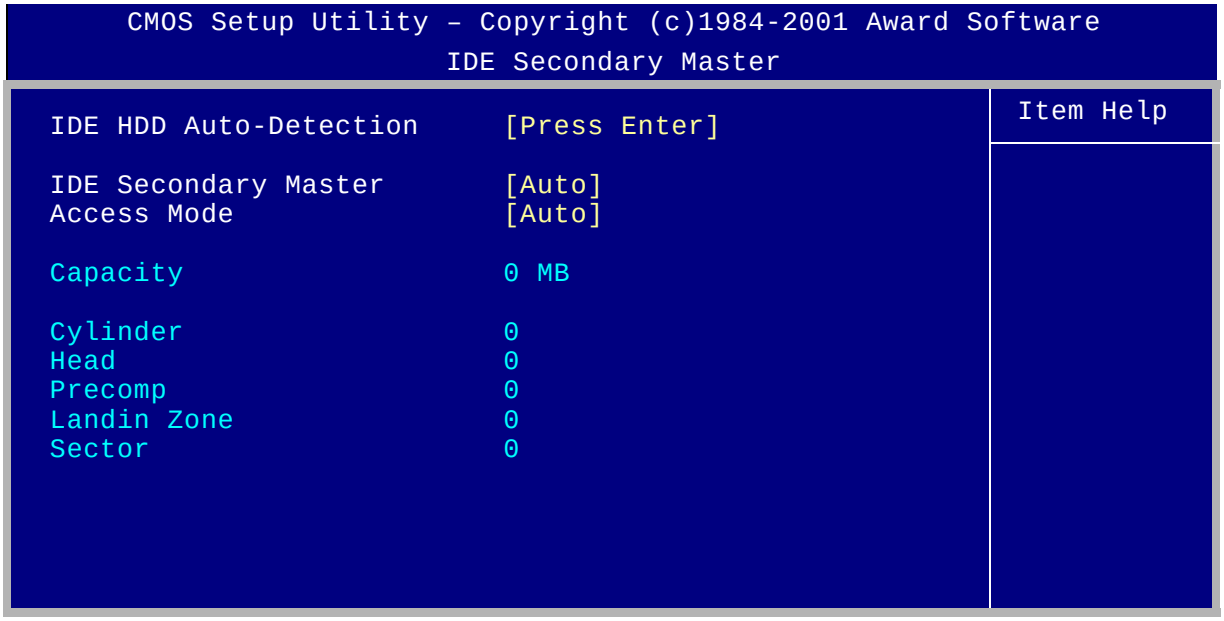
Important:

We recommend that you select the AUTO type for all drives.

The BIOS has the capability to automatically detect the specifications and optimal operating mode of almost all EIDE hard drives. When AUTO is selected in the hard drive field, the BIOS detects its specifications during POST, every time the system boots.

If you do not want to select drive type AUTO, choose the IDE Drive you will change, press Enter and the Master/Slave menu pops up.

Figure 5-4: IDE Secondary Master — Screen Display



IDE HDD Auto Detection

The BIOS auto-detects the HDD´s size, head and other characteristics on this channel.

IDE Primary Slave/Master

Select drive type for hard drive detection.

Access Mode

Select the Access Mode for the hard drive and enter values into each drive parameter field.

The following table provides a brief explanation of drive specifications:

Table 5-2: Description of Drive Specifications

Spec.		Description
Type		The BIOS contains a table of pre-defined drive types. Each defined drive type has a specified number of cylinders, number of heads, write pre-compensation factor, landing zone, and number of sectors. Drives whose specifications do not accommodate any pre-defined type are classified as type USER.
Size		Disk drive capacity (approximate). Note that this size is usually slightly greater than the size of a formatted disk given by a disk-checking program.
Cyls.		Number of cylinders
Head		Number of heads
Precomp.		Write pre-compensation cylinder
Landz		Landing zone
Sector		Number of sectors
Mode	Auto	Auto: The BIOS automatically determines the optimal mode.
	CHS	The maximum number of cylinders, heads, and sectors supported are 65535, 255, and 255 respectively.
	Large	For drives that do not support LBA and have more than 1024 cylinders.
	LBA	During drive accesses, the EIDE controller transforms the data address described by sector, head, and cylinder number into a physical block address, significantly improving data transfer rates. For drives with greater than 1024 cylinders.

Halt On

During the power-on self-test (POST), the computer stops if the BIOS detects a hardware error. You can program the BIOS to ignore certain errors during POST and continue the boot-up process. The possible selections are listed in the following table.

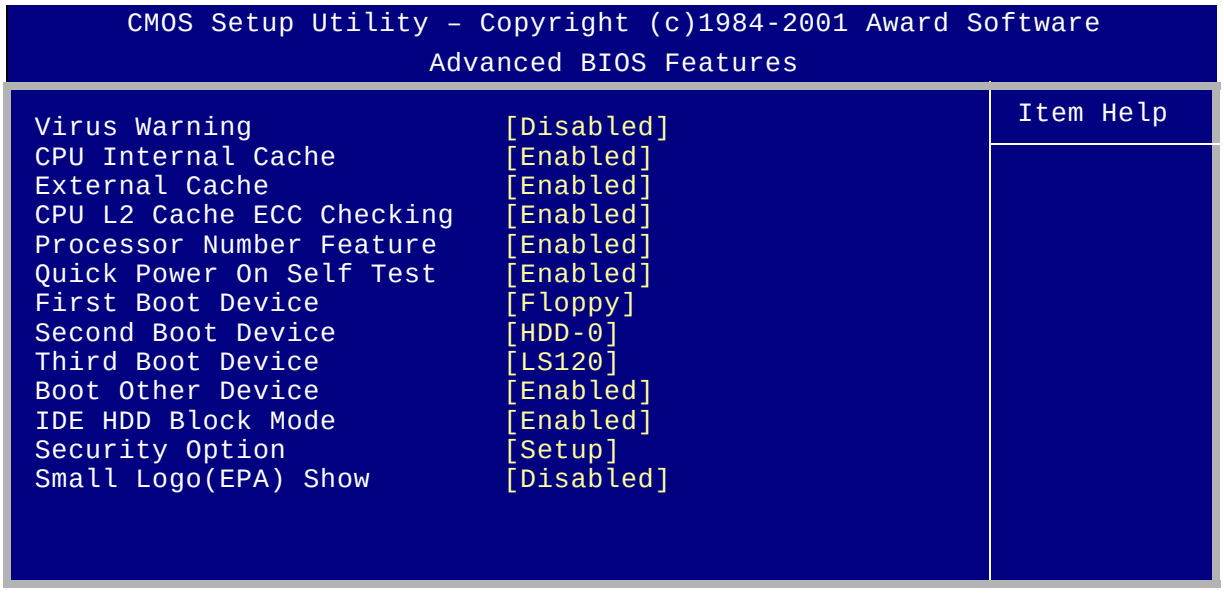
Table 5-3: POST Specific Commands

Command	POST Action
No errors	POST does not stop for any errors.
All errors	If the BIOS detects any non-fatal error, POST stops and prompts you to take corrective action.
All, but keyboard	POST does not stop for a keyboard error, but stops for all other errors.
All, but diskette	POST does not stop for diskette drive errors, but stops for all other errors.
All, but disk/Key	POST does not stop for a keyboard or disk error, but stops for all other errors.

5.5 Advanced BIOS Features

This screen contains industry-standard options additional to the core PC AT BIOS. This section describes all fields presented by Award Software in this screen. The example screen below may vary somewhat from the one in your Setup program; your system board designer may omit or modify some fields

Figure 5-5: Advanced BIOS Features - Screen Display



Virus Warning

Virus Warning is a primary IDE hard disk boot sector protection. When this function is enabled it prevents the writing of data to the Master Boot Record.

CPU Internal Cache / External Cache

Cache memory is additional memory that is much faster than conventional DRAM (system memory). CPU's from 486-type on up contain internal cache memory, and most, but not all, modern PC's have additional (external) cache memory. When the CPU requests data, the system transfers the requested data from the main DRAM into cache memory, for even faster access by the CPU.

The External Cache field may not appear if your system does not have external cache memory.

CPU L2 Cache ECC Checking

When you select *Enabled*, memory checking is enabled when the external cache contains ECC SRAM's.

Processor Number Feature

Selecting disable means that it is not possible to read the Serial Number of the processor.

Quick Power-on Self Test

Select Enabled to reduce the amount of time required to run the power-on self-test (POST). A quick POST skips certain steps. We recommend that you normally disable quick POST. Better to find a problem during POST than lose data during your work.

First - Second - Third Boot Device / Boot Other Device

The options First, Second and Third Boot Device and Boot Other Device gives you the possibility to create your own Boot Sequence.

This BIOS includes a feature for booting from LAN using the BOOTP / DHCP protocol.

Lan-Boot is based on Etherboot-5.04, a LAN-Boot implementation, which is covered by the GNU public licence. It has been adopted for use with *PEP* CompactPCI Hardware. As required by the GNU public licence, the complete sourcecode and further information are available via the internet (www.sourceforge.net).

Using this option requires an understanding of the BOOTP and/or DHCP mechanisms and knowledge in configuring a BOOTP or DHCP server. These topics are not described within this manual.

IDE HDD Block Mode

Select Enabled only if your hard drives support block mode.

Security Option

If you have set a password, select whether the password is required every time the system boots, or only when you enter Setup.

Small Logo (EPA) Show

Disable this item and the EPA symbol is not shown on the screen during booting.

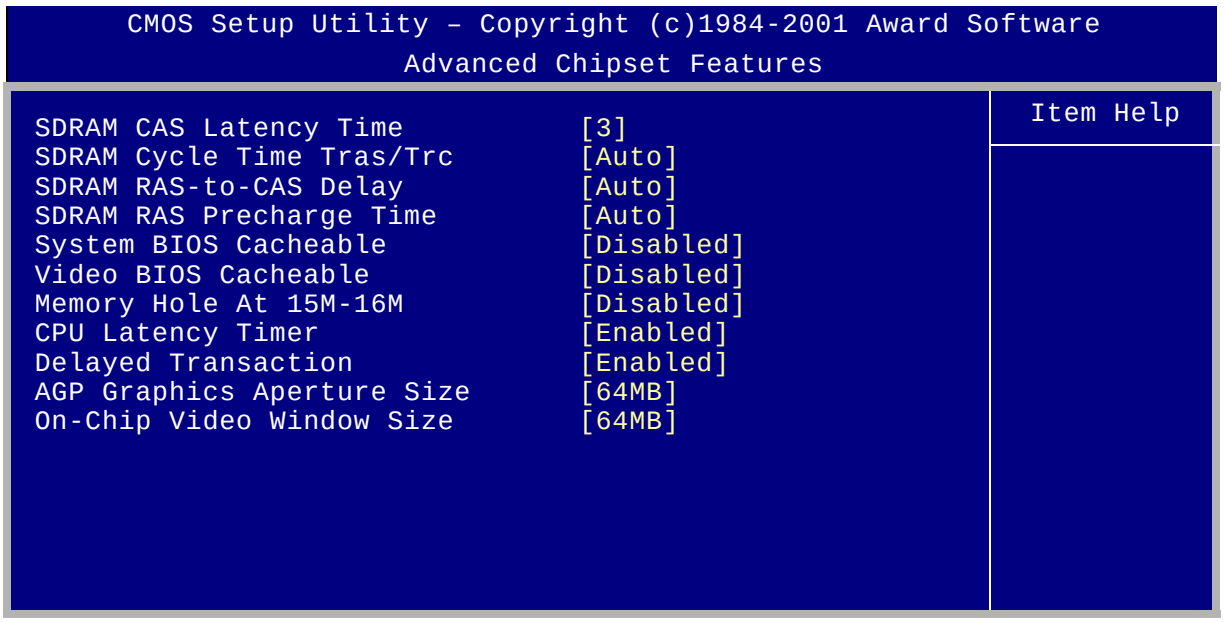
5.6 Advanced Chipset Features

This section describes features of the ICH2 PCI set and describes all the fields presented on this screen display. Please note that your system board designer may omit or modify some of the fields described in the following.

Advanced Options

The parameters in this screen are for system designers, service personnel, and technically competent users only. Do not reset these values unless you understand the consequences of your changes.

Figure 5-6: Chipset Features Setup - Screen Display



SDRAM CAS Latency Time

When synchronous DRAM is installed, you can control the number of CLK's between the SDRAM's sample of a read command and the time when the controller samples read data from the SDRAM's. Do not reset this field from the default value specified by the system designer.

SDRAM Cycle Time Trans/Trc

In this Item you can select the Cycle Time which a memory line is open (Trans), also you can select the Bank Cycle Time (Trc).

SDRAM RAS To CAS Delay

Select the RAS to CAS delay time. See Refresh Cycle Time for information about the Auto Configuration of this value.

SDRAM RAS Precharge Time

The precharge time is the number of cycles it takes for the RAS to accumulate its charge before DRAM refresh. If insufficient time is allowed, refresh may be incomplete and the DRAM may fail to retain data.

System BIOS Cacheable

Selecting *Enabled* allows caching of the system BIOS ROM at 0xF0000 to 0xFFFFF, resulting in better system performance. However, if any program writes to this memory area, a memory access error may result.

Video BIOS Cacheable

Selecting *Enabled* allows caching of the video BIOS ROM at 0xC0000 to 0xC7FFF, resulting in better video performance. However, if any program writes to this memory area, a memory access error may result.

Memory Hole at 15M-16M

You can reserve this area of system memory for ISA adaptor ROM. When this area is reserved, it cannot be cached. The user information for peripherals that need to use this area of system memory usually discusses their memory requirements.

CPU Latency Timer

CPU Latency Timer Disabled: deferrable processor cycle will be deferred immediately after receiving another ADS#

CPU Latency Timer Enabled = deferrable processor cycle will only be deferred after it has been held in a “Snoop Stall” for 31 clocks and another ADS# has arrived (default).

Delayed Transaction

The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select *Enabled* to support compliance with PCI specification version 2.1.

AGP Graphics Aperture Size

Select the size of the Accelerated Graphics Port (AGP) aperture. The aperture is a portion of the PCI memory address range dedicated for graphics memory address space. Host cycles that hit the aperture range are forwarded to the AGP without any translation.

See http://www.agpforum.org for AGP information.

On-Chip Video Window Size

Programs On-Chip VGA memory cache window in the configured size (Default 64 MB).

5.7 Integrated Peripherals

Important:

This section describes all the fields presented by Award Software in this screen display. Please note that your system board designer may omit or modify some fields.

Figure 5-7: Integrated Peripherals — Screen Display

```
      CMOS Setup Utility – Copyright (c)1984-2001 Award Software
                        Integrated Peripherals
```

			Item Help
	On-Chip Primary PCI IDE	[Enabled]	
	On-Chip Secondary PCI IDE	[Enabled]	
	IDE Primary Master PIO	[Auto]	
	IDE Primary Slave PIO	[Auto]	
	IDE Secondary Master PIO	[Auto]	
	IDE Secondary Slave PIO	[Auto]	
	IDE Primary Master UDMA	[Auto]	
	IDE Primary Slave UDMA	[Auto]	
	IDE Secondary Master UDMA	[Auto]	
	IDE Secondary Slave UDMA	[Auto]	
	Init Display First	[PCI Slot]	
	Watchdog Timer	[Disabled]	
X	WDT Active for Booting	Disabled	
X	WDT Active Time	256 sec	
	CPCI-Enum Signal	[Disabled]	
	CPCI-Derate Signal	[Disabled]	
	CPCI-Fail Signal	[Disabled]	
	Onboard Serial Port 1	[Disabled]	
	Onboard Serial Port 2	[Disabled]	

On-Chip PCI IDE (Primary/Secondary)

The Intel® 815 chipset contains a PCI EIDE interface with support for two EIDE channels. Select *Enabled* to activate the primary and/or secondary EIDE interface. Select *Disabled* to deactivate this interface if you instal a primary and/or secondary add-in EIDE interface.

IDE PIO Modes (Primary/Secondary Master/Slave)

The four EIDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of up to four EIDE devices that the internal PCI EIDE interface supports. Modes 0 through 4 provide successively increased performance. In *Auto* mode, the system automatically determines the best mode for each device.

IDE Primary/Secondary Master/Slave UDMA

UDMA (Ultra DMA) is a DMA data transfer protocol that utilizes ATA commands and the ATA bus to allow DMA commands to transfer data at a maximum burst rate of 33 MB/s. When you select *Auto* in the four EIDE UDMA fields (for each of up to four EIDE devices that the internal PCI EIDE interface supports), the system automatically determines the optimal data transfer rate for each EIDE device.

Init Display First

Initialise the PCI slot video display before initialising any other display device on the system. Thus, the PCI Slot display becomes the primary display. You also can select the AGP.

Watchdog Timer

When enabled, the Watchdog Timer may be used to select the watchdog routing to NMI, NMI + Reset, IRQ5 or Reset.

WDT Active for Booting

Select *Enable* if the watchdog timer requires to be started before the operating system is booted from the BIOS.

WDT Active Time

Select the time after which the action selected occurs, if the watchdog timer is not retriggered.

CPCI-Enum Signal

The enumeration signal is generated by a hotswap compatible board after insertion and prior to removal. The system uses this interrupt signal to force software to configure the new board.

If this signal is to used inside an application, it may be routed to the IRQ5 interrupt here.

CPCI-Derate signal

The derate signal indicates that the power supply is beginning to derate its power output.

If this signal is to used inside an application, it may be routed to the IRQ5 interrupt here.

CPCI-Fail Signal

Fail signal from the power supply. If this signal is to used inside an application, it may be routed to the IRQ5 interrupt here.

Onboard Serial Port 1/2

Here you may disable or enable the two serial ports on the CP304 Motherboard.

5.8 Special OEM Features

Important:

This section describes all the fields presented by Award Software in this screen display. Your system board designer may omit or modify some fields.

Figure 5-8: Special OEM Features — Screen Display

```
      CMOS Setup Utility – Copyright (c)1984-2001 Award Software
                          Special OEM Features
```

		Item Help
Bootrom Os-Loader	[Disabled]	
System Slot	Yes	
RIO Board installed	No	
Onboard Ethernet1	[Auto]	
Onboard Ethernet2	[Auto]	
Ethernet2/Slot 8 CPCI	[Ethernet]	
Onboard Serial Port 1	[Front]	
Onboard Serial Port 2	Rear	
Board Version	CP-303	
Board Index	00	
Logic Index	00	
EKS Number	----------	
EKS Index	----------	
Serial Number	----------	

Bootrom OS-Loader

Loading for VxWorks or other OS Bootimages.

System Slot

This is a display only field. Yes indicates that this CPU is the system controller configuring the backplane and handling all interrupts relating to the backplane. No indicates that this CPU is a slave CPU.

RIO Board Installed

This is a display only field, which shows, if a RIO board is installed in the system.

Onboard Ethernet1/2, Onboard Serial Port 1/2

This item allows Ethernet1/2 and Serial Port1/2 to be configured, regardless of whether they are connected physically to the front panel (Front) or to the Rear IO connector (Rear).

Ethernet2/Slot 8 CPCI

When the second Ethernet controller is enabled, the system has 7 CompactPCI slots. When the second Ethernet controller is disabled, 8 CompactPCI slots are available.

Board Version

This is a display only field, which reflects the value of an onboard register. This must always correspond with the CPU on which the BIOS is installed.

Board Index

This is a display only field, which reflects the value of an onboard register. It shows the index of the hardware.

Logic Index

This is a display only field, which reflects the value of an onboard register. It shows the index of the onboard logic. When the Board Index is 00 this item is not displayed.

EKS Number, EKS Index, Serial Number

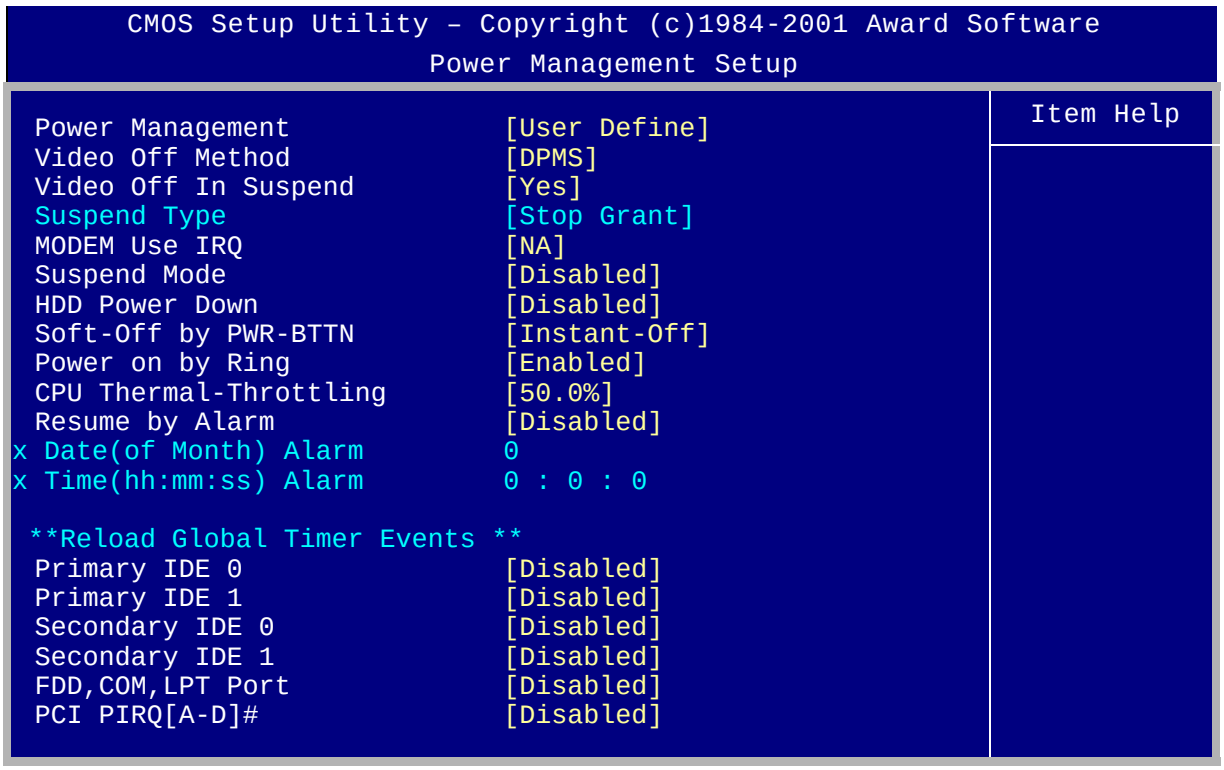
This is a display only field, which shows *PEP* internal information about the board. EKS-Number and EKS-Index refer to the production number and version respectively.

The serial number is unique to each board produced by *PEP*. It could be used also by the customer to identify specific boards.

5.9 Power Management Setup

This section describes all fields presented on this screen display. Please note that your system board designer may omit or modify some of the fields described in the following.

Figure 5-9: Power Management Setup — Screen Display



Power Management

This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. See the section *PM Timers* for a brief description of each mode.

The following table describes each power management mode:

Table 5-4: Power Management Modes

Mode	Description
Maximum Saving	Maximum power savings. Inactivity period is 1 minute in each mode.
User Defined	Sets each mode individually. Select time-out periods in the *PM Timers* section, which follows.
Minimum Saving	Minimum power savings. Inactivity period is one hour in each mode (except the hard drive).

Video-Off Method

Determines the manner in which the monitor is blanked.

Table 5-5: Video-Off Commands

Command	Description
Blank Screen	System only writes blanks to the video buffer.
V/H SYNC + Blank	System switches off vertical and horizontal synchronization ports and writes blanks to the video buffer.
DPMS Support	Select this option if your monitor supports the Display Power Management Signalling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsystem to select video power management values.

Video Off in Suspend

In this option you can choose either Yes or No and select the manner in which the monitor is switched off.

Suspend Type (display only)

Suspend Type is factory set to the function “Stop Grant” (CPU off during system inactivity).

Modem Use IRQ

Name the interrupt request (IRQ) line assigned to the modem (if any) on your system. Activity by the selected IRQ always awakens the system.

Suspend Mode

After the selected period of system inactivity (1 minute to 1 hour), all devices except the CPU shut down.

HDD Power Down

After the selected period of drive inactivity (1 to 15 minutes), the hard disk drive powers down while all other devices remain active.

Soft-Off by PWR-BTTN

When you select Instant Off or Delay 4 Sec., turning the system off with the on/off button places the system in a very low power usage state, either immediately or after 4 seconds, with only enough circuitry receiving power to detect power button activity or Resume by Ring activity.

Power on by Ring

When enabled, an input signal on the Signal Ring Indicator (RI) line (i.e. an incoming call on the modem) awakens the system from a soft off state.

CPU Thermal-Throttling

When the system enters Suspend mode, the CPU clock runs only part of the time. You may select the percentage of the time that the clock runs.

Resume by Alarm

When Enabled, you can set the date and time at which the RTC (real-time clock) alarm

awakens the system from suspend mode.

Date (of Month) Alarm

Select a date in the month when you want the alarm to go off. Select 0 (zero) if you prefer to set a weekly alarm

Time (hh:mm:ss) Alarm

Set the time at which you want the alarm to go off the days when it is activated..

Reload Global Timer Events

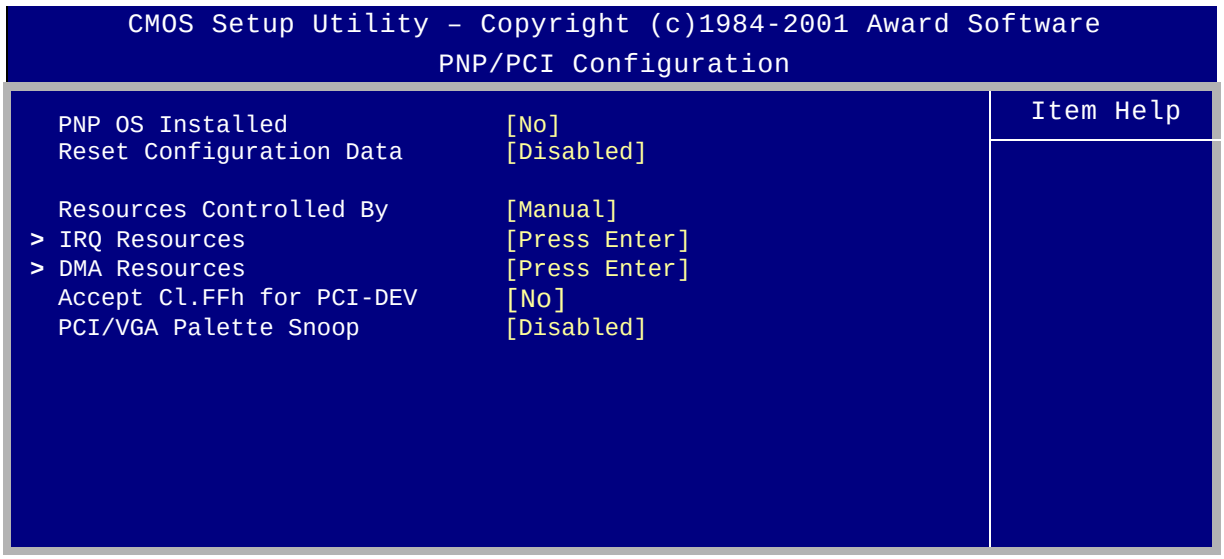
When Enabled, an event occurring on each of the devices listed below restarts the global timer for Standby mode:

- Primary EIDE 0,
- Primary EIDE 1,
- Secondary EIDE 0,
- Secondary EIDE 1,
- Floppy Disk,COM;LPT Port
- PCI PIRQ[A-D]#

5.10 PNP/PCI Configuration

This section describes all the fields presented by this screen display. Please note that your system board designer may omit or modify some of the fields described in the following.

Figure 5-10:PNP/PCI Configuration — Screen Display



PNP OS Installed

Select “Yes” if the system operating environment is PlugandPlay aware (e.g. Win 95).

Reset Configuration Data

Normally this field is left *Disabled*. Select *Enabled* to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system re-configuration has caused such a serious conflict that the operating system cannot boot.

Resources Controlled by

The Award PlugandPlay BIOS can automatically configure all the boot and PlugandPlay-compatible devices. If you select *Auto*, all the interrupt request (IRQ) and DMA assignment fields disappear, as the BIOS automatically assigns them.

IRQ Resources

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt.

Legacy ISA	Devices compliant with the original PC AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1).
PCI/ISA PnP	Devices compliant with the PlugandPlay standard, whether designed for PCI or ISA bus architecture.

DMA Resources

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt.

Legacy ISA	Devices compliant with the original PC AT bus specification, requiring a specific DMA channel
PCI/ISA PnP	Devices compliant with the PlugandPlay standard, whether designed for PCI or ISA bus architecture.

Accept Class FFh for PCI-device

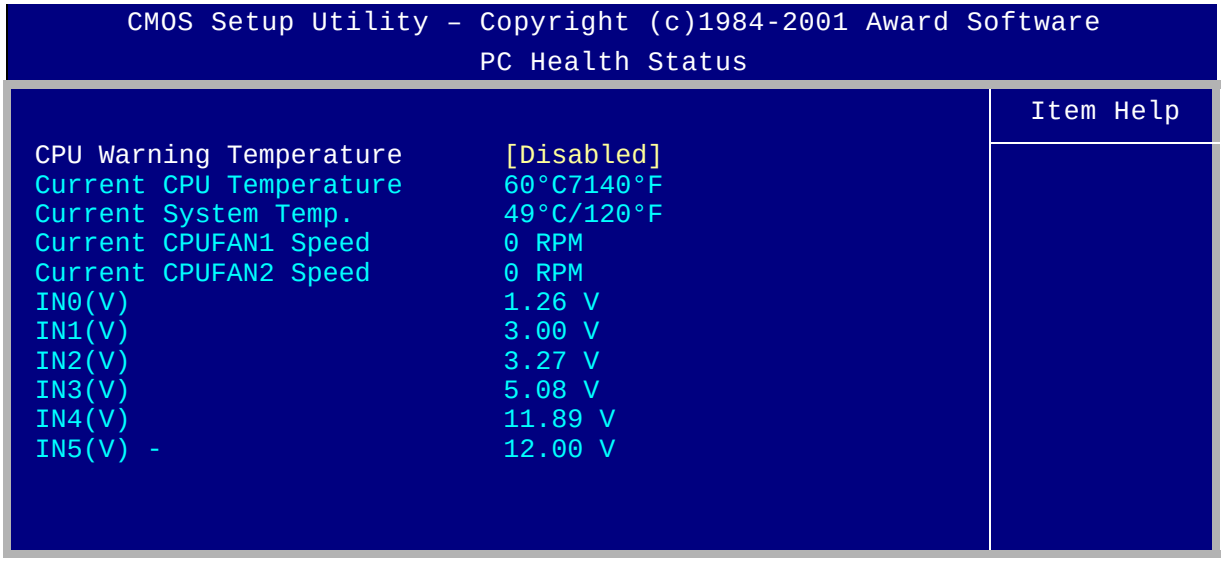
Some PCI boards use the class code 0FFh. Boards with class code FF are distributed by some vendors in the knowledge that there will be different handling of such devices. The PCI standard does not define configuration rules for class code FF. To make it transparent to the user that such a board has been identified in the system, the BIOS will display the text "Class-Code FF Device" highlighted and blinking in the PCI device list, which is displayed on system startup before booting. By setting this field to “No”, these non-standard boards will be ignored. By setting this field to “Yes”, these non-standard boards will also be configured by the BIOS and made operable.

PCI/VGA Palette Snoop

Your BIOS Setup may not contain this field. If the field is present, leave at Disabled.

5.11 PC Health Status

Figure 5-11: PC Health Status — Screen Display



CPU Warning Temperature

Select the combination of lower and upper limits for the CPU temperature. If the CPU temperature extends beyond either limit, any warning mechanism programmed into your system will be activated.

5.12 Password Setting

When you select this function, the following message appears at the center of the screen:

`Enter password:`

Type the password, up to eight characters in length, and press "↵". Typing a password clears any previously entered password from the CMOS memory.

After having pressed "↵" the message changes to:

`Confirm password:`

Type the password again and press "↵". To abort the process at any time, press "Esc".

In the "Security Option" item in the "BIOS Features Setup" screen, select `System` or `Setup`:

Important:

To clear the password, simply press "↵" when asked to enter a password. Then the password function is disabled.

Table 5-6: Security Options

Option	Description
System	Enter a password each time the system boots and whenever you enter Setup.
Setup	Enter a password whenever you enter Setup.

5.13 POST Messages

During the Power-on Self Test (POST), the BIOS displays a message whenever it detects a correctable error. Any error message is followed by this prompt:

```
Press “F1” to continue, “Ctrl-Alt-Esc” or “Del” to enter setup.
```

Following is a list of POST error messages for both the ISA and the EISA BIOS.

CMOS Battery Has Failed

The CMOS battery is no longer functional. It should be replaced.

CMOS Checksum Error

Checksum of CMOS is incorrect. This can indicate that the CMOS has become corrupted. This error may have been caused by a weak battery. Check the battery and replace it, if necessary.

Disk Boot Failure, Insert System Disk and Press Enter

No boot device was found. This could mean that either a boot drive was not detected or that the drive does not contain proper system boot files. Insert a system disk into
Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

Diskette Drives or Types Mismatch Error - Run Setup

Type of floppy-disk drive installed in the system is different from the CMOS definition. Run “Setup” to reconfigure the drive type correctly.

Display Switch is Set Incorrectly

Display switch on the motherboard can be set to either monochrome or color. This error message indicates that the switch has a setting other than that indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the video selection.

Display Type Has Changed Since Last Boot

Since the last powering-down of the system, the display adapter has been changed. You must configure the system for the new display type.

EISA Configuration Checksum Error - Please Run EISA Configuration Utility

The EISA non-volatile RAM checksum is incorrect or cannot correctly read the EISA slot. This can indicate either the EISA non-volatile memory has become corrupted or the slot has been configured incorrectly. Ensure also that the card is installed firmly in the slot.

EISA Configuration Is Not Complete - Please Run EISA Configuration Utility

The slot configuration information stored in the EISA non-volatile memory is incomplete.

Note:

When either of the above EISA error messages appears, the system boots in ISA mode so that you can run the EISA Configuration Utility.

Error Encountered Initializing Hard Drive

Hard drive cannot be initialized. Make sure that the adapter is installed correctly and that all cables are correctly and firmly attached. Ensure also that the correct hard drive type is selected in “Setup”.

Error Initializing Hard Disk Controller

Cannot initialize controller. Make sure that the cord is correctly and firmly installed in the bus. Ensure also that the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

Floppy-Disk Controller Error or No Controller Present

Cannot find or initialize the floppy drive controller. Make sure that the controller is installed correctly and firmly. If there are no floppy drives installed, ensure that the floppy-disk drive selection in “Setup” is set to `NONE`.

Invalid EISA Configuration - Please Run EISA Configuration Utility

The non-volatile memory containing EISA configuration information was programmed incorrectly or has become corrupted. Re-run EISA configuration utility to correctly program the memory.

Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

Keyboard Error or No Keyboard Present

Cannot initialize the keyboard. Make sure that the keyboard is attached correctly and that no keys are being pressed during the boot process.

If you are deliberately configuring the system without a keyboard, set the “Error Halt” condition in “Setup” to `HALT ON ALL, BUT KEYBOARD`. This causes the BIOS to ignore the missing keyboard and continue the boot process.

Memory Address Error at ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

Memory Parity Error at ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

Memory Size Has Changed Since Last Boot

Memory has been added or removed since the last boot. In EISA mode use the configuration utility to reconfigure the memory configuration. In ISA mode enter “Setup” and enter the new memory size into the memory fields.

Memory Verify Error at ...

Indicates an error verifying a value already written to memory. Use the location along with your system's memory map to locate the bad chip.

Offending Address not Found

This message is used in conjunction with the “I/O Channel Check” and “RAM Parity Error” messages whenever the segment that has caused the problem cannot be isolated.

Offending Segment

This message is used in conjunction with the “I/O Channel Check” and “RAM Parity Error” messages whenever the segment that has caused the problem has been isolated.

Press a Key to Reboot

This message appears at the bottom of the screen when an error occurs that requires you to reboot. Press any key to reboot the system.

Press “F1” to Disable NMI, “F2” to Reboot

When the BIOS detects a non-maskable interrupt condition during boot, you can disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

RAM Parity Error - Checking for Segment ...

Indicates a parity error in the random access memory.

Should Be Empty But EISA Board Found - Please Run EISA Configuration Utility

A valid board ID was found in a slot that was configured as having no board ID.

Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

Should Have EISA Board but not Found - Please Run EISA Configuration Utility

The board installed is not responding to the ID request, or no board ID has been found in the indicated slot.

Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

Slot not Empty

Indicates that a slot designated as empty by the EISA Configuration Utility actually contains a board.

Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

System Halted, <CTRL-ALT-DEL> to Reboot ...

Indicates that the present boot attempt has been aborted and that the system must be rebooted. Press and hold down the “CTRL” and “ALT” keys and press “DEL”.

Wrong Board in Slot - Please Run EISA Configuration Utility

The board ID does not match the ID stored in the EISA non-volatile memory.

Note:

When this error appears, the system boots in ISA mode so that you can run the EISA configuration utility.

5.14 POST Codes

ISA and PCI POST codes are routed to port address 80H.

Table 5-7: Early POST Codes before System BIOS is Shadowed

POST Code	Action
Reset	RTC& KBC initialisation
0CFh	Early CPU Detection
0C0h	Early Chipset initialisation
0C1h	Memory presence test: detects memory modules and programs chipset accordingly
0C3h	Decompresses Bios
0C5h	Shadows Main Bios and jumps to POST

Table 5-8: Normal POST Codes after System BIOS is Shadowed

POST Code	Action
02h	- Jump to E000 segment - Commences execution of POST routines in E000 - Starting with POST 3h
03h	Early initialisation of Super I/O
04h	Reserved
05h	Blank Video, reset video controller
06h	Reserved
07h	Initialise Keyboard Controller
08h	Keyboard Test
09h	Reserved
0Ah	Mouse Initialisation
0Bh	Reserved
0Ch	Reserved
0Dh	Reserved
0Eh	Checksum ROM, verify Shadow
0Fh	Reserved

Table 5-8: Normal POST Codes after System BIOS is Shadowed (cont'd)

POST Code	Action
10h	Detect EEPROM
11h	Reserved
12h	Test and Reset CMOS
13h	Reserved
14h	Load Chipset Defaults
15h	Reserved
16h	Initialise onboard clock generator
17h	Reserved
18h	CPU ID and initialise L1/L2 Cache
19h	Reserved
1Ah	Reserved
1Bh	Initialise interrupt vector table
1Ch	Test CMOS and Check Battery Fail
1Dh	Early PM initialisation
1Eh	Reserved
1Fh	Load Keyboard Matrix
20h	Reserved
21h	Init Heuristic Power Management (HPM)
22h	Reserved
23h	Early Prog chipset (PM) registers
24h	Init PNP
25h	Shadow system/video BIOS
26h	Init onboard clock generator and sensor
27h	Setup BIOS DATA AREA (BDA)
28h	Reserved
29h	Chipset programming and Cpu Speed detect
2Ah	Reserved

Table 5-8: Normal POST Codes after System BIOS is Shadowed (cont'd)

POST Code	Action
2Bh	Initialize Video
2Ch	Reserved
2Dh	Test Video Memory and display Logos
2Eh	Reserved
2Fh	Reserved
32h	Reserved
33h	Early Keyboard Reset
34h	Reserved
35h	Test DMA channel 0
36h	Reserved
37h	Test DMA channel 1
38h	Reserved
39h	Test DMA Page Registers
3Ah	Reserved
3Bh	Reserved
3Ch	Test 8254 chip
3Dh	Reserved
3Eh	Test 8259 Channel 1 mask bits
3Fh	Reserved
40h	Test 8259 channel 2 mask bits
41h	Reserved
42h	Reserved
43h	Test 8259 functionality
44h	Reserved
45h	Reinitialize Preboot agent serial port
46h	Reserved
47h	EISA test (if applicable)

Table 5-8: Normal POST Codes after System BIOS is Shadowed (cont'd)

POST Code	Action
48h	Reserved
49h	Size base and extended memory
4Eh	Initialise APIC and set MTRR
4Fh	Reserved
50h	USB Initialisation
51h	Reserved
52h	Memory Test
53h	Reserved
54h	Reserved
55h	Display CPU type string
56h	Reserved
57h	Early PNP Init and Display PNP logo
58h	Reserved
59h	Initialize Trend Antivirus
5Ah	Reserved
5Bh	Auto Load Awdflash (optional)
5Ch	Reserved
5Dh	Initialize onboard IO
5Eh	Reserved
5Fh	Reserved
60h	Display Setup message and enable Setup functions
61h	Reserved
62h	Reserved
63h	Check for PS2 mouse and reset keyboard
64h	Reserved
65h	Install Mouse
66h	Reserved

Table 5-8: Normal POST Codes after System BIOS is Shadowed (cont'd)

POST Code	Action
67h	ACPI sub-system initialisation
68h	Reserved
69h	Initialize Cache
6Ah	Reserved
6Bh	Enter Setup check and auto config prog.
6Ch	Reserved
6Dh	Initialize floppy controller
6Eh	Reserved
6Fh	Install FDDs
70h	Reserved
71h	Reserved
72h	Reserved
73h	Initialize IDE controller
74h	Reserved
75h	Detect IDE devices
76h	Reserved
77h	Initialize serial ports
78h	Reserved
79h	Reserved
7Ah	Initialize Parallel Ports
7Bh	Reserved
7Ch	HDD write protect (optional)
7Dh	Reserved
7Eh	Reserved
7Fh	Check and Display POST error messages
80h	Reserved
81h	Reserved

Table 5-8: Normal POST Codes after System BIOS is Shadowed (cont'd)

POST Code	Action
82h	Password Check
83h	Write CMOS back to RAM
84h	Display PNP devices detected
85h	USB Final Initialisation
86h	Reserved
87h	Reserved
88h	Reserved
89h	Setup ACPI tables
8Ah	Reserved
8Bh	Scan for Option ROMs
8Ch	Reserved
8Dh	Enable parity check
8Eh	Reserved
8Fh	Enable IRQ12 if mouse present
90h	Reserved
91h	Reserved
92h	Reserved
93h	Read and store boot partition info in RAM
94h	Final Init – for last minute details
95h	Set NUMLOCK status
96h	Set Low Stack and BOOT via INT 19h

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Appendix A

PS2 Module

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A. PS2 Module

A.1 Overview

The *PEP* CP304-PS2 module has been designed to make all PC legacy I/O ports accessible to the user. The module includes two COM ports, a PS/2 keyboard and mouse port, floppy, hard disk and CompactFlash interfaces. This additional capability opens up the broadest range of expansion possibilities.

The connectors for the two COM ports, the PS/2 keyboard and mouse are situated at the front panel, while the floppy and CompactFlash connector can be attached on the on-board connectors. The module connects to the CP304 across an I/O extension connector.

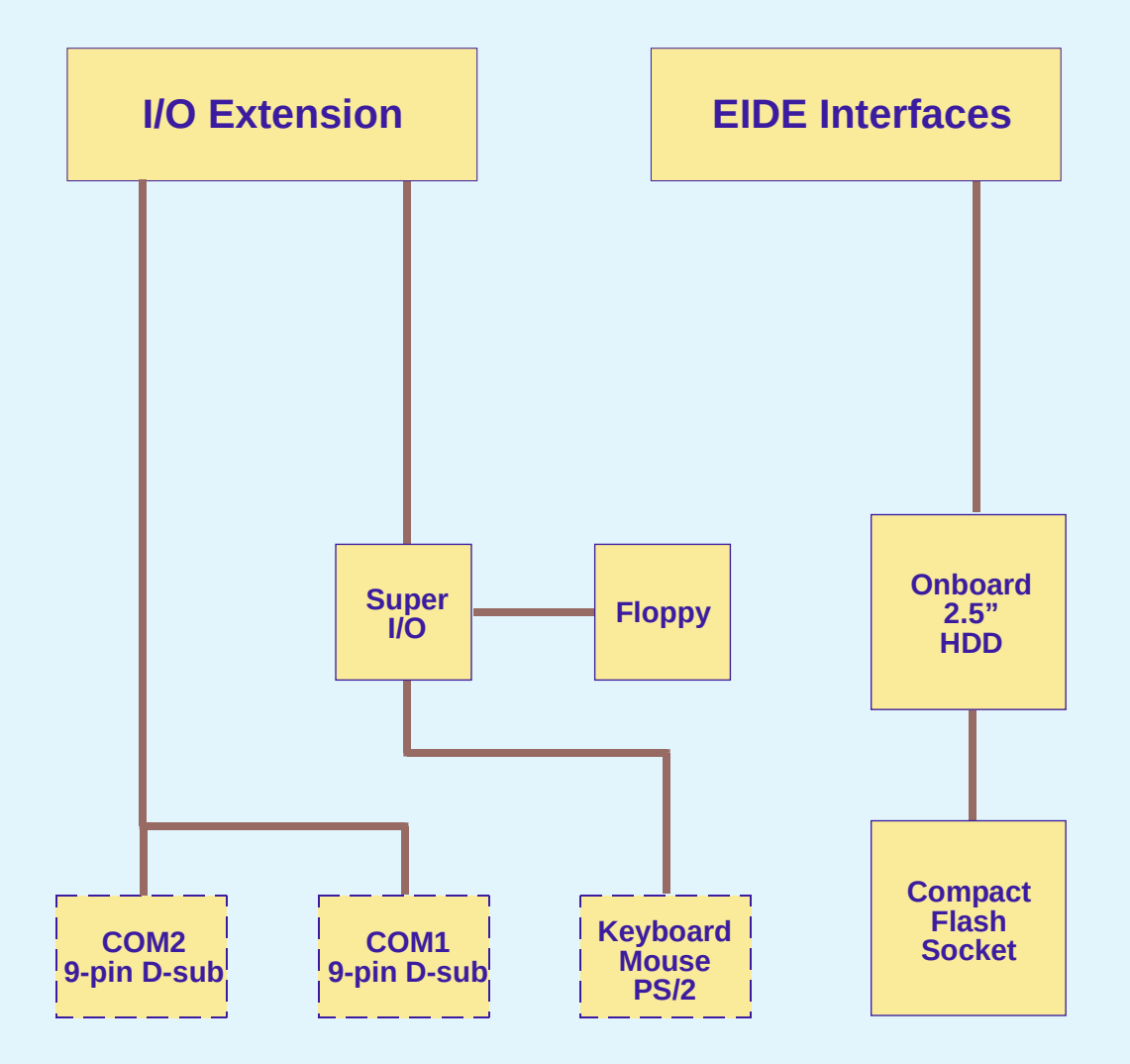
A.2 Technical Specifications

Table A-1: CP304-PS2 Module Main Specifications

	CP304-PS2	Specifications
Controller	Super I/O Controller	The LPC47M107 from SMSC is an LPC Plug and Play compatible I/O device that provides functions for the keyboard and mouse interface and the floppy disk interface.
External Interfaces	Keyboard and Mouse Interface	PS/2 type, 6-pin, shielded mini-DIN connector for the keyboard and mouse (via Y-cable)
	Floppy	One floppy disk interface (up to 2.88 MB) on 34-pin 2.54mm connector and 20-pin connector
	Serial Port	Up to two UART's, 16C550 compatible COM1/2 RS-232, two 9-pin D-sub connectors
Internal Interfaces	CompactFlash interface	CompactFlash socket for type II devices (primary EIDE interface)
General	Power Consumption Module	3.3 V at 100 mW 5.0 V at 100 mW (without hard disk)
	Temperature Range	Operating temp.: 0°C to +60°C Storage temp.: -55°C to +85°C
	Humidity	Operating humidity: 0% to 95% non-condensing
	Dimensions	Dimensions: 100 mm x 160 mm
	Board Weight	CP304 8HP with heatsink and PS2 module: 570 grams (without hard disk)

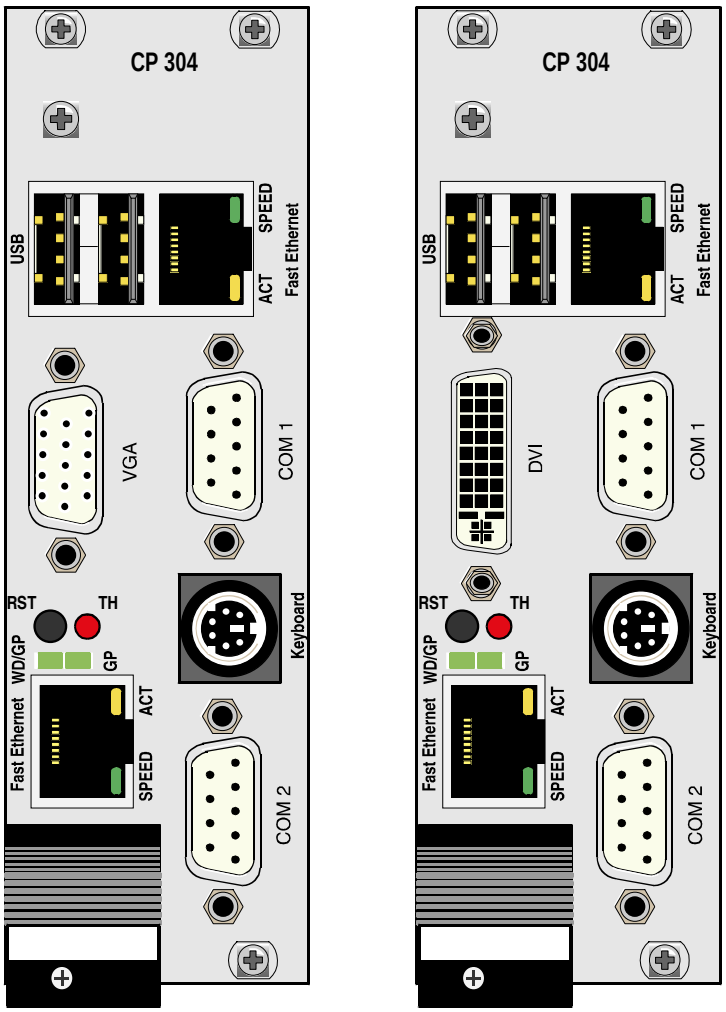
A.3 CP304-PS2 Module Functional Block Diagram

Figure A-1: CP304-PS2 Module Functional Block Diagram



A.4 CP304-PS2 Module Front Panels

Figure A-2: CP304-PS2 Module Front Panels



LEGEND:

Front panels of the two versions of the CP304 are shown above, the DVI version and the VGA version.

General Purpose LED's

- WD/GP (green): Watchdog or General Purpose
- GP (green): General Purpose
- TH (red): Overtemperature Status

Integral Ethernet LED's

- ACT (yellow): Ethernet Link/Activity
- SPEED (green): Ethernet Speed

A.5 CP304-PS2 Module Layout

The transition module includes additional standard PC interfaces.

A.5.1 CP304-PS2 Module Layout

Figure A-3: CP304-PS2 Module Layout (Front Side)

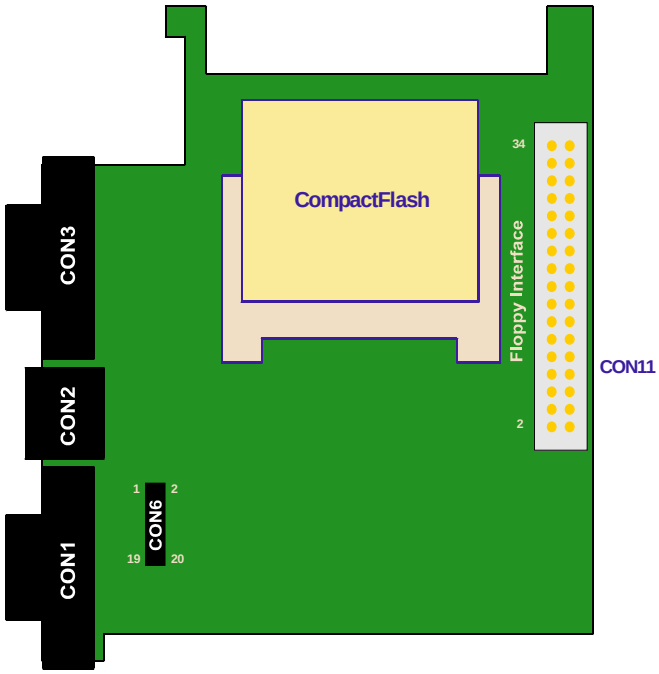


Figure A-4: CP304-PS2 Module for Hard Disk Layout (Front Side)

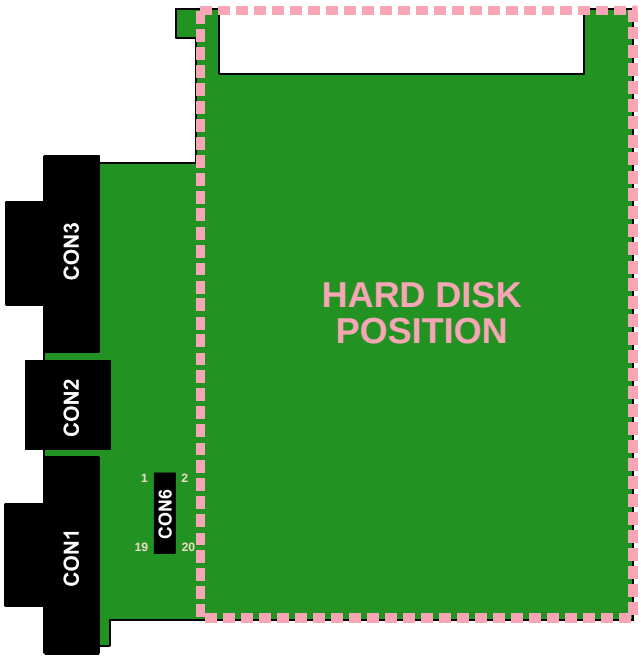


Figure A-5: Installing the CP304 with PS/2 Module in the Rack

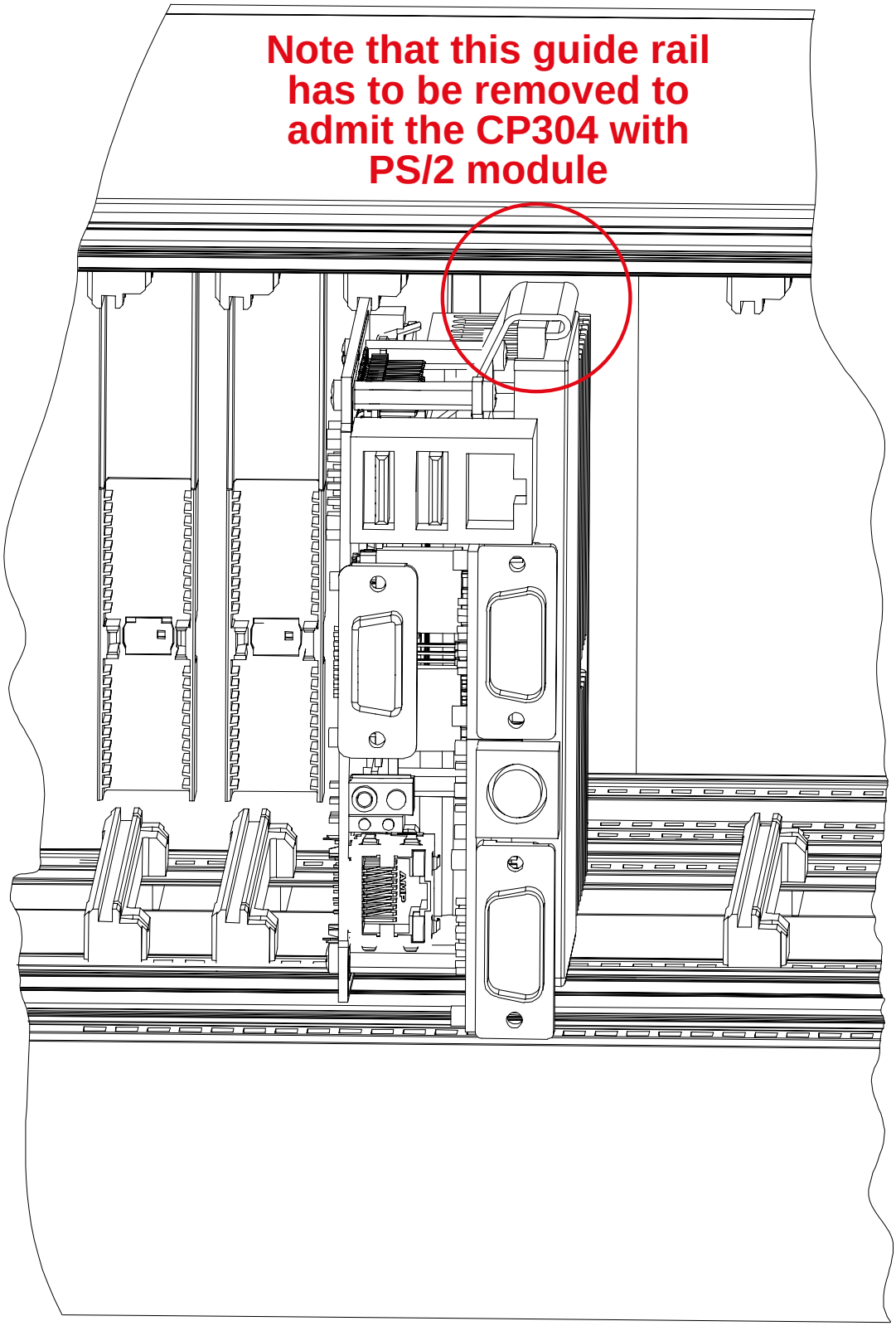
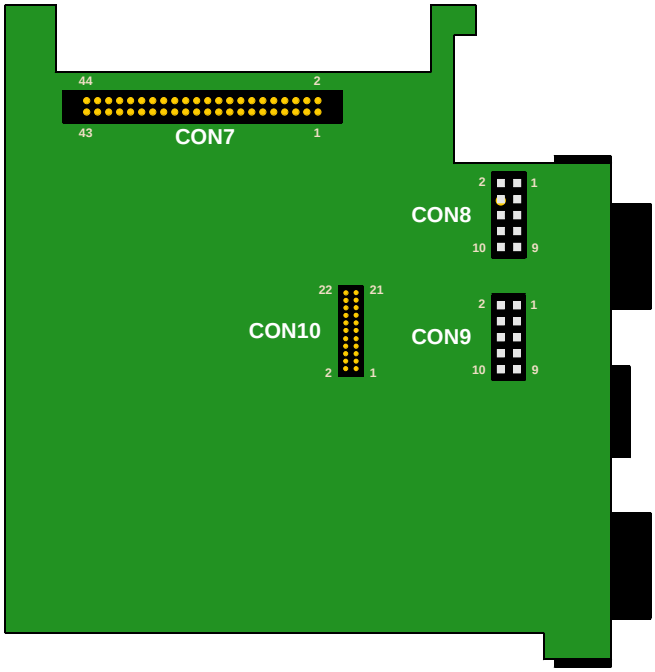


Figure A-6: CP304-PS2 Module Layout (Reverse Side)



A.6 Module Interfaces (Front Panel and Onboard)

A.6.1 Keyboard/Mouse Interface

The onboard keyboard controller is 8042 software compatible.

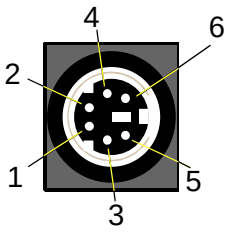
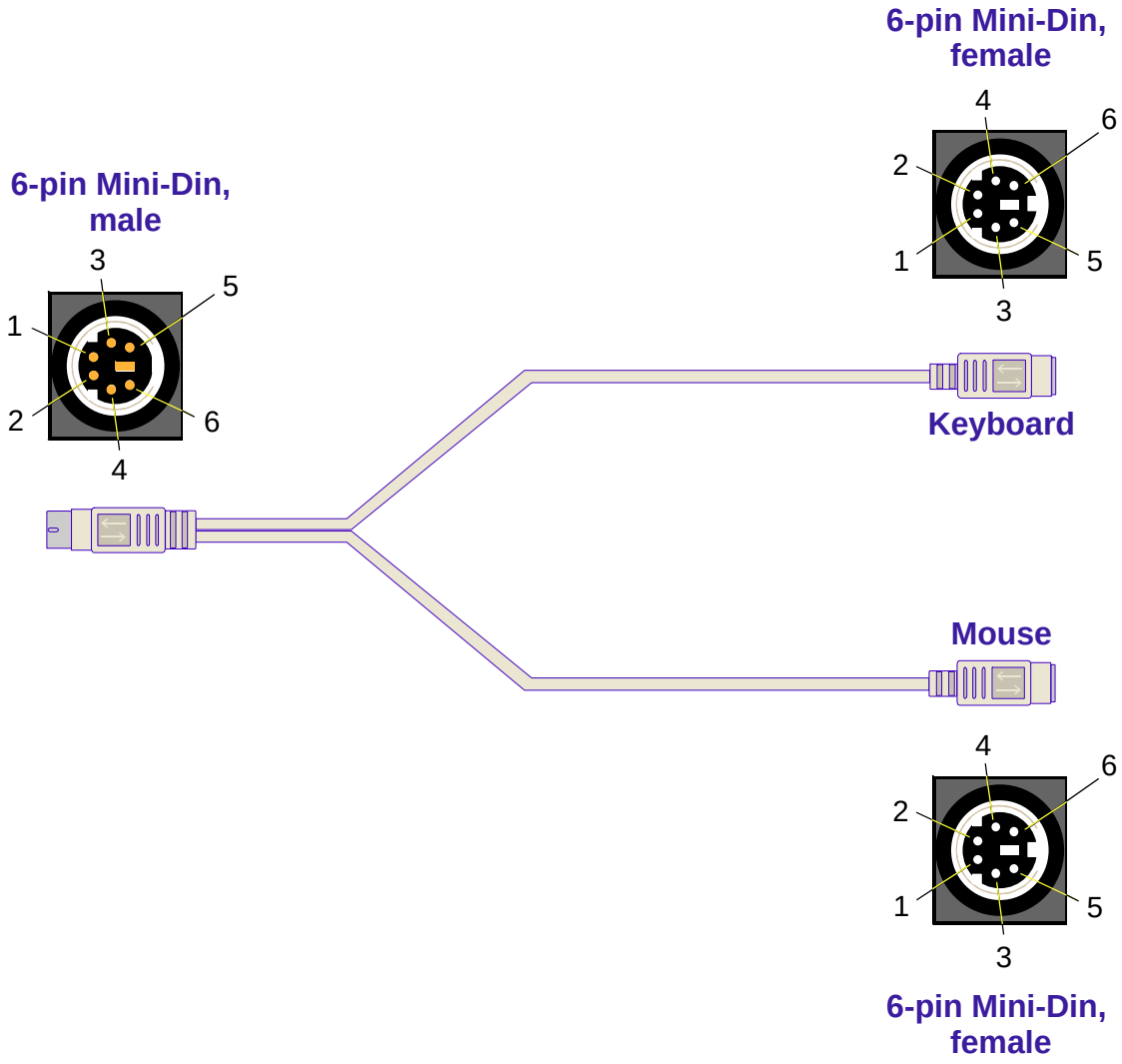


Figure A-7:Keyboard/Mouse Connector

The PC/AT standard keyboard/mouse connector is a PS/2-type 6-pin shielded Mini-DIN connector. The keyboard power supply unit is protected by a 500 mA fuse. All signal lines are EMI-filtered.

A special adapter to connect a mouse device and/or a keyboard to the PS/2 connector ia available from *PEP.*

Figure A-8: Adapter for Connecting Mouse/Keyboard via PS/2



A.6.1.1 Keyboard Connector CON2 Pinout

The PS2 module has the AT keyboard connector implemented on a 6-pin Mini-Din connector.

Table A-2: Keyboard Connector CON2 Pinout

Pin Number	Signal	Function	In/Out
1	KDATA	Keyboard data	In/Out
2	MDATA	Mouse data	In/Out
3	GND	Ground signal	--
4	VCC	VCC signal	--
5	KCLK	Keyboard clock	Out
6	MCLK	Mouse clock	Out

Note:

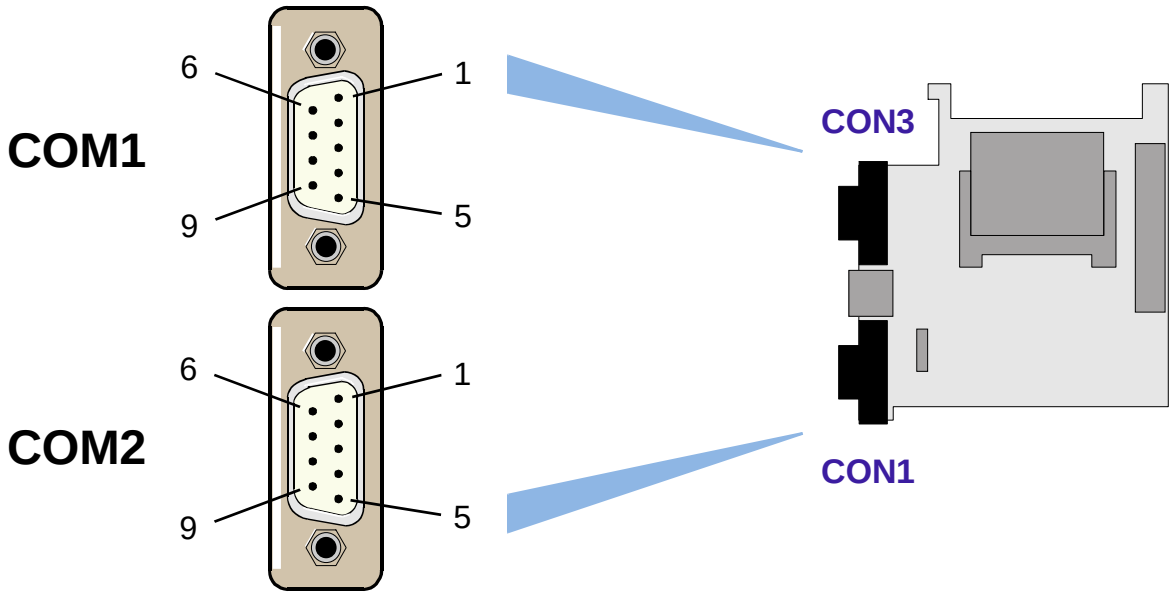
The keyboard power supply is protected with a fuse (500mA) and all the signal lines are EMI-filtered.

A.6.2 Universal Serial Ports (UART)

Two PC-compatible serial 9-pin DSUB ports are available. The two COM ports, which are fully compatible with the 16550 controller, include a complete set of handshaking and modem control signals, maskable interrupt generation and data transfer of up to 460.8 kB/s.

The two COM interfaces are configured as RS232 ports.

Figure A-9: PC-Compatible D-sub Serial Interface Connectors CON1 and CON3



A.6.2.1 Serial Port Connectors CON1 and CON3 Pinouts

The COM1 interface is routed to the connector CON3 and the COM2 interface is routed to CON1.

A.6.2.2 Serial Port Connector CON3 and CON1 Pinout

Table A-3: Serial Port Connector CON3 (COM1) and CON1 (COM2) Pinout

Pin Number	Signal	Function	In/Out
1	DCD	DCD Data carrier detect	In
2	RXD	RXD Receive data	In
3	TXD	TXD Transmit data	Out
4	DTR	DTR Data terminal ready	Out
5	GND	GND Signal ground	--
6	DSR	DSR Data send request	In
7	RTS	RTS Request to send	Out
8	CTS	CTS Clear to send	In
9	RIN	RI Ring indicator	In

A.6.3 EIDE Interface (Primary Port)

The EIDE interface on the CP304-PS2 module comprises two connectors, CON4 and CON7. The CON4 connector is used to connect a CompactFlash device to the CP304-PS2 module. The CON7 connector, situated on the reverse of the board, is used to connect the CP304-PS2 module to the baseboard.

A.6.3.1 CompactFlash Connector CON4

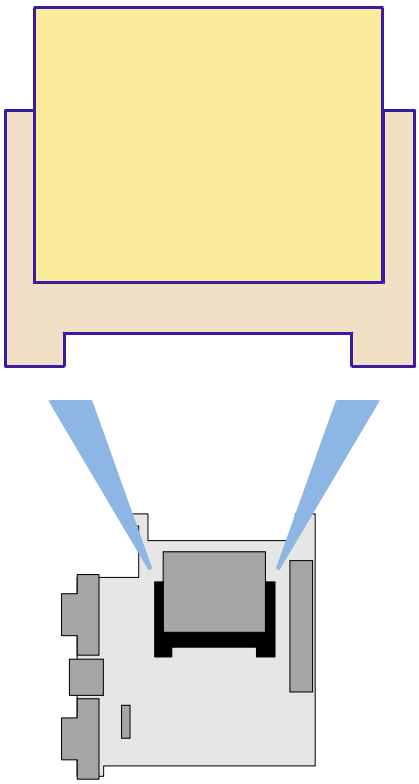
To enable flexible flash extension a CompactFlash (CF) type II socket, CON4, is available.

CF is a very small removable mass storage device. It provides true IDE functionality compatible with the 16 bit ATA/ATAPI-4 interface. CF cards are also available for data storage using the Microdrive hard disk from IBM with up to 1 GB capacity.

The primary EIDE port is connected to the onboard CompactFlash socket.

The board supports both CF types (type I and type II). CompactFlash is available in both CF type I and CF type II cards. The IBM Microdrive is a CF type II card.

Figure A-10: Front Side CompactFlash Interface Connector CON4



The CompactFlash connector pinout appears on the following page

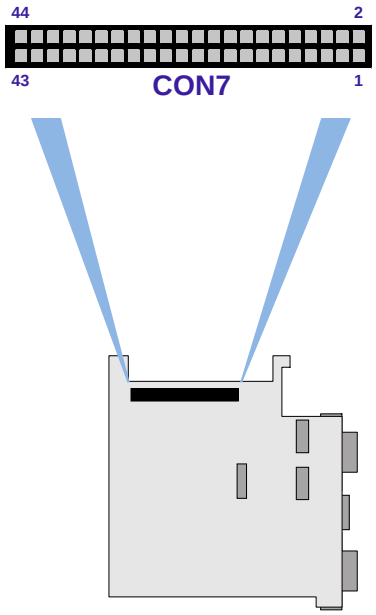
Table A-4: CompactFlash Connector CON4 Pinout

Pin Number	Signal	Function	In/Out
1	GND	Ground signal	--
2	D03	Data 3	In/Out
3	D04	Data 4	In/Out
4	D05	Data 5	In/Out
5	D06	Data 6	In/Out
6	D07	Data 7	In/Out
7	IDE_CS0	Chip select 0	Out
8	GND (A10)	--	--
9	GND (ATASEL)	--	--
10	GND (A09)	--	--
11	GND (A08)	--	--
12	GND (A07)	--	--
13	5 V	5 V power	--
14	GND (A06)	--	--
15	GND (A05)	--	--
16	GND (A04)	--	--
17	GND (A03)	--	--
18	A02	Address 2	Out
19	A01	Address 1	Out
20	A00	Address 0	Out
21	D00	Data 0	In/Out
22	D01	Data 1	In/Out
23	D02	Data 2	In/Out
24	NC (IOCS16)	--	--
25	NC (CD2)	--	--
26	NC (CD1)	--	--
27	D11	Data 11	In/Out
28	D12	Data 12	In/Out
29	D13	Data 13	In/Out
30	D14	Data 14	In/Out
31	D15	Data 15	In/Out
32	IDE_CS1	Chip select 1	Out
33	NC (VS1)	--	--
34	DIOR	I/O read	Out
35	DIOW	I/O write	Out
36	5 V (WE)	5 V power	--
37	INTRQ	Interrupt	In
38	5 V	5 V power	--
39	CSEL (GND pullup)	Master/Slave	Out
40	NC (VS2)	--	--
41	Reset	Reset	Out
42	IORDY	I/O ready	In
43	INPACK	Acknowledge	Out
44	5 V (REG)	5 V power	--
45	NC (ACTIVE)	--	--
46	NC (PDIAG)	--	--
47	D08	Data 08	In/Out
48	D09	Data 09	In/Out
49	D10	Data 10	In/Out
50	GND	--	--

A.6.3.2 Rear Side EIDE Interface Connector CON7

Situated on the reverse of the board, this connector is used to connect the CP304-PS2 module to the baseboard.

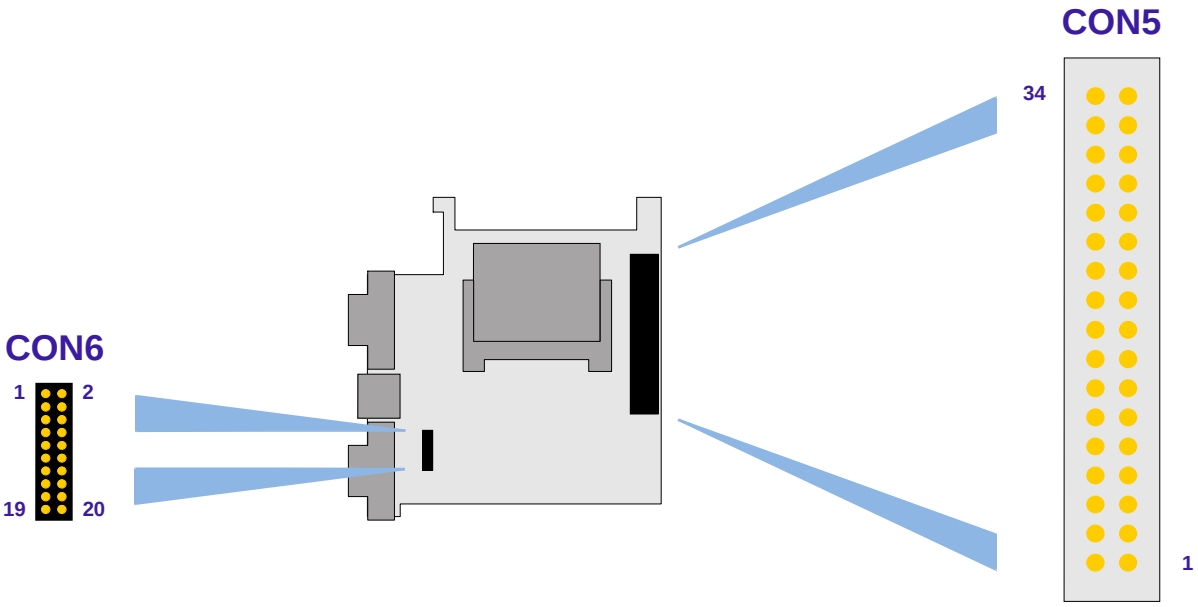
Figure A-11: Rear Side EIDE Interface Connector CON7



A.6.4 Floppy Drive Interface

The floppy drive interface of the CP304-PS2 module is realized as a 34-pin, 2.54-mm pitch pin row connector and a 20-pin connector which provides the signals for an optional floppy-drive that can be installed by means of a special adapter.

Figure A-12: Floppy Drive Interface Connector CON5 and CON6



Note:

The version of the module which carries the Compact Flash interface is equipped with the 34-pin floppy drive connector CON5, while the version without the Compact Flash interface is equipped with the 20-pin floppy drive connector CON6.

The adapter must be mounted directly onto the floppy drive. There is therefore no necessity for an intermediate cable between the floppy drive and the adapter. The adaptor CP-ADAP-FD (order number 20536) may be ordered from Kontron

A.6.4.1 Floppy Drive Connector CON5 Pinout

Please note that all odd numbered pins are used as GND (ground signal)

Table A-5: Floppy Drive Connector CON5 Pinout

Pin Number	Signal	Function	In/out
2	RWC	Write precompensation	Out
4	N/C	--	--
6	N/C	--	--
8	INDEX	Index pulse	In
10	MOTEN1	Motor 1 enable	Out
12	DRVSEL2	Driver select 2	Out
14	DRVSEL1	Driver select 1	Out
16	MOTEN2	Motor 2 enable	Out
18	DIRECTION	Step direction	Out
20	STEP	Step pulse	Out
22	WRDATA	Write data	Out
24	WREN	Write enable	Out
26	TRACK0	Track 0 signal	In
28	WRPROT	Write protect	In
30	RDDATA	Read data	In
32	HEADSEL	Head select	Out
34	DSKCHG	Disk change	In
ODD NUMBERS.	GND	Ground signal	--

A.6.4.2 Floppy Disk Connector CON6

Table A-6: Floppy Disk Connector CON6 Pinout

Pin	Signal	Function	In/Out
1-4	GND	Ground signal	--
5	DSKCH	Disk change	In
6	HDSEL	Head select	Out
7	RDATA	Read data	In
8	WP	Write protect	In
9	TRK0	Track 0 signal	In
10	WGAT	Write enable	Out
11	WDAT	Write data	Out
12	STEP	Step pulse	Out
13	DIR	Step direction	Out
14	MTR1	Motor 1 enable	Out
15	DS0	Driver select 0	Out
16	DS1	Driver select 1	Out
17	MTR0	Motor 0 enable	Out
18	INDEX	Index pulse	In
19	DRVDEN1	Drive and media select	Out
20	DRVDEN0	Drive and media select	Out

Warning!

If the floppy drive connection cable is inverted (pin “1” in place of pin “34”) at “power on”, the floppy drive will work uninterruptedly, with consequent risk of damaging the floppy disk inserted.

A.6.5 I/O Extension Interface Connector CON8, CON9 and CON10

The I/O interface connectors CON8, CON9 and CON10 provide all the necessary signals for the CP304-PS2 module.

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Appendix B

CP-RIO3-01 Rear IO Module

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B. CP-RIO3-01 Rear IO Module

B.1 Overview

The CP304 (and also the CP303, CP302, CP302-PM and CP301) provides optional Rear I/O connectivity for peripherals, a feature which may be particularly useful in specialised CompactPCI systems. Some standard PC interfaces are implemented and assigned to the front panel and to the rear connector J2.

When the Rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus the Rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the system Rear I/O feature a special backplane is necessary. The CPU board with Rear I/O is compatible with all standard CompactPCI passive backplanes with Rear I/O support on the system slot.

The CP-RIO3-01 Rear I/O provides the following interfaces, all signals are available via jumper J2 .

32-bit CompactPCI and Rear I/O

- 32-bit/33 MHz CompactPCI
- PS/2 keyboard (not implemented on CP304)
- PS/2 mouse (not implemented on CP304)
- Two USB ports
- Ethernet port without LED
- Two COM ports
- VGA CRT interface
- Second EIDE port
- Fan control input

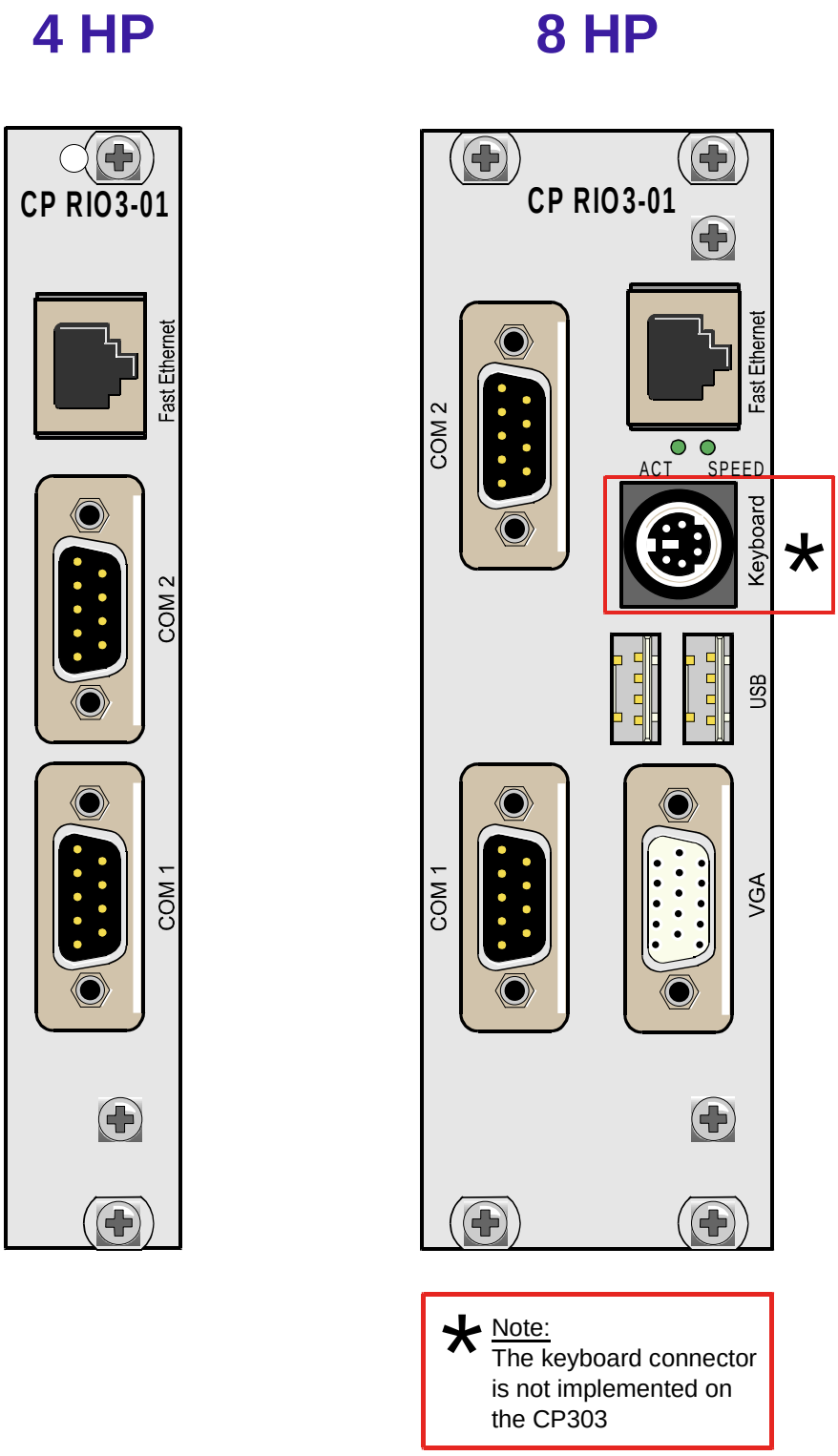
The following ports may be used either for rear or front I/O, the combination of both rear and front is not possible.

- Ethernet port without LED
- Two COM ports
- VGA CRT interface

B.2 Front Panels

Note that the two green Ethernet LED's are not active on the CP-RIO3-01.

Figure B-1: CP-RIO3-01 Front Panels, 4HP and 8HP Versions



B.3 Module Layout: 4HP and 8HP Versions

Figure B-2: CP-RIO3-01 Module Layout, 4HP Version

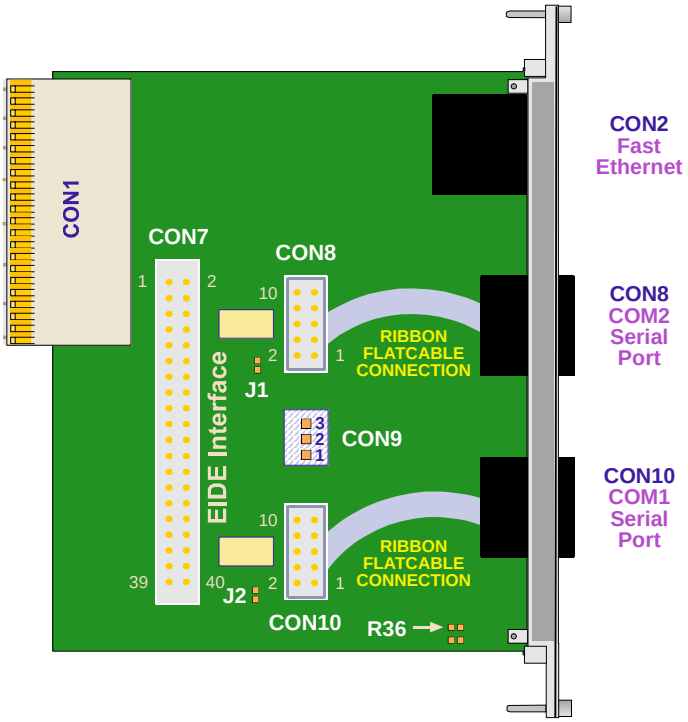
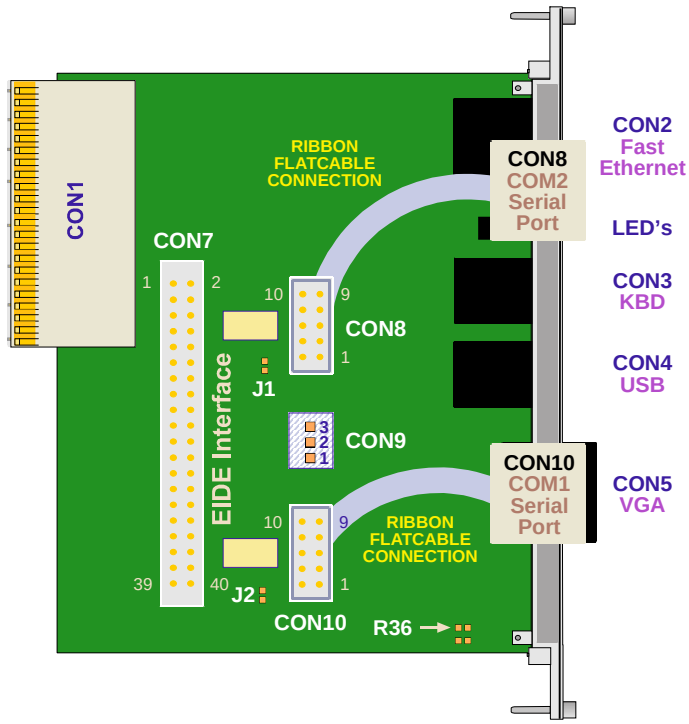


Figure B-3: CP-RIO3-01 Module Layout, 8HP Version



B.4 Module Interfaces

B.4.1 Keyboard/Mouse Interface

Important Note...

The Keyboard/Mouse interface is not implemented on the CP304.

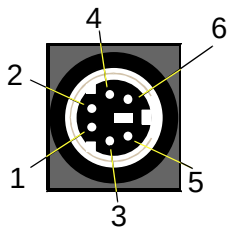


Figure B-4:Keyboard/Mouse Connector

The PC/AT standard keyboard/mouse connector is a PS/2-type 6-pin shielded mini-DIN connector. The keyboard power supply unit is protected by a 500 mA fuse. All signal lines are EMI-filtered.

A special adapter to connect a mouse device and/or a keyboard to the PS/2 connector ia available from *PEP*

B.4.1.1 Keyboard Connector CON3 Pinout

The CP-RIO3-01 (8HP version) has the AT keyboard connector implemented on a 6-pin Mini-Din connector.

A special adapter to connect a mouse device and/or keyboard to the PS/2 connector is available from *PEP*.

Table B-1: Keyboard Connector CON3 Pinout

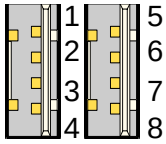
Pin Number	Signal	Function	In/Out
1	KDATA	Keyboard data	In/Out
2	MDATA	Mouse data	In/Out
3	GND	Ground signal	--
4	VCC	VCC signal	--
5	KCLK	Keyboard clock	Out
6	MCLK	Mouse clock	Out

Note:

The keyboard power supply is protected with a fuse (500mA) and all the signal lines are EMI-filtered.

B.4.2 USB Interfaces

Figure B-5: USB Connector CON4



There are two identical USB interfaces on the CP-RIO3-01 module (8HP version) each with a maximum transfer rate of 12 Mbit provided for connecting USB devices. One USB peripheral may be connected to each port. To connect more than two USB devices an external hub is required.

B.4.2.1 USB Connector CON4 Pinout

Table B-2: USB Connector CON4 Pinout

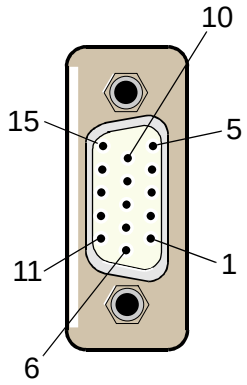
Pin Number	Signal	Function	In/Out
1	VCC	VCC signal	--
2	UV0-	Differential USB-	--
3	UV0+	Differential USB+	--
4	GND	GND signal	--
5	VCC	VCC signal	--
6	UV0-	Differential USB-	--
7	UV0+	Differential USB+	--
8	GND	GND signal	--

Note:

The USB power supply feeding the two ports is protected by a 1.5 A fuse. All signal lines are EMI-filtered.

B.4.3 VGA Interface

Figure B-6: D-sub VGA Connector



B.4.3.1 VGA Connector CON5 Pinout

The 15-pin female connector CON5 is used to connect a VGA monitor to the CP-RIO3-01 (8HP version) board.

Table B-3: VGA Connector CON5 Pinout

Pin Number	Signal	Function	In/Out
1	Red	Red video signal output	Out
2	Green	Green video signal output	Out
3	Blue	Blue video signal output	Out
13	Hsync	Horizontal sync.	TTL out
14	Vsync	Vertical sync.	TTL out
12	Sdata	Not supported	In/Out
15	Sclk	Not supported	Out
9	VCC	Power +5V 200 mA no fuse protection	Out
5,6,7,8,10	GND	Signal ground	--
4,11	Free	--	--

Note:

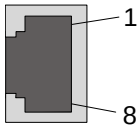
The 75 Ohm termination resistors for the three VGA signals (red, green, blue) are located on the baseboard.

B.4.4 Fast Ethernet Interface

Note...

Only one Fast Ethernet interface may be used; the 2nd is not available.

Figure B-7: Ethernet/Fast Ethernet Connector



The Ethernet connector is realized as an RJ45 twisted-pair connector. The interface provides automatic detection and switching between 10Base-T and 100Base-TX data transmission.

B.4.4.1 RJ45 Connector CON2 Pinout

CON2 supplies the 10Base-TX/100Base-TX interface to the Ethernet controller.

Table B-4: RJ45 Connector CON2 Pinout

Pin Number	Signal	Function	In/Out
1	TX+	Transmit +	Out
2	TX-	Transmit -	Out
3	RX+	Receive +	In
4	NC	--	--
5	NC	--	--
6	RX-	Receive -	In
7	NC	--	--
8	NC	--	--

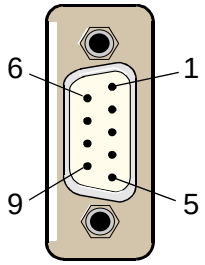
B.4.5 Ethernet LED Status

Important note:

The two green Ethernet LED’s are not active on the CP-RIO3-01.

B.4.6 Serial Port Interfaces

Figure B-8:PC-compatible D-sub Serial Interface



B.4.6.1 Serial Port Connectors CON8 and CON10 Pinouts

The serial port male connectors CON2 and CON6 allow the connection of RS232 devices to the CP-RIO3-01 board.

Table B-5: Serial Port Connectors CON8 and CON10 Pinouts

Pin Number	Signal	Function	In/Out
1	DCD	Data carrier detect	In
2	RXD	Receive data	In
3	TXD	Transmit data	Out
4	DTR	Data terminal ready	Out
5	GND	Signal ground	--
6	DSR	Data send request	In
7	RTS	Request to send	Out
8	CTS	Clear to send	In
9	RI	Ring indicator	In

Note:

To ensure the proper functioning of the Rear I/O serial interfaces, the drivers for COM1 and COM2 on the CP302 I/O module must be disabled.

B.4.7 Fan Control Interface (optional)

A fan for CPU cooling can be connected via the power connector CON9.

B.4.7.1 Fan Control Connector CON9 Pinout

Table B-6: Fan Control Connector CON9 Pinout

Pin Number	Function
1	Ground
2	5V Fan Supply Voltage at a maximum current of 300 mA
3	Fansense

B.4.8 EIDE Interface

B.4.8.1 EIDE Connector EIDE2 (CON7) Pinout

The following table sets out the pin numbers of connector CON7 and sets out its corresponding signal names and functions.

Table B-7: Pinout of AT Standard Connector EIDE2

Pin Number	Signal	Function	In/Out
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	N/C	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--
25	IOR	I/O read	Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	N/C		--
33	A1	Address 1	Out
34	N/C	--	--
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	LED	LED driving	In
40	GND	Ground signal	--

B.4.9 Rear I/O interface on Compact PCI Connector CON1

The CP-RIO3-01 conducts a wide range of I/O signals through the Rear I/O connector J2.

Note:

If the Rear I/O feature is selected the PCI interface is only 32-bit. For the 3U Rear I/O a special backplane is necessary.

Table B-8: Rear I/O CompactPCI Bus Connector J2 (CON2) Pinout

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	TDN1	RDN1	RDP1	GND
20	GND	CLK5	GND	TDP1	GND	VCC	GND
19	GND	GND	GND	RES	RES	+3.3V	GND
18	GND	RDN2	UV0-	UV3+	RTC Bat	+3.3V	GND
17	GND	RDP2	ROUT (GND)	PRST	REQ6	GNT6	GND
16	GND	TDN2	UV0+	DEG	GND	UV3-	GND
15	GND	TDP2	GOUT (GND)	FAL	REQ5	GNT5	GND
14	GND	2RIN	2DSR	2RTS	VSYNC (GND)	2CTS	GND
13	GND	2RXD	FANSENSE (GND)	BOUT (VIO)	2DTR	2DCD	GND
12	GND	1DSR	1RTS	1CTS	HSYNC (GND)	2TXD	GND
11	GND	1DTR	GND	--	1DCD	1RIN	GND
10	GND	--	--	1TXD	GND	1RXD	GND
9	GND	--	--	--	--	--	GND
8	GND	--	--	--	GND	--	GND
7	GND	--	--	--	--	--	GND
6	GND	--	--	--	GND	--	GND
5	GND	--	GND	--	--	GPLED	GND
4	GND	VIO	VCC	--	GND	--	GND
3	GND	CLK4	GND	GNT3	REQ4	GNT4	GND
2	GND	CLK2	CLK3	SSYSEN	GNT2	REQ3	GND
1	GND	CLK1	GND	REQ1	GNT1	REQ2	GND

The legend for this table appears on the next page

Legend for table B-8 on preceding page

Ethernet1

TDP1/TDN1	Transmit Differential Pair.
RDP1/RDN1	Receive Differential Pair.

Ethernet2

TDP2/TDN2	Transmit Differential Pair.
RDP2/RDN2	Receive Differential Pair.

USB ports

USB1+/-	USB data differential data signals
USB3+/-	USB data differential data signals

Serial Port 1

S1*	Serial port signals; TTL level

Serial Port 2

S2*	Serial port signals; TTL level

CONTROL Signals

FANSENSE	Schmitt Trigger fan tachometer inputs; TTL level

VGA CRT signals

ROUT	Red signal
GOUT	Green signal
BOUT	Blue signal
HSYNC	Horizontal Sync.
VSYNC	Vertical Sync.

Reserved Signals

RES	Reserved (leave open)

B.5 Jumper Setting

B.5.1 COM Port Configuration

The two COM ports are configured using solder jumpers J1 and J2

B.5.1.1 COM1 Configuration

Table B-9: COM1 Configuration using Jumper J2

J2	Function
Open	RS232 enabled
Closed	RS232 disabled

The default setting is indicated by italics.

B.5.1.2 COM2 Configuration

Table B-10:COM2 Configuration using Jumper J1

J1	Function
Open	RS232 enabled
Closed	RS232 disabled

The default setting is indicated by italics.

B.5.2 Shorting Chassis GND (Shield) to Logic GND

The front panel including the front panel connectors are isolated to the logic ground. This zero Ohm resistor enables connection between the chassis GND and logic GND.

Table B-11:Shorting Chassis GND (Shield) to Logic GND

R36	Function
Open	Connectors are isolated to logic GND
Short	Connectors are connected to logic GND and chassis GND

The default setting is indicated by italics.

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Appendix C

CP-RIO3-02 Rear IO Module

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C. CP-RIO3-02 Rear IO Module

C.1 Overview

The CP304 (and also the CP303, CP302, CP302-PM and CP301) provides optional Rear I/O connectivity for peripherals, a feature which may be particularly useful in specialised CompactPCI systems. Some standard PC interfaces are implemented and assigned to the front panel and to the rear connector J2.

When the Rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus the Rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the system Rear I/O feature a special backplane is necessary. The CPU board with Rear I/O is compatible with all standard CompactPCI passive backplanes with Rear I/O support on the system slot.

The CP-RIO3-02 Rear I/O provides the following interfaces, all signals are available via connector P2 .

32-bit CompactPCI and Rear I/O

- 32-bit/33 MHz CompactPCI
- Two USB ports
- Two Ethernet ports without LED
- Two COM ports
- VGA CRT interface
- Fan control input

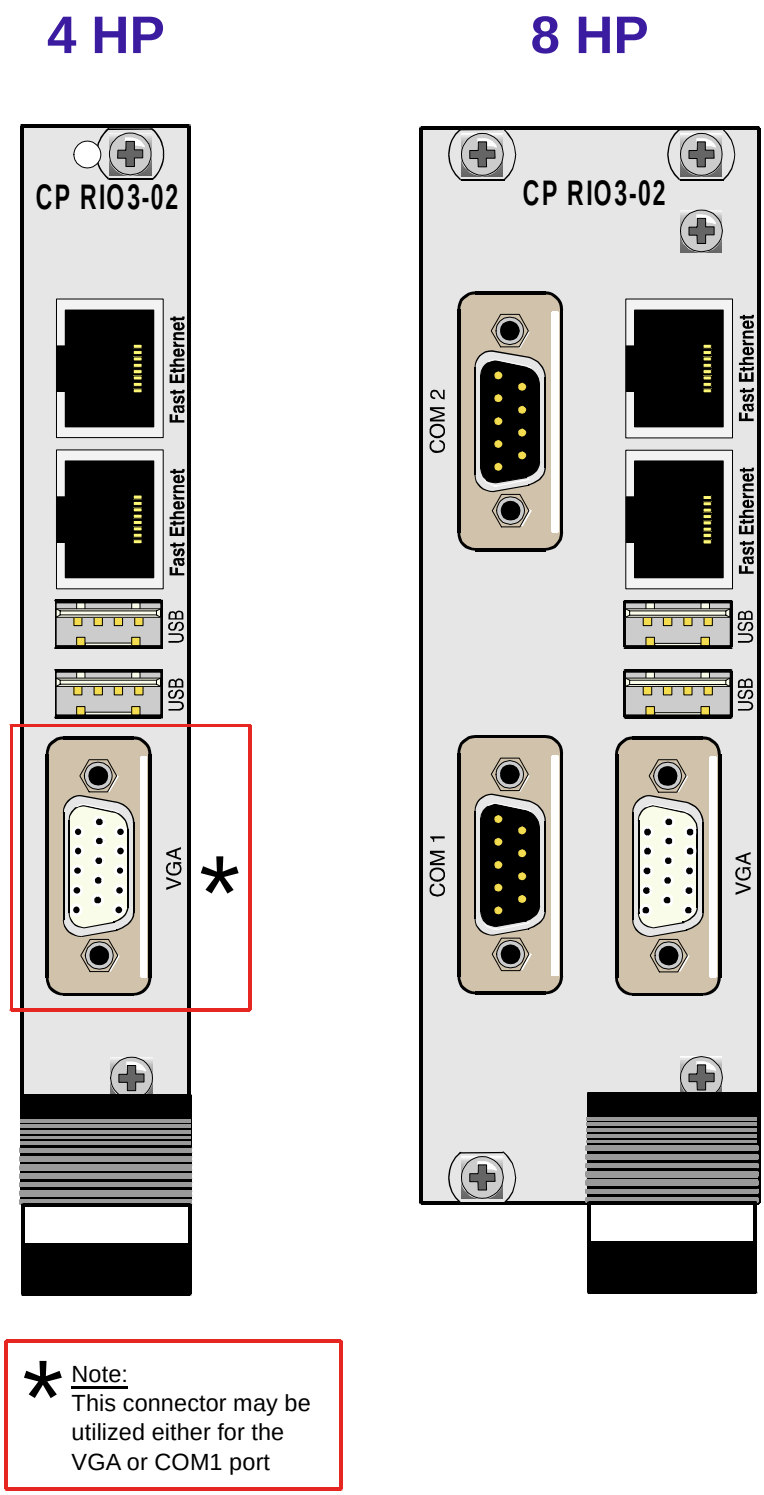
The following ports may be used either for rear or front I/O, the combination of both rear and front is not possible.

- The two Ethernet ports without LED’s
- Two COM ports
- VGA CRT interface

C.2 Front Panels

Note that the four Ethernet LED's are not active on the CP-RIO3-02.

Figure C-1: CP-RIO3-02 Front Panels, 4HP and 8HP Versions



C.3 Module Layout: 4HP and 8HP Versions

Figure C-2: CP-RIO3-02 Module Layout, 4HP Version

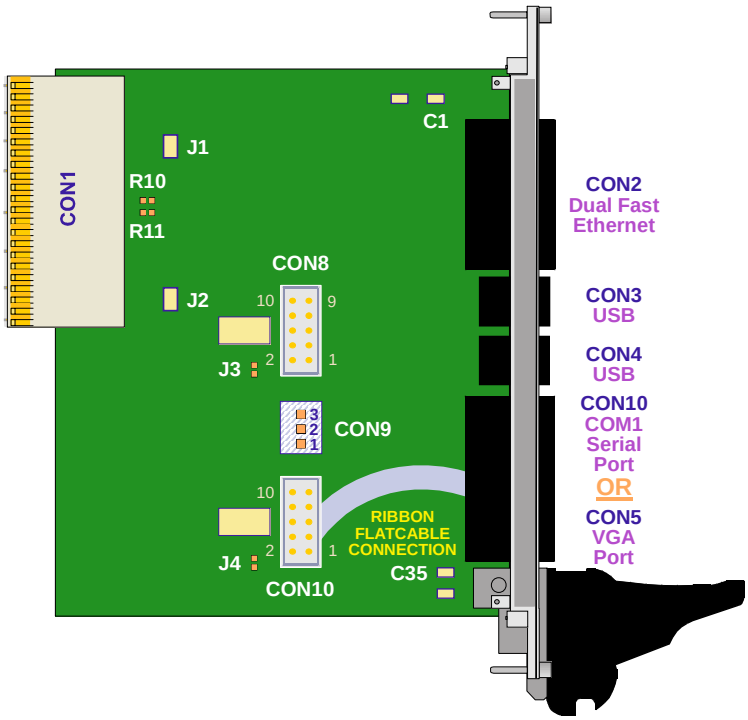
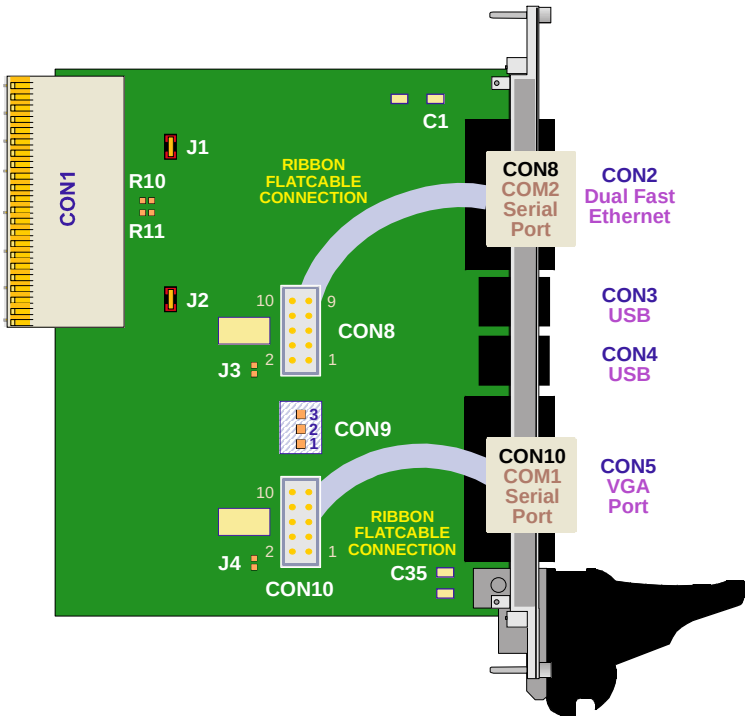


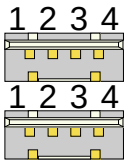
Figure C-3: CP-RIO3-02 Module Layout, 8HP Version



C.4 Module Interfaces

C.4.1 USB Interfaces

Figure C-4: USB Connectors CON3 and CON4



There are two identical USB interfaces on the CP-RIO3-02 module (8HP version) each with a maximum transfer rate of 12 Mbit provided for connecting USB devices. One USB peripheral may be connected to each port. To connect more than two USB devices an external hub is required.

C.4.1.1 USB Connectors CON3 and CON4 Pinout

Table C-1: USB Connectors CON3 and CON4 Pinout

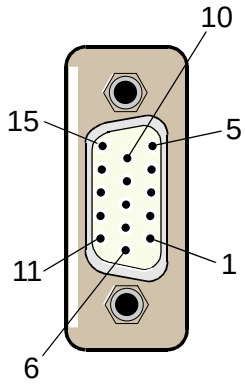
Pin Number	Signal	Function	In/Out
1	VCC	VCC signal	--
2	UV0-	Differential USB-	--
3	UV0+	Differential USB+	--
4	GND	GND signal	--
5	VCC	VCC signal	--
6	UV0-	Differential USB-	--
7	UV0+	Differential USB+	--
8	GND	GND signal	--

Note:

The USB power supply feeding the two ports is protected by a 500 mA fuse. All signal lines are EMI-filtered.

C.4.2 VGA Interface

Figure C-5: D-sub VGA Connector CON5



C.4.2.1 VGA Connector CON5 Pinout

The 15-pin female connector CON5 is used to connect a VGA monitor to the CP-RIO3-02 board.

Table C-2: VGA Connector CON5 Pinout

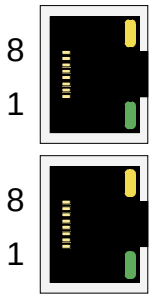
Pin Number	Signal	Function	In/Out
1	Red	Red video signal output	Out
2	Green	Green video signal output	Out
3	Blue	Blue video signal output	Out
13	Hsync	Horizontal sync.	TTL out
14	Vsync	Vertical sync.	TTL out
12	Sdata	Not supported	In/Out
15	Sclk	Not supported	Out
9	VCC	Power +5V 200 mA no fuse protection	Out
5,6,7,8,10	GND	Signal ground	--
4,11	Free	--	--

Note:

The 75 Ohm termination resistors for the three VGA signals (red, green, blue) are located on the baseboard.

C.4.3 Fast Ethernet Interfaces

Figure C-6: Dual Ethernet/Fast Ethernet Connector CON2



The Ethernet connector are realized as RJ45 twisted-pair connectors. The interfaces provide automatic detection and switching between 10Base-T and 100Base-TX data transmission.

C.4.3.1 RJ45 Connector CON2 Pinout

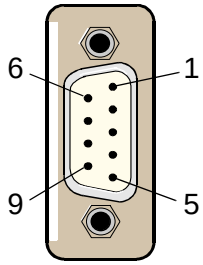
CON2 supplies the 10Base-TX/100Base-TX interface to the Ethernet controller.

Table C-3: RJ45 Connector CON2 Pinout

Pin Number	Signal	Function	In/Out
1	TX+	Transmit +	Out
2	TX-	Transmit -	Out
3	RX+	Receive +	In
4	NC	--	--
5	NC	--	--
6	RX-	Receive -	In
7	NC	--	--
8	NC	--	--

C.4.4 Serial Port Interfaces

Figure C-7:PC-compatible D-sub Serial Interface



C.4.4.1 Serial Port Connectors CON8 and CON10 Pinouts

The serial port male connectors CON8 and CON10 allow the connection of RS232 devices to the CP-RIO3-02 board.

Table C-4: Serial Port Connectors CON8 and CON10 Pinouts

Pin Number	Signal	Function	In/Out
1	DCD	Data carrier detect	In
2	RXD	Receive data	In
3	TXD	Transmit data	Out
4	DTR	Data terminal ready	Out
5	GND	Signal ground	--
6	DSR	Data send request	In
7	RTS	Request to send	Out
8	CTS	Clear to send	In
9	RI	Ring indicator	In

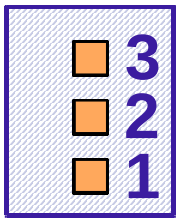
Note:

To ensure the proper functioning of the Rear I/O serial interfaces, the drivers for COM1 and COM2 on the CP304 module must be disabled.

C.4.5 Fan Control Interface (optional)

A fan for CPU cooling can be connected via the power connector CON9.

Figure C-8: Fan Control Interface Connector CON9



C.4.5.1 Fan Control Connector CON9 Pinout

Table C-5: Fan Control Connector CON9 Pinout

Pin Number	Signal	Function	In/Out
1	GND	Ground	--
2	VCC	5V Fan Supply Voltage at a maximum current of 300 mA	Out
3	FAN	Fansense	In

C.4.5.2 External LED

An external LED can be plugged to this jumper.

Table C-6: J2 External LED

Pin Number	Signal	Function	In/Out
1	LED	LED Control	Out max. 4mA
2	VCC	Power	Out max. 10mA

C.4.6 Rear I/O interface on Compact PCI Connector CON1

The CP-RIO3-02 conducts a wide range of I/O signals through the Rear I/O connector J2.

Note:

If the Rear I/O feature is selected the PCI interface is only 32-bit. For the 3U Rear I/O a special backplane is necessary.

Table C-7: Rear I/O CompactPCI Bus Connector J2 (CON2) Pinout

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND	TDN1	RDN1	RDP1	GND
20	GND	CLK5	GND	TDP1	GND	VCC	GND
19	GND	GND	GND	RES	RES	+3.3V	GND
18	GND	RDN2	UV0-	UV3+	RTC Bat	+3.3V	GND
17	GND	RDP2	ROUT (GND)	PRST	REQ6	GNT6	GND
16	GND	TDN2	UV0+	DEG	GND	UV3-	GND
15	GND	TDP2	GOUT (GND)	FAL	REQ5	GNT5	GND
14	GND	2RIN	2DSR	2RTS	VSYNC (GND)	2CTS	GND
13	GND	2RXD	FANSENSE (GND)	BOUT (VIO)	2DTR	2DCD	GND
12	GND	1DSR	1RTS	1CTS	HSYNC (GND)	2TXD	GND
11	GND	1DTR	BOUT (GND)	--	1DCD	1RIN	GND
10	GND	--	--	1TXD	GND	1RXD	GND
9	GND	--	--	--	--	--	GND
8	GND	--	--	--	GND	--	GND
7	GND	--	--	--	--	--	GND
6	GND	--	--	--	GND	--	GND
5	GND	--	GND	--	--	GPLED	GND
4	GND	VIO	VCC	--	GND	--	GND
3	GND	CLK4	GND	GNT3	REQ4	GNT4	GND
2	GND	CLK2	CLK3	SSYSEN	GNT2	REQ3	GND
1	GND	CLK1	GND	REQ1	GNT1	REQ2	GND

Legend for table on preceding page

Ethernet1

TDP1/TDN1	Transmit Differential Pair.
RDP1/RDN1	Receive Differential Pair.

Ethernet2

TDP2/TDN2	Transmit Differential Pair.
RDP2/RDN2	Receive Differential Pair.

USB ports

USB1+/-	USB data differential data signals
USB3+/-	USB data differential data signals

Serial Port 1

S1*	Serial port signals; TTL level

Serial Port 2

S2*	Serial port signals; TTL level

CONTROL Signals

FANSENSE	Schmitt Trigger fan tachometer inputs; TTL level

VGA CRT signals

ROUT	Red signal
GOUT	Green signal
BOUT*	Blue signal
HSYNC	Horizontal Sync.
VSYNC	Vertical Sync.

* Note that this signal (BOUT) appears twice in the rear I/O compactPCI bus connector J2 pinout in order to provide compatibility with the CP302. Pin number B11 refers to the CP304 and C13 refers to the CP302. The default configuration is CP304 (B11).

Reserved Signals

RES	Reserved (leave open)

C.5 Jumper Setting

C.5.1 External Reset

An external reset button can be enabled via this jumper.

C.5.1.1 External Reset

Table C-8: Jumper J1 External Reset

J1	Function
Open	*Normal operation*
Closed	System reset

The default setting is indicated by italics.

C.5.2 COM Port Configuration

The two COM ports are configured using solder jumpers J3 and J4

C.5.2.1 COM1 Configuration

Table C-9: COM1 Configuration using Jumper J4

J4	Function
Open	*RS232 enabled*
Closed	RS232 disabled

The default setting is indicated by italics.

C.5.2.2 COM2 Configuration

Table C-10:COM2 Configuration using Jumper J3

J3	Function
Open	*RS232 enabled*
Closed	RS232 disabled

The default setting is indicated by italics.

C.5.3 Shorting Chassis GND (Shield) to Logic GND

The front panel and front panel connectors are isolated to the logic ground.

To enable the connection between the chassis GND and logic GND the capacitors must be exchanged with zero ohm resistors.

Table C-11:Shorting Chassis GND (Shield) to Logic GND

CAPACITOR	SETTING	DESCRIPTION
C1, C35	*Closed 470pF 2KV capacitors*	*Connectors are isolated to logic GND with three 470pF 2KV capacitors*
	Closed zero ohm resistors	Connectors are connected to logic GND and chassis GND

The default setting is indicated by italics.

Errata 1

Manual: 24401

Manual Index: 03

Table of Contents:

This page has been intentionally left blank.

1. Reference: Page 4 - 5, Chapter 4.2, Table 4-5

The referenced information (description in table) is revised as follows:

The following text is added:

Warning!

IRQ5 should normally have only **one** source enabled, otherwise improper system operation may result.

If more than one source is required to be enabled, contact Kontron's technical support before implementing the IRQs.

For events that are not time critical, such as ENUM, DERATE, etc., polling should be considered instead of using an IRQ.

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