kontron

VMP3

PowerPC CPU Board
for VME Applications

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USER GUIDE

E2BRAIN®

The product described in this manual is in compliance with all applied CE standards.

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29230.01.UG.VC.050727/091404

Table of Contents

Chapter 1

29230.01.UG.VC.050727/091405

Chapter 2

Chapter 3

29230.01.UG.VC.050727/091405

Chapter 4

29230.01.UG.VC.050727/091405

Chapter 5

Chapter 6

29230.01.UG.VC.050727/091405

Annex A

Annex B

29230.01.UG.VC.050727/091406

Annex C

List of Tables

29230.01.UG.VC.050727/091406

29230.01.UG.VC.050727/091407

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29230.01.UG.VC.050727/091407

List of Figures

29230.01.UG.VC.050727/091407

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29230.01.UG.VC.050727/091407

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29230.01.UG.VC.050727/091407

Explanation of Symbols

CE Conformity

This symbol indicates that the product described in this manual is in compliance with all applied CE standards. Please refer also to the section “Applied Standards” in this manual.

Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.

Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.

Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.

Note...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

29230.01.UG.VC.050727/091407

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

Warning!

All operations on this device must be carried out by sufficiently skilled personnel only.

Caution, Electric Shock!

Before installing your new Kontron product into a system always ensure that the mains power is switched off. This applies also to the installation of piggybacks.

Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory back-up, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

29230.01.UG.VC.050727/091408

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron Modular Computers GmbH and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered. In the event that the original packaging material is not available for storage or warranty shipments, packaging which complies with the standards indicated in section 1.8 may be used to ensure the proper protection of this product.

Special care is necessary when handling or unpacking the product. Please, consult the special handling and unpacking instruction on the previous page of this manual.

29230.01.UG.VC.050727/091408

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29230.01.UG.VC.050727/091408

Chapter 1

Introduction

29230.01.UG.VC.050727/091408

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29230.01.UG.VC.050727/091408

1. Introduction

The VMP3 is a comprehensive computing platform which brings together the latest advances in computing technology in a board designed for maximum performance, flexibility, and versatility within a rugged compact format.

The VMP3 is designed to accept the E²Brain™ module EB8541 as its core processor unit. This module which is based on the MPC8541E PowerPC CPU – a highly integrated microprocessor containing a PowerPC e500 core – provides a very comprehensive set of system and communications interfaces.

In addition to the standard VME system interface, the VMP3 incorporates a PCI extension interface for a full range of PCI peripherals, two Gigabit Ethernet interfaces, one Fast Ethernet interface, high speed serial connectivity, an optional CompactFlash socket, and an IO extension interface which provides optional high speed serial as well as CAN interfacing, LPC interfacing, and an external I²C interface. For board logic and CPU test and debugging there is a JTAG interface.

The VMP3 employs an OS-independent boot loader that enables the loading of any PowerPC enabled operating system. This boot loader makes an update of the Flash contents and automatically downloads from Flash to SDRAM before booting the OS. For performance reasons the OS is started from the DDR-SDRAM.

The power of the board is greatly enhanced by means of the PCI expansion connector which makes it possible to cascade one or two additional VMP1-IO1 modules onto the board resulting in a total package of up to 14HP. Both VMP1-IO1 modules may be used to carry PMC modules. Given the wide range of PMC modules now available, this feature affords the user a very wide range of options. Additionally, one can substitute a module designed to provide an even greater range of PCI peripherals in place of either of the IO1 modules. These features enable, for example, the connection of the widest range of system I/O components such as various field busses and Ultra 2 SCSI, to name just a few. The complete range of expansion possibilities is thus made available to the user by the VMP3.

29230.01.UG.VC.050727/091408

1.1 Board Overview

1.1.1 Board Introduction

The VMP3 is a VME PowerPC-based single-board computer specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

Some of the VMP3's outstanding features are:

- PowerPC MPC8541E Power QUICC III (e500 core)
- 32 kB data cache
- 32 kB instruction cache
- 256 kB L2 cache
- up to 256 MB DDR-I-SDRAM, 64-bit, 264 MHz with ECC support
- up to 64 MB onboard Flash
- onboard PCI bus with expansion connector
- a Fast Ethernet interface
- two Gigabit Ethernet interfaces
- one serial terminal interface
- an IO extension interface for optional interfacing:
  - up to five high speed serial I/O's (RS232, RS422/485)
  - a CAN interface
  - an LPC interface
  - an I²C interface
- optional CompactFlash socket (6 or 10 HP versions)
- programmable watchdog timer
- programmable hardware delay timer
- real-time clock
- optional versions for PCI expansion
- PCI-to-VME Bridge
- compliance with VITA VME-Specification ANSI / IEEE STD1014-1987 / IEC 821 and 297

1.1.2 Board Specific Information

Major board components of the VMP3 are:

- EB8541 E²Brain™ computer core module
- Tundra Universe II PCI-to-VME bridge (VME A24 / D16 operation)
- CPLD logic device
- Fast Ethernet interface
- Gigabit Ethernet interfaces
- Interfacing connectors for:
  - VME-bus
  - Fast Ethernet
  - Gigabit Ethernet (2)
  - serial Terminal (RJ45)
  - PCI-bus expansion
  - I/O expansion
  - Test and Programming (2)
- Abort and Reset switches
- Monitor and Control (MC) LEDs
- BrainCAP™ heat sink for VMP3

29230.01.UG.VC.050727/091408

1.2 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the VMP3.

Table 1-1: System Relevant Information

SUBJECT	INFORMATION
System Configuration	The VMP3 operates onboard with a PCI system clock frequency of 33.
System Controller	The VMP3 provides first slot detection, therefore it can be the system controller.
Application Interfacing	The application interfacing to the VMP3 must comply with the specifications set forth in this manual.

1.2.1 System Configuration

System configuration is solely a function of the application, however, when implementing applications, precautions must be taken to ensure that the signals of the VMP3 are properly terminated in accordance with the specifications set forth in this manual. For this reason it will be necessary for system integrators to ensure proper signal conditioning for their applications before interfacing with the VMP3. In addition, it is imperative that signal interference be kept to a minimum.

1.2.2 Operating Software

The VMP3 is supplied with appropriate operating system and board support software for board operation.

1.3 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

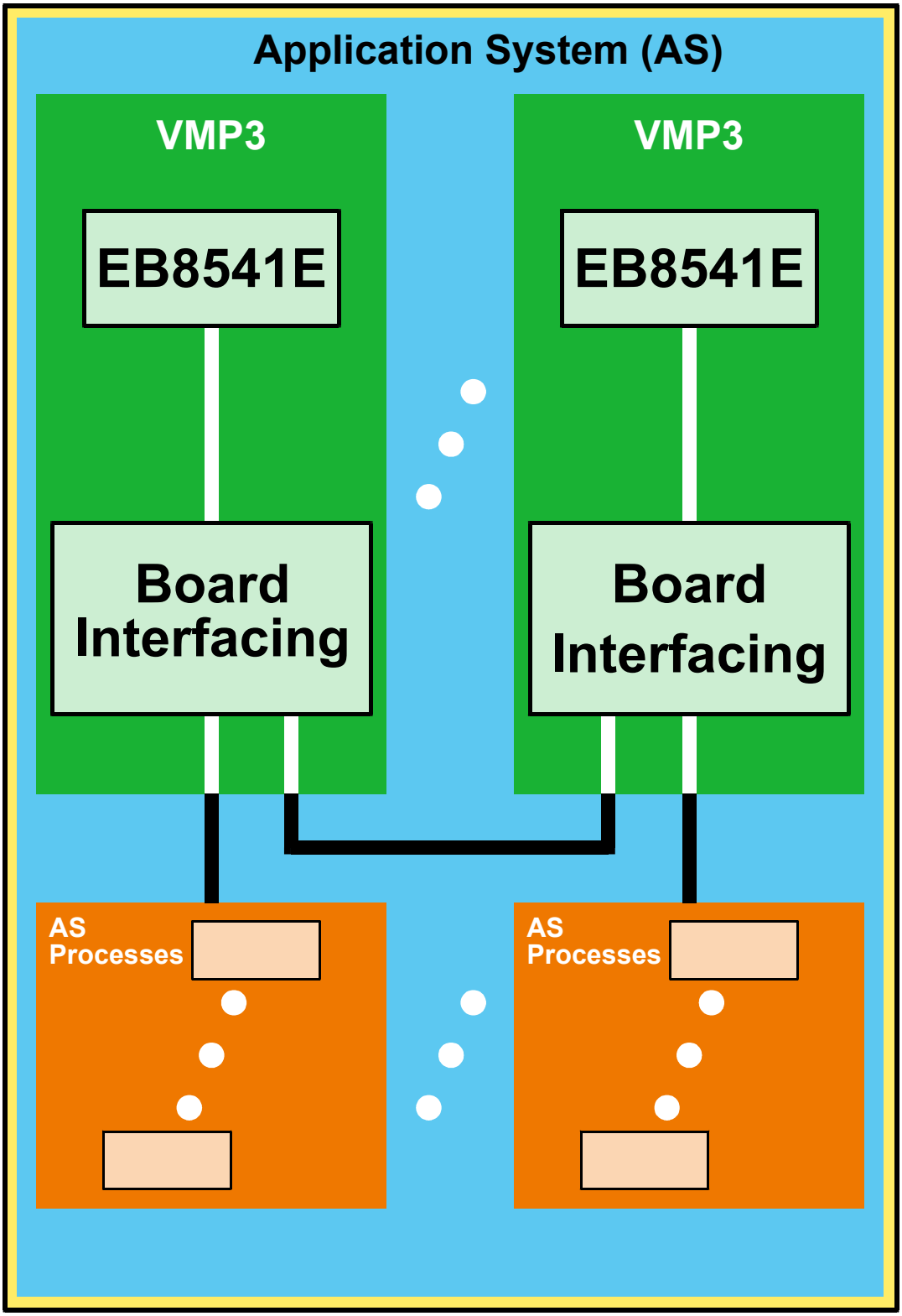
LEGEND FOR FIGURE 1-2:

CAN Communications Area Network
CF CompactFlash
FE Fast Ethernet
HSS High Speed Serial
I²C Inter-Integrated Circuit
LPC Low Pin Count
M/C Monitor and Control
PCI Peripheral Component Interface
T/C Terminal/Console (Serial Interface)
T/P Test/Programming
TSE Gigabit Ethernet (Three Speed Ethernet)

29230.01.UG.VC.050727/091408

1.3.1 Application System Interfacing

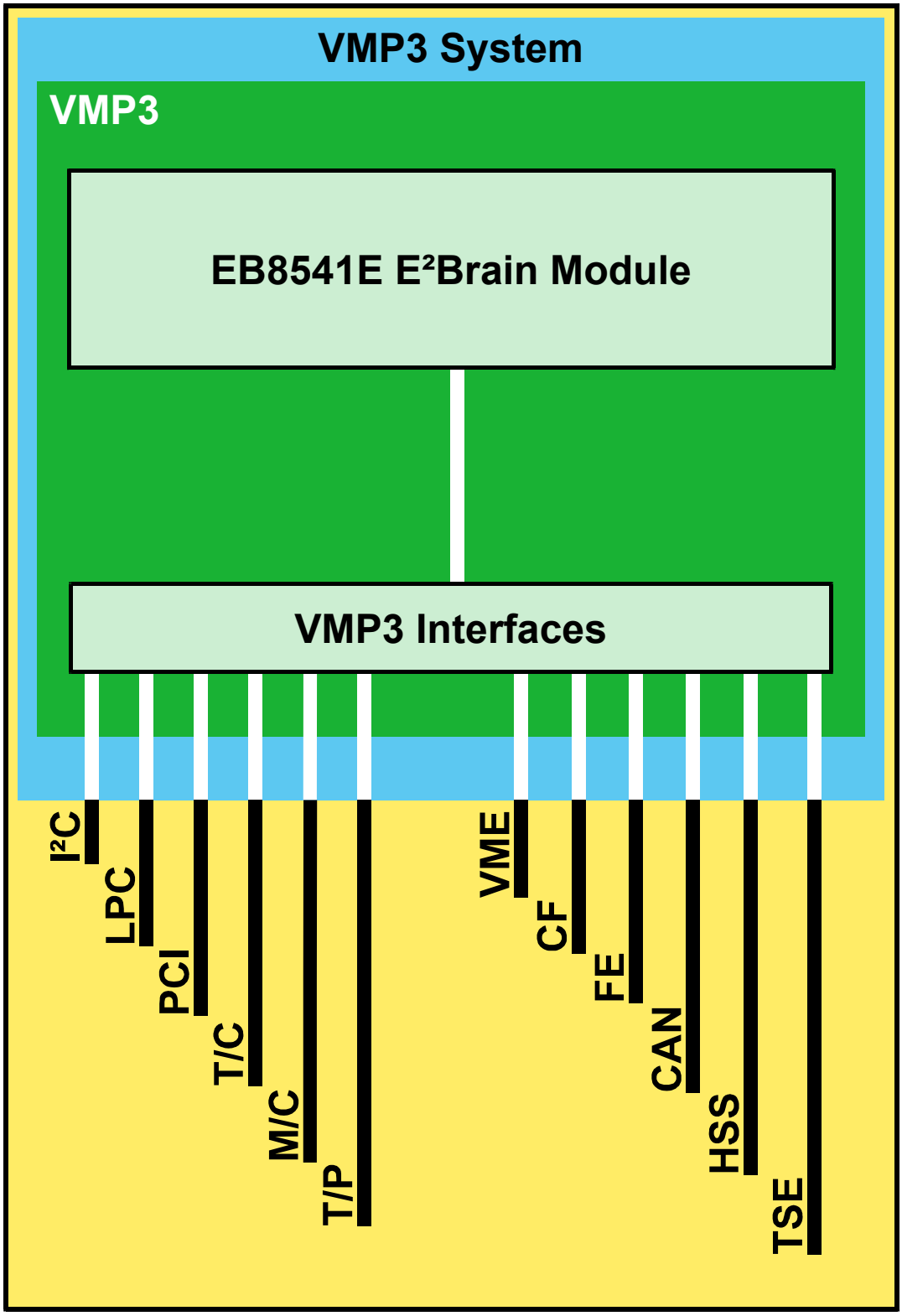
Figure 1-1: VMP3 Application System Interfacing Diagram



29230.01.UG.VC.050727/091408

1.3.2 System Level Interfacing

Figure 1-2: VMP3 System Level Interfacing Diagram



1.3.3 Board Layout

Figure 1-3: VMP3 Board (Front View Without E²Brain™ Module)

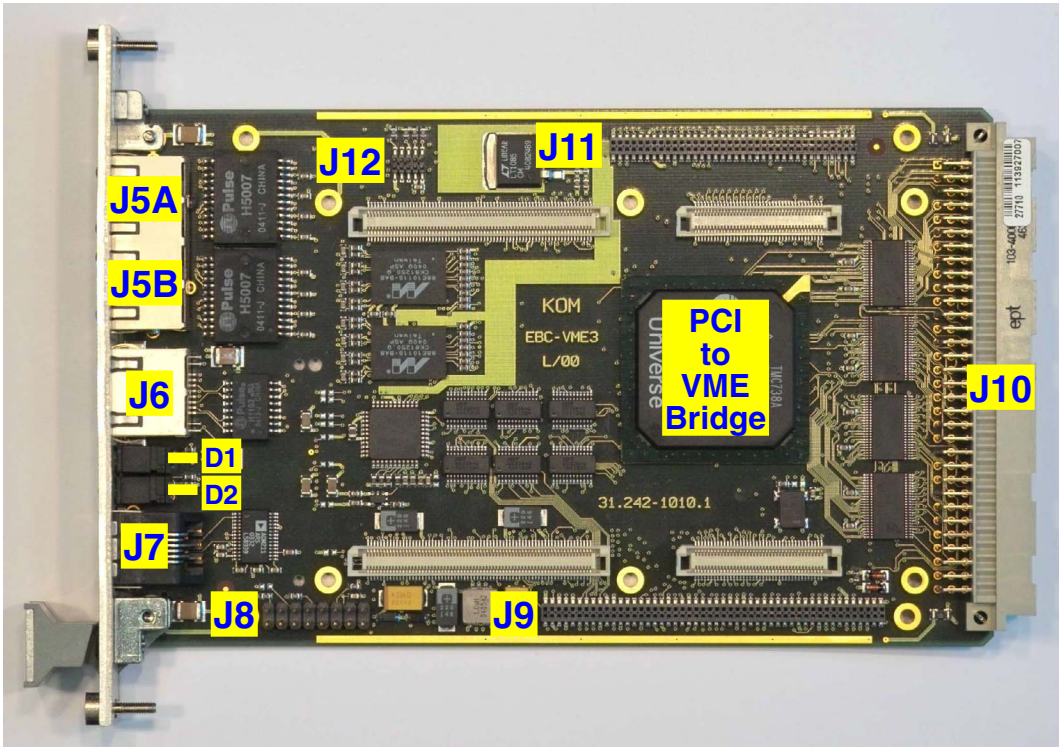
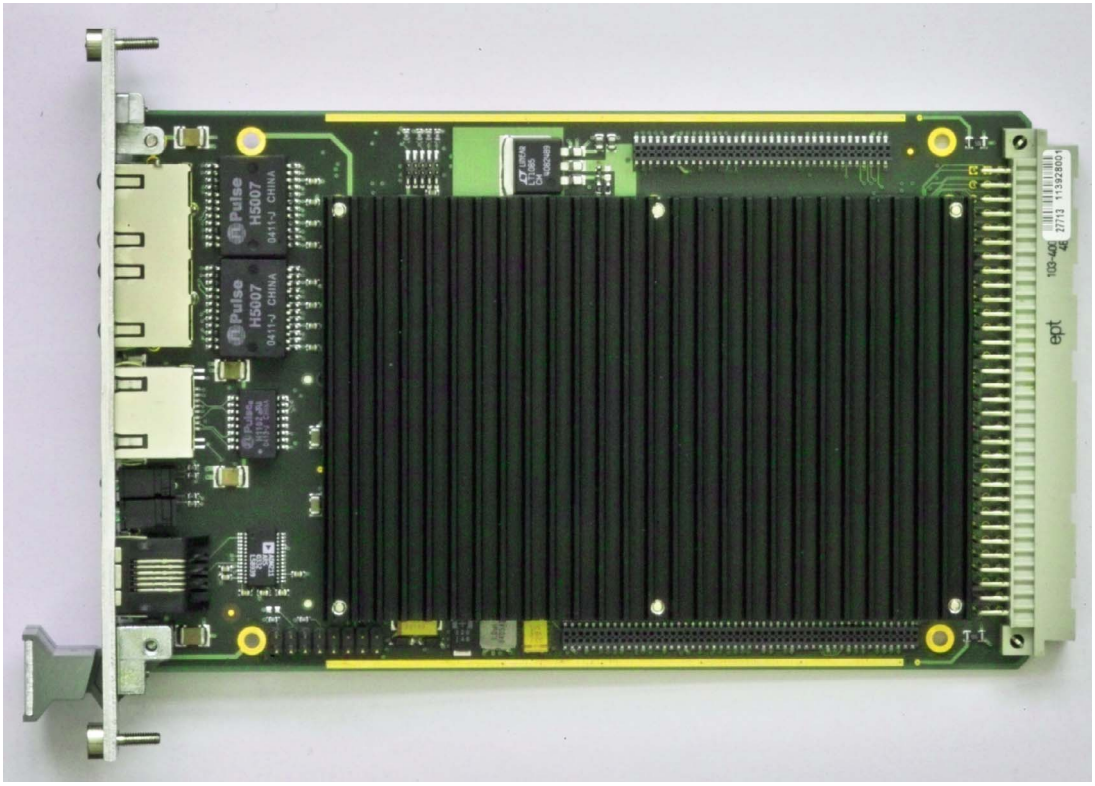


Figure 1-4: VMP3 Board (Front View With E²Brain™ Module)



29230.01.UG.VC.050727/091408

Figure 1-5: VMP3 Board (Rear View)

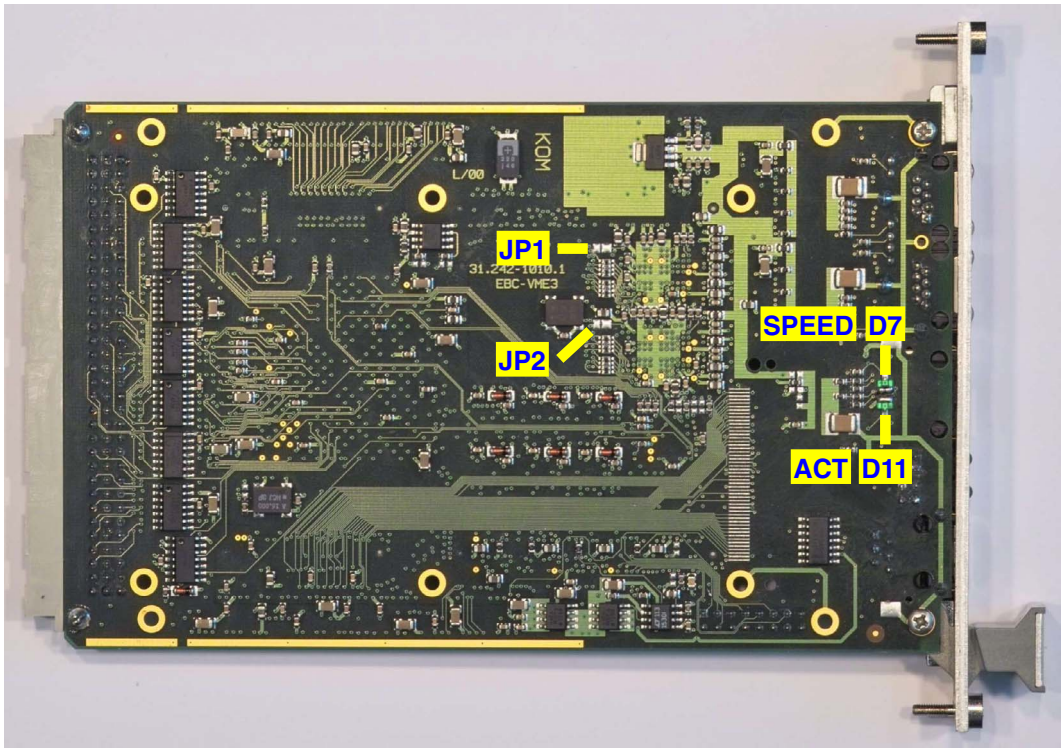


Figure 1-6: VMP3 Board (Rear View with Optional CompactFlash Socket)

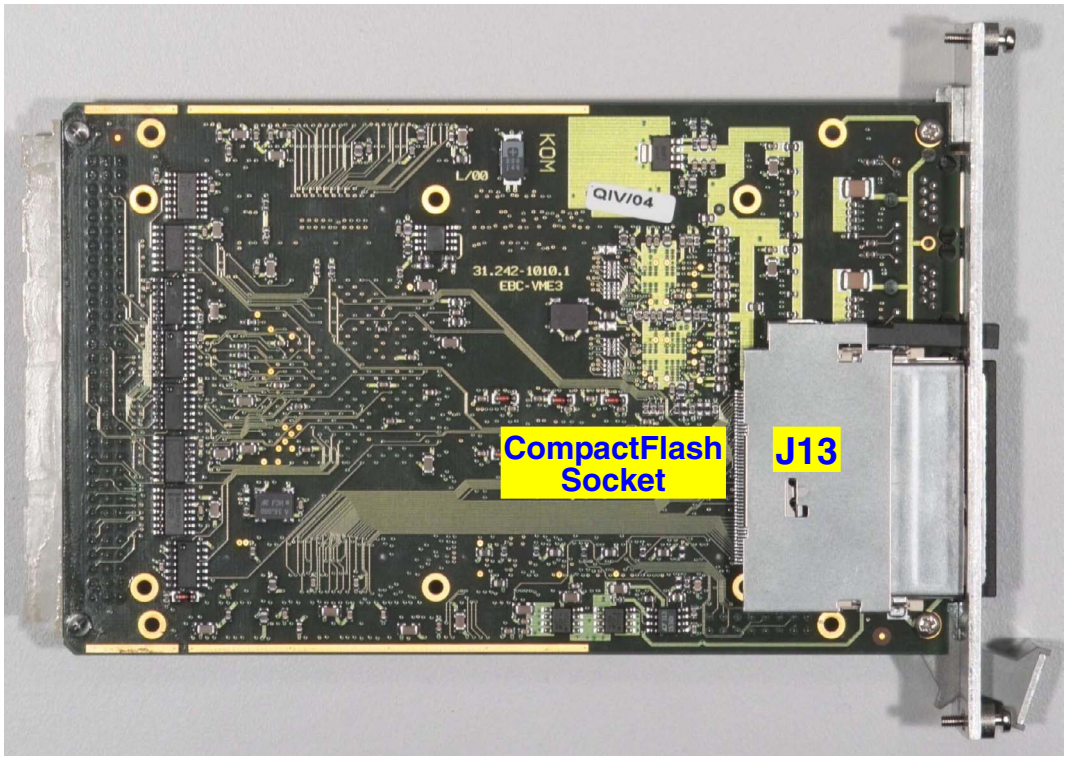
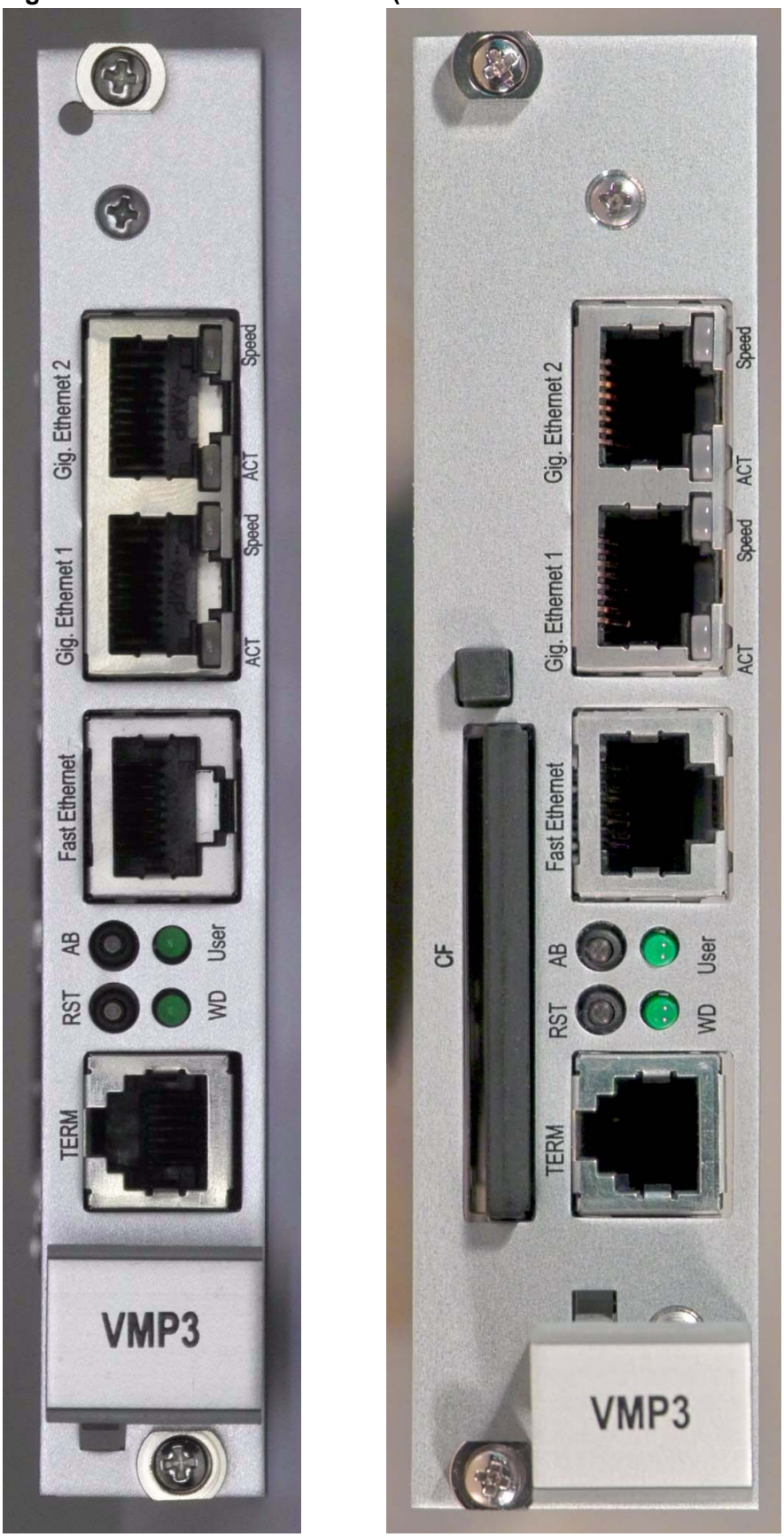


Figure 1-7: VMP3 Front Panels (4HP Standard and 6HP with CompactFlash)



29230.01.UG.VC.050727/091416

1.4 Technical Specifications

Table 1-2: VMP3 Main Specifications

	VMP3	Specifications
Processor and Related	Processor	Motorola MPC8541E Integrated Processor PowerPC, e500 core
	Cache Structure	32 KB instruction cache and 32 KB data cache; L2 cache: 256 KB
	On Chip Controllers	Coherency Module, DDR-SDRAM, OCeaN switch fabric, Local Bus, FCC, TSEs, Security Engine
	Main Memory	Soldered DDR-SDRAM: up to 256 MB, 64-bit, 264 MHz with ECC
	Watchdog	Watchdog generates exception condition: system reset, NMI, or cascading
	RTC	Real-time clock, backed up via VME auxiliary power (+5VSTDBY)
	BPCC	E²Brain™ Board Process/Communications Controller: controls Local Bus interfacing, provides LPC interface and monitor and control functions
Peripheral Memory	SRAM	1 MB soldered, 512k x 16, optionally backed up via auxiliary power (+5VSTDBY)
	EEPROM (I²C)	64 kBit soldered, serial access
	Flash	Minimum of 4 MB and up to 64 MB soldered
External Interfaces	VME	ANSI/VITA 1-1994 for VME, approved April 10.1995 Support for A24:D16/8 master and A24:D16/8 slave interface
	PCI	On-chip controller, 32-bit, 33 MHz, PCI System Master
	LPC	Low Pin Count sub-set, 8-bit IO and memory space access, realized in BPCC
	I²C	On-chip, message interface, full master/slave
	CF	CompactFlash, optional (PIO mode)
	Fast Ethernet	One 10baseT, 100baseTX, FCC integrated in MPC8541E, Intel PHY: LXT 972
	Gigabit Ethernet	Two three speed Ethernet (TSE): 10/100/1000 Mbit GMII (Marvell PHY: 88E1011)
	CAN	Controller Area Network interface (Philips SJA1000)
	Serial Ports	Terminal and Console: Two serial ports: RS232: TERM1 (Terminal on front panel) TTL: TERM2 (Console on I/O expansion) High Speed Serial: Four ports, full modem : SER1 (on I/O expansion) (Local Bus) : SER2 (on I/O expansion) (Support for RS485 direction control) : SER3 (on I/O expansion) : SER4 (on I/O expansion)
T/P Interfaces	JTAG/Debug	JTAG/Debug interface for MPC8541E emulation probe
	In-System Programming	In-System-Programming interface for the VMP3 CPLD logic device

Table 1-2: VMP3 Main Specifications (Continued)

	VMP3	Specifications
M/C Interfaces	LEDs	Six LEDs: One general pupose (USER) One Watchdog (WD) Two Ethernet Activity/Link Two Ethernet Speed
	Switches	Two puch buttons: Reset and Abort
General	Connectors	VME connector, 96-pin Onboard connectors: 1 x RJ12 for RS232; 2 x RJ45 for GigaEthernet; 1 x RJ45 for Fast Ethernet PCI expansion connector: Samtec FLE-150-01-G-DV I/O expansion connector: Samtec FLE-136-01-G-DV
	Power Consumption	Source: 5 V: consumption: 10.85 watts @ 800 MHz (Ethernet not connected)
	Temperature Range	Operational: 0ºC to +60ºC Standard -40ºC to +85ºC E2 (on request) Storage: -55ºC to +125ºC
	Climatic Humidity	93% relative humidity at 40°C, non-condensing
	Dimensions	160 mm L x 100 mm W x 4HP H (minimum height) The maximum height of the VMP3 is a function of the BrainCAP™ options as well as the other possible optional interfaces.
	Board Weight	300 g (4HP); 447 g (8HP)

29230.01.UG.VC.050727/091420

1.5 Applied Standards

The Kontron Modular Computers' VMP3 board complies with the requirements of the following standards:

Table 1-3: Applied Standards

COMPLIANCE	TYPE	STANDARD	TEST LEVEL
CE	Emission	EN55022 EN61000-6-3	--
	Immission	EN55024 EN61000-6-2	--
	Electrical Safety	EN60950	--
Mechanical	Mechanical Dimensions	IEEE 1101.10	--
	Transport and Storage	IEC 61131-2	--
Environmental and Health Aspects	Vibration (sinusoidal)	IEC60068-2-6	10 - 300 [Hz] / 5 [g] / 1 [oct / min] 10 [cycles / axis] 3 [axis: x, y, z]
	Shock	IEC60068-2-27	30 [g] 9 [ms] 3 [shocks per direction] 5 [s] recovery time 6 [directions, ±x, ±y, ±z]
	Bump	IEC60068-2-29	15 [g] 11 [ms] 500 [shocks per axis] 1 [s] recovery time 3 [axis: x, y, z]
	Vibration, broad-band random (digital control) and guidance	IEC60068-2-64	20 - 2000 [Hz] / 3.5 [g RMS] 30 [min.] test time / axis 3 [axis: x, y, z]
	Climatic Humidity	IEC60068-2-78	93% RH at 40°C, non-condensing

1.6 Related Publications

Table 1-4: Related Publications

	ISSUED BY	DOCUMENT
PCI	PCI-SIG	PCI Local Bus Specification, R.2.2
VME	ANSI/VITA	1-1994 for VME
LPC	Intel®	Intel® Low Pin Count (LPC) Interface Specification, Rev. 1.1
I²C	Philips	I2C-BUS SPECIFICATION, Rev. 2.1
E²Brain	Kontron Modular Computers	E²Brain™ Module Specification, Rev. 01

Chapter 2

Functional Description

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2. Functional Description

The following chapters present more detailed, board level information about the VMP3 E²Brain™ High Performance PowerPC Processor VME board whereby the board components and their basic functionality are discussed in general.

2.1 General Information

The VMP3 is comprised basically of the EB8541 E²Brain™ module and the EBC-VME3 carrier board.

The EB8541 E²Brain™ module consists of the following:

- a Motorola MPC8541E Integrated Processor, Power QUICC III with a PPC e500 core
- a Board Process/Communications Controller (BPCC)
- System and Communications interfacing to the EBC-VME3 for:
  - I²C bus
  - LPC bus
  - PCI bus
  - CompactFlash (CF) interface
  - Terminal and Console (T/C) serial interfacing
  - Monitor and Control (M/C) interfacing
  - Test and Programming (T/P) interfacing
  - High Speed Serial (HSS) communications
  - Communications Area Network (CAN) bus
  - Fast Ethernet (FE)
  - Gigabit Ethernet (TSE)
- Memory elements:
  - Main memory DDR-I-SDRAM, soldered
  - Soldered SRAM, backed-up using an auxiliary power line
  - Soldered FLASH
  - Serial EEPROM
- a BrainCAP™ heat sink for the EB8541
- Software
  - Operating system
  - Board support package
  - Boot strap loader (NetBootLoader)

The EB8541 carrier board, EBC-VME3, consists of the following:

- a Tundra Universe II PCI-to-VME bridge and VME-bus connector for VME-bus system interfacing
- PHYs, magnetics, and connectors for Gigabit Ethernet interfacing
- magnetics and connector for Fast Ethernet interfacing
- a Terminal connector for serial interfacing
- a PCI expansion connector for PCI peripheral interfacing
- an I/O expansion connector for additional system and communications interfacing
- two test and programming connectors for JTAG and ISP logic interfacing
- switches and LEDs for Monitor and Control interfacing
- an optional CompactFlash socket for Type I and II CF cards

29230.01.UG.VC.050727/091420

2.2 Board-Level Interfacing Diagram

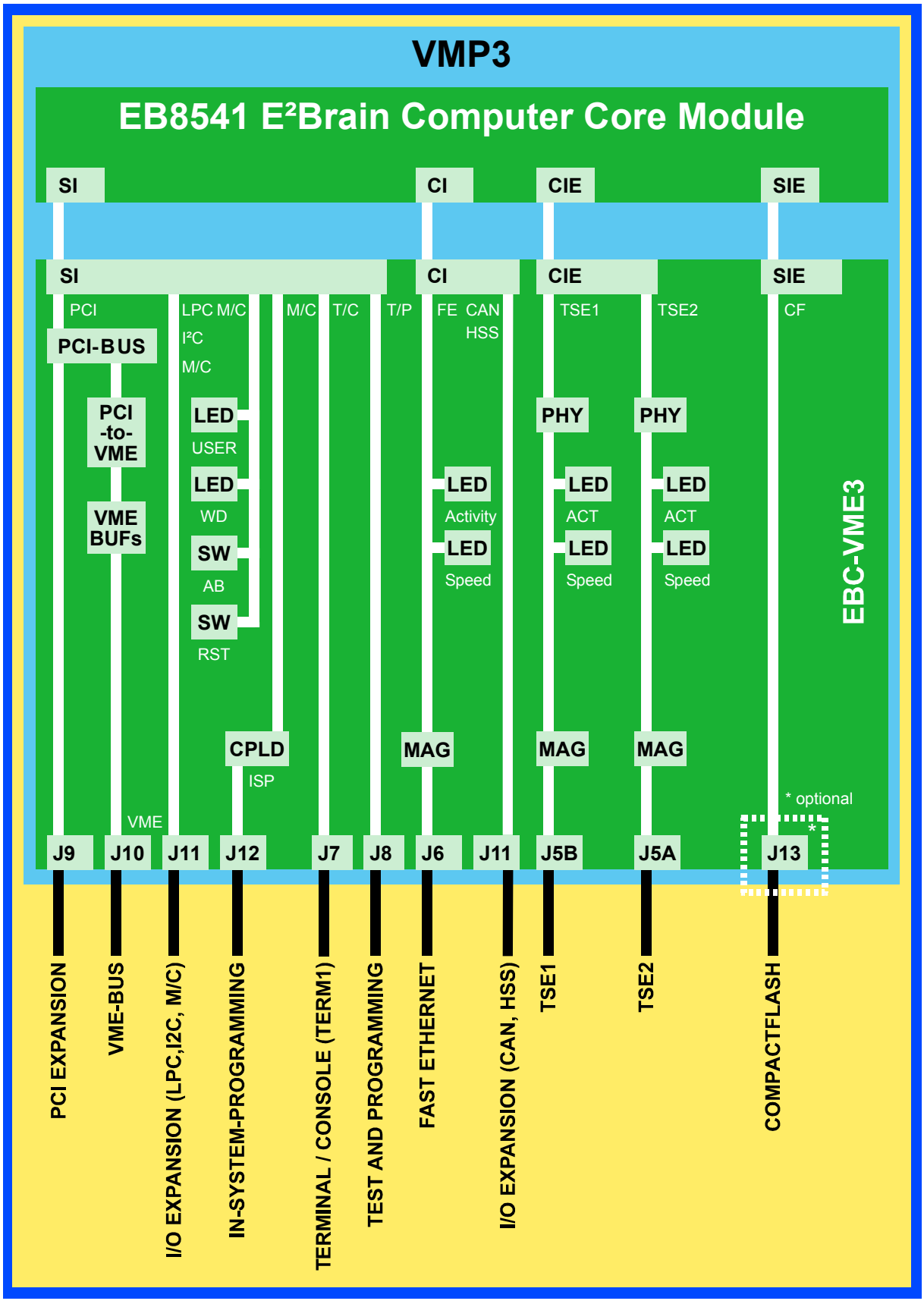
The following figure demonstrates the interfacing structure between the internal processing elements of the EBC-VME3 and other major VMP3 module components. Where system elements have common interfacing they are grouped into a block. Interfacing common to only one element of a block is indicated with a direct connecting line. The interfacing lines are shown in white where they are on board and in black for board external interfacing.

LEGEND FOR FIGURE 2-1

AB	Abort
ACT	Activity
CAN	Communications Area Network
CI	Communications Interface
CIE	Communications Interface Extension
CF	CompactFlash
FE	Fast Ethernet
HSS	High Speed Serial
I²C	Inter-Integrated Circuit
LPC	Low Pin Count
MAG	Magnetics
M/C	Monitor/Control
PCI	Peripheral Component Interface
PHY	PHY
RST	Reset
SI	System Interface
SIE	System Interface Extension
T/C	Terminal/Console (Serial Interface)
T/P	Test/Programming
TSE	Three Speed Ethernet
VME	VME
VME BUFs	VME buffers
WD	Watchdog

29230.01.UG.VC.050727/091420

Figure 2-1: VMP3 Board Level Interfacing



2.3 EB8541 E²Brain™ Module Interfaces

The following sections provide a very brief description of the interfacing between the E²Brain™ module and the EBC-VME3 board.

2.3.1 System Interface

As the name implies, this interface provides the basic application connection functionality required to integrate the EB8541 E²Brain™ module as the high performance core of the VMP3.

The System Interface is realized using a 140-pin, HIROSE FX8C-140P-SV connector. The following table provides an overview of the signal types and a brief description of the interfacing realized on this connector.

Table 2-1: System Interface Signal Types

SIGNAL TYPE	DESCRIPTION
POWER	VMP3 E²Brain™ module input power, grounds, battery backup power, PCI signaling voltage V(I/O)
MONITOR AND CONTROL (M/C)	Control signals for E²Brain™ module operation, configuration, and additional GPIO interfacing
TEST AND PROGRAMMING (T/P)	JTAG/Debug signals for Emulator interfacing
TERMINAL AND CONSOLE (T/C)	Two 2-wire serial interfaces: RxD1/TxD1: Used by the boot loader during startup as a terminal interface; once the system has been booted, is available as general purpose serial interface (Terminal) RxD2/TxD2: general purpose serial interface (Console)
I2C	One I2C standard interface for low speed, serial, inter-chip communications
LPC	One LPC standard interface for (GP)IOs and simple memory interfacing
PCI	One PCI standard interface for PCI-bus interfacing

2.3.2 System Interface Extension

The System Interface Extension is realized using an 80-pin, HIROSE FX8C-80P-SV connector, and it is used to provide CPU architecture specific system interfaces.

In the case of the VMP3, a CompactFlash interface is made available on the System Interface Extension.

Table 2-2: System Interface Extension Signal Types

SIGNAL TYPE	DESCRIPTION
COMPACTFLASH	One CompactFlash interface (true IDE mode)
POWER	VMP3 E²Brain™ module input power and grounds

2.3.3 Communications Interface

The Communications Interface Connector is used to provide a set of standard communications interfaces. In the case of the VMP3, there are three types of interfaces provided: four high speed serial interfaces, one CAN interface, and one Fast Ethernet interface.

29230.01.UG.VC.050727/091420

Table 2-3: Communications Interface Signal Types

SIGNAL TYPE	DESCRIPTION
High Speed Serial (HSS)	Four high speed serial interfaces
Fast Ethernet	One Fast Ethernet 10/100 Mbps interface
CAN	One standard CAN interface

2.3.4 Communications Interface Extension

The Communications Interface Extension is realized using a 140-pin, HIROSE FX8C-140P-SV connector. The following table provides an overview of the signal types and a brief description of the interfacing realized on this connector.

Table 2-4: Communications Interface Extension Signal Type

SIGNAL TYPE	DESCRIPTION
GIGABIT ETHERNET	Two Gigabit Ethernet interfaces (10/100/1000 Mbps, GMII)

2.4 VMP3 Board Interfaces

The following sections provide a specific information regarding the application interfaces available with the EBC-VME3 board.

2.4.1 J10 – VME Interface

The VME interface is based on the TUNDRA UNIVERSE II Bridge which includes the following features required for 3U VME systems.

- A24/A16 addressing modes capability
- D16/D8 data transfer capability
- Automatic First-Slot-Detection
- Single level BR3 arbitration release-when-done option
- FAIR VMEbus arbitration option
- ACFAIL NMI option
- SYSFAIL IRQ option
- System controller functions (SYSCLK, Bus monitor, Power monitor)
- Compatibility with Kontron 3U VME system addressing schemes
- Compatibility with Kontron VME backplane design and feature set
- Compatibility with Kontron backplane transceiver logic

The following figure and table provide pinout and signal information for this interface.

Figure 2-2: J10 - VME Connector

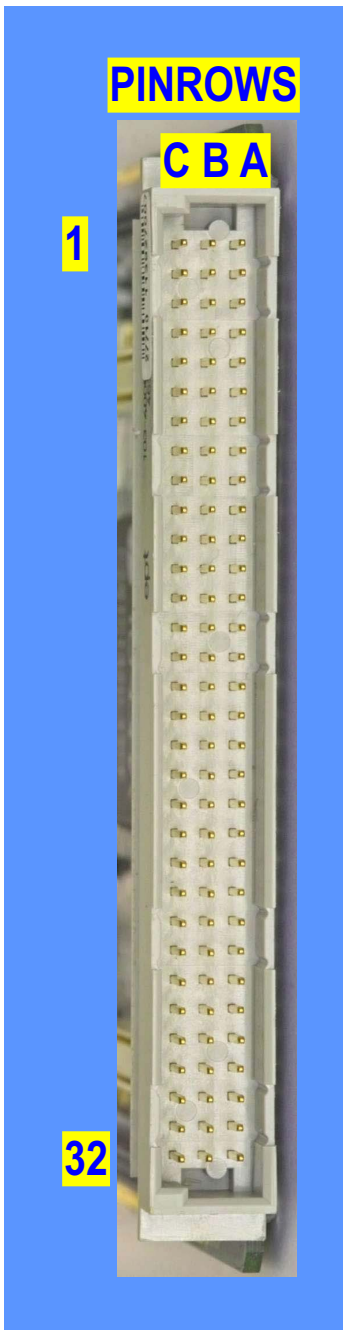


Table 2-5: Pinout of J10 Connector

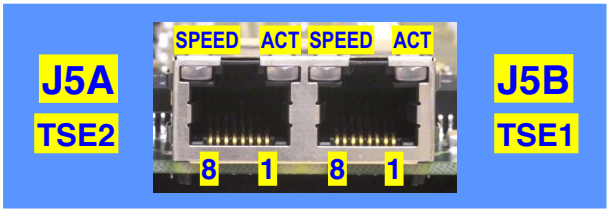
PIN	PINROW A	PINROW B	PINROW C
1	D00	BBSY	D08
2	D01	BCLR	D09
3	D02	ACFAIL	D10
4	D03	BG0IN	D11
5	D04	BG0OUT	D12
6	D05	BG1IN	D13
7	D06	BG1OUT	D14
8	D07	BG2IN	D15
9	GND	BG2OUT	GND
10	SYSCLK	BG3IN	SYSFAIL
11	GND	BG3OUT	BERR
12	DS1	BR0	SYSRESET
13	DS0	BR1	LWORD
14	WRITE	BR2	AM5
15	GND	BR3	A23
16	DTACK	AM0	A22
17	GND	AM1	A21
18	AS	AM2	A20
19	GND	AM3	A19
20	IACK	GND	A18
21	IACKIN	NC	A17
22	IACKOUT	NC	A16
23	AM4	GND	A15
24	A07	IRQ7	A14
25	A06	IRQ6	A13
26	A05	IRQ5	A12
27	A04	IRQ4	A11
28	A03	IRQ3	A10
29	A02	IRQ2	A09
30	A01	IRQ1	A08
31	-12V	+5VSTDBY	+12V
32	+5V	+5V	+5V

2.4.2 J5A/B – Dual Gigabit Ethernet Interface

This connector provides two three speed Ethernet (TSE1 and TSE2) interfaces (10/100/1000 mega-bit operation) for application communications interfacing. This is a dual RJ45 connector with LEDs to indicate the status of the links.

The following figure and table provide pinout and signal information for this interface.

Figure 2-3: J5A/B - Dual Gigabit Ethernet Connector



LED OPERATION:

ACT	OFF:	link not active
	GREEN:	link active
	GREEN BLINKING:	activity on link
SPEED	OFF:	10 Mbps
	GREEN:	100 Mbps
	YELLOW:	1000 Mbps

Table 2-6: Pinouts of J5A and J5B Based on the Implementation

MDI / Standard Ethernet Cable						PIN	MDIX / Crossed Ethernet Cable					
10BASE-T		100BASE-TX		1000BASE-T			10BASE-T		100BASE-TX		1000BASE-T	
I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL		I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
O	TX+	O	TX+	I/O	BI_DA+	1	I	RX+	I	RX+	I/O	BI_DB+
O	TX-	O	TX-	I/O	BI_DA-	2	I	RX-	I	RX-	I/O	BI_DB-
I	RX+	I	RX+	I/O	BI_DB+	3	O	TX+	O	TX+	I/O	BI_DA+
-	-	-	-	I/O	BI_DC+	4	-	-	-	-	I/O	BI_DD+
-	-	-	-	I/O	BI_DC-	5	-	-	-	-	I/O	BI_DD-
I	RX-	I	RX-	I/O	BI_DB-	6	O	TX-	O	TX-	I/O	BI_DA-
-	-	-	-	I/O	BI_DD+	7	-	-	-	-	I/O	BI_DC+
-	-	-	-	I/O	BI_DD-	8	-	-	-	-	I/O	BI_DC-

Note ...

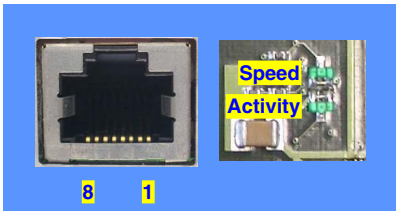
The Gigabit PHYs on the VMP3 support automatic MDI/MDIX crossover at all speeds of operation. Therefore both standard as well as crossed Ethernet cables can be used with these interfaces.

2.4.3 J6 – Fast Ethernet Interface

This connector provides a single Fast Ethernet interface (10/100 mega-bit operation) for application communications interfacing. This is a single RJ45 connector without link status LEDs. Link status LEDs for this interface are located on the bottom side of the EBC-VME3 board.

The following figure and table provide pinout and signal information for this interface.

Figure 2-4: J6 - Fast Ethernet Connector



LED OPERATION:

Activity	**OFF:**	**link not active**
	GREEN:	**link active**
	GREEN BLINKING:	**activity on link**
Speed	**OFF:**	**10 Mbps**
	GREEN:	**100 Mbps**

Table 2-7: Pinout of J6

PIN	SIGNAL	DESCRIPTION
1	TX+	Transmit data +
2	TX-	Transmit data -
3	RX+	Receive data +
4	Terminated	Bob-Smith termination
5	Terminated	Bob-Smith termination
6	RX-	Receive data -
7	Terminated	Bob-Smith termination
9	Terminated	Bob-Smith termination

29230.01.UG.VC.050727/091422

2.4.4 J7 Terminal Interface

The VMP3 provides one serial interface for supporting a terminal port (TERM1). This interface is realized using one of the MPC8541E on-chip UARTs, and as such provides only a two wire interface without hardware handshake signals.

The connector J7 provides interfacing to the TERM1 port. This port can also be used as a low speed solution for firmware updating. The signal levels on this connector are RS232 compliant. The UART itself is a 16550 type UART.

The following figure and table provide pinout and signal information for the TERM1 interface.

Figure 2-5: J7 - TERM Connector

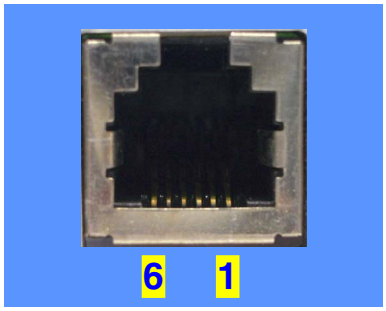


Table 2-8: Pinout of J7

PIN	SIGNAL
1	NC
2	GND
3	TxD1
4	RxD1
5	NC
6	NC

2.4.5 J8 JTAG/Debug Interface

This Test and Programming interface supports JTAG/Debug operations. This interface can be used for connecting hardware emulators and debuggers (e.g. BDM, COP, …). It is comprised of a set of ten signals whereby some are common to both interfaces and some are dedicated to only one.

The following figure and tables provide pinout and signal information for this connector.

Figure 2-6: J8 - JTAG/Debug Connector

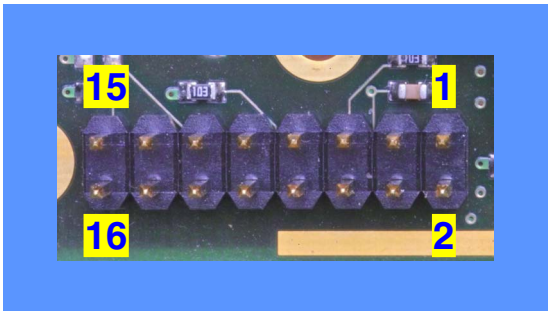


Table 2-9: Pinout of J8

SIGNAL	PIN	PIN	SIGNAL
TDO	1	2	NC
TDI	3	4	TRST
(pulled to +3.3V with 10 kΩ)	5	6	EMU_VCC
TCK	7	8	CHKSTP_IN (pulled to +3.3V with 10 kΩ)
TMS	9	10	NC
SRST	11	12	NC
HRST	13	14	NC
CHKSTP_OUT (pulled to +3.3V with 10 kΩ)	15	16	GND

Table 2-10: JTAG/Debug Signal Descriptions

SIGNAL	DESCRIPTION
TCK	Test Clock in for JTAG and emulator/debugger
TDI	Test Data In for JTAG and emulator/debugger
TDO	Test Data Out JTAG and emulator/debugger
TMS	Test Mode Select, input for JTAG and emulator/debugger
TRST	Test Reset, input for JTAG and emulator/debugger
HRST	Hard Reset, emulator/debugger hard reset input
SRST	Soft Reset, emulator/debugger reset input
CHKSTP_IN	Checkstop input
CHKSTP_OUT	Checkstop output
EMU_VCC	Reference Voltage of the JTAG/DEBUG core

2.4.6 J9 PCI Expansion Interface

The PCI Expansion connector provides the possibility to mount several transition boards above the VMP3 for adding special functionality which is not provided on the VMP3 main board or on the VME bus. All the PCI signals of the onboard PCI bus are routed to this connector, so that a complete PCI bus is provided on this connector. In addition, almost the same number of ground and power pins (3.3V and 5V) as are on a PCI or PMC connector are provided.

Examples of transition boards are:

- PMC carrier
- IO board with Graphic interface, SCSI, etc.

Figure 2-7: J9 PCI Expansion Connector

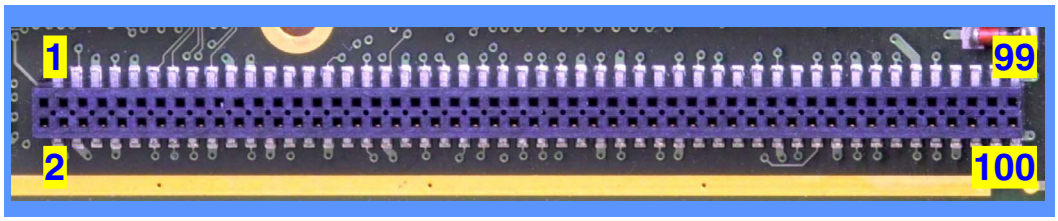


Table 2-11: Pinout of J9

SIGNAL	PIN	PIN	SIGNAL
GND	1	2	SCL (I2C)
RST#	3	4	+3.3V
+3.3V	5	6	CLK1
CLK2	7	8	GND
GND	9	10	NC
INTB#	11	12	INTA#
INTD#	13	14	INTC#
+5V	15	16	GNT1#
GNT2#	17	18	+5V
+3.3V	19	20	NC
GND	21	22	REQ1#
REQ2#	23	24	GND
+5V	25	26	NC
AD31	27	28	AD30
AD29	29	30	+5V
GND	31	32	AD28
AD27	33	34	AD26
AD25	35	36	GND
+3.3V	37	38	AD24
C/BE3	39	40	SDA (I2C)
AD23	41	42	+3.3V
GND	43	44	AD22
AD21	45	46	AD20
AD19	47	48	GND
+5V	49	50	AD18

SIGNAL	PIN	PIN	SIGNAL
AD17	51	52	AD16
C/BE2	53	54	+5V
GND	55	56	FRAME#
IRDY#	57	58	GND
+3.3V	59	60	TRDY#
DEVSEL#	61	62	NC
GND	63	64	STOP#
LOCK#	65	66	+3.3V
PERR#	67	68	+5V
SERR#	69	70	GND
+5V	71	72	PAR
C/BE1	73	74	AD15
AD14	75	76	+3.3V
GND	77	78	AD13
AD12	79	80	AD11
AD10	81	82	GND
GND	83	84	AD9
AD8	85	86	C/BE0
AD7	87	88	+5V
+3.3V	89	90	AD6
AD5	91	92	AD4
AD3	93	94	GND
NC	95	96	AD2
AD1	97	98	AD0
+12V	99	100	-12V

Note...

The PCI signalling voltage is 5V on this connector.

2.4.7 J11 I/O Expansion Interface

The I/O Expansion connector provides additional capability for LPC, TERM2, M/C, CAN, and HSS/UART interfacing. All signals on this connector are at TTL levels which means that they will require additional signal conditioning prior to interfacing to VMP3 external devices.

Figure 2-8: J11 I/O Expansion Connector

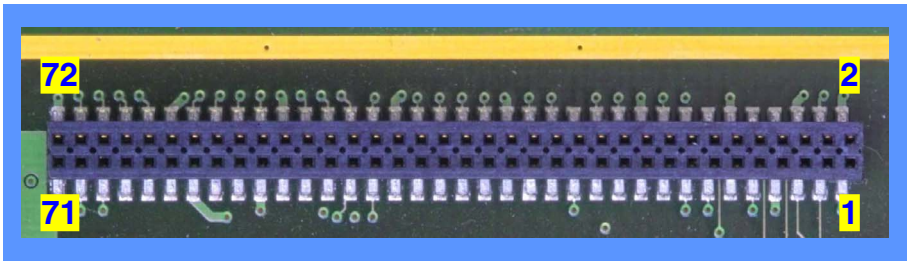


Table 2-12: Pinout of J11

SIGNAL	PIN	PIN	SIGNAL
+BAT (see Note)	1	2	GND
MC4	3	4	LPC_CLK
LAD1	5	6	+3V3
+5V	7	8	LAD0
LAD3	9	10	LAD2
PCI_RST	11	12	GND
TXD2	13	14	LFRAME
RXD2	15	16	+5V
GND	17	18	SERIRQ
CAN1_RX1	19	20	+3V3
CAN1_RX0	21	22	CAN1_TX1
GND	23	24	CAN1_TX0
CAN2_RX1	25	26	+5V
CAN2_RX0	27	28	CAN2_TX1
GND	29	30	CAN2_TX0
SER4_CD	31	32	GND
SER4_RXD	33	34	SER4_DTR
SER4_CTS	35	36	SER4_TXD

SIGNAL	PIN	PIN	SIGNAL
SER4_RI	37	38	SER4_RTS
SER3_CD	39	40	SER4_DSR
SER3_RXD	41	42	GND
SER3_CTS	43	44	SER3_DTR
SER3_RI	45	46	SER3_TXD
+3V3	47	48	SER3_RTS
SER2_CD	49	50	SER3_DSR
SER2_RXD	51	52	GND
GND	53	54	SER2_DTR
SER2_CTS	55	56	SER2_TXD
SER2_RI	57	58	SER2_RTS
+5V	59	60	SER2_DSR
SER1_CD	61	62	+3V3
SER1_RXD	63	64	SER1_DTR
GND	65	66	SER1_TXD
SER1_CTS	67	68	SER1_RTS
SER1_RI	69	70	SER1_DSR
+3V3	71	72	+5V

Note...

+BAT = 3.2V is derived from the 5V standby (is not regulated)

2.4.7.1 LPC Interface

One Low Pin Count (LPC) interface for supporting simple IOs, simple static memory devices, and IO controllers is available via the I/O Expansion interface.

The controller is completely integrated in the BPCC and offers a 8-bit data access port to devices which use LPC IO or memory access protocols. I/O and memory area are selected using different address spaces.

The I/O address space is 64 kByte in size, whereas the memory area offers 16 MByte address space. DMA is not supported by this interface.

In addition, a serial IRQ controller is also implemented in the BPCC, controlling and collecting the serial LPC IRQs and converting and processing them to IRQs for the CPU.

The serial IRQ controller is realized according to the “Serialized IRQ Support for PCI Systems” Specification, Rev. 6.0, Sept. 1, 1995

The following table provides a listing of the LPC interface signals and a brief description.

Table 2-13: LPC Interface Signal Description

SIGNAL	DESCRIPTION
LAD[0:3]	Multiplexed Command, Address, and Data lines
LFRAME#	Indicates start of a new cycle, termination of broken cycle
LPCCLK	33 MHz clock
SERIRQ	Serialized IRQ, optional for peripherals that need interrupt

2.4.7.2 Terminal Interface

A second serial interface for supporting a terminal port and a low speed communications interface (TERM2) for firmware updating is provided on this connector. This interface is realized using one of the MPC8541E on-chip UARTs, and, as such, provides only a two wire interface without hardware handshake signals.

Note...

The corresponding serial signals on the VMP3 are TTL logic level signals. Therefore, the transceivers for RS232 must be provided by the carrier board.

WARNING!

The signal level on the receive lines must not exceed 3.3V. Transients and signal levels higher than 3.3V may damage the VMP3 board.

2.4.7.3 CAN Interface

To provide field bus support, there are signals available to implement a CAN bus interface (Philips SJA 1000) via the J11 connector. The signals provided are at 5V TTL voltage levels and must be adapted to the CAN bus levels through the use of appropriate CAN transceivers on the carrier board.

Table 2-14: CAN Interface Signal Type and Description

SIGNAL	DESCRIPTION
CAN1_TX[0:1]	Transmit data output driver
CAN1_RX[0:1]	Receive data input channel

Note...

For more information concerning interfacing of the SJA 1000 to the CAN PHY, refer to the Philips Application Note: AN97076 or the datasheet of the PCA 82C250 CAN controller interface.

2.4.7.4 High Speed Serial Interfaces

Four, full modem, serial ports (SER1, 2, 3, and 4) are available on the I/O expansion connector. Eight signals per port are provided to realize asynchronous high speed serial links interfaced using dedicated controlling/handshaking. The VMP3 uses DUARTs (EXAR XR 16C2850 or XR16L2750) which are 16550 compatible and provide hardware handshaking support for RS485 operation.

Table 2-15: High Speed Serial Interface Signal Type and Description

SIGNAL	DESCRIPTION
SERn_TXD	Transmit data output
SERn_RXD	Receive data input
SERn_RTS	Request to send output
SERn_CTS	Clear to send input
SERn_DTR	Data terminal ready output
SERn_CD	Carrier detect input
SERn_DSR	Data set ready input
SERn_RI	Ring indicator input

Note...

All signals are available and supplied at 3.3V TTL levels. Further signal conditioning via appropriate transceivers on the carrier board is required to support the respective communications standards.

2.4.7.5 Monitor and Control Interfaces

The I/O expansion connector provides one MC signal: the MC4 which is an input and is used as a boot control signal. Low = boot from LPC device; high or open = boot from onboard FLASH.

2.4.8 J12 In-System-Programming Interface

This programming interface supports in-system-programming of the VMP3 CPLD logic device.

The following figure and table provide pinout and signal information for this connector.

Figure 2-9: J12 In-System-Programming Connector

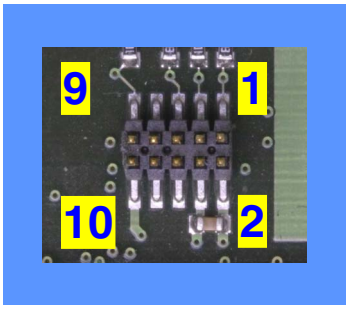


Table 2-16: Pinout of J12

SIGNAL	PIN	PIN	SIGNAL
L_TCK	1	2	GND
L_TDO	3	4	+3V3
L_TMS	5	6	NC
NC	7	8	NC
L_TDI	9	10	GND

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Chapter 3

Installation

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3. Installation

The VMP3 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board or injury to personnel.

3.1 Hardware Installation

The product described in this manual can be installed in any available slot of a VMEbus system. However, to function as a system controller it must be installed in slot 1 (far left).

3.1.1 Safety Requirements

The module must be securely fastened to the carrier board using the mounting standoffs and screws provided with the module.

In addition the following electrical hazard precautions must be observed.

Caution, Electric Shock Hazard!

Ensure that the system main power is removed prior to installing or removing this board. Ensure that there are no other external voltages or signals being applied to this board or other boards within the system. Failure to comply with the above could endanger your life or health and may cause damage to this board or other system components including process-side signal conditioning equipment.

ESD Equipment!

This Kontron board contains electrostatic sensitive devices. Please observe the following precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

Do not touch any on board components, connector pins, or board conductive circuits.

If working at an anti-static workbench with professional discharging equipment, ensure compliance with its usage when handling this product.

29230.01.UG.VC.050727/091427

3.1.2 Installation Procedures

To install the board proceed as follows:

1. Ensure that the safety requirements indicated above are observed.

Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation. Please refer to chapter 4 for configuration information.

2. Ensure that the board is properly configured for operation before installing.

Note...

Care must be taken when applying the procedures below to ensure that when the board is inserted it is not damaged through contact with other boards in the system.

3. Install the board in the appropriate slot and ensure that it is properly seated in the backplane (front panel is flush with the rack front).
4. Fasten the front panel retaining screws.
5. Connect external interfacing cables to the board as required.
6. Ensure that the board and interfacing cables are properly secured.

3.1.3 Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated above are observed.

Warning!

Care must be taken when applying the procedures below to ensure that when the board is removed it is not damaged through contact with other boards in the system. This applies in particular when complementary boards are connected to the VMP3 via the J9 or J11 connectors. In this case, both boards must be removed together as a unit and not separately.

2. Disconnect any interfacing cables that may be connected to the board.
3. Loosen the front panel retaining screws.
4. Disengage the board from the backplane by pressing down on the front panel handle and pull the board out of the slot.
5. Dispose of the module as required observing applicable environmental regulations governing the handling and disposition of this type of product.

29230.01.UG.VC.050727/091427

Note...

If the removed board is to be returned to the manufacturer, ensure that the packaging and ESD requirements are observed as specified by the following sections of this guide:

- page xv, "Special Handling and Unpacking Instructions"
- page xvi, "General Instructions on Usage"
- section 1.8, "Applied Standards"

3.2 Software Installation

Software installation is a function of the NetBootLoader and is described in chapter 5 of this manual.

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Chapter 4

Configuration

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4. Configuration

The following sections provide system integrators with detailed information for configuring the VMP3 module for operation

4.1 Board Address Map

The following table illustrates the address mapping of the VMP3.

Table 4-1: Board Address Map

	AREA NAME	SIZE BYTE	START ADDRESS
OVERLAP	ROM/REGs/ UARTs	32 k	0xFFFF 8000
	CAN	32 k	0xFFFF 0000
	CF	64 k	0xFFFE 0000
	Reserved	896 k	0xFFF0 0000
	MPC8541E REGs	1 M	0xFFE0 0000
	Reserved	2 M	0xFFC0 0000
	SRAM	4 M	0xFF80 0000
	Reserved	8 M	0xFF00 0000
	LPC IO	16 M	0xFE00 0000
	LPC MEM	16 M	0xFD00 0000
	Reserved	16 M	0xFC00 0000
	FLASH	64 M	0xF800 0000
	PCI	2 G	0x9000 0000
	VME	256 M	0x8000 0000
	DDR-SRAM	2 G	0x0000 0000

START ADDRESS	REGISTER NAME	ACC.
0xFFFF E000	ROM	R
0xFFFF C000	Reserved	
0xFFFF A014	Delay Timer Control/Status	R/W
0xFFFF A013	Device Disable Register	R
0xFFFF A011	Serial Interrupt Polarity2	R/W
0xFFFF A010	Serial Interrupt Polarity1	R/W
0xFFFF A00F	Serial Interrupt Mask 2 Register	R/W
0xFFFF A00E	Serial Interrupt Mask 1 Register	R/W
0xFFFF A00D	Serial Interrupt 2 Pending	R/W
0xFFFF A00C	Serial Interrupt 1 Pending	R/W
0xFFFF A00B	Reserved	R/W
0xFFFF A00A	Reserved	R
0xFFFF A009	Board/Logic Revision	R/W
0xFFFF A008	Watchdog Control Register	R/W
0xFFFF A007	Reserved	
0xFFFF A006	Device Interrupt Pending	R/W
0xFFFF A005	Interrupt Config Register	R/W
0xFFFF A004	Event Register	R/W
0xFFFF A003	Control Register	R/W
0xFFFF A002	Memory Configuration Register	R
0xFFFF A001	Software Compatibility ID	R
0xFFFF A000	Board ID	R
0xFFFF 8018	UART_D	R/W
0xFFFF 8010	UART_C	R/W
0xFFFF 8008	UART_B	R/W
0xFFFF 8000	UART_A	R/W

4.2 Board Control Registers

The Board Control registers may be accessed through byte-wide read and write operations.

4.2.1 Board ID Register

The Board ID is used to identify the VMP3 in a E²Brain™ system. The value for the VMP3 is 0x45 which is factory set and cannot be changed.

Table 4-2: Board ID Register

REGISTER NAME	BOARD ID						ACCESS	
ADDRESS	0xFFFF A000						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	BID7	BID6	BID5	BID4	BID3	BID2	BID1	BID0
DEFAULT	0	1	0	0	0	1	0	1

4.2.2 Software Compatibility ID

The Software Compatibility ID will signal to the software when differences in hardware require different handling by the software. It starts with the value 0x00 and will be incremented with each change in hardware (software sensitive only). This register is set at the factory and is for use only by the boot strap loader “NetBootLoader” and the BSP software, and, as such, is not user relevant.

Table 4-3: Software Compatibility ID

REGISTER NAME	SOFTWARE COMPATIBILITY ID						ACCESS	
ADDRESS	0xFFFF A001						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0
DEFAULT	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a

29230.01.UG.VC.050727/091434

4.2.3 Memory Configuration Register

The memory configuration register provides information concerning SDRAM size, ECC, and memory bus clock.

Table 4-4: Memory Configuration Register

REGISTER NAME		MEMORY CONFIGURATION						ACCESS	
ADDRESS		0xFFFF A002						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		res.	SYS_ CLK	MEM BUS CLOCK	ECC	res.	MEM_ SZ1	MEM_ SZ0	res.
DEFAULT		n/a	0	1	0	n/a	n/a	n/a	n/a
BIT	**CONTENT**	**STATE**	**DESCRIPTION**						
0	reserved	0							
		1							
1	MEM_SZ0	0	Memory size: Bit 2 Bit 1 0 0 128 MB (256 Mbit chips) 0 1 256 MB (512 Mbit chips) 1 0 512 MB (1 Gbit chips) 1 1 reserved						
		1							
2	MEM_SZ1	0							
		1							
3	reserved	0							
		1							
4	ECC	0	ECC not available						
		1	ECC available						
5	MEM BUS CLOCK	0	264 MHz (Maximum possible memory bus clock)						
		1	330 MHz (Maximum possible memory bus clock)						
6	SYS_CLK	0	0 = 33 MHz; 1 = 66 MHz						
		1	This information is required in order to configure the PLL settings inside the SOC.						
7	reserved	0							
		1							

4.2.4 Control Register

The Control register provides output interfacing to the application software. Assertion of the appropriate bits by the application software will cause the BPCC to generate outputs accordingly.

During startup, the state of Bit 0 is controlled by the NetBootLoader software. After the startup is completed, the NetBootLoader sets Bit 0 to 1.

Table 4-5: Control Register

REGISTER NAME		CONTROL						ACCESS	
ADDRESS		0xFFFF A003						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		res.	res.	MC10	S_RST	MC9	res.	MC11	MC6
DEFAULT		n/a	n/a	0	n/a	0	n/a	0	n/a
BIT	**CONTENT**	**STATE**	**DESCRIPTION**						
0	MC6	0	Logical high on the MC6 output pin						
		1	Logical low on the MC6 output pin						
1	MC11	0	Logical high on the MC11 output pin						
		1	Logical low on the MC11 output pin						
2	reserved	0							
		1							
3	MC9	0	Logical low on the MC9 output pin						
		1	High impedance (Z) on the MC9 output pin						
4	S_RST	0	no operation						
		1	Causes a complete system reset (S_RST) to be initiated						
5	MC10	0	Logical low on the MC10 output pin						
		1	High impedance (Z) on the MC10 output pin						
6	reserved	0							
		1							
7	reserved	0							
		1							

4.2.5 Event Register

The Event register provides status information about the Watchdog timer and various monitor and control inputs. Depending on the type of event which occurs, interrupts may be generated automatically which then require servicing. The application software is responsible for servicing the interrupts as well as the other events, and, where applicable, the resetting of the event bits.

29230.01.UG.VC.050727/091435

Table 4-6: Event Register

REGISTER NAME		EVENT						ACCESS	
ADDRESS		0xFFFF A004						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		MC5	MC3	res.	MC2	MC8	MC1	ALARM	res.
DEFAULT		n/a	n/a	n/a	n/a	n/a	0	0	n/a
BIT	**CONTENT**	**STATE**	**DESCRIPTION**						
0	reserved	0							
		1							
1	ALARM	0	Indicates that ALARM signal on RTC has not been asserted						
		1	Indicates that ALARM signal on RTC has been asserted						
2	MC1	0	Indicates that the MC1 signal has not been asserted						
		1	Indicates that the MC1 signal has been asserted (This will result in a NMI being generated which can be cleared by writing a '1'.)						
3	MC8	0	Indicates that the EB405 is being operated in Agent mode						
		1	Indicates that the EB405 is being operated in Master mode						
4	MC2	0	Case: MC2_INT_EN = 0 Indicates the status of the MC2 input: electrical: low = 0, high = 1 Case: MC2_INT_EN = 1 (default = 0)						
		1	The falling edge of the signal on MC2 pin sets this bit to '1' and generates the MCInt on the CPU provided it is enabled there (This may be cleared by writing a '1'.)						
5	reserved	0							
		1							
6	MC3	0	Case: MC3_INT_EN = 0 Indicates the status of the MC3 input: electrical: low = 0, high = 1 Case: MC3_INT_EN = 1 (default = 0)						
		1	The falling edge of the signal on MC3 pin sets this bit to '1' and generates the MCInt on the CPU provided it is enabled there (This may be cleared by writing a '1'.)						
7	MC5	0	Case: MC3_INT_EN = 0 Indicates the status of the MC3 input: electrical: low = 0, high = 1 Case: MC3_INT_EN = 1 (default = 0)						
		1	The falling edge of the signal on MC3 pin sets this bit to '1' and generates the MCInt on the CPU provided it is enabled there (This may be cleared by writing a '1'.)						

4.2.6 Interrupt Configuration Register

The interrupt configuration register acts as an interrupt enable register for the MC2, MC3 and MC5 signals.

Table 4-7: Interrupt Configuration Register

REGISTER NAME		INTERRUPT CONFIGURATION						ACCESS	
ADDRESS		0xFFFF A005						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		MC5_INT_EN	MC3_INT_EN	res.	MC2_INT_EN	res.	res.	res.	res.
DEFAULT		0	0	n/a	0	n/a	n/a	n/a	n/a
BIT	**CONTENT**	**STATE**	**DESCRIPTION**						
0	reserved	0							
		1							
1	reserved	0							
		1							
2	reserved	0							
		1							
3	reserved	0							
		1							
4	MC2_INT_EN	0	Disabled						
		1	Enabled						
5	reserved	0							
		1							
6	MC3_INT_EN	0	Disabled						
		1	Enabled						
7	MC5_INT_EN	0	Disabled						
		1	Enabled						

4.2.7 Device Interrupt Pending Register

The Device Interrupt Pending Register is used to identify the source of the pending interrupt request of the following onboard devices:

- Temperature sensor (TEMP)
- Fast Ethernet PHY interrupt (FCC1 and FCC2)
- UARTs (SER1, SER2, SER3, and SER4)

29230.01.UG.VC.050727/091435

Table 4-8: Device Interrupt Pending Register

REGISTER NAME	DEVICE INTERRUPT PENDING						ACCESS	
ADDRESS	0xFFFF A006						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	res.	TEMP	FCC2	FCC1	SER4	SER3	SER2	SER1
DEFAULT	0	0	0	0	0	0	0	0

For information regarding the required hardware resources, refer to chapter “Interrupt Mapping” in this manual. A logical ’1’ indicates that an interrupt has been asserted.

4.2.8 Watchdog Control Register

The Watchdog Control register is the interface between applications and the operating system for controlling the functioning of the Watchdog timer. There are four possible modes of operation involving the Watchdog timer:

- Timer only
- Reset
- Interrupt
- Dual stage

At power on the Watchdog is not enabled. If not required, it is not necessary to enable it. If required, the bits of the Watchdog Control register must be set according to application requirements. To operate the Watchdog, the mode and time period required must first be set and then the Watchdog enabled. Once enabled, the Watchdog can only be disabled or the mode changed by powering down and then up again. To prevent a Watchdog timeout the Watchdog must be retriggered before timing out. This is done by writing a ’1’ to the WTR bit. In the event a Watchdog timeout does occur, the WTE bit is set to ’1’. What transpires after this depends on the mode selected. The four operational Watchdog timer modes are described as follows.

Timer only - In this mode the Watchdog is enabled using the required timeout period. Normally the Watchdog is retriggered by writing a ’1’ to the WTR bit. In the event a timeout occurs, the WTE bit is set to ’1’. This bit can then be polled by the application and handled accordingly. To continue using the Watchdog, write a ’1’ to the WTE bit, and then retrigger the Watchdog using WTR. The WTE bit retains its setting as long as no power down-up is done. Therefore, this bit may be used to verify the status of the Watchdog.

Reset mode - This mode is used to force a hard reset in the event of a Watchdog timeout. To be effective, the hard reset must not be masked or otherwise negated. In addition, the WTE bit is not reset by the hard reset which makes it available if necessary to determine the status of the Watchdog prior to the reset.

Interrupt mode - This mode causes the generation of an interrupt in the event of a Watchdog timeout. The interrupt handling is a function of the application. If required the WTE bit can be used to determine if a Watchdog timeout has occurred.

Dual stage mode - This a complex mode where in the event of a timeout two things occur: 1) an interrupt is generated, and 2) the Watchdog is retriggered automatically. In the event a second timeout occurs immediately following the first timeout, a hard reset will be generated. If the Watchdog is retriggered normally, operation continues. The interrupt generated at the first timeout is available to the application to handle the first timeout if required. As with all of the

29230.01.UG.VC.050727/091435

other modes the WTE bit is available for application use.

Refer to Appendix A for further information regarding the Watchdog functional logic.

Table 4-9: Watchdog Control Register

REGISTER NAME		WATCHDOG CONTROL						ACCESS	
ADDRESS		0xFFFF A008						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		WTE	WDM1	WDM0	WEN/WTR	WTM3	WTM2	WTM1	WTM0
DEFAULT		0	0	0	0	0	0	0	0
BIT	**CONTENT**	**STATE**	**DESCRIPTION**						
0	WTM0	0	Watchdog timeout time: Settings: **WTM3 WTM2 WTM1 WTM0** 0 0 0 0 125 ms 0 0 0 1 250 ms 0 0 1 0 500 ms 0 0 1 1 1 s 0 1 0 0 2 s 0 1 0 1 4 s 0 1 1 0 8 s 0 1 1 1 16 s 1 0 0 0 32 s 1 0 0 1 64 s 1 0 1 0 128 s 1 0 1 1 256 s 1 1 0 0 reserved 1 1 0 1 reserved 1 1 1 0 reserved 1 1 1 1 reserved						
		1							
1	WTM1	0							
		1							
2	WTM2	0							
		1							
3	WTM3	0							
		1							
4	WEN/WTR	0	Indicates that the Watchdog timer has not been enabled. Prior to the Watchdog being enabled, this bit is known as WEN. After the Watchdog is enabled, it is known as WTR. Once the Watchdog timer has been enabled, this bit cannot be reset to 0. As long as the Watchdog timer is enabled it will indicate a 1.						
		1	Indicates that the Watchdog timer is enabled. Writing a '1' to this bit causes the Watchdog to be retriggered to the timer value indicated by bits WTM[3:0].						
5	WMD0	0	Watchdog mode: Settings: **WMD1 WMD0 Mode** 0 0 Timer only 0 1 Reset 1 0 Interrupt 1 1 Dual Stage						
		1							
6	WMD1	0							
		1							
7	WTE	0	Indicates that the Watchdog timer has not expired.						
		1	Indicates that the Watchdog timer has expired. Writing a '1' to this bit resets it to 0.						

4.2.9 Board Logic / Revision Register

The Board Revision Register provides the hardware (BRn) and logic (LRn) status of the board. It is set at the factory and starts with the value 0x00 for the initial board prototypes and will be incremented with each redesign / logic release.

Table 4-10:Board Logic / Revision Register

REGISTER NAME	BOARD LOGIC/REVISION						ACCESS	
ADDRESS	0xFFFF A009						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	LR3	LR2	LR1	LR0	BR3	BR2	BR1	BR0
DEFAULT	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a

4.2.10 Serial Interrupt Pending 1 Register

The Serial Interrupt Pending 1 Register in conjunction with the Serial Interrupt Pending 2 Register is used to identify the source of the pending interrupt request. All serial interrupts are coupled together to one CPU Interrupt (IRQ8). A logical 1 indicates that an interrupt has been asserted.

Table 4-11: Serial Interrupt Pending 1 Register

REGISTER NAME	SERIAL INTERRUPT PENDING 1						ACCESS	
ADDRESS	0xFFFF A00C						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	SIRQ7	SIRQ6	SIRQ5	SIRQ4	SIRQ3	SIRQ2	SIRQ1	SIRQ0
DEFAULT	0	0	0	0	0	0	0	0

4.2.11 Serial Interrupt Pending 2 Register

The Serial Interrupt Pending 2 Register in conjunction with the Serial Interrupt Pending 1 Register is used to identify the source of the pending interrupt request. All serial interrupts are coupled together to one CPU Interrupt (IRQ8). A logical 1 indicates that an interrupt has been asserted.

Table 4-12: Serial Interrupt Pending 2 Register

REGISTER NAME	SERIAL INTERRUPT PENDING 2						ACCESS	
ADDRESS	0xFFFF A00D						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	SIRQ15	SIRQ14	SIRQ13	SIRQ12	SIRQ11	SIRQ10	SIRQ9	SIRQ8
DEFAULT	0	0	0	0	0	0	0	0

4.2.12 Serial Interrupt Mask 1 Register

The Serial Interrupt Mask 1 and 2 Registers enable the generation of a CPU interrupt. Writing a '1' to the bit “SIRQ_ENx” enables the generation of a CPU interrupt and enables the corresponding bit in the Serial Interrupt Pending 1 and 2 Register.

Table 4-13: Serial Interrupt Mask 1 Register

REGISTER NAME	SERIAL INTERRUPT MASK 1						ACCESS	
ADDRESS	0xFFFF A00E						R	W
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	SIRQ_EN 7	SIRQ_EN 6	SIRQ_EN 5	SIRQ_EN 4	SIRQ_EN 3	SIRQ_EN 2	SIRQ_EN 1	SIRQ_EN 0
DEFAULT	0	0	0	0	0	0	0	0

4.2.13 Serial Interrupt Mask 2 Register

The Serial Interrupt Mask Registers 1 and 2 enable the generation of a CPU interrupt. Writing a '1' to the bit “SIRQ_ENx” enables the generation of a CPU interrupt and enables the corresponding bit in the Serial Interrupt Pending Registers 1 and 2.

Table 4-14: Serial Interrupt Mask 2 Register

REGISTER NAME	SERIAL INTERRUPT MASK 2						ACCESS	
ADDRESS	0xFFFF A00F						R	W
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	SIRQ_EN 15	SIRQ_EN 14	SIRQ_EN 13	SIRQ_EN 12	SIRQ_EN 11	SIRQ_EN 10	SIRQ_EN 9	SIRQ_EN 8
DEFAULT	0	0	0	0	0	0	0	0

4.2.14 Serial Interrupt Polarity 1 Register

The Serial Interrupt Polarity 1 Register bits define the polarity of their corresponding serial interrupt. A '1' written to the required bit position results in an active high sensitivity of the corresponding interrupt and vice versa.

Table 4-15: Serial Interrupt Polarity 1 Register

REGISTER NAME	SERIAL INTERRUPT POLARITY 1						ACCESS	
ADDRESS	0xFFFF A010						R	W
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	SerInt_POL 7	SerInt_POL 6	SerInt_POL 5	SerInt_POL 4	SerInt_POL 3	SerInt_POL 2	SerInt_POL 1	SerInt_POL 0
DEFAULT	0	0	0	0	0	0	0	0

4.2.15 Serial Interrupt Polarity 2 Register

The Serial Interrupt Polarity 2 Register bits define the polarity of their corresponding serial interrupt. A '1' written to the required bit position results in an active high sensitivity of the corresponding interrupt and vice versa.

Table 4-16: Serial Interrupt Polarity 2 Register

REGISTER NAME	SERIAL INTERRUPT POLARITY 2						ACCESS	
ADDRESS	0xFFFF A011						R	W
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	SerInt_POL 15	SerInt_POL 14	SerInt_POL 13	SerInt_POL 12	SerInt_POL 11	SerInt_POL 10	SerInt_POL 9	SerInt_POL 8
DEFAULT	0	0	0	0	0	0	0	0

4.2.16 Device Disable Register

The register provides the capability to disable certain internal functions of the CPU and is reserved for manufacturing use only.

Table 4-17: Device Disable Register

REGISTER NAME	DEVICE DISABLE REGISTER						ACCESS	
ADDRESS	0xFFFF A013						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	res.	res.	res.	res.	DIS_ENCR	res.	res.	DIS_PCI
DEFAULT	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a

4.2.17 Delay Timer Control/Status Register

The delay timer provides the capability to realize short, reliable delay times. The delay timer control/status register provides three functions for operating the delay timer. The first function is to indicate the timing intervals available, the second function is to trigger/reset the timer, and the third is to indicate the time elapsed since the initial triggering or the last timer reset.

Writing a 0x00 and then reading the register will provide the timer intervals that are available for application usage. In the case of the VMP3, all of the possible timer intervals are available.

Writing anything other than 0x00 to the register sets the timer to zero and restarts it, and sets all of this register's bits to 0. As time elaspes, interval bits are set accordingly and remain set until the timer is retriggered.

For example, the timer is started, after 1 µs bit 0 is set to 1, after 5 µs bit 1 is set 1. This process continues until all bits are set or the timer is retriggered. Once a bit is set it remains set until the timer is again retriggered.

29230.01.UG.VC.050727/091436

Table 4-18: Delay Timer Control/Status Register

REGISTER NAME		DELAY TIMER CONTROL/STATUS REGISTER						ACCESS	
ADDRESS		0xFFFF A014						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		DTC7	DTC6	DTC5	DTC4	DTC3	DTC2	DTC1	DTC0
DEFAULT		0	0	0	0	0	0	0	0

BIT	CONTENT	STATE	DESCRIPTION
0	DTC0	0 1	The hardware delay timer is operated via one simple 8-bit control/status register. The following table indicates 1) the possible timing intervals provided, and 2) when read, the time elapsed since the last trigger/reset of the timer.
1	DTC1	0 1	
2	DTC2	0 1	
3	DTC3	0 1	
4	DTC4	0 1	
5	DTC5	0 1	
6	DTC6	0 1	
7	DTC7	0 1	

DTC[7:0]	Value	Accuracy
Bit 0:	1 µs	< + 40%
Bit 1:	5 µs	< + 8%
Bit 2:	10 µs	< + 4%
Bit 3:	50 µs	< + 0.8%
Bit 4:	100 µs	< + 0.4%
Bit 5:	250 µs	< + 0.16%
Bit 6:	0.5 ms	< + 0.08%
Bit 7:	1 ms	< + 0.04%

4.3 UART Registers Address Mapping

4.3.1 UART A (SER1)

The following table indicate the address mapping of the UART A (SER1). For a more detailed description please refer to the EXAR XR16C2850 or XR16C2750 DUART manual.

Table 4-19: UART A General Register Set

READ MODE	WRITE MODE	ADDRESS
Receive Holding Register	Transmit Holding Register	0xFFFF 8000
n/a	Interrupt Enable Register	0xFFFF 8001
Interrupt Status Register	FIFO Control Register	0xFFFF 8002
n/a	Line Control Register	0xFFFF 8003
n/a	Modem Control Register	0xFFFF 8004
Line Status Register	n/a	0xFFFF 8005
Modem Status Register	n/a	0xFFFF 8006
Scratchpad Register	Scratchpad Register	0xFFFF 8007

Accessible only when CS A/B is logical 0.

Table 4-20: UART A Baud Rate Register Set

READ MODE	WRITE MODE	ADDRESS
LSB of divisor latch	LSB of divisor latch	0xFFFF 8000
MSB of divisor latch	MSB of divisor latch	0xFFFF 8001

Accessible only when CS A/B is logical 0 and LCR bit 7 is a logical 1.

Table 4-21: UART A Enhanced Register Set

READ MODE	WRITE MODE	ADDRESS
Trigger Level Register	Trigger Level Register	0xFFFF 8000
Feature Control Register	Feature Control Register	0xFFFF 8001
Enhanced Feature Register	Enhanced Function Register	0xFFFF 8002
Enhanced Mode Select Register	Enhanced Mode Select Register	0xFFFF 8007
Xon-1	Xon-1	0xFFFF 8004
Xon-2	Xon-2	0xFFFF 8005
Xoff-1	Xoff-1	0xFFFF 8006
Xoff-2	Xoff-2	0xFFFF 8007

Accessible only when LCR is set to “BF” hex.

29230.01.UG.VC.050727/091436

4.3.2 UART B (SER2)

The following table indicate the address mapping of the UART B (SER2). For a more detailed description please refer to the EXAR XR16C2850 or XR16C2750 DUART manual.

Table 4-22: UART B General Register Set

READ MODE	WRITE MODE	ADDRESS
Receive Holding Register	Transmit Holding Register	0xFFFF 8008
n/a	Interrupt Enable Register	0xFFFF 8009
Interrupt Status Register	FIFO Control Register	0xFFFF 800A
n/a	Line Control Register	0xFFFF 800B
n/a	Modem Control Register	0xFFFF 800C
Line Status Register	n/a	0xFFFF 800D
Modem Status Register	n/a	0xFFFF 800E
Scratchpad Register	Scratchpad Register	0xFFFF 800F

Accessible only when CS A/B is logical 0.

Table 4-23: UART B Baud Rate Register Set

READ MODE	WRITE MODE	ADDRESS
LSB of divisor latch	LSB of divisor latch	0xFFFF 8008
MSB of divisor latch	MSB of divisor latch	0xFFFF 8009

Accessible only when CS A/B is logical 0 and LCR bit 7 is a logical 1.

Table 4-24: UART B Enhanced Register Set

READ MODE	WRITE MODE	ADDRESS
Trigger Level Register	Trigger Level Register	0xFFFF 8008
Feature Control Register	Feature Control Register	0xFFFF 8009
Enhanced Feature Register	Enhanced Function Register	0xFFFF 800A
Enhanced Mode Select Register	Enhanced Mode Select Register	0xFFFF 800F
Xon-1	Xon-1	0xFFFF 800C
Xon-2	Xon-2	0xFFFF 800D
Xoff-1	Xoff-1	0xFFFF 800E
Xoff-2	Xoff-2	0xFFFF 800F

Accessible only when LCR is set to “BF” hex.

29230.01.UG.VC.050727/091436

4.3.3 UART C (SER3)

The following table indicate the address mapping of the UART C (SER3). For a more detailed description please refer to the EXAR XR16C2850 or XR16C2750 DUART manual.

Table 4-25: UART C General Register Set

READ MODE	WRITE MODE	ADDRESS
Receive Holding Register	Transmit Holding Register	0xFFFF 8010
n/a	Interrupt Enable Register	0xFFFF 8011
Interrupt Status Register	FIFO Control Register	0xFFFF 8012
n/a	Line Control Register	0xFFFF 8013
n/a	Modem Control Register	0xFFFF 8014
Line Status Register	n/a	0xFFFF 8015
Modem Status Register	n/a	0xFFFF 8016
Scratchpad Register	Scratchpad Register	0xFFFF 8017

Accessible only when CS A/B is logical 0.

Table 4-26: UART C Baud Rate Register Set

READ MODE	WRITE MODE	ADDRESS
LSB of divisor latch	LSB of divisor latch	0xFFFF 8010
MSB of divisor latch	MSB of divisor latch	0xFFFF 8011

Accessible only when CS A/B is logical 0 and LCR bit 7 is a logical 1.

Table 4-27: UART C Enhanced Register Set

READ MODE	WRITE MODE	ADDRESS
Trigger Level Register	Trigger Level Register	0xFFFF 8010
Feature Control Register	Feature Control Register	0xFFFF 8011
Enhanced Feature Register	Enhanced Function Register	0xFFFF 8012
Enhanced Mode Select Register	Enhanced Mode Select Register	0xFFFF 8017
Xon-1	Xon-1	0xFFFF 8014
Xon-2	Xon-2	0xFFFF 8015
Xoff-1	Xoff-1	0xFFFF 8016
Xoff-2	Xoff-2	0xFFFF 8017

Accessible only when LCR is set to “BF” hex.

29230.01.UG.VC.050727/091437

4.3.4 UART D (SER4)

The following table indicate the address mapping of the UART D (SER4). For a more detailed description please refer to the EXAR XR16C2850 or XR16C2750 DUART manual.

Table 4-28: UART D General Register Set

READ MODE	WRITE MODE	ADDRESS
Receive Holding Register	Transmit Holding Register	0xFFFF 8018
n/a	Interrupt Enable Register	0xFFFF 8019
Interrupt Status Register	FIFO Control Register	0xFFFF 802A
n/a	Line Control Register	0xFFFF 802B
n/a	Modem Control Register	0xFFFF 802C
Line Status Register	n/a	0xFFFF 802D
Modem Status Register	n/a	0xFFFF 802E
Scratchpad Register	Scratchpad Register	0xFFFF 802F

Accessible only when CS A/B is logical 0.

Table 4-29: UART D Baud Rate Register Set

READ MODE	WRITE MODE	ADDRESS
LSB of divisor latch	LSB of divisor latch	0xFFFF 8018
MSB of divisor latch	MSB of divisor latch	0xFFFF 8019

Accessible only when CS A/B is logical 0 and LCR bit 7 is a logical 1.

Table 4-30: UART D Enhanced Register Set

READ MODE	WRITE MODE	ADDRESS
Trigger Level Register	Trigger Level Register	0xFFFF 8018
Feature Control Register	Feature Control Register	0xFFFF 8019
Enhanced Feature Register	Enhanced Feature Register	0xFFFF 802A
Enhanced Mode Select Register	Enhanced Mode Select Register	0xFFFF 802F
Xon-1	Xon-1	0xFFFF 802C
Xon-2	Xon-2	0xFFFF 802D
Xoff-1	Xoff-1	0xFFFF 802E
Xoff-2	Xoff-2	0xFFFF 802F

Accessible only when LCR is set to “BF” hex.

29230.01.UG.VC.050727/091437

4.4 Real-time Clock

Access to the real-time clock (RTC) is effected via the I2C bus. The RTC uses address 0xD0. For more detailed information please refer to the manuals for the ST - Microelectronics M41T81 and the Motorola MPC8541E (I2C bus).

Table 4-31: Register Map RTC M41T81

ADR (HEX)	ADDRESS BITS								FUNCTION RANGE IN BCD FORMAT
	D7	D6	D5	D4	D3	D2	D1	D0	
00	0.1 Seconds				0.01 Seconds				Seconds: 00 - 99
01	ST	10 Seconds			Seconds				Seconds: 00 - 59
02	0	10 Minutes			Minutes				Minutes: 00 - 59
03	CEB	CB	10 Hours		Hours				Century: 0 - 1 Hours: 00 - 23
04	0	0	0	0	0	Day			Day: 00 - 07
05	0	0	10 Date		Date				Date: 01 - 31
06	0	0	0	10M.	Month				Month: 01 - 12
07	10 Years				Year				Year: 00 - 99
08	OUT	FT	S	Calibration					Control:
09	0	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog:
0A	AFE	SQWE	ABE	Al 10M	Alarm Month				Alarm Month: 01 - 12
0B	RPT4	RPT5	Al 10 Date		Alarm Date				Alarm Date: 01 - 31
0C	RPT3	HT	Al 10 Hour		Alarm Hour				Al Hour: 00 - 23
0D	RPT2	Alarm 10 Minutes			Alarm Minutes				Al Min: 00 - 59
0E	RPT1	Alarm 10 Seconds			Alarm Seconds				Al Sec: 00 - 59
0F	WDF	AF	0	0	0	0	0	0	Flags:
10	0	0	0	0	0	0	0	0	Reserved:
11	0	0	0	0	0	0	0	0	Reserved:
12	0	0	0	0	0	0	0	0	Reserved:
13	RS3	RS2	RS1	RS0	0	0	0	0	SQW:

29230.01.UG.VC.050727/091437

Legend for Table 4-22

0 = Must set to ’0’
ABE = Alarm in battery back-up mode enable bit
AF = Alarm flag (read only)
AFE = Alarm flag enable flag
BMBn = Watchdog multiplier bit(s)
CB = Century bit
CEB = Century enable bit
FT = Frequency test bit
HT = Halt update bit
OUT = Output level
RBn = Watchdog resolution bit(s)
RPTn = Alarm repeat mode bit(s)
RSn = SQW frequency
S = Sign bit
SQWE = Square wave enable
ST = Stop bit
WDF = Watchdog flag (read only)

Note...

When the RTC has once been stopped due to low voltage, it is necessary to re-initialize the “Seconds” “Minutes” and “Hours” registers before it will run again.

4.5 IRQ Routing

The Embedded Programmable Interrupt Controller of the MPC8541E (CPU) supports 12 external IRQs. The IRQ routing is listed below. All VME interrupts are accumulated to PCI_INTA.

Table 4-32: IRQ Routing

IRQ NAME	SOURCE
IRQ0	Watchdog Timer
IRQ1	MC2 or MC3 or MC5 IRQ
IRQ2	PCI_INTA
IRQ3	PCI_INTB
IRQ4	PCI_INTC
IRQ5	PCI_INTD
IRQ6	Ser1/2
IRQ7	Ser3/4
IRQ8	SIRQ (Serial IRQs)
IRQ9	Alarm, Temperature, Fast_Eth_Phy1
IRQ10	CAN IRQ
IRQ11	CF IRQ

29230.01.UG.VC.050727/091437

4.6 CompactFlash

Write access to the CompactFlash address area is only possible using word-wide (16-bit) write commands.

Table 4-33: CompactFlash Register

REGISTER	READ/WRITE	ADDRESS
Data Register	R/W	0xFFFE 0000
Error Register	R	0xFFFE 8003
Feature Register	W	0xFFFE 8003
Sector Count Register	R/W	0xFFFE 8005
Sector Number Register	R/W	0xFFFE 8007
Cylinder Low Register	R/W	0xFFFE 8009
Cylinder High Register	R/W	0xFFFE 800B
Drive/Head Register	R/W	0xFFFE 800D
Status Register	R	0xFFFE 800F
Device Control Register	W	0xFFFE 801D
Alternate Status Register	R	0xFFFE 801D
Card Drive Address Register	R	0xFFFE 801F

4.7 EEPROM

Access to the EEPROM is effected via the I2C bus controller of the MPC8541E and not the CPM I2C channel. The EEPROM uses the I2C address 0xA0. Write protection is achieved by installing a 0 ohm resistor (R22) and removing a 0 ohm resistor (R23). Default is unprotected.

For more detailed information please refer to the manuals for the MICROCHIP 24LC64 or Catalyst 24WC64, and the MOTOROLA MPC8555 (chapter 11, I2C Interface).

4.8 Digital Temperature Sensor, LM75

Access to the onboard digital temperature sensor (DTS) is effected via the I2C bus controller of the MPC8541E. The DTS uses the I2C address 0x90.

For more detailed information please refer to the manuals for the National Semiconductor LM75 and the MOTOROLA MPC8555 (chapter 11, I2C Interface).

4.9 Ethernet PHY Addresses

The Gigabit Ethernet PHYs of the VMP3 are accessible via the MDIO interface of the MPC8541. Their addresses are 0x01 for the PHY of the TSEC1 and 0x00 for the TSEC2. The PHY of the FCC1 is accessible via the parallel port pins PD[18] (MDIO) and PD[17] (MDC) and has the PHY address 0x04.

29230.01.UG.VC.050727/091437

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29230.01.UG.VC.050727/091437

Chapter 5

NetBootLoader

29230.01.UG.VC.050727/091438

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29230.01.UG.VC.050727/091438

5. NetBootLoader

This E²Brain™ module is delivered with the NetBootLoader software already programmed into the onboard soldered Flash memory. The NetBootLoader itself is a software utility which initializes the module for operation before turning control over to either an application or to an operator. This software also provides the capability to monitor and control the operation of the NetBootLoader itself, display system status information, to program executable code and data to the Flash memory, and to load and start application software.

To attain full operational capability, the VMP3 FLASH must be programmed by the user with application software. Once the application has been programmed to Flash memory, the NetBootLoader will support the complete boot operation. The following chapters describe the functioning of the NetBootLoader and how to program the Flash memory.

Note...

The following description assumes a standard CPU board with appropriate hardware. In the event such hardware is not available, disregard the text that applies to the missing hardware and proceed as appropriate.

5.1 General Operation

Upon power on or a system reset, the NetBootLoader is started. The CPU board is configured for operation and control is either passed to an application or an operator. In the event a valid application has been programmed into the Flash memory and no operator intervention takes place, the application is copied from FLASH into SDRAM and control is passed to the application. If the NetBootLoader does not find a valid application or operator intervention has occurred, control is passed to the operator. The operator now has control to determine the system status, make configuration changes, read or program the Flash memory, or to restart or shut down the system.

The operator command interfacing with the NetBootLoader is accomplished either via the TERM serial port or the Ethernet port FCC1 (FE). During the boot operation a command interpreter is started which allows the operator to input commands to the NetBootLoader. Prior to interfacing via the Ethernet port FCC1 (FE), the port must be configured. This is done either via the TERM port or via a dhcp/bootp server.

5.2 NetBootLoader Interfaces

There are four possibilities to interface with the NetBootLoader:

- Via the MC1 (Abort) signal
- Via the TERM serial interface
- Via the SER0 serial interface
- Via the Ethernet port FCC1 (FE) interface

Gaining access to the NetBootLoader is a function of the contents of the Flash memory and the “BootWaitTime” setting. If there is not a valid application programmed into the Flash memory, the boot operation automatically terminates after the module has been initialized and control is passed to the command interpreter.

If there is a valid application in the Flash memory, the boot operation is delayed according to the setting of the boot wait time, and the MC6 (LED1) output signal is alternately asserted indicating that the boot operation is in a wait state. During this time the operator may intervene in the boot operation either by asserting the MC1 (Abort) signal, entering the “abort” command

29230.01.UG.VC.050727/091438

via the TERM interface, or by performing a successful telnet login via the Ethernet port FCC1 (FE). If the operator does not intervene, the boot operation is continued after the boot wait time has been exceeded.

5.2.1 MC1 (Abort) Signal

The MC1 (Abort) signal is routed to the VMP3 from the carrier board via the System Interface (CON1 connector) and, if made available from the carrier, provides the operator with the ability to directly terminate the boot operation during the boot wait time which is indicated by the alternately asserted MC6 (LED1) signal. This is the sole purpose of the MC1 (Abort) signal during the NetBootLoader operation.

5.2.2 TERM Serial Interface

The TERM serial port, if realized on the carrier board, is used to provide direct operator interfacing to the NetBootLoader. As soon as the CPU board has been initialized this port is activated and the operator may input commands. During the boot wait time the operator may terminate the boot operation and take control of the NetBootLoader. Once the boot wait time is exceeded the command interpreter is normally deactivated and the boot process is continued. If the NetBootLoader does not find a valid boot image, the boot process is discontinued and system control is returned to the operator via the NetBootLoader.

The TERM serial interface may either be directly connected to a terminal device or may interface with a terminal emulator.

5.2.3 SER0 Serial Interface

The SER0 serial port is used to provide the NetBootLoader with the ability to access Motorola S-Records for programming an application to FLASH. No command interpreter is available for this interface.

5.2.4 Ethernet Port FCC1 (FE) Interface

The Ethernet port FCC1 (FE) provides the capability of remotely interfacing with the NetBootLoader. Prior to using this interface it is necessary to configure the Ethernet port settings. This is accomplished via the TERM interface or a dhcp/bootp server. Once the port settings have been configured, the remote operator has the same capabilities as with the TERM interface. During the boot wait time the operator gains control of the NetBootLoader by performing a telnet login it via the Ethernet port FCC1 (FE). This causes the boot operation to be terminated and gives control to the remote operator.

In addition to the operator interface via this interface, the NetBootLoader can also use it for tftp and ftp server accessing.

29230.01.UG.VC.050727/091438

5.3 NetBootLoader Functions

In addition to initializing the CPU board for operation and the loading and starting of applications, the NetBootLoader provides the following operator monitor and control functions:

- NetBootLoader control
- system status monitoring
- network accessing
- FLASH reading and programming operations
- Motorola S-Record acquisition

These functions are described in detail in the following chapters.

NOTE ...

The command title (CMD TITLE) is expressed in capital letters and is not the same as the syntax of the command. The command syntax is always written using small letters

5.3.1 NetBootLoader Control

The NetBootLoader provides various functions for controlling the operation of the NetBootLoader itself as well as the setting of operational parameters. The following table provides an overview of available NetBootLoader control functions.

Table 5-1: NetBootLoader Control Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
ABORT	-	Terminate boot wait	
BW	Boot Wait	Set or display BootWaitTime	
CBL	Change Bootline	Set or display a bootline	Applies to a specific kernel
DHCP	-	Dynamically set Ethernet port FCC1 (FE) parameters	Requires that a dhcp or bootp server be available in the same network as the VMP3
HELP or ?	-	Display online HELP pages	
LOGOUT	-	Terminate telnet session	
NET	-	Manually set Ethernet port FCC1 (FE) parameters	Must be set before attempting to use the Ethernet port; see also the DHCP command
PASSWD	Password	Set telnet password	Must be set before attempting telnet login
PF	Port Format	Set serial port parameters	Used for the TERM and SER0 ports
RS	Reset	Resets system	
SCRIPT	-	Command scripting	Contents are executed only during boot up
SQ	Boot Sequence	Set or display boot sequence	Defines selection order of image booting

29230.01.UG.VC.050727/091438

5.3.2 System Status Monitoring

The NetBootLoader provides various functions for monitoring the overall status of the system during the operation of the NetBootLoader. The following table provides an overview of available system status monitoring functions.

Table 5-2: System Status Monitoring Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
CHECK	-	Application validation; displays information for each image	Verifies validity of user image programmed to FLASH
INFO	-	Display system information	
MD	Memory Display	Display memory contents	Applies to all visible memory
PCI	-	Display PCI device information	
PING	-	Verify network status	
VER	Version	Display version number of NetBootLoader	

5.3.3 Network Accessing

To support application development and operational requirements for various boot strategies, the NetBootLoader provides several functions for gaining access to network services. These functions include: access to dhcp/bootp servers, accessing tftp servers, and accessing ftp servers.

At initial startup of the VMP3, only the NetBootLoader is installed in onboard FLASH. To support application development or remote boot capability, the NetBootLoader can provide networking interfacing via the Ethernet port FCC1 (FE).

To achieve this, certain network parameters must first be configured. This can be done manually via a terminal or dynamically via the network. The command DHCP makes it possible to download such parameters and to configure the Ethernet port FCC1 (FE) for network operation. Once the Ethernet port is configured, the commands TFTP and FTP are available to download bootable images or other files as required.

5.3.3.1 dhcp/bootp Server Access

Use of this access method requires the availability of either a dhcp or bootp server in the same network as the VMP3. The DHCP command causes the NetBootLoader to first attempt to establish contact with a DHCP server. If contact is not achieved, it then tries to contact a BootP server. When contact is established, parameters required by the VMP3 are provided accordingly and the Ethernet port is configured and then made available for normal operation.

In the event the VMP3 is reset or cold started the configuration parameters set by the above method are lost. Only if the parameters have been set by the NET command are they still available.

Prior to using the "dhcp" command, the IP address of the VMP3 must be set to 255.255.255.255 using the "net" command.

29230.01.UG.VC.050727/091438

5.3.3.2 tftp/ftp Server Access

The NetBootLoader provides various functions for interfacing with either a tftp or ftp server.

The tftp server access is a simple method of acquiring a userimage from a remote source. Its primary use is to download a single executable userimage from a given source. For example, once an application has been programmed it would be possible to store it at a remote location where it then would be available for remote booting of an VMP3 via the Ethernet port FCC1 (FE).

The ftp server commands provide various functions consistent with interfacing with such a server.

The following table provides an overview of available tftp/ftp server functions.

Table 5-3: tftp/ftp Server Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
BYE	-	Terminate session with ftp server	
CD	Change Directory	Change ftp server directory	
GET	-	Download a file from ftp server	Only for executable applications. Data buffer is target.
LOGIN	-	Login to ftp server	
LS	List Directory	List ftp server directory	Lists contents of directory.
PUT	-	Upload a file to ftp server	Data buffer is source.
PWD	Print Working Directory	Display current ftp server directory	Lists name of directory
TFTP	-	Download a file from tftp server	

5.3.4 FLASH Operation

The NetBootLoader provides various functions for performing operations with Flash memory. The following table provides an overview of available FLASH operation functions.

Table 5-4: FLASH Operation Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
CLONE	-	Program NetBootLoader to FLASH	Uses data buffer or socket as source
LF	Load FLASH	Program application to FLASH	Uses data buffer as source
SF	Store FLASH	Reads FLASH to data buffer	Uses data buffer as target

29230.01.UG.VC.050727/091438

5.3.5 Motorola S-Records

The NetBootLoader provides one function for acquiring Motorola S-Records. The following table provides an overview of this function.

Table 5-5: Motorola S-Records Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
SL	SLoad	Download Motorola S-Records	Uses data buffer as target

5.4 Operating the NetBootLoader

5.4.1 Initial Setup

The VMP3 is delivered with the NetBootLoader already installed in the onboard soldered FLASH and is ready for operation. However, in order for the CPU board to be used in a system, application software must be made available for use. This is accomplished by programming the application also to the onboard soldered Flash memory where the NetBootLoader is located.

Upon initial power up the NetBootLoader is started automatically. As soon as the NetBootLoader has completed initialization of the CPU board, it checks to see if there is a valid application programmed in FLASH and at the same time initiates a command interpreter which the operator can access either via the TERM or the Ethernet port FCC1 (FE) interfaces. If there is not a valid application in memory, the NetBootLoader terminates the boot operation, and waits for operator intervention. As this is the case when the CPU board is first powered up, the operator now has the opportunity to program an application.

Prior to programming an application it may be necessary to configure the NetBootLoader or perform other functions depending on the user's application development environment or application requirements. Once this has be accomplished and the application has been programmed, the CPU board is ready for operation.

The following chapters provide information on how to set up and operate the NetBootLoader itself, initiation of the telnet interface, and how to program an application to FLASH.

5.4.2 Accessing the NetBootLoader

Initial access to the NetBootLoader can only be achieved via the TERM interface. Prior to using the telnet interface, the Ethernet port parameters must be set and this can only be accomplished initially via the TERM interface.

The operator must either manually set the parameters using the "net" command or dynamically via the "dhcp" command. Prior to using the "dhcp" command, the IP address of the VMP3 must be set to 255.255.255.255 using the "net" command.

Once valid Ethernet port parameters and the telnet login password have be set, the telnet interface is available for operation.

Use of the TERM interface requires either a terminal or a terminal emulator. Use of the telnet interface requires a remote telnet login to the NetBootLoader.

Availability of the command interpreter depends on the system status. If there is no valid application programmed, the command interpreter is available as long as the operator requires it. If

29230.01.UG.VC.050727/091438

a valid application is programmed, the command interpreter is only available for the duration of the boot wait time. If the operator requires the command interpreter for a longer time he must terminate the boot operation before the boot wait time is exceeded.

Upon initiation of the command interpreter, a prompt is sent to the TERM interface and commands may be entered. To gain access to the NetBootLoader from a remote location via the Ethernet port FCC1 (FE), a telnet login must be performed. If the boot wait time has not been exceeded, a telnet login automatically terminates the boot operation and a command prompt is sent to the telnet remote interface.

Once the operator has control of the NetBootLoader, he may perform any required action. To continue with the operation of the CPU board, the system must either be cold started or the operator must issue a “reset” command. In either event, the NetBootLoader is restarted and the boot operation begins anew.

5.4.3 NetBootLoader Configuration

There are several NetBootLoader commands which provide the operator with the capability to configure specific parameters which are used by the NetBootLoader for interfacing operations. These commands are:

- BW (BootWait)
- CBL (Change Bootline)
- DHCP
- NET
- PASSWD
- PF (Port Format)
- SCRIPT
- SQ (Boot Sequence)

Default settings are available for all the above commands except for "dhcp, net, and script”.

5.4.3.1 BW

This command is used to display or set the actual boot wait time used by the NetBootLoader to delay the boot operation before proceeding with the loading and starting of an application. If this time is set too short it may only be possible to gain access to the NetBootLoader via the MC1 (Abort) signal.

The BootWaitTime value is stored in the boot section of the serial EEPROM. This section is validated with a CRC code to avoid the setting of random parameters.

Note ...

If the CRC of the boot section is not valid, changing the BootWaitTime will have no effect because the “bw” command does not validate an invalid CRC. In this case, a default timing of 5 seconds is always used.

29230.01.UG.VC.050727/091438

To validate an invalid CRC, an operating system utility must be used, or, alternatively, the “-f” option of the “bw” command must be issued.

Warning !!!

Using the “bw -f” command to validate invalid entries may adversely impact the operation of the operating system.

5.4.3.2 CBL

This command is used to set or display the bootline associated with a particular kernel image or which is common to all images.

5.4.3.3 DHCP

This command is used to obtain automatically networking parameters from either a dhcp or bootp server for the Ethernet port FCC1 (FE). Its use requires the availability of one or the other of these servers to function.

5.4.3.4 NET

This command is used to set or display the parameters for the configuration of the Fast Ethernet interface of the CPU board. The Fast Ethernet interface is only available after these settings have been made. Once these settings have been made, the system must be cold started or reset for them to take effect.

5.4.3.5 PASSWD

This command is used to set the password used by the NetBootLoader for the operation of the telnet interface. No password is required for access from the TERM interface.

5.4.3.6 PF

This command is used to set the port parameters for the TERM and SER0 serial interfaces only for the current operator session. The next system restart will cause these settings to revert to the default settings of: 9600 Baud, 8 bits per character, 1 stop bit, and no parity. This is done to preclude a system lockout when restarting due to incompatible settings.

5.4.3.7 SCRIPT

This command permits the automatic invoking of NetBootLoader commands during boot up. The operator issues this command with appropriate options and then restarts the system. During the boot operation at boot wait time expiration, the "script" commands will be executed.

Use of this command permits, for example, remote booting from an tftp server.

5.4.3.8 SQ

This command is used to set or display the order in which application images are to be booted.

The NetBootLoader provides the capability to program up to four application images into the FLASH. With this command the operator can define the order in which images may be used when the system is booted. This provides operational flexibility as well as the possibility for the system to compensate for a defective image.

29230.01.UG.VC.050727/091438

For example, in the event the first image specified is defect, the NetBootLoader will attempt to load the next image specified. This is continued until either a valid image is loaded or no further image is available.

If no valid image is found, the NetBootLoader invokes its command interpreter and remains available for inputs.

5.4.4 telnet Login

A telnet login to the NetBootLoader is only possible during the boot wait time and only after the Ethernet port FCC1 (FE) parameters have been set.

To effect a telnet login the operator performs the standard telnet login procedure during the boot wait time. The NetBootLoader responds by suspending the boot wait and requests a login password. The operator then enters a password. If the password is valid, the boot wait is terminated and the operator can now access the NetBootLoader. If the password is invalid, the telnet login procedure is terminated and the boot operation continues.

In the case of an invalid password, the login procedure may be repeated as often as required within the boot wait time. Once the boot wait time is exceeded, a telnet login is no longer possible.

5.4.5 FLASH Operations

To achieve an operable system for an application, the application software may be programmed to FLASH. As mentioned before, the NetBootLoader supports the programming of up to four application images to FLASH whereby each image is assigned its own image number. In addition to this, it also supports the updating of the NetBootLoader itself as well as data transfer from the FLASH to the data buffer and from the data buffer to an ftp server. The following chapters provide information on performing the various types of FLASH operations.

5.4.5.1 FLASH Offsets

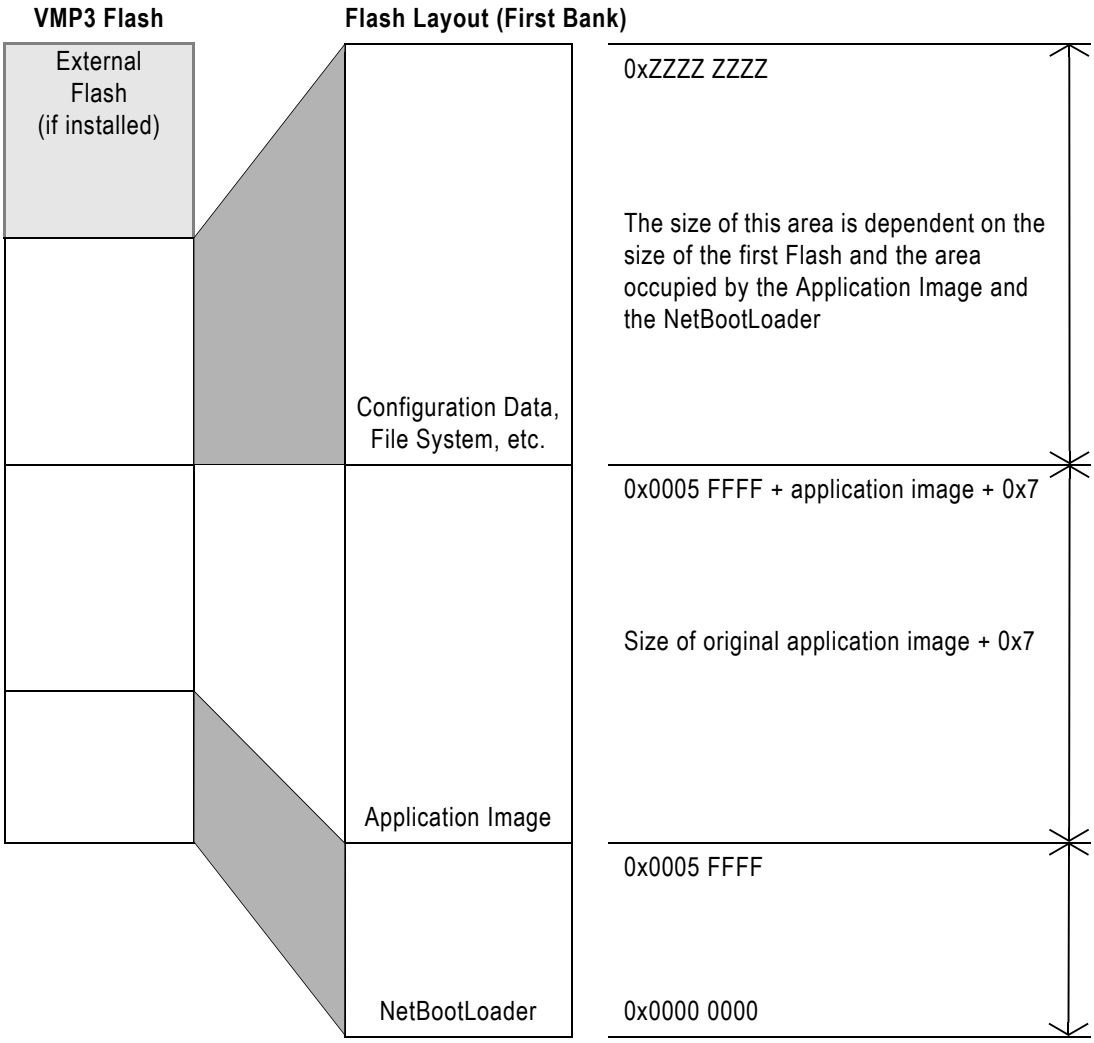
All FLASH is treated as one uniform FLASH, regardless of the physical addresses of the devices involved. All offsets are based from the beginning of the FLASH area. This means that 0x0 is the beginning of the first FLASH bank. The NetBootLoader itself is located at the beginning of the first bank of the FLASH area and for this reason this area cannot be used for application image programming. Figure 5-1 on the next page illustrates this concept. To display an overview of the current FLASH organization use the “info” command.

If the application image is an operating system (which is the default case), it must be programmed without an offset. When such an image is programmed to FLASH, the image length and CRC information is also programmed along with the image to FLASH. This information is used by the NetBootLoader to determine the validity of the image during the boot operation. During system startup, a valid image is copied to SDRAM address 0x0 and started at offset 0x100 after the boot wait time is exceeded.

If an offset is specified, the image will be programmed exactly at this offset without adding length or CRC information. This option is intended for the storing of configuration information which is required to be located in FLASH.

29230.01.UG.VC.050727/091438

Figure 5-1: Flash Addressing Scheme - VMP3



To understand the above concept assume for example that the onboard soldered Flash is an 16 MB device, and the application image is 4 MB.

Then:

4 MB application size	=	0x0040 0000
application size + 0x7	=	0x0040 0007
0x0005 FFFF + application size + 0x7	=	0x0046 0006
0xZZZZ ZZZZ	=	0x00FF FFFF

Addressing of off-board Flash would begin with 0x0100 0000.

5.4.5.2 Programming an Application

The application image itself must be compiled and linked to run from the SDRAM base address 0x0 of the CPU. The image must contain executable PPC code at offset 0x100 which is the usual case with ROM/Flash images.

Gaining access to the image for programming to FLASH depends on where it is located. The NetBootLoader can access four different sources for images:

- tftp server
- ftp server
- Motorola S-Records
- memory within the visible address range of the CPU board

The NetBootLoader uses a single data buffer for downloading an image from a tftp server, ftp server, or an image as Motorola S-Records. These images must first be downloaded to the data buffer prior to being programmed to FLASH. An image located within the visible address range of the CPU board is directly accessible for programming.

To access an image located on an tftp server, the “tftp” command is used. To access an image located on an ftp server, the “get” command is used. To perform Motorola S-Record acquisition, the “sl” (SLoad) command is used. Once the image is in the data buffer, the FLASH is programmed using the “lf” (Load Flash) command. For an image within visible memory, the “lf” (LoadFlash) command is used to program directly to FLASH.

5.4.5.3 Accessing tftp and ftp Servers

To gain access to an application image file stored on a tftp or ftp server the Ethernet port FCC1 (FE) is used. Images are downloaded to the data buffer using the ftp protocol. To use this interface the Ethernet port parameters must first be set and the operator must have control of the NetBootLoader.

To download an application image from a tftp server, the command "tftp" is used. The tftp server IP and file name of the application must be known and provided to the "tftp" command or be provided by the dhcp server via the "dhcp" command.

To perform a download from an ftp server, the operator must first login to the ftp server. After a successful login, the operator then locates the image file required and downloads it to the data buffer. As with any type of server session, the operator should logout when the session is finished.

Note ...

The commands "tftp", “get”, and “ls” use the same data buffer. Therefore if an “ls” command is issued after a "tftp" or “get” command the data buffer will be overwritten. If an “lf” command follows the “ls” the NetBootLoader refuses to program the overwritten data buffer to the FLASH.

5.4.5.4 Motorola S-Records

The NetBootLoader will also accept Motorola S-Records as an application image. The “sl”’ command accepts S1, S2 and S3 records. Operation is terminated by the appropriate S9, S8 or S7 record. Other types of records are ignored.

29230.01.UG.VC.050727/091439

The checksum of every record except end records is checked. Bad records are rejected by the NetBootLoader. The address range of every record is also checked. Records which fall outside of the internal buffer are rejected.

The records must be 0-based. This means that it's address must correspond to the address where they will be loaded in the data buffer relative to its start. If necessary, the base address can be modified with the -o option of the "sl" command.

Note ...

If the data buffer is programmed to FLASH without the -o option (program a startable image) the downloaded image is copied to RAM during startup and is executed there. For this reason application images which require to be programmed must start at the address 0x0.

The image must start at the absolute address 0x0 and must contain executable PPC code at the absolute address 0x100. If S1 or S2 record input is preferred, please note that these records only include 16 and 24-bit wide addresses. If no switch to another record type is included it must be ensured that the code is not larger than the address range covered.

Note ...

Neither the "sl" nor "lf" command can be used to program Motorola S-Records to RAM areas.

For accessing the Motorola S-Records, both the TERM and SER0 interfaces can be used. The MC6 (LED1) signal is asserted alternately at a low rate while downloading indicating that the transfer is in progress. The transfer itself may take several minutes to complete.

Ensure that the XON/XOFF protocol is used on the host side. This is a fixed setting and cannot be changed. Additionally, ensure that the host does not stop transmission after a number of lines (e.g. OS-9: use the 'nopause' attribute).

The TERM and SER0 serial interface parameters can be modified with the "pf" command.

5.4.6 Updating the NetBootLoader

In addition to programming an application to FLASH, the NetBootLoader itself can be updated. The new version of the image must be made available via an ftp server.

5.4.7 Updating With an Image Loaded Via an ftp Server

The image is downloaded in the same way as an application image (refer to chapter 5.4.5.3). The new version of NetBootLoader image is then programmed using the "clone -n" command.

5.4.8 Uploading a FLASH Area

The NetBootLoader also has the possibility to upload certain areas of the FLASH to a host using the Ethernet port FCC1 (FE). To use this interface this Ethernet port parameters must first be set and then the operator must gain control of the NetBootLoader and perform an ftp server login. After a successful login, the operator then stores the FLASH area to be uploaded to the local data buffer using the "sf" command. Using the "put" command transfers the contents of the data buffer to the ftp server. As with any type of server session, the operator should logout when the session is finished.

29230.01.UG.VC.050727/091439

5.5 Plug and Play

On the CPU board the NetBootLoader includes “Plug and Play” functionality. This ensures that the board is completely initialized and that all resources necessary for PCI devices (addresses, interrupts etc.) are assigned automatically. This important feature has the advantage that conflicts do not arise when PCI devices are added or removed. Furthermore, the operating system itself does not include the board initialization code.

5.6 Porting an Operating System to the CPU Board

The image for the absolute address 0x0 should be linked with an entry point at the absolute address 0x100.

One should not attempt to reassign the PCI BAR registers. The assigned values should be read back and these should always be used in the drivers.

The “interrupt line” field in the PCI configuration header is initialized with the IRQ line number to which the INTA of the device is routed.

Downloaded images are never executed from the FLASH. The programmed image is always downloaded to SDRAM, the absolute address 0x0 being downloaded first. There is no configuration option available to amend this process. If it is necessary to relocate the image to another address after download, simply add a small assembly routine at the beginning of the code which will move the image to the correct address.

29230.01.UG.VC.050727/091439

5.7 Commands

The following commands are available with the NetBootLoader. Where an ellipsis (…) appears in the command syntax it means that the command is continued from the previous line. Observe any spaces that may be between the ellipsis and the remainder of the command.

ABORT

FUNCTION:	Terminate the NetBootLoader boot operation
SYNTAX:	**abort**
DESCRIPTION:	This command is used by the operator to terminate the boot operation during the boot wait time to allow the operator to perform other NetBootLoader operations. To be asserted it must be issued during the boot wait time which is indicated by the alternating assertion of the MC6 (LED1) signal.

BW

FUNCTION:	Set or display the parameters of the boot wait function of the NetBootLoader
SYNTAX:	**bw [<time>| -f]** where: bw command <time> parameter: value: seconds 0, 1, 2, 5, 10, 20, 50 -f option: force CRC update

29230.01.UG.VC.050727/091439

BW

DESCRIPTION:	The command “bw” displays the parameter “<time>” setting. The parameter “<time>” stipulates the waiting time in seconds that the boot operation is delayed before the application is loaded and started. No values other than these are supported. Bear in mind when setting the boot wait time that the MC6 (LED1) signal is asserted alternately at the rate of two times a second. Therefore, if the boot wait is set to 1 second the MC6 signal will only be alternately asserted two times. The option “-f” is used to force updating of the CRC value of boot section of the EEPROM. For further information refer to chapter 5.4.3.1.
USAGE:	Display setting of “<time>” parameter COMMAND / RESPONSE: **bw** **WaitTime: 20**
	Set boot wait time to 50 seconds COMMAND / RESPONSE (none): **bw 50**
	Set boot wait time to 0 seconds COMMAND / RESPONSE (none): **bw 0** **Choosing a waittime of 0s will make a network login impossible**

BYE

FUNCTION:	Terminate an ftp server session
SYNTAX:	**bye**
DESCRIPTION:	An ftp server session which has been established with the command “login” is terminated with the command “bye”.

CBL

FUNCTION:	Set or display the parameters of the bootline function
SYNTAX:	**cbl <num> [<bootline>]** where: cbl — command <num> — parameter: value: string “0, 1, 2, 3, c” ID number of the image to be associated with the bootline or bootline which is common to all images <bootline> — parameter: value: string (max. of 256 characters) defines the bootline to be used with the kernel indicated by <num> or the common bootline
DESCRIPTION:	When an application image is programmed to FLASH, it is assigned an ID number (0, 1, 2, or 3). This number is used to identify which image is to be addressed by the command “cbl”. In addition, a bootline common to all images may also be defined using the “c” parameter. If the command “cbl” is invoked with only the <num> parameter, it returns the bootline for the image specified or the common bootline. Invoking the command “cbl” with the <bootline> parameter overwrites any previous bootline for the image specified.
USAGE:	Display the bootline for image 2 COMMAND / RESPONSE: **cbl 2** <contents of the bootline of image 2>

CD

FUNCTION:	Change the current ftp server directory
SYNTAX:	**cd <new-path>** where: cd command <new-path> parameter: string new directory path
DESCRIPTION:	If an ftp server session has been established with the “login” command, the command “cd” is used to change the current ftp server directory. The argument “<new-path>” may be an absolute or relative path. The format depends on what the server accepts. For example, UNIX hosts require that the directory names must be entered exactly in the same case.

CHECK

FUNCTION:	Verify validity of application programmed to FLASH
SYNTAX:	**check**
DESCRIPTION:	When an application is programmed to FLASH, a CRC is performed and the results are stored in FLASH along with the application. The “check” command provides status information for the current application images in FLASH.
USAGE:	Verify valid application is stored in FLASH COMMAND / RESPONSE: **check** **Checking Image: 0** **check image crc: ok** **length in flash: 0x0053d004** **sectors used : 84**

CHECK

USAGE:

```
Checking Image: 1
  check image crc: ok
  length in flash: 0x0001029c
  sectors used   :     2

Checking Image: 2
  check image crc: fail
  length in flash: -
  sectors used   : -

Checking Image: 3
  check image crc: fail
  length in flash: -
  sectors used   : -
```

CLONE

FUNCTION: Program the NetBootLoader to FLASH

SYNTAX:

clone [-n]

where:

clone	command
-n	option: program from data buffer

DESCRIPTION:

To update the NetBootLoader itself, the command “clone” is used.

The application image source for programming is the data buffer. The image must first be downloaded to the data buffer from an ftp server.

To program from the data buffer, the command “clone -n” is used.

The new image is checked for validity. If an image is invalid, the update is aborted. Additionally, the operation must be confirmed by typing the word “yes”. Any other or no input will cancel the operation.

29230.01.UG.VC.050727/091439

CLONE

USAGE:

Program NetBootLoader (normal operation)

COMMAND / RESPONSE:

```
NetBtLd> clone -n
clone: Fixup FLASH info from ftp buffer
This will overwrite the current ...
NetBootLoader, are you sure? [no] yes
clone: System transferred; Start again, ...
assure that Bootjumper is removed.
NetBtLd>
```

Note: When responding to the overwrite query, “yes” must be spelled out. Any other response will terminate the cloning operation.

Program NetBootLoader (image not valid)

COMMAND / RESPONSE:

```
NetBtLd> clone -n
clone: Fixup FLASH info from ftp buffer
Image length invalid, image is damaged,
abort.
NetBtLd>
```

DHCP

FUNCTION:	Interface to a dhcp or bootp server; exchange network configuration parameters
SYNTAX:	**dhcp [<timeout>]** where: dhcp command <timeout> paramenter: value: numerical string set timeout, in seconds
DESCRIPTION:	This command is used to set the network parameters for operation of the Ethernet port FCC1 (FE) via either a dhcp or bootp server. Initially the CPU board does not have a valid Ethernet interface configuration, and, therefore, this interface is inoperable. The initial configuration must be done either manually from the TERM interface using the command "net", or, if a dhcp or bootp server is available, it can be done automatically by the "dhcp" command. Manually configured parameters are permanently stored. Parameters configured using the "dhcp" command are temporary and will be lost if the system is reset or cold started. Prior to using the "dhcp" command, the IP address must be set to 255.255.255.255 with the "net" command.
USAGE:	Program NetBootLoader (normal operation) COMMAND / RESPONSE: **NetBtLd> dhcp** **Sending request... reply from BOOTP/DHCP server.** **Network eth0 initializated ok.** **Server address is 192.168.112.2, our IP address is 192.168.112.14.** **Filename :** **NetBtLd>**

GET

FUNCTION:	Download file from ftp server
SYNTAX:	**`get <filename>`** where: get command <filename> parameter: string name of image file to be downloaded, or path and name of image file to be downloaded
DESCRIPTION:	To download a file from the ftp server to the local data buffer, the command “get” is used. A successful ftp server login must be carried out before a file can be downloaded and the file must be in binary format. The argument “<filename>” must refer to an existing and accessible file on the server and the syntax must follow the requirements on the server, e.g. case sensitiveness. The argument may also include a path specification, if the server supports this.

HELP or ?

FUNCTION:	Display online help pages
SYNTAX:	**`help`** **`?`**
DESCRIPTION:	This command displays the online help pages. The display of the help text varies between the different CPU’s reflecting their differences. The syntax of every command and a brief description is shown. The display output pauses after every page. The output can be continued with any key. Entering a “.” (period) aborts the help function.

29230.01.UG.VC.050727/091439

INFO

FUNCTION:	Display system information
SYNTAX:	**info**
DESCRIPTION:	The command “info” is used to display an information summary for the running system. Displayed are the following: CPU type, the board type, the size of the installed RAM and FLASH, and the FLASH areas occupied by the NetBootLoader and the operating system images. This information is displayed in hexadecimal offsets. Images programmed using the “-o” option of the command “lf” are not shown.
USAGE:	Display system information COMMAND / RESPONSE: **info** **CPU : Motorola MPC8541** **Board : EB8541** **Ram : 4000000** **Flash :** **Name : AMD 29LV640** **Bank : 0** **Bytelane : 0** **BankPortsize : 16** **ChipPortsize : 16** **Offset : 0x0** **Size : 0x800000** **NetBootLoader used FLASH: 0x0 - 0x60000** **Sector usage map:** **0x0000: nnnnnn00 00000000** **0x0010: 00000000 00000000** **0x0020: 00000000 00000000** **0x0030: 00000000 00000000** **0x0040: 00000000 00000000** **0x0050: 00000000 0011....** **0x0060: ....** **0x0070: ....** Where: n = NetBootLoader; 0 = image 0; 1 = image 1; . = usage unknown

LF

FUNCTION:	Load Flash
SYNTAX:	**lf [<num>][-o[=]<offset> [-k]]** **… [-m[=]<adr> -l[=]<len>]** where: lf command <num> parameter: value: numeric “0, 1, 2, 3” ID number assigned to this image -o option: offset <offset> parameter: value: hexadecimal program to FLASH offset of ... -k option: keep retain surrounding contents -m option: memory (address) <adr> parameter: value: hexadecimal absolute address of image to be programmed -l option: length <len> parameter: value: hexadecimal length of image to be programmed
DESCRIPTION:	If <num> is not specified, 0 is assumed. Without options, the FLASH is programmed using the contents of the data buffer. If no image is available in the data buffer, the FLASH programming is terminated. If no offset option (“-o”) is specified the image is added along with the CRC and length information. If the CRC is determined to be valid during the next startup, the image is copied to the absolute address 0x0 and started at 0x100 after the boot wait time has been exceeded. Normally, the local data buffer holds the image to be programmed. However, if the “-m” and “-l” options are specified, the image is programmed from the absolute address specified. If the “-o” option is specified, the contents are programmed exactly at this offset in FLASH. No length and no CRC information is added. The “-k” option can be specified to prevent deletion of the surrounding FLASH contents.

29230.01.UG.VC.050727/091439

LF

DESCRIPTION:	FLASH memory can only be erased sector-wise. If an image is programmed to a certain offset with the “-o” option, at least this sector (and maybe one or more of the following sectors depending on the size of the image) will be erased. The “-k” option can be used to retain the surrounding data, however, this slows down the operation significantly. To achieve fast programming of parameter images without destroying other FLASH contents, the data should be placed at a sector boundary and the sector(s) must not contain any other data or executable images. If organized this way, use of the “-k” option can be avoided. Note: The “lf” command cannot be used to program the NetBootLoader.
USAGE:	Program FLASH from data buffer and add CRC and image length (Image ID = 0 is assumed) COMMAND / RESPONSE (none): **`lf`**
	Program FLASH from visible address at 0x87000000 for length of 0x123456 COMMAND / RESPONSE (none): **`lf -m=87000000 -l=123456`**
	Program FLASH from data buffer to offset 0xF4240 and retain adjacent FLASH contents COMMAND / RESPONSE (none): **`lf -o=f4240 -k`**

29230.01.UG.VC.050727/091440

LOGIN

FUNCTION:	Initiate ftp server session
SYNTAX:	**login <ip-of-host> <username> [<password>]** where: login command <ip-of-host> parameter: value: numerical string IP address of host: nnn.nnn.nnn.nnn <username> parameter: value: string ftp server “username” <password> parameter: value: string user’s password
DESCRIPTION:	The command “login” is used to establish an ftp server session. The “<ip-of-host>” must be specified as four numbers separated by single dots. The “<password>” parameter is not necessary if the server does not request one.
USAGE:	Initiate ftp server session COMMAND / RESPONSE: **login 192.168.47.12 johndoe mypassword** (Response is dependent on the server accessed)

LOGOUT

FUNCTION:	Terminate telnet session with NetBootLoader
SYNTAX:	**logout**
DESCRIPTION:	A remote telnet session will be terminated with the command “logout”. No application is loaded and started if the session is terminated with “logout”. The NetBootLoader waits for a new session to be initiated or for a command entry from the serial console.

29230.01.UG.VC.050727/091440

LS

FUNCTION:	Display listing of the current ftp server directory
SYNTAX:	**ls**
DESCRIPTION:	To display a listing of the current ftp server directory the command “ls” is used. This command downloads the listing to the data buffer and then the listing is displayed. Any previously loaded image in the data buffer is overwritten. If an attempt is then made to program the FLASH after the “ls” command has been issued it will fail.

MD

FUNCTION:	Display visible memory
SYNTAX:	**md [<adr>]** where: md command <adr> parameter: value: hexadecimal starting address of a visible memory area
DESCRIPTION:	To display a visible memory area the command “md” is used. The first time the command “md” is issued, visible memory contents starting at the address 0x0 are displayed if no “<adr>” parameter is used. If issued again without the “<adr>” parameter, the display starts with the end address of the previous display. Data is displayed as hexadecimal 32-bit words and as ASCII dump.

NET

FUNCTION:	Set or display the parameters for the Fast Ethernet interface
SYNTAX:	**net [<ip-addr>][-netmask <netmask>]** **…[-gw <gateway>][-f]** where: net — command <ip-addr> — parameter: value: numerical string IP address of CPU board: nnn.nnn.nnn.nnn -netmask — option: netmask <netmask> — parameter: value: numerical string netmask of CPU board: nnn.nnn.nnn.nnn -gw — option: gateway <gateway> — parameter: value: numerical string gateway address for network: nnn.nnn.nnn.nnn -f — option: force CRC update
DESCRIPTION:	To set or display the parameters of the Fast Ethernet interface the command “net” is used. Initially the CPU board does not have a valid Fast Ethernet interface configuration, and, therefore, this interface is inoperable. The initial configuration must be done from the TERM interface using the command “net ... -f”. Using the “-f” option forces a CRC to be performed and stored along with the other configuration parameters in the serial EEPROM. Once the initialization of the Fast Ethernet interface is done, the CPU board must be restarted for the parameters to take effect. Later changes to the parameters do not require the use of the “-f” option to force a CRC. This is done automatically. Only in the event that the Fast Ethernet interface does not properly initialize, may it be necessary to re-enter the parameters using the “-f” option. The <ip-addr> parameter must be set to 255.255.255.255 if the "dhcp" command is to be used for the configuration of the Ethernet port.

29230.01.UG.VC.050727/091440

PASSWD

FUNCTION:	Set the telnet password
SYNTAX:	**passwd [-f | -d]** where: passwd command -f option: if password is not known -d option: disable disable telnet login (remote access)
DESCRIPTION:	To set the password for telnet sessions with the NetBootLoader the command “passwd” is used. This command is interactive, meaning that after it is issued, the NetBootLoader responds with an appropriate request to the operator which must be properly acknowledged or the operation fails (refer to USAGE below). To set the password in the event it is unknown, use the option “-f”. This is can only be accomplished from the TERM interface and not from the Fast Ethernet interface. With the option “-d”, the remote telnet login can be disabled by invalidating the password.
USAGE:	Set password COMMAND / RESPONSE: **NetBtLd> passwd** **Old Password: ***** New Password: ***** Type again : ***** NetBtLd>** (The old password must be known)
	Set password when the old password is not known COMMAND / RESPONSE: **NetBtLd> passwd -f New Password: ***** Type again : ***** NetBtLd>**

PCI

FUNCTION:	Display PCI information
SYNTAX:	**pci**
DESCRIPTION:	The command “pci” is used to display detailed information on all detected PCI devices. The bus number, device number, function number, vendor, and device ID’s are displayed together with the configured base addresses and the assigned IRQ number.

PF

FUNCTION:	Set or display the serial port parameters (format)
SYNTAX:	**pf [<port> [<baud>][/[<bitschar>]** **…[/[<parity>][/<stops>]]]]**

where:

pf	command
<port>	parameter: string: “term” or “ser0” defines serial port to be configured where: term = SP4 and ser0 = SP6
<baud>	parameter: value: numeric: “300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19200, 38400, 115200” defines the baud rate for the port
<bitschar>	parameter: value: numeric: “7” or “8” defines the number of bits per character
<parity>	parameter: string: “n” (none), “o” (odd), “e” (even) defines parity to be used
<stops>	parameter: value: number: “1”, “2” defines number of stop bits

29230.01.UG.VC.050727/091440

PF

DESCRIPTION:	To set or display the operational parameters for the available serial interfaces the command “pf” is used. At startup the settings for the SP4 and the SP6 interfaces are always set to the default values (38400/8/n/1). This is to avoid a possible system lockout. If other settings are required during operation of the NetBootLoader they may be made. If changes are made, it must be ensured that corresponding parameters are used for the operator consle. Issuing this command without parameters being specified will display the current serial port settings. Syntax-wise, no spaces are permitted between the parameters and they must be separated with a slash. Not all parameters must be specified, but the “/” characters must be present to distinguish the different parameters from each other. The sequence can be aborted after every option.
USAGE:	Set SP4 to 300 Baud, 7 Bits/char, odd parity, and 2 stop bits COMMAND / RESPONSE (none): **`pf term 300/7/o/2`**
	Set the bits per character parameter of SP6 to 7 COMMAND / RESPONSE (none): **`pf ser0 //7`**
	Set the stop bits parameter of SP6 to 2 COMMAND / RESPONSE (none): **`pf ser0 ///2`**

29230.01.UG.VC.050727/091440

PING

FUNCTION:	Verify operability of the Fast Ethernet interface
SYNTAX:	**ping <ip_addr> [-c <count>] [-s <size>]** **… [-w <wait>]** where: ping command <ip-addr> parameter: value: numerical string IP address of target: nnn.nnn.nnn.nnn -c option: count <count> parameter: value: numeric: “[n ...]n” number of packets to send -s option: size <size> parameter: value: numeric: “[n ...]n”: bytes size of packet to send -w option: wait <wait> parameter: value: numeric: “[n ...]n”: seconds wait time between packets
DESCRIPTION:	To verify the operational status of the Fast Ethernet interface the command “ping” is used. This command tests the network connection and target server’s ability to respond. If no other parameters are specified, four requests will be sent. This can be changed with the parameter “-c”. The typical size of a ping packet can be changed with the parameter “-s” and the time between requests, which is typically one second, can be changed with the parameter “-w”. Reponses to the “ping” command are dependent on the performance of the network.
USAGE:	Send four packets COMMAND / RESPONSE: **ping 192.192.158.7**
	Send ten packets, 100 bytes long, and wait two seconds between packets COMMAND / RESPONSE: **ping 192.192.158.7 -c 10 -s 100 -w 2**

29230.01.UG.VC.050727/091440

PUT

FUNCTION:	Upload contents of the data buffer to the ftp server.
SYNTAX:	**put <filename>** where: put command <filename> parameter: string file name to be used for contents of data buffer to be uploaded
DESCRIPTION:	To upload the contents of the data buffer to a file on an ftp server, the command “put” is used. The file indicated by the parameter “<filename>” is created on the server. In the event that a file with this name already exists, its contents will be overwritten.

PWD

FUNCTION:	Display the current ftp server directory.
SYNTAX:	**pwd**
DESCRIPTION:	If a ftp connection has been established with the “login” command, the command “pwd” is used to display the complete path of the current directory on the ftp server.

RS

FUNCTION:	Reset the system
SYNTAX:	**rs**
DESCRIPTION:	To permit the operator to force a restart of the system, the command “rs” is used. This command terminates the NetBootLoader command interpreter and resets the entire system, generating a system reset with the onboard watchdog. If this command is issued over a remote telnet connection, the telnet session is terminated prior to the generation of the reset.

29230.01.UG.VC.050727/091440

SCRIPT

FUNCTION:	Provides very basic scripting capability
SYNTAX:	**`script [<newscript>]`** where: script — command <newscript> — parameter: string string may only include simple commands; flow control constructs are not permitted; commands must be separated by semi-colons
DESCRIPTION:	With the "script" command, it is possible to control the boot process. During booting, if a valid script is available, the NetBootLoader will process it once the boot wait time is expired. If this command is issued without any parameters, the currently active script contents are displayed.
USAGE:	Download a boot image from a tftp server and run the boot image. COMMAND / RESPONSE (none): **`script dhcp; tftp; run`** Upon the next reset or cold start, after the boot wait time has expired the commands "dhcp", "tftp", and "run" will be executed in that order. This command sequence configures the Ethernet port FCC1 (FE), downloads the specified bootable image from an tftp server, and then starts this image.

29230.01.UG.VC.050727/091440

SF

FUNCTION:	Store FLASH contents to data buffer
SYNTAX:	**sf -o[=]<offset> -l[=]<length>** where: sf — command -o — option: offset <offset> — parameter: value: hexadecimal relative offset to start of FLASH contents to be stored to the data buffer -l — option: length <length> — parameter: value: hexadecimal length of FLASH contents to be stored to the data buffer
DESCRIPTION:	With the command “sf” a selected portion of the FLASH contents may be copied to the local data buffer, e.g. for a subsequent upload to the ftp server with the “put” command. The “<offset>” parameter refers to the relative offset within the FLASH area similar to the “lf” command. The parameter “<length>” specifies the length to store.
USAGE:	Store 64 kB of FLASH contents to the data buffer beginning at an offset of 1 MB COMMAND / RESPONSE (none): **sf -o=100000 -l=10000**

SL

FUNCTION:	Download Motorola S-Records to data buffer
SYNTAX:	**sl [-o[=]<offset>] [-u]** where: sl command -o option: offset <offset> parameter: value: hexadecimal: unsigned offset to be subtracted from each record's address -u option: source = SER0 instead of TERM
DESCRIPTION:	With the command “sl” Motorola S-Records are downloaded to the data buffer and the record addresses modified accordingly as required for SDRAM operation (for copying to 0x0). The “<offset>” parameter may be used to change the record base to 0x0. The “-u” option selects the SER0 interface as source for the S-Records otherwise the TERM interface is used..
USAGE:	Download S-Records to data buffer and reduce each record’s address by 0x10000. COMMAND / RESPONSE (none): **sl -o=10000**

SQ

FUNCTION:	Set or display the boot sequence
SYNTAX:	**sq [<num1> <num2> <num3> <num4>]** where: sq command <num1> parameter: value: numeric: “0, 1, 2, 3” ID number of image to be booted <num2> parameter: value: numeric: “0, 1, 2, 3” ID number of image to be booted <num3> parameter: value: numeric: “0, 1, 2, 3” ID number of image to be booted <num4> parameter: value: numeric: “0, 1, 2, 3” ID number of image to be booted
DESCRIPTION:	Up to four bootable images may be programmed into the boot FLASH. The boot sequence defines to the NetBootLoader the order in which images are to be accessed when booting. The NetBootLoader starts with num1 and continues until a valid image is found. In the case no valid image is found, the NetBootLoader stops searching and waits for operator intervention. All four number parameters must be defined even if there is not an image in the FLASH with that ID number. Any given ID number may only be used once: e.g. a sequence of 0120 is not permitted. The default sequence is 0123 if the boot sequence has not been programmed.
USAGE:	Display the current boot sequence setting. COMMAND / RESPONSE: **sq <cr>** **0312**
	Set the boot sequence to 3201. COMMAND / RESPONSE(none): **sq 3201**

29230.01.UG.VC.050727/091440

TFTP

FUNCTION:	Download file from a tftp server
SYNTAX:	**`tftp [<serverip>] [<filename>]`** where: tftp — command <serverip> — parameter: value: numerical string IP address of the tftp server <filename> — parameter: value: string name of image file to be downloaded, or path and name of image file to be downloaded
DESCRIPTION:	The "tftp" command makes it possible to download a file from a tftp server via the Ethernet channel FCC1 (FE). If used with the "dhcp" command, it is possible to use the IP address and file information returned by the "dhcp" command. If this command is issued without any parameters, it will use the previously stored information returned with the "dhcp" command.
USAGE:	Download a file from a tftp server. COMMAND / RESPONSE (none): **`tftp 195.178.125.55 image2`** This command downloads the file "image2" from the specified tftp server.

VER

FUNCTION:	Display version number
SYNTAX:	**`ver`**
DESCRIPTION:	The command “ver” displays the actual version number of the NetBootLoader.

29230.01.UG.VC.050727/091440

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29230.01.UG.VC.050727/091440

Chapter 6

System Considerations

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30504.01.VC.050727/091441

6. System Considerations

Successful implementation of the VMP3 CPU board in any given application is a function of a wide variety of factors. To assist system integrators in achieving optimum solutions, additional technical information concerning:

- Thermal design
- Power requirements

is provided by this section.

6.1 Thermal Design Considerations

The VMP3 is designed to be operated in a wide range of thermal environments. Basic thermal management mechanisms have been incorporated, and, depending on the application requirements, there are configurations available which should satisfy most situations. Still it is necessary for system integrators to be aware of certain concepts and capabilities of the VMP3 when projecting overall system thermal management. The following provides more detailed information concerning aspects that must be considered before the VMP3 is integrated in an application system.

6.1.1 Thermodynamics Terminology

In order to facilitate understanding the factors involved in the thermal considerations being discussed here, the following definitions provided.

Table 6-1: Thermodynamics Terminology as Relating to the VMP3

TERM	DEFINITION
Heat	The thermal energy of a body. The primary source of heat in VMP3 is the CPU which requires cooling.
Cooling	Reduction of the temperature of a body. The transfer of heat from a body. Cooling is a somewhat relative term when applied to systems which generate heat due to the continuous application of external energy. In the case of the VMP3 continuous operation without “cooling” would lead to the ultimate destruction of the CPU and other components. With cooling, however, board components are allowed to operate within a range of higher temperatures than would otherwise be possible. Cooling in this case means maintaining a working temperature that does not exceed the maximum level.
Conduction	The cooling of a body by means of direct contact with another body whose temperature is lower. The VMP3 uses conduction to transfer heat from the CPU to a heat sink. The heat sink is the primary thermal interface to the VMP3 and is an integrated part of the VMP3. Secondary cooling of the VMP3 may be achieved either by conduction or convection.

30504.01.VC.050727/091441

Table 6-1: Thermodynamics Terminology as Relating to the VMP3

TERM	DEFINITION
Convection (Free and Forced)	The cooling of a body by means of the use of a fluid (liquid or gas) whose temperature is lower. Convectional cooling always requires that some fluid is moved over a body and that the fluid temperature is lower than that of the body to be cooled. Free convection relies on the buoyancy of the fluid caused by the transfer of heat from the body to be cooled to the fluid. This results in a very minimal amount of fluid flow which, depending on the temperature of the fluid and the amount of fluid available, may be sufficient to cool the body. In the case of the VMP3, the fluid would be ambient air. Forced convection relies on the forceful movement of a fluid across a body caused by the application of external energy. Again in the case of the VMP3, the fluid would be ambient air which is forced over the heat sink of the VMP3.
Radiation	The transfer of heat from a body by means of thermal radiation. The VMP3 is not designed for radiation cooling.
Ambient Air	The air occupying the immediate space surrounding a body to be cooled. For cooling to take place using ambient air, the ambient air must pass over the body to be cooled and the ambient air temperature must be lower than that of the body to be cooled.
Ambient Air Temperature	The temperature of the ambient air surrounding the body to be cooled. When applied to convectional cooling, it is the temperature of the ambient air directly prior to its flowing over the body to be cooled.
Air Flow	Movement of ambient air across a body to be cooled. The flow of ambient air is critical to convectional thermal management in particular if the ambient air is recycled (reflowed over the body to be cooled). Continuous recycling without cooling of the ambient air will quickly lead to overheating. In addition, the cooling effect of air flow in itself is limited. It requires a minimum velocity in order to have any cooling effect at all, and above a given velocity no further increase in real cooling effect is achieved.
Heat Spreader	A mechanism to achieve a rapid transfer of heat away from one body to another.
Heat Sink	A mechanism to achieve a (rapid) transfer of heat away from a body and to act as a transport medium to another body or fluid.
Heat Pipe	A special form of heat spreader which employes both conduction and convection in a discrete body to achieve a rapid transfer of heat from one body to another or to a fluid.

6.1.2 System Environment

The VMP3 system environment plays the major role in determining the thermal management concept to be applied to the VMP3. Generally speaking, there are two basic types of system environments: open and closed.

Open environments use ambient air convectional cooling as their main instrument of system thermal management. Closed environments rely heavily on conductional cooling as their first line of system thermal management. Closed systems may also be of a hybrid nature where convectional cooling is used on top of conductional cooling. The initial means of cooling the VMP3 is convectional.

30504.01.VC.050727/091441

From the above it can be readily seen that the VMP3 supports both open and closed system environments. The key point of issue regardless of the type of environment, however, is the requirement of the VMP3 for additional cooling. In particular, if convectional cooling is planned it is imperative that a minimum air flow be ensured. The minimum air flow requirement is dependent on the configuration employed and the temperature of the ambient air.

6.2 Heat Sinks

The VMP3 and its available versions are fitted with optimally designed heat sinks. The physical size, shape, and construction ensures the best possible thermal resistance (R_{th}) coefficients. In addition, it is specifically designed to efficiently support forced air flow concepts as found also in modern VNE system chassis.

Even though the VMP3 is fitted with an optimally designed heat sink, the thermal energy dissipated by the high performance CPU exceeds the thermal capabilities of the heat sink for some applications. In these cases, the VMP3 must operated with forced airflow cooling. For further assistance regarding cooling requirements, please contact Kontron's technical support.

6.3 Power Considerations

6.3.1 System Power

Increasing the performance of a CPU in addition to higher integration results in higher power consumption. This results in special requirements for the power supply of a VME system. The considerations presented in the ensuing sections must be taken into account by system integrators when specifying the VMP3 system environment.

6.3.2 VMP3 Voltage Ranges

The VMP3 board itself has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The table below indicates the absolute maximum input voltage rating that must not be exceeded. Power supplies to be used with the VMP3 should be carefully tested to ensure compliance with these ratings. The +12V and -12V inputs are not used by the VMP3**.**

Table 6-2: Absolute Maximum Rating

SUPPLY VOLTAGE	ABSOLUTE MAXIMUM RATINGS
+5 V	+7 V

Warning!

The maximum permitted voltage indicated in the table above must not be exceeded. This may also be reduced if an expansion board requires a lower voltage. Failure to comply with the above may result in damage to your board.

The following table specifies the range for the input power voltage within which the board is functional. The VMP3 is not guaranteed to function if the board is not operated within the prescribed limits.

Table 6-3: DC Operational Input Voltage Range

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE	RECOMMENDED RANGE	REMARKS
+5 V	4.6 V min. to 5.5 V max.	4.75 V min. to 5.25 V max.	Main voltage

6.3.3 Backplane Requirements

Backplanes to be used with the VMP3 must be adequately specified. The backplane must provide optimal power distribution for the +5 V power input. It is recommended to use only backplanes which have two power planes for the +5 V and GND.

Input power connections to the carrier itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided.

6.3.4 Power Supply Units

Power supplies for the VMP3 must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. An industrial power supply unit should be able to provide at least twice as much power as the entire system requires.

As the design of the VMP3 has been optimized for minimal power consumption, the power supply unit should be stable even under no load conditions.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate carrier. The power supply should be sufficient to allow for die resistance variations.

Note ...

Some PSUs require a greater minimum load than a single VMP3 is capable of creating. When a PSU of this type is used, it will not power up correctly and the VMP3 may hangup. The solution is to use an industrial PSU or to add more load to the system.

If DC/DC power supplies are used, please ensure that the external main supply provides sufficient power in order to start-up the system properly. The external main supply should provide at least as much power as the system power supply is able to provide taking into consideration the inrush current.

Warning!

An underdimensioned power supply may cause damage to system components.

30504.01.VC.050727/091441

6.3.4.1 Voltage Ramp

Power supplies must comply with the following guidelines, in order to be used with the VMP3.

- Beginning at 10% of the nominal output voltage, the voltage must rise within > 0.1 ms to < 20 ms to the specified regulation range of the voltage. Typically: > 5 ms to < 15 ms.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.
- The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal Vout.

6.3.4.2 Recommended Operating Conditions

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

The following table provides information regarding the required characteristics for the input voltage.

Table 6-4: Input Voltage Characteristics

VOLTAGE	NOMINAL VALUE	TOLERANCE	MAX. RIPPLE (p-p)
+5 V	+5 VDC	+5%/-3%	50 mV
GND	Ground, not directly connected to protective earth (PE)		

6.3.4.3 Supply Voltage Regulation

The power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

Note ...

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it has gone below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

6.3.5 Power Consumption of the VMP3

The goal of this description is to provide a method to calculate the power consumption for the VMP3 board and for additional configurations. The MPC8541E processor, the Gigabit Ethernet, and the DDR SDRAM dissipate the majority of the thermal power.

The power consumption tables below list the voltage and power specifications for the VMP3 PHYs. The software used for this test was the ECOS based NetBootLoader without any power management features being enabled during the measurement. All measurements were conducted at a temperature of 25°C.

30504.01.VC.050727/091441

The following table provides power consumption information based on one memory size. Each Gigabit Ethernet channel will add up to 1.25 watts to the power envelope when connected and active.

Table 6-5: Power Consumption with 256 MB Memory

CORE FREQ (MHZ)	MEMORY FREQ (MHZ)	WATTS	REMARKS
528	264	7.92	Without the Gigabit Ethernet being connected
660	264	8.21	Without the Gigabit Ethernet being connected
792	264	8.44	Without the Gigabit Ethernet being connected

Note...

If less power consumption is required, it is possible to disable features of the CPU such as TSEC controllers, PCI, Security Engine, etc. which are not being used. For further assistance, contact technical Support at Kontron Modular Computers.

6.4 Start-Up Current of the VMP3

During the startup process, clamping and leakage effects result in a much higher “inrush current” than the current required for normal operation. For this reason power supplies used with the VMP3 must be able to provide 7 A during the first 10 ms of operation.

30504.01.VC.050727/091441

Appendix A

WDOG Functionality

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A. WDOG Functionality

To assist in understanding the functionality of the VMP3 watchdog (WDOG), the following functional state diagram is provided.

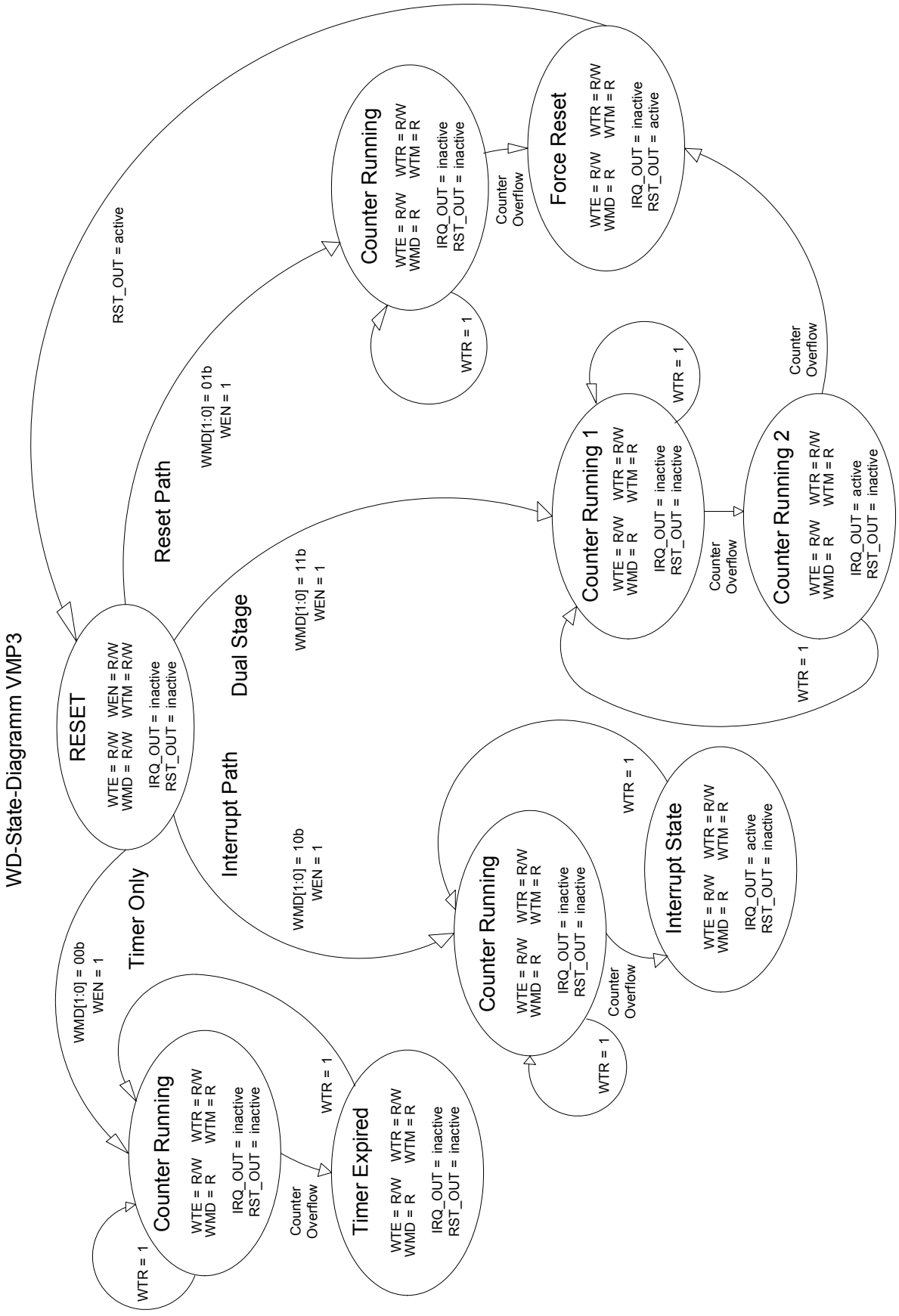

Figure A-1: WDOG Functional States

29230.01.UG.VC.050727/091441

Appendix B

VMP1-IO1 Module

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29230.01.UG.VC.050727/091442

B. VMP1-IO1 Module

B.1 Overview

The VMP1-IO1 module has been designed to provide an effective gateway to the world of PMC modules. Although developed for the VMP1, this module is suitable for use with the VMP3 and thus opens up a broad range of expansion possibilities.

PMC modules are renowned for their flexibility and versatility of use. They afford the user wide ranging system-independent solutions by means of easily interchanged or upgraded mezzanine add-on modules. The VMP1-IO1 has been designed to maximize the advantages provided by PMC modules in a 3U environment.

A special feature of the VMP3 is the ability to cascade two of these IO1 modules on top of one another. This means that the VMP3 is able to carry any two PMC modules. Tremendous advantages in terms of expandability and flexibility are thus made available to the user as a result of the addition of this capability to the board's many outstanding features.

The VMP1-IO1 is a 3U non-intelligent, passive CPCI-like carrier board with one PMC slot.

Some of the Outstanding Features of the VMP1-IO1:

- 32 Bit / 33MHz PCI-bus on the PMC side
- supports the Interrupts INTA, INTB, INTC and INTD
- supports all the signals of the PCI-bus on its connectors Jn1 (CON2) and Jn2 (CON3)
- connectors to the mezzanine board include all the signals of a 33MHz, 32-bit, multi-master PCI-bus, the power rails for 5V, 3.3V, V(I/O), and other specialized signals for board detection

B.2 Board Interfaces

B.2.1 PCI Expansion Connector

The PCI expansion connectors CON2/CON3 provide all the necessary signals for data transfer as defined by PCI Specification Rev. 2.1.

B.2.2 PMC Interface

The PMC interface provides an easy way to extend the VMP3 via the wide array of interfaces and functions which are available on PMC modules produced by the entire range of PMC vendors. PMC connectors provide a 32-bit wide PCI data path with a speed of up to 33MHz which is routed to the onboard connectors Jn1 and Jn2. These connectors also provide the power supply for the PMC module. The interface has been designed to comply with the IEEE 1386.1 specification which defines a PCI electrical interface for the CMC (Common Mezzanine Card) form factor.

B.2.3 Power Supply

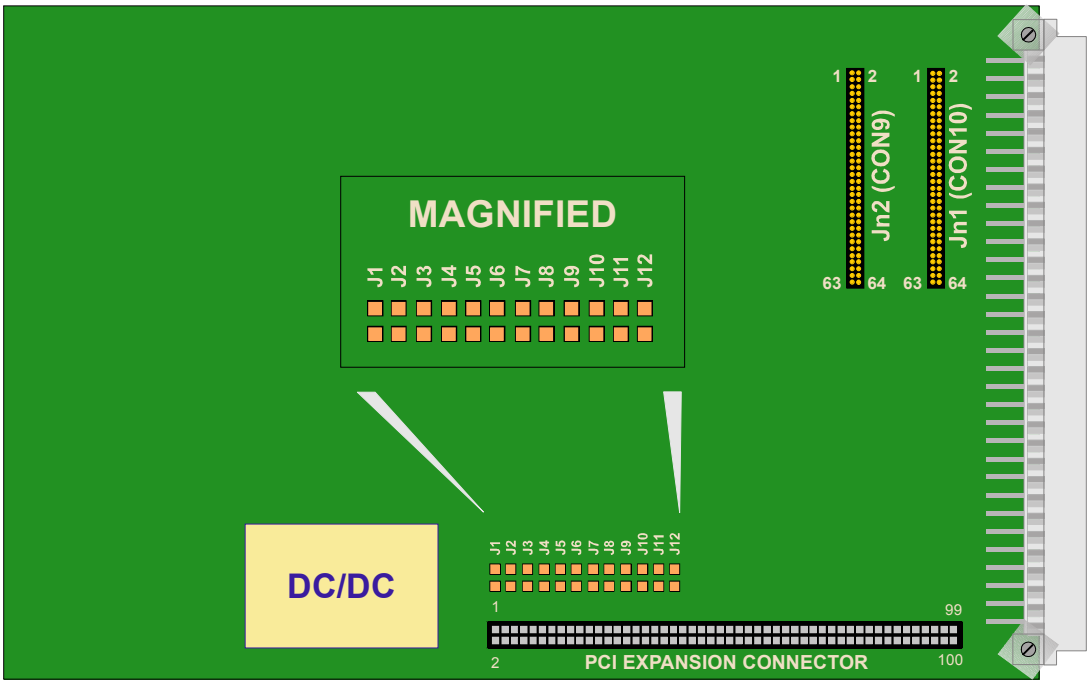
The onboard DC/DC converter of the VMP1-IO1 also produces a 3.3V supply voltage from the 5V provided on the VME backplane. This is necessary in order to create compatibility with the PMC modules whose power consumption is in excess of what the baseboard (VMP1-IO1) can provide.

29230.01.UG.VC.050727/091442

B.3 Board Layout

The VMP1-IO1 has two onboard connectors (CON9 and CON10) which provide all the PCI signals and the power supply for the PMC module.

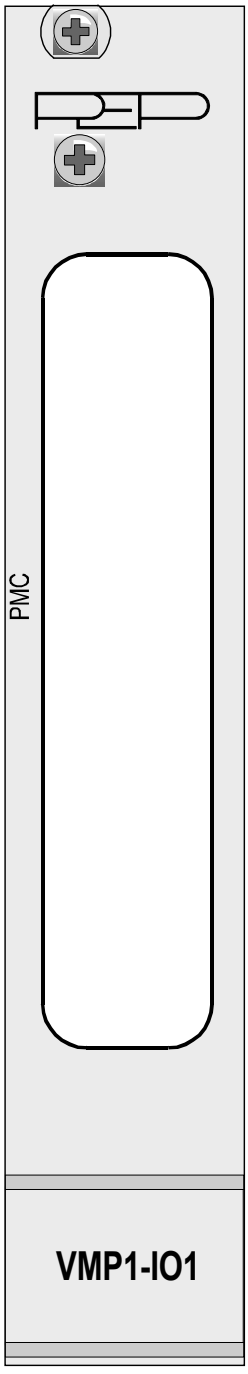
Figure B-1: Board Layout (Front View)



B.4 VMP1-IO1 Front Panel

The VMP1-IO1 front panel is provided with a window for the insertion of a PMC module bezel.

Figure B-2: VMP1-IO1 Front Panel



29230.01.UG.VC.050727/091442

B.5 Technical Specifications

Table B-1: VMP1-IO1 Specifications

VMP1-IO1	SPECIFICATIONS
PCI-Standard	Compliant with PCI 2.1
Signaling Voltage	PMC-Side: 5V signaling
Connectors	PMC Jn1 (CON4) and Jn2 (CON5) connectors
Mechanical Compliance	IEEE 1101.10 CMC IEEE P1386/Draft 2.0 (with minor exceptions)
Temperature Range	Operation: • -40° to +85°C Storage: • -55° to +85°C
Operating Humidity	5 – 95% (non condensing)
Vibrations and Broad-Band Random Vibration	IEC68-2-6 compliant IEC68-2-64
Shocks: Permanent Shocks Single Shock	 IEC68-2-29 IEC68-2-27
Board Dimensions	Single-height Eurocard: 100 mm x 160 mm 1 x 4 HP slot
Board Weight	114 grams

29230.01.UG.VC.050727/091442

B.6 Board Installation

In order to keep the installation process as simple and easy as possible please follow the recommended order of work:

1. Install the PMC module on the VMP1-IO1
2. Install the package (VMP1-IO1 plus PMC module) on the VMP3

ESD Equipment!

Your carrier board and PMC module contain electrostatic sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector pins, or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

PMC Module Installation

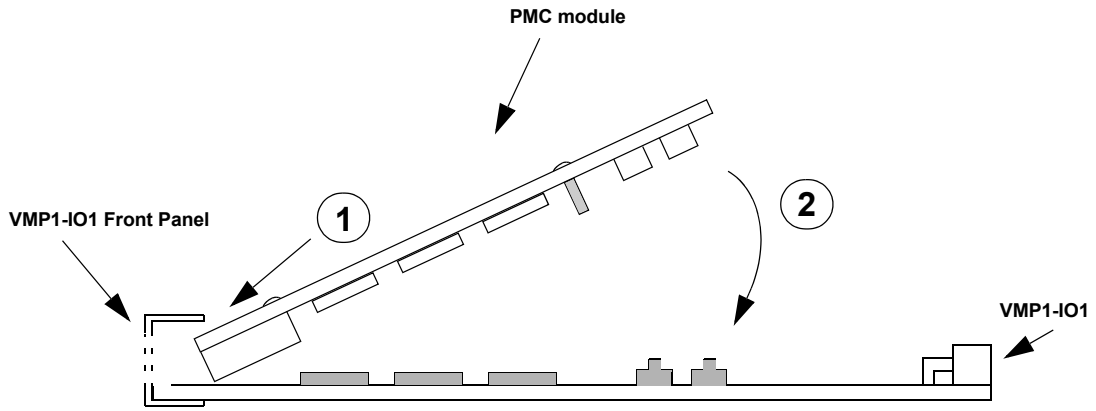
3. Place the EMC gasket on the bezel of your PMC module
4. Push the PMC bezel into the window of the front panel of the VMP3 and plug the connectors together.
5. Use three screws (M2.5 x 6mm) to secure the module to the board

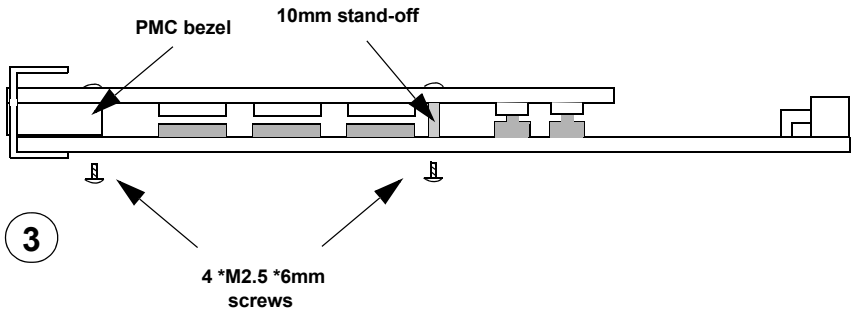
Installation of the VMP1-IO1 Module on the VMP3

6. Place the VMP1-IO1 exactly above the VMP3
7. Plug them together
8. Use 4 screws (2.5 x 6 mm) to secure the board to the VMP3

29230.01.UG.VC.050727/091442

Figure B-3: Installation Diagrams





B.7 Pinouts

B.7.1 Jn1 (CON4) Pin Assignment

Table B-2: Jn1, 32-bit PCI

PIN NUMBER	SIGNAL NAME	SIGNAL NAME	PIN NUMBER
1	TCK	-12V	2
3	Ground	INTA#	4
5	INTB#	INTC#	6
7	BUSMODE1#	+5V	8
9	INTD#	PCI-RSVD	10
11	Ground	PCI-RSVD	12
13	CLK	Ground	14
15	Ground	GNT#	16
17	REQ#	+5V	18
19	V(I/O)	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	Ground	24
25	Ground	C/BE[3]#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	V(I/O)	AD[17]	32
33	FRAME#	Ground	34
35	Ground	IRDY#	36
37	DEVSEL#	+5V	38
39	Ground	LOCK#	40
41	SDONE#	SBO#	42
43	PAR	Ground	44
45	V(I/O)	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	Ground	C/BE[0]#	52
53	AD[06]	AD[05]	54
55	AD[04]	Ground	56
57	V(I/O)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	Ground	REQ64#	64

29230.01.UG.VC.050727/091442

B.7.2 Jn2 (CON5) Pin Assignment

Table B-3: Jn2, 32-bit PCI

PIN NUMBER	SIGNAL NAME	SIGNAL NAME	PIN NUMBER
1	+12V	TRST#	2
3	TMS	TDO	4
5	TDI	Ground	6
7	Ground	PCI-RSVD	8
9	PCI-RSVD*	PCI-RSVD	10
11	BUSMODE2#	+3.3V	12
13	RST#	BUSMODE3#	14
15	3.3V	BUSMODE4#	16
17	PCI-RSVD*	Ground	18
19	AD[30]	AD[29]	20
21	Ground	AD[26]	22
23	AD[24]	+3.3V	24
25	IDSEL	AD[23]	26
27	+3.3V	AD[20]	28
29	AD[18]	Ground	30
31	AD[16]	C/BE[2]#	32
33	Ground	PMC-RSVD	34
35	TRDY#	+3.3V	36
37	Ground	STOP#	38
39	PERR#	Ground	40
41	+3.3V	SERR#	42
43	C/BE[1]#	Ground	44
45	AD[14]	AD[13]	46
47	Ground	AD[10]	48
49	AD[08]	+3.3V	50
51	AD[07]	PMC-RSVD	52
53	+3.3V	PMC-RSVD	54
55	PMC-RSVD	Ground	56
57	PMC-RSVD	PMC-RSVD	58
59	Ground	PMC-RSVD	60
61	ACK64#	+3.3V	62
63	Ground	PMC-RSVD	64

29230.01.UG.VC.050727/091442

B.8 Jumper Setting

The jumper settings of the IO1 module depend on the module's position relative to the VMP3 and other modules, if any.

Table B-4: IO1 Jumper Settings for Different Module Positions

	IDSEL			Clock			GNT#			REQ#		
	J12	J11	J10	J1	J2	J3	J4	J5	J6	J7	J8	J9
Position 1	Set	Open	Open	Set	Open	Open	Set	Open	Open	Set	Open	Open
Position 2	Open	Set	Open	Open	Set	Open	Open	Set	Open	Open	Set	Open
Position 3	Open	open	Set	Open	Open	Set	Open	Open	Set	Open	Open	Set

Note:

Position 1 refers to the settings applicable when 1 module (IO1 or other) is attached to the VMP3.

Position 2 refers to the settings applicable when 2 modules (IO1 or other) are attached to the VMP3.

Position 3 refers to the settings applicable when 3 modules (IO1 or other) are attached to the VMP3.

Important!:

Position 3 has not yet been tested and approved and is not recommended for use with this issue of the manual.

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29230.01.UG.VC.050727/091443

Appendix C

VMP1-HDD1 Module

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C. VMP1-HDD1 Module

C.1 Board Description

The VMP1-HDD1 Module provides the PowerPC-based CPU boards with a cost-effective way to add substantial mass storage capacity. It is designed to connect a 2.5” IDE hard disk drive to the PCI bus of those boards. It is based on the silicon image IDE controller SiI0680, which provides the interface between the 32-bit wide, 33 MHz PCI bus and a standard IDE hard disk drive. It is able to handle transfer rates up to the ATA-133 speed standard.

Note...

The maximum transfer rate which can be achieved with this module is restricted by the hard drive in use.

The capacity of the module is defined by the hard drive in use.

Figure C-1: VMP1-HDD1 Module with Hard Disk Drive Attached

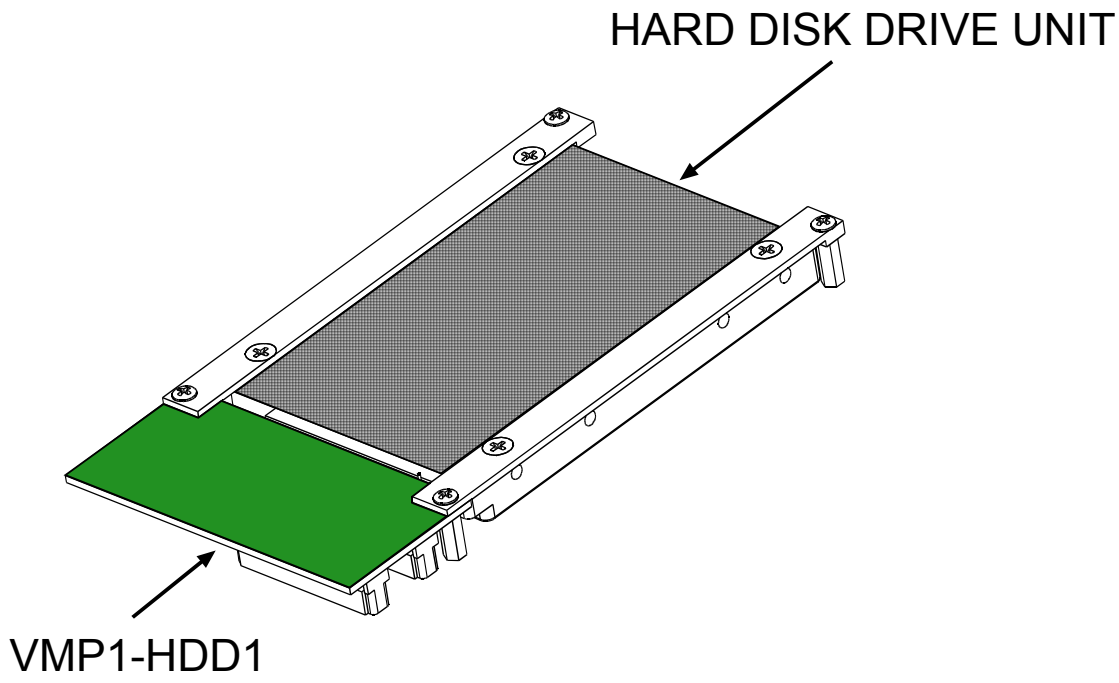

Table C-1: Pinout of the PMC Connectors

PN1/JN1 (CON1)				PN2/JN2 (CON2)			
PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN
1	Signal	-12V	2	1	+12V	Signal	2
3	Ground	Signal	4	3	Signal	Signal	4
5	Signal	Signal	6	5	Signal	Ground	6
7	BUSMODE1#	+5V	8	7	Ground	Signal	8
9	Signal	Signal	10	9	Signal	Signal	10
11	Ground	Signal	12	11	BUSMODE2#	+3.3V	12
13	Signal	Ground	14	13	Signal	BUSMODE3#	14
15	Ground	Signal	16	15	+3.3V	BUSMODE4#	16
17	Signal	+5V	18	17	Signal	Ground	18
19	V (I/O)	Signal	20	19	Signal	Signal	20
21	Signal	Signal	22	21	Ground	Signal	22
23	Signal	Ground	24	23	Signal	+3.3V	24
25	Ground	Signal	26	25	Signal	Signal	26
27	Signal	Signal	28	27	+3.3V	Signal	28
29	Signal	+5V	30	29	Signal	Ground	30
31	V (I/O)	Signal	32	31	Signal	Signal	32
33	Signal	Ground	34	33	Ground	Signal	34
35	Ground	Signal	36	35	Signal	+3.3V	36
37	Signal	+5V	38	37	Ground	Signal	38
39	Ground	Signal	40	39	Signal	Ground	40
41	Signal	Signal	42	41	+3.3V	Signal	42
43	Signal	Ground	44	43	Signal	Ground	44
45	V (I/O)	Signal	46	45	Signal	Signal	46
47	Signal	Signal	48	47	Ground	Signal	48
49	Signal	+5V	50	49	Signal	+3.3V	50
51	Ground	Signal	52	51	Signal	Signal	52
53	Signal	Signal	54	53	+3.3V	Signal	54
55	Signal	Ground	56	55	Signal	Ground	56
57	V (I/O)	Signal	58	57	Signal	Signal	58
59	Signal	Signal	60	59	Ground	Signal	60
61	Signal	+5V	62	61	Signal	+3.3V	62
63	Ground	Signal	64	63	Ground	Signal	64

29230.01.UG.VC.050727/091443

Table C-2: IDE Hard Disk Drive Connector Pinout

PIN	SIGNAL	FUNCTION	IN/OUT
1	IDERESET	Reset HD	Out
2	GND	Ground signal	--
3	HD7	HD data 7	In/Out
4	HD8	HD data 8	In/Out
5	HD6	HD data 6	In/Out
6	HD9	HD data 9	In/Out
7	HD5	HD data 5	In/Out
8	HD10	HD data 10	In/Out
9	HD4	HD data 4	In/Out
10	HD11	HD data 11	In/Out
11	HD3	HD data 3	In/Out
12	HD12	HD data 12	In/Out
13	HD2	HD data 2	In/Out
14	HD13	HD data 13	In/Out
15	HD1	HD data 1	In/Out
16	HD14	HD data 14	In/Out
17	HD0	HD data 0	In/Out
18	HD15	HD data 15	In/Out
19	GND	Ground signal	--
20	N/C	--	--
21	IDEDRQ	DMA request	In
22	GND	Ground signal	--
23	IOW	I/O write	Out
24	GND	Ground signal	--
25	IOR	I/O read	Out
26	GND	Ground signal	--
27	IOCHRDY	I/O channel ready	In
28	GND	Ground signal	--
29	IDEDACKA	DMA Ack	Out
30	GND	Ground signal	--
31	IDEIRQ	Interrupt request	In
32	N/C	--	--
33	A1	Address 1	Out
34	N/C	--	--
35	A0	Address 0	Out
36	A2	Address 2	Out
37	HCS0	HD select 0	Out
38	HCS1	HD select 1	Out
39	NC	--	In
40	GND	Ground signal	--
41	VCC	5V power	--
42	VCC	5V power	--
43	GND	Ground signal	--
44	N/C	--	--

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