Modular Computers®

CP620-PM

Power PC-based 6U CPU Board for CompactPCI Applications

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The product described in this manual is in compliance with all applied CE standards.

Revision History

Manual/Product Title:	CP620-PM		
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04	New board index with PICMG 2.16 features	02	Aug. 2002

Imprint

Modular Computers®

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This manual was realized by: **TPD/Engineering, PEP Modular Computers GmbH**.

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This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.

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This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.

Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.

Note...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

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High Voltage Safety Instructions

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Special Handling and Unpacking Instructions

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Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board please re-pack it as nearly as possible in the manner in which it was delivered.

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Chapter 1

Introduction

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1. Introduction

1.1 System Overview

The CompactPCI board described in this manual operates with the PCI bus architecture to support additional I/O and memory-mapped devices as required by various industrial applications. For detailed information concerning the CompactPCI standard, please consult the complete Peripheral Component Interconnect (PCI) and CompactPCI Specifications. For further information regarding these standards and their use, visit the homepage of the *PCI Industrial Computer Manufacturers Group (PICMG)*.

Many system-relevant CompactPCI features that are specific to *PEP Modular Computers* CompactPCI systems may be found described in the *PEP* CompactPCI System Manual. Due to its size, this manual cannot be downloaded via the internet. Please refer to the section “Related Publications” at the end of this chapter for the relevant ordering information.

The CompactPCI System Manual includes the following information:

- Common information that is applicable to all system components, such as safety information, warranty conditions, standard connector pinouts etc.
- All the information necessary to combine *PEP's* racks, boards, backplanes, power supply units and peripheral devices in a customized CompactPCI system, as well as configuration examples.
- Data on rack dimensions and configurations as well as information on mechanical and electrical rack characteristics.
- Information on the distinctive features of *PEP* CompactPCI boards, such as functionality, hotswap capability. In addition, an overview is given for all existing *PEP* CompactPCI boards with links to the relating datasheets.
- Generic information on the *PEP* CompactPCI backplanes, such as the slot assignment, PCB form factor, distinctive features, clocks, power supply connectors and signalling environment, as well as an overview of the *PEP* CompactPCI standard backplane family.
- Generic information on the *PEP* CompactPCI power supply units, such as the input/output characteristics, redundant operation and distinctive features, as well as an overview of the *PEP* CompactPCI standard power supply unit family.

1.2 Product Overview

The principal difference between a system controller board such as the CP604 and the peripheral controller CP620-PM lies in the nature of the CompactPCI architecture. The system controller generates all necessary PCI control signals, reset, clock and arbitration, and uses a transparent bridge for the PCI interface, therefore all PCI devices are visible to the system controller and all standard drivers may be used.

The CP620-PM (Peripheral Master) uses a non-transparent PCI bridge, a so called “drawbridge”. This bridge is specifically designed to bridge between two processor domains, one on the CompactPCI interface and the other local on the CP620-PM controller. The drawbridge is the first PCI bridge to enable multiprocessing on a CompactPCI system. This bridge can isolate two PCI busses.

The CP620-PM with all onboard PCI devices is to the CompactPCI bus visible as a single PCI device. With this configuration the system controller CPU board could control all PCI devices on the CompactPCI bus, while the CP620-PM controls all onboard PCI devices.

Communication between the system master and the peripheral CP620-PM may be effected via the *PEP* TCP/IP backplane software package RackNet.

A special board version of the CP620-PM has the additional possibility to communicate with its neighbourhood via IEEE 802 (Ethernet) providied on J3. This is in accordance with the CompactPCI Packet Switching Backplane Specification PICMG 2.16, Revision 1.0, September 5th 2001.

Designed for stability and packaged in a rugged format, the board fits into all applications situated in industrial environments. The low power consumption of the board is further assured through the use of IBM PowerPC technology.

The performance of CompactPCI can be tailored to suit real-time applications and operating systems such as Linux®, QNX® or VxWorks® which are instrumental to the success of CompactPCI in these market sectors.

1.3 Board Overview

1.3.1 Board Introduction

The CP620-PM is a highly integrated 6U CompactPCI Peripheral Master CPU board. The design is based on the combination of an IBM PPC750CX/CXE PowerPC CPU with the MPC107 Motorola PCI-Bridge/Memory Controller and can support CPU speeds of 400 through 700 MHz (with higher speeds available in the future) and host bus speeds up to 100MHz.

The design centered on realizing a board which addresses the need for extending IO capability with PMC-Modules while at the same time having a powerful CPU, a big amount of memory and a optimized power dissipation. Therefore the CP620-PM provides 2 PMC slots with rear I/O routing to CompactPCI P3 and P5 connectors and a powerful CPU from IBM with speeds up to 700 MHz (and even higher in the future).

Memory configurations of 128 MB to 1GB SDRAM are possible, running at 100 MHz and providing ECC error correction mechanism. This provides single-bit error correction or double-bit error detection for critical applications. In addition to the normal system memory, 8 MB of onboard flash memory for including the initial bootloader and romable operating systems are provided . For extending this onboard memory, sockets for DIL-Flash/NVSRAM and CompactFlash are supported by the CP620-PM.

The processor chip itself contains a powerful general purpose G3 processing unit, a floating point unit and a 256 kB internal second level cache which runs at the CPU clock speed. The combination of high integration within a small form factor makes it possible for a sophisticated 6U board with a comprehensive set of features to carry, in addition, two PMC modules.

Both PMC Slots have a 32-bit/33 MHz PCI interface.

The connection to the CompactPCI bus is achieved using the Intel non-transparent 21554/21555-PCI-to-PCI bridge which makes it possible to add of further CP620-PM's or CP604-PM's with a system controller CPU on one CompactPCI bus, i.e. multiprocessing. The CompactPCI bus width is 64-bit at 33MHz with the functionality of CompactPCI Hotswap. Hotswap means that the board can be installed in and removed from a hotswap compliant backplane while the rest of the system is powered up and running.

The local PCI bus runs at a 33 MHz PCI clock frequency and the bus has a 32-bit width.

The CP620-PM communicates with its environment using two Fast Ethernet interfaces and one RS-232 terminal interface on the front side, or by using an optional rear IO board, which can provide the 2 Ethernet channels and 4 serial interfaces.

The Ethernet is realized using the Intel 82559 Fast Ethernet controller. Full duplex support at both 10 and 100 Mbps is possible.

The serial interfaces are realized with two DUAL UART 16C2850's, which include two 16550 software compatible serial interfaces in one package. They contain 128 Bytes Transmit and 128 Bytes receive FIFO each to increase the CPU availability for other operations. These UART's also provide the hardware control signals for RS-422/485 transmission. If galvanic decoupling needs to be realized, the isolation will have to be effected on the rear I/O board.

The CP620-PM employs an OS-independent boot loader that enables the loading of any operating system available for the PowerPC. This boot loader makes an update of the Flash contents and automatically downloads from Flash to SDRAM before booting the OS. For performance reasons, the OS and user programms are started from the SDRAM.

The first operating systems which will be available for the CP620-PM are Linux and VxWorks. Others will follow on demand.

1.3.2 Board-Specific Information

The CP620-PM is a CompactPCI PowerPC-based single-board computer specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

- Processor: IBM PPC750CX/CXE (Generation 3) with CPU speeds of up to 700 MHz and an integrated FPU
- 256 kB L2 Cache running at CPU speed
- Chipset: Motorola MPC107
- Compliance with 64-bit CompactPCI Interface 2.0 R3.0 at 33 MHz
- Peripheral Master with HotSwap capability (PICMG 2.1, version 1.0)
- 4HP 6U CompactPCI
- Up to 1 GB SDRAM / 100 MHz with ECC
- Up to 8 MB onboard Flash
- One user EEPROM (8192 x 8) / one system EEPROM
- CompactFlash expansion port
- 32-pin DIP Memory expansions socket for additional Flash/SRAM/NVSRAM/EPROM
- Two PMC PCI-Bus expansion slots (33 Mhz, 32-bit)
- PMC slots with rear I/O routing
- On-board interfaces:
- 2 Fast Ethernet interfaces
- 4 serial interfaces / one available on the front panel / all 4 serial interfaces available on rear I/O
- ESD protected and EMI compliant
- Four counters/timer
- Programmable watchdog timer
- Real time clock
- IPMI compliant baseboard management controller (optional)
- Temperature sensing
- Front panel LED status indicators
- Debug interface, JTAG/COP
- Operating systems: VxWorks, Linux.....

1.4 Extension Modules

The CP620-PM has been designed to hold up to two PMC modules and has rear I/O capability

1.4.1 PMC Modules

PMC modules provide an easy, very flexible way to configure the CP620-PM for different interfaces. A wide range of PMC modules exists on the market (including PEP's PMC modules; such as the PMC260 and PMC251) which can be connected to CP620-PM via the onboard PMC slots. Up to two of these modules can be placed on the CP620-PM at the same time.

1.4.2 Rear I/O

All interfaces on the CP620-PM are also available via the rear I/O connectors J3 - J5. These interfaces include four serial ports, two Fast Ethernet ports, the IPMI signals and the rear I/O signals from the PMC modules. If these interfaces are needed on the rear side of a system, a board specific rear I/O Module has to be defined, designed to meet the users' specific requirements.

A special board version of the CP620-PM provides, in addition, the Ethernet channels on J3, for use with a PICMG 2.16 compliant backplane.

1.4.3 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the CP620-PM.

Table 1-1: System Relevant Information

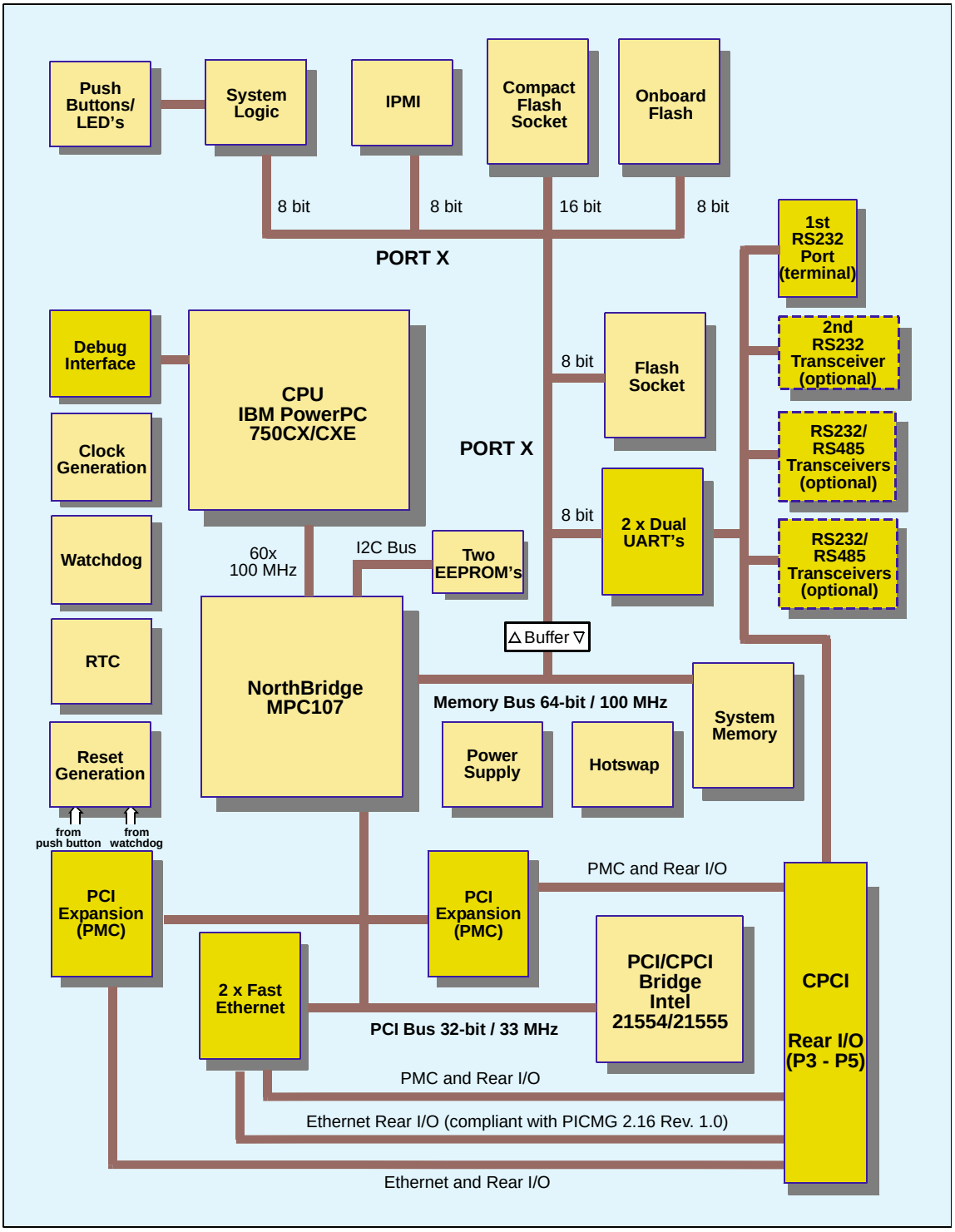
SUBJECT	INFORMATION
System Configuration	A CP620-PM-based system is made up of at least one system controller (for example CP603, CP604 or CP612) and up to 7 other I/O boards can be located within one system.
Master/Slave Functionality	The CP620-PM can operate only as a peripheral board.
Board Location in the System	The CP620-PM board must be installed in a peripheral slot of a CPCI backplane.
Hot-Swap Compatibility	The CP620-PM supports all necessary signals to be removed or added while the system remains in a powered-up state.The CP620-PM is complies with the PICMG 2.1 hotswap specification.
Hardware Requirements	The CP620-PM can be installed in any CompactPCI 6U rack.
Operating Systems	The CP620-PM can operate under the following operating systems: VxWorks®, Linux plus others

1.5 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

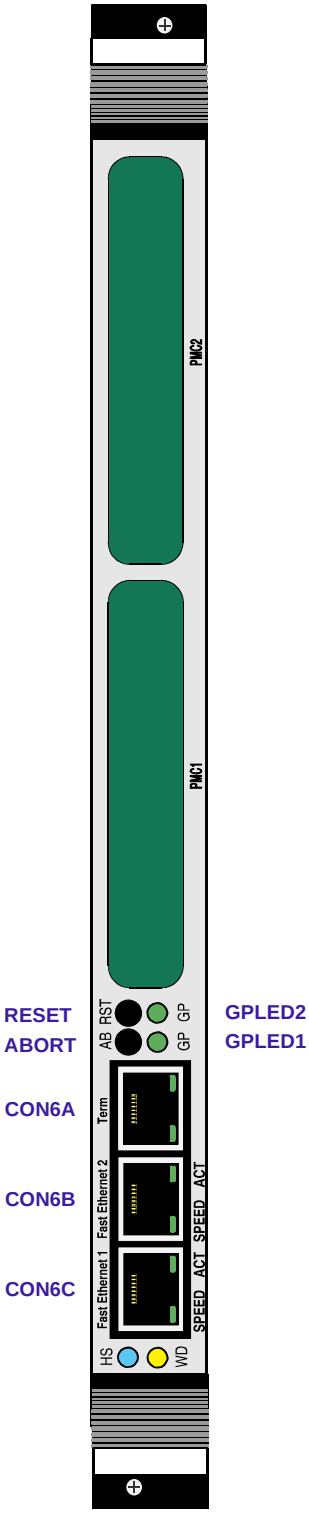
1.5.1 Functional Block Diagram

Figure 1-1: Functional Block Diagram



1.5.2 Front Panel

Figure 1-2: CP620-PM Front Panel



LEGEND:

LED's

GP	User	(green)
HS	Hotswap	(blue)
WD	Watchdog	(yellow)

Ethernet LED's

ACT	Activity	(yellow)
SPEED	Speed	(green)

Switches

RST	Reset
AB	Abort

1.5.3 Board Layout

Figure 1-3: CP620-PM Board (Front View)

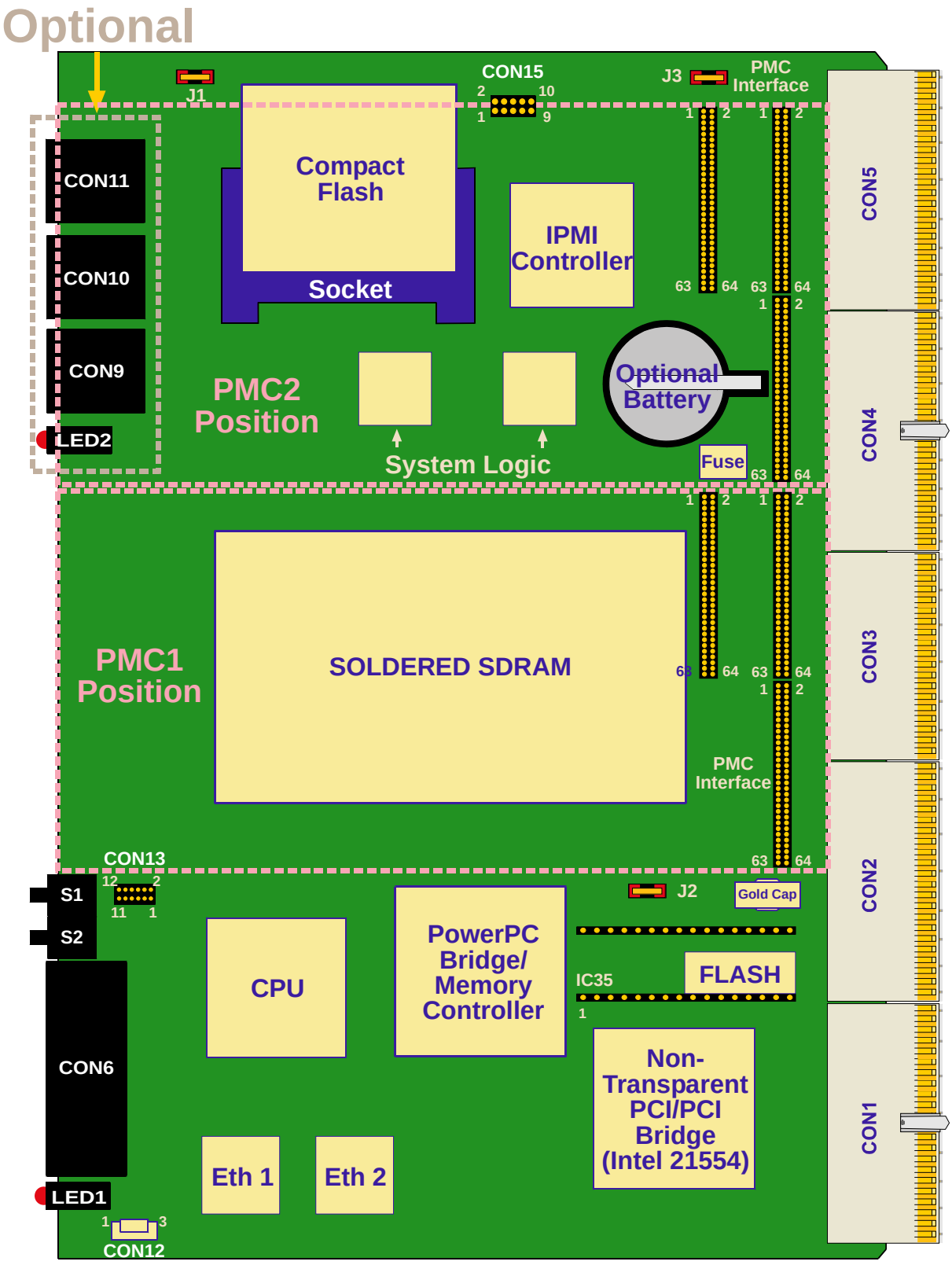
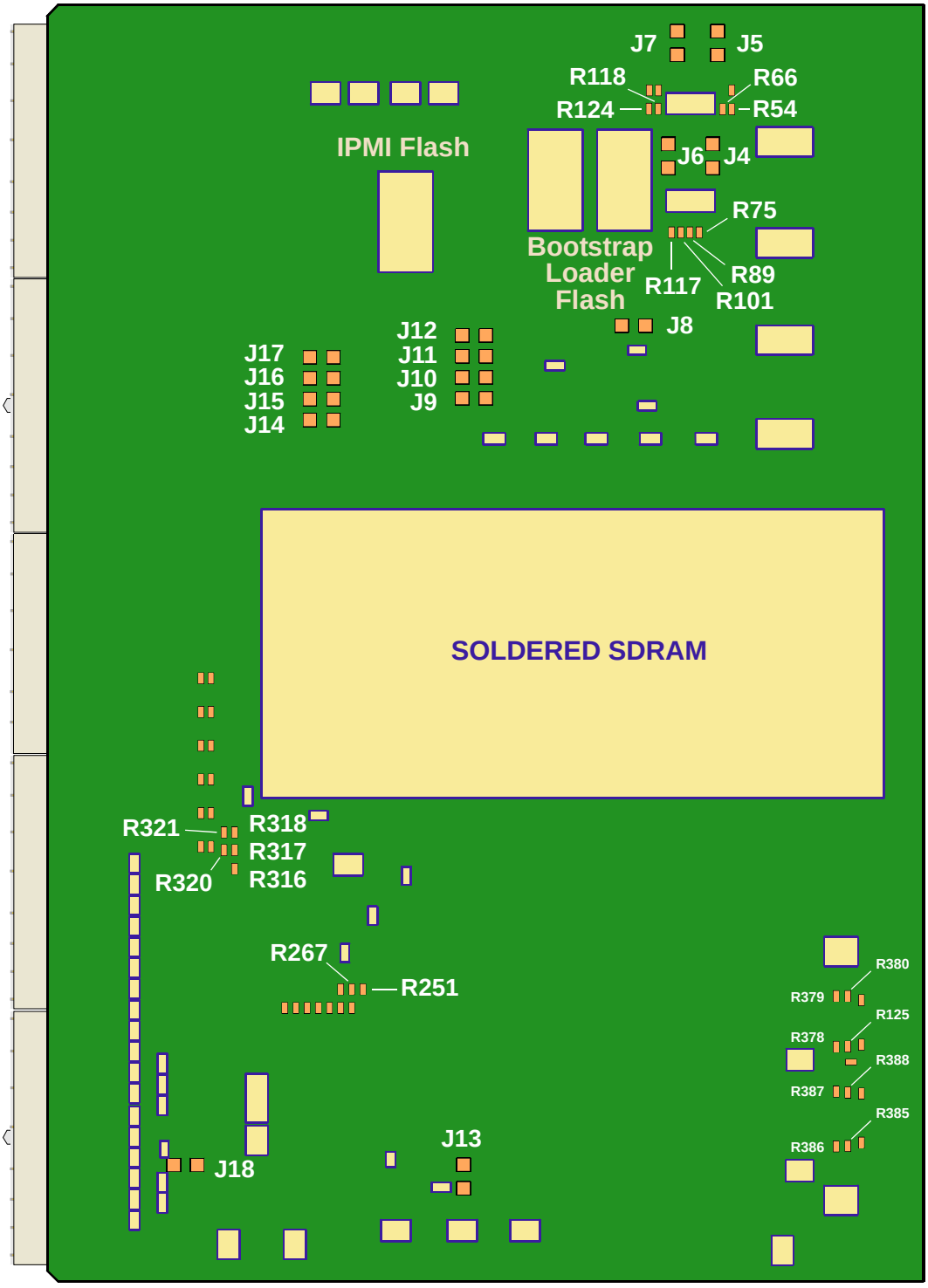


Figure 1-4: CP620-PM Board (Reverse View)



1.6 Technical Specifications

Table 1-2: CP620-PM Main Specifications

	CP620-PM	Specifications
Processor and Related	Processor	IBM PPC750CX/CXE with integrated Level 2 cache (256 kB) Clock speed up to 700 MHz / Level 2 cache at CPU speed
	Chipset	Motorola MPC107 PowerPC-PCI Bridge/Memory Controller with 100 MHz CPU bus clock speed
	CompactPCI Interface	Peripheral Master, compliant with PICMG 2.0 Rev.3.0 and CompactPCI Hotswap specification PICMG 2.1 version 1.0 64-bit/33 MHz peripheral interface, universal signaling voltage (3.3V, to fit in 3.3V or 5V bus) Intel Drawbridge 21554/21555
	Main memory	128 MB to 1 GB of onboard SDRAM (soldered) with ECC support running at 100 MHz 64-bit wide
	Cache Structure	256 KB, 256-bit wide, running at CPU speed
	Watchdog	Software configurable Watchdog generates Exception-Condition / Reset or NMI
	RTC	Realtime clock backed up using Gold Cap with the Data retention being about 5 days (optionally, a backup battery is available)
	TemperatureSensor	1x LM75, connected to I2C bus
Peripheral Memory	Flash / Boot device	8 MB soldered flash for bootloader and romable OS 32-pin DIP600 expansion socket
	SRAM	- support for 256 or 512 kB NVSRAM on DIP600 socket
	EEPROM (I2C)	1 x serial EEPROM for system purpose (8 x 8kB) plus 1 x serial EEPROM for general purpose (8 x 8kB) write protection possible
	Memory Expansion	1x 32-pin DIP600 socket which can be jumpered for use with Flash-, Eprom-, SRAM-Memory 1x CompactFlash Socket Type II (IDE-Mode)

Table 1-2: CP620-PM Main Specifications (cont'd)

	CP620-PM	Specifications
External Interfaces	Fast-Ethernet	2 x 10Base-T / 100Base-TX realised with 2 Intel 82559ER Fast Ethernet controllers cabling: Category 5 two-pair cabling with RJ45 connectors Optional: connection via PICMG 2.16 backplane
	Serial Ports	4 UART's (16550 compliant) with additional RS-485 support. 128 Byte transmit and 128 Byte receive buffer each The following interfaces are available if the board is used with 2 PMC's: all 4 UART's connected to rear I/O or 1 x RS-232 interface at the front panel (TERM) + 3 Uart's connected to rear I/O The following interfaces are available when only one PMC slot is used: all 4 UART's connected to rear I/O or 1x RS-232 interface at front panel (terminal) + 3 UART's connected to rear I/O or optional (special front panel version): 2x RS-232 + 2x RS-232/RS-485 (configurable) at front panel
	CPCI Connectors	CPCI- J1, J2, J3 and J5 equipped by default. J4 optional
Internal Interfaces	PCI Expansion	2 PMC interfaces, compliant with Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards PMC, P1386.1/Draft 2.0, 04-APR-1995. PCI master interfaces with 32-bit width and 33 MHz clock. 3.3V/5.0V compatible. PMC-Rear-IO routing to CPCI connectors J3 and J5
	Debug Interface	JTAG/COP interface for testing purposes (Connector type: SAMTEC FTSH-105-01-L-DV)
	Programming Interface	Second JTAG chain for logic programming
Indicators / Switches	LEDs	1 x LED blue: indicating HotSwap status 1 x LED yellow: indicating that "Watchdog Counter" is active 2 x LED green: General purpuse LED 2 x LED green (integrated in Ethernet RJ45 jack): Ethernet Link/Activity 2 x LED green (integrated in Ethernet RJ45 jack): Ethernet Speed
	Switches	Two, non-latching, debounced, push button type swithes: one for resetting the CPU and the other for aborting the boot process
Monitor and Control	IPMI	Onboard independent IPMI compliant baseboard management (BMC) controller realised with the Qlogic Zircon LT. The Zircon LT BMC controls all onboard voltages, the CPU temperature and optional external fans connected via the rear I/O interface connectors J4.

Table 1-2: CP620-PM Main Specifications (cont'd)

	CP620-PM	Specifications
General	Mechanical conformance	Conforms with IEEE 1101.10
	Power Consumption	400 MHz/128 MB: 5V/0.6A; 3.3V/1.5A 500 MHz/512 MB: 5V/0.9A; 3.3V/1.4A
	Temperature Range	0°C to +70°C Standard -25ºC to + 75ºC (E1) -40ºC - + 85ºC (E2) -55ºC ... +125ºC storage
	Humidity	0..95% non-condensing
	Dimensions	233,35mm x 160mm, double-height Eurocard (6U)
	Board Weight	400g
Software	Software/Operating System Support	Initial Boot loader , VxWorks, Linux etc.

1.7 Environmental Considerations

1.7.1 Absolute Maximum Electrical Ratings

Absolute Maximum Ratings indicate limits beyond which damage to the board may occur. Do not operate the CP620-PM at or beyond these maximum values.

Table 1-3: Voltage Limits

Supply Voltage	Maximum Permitted Value
+3.3V	+4.5V
+5V	+5.5V
+12V	+14V
-12V	-14V

1.7.2 DC Operating Characteristics

Operating Ratings indicate the parameters within which the board is functional. The CP620-PM cannot be guaranteed to function if the board is not operated under the limits described.

Table 1-4: Voltage Range

Supply Voltage	Limit
+3.3V	+3.20V min. to +3.47V max.
+ 5V	+4.85V min. to +5.25V max.
+12V	+11.4V min. to +12.6V max.
-12V	-11.4V min. to -12.6V max.

1.7.3 Power Consumption

The CP620-PM board is based on the IBM PPC750CXE PowerPC CPU processor. This processor consumes less power than the x86 based CPU's and the PowerPC's from Motorola and therefore dissipates less heat. The design is optimized for low power consumption applications.

The goal of this description is to provide a method to calculate the power consumption for the CP620-PM base board and for additional configurations. The processor dissipates the majority of the thermal power.

The power consumption table lists the voltage and current specifications for the CP620-PM board and the CP620-PM accessories. The values were measured with an 8-slot passive CompactPCI backplane. During measurement the power consumption of the backplane was ignored. Measurements were taken using the Bootstrap loader (no OS) and under the operating system VxWorks . All measurements were conducted at a temperature of 25°C. The measured values varied, because power consumption was dependent on processor activity. All PPC750CXe processors are powered with 1.8V core voltage.

Table 1-5: Power Consumption Table with Bootstrap Loader

Power	400 MHz 128 MB (128 Mbit chips)	500 MHz 512 MB (128 Mbit chips)	600 MHz 512 MB (128 Mbit chips)
5 V	0.6A / 3W	0.78A / 3.9W	TBD
3.3 V	1,54A / 5.08W	1.66A / 5.48W	TBD
Total	8.08W	9.38W	TBD

Table 1-6: Power Consumption Table with VxWorks Running (Application: Memory Transfer Test)

Power	400 MHz 128 MB (128 Mbit chips)	500 MHz 512 MB (128 Mbit chips)	600 MHz 512 MB (128 Mbit chips)
5 V	TBD	1.14A / 5.7W	TBD
3.3 V	TBD	1.12A / 3.7W	TBD
Total	TBD	9.4W	TBD

Table 1-7: Power Consumption Table for CP620-PM Accessories

Module	Power 5V	Power 3.3V
DiskOnChip™ 16 MB	100 mW	--
DiskOnChip™ 144 MB	100 mW	--
CompactFlash	--	TBD

1.7.4 Temperature Range and Air Flow

The CP620-PM has been designed to operate at an extended temperature range from -40°C up to + 85°C. All onboard components are specially selected for the higher temperature range. The processors used here are produced with the new 0.18-micron copper process which have lower power consumption and support high case temperatures (105°C).

These values have been measured with typical applications under Linux and VxWorks. In worst case situations the values and the temperature range must be reduced accordingly. For all situations the maximum case temperature of the PPC750CXE processor must not exceed 105°C. This temperature value can be measured using the on-chip thermal management unit of the PPC750CXE processor. In instances of overtemperature the thermal management unit will reduce the processor clock speed in order to reduce power generation.

Table 1-8: Typical Temperature Range and Required Air Flow

Heat Sink Version	Range	400 MHz	500 MHz	600 MHz
4HP	0°C to +60°C	TBD	TBD	TBD
	-25°C to +75°C	TBD	TBD	TBD
	-40°C to +85°C	TBD	TBD	TBD

0 m/s air flow means standard convection cooling with the board in an upright position. An airflow of 1 m/s is a typical value for a standard *PEP* ASM 4 rack (6U CompactPCI rack with 1U cooling fans). For other racks or housings the available airflow will be different. The maximum ambient temperature must be recalculated and / or measured for such environments. For the calculation of the maximum ambient temperature the processor case temperature must never exceed 105°C. The maximum heatsink temperature depends on the physical characteristics of the heatsink and thermal connection to the processor. To ensure that the heatsink temperature does not exceed its limits an airflow may be needed for a given ambient temperature. Heatsink temperature is measured at the top of the heatsink base, closest to the processor.

Warning!

It is the responsibility of the end user to ensure that the processor case temperate never exceeds 105°C in order to protect the board against overheating. Permanent overheating can damage the board.

If the temperature on the processor die is greater than 105°C the maximum ambient temperature must be reduced or an external airflow must be provided by means of an additional fan.

1.7.5 Storage Temperatures

- Storage temperature –55°C to +85°C
- Humidity non-condensing 0% to 95% at 40°C

1.8 Applied Standards

The *PEP Modular Computers'* CompactPCI systems comply with the requirements of the following standards:

Table 1-9: Applied Standards

COMPLIANCE	TYPE	STANDARD	Test Level (Ruggedized Version)
CE	Emission	EN50081-1	--
	Immission	EN50082-2	--
	Electrical Safety	EN60950	--
Mechanical	Mechanical Dimensions	IEEE 1101.10	--
Environmental	Vibration (Sinusoidal)	IEC68-2-6	2g/12-300Hz/10 acceleration / frequency range / test cycles
	Random Vibration (Broadband)	IEC68-2-64 (3U boards)	20-500Hz,0.1g²/500-2000Hz,0.01g²/7g rms/3/30min frequency range1 / frequency range2 /acceleration / cycle / duration
	Permanent Shock	IEC68-2-29	15g/11ms/3000/1s peak acceleration / shock duration half sine / number of shocks / recovery time
	Single Shock	IEC68-2-27	30g/9ms/18/5s peak acceleration / shock duration / number of shocks / recovery time in sec.

1.9 Related Publications

The following publications contain information relating to this product.

Table 1-10: Related Publications

PRODUCT	PUBLICATION
CompactPCI Systems and Boards	CompactPCI Specification 2.0, Rev. 3.0
	PEP Modular Computers' CompactPCI System Manual, ID 19954
	CompactPCI Packet Switching Backplane Specification PICMG 2.16 Rev 1.0
PMC Add-on Modules and Carriers	Draft standard for Common Mezzanine Card Family: P1386, Draft 2.0
	Draft standard for Physical and Environment Layers for PCI Mezzanine Cards: P1386.1, Draft 2.0
Compact Flash Cards	CF+ and Compact Flash Specification Revision 1.4

1.10 Trademarks

CompactPCI is a trademark of the PCI industrial Computers manufacturers group.

Ethernet is a registered trademark of Xerox corporation.

IEEE is a registered trademark of the Institute of Electrical and Electronics Engineers Inc.

VxWorks is a registered trademark of Wind River Systems, Inc.

Chapter 2

Functional Description

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2. Functional Description

This chapter presents more detailed, board level information about the CP620-PM Peripheral Master whereby the board components and their basic functionality are discussed in general.

2.1 General Information about the CP620-PM

The CP620-PM is comprised basically of the following:

- CPU
  - PowerPC G3 (IBM PPC750CXE)
- PCI-Bridge/Memory Controller
  - Motorola MPC107
- Memory
  - System Memory (SDRAM)
  - FLASH
  - FLASH Socket / SRAM Socket
  - FLASH expansion (CompactFlash)
  - Serial EEPROM’s
- Interfaces
  - CompactPCI Interface including rear I/O
  - Ethernet Interfaces
  - Serial Interfaces
  - PCI Expansion (PMC)
  - JTAG/COP - Debug interface
- Monitor and Control
  - System Logic
  - Push Buttons / LED’s
  - Watchdog
  - RTC
  - Temperature Sensor
- HotSwap Circuitry
- IPMI
- JTAG/COP - Debug Interface
- Software

2.2 CPU

The heart of the CP620 is the IBM PPC750CX/CXE, a PowerPC of the "Generation 3" hardware architecture. It combines a powerful processing unit, floating point unit and a 256 kB level 2 cache in one package and this with very low power consumption.

2.2.1 IBM PPC750CX/CXE Key Features

This section summarizes the features of the PPC750CXe's implementation of the PowerPC architecture. Major features of the PPC750CXe are as follows.

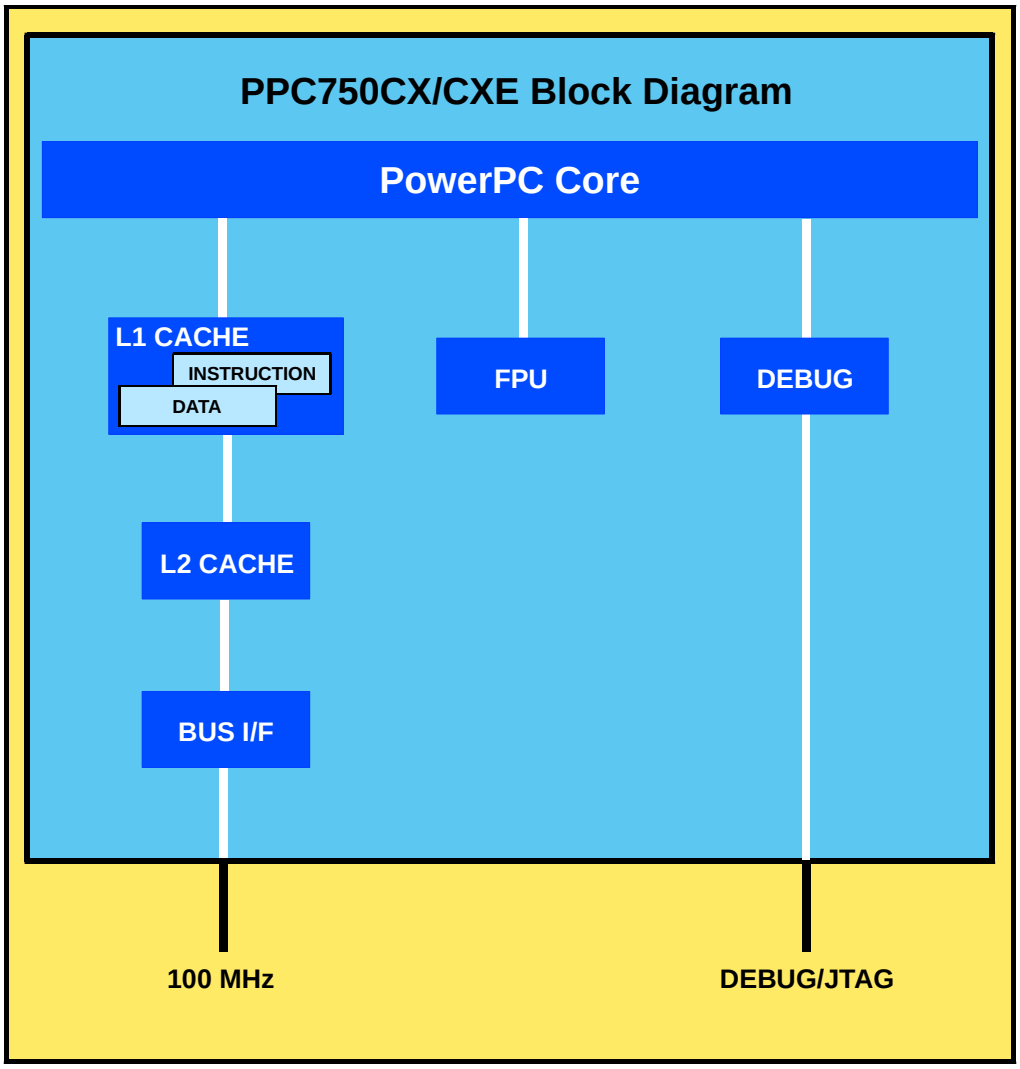
- G3 PowerPC core
  - Branch processing unit
  - Dispatch unit
  - Decode
  - Load/store unit
  - Fixed-point units
- Floating-point unit
  - Support for IEEE-754 standard single and double precision floating-point arithmetic
  - Optimized for single-precision multiply/add
  - Thirty-two floating point registers, 64-bit wide
  - Enhanced reciprocal estimates
  - 3-cycle latency, 1-cycle throughput, single-precision multiply-add
  - 3-cycle latency, 1-cycle throughput, double-precision add
  - 4-cycle latency, 2-cycle throughput, double-precision multiply-add
  - Hardware support for division
  - Hardware support for denormalized numbers
  - Time deterministic non-IEEE mode
- L1 Cache structure
  - 32K, 32-byte line, 8-way set associative instruction cache
  - 32K, 32-byte line, 8-way set associative data cache
  - Single-cycle cache access
  - Pseudo-LRU replacement
  - Copy-back or write-through data cache (on a page per page basis)
  - 3-state (MEI) memory coherency
  - Hardware support for data coherency
  - Non-blocking instruction and data cache (one outstanding miss under hits)
  - No snooping of instruction cache

- Memory management unit
  - 128 entry, 2-way set associative instruction TLB
  - 128 entry, 2-way set associative data TLB
  - Hardware reload for TLB's
  - 4 instruction BAT’s and 4 data BAT’s
  - Virtual memory support for up to 4 exabytes (2^{52}) virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
  - Support for big/little-endian addressing
- Level 2 (L2) cache
  - Internal L2 cache controller and 4K-entry tags; 256K data SRAM’s
  - Copy-back or write-through data cache on a page basis, or for all L2
  - 64-byte sectored line size
  - L2 frequency at core speed
  - On-board ECC
- Bus interface
  - Compatible with 60X processor interface
  - 32-bit address bus
  - 64-bit data bus
- Testability
  - Powerful diagnostic and test interface through Common On-Chip Processor (COP) and IEEE 1149.1 (JTAG) interface

2.2.2 The Principal Functional Blocks of the IBM PPC750CX/CXE

The diagram below illustrates the principal functional blocks of the IBM PPC750CX/CXE chip.

Figure 2-1: Overview of the Main Elements of the IBM PPC750CX/CXE



2.3 PCI-Bridge/Memory Controller

The PCI-Bridge/Memory Controller (also named Northbridge) is used to interface the CPU to memory and a larger number of peripheral busses. On the CP620-PM, the Motorola MPC107 is used.

The principal features of the MPC107 are used on the CP620-PM as follows:

- Processor interface
  - 60x compliant bus interface
  - 32-bit address bus, 64-bit data bus supported at 100 MHz
- Memory interface
  - 64-bit 100 MHz bus
  - support of PC100 SDRAM
  - Supports one to four banks 64-, 128- or 256 Mbit SDRAM devices
  - Supports 128 MB to 1 GB SDRAM memory
  - ROM interface, 8 and 16-bits in use
  - Supports ECC
  - Low-voltage TTL logic (LVTTL) interfaces
  - Port X: 8-, 32-bit genera purpose I/O port using ROM controller interface with programmable address strobe timing
- 32-bit PCI interface operating at 33 MHz
  - PCI 2.1-compliant
  - PCI 5.0-V tolerance
  - Support for accesses to PCI memory, I/O, and configuration spaces
  - PCI bus arbitration unit (five request/grant pairs)
  - Address translation unit
- Two channel integrated DMA controller (writes to ROM/Port X not supported)
  - Local-to-local memory
  - PCI-to-PCI memory
  - PCI-to-local memory
  - PCI memory-to-local memory
- I2C controller with full master/slave support (except broadcast all)
- Embedded programmable interrupt controller (EPIC)
  - 16 serial interrupts
  - Four programmable timers
- Dynamic power management - supports 60x nap, doze, sleep, and suspend modes

2.3.1 System Memory (SDRAM)

The main memory of the CP620-PM consists of four memory banks, equipped with 64 Mbit/128 Mbit or 256 Mbit SDRAM chips (8-bit width), soldered onto the board. This results in a minimum memory size of 128 MB if 2 Banks are equipped with 64 Mbit chips. The maximum possible Memory is 1 GB. The SDRAM is soldered onto the board for mechanical stability. It provides ECC support for data critical applications.

2.3.2 Flash (Onboard Soldered)

Four or eight megabyte of soldered Flash memory accommodates the bootstrap loader software and can be used to store a ROMable operating system and user data. This Flash memory is 8-bit wide and windowed with window sizes of 512 kB.

2.3.3 FLASH Socket / SRAM Socket

The CP620-PM provides one 32-pin DIL socket on which to place Flash, SRAM, non-volatile SRAM, or other DIL600 devices on the board. Access to this memory is controlled by the onboard logic.

The following devices may be added to the CP620-PM via the 32-pin DIL600 socket:

- standard EPROM devices;
- standard Flash memory of up to 512 kB (e.g. the AMD29F010 and AMD29F040);
- the NV SRAM from Dallas Semiconductor.
- These devices are available in the temperature range -40°C to +85°C for the industrial environment and guarantee a minimum data retention of 10 years (e.g. DS1250Y-100).

2.3.4 Flash Expansion

The CP620-PM provides a CompactFlash Type II interface which is placed below the upper PMC slot. Its electrical interface (3.3V IDE mode) is provided by the system logic.

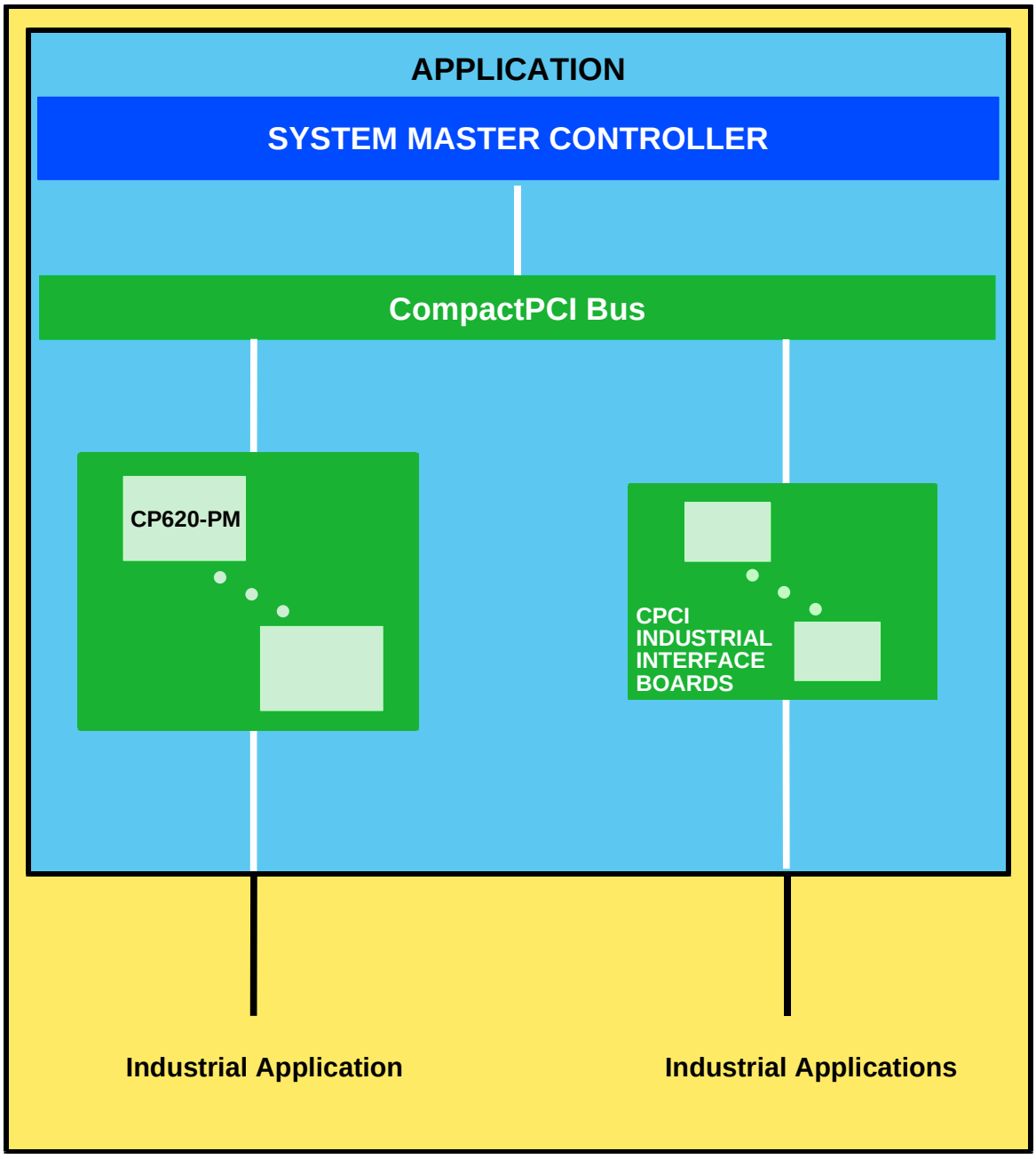
2.3.5 Serial EEPROM

Two 64-kbit serial EEPROM’s are provided, organized as 8192 x 8-bit. One EEPROM is for system purposes; the other is available to the user. Both EEPROM’s may be write protected. These EEPROM’s are connected to the I2C bus provided by the MPC107.

2.4 System Level Interfacing

The following illustration shows the system level dependencies of a complete CPCI system. The control of the boards on the CPCI bus is maintained by a system master CPU board. Other boards within the system may be either peripheral master CPU boards or simple I/O boards (for example, mass storage devices, field buses etc.)

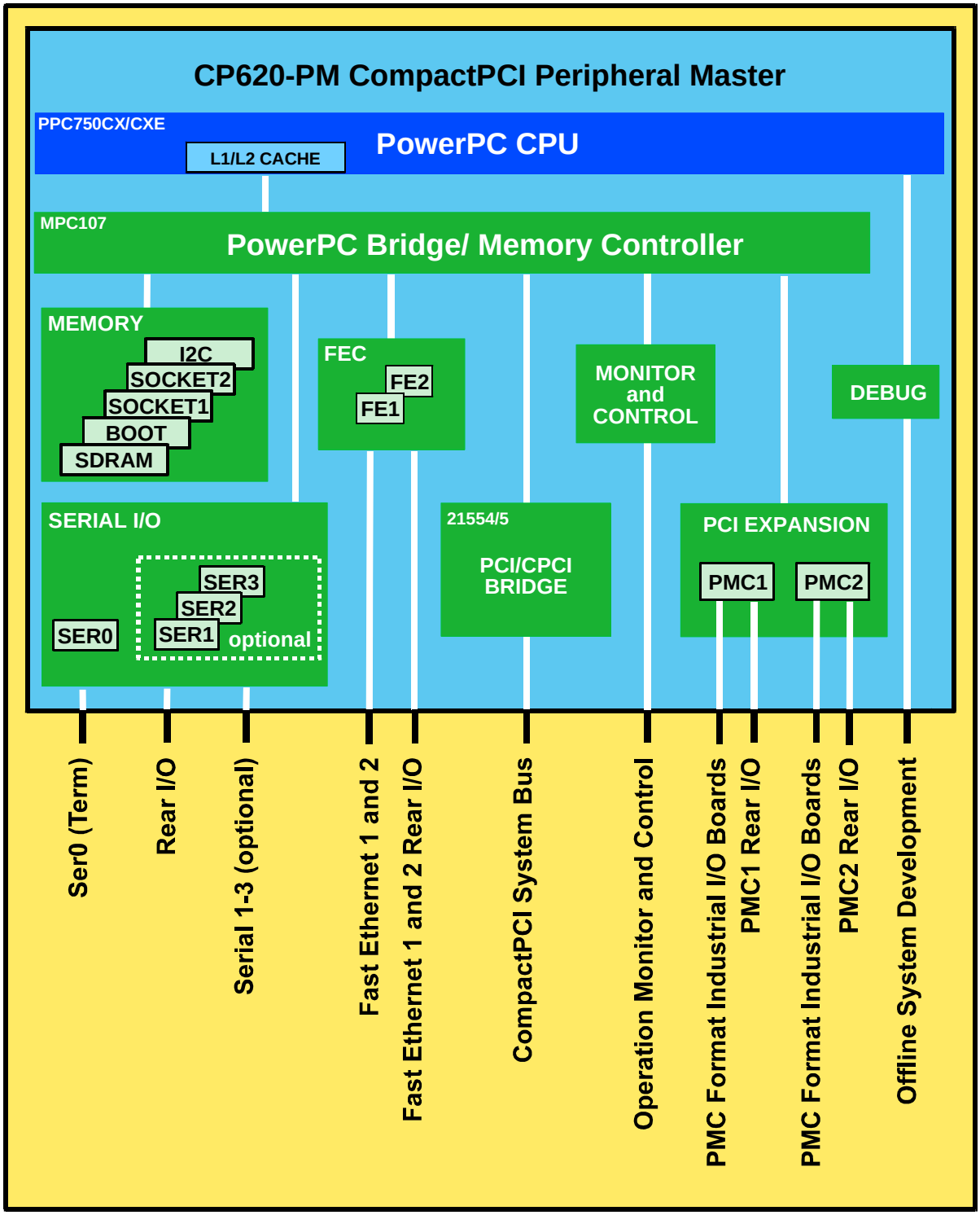
Figure 2-2: System Level Interfacing



2.5 Board Level Interfacing

The following illustration shows all the possible application interfaces of the CP620-PM.

Figure 2-3: Board Level Interfacing



2.6 System Interfaces

2.6.1 CompactPCI Interface including Rear I/O

2.6.1.1 Non-transparent PCI-to-PCI Bridge

The CP620-PM interfaces with the CompactPCI bus using the 21554/21555 bridge from Intel. This “non-transparent” PCI-to-PCI bridge makes it possible to isolate two PCI bus segments. The 21554/21555 PCI-to-PCI bridge is fully compliant with the PCI Local Bus Specification Rev. 2.1.

The 21554/21555 is specifically designed to bridge between two processor domains. The processor domain on the primary interface of the 21554/21555 is referred to as the host domain, this interface resides on the CompactPCI connector. The secondary bus interfaces, referred to as the local domain, reside on all onboard PCI devices.

The 21554/21555 bridge maps the entire CP620-PM subsystem as a single virtual device. The 21554/21555 PCI-to-PCI bridge is designed to allow configuration and addressing isolation, so that the local processor can effectively control the subsystem.

Key features of the Intel 21554/21555 bridge:

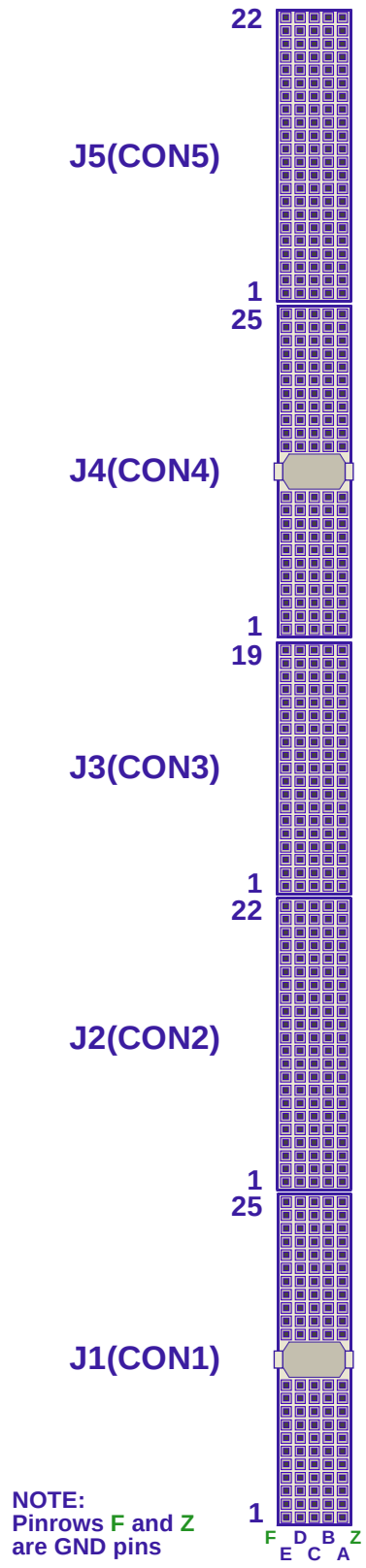
- optimized for multiprocessor application
- supports asynchronous PCI clock (primary and secondary interface)
- address translation between the two domains (host and slave)
- full 64-bit 33 MHz PCI interface
- I2O support
- Hotswap status and control register

Note...

The CP620-PM has been designed for use in a peripheral slot only; it is not intended for use in the system slot.

2.6.2 CompactPCI Bus Interface

Figure 2-4: CompactPCI Connectors CON1-CON5



2.6.2.1 CompactPCI Connector Overview

The complete CompactPCI connector configuration comprises five connectors named J1 to J5. Their functions are as follows:

- J1/J2: 64-bit CompactPCI interface with PCI bus signals, arbitration, clock and power.
- J3 and J5 have rear I/O interface functionality.
- the optional J4 connector has rear I/O interface functionality.

The CP620-PM is designed for a CompactPCI bus architecture. The CompactPCI standard is electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

The CP620-PM is hotswappable, which means it may be installed in and removed from a hotswap compliant backplane while the system is powered-up and running. The board may also be used in a standard CompactPCI system without hotswap support.

2.6.2.2 CompactPCI Connector Keying

CompactPCI connectors support guide lugs to ensure a correct polarized mating. A proper mating is further assured by the use of color coded keys for 3.3V and 5V operation.

Color coded keys prevent inadvertent installation of a 5V peripheral board into a 3.3V slot. The CP620-PM hotswap board is a 5V version. Backplane connectors are always keyed according to the signaling (VIO) level. Coding key colors are defined as follows:

Table 2-1: Coding Key Colors

Signaling Voltage	Key Color
3.3V	Cadmium Yellow
5V	Brilliant Blue
Universal board (5V and 3.3V)	None

CompactPCI connector pinouts appear on the following pages

2.6.2.3 CompactPCI Connectors CON1 and CON2 Pinouts

The CP620-PM interfaces with the PCI bus using two 2 mm x 2 mm pitch female CompactPCI bus connectors, J1 and J2.

Table 2-2: CompactPCI Bus Connector CON1 Pinout

Pin #	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	V(I/O) 2)	AD[0]	ACK64#	GND
23	GND	3.3V	AD[4]	AD[3]	5V 2)	AD[2]	GND
22	GND	AD[7]	GND	3.3V 2)	AD[6]	AD[5]	GND
21	GND	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	GND	3.3V	AD[15]	AD[14]	GND 2)	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	GND	3.3V	IPMB SCL	IPMB SDA	GND 2)	PERR#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	GND	3.3V	FRAME#	IRDY#	BD SEL# 1)	TRDY#	GND
12-14	Key Area						
11	GND	AD[18]	AD[17]	AD[16]	GND 2)	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	GND	C/BE[3]#	IDSEL 1)	AD[23]	GND 2)	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	GND	AD[30]	AD[29]	AD[28]	GND 2)	AD[27]	GND
6	GND	REQ#	GND	3.3V 2)	CLK	AD[31]	GND
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND 2)	GNT#	GND
4	GND	IPMB PWR	HEALTHY#	V(I/O) 2)	NC	NC	GND
3	GND	INTA#	INTB#	INTC#	5V 2)	INTD#	GND
2	GND	NC	5V	NC	NC	NC	GND
1	GND	5V	-12V	NC	+12V	5V	GND

Legend:

1)	Short pins on front side of backplane
2)	Long pins on front side of backplane

Table 2-3: CompactPCI Bus Connector CON2 Pinout

Pin #	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	NC	NC	NC	NC	NC	GND
20	GND	NC	NC	NC	GND	NC	GND
19	GND	NC	NC	IPMI_SDA	IPMI_SCL	IPMI_ALERT	GND
18	GND	NC	NC	NC	GND	NC	GND
17	GND	NC	GND	NC	NC	NC	GND
16	GND	NC	NC	NC	GND	NC	GND
15	GND	NC	GND	NC	NC	NC	GND
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	GND	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	GND	C/BE[5]	64EN#	V(I/O)	C/BE[4]#	PAR64	GND
4	GND	V(I/O)	NC	C/BE[7]#	GND	C/BE[6]#	GND
3	GND	NC	GND	NC	NC	NC	GND
2	GND	NC	NC	SYSEN	NC	NC	GND
1	GND	NC	GND	NC	NC	NC	GND

2.6.2.4 CompactPCI Rear I/O Connectors CON3-CON5 Pinouts

The CP620-PM provides all I/O signals through the rear I/O connectors J3, J4 and J5.

When the rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus the rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the rear I/O feature a special backplane is necessary. The CP620-PM with rear I/O is compatible with all standard 6U CompactPCI passive backplanes with rear I/O support

Table 2-4: Rear I/O Connector J3 (CON3) Pin Definitions

Pin	Row A	Row B	Row C	Row D	Row E	Row F
19	NC	minus 12V	RS485_ECHO	plus 12V	RearBatt	GND
18	LPa_DA+	LPa_DA-	GND	NC	NC	GND
17	LPa_DB+	LPa_DB-	GND	NC	NC	GND
16	LPb_DA+	LPb_DA-	GND	NC	NC	GND
15	LPb_DB+	LPb_DB-	GND	NC	NC	GND
14	3.3V	3.3V	3.3V	VCC	VCC	GND
13	PMC1IO5	PMC1IO4	PMC1IO3	PMC1IO2	PMC1IO1	GND
12	PMC1IO10	PMC1IO9	PMC1IO8	PMC1IO7	PMC1IO6	GND
11	PMC1IO15	PMC1IO14	PMC1IO13	PMC1IO12	PMC1IO11	GND
10	PMC1IO20	PMC1IO19	PMC1IO18	PMC1IO17	PMC1IO16	GND
9	PMC1IO25	PMC1IO24	PMC1IO23	PMC1IO22	PMC1IO21	GND
8	PMC1IO30	PMC1IO29	PMC1IO28	PMC1IO27	PMC1IO26	GND
7	PMC1IO35	PMC1IO34	PMC1IO33	PMC1IO32	PMC1IO31	GND
6	PMC1IO40	PMC1IO39	PMC1IO38	PMC1IO37	PMC1IO36	GND
5	PMC1IO45	PMC1IO44	PMC1IO43	PMC1IO42	PMC1IO41	GND
4	PMC1IO50	PMC1IO49	PMC1IO48	PMC1IO47	PMC1IO46	GND
3	PMC1IO55	PMC1IO54	PMC1IO53	PMC1IO52	PMC1IO51	GND
2	PMC1IO60	PMC1IO59	PMC1IO58	PMC1IO57	PMC1IO56	GND
1	V(I/O)	PMC1IO64	PMC1IO63	PMC1IO62	PMC1IO61	GND

The legend for this table appears on the following page

Legend for Rear I/O Connector J3 (CON3) Table

Table 2-5: Backplane J3 Signal Functions

Signal	Function
PMC1 Rear I/O	
PMC1IO1 - PMC1IO64	Rear I/O signals for 1st PMC slot
Ethernet 1	
LPa_DA+/LPa_DA-	Ethernet 1 transmit signals
LPa_DB+/LPa_DB-	Ethernet 1 receive signals
Ethernet 2	
LPb_DA+/LPb_DA-	Ethernet 2 transmit signals
LPb_DB+/LPb_DB-	Ethernet 2 receive signals
Others	
P3RST	Reset input from rear I/O module
Minus 12V	-12V path to rear I/O module
Plus 12V	+12V path to rear I/O module
RearBatt	Battery input from battery on rear I/O module

Note...

An asterisk (*) means that all signals in this signal category may be used.

Table 2-6: Backplane J4 Pin Definitions

Pin	Row A	Row B	Row C	Row D	Row E	Row F
25	VCC	NC	JPO	3.3V	VCC	GND
24	NC	NC	NC	NC	NC	GND
23	3.3V	NC	JP1	VCC	NC	GND
22	NC	NC	NC	NC	NC	GND
21	3.3V	NC	JP2	NC	J2ALERT	GND
20	NC	NC	NC	J2SCL	J2SDA	GND
19	3.3V	NC	NC	NC	IPMIGPIO2	GND
18	NC	NC	NC	PWM1	PWM0	GND
17	3.3V	IPMI_3.3V	SPLED1	NC	Tach_IN3	GND
16	NC	NC	NC	Tach_IN2	Tach_IN1	GND
15	3.3V	IPMI_3.3V	ACLED1	NC	Tach_IN0	GND
14	Key	Key	Key	Key	Key	Key
13	Key	Key	Key	Key	Key	Key
12	Key	Key	Key	Key	Key	Key
11	NC	IPMI_VCC	LILED1	NC	CONN_ID_DRV	GND
10	NC	NC	NC	ID_XMIT_EN	CONN_ID1	GND
9	NC	IPMI_VCC	SPLED2	NC	CONN_ID0	GND
8	NC	GND	NC	XMIT_EN	UART0_RI	GND
7	GND	NC	ACLED2	NC	UART0_RTS	GND
6	NC	NC	NC	UART0_DCD	UART0_CTS	GND
5	GND	GND	LILED2	UART0_DOUT	UART0_DIN	GND
4	NC	GND	NC	GND	GND	GND
3	NC	NC	GND	NC	LED1	GND
2	NC	NC	GND	NC	LED2	GND
1	VCC	minus 12V	GND	pos 12V	VCC	GND

Legend:

Yellow table cells IPMI signals

Table 2-7: Backplane J5 Pin Definitions

Pin	Row A	Row B	Row C	Row D	Row E	Row F
22	PMC2IO5	PMC2IO4	PMC2IO3	PMC2IO2	PMC2IO1	GND
21	PMC2IO10	PMC2IO9	PMC2IO8	PMC2IO7	PMC2IO6	GND
20	PMC2IO15	PMC2IO14	PMC2IO13	PMC2IO12	PMC2IO11	GND
19	PMC2IO20	PMC2IO19	PMC2IO18	PMC2IO17	PMC2IO16	GND
18	PMC2IO25	PMC2IO24	PMC2IO23	PMC2IO22	PMC2IO21	GND
17	PMC2IO30	PMC2IO29	PMC2IO28	PMC2IO27	PMC2IO26	GND
16	PMC2IO35	PMC2IO34	PMC2IO33	PMC2IO32	PMC2IO31	GND
15	PMC2IO40	PMC2IO39	PMC2IO38	PMC2IO37	PMC2IO36	GND
14	PMC2IO45	PMC2IO44	PMC2IO43	PMC2IO42	PMC2IO41	GND
13	PMC2IO50	PMC2IO49	PMC2IO48	PMC2IO47	PMC2IO46	GND
12	PMC2IO55	PMC2IO54	PMC2IO53	PMC2IO52	PMC2IO51	GND
11	PMC2IO60	PMC2IO59	PMC2IO58	PMC2IO57	PMC2IO56	GND
10	Board-V(I/O)	PMC2IO64	PMC2IO63	PMC2IO62	PMC2IO61	GND
9	Eth-TDN2	Eth-RDN2	S1RXD	Eth-TDN1	Eth-RDN1	GND
8	Eth-TNP2	Eth-RDP2	S1TXD	Eth-TDP1	Eth-RDP1	GND
7	RS232_2	RS232_1	S1RTS	S3RIN	3.3V	GND
6	S1DTR	S1CTS	S1DSR	S1DCD	S1RIN	GND
5	S2RXD	S2TXD	S2RTS	S2DTR	S3TXD	GND
4	S2DSR	S2DCD	S2RIN	S2CTS	S3RXD	GND
3	S4DTR	S4CTS	S4DSR	GPLED	S3DTR	GND
2	S4RTS	S4RIN	S4RXD	S3DSR	S3DCD	GND
1	S4DCD	P3RST	S4TXD	S3CTS	S3RTS	GND

The legend for this table appears on the following page

Legend for Backplane J5 Table

Table 2-8: Backplane J5 Signal Functions

Signal	Function
PMC2 Rear I/O	
PMC2IO1 - PMC2IO64	Rear I/O signals for 2nd PMC slot
Ethernet 1	
Eth-TDP1	Ethernet high transmit Data line
Eth-TDN1	Ethernet low transmit Data line
Eth-RDP1	Ethernet high receive Data line
Eth-RDN1	Ethernet low receive Data line
Ethernet 2	
Eth-TDP2	Ethernet high transmit Data line
Eth-TDN2	Ethernet low transmit Data line
Eth-RDP2	Ethernet high receive Data line
Eth-RDN2	Ethernet low receive Data line
Serial Port 1	
S1*	Serial port signals; TTL level
Serial Port 2	
S2*	Serial port signals; TTL level
Serial Port 3	
S3*	Serial port signals; TTL level
Serial Port 4	
S4*	Serial port signals; TTL level

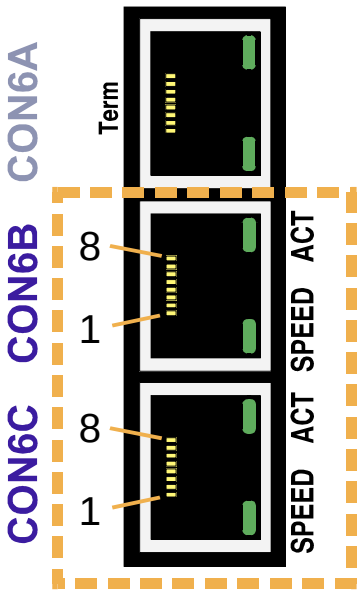
Note...

An asterisk (*) means that all signals in this signal category may be used.

2.6.3 Fast Ethernet

The CP620-PM board includes two 10BASE-T/100BASE-TX ethernet ports based on the Intel® 82559ER Fast Ethernet PCI Bus Controller. The controller contains two receive and transmit FIFO buffers that prevent data overruns or underruns while waiting for access to the PCI bus.

Figure 2-5: Ethernet/Fast Ethernet Connector



The Ethernet connectors are realized as RJ45 twisted-pair connectors. The interfaces provide automatic detection and switching between 10Base-T and 100Base-TX data transmission. The two Ethernet channels may be configured via the Bootstrap Loader setting or the rear I/O configuration register for front I/O or rear I/O. The standard software configuration is front I/O.

Note...

The CP620-PM versions which are compliant with PICMG 2.16 provide the Ethernet interfaces only on the rear I/O connector J3/P3. The Ethernet connectors CON6B and CON6C must, therefore, not be connected. A protective dummy plug is provided which should protect the user from incorrect usage; please do not remove this plug.

2.6.3.1 RJ45 Connectors CON8 and CON9 Pinouts

The CON8 and CON9 connectors supply the 10Base-TX/100Base-TX interfaces to the Ethernet controller.

Table 2-9: RJ45 Connectors CON8 and CON9 Pinouts

RJ45	Signal	Function
1	TX+	Transmit +
2	TX-	Transmit -
3	RX+	Receive +
4	NC	--
5	NC	--
6	RX-	Receive -
7	NC	--
8	NC	--

2.6.3.2 Ethernet LED Status

The two green LED's located within the ethernet connectors have the following functions:

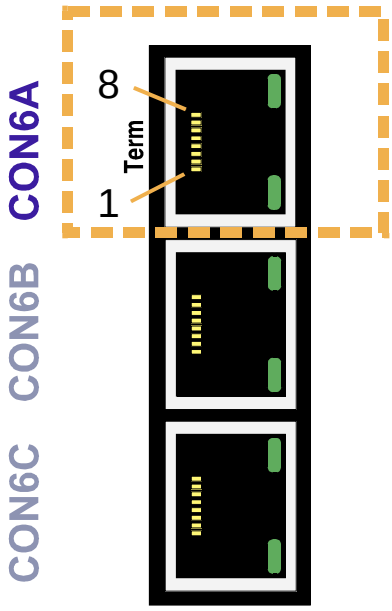
ACT: This LED monitors network connection and activity. The LED lights up when network packets are sent or received through the RJ45 port. When this LED is not lit it means that either the computer is not sending or receiving network data or that the cable connection is faulty.

SPEED: This LED lights up to indicate a successful 100Base-TX connection. When not lit the connection is operating at 10Base-T.

2.6.4 Serial Interfaces

The CP620-PM provides up to four 16550 compliant serial interfaces. These interfaces are realized by two dual-UARTS from EXAR, the 16C2850, which also provide half-duplex control for RS-485 interfacing. One part of each UART pair provides 128 Bytes transmit buffer and 128 Bytes receive buffer per channel and so it reduces the bandwidth requirements of the CPU. It has independent transmit and receive UART control signals and four selectable receive FIFO interrupt trigger levels. The UART's provide support for various character lengths (5,6,7,8) with even or odd or no parity.

Figure 2-6: Serial Connector



The four serial interfaces on the CP620-PM can be divided into 3 groups:

Group 1 (serial interface 1): This interface is available with RS-232 levels (TERM) on the front panel or with TTL levels on the rear I/O connector J5. The direction of this interface can be programmed via the register-setting in the
interface route register. Additionally, the interface will be routed to the front panel if the jumper J1 is set (highest priority). The default configuration is front I/O

Group 2 (serial interface 2): This interface is available with TTL levels on the REAR-IO connector. A special board variant (1 PMC version) also provides this interface with RS-232-levels on the front panel. The direction of this interface can be programmed via the register-setting within the interface route register. The default setting is disabled.

Group 3 (serial interfaces 3 and 4): These interfaces are available with TTL level on the rear I/O connectors. A special board variant (1 PMC version) also provides these interfaces as RS-232 interfaces or RS-485/RS-422 interfaces on the front panel. The direction and type of interface can be programmed via the register setting in the interface route register.

RS-422 configuration:

The RS-422 interface use two differential data pairs RX and TX for communication (Full-Duplex)

RS-485 configuration:

The RS-485 interface uses one differential data pair. It differs from the RS-422 mode in that it provides the ability to transmit and receive over the same wire. The RTS signal is used to distinguish between receiving and sending data.

2.6.4.1 Serial interface 1 Pinout (TERM)

Table 2-10: CON8 RJ45 Connector Pinout

Pin Number	Signal
1	DSR
2	RTS
3	GND
4	TXD
5	RXD
6	DCD
7	CTS
8	DTR

2.6.4.2 Serial Interfaces 2, 3 and 4 Pinout

Table 2-11: Optional CON9*, CON10, CON11 (RJ45 Connector) Pinout

Pin Number	RS-232 Signals	RS-485 Half-Duplex	RS-422 Full-Duplex
1	DSR	NC	-RxD
2	RTS	NC	NC
3	GND	GND	GND
4	TXD	+TRXD	-TxD
5	RXD	NC	NC
6	DCD	NC	+RxD
7	CTS	-TRXD	+TxD
8	DTR	NC	NC

Note...

CON9* carries only the RS-232 signals.

If these interfaces are connected via rear I/O, the RS-232 or RS-485 transceivers must be realized on the rear I/O board.

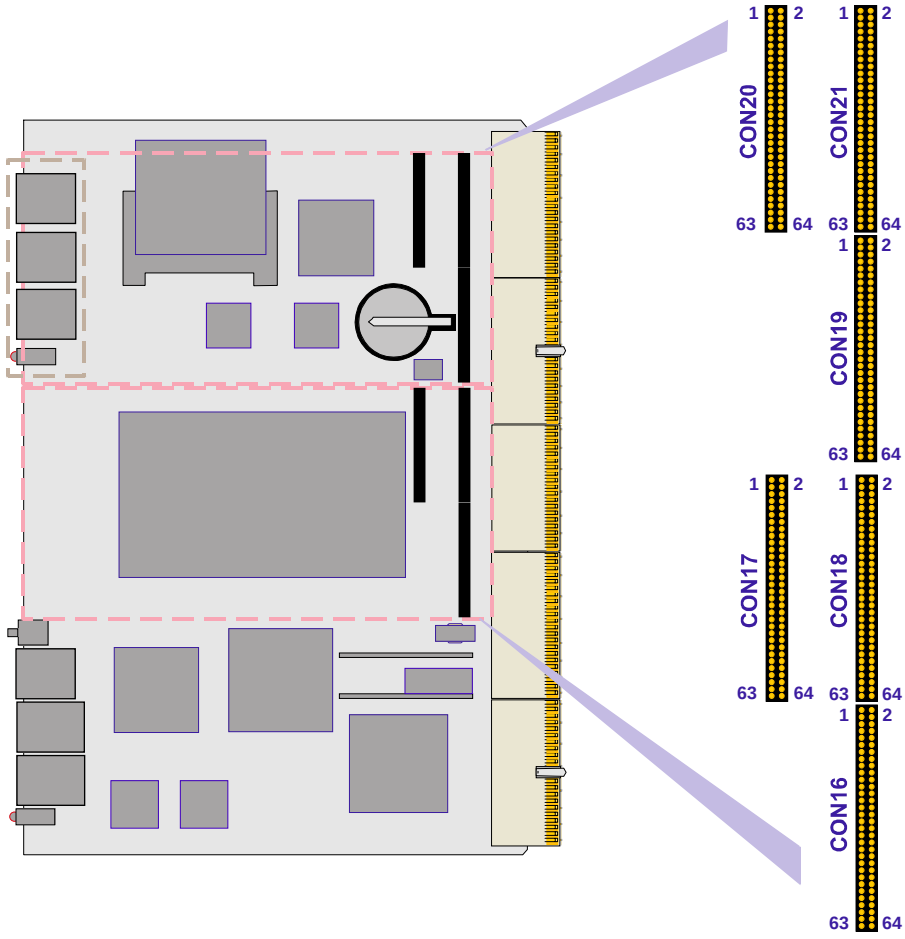
The RS-485 interfaces on the front panel or not galvanically isolated.

2.6.5 PMC Interfaces

For flexible and easy configuration two onboard PMC sockets are available. The connectors CON17, CON20 (Jn1/Pn1) and CON18, CON21 (Jn2/Pn2) provide the signals for the 32-bit PCI bus. The 64-bit interface for the PMC interface is not implemented. User defined I/O signals are supported and are connected to the CompactPCI rear I/O connectors J3 and J5.

This interface has been designed to comply with the IEEEP1386.1 specification which defines a PCI electrical interface for the CMC (Common Mezzanine Card) form factor. The CP620-PM provides for either a 5V or 3.3V PMC PCI signaling environment.

Figure 2-7: PMC Connectors CON16, 17 and 18 and CON19, 20 and 21



Note...

The PMC rear I/O signals from CON16 are routed to CompactPCI connector J3 (CON3), whose pinout is provided in Table 2-4.

The PMC rear I/O signals from CON19 are routed to CompactPCI connector J5 (CON5), whose pinout is provided in Table 2-7.

2.6.5.1 PMC Connectors CON19 and CON21 Pinouts

Table 2-12: PMC Connectors CON19 and CON21 Pinouts

PN1/JN1 (CON17/CON20)				PN2/JN2 (CON18/CON21)			
Pin #	Signal Name	Signal Name	Pin #	Pin #	Signal Name	Signal Name	Pin #
1	Signal	-12V	2	1	+12V	Signal	2
3	Ground	Signal	4	3	Signal	Signal	4
5	Signal	Signal	6	5	Signal	Ground	6
7	BUSMODE1#	+5V	8	7	Ground	Signal	8
9	Signal	Signal	10	9	Signal	Signal	10
11	Ground	Signal	12	11	BUSMODE2#	+3.3V	12
13	Signal	Ground	14	13	Signal	BUSMODE3#	14
15	Ground	Signal	16	15	+3.3V	BUSMODE4#	16
17	Signal	+5V	18	17	Signal	Ground	18
19	V (I/O)	Signal	20	19	Signal	Signal	20
21	Signal	Signal	22	21	Ground	Signal	22
23	Signal	Ground	24	23	Signal	+3.3V	24
25	Ground	Signal	26	25	Signal	Signal	26
27	Signal	Signal	28	27	+3.3V	Signal	28
29	Signal	+5V	30	29	Signal	Ground	30
31	V (I/O)	Signal	32	31	Signal	Signal	32
33	Signal	Ground	34	33	Ground	Signal	34
35	Ground	Signal	36	35	Signal	+3.3V	36
37	Signal	+5V	38	37	Ground	Signal	38
39	Ground	Signal	40	39	Signal	Ground	40
41	Signal	Signal	42	41	+3.3V	Signal	42
43	Signal	Ground	44	43	Signal	Ground	44
45	V (I/O)	Signal	46	45	Signal	Signal	46
47	Signal	Signal	48	47	Ground	Signal	48
49	Signal	+5V	50	49	Signal	+3.3V	50
51	Ground	Signal	52	51	Signal	Signal	52
53	Signal	Signal	54	53	+3.3V	Signal	54
55	Signal	Ground	56	55	Signal	Ground	56
57	V (I/O)	Signal	58	57	Signal	Signal	58
59	Signal	Signal	60	59	Ground	Signal	60
61	Signal	+5V	62	61	Signal	+3.3V	62
63	Ground	Signal	64	63	Ground	Signal	64

Table 2-13: PMC Connectors CON19 and CON21 Pinouts

CON16 (PN4/JN4)				CON19 (PN4/JN4)			
Pin #	Signal Name	Signal Name	Pin #	Pin #	Signal Name	Signal Name	Pin #
1	PMC1IO1	PMC1IO2	2	1	PMC2IO1	PMC2IO2	2
3	PMC1IO3	PMC1IO4	4	3	PMC2IO3	PMC2IO4	4
5	PMC1IO5	PMC1IO6	6	5	PMC2IO5	PMC2IO6	6
7	PMC1IO7	PMC1IO8	8	7	PMC2IO7	PMC2IO8	8
9	PMC1IO9	PMC1IO10	10	9	PMC2IO9	PMC2IO10	10
11	PMC1IO11	PMC1IO12	12	11	PMC2IO11	PMC2IO12	12
13	PMC1IO13	PMC1IO14	14	13	PMC2IO13	PMC2IO14	14
15	PMC1IO15	PMC1IO16	16	15	PMC2IO15	PMC2IO16	16
17	PMC1IO17	PMC1IO18	18	17	PMC2IO17	PMC2IO18	18
19	PMC1IO19	PMC1IO20	20	19	PMC2IO19	PMC2IO20	20
21	PMC1IO21	PMC1IO22	22	21	PMC2IO21	PMC2IO22	22
23	PMC1IO23	PMC1IO24	24	23	PMC2IO23	PMC2IO24	24
25	PMC1IO25	PMC1IO26	26	25	PMC2IO25	PMC2IO26	26
27	PMC1IO27	PMC1IO28	28	27	PMC2IO27	PMC2IO28	28
29	PMC1IO29	PMC1IO30	30	29	PMC2IO29	PMC2IO30	30
31	PMC1IO31	PMC1IO32	32	31	PMC2IO31	PMC2IO32	32
33	PMC1IO33	PMC1IO34	34	33	PMC2IO33	PMC2IO34	34
35	PMC1IO35	PMC1IO36	36	35	PMC2IO35	PMC2IO36	36
37	PMC1IO37	PMC1IO38	38	37	PMC2IO37	PMC2IO38	38
39	PMC1IO39	PMC1IO40	40	39	PMC2IO39	PMC2IO40	40
41	PMC1IO40	PMC1IO42	42	41	PMC2IO41	PMC2IO42	42
43	PMC1IO43	PMC1IO44	44	43	PMC2IO43	PMC2IO44	44
45	PMC1IO45	PMC1IO46	46	45	PMC2IO45	PMC2IO46	46
47	PMC1IO47	PMC1IO48	48	47	PMC2IO47	PMC2IO48	48
49	PMC1IO49	PMC1IO50	50	49	PMC2IO49	PMC2IO50	50
51	PMC1IO51	PMC1IO52	52	51	PMC2IO51	PMC2IO52	52
53	PMC1IO53	PMC1IO54	54	53	PMC2IO53	PMC2IO54	54
55	PMC1IO55	PMC1IO56	56	55	PMC2IO55	PMC2IO56	56
57	PMC1IO57	PMC1IO58	58	57	PMC2IO57	PMC2IO58	58
59	PMC1IO59	PMC1IO60	60	59	PMC2IO59	PMC2IO60	60
61	PMC1IO61	PMC1IO62	62	61	PMC2IO61	PMC2IO62	62
63	PMC1IO63	PMC1IO64	64	63	PMC2IO63	PMC2IO64	64

2.6.6 CompactFlash

To enable highly flexible flash extension a CompactFlash (CF) type II socket is available.

CF is a very small removable mass storage device. It provides IDE functionality compatible with the 16-bit ATA/ATAPI-4 interface. CF cards are also available for data storage using the Microdrive harddisk from IBM with up to 1 GB capacity.

The board supports both CF types (type I and type II). The only difference between CF type I and CF type II cards is the card thickness. CF type I is 3.3 mm thick and CF type II cards are 5 mm thick. A CF type I card will operate in a CF type I or CF type II slot. A CF type II card will only fit in a CF type II slot. The electrical interfaces are identical. CompactFlash is available in both CF type I and CF type II cards. The IBM Microdrive is a CF type II card.

Table 2-14: CompactFlash Connector Pinout

Number	Signal Name	Signal Name	Number
1	GND	NC (CD1)	26
2	D03	D11	27
3	D04	D12	28
4	D05	D13	29
5	D06	D14	30
6	D07	D15	31
7	IDE_CS0	IDE_CS1	32
8	GND (A10)	NC (VS1)	33
9	GND (ATASEL)	DIOR	34
10	GND (A09)	DIOW	35
11	GND (A08)	WE	36
12	GND (A07)	INTRQ	37
13	VCC	VCC	38
14	GND (A06)	CSEL	39
15	GND (A05)	NC (VS2)	40
16	GND (A04)	Reset	41
17	GND (A03)	IORDY	42
18	A02	INPACK	43
19	A01	VCC	44
20	A00	NC (ACTIVE)	45
21	D00	PDIAG	46
22	D01	D08	47
23	D02	D09	48
24	NC (IOCS16)	D10	49
25	NC (CD2)	GND	50

2.6.7 Test and Program Development

2.6.7.1 DEBUG Interface and Pinout

A JTAG/COP interface is provided on the CP620-PM for software debugging. The CPU can accessed using an emulator probe via CON13. It provides all the signals required for control of the CPU via the common on-chip processor (COP).

Figure 2-8: DEBUG Connector CON13

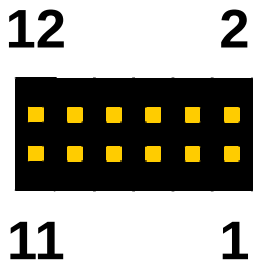


Table 2-15: DEBUG Connector CON13 Pinout

SIGNAL	PIN	I/O	DESCRIPTION
TDI	1	O	Input serial data
TDO	2	I	Output serial data
CKSTP_IN	3	I	Checkstop in
TRST	4	I	Test reset
TMS	5	I	Command type
TCK	6	I	Debug clock
HRESET	7	I	Hard reset
SRESET	8	I	Soft reset
GND	9	O	Ground
CHKSTP	10	--	Checkstop out
+2.5V	11	--	+2.5V
NC	12	--	--

2.6.7.2 JTAG/ISP Interface and Pinout

CON15 provides JTAG/ISP signals for programming the system logic chips and is for factory use only. This interface utilizes a connector which is physically identical with the Debug interface.

Figure 2-9: JTAG Connector CON15

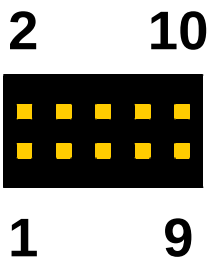


Table 2-16: JTAG Connector CON15 Pinout

SIGNAL	PIN	PIN	SIGNAL
TCK	1	2	GND
TDO	3	4	VCC
TMS	5	6	GND
OE_CLKS	7	8	N/C
TDI	9	10	GND

Note...

This connector is reserved for factory use only. The description of this connector is provided for information purposes.

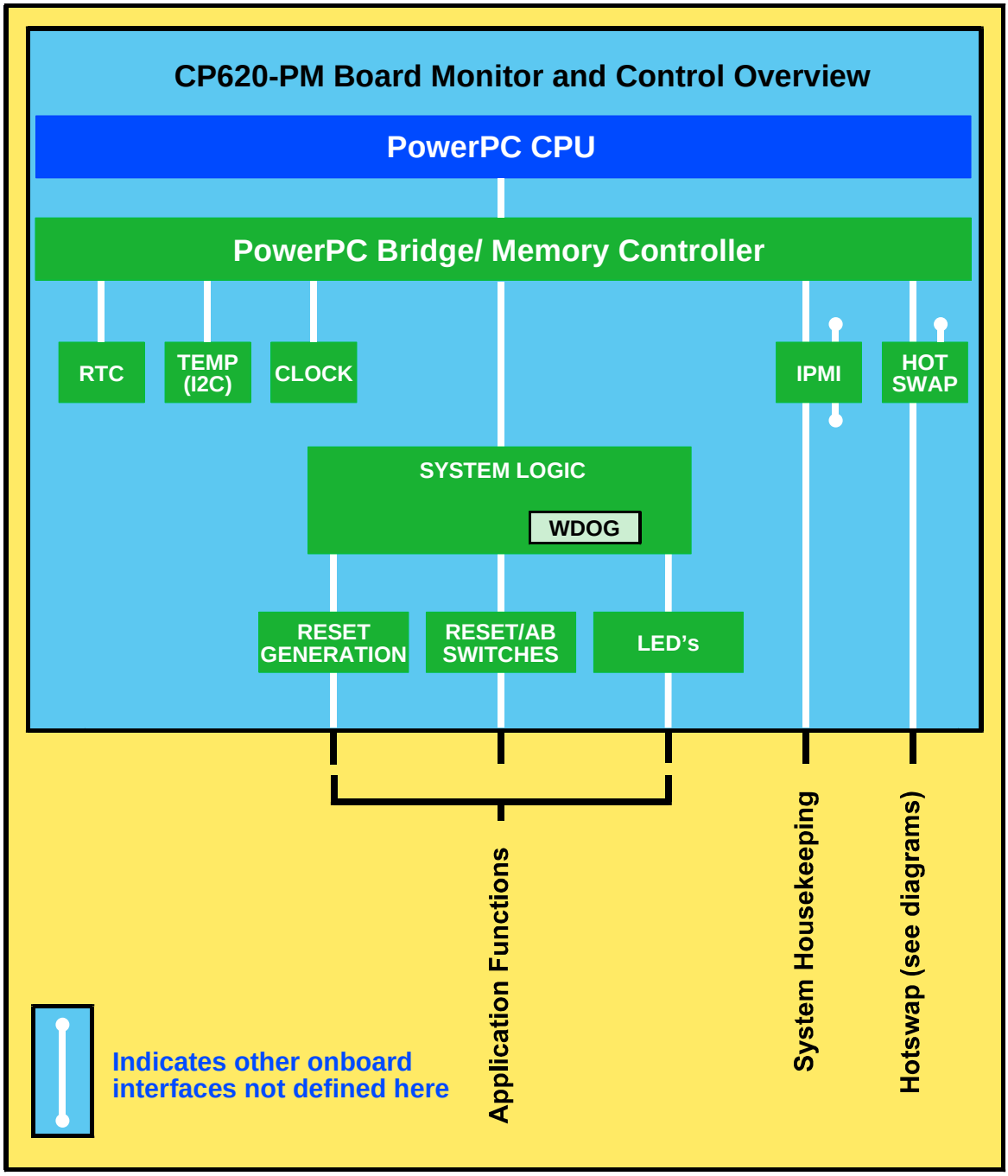
2.6.8 Non-System Relevant Connectors

CON12 is non-system relevant. It is used to connect the hotswap handle switch.

2.7 Monitor and Control (M/C)

Monitor and Control functions are divided essentially into pre-operation and operation. Pre-operation M/C deals with memory configuration aspects, board jumper configurations, and system requirements. Operation M/C covers direct operator interfaces, register handling, and the use of clocks, timers, and counters.

Figure 2-10: Monitor and Control Overview



2.7.1 Watchdog Timer

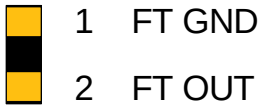
A watchdog timer is available which (when enabled) on timeout forces either a non-maskable interrupt (NMI) to be generated or causes a system reset to occur (refer to chapter 4 for configuration details). It is also possible to generate, as a first step, an NMI and then, as a second step, a system reset (in Cascade mode).The watchdog timing has four possible settings: 0.5, 1.0, 1.5, and 2.0 seconds. After selecting the timeout value and routing (NMI or reset) the watchdog can be enabled. Once enabled, the watchdog must be continuously retriggered or a timeout will occur. When the watchdog timer is enabled, it cannot be stopped or reprogrammed except by resetting the system. The yellow watchdog LED (W) indicates the enabling status of the watchdog. Prior to the watchdog being enabled it is off. After enabling it comes on and remains on until a system reset occurs.

2.7.2 Realtime Clock (STC M41T56)

A separate hardware realtime clock (RTC) is incorporated on the CP620-PM board which provides clock information via the I²C bus for application use. An eight byte wide register (refer to chapter 4 for description) is available for accessing, setting, and starting the RTC. The RTC must be initialized prior to its use whereby settings are possible for seconds, minutes, hours, day, date, month, year, and calibration information. Continuous clock operation (even with system power off) is possible through the use of a rechargable Gold Cap, or alternately, lithium battery buffering is possible. Accuracy of the RTC is 35 ppm whereby temperature compensation can be adjusted in steps of +4.068 or -2.034 ppm per software using the onboard digital temperatur sensor (LM75).

For calibration purposes the RTC can also generate a 512 Hz test signal which is made available at test jack J2 (figure 1-3 indicates the location of J2 on the board). Please refer to the datasheet of the ST M41T56 for more information concerning calibration.

Figure 2-11: RTC J2 Pinout



2.7.3 Reset/Abort

On the CP620-PM front panel there are two push button switches for interacting with the system: RST for reset and AB for abort.

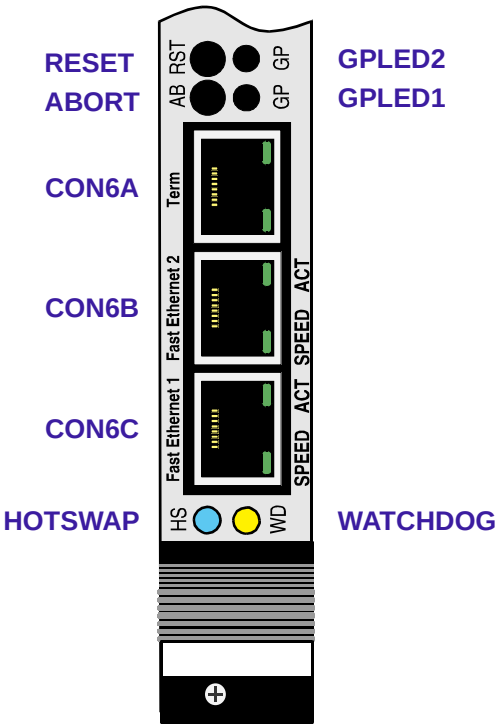
The RST button is routed directly to the power supervisor/reset controller chip. Pressing the RST button initiates an immediate hardware reset of the system.

During normal operation pressing the AB button causes a non-maskable interrupt (NMI) to be generated. In addition it is latched into a bit in the System Logic, in order to differentiate between NMI's initiated from the ABORT Button and NMI's initiated from the Watchdog Timer.

Pressing the AB button during system startup when the U LED (green) is blinking causes the bootstrap loader to enter interactive command mode. Commands can then be entered for processing by the bootstrap loader. Please refer to chapter 5 for Bootstrap Loader information.

The Buttons must be debounced.

Figure 2-12: Front Panel LED's and Push Buttons



2.7.4 System Status Indicators

The system status indicators aredivided into three groups. The first group (the LEDs beside the push buttons) are application oriented whereas the second group (the LEDs integrated within the Ethernet connectors) are dedicated to and controlled by the Ethernet interface. The third group has dedicated functions (hotswap and watchdog timer). The table below provides an overview of the functionality associated with these indicators.

Table 2-17:System Status Indicators

FP DES.	COLOR	NAME	DESCRIPTION
HS	BLUE	LED3B	Lit when safe to extract the board from backplane.
WD	YELLOW	LED3Y	Watchdog timer: indicates that the watchdog is active

2.7.5 Digital Temperature Sensor (LM75)

The digital temperature sensor (National Semiconductor LM75) installed on the CP620-PM measures the board temperature. Used as a thermal watchdog, the LM75 can generate a maskable interrupt which can be used by an application. In addition, the actual temperature can be read out of the LM75 via the I²C bus. This may be used, for example, to maintain the calibration of the onboard RTC over a wide operational temperature range. Please refer to chapter 4.6, Digital Temperature Sensor, LM75, for additional information.

2.8 Hotswap

2.8.1 Technical Background of CompactPCI Hotswap

In many modern application systems downtime is costly and/or unacceptable. Server applications, telecommunications networks and automated systems requiring continuous monitoring call for a system design in which a single card can be inserted or extracted without affecting the rest of the system. The ease with which a board may be removed and replaced is dependent on the mechanical design (form factor), the possibility of deactivating the software drivers for the board (operating system) and the possibility of removing and inserting the board without disturbing the signal quality on the bus.

CompactPCI hotswap is currently the most effective way to meet this need. Staggered pins on the backplane guarantee controlled power sequencing of the board, while the signals ENUM, BDSEL, HEALTHY and the hotswap control and status register bits may be used to control board access from the software side.

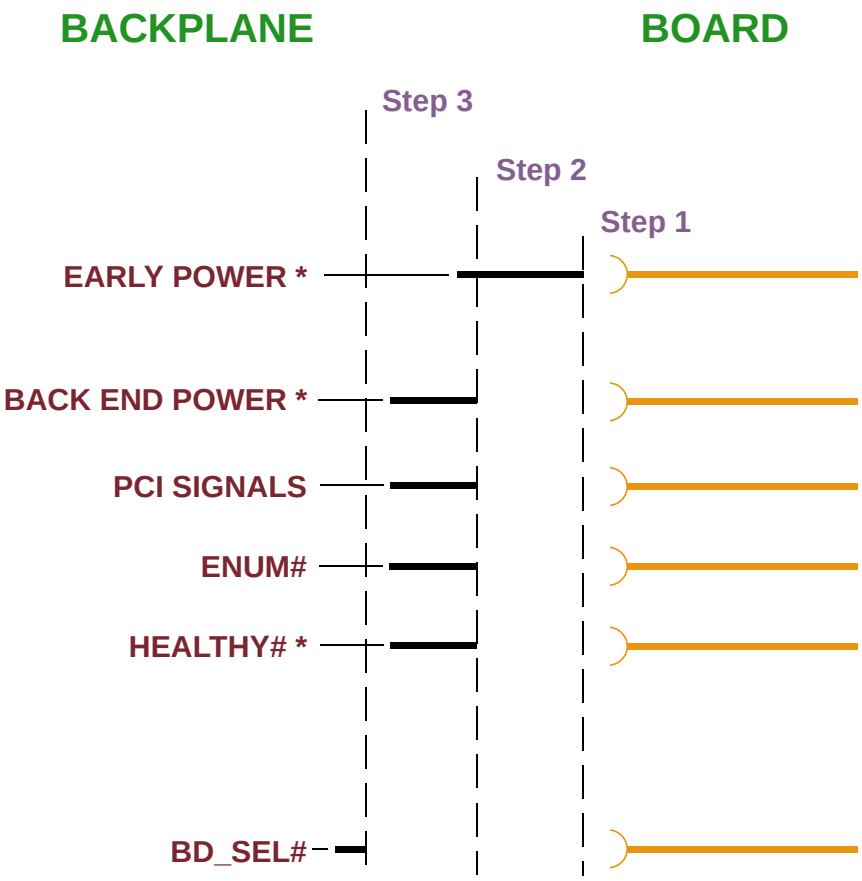
2.8.2 Hotswap System

A hotswap system consists of a hotswap platform which comprises a hotswap backplane, the system host (CPU) with hotswap features, cooling, power supplies etc. plus the boards to be hotswapped. Hotswapping is not possible unless the operating system has the capability to enable and disable the board specific driver during normal operation.

2.8.2.1 The Hotswap Backplane

The hotswap backplane, illustrated on the following page, has staggered pins to ensure defined power sequencing.

Figure 2-13: Illustration of Staggered Pinning on the Hotswap Backplane



EXPLANATORY KEY

***EARLY POWER: a part of VCC, 3.3V, V(I/O) and GND**

***BACK END POWER: the main part of VCC, +3.3V, V(I/O), +/-12V and GND**

***HEALTHY: only for high availability**

Note...

Some special signals (e.g. ENUM, HEALTHY, BDSEL...) have particular routing requirements.

2.8.2.2 The System Controller/Master

The System Controller must have the possibility to utilize the special signals defined by the CompactPCI hotswap specification. If a high availability system is used it must additionally be able to control the hardware connection with the peripheral boards (Hardware Connection Control).

2.8.2.3 The Hotswap Board Additional Features

To ensure that a board may be removed and replaced in a working bus without disturbing the system it requires the following additional features.

- precharge
- power ramping
- hotswap control and status register bits
- automatic interrupt generation whenever a board is about to be removed or replaced.
- an LED to indicate that the board may be safely removed.

2.8.3 The Hotswap Process

The hotswap process has two components; board extraction and board insertion

2.8.3.1 Board Extraction

Start by opening (pulling down) the lower board handle, this will result in the CompactPCI bridge generating an interrupt (ENUM). The system master will now identify the board to be extracted and, when safe to do so, will disable the relevant software drivers. Next the system master lights the blue LED which signals that it is now safe to remove the board by means of its handles.

- open lower board handle - this results in an interrupt from the CPCI bridge (ENUM)
- system master identifies board to be extracted
- when safe to do so the system master disables the relevant software drivers
- system master lights blue LED on the board to signal that it may be safely removed
- board may now be removed by means of its handles

2.8.3.2 Board Insertion

Take hold of the board by the handles and push it steadily into its slot. The long pins are the first to connect and power up the CompactPCI bridge and hotswap controller and preload the CompactPCI signal pins. Next the medium length pins connect leading to the power ramping of the entire board and the mating of the signal pins. Lastly the one short pin connects, generating an onboard reset. With the board fully inserted the lower handle is now closed, this generates an interrupt (ENUM) which signals to the system master that a board has been added to the system. The system master identifies the board and allocates system resources to the board. Next the system master activates software drivers relating to the board. Finally the blue LED is deactivated indicating that the process is complete.

- commence insertion of the board using the handles
  - the long pins are the first to connect and power up CPCI bridge and hotswap controller and preload the CompactPCI signal pins
  - the medium pins connect leading to the power ramping of the entire board and the signals pins mate
  - the short pin connects generating an onboard reset
- lower handle is closed, this generates an interrupt (ENUM) which signals to the system master that a board has been added to the system
- system master identifies the board and allocates system resources to the board
- system master activates software drivers relating to the board
- blue LED is deactivated indicating that the process is complete

2.8.4 Design Implementation on CP620-PM

2.8.4.1 Power Ramping

On the CP620-PM, a special hotswap controller is used to ramp up the onboard supply voltage The reason for this is to avoid transients on the 3.3V, 5V, +12V and -12V power supplies from the Hotswap system. When the power supply is stable, the hotswap controller generates a reset on the PMC slots to put the devices into a definite state.

2.8.4.2 Precharge

Precharge is provided on the CP620-PM by a resistor on each signal line (PCI bus), connected to a 1V reference voltage.

2.8.4.3 Handle Switch

A microswitch is situated in the extractor handle. Opening the handle initiates the generation of the ENUM interrupt (produced by the onboard logic). The microswitch is routed to CON12 on the board.

2.8.4.4 ENUM# Interrupt

The onboard logic generates a low active interrupt signal to indicate that the board is about to be extracted from the system or inserted into the system.

2.9 Intelligent Platform Management Interface (IPMI)

2.9.1 Technical Background of IPMI

The CP620-PM has been configured to support the "Intelligent Platform Management Interface" (IPMI) subsystem which is another step in providing high availability platforms. Intelligent Platform Management means monitoring the health of the entire system beyond the confines of the board itself, so that the status of the complete system is available to be used, for example, for control and intervention purposes. A range of variables is monitored on every board, to provide information on the system status, e.g. voltages, temperature, powergood signals, reset signals etc. Additionally, the IPMI Baseboard controller can intervene, regulating the operating status of the system by controlling fans, shutting down systems and generating alarm signals as and when fault conditions occur. These fault conditions are simultaneously logged in non-volatile memory for analysis and for fault recovery. IPMI also defines a protocol (software stack) for exchanging the status messages of the board, so that "IPMI ready" boards/systems from different suppliers can be monitored. In addition, a clear interface (registers, addresses etc.) is defined for guaranteeing that System-Management software can work with every compliant IPMI hardware.

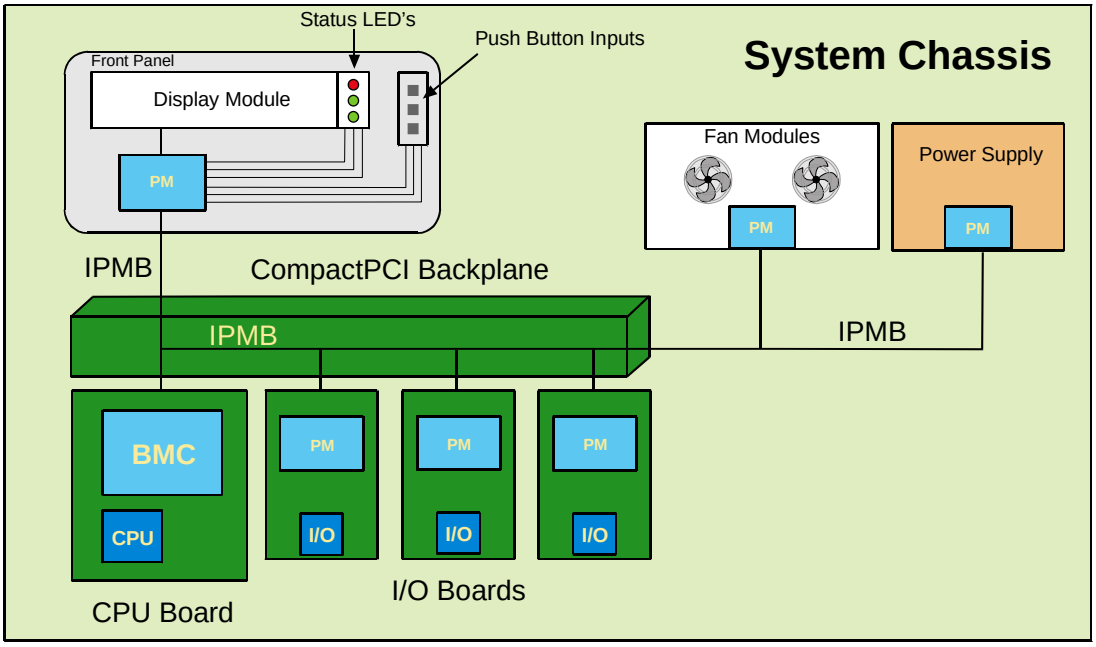
The electrical interconnection between IPMI capable boards is an I2C interface (IPMB). On CompactPCI systems, this interface is provided on IPMI-prepared backplanes and guarantees the data path between the boards.

The devices which handle the measurements and the protocol stack are microcontrollers which are named Baseboard-Management-Controller (BMC) and Peripheral-Management-Controller (PM) depending on their position in a CompactPCI backplane. The IPMI microcontroller which is on the System Master board in a CompactPCI system is called BMC and the IPMI controller which is on a Peripheral board is named PM.

The interface between the system controller CPU’s System Management software and the BaseBoard Management Controller can be realized in two different ways, a keyboard controller style interface (KCS) or a block transfer interface (BT) which can be found in the system master’s I/O space.

A Functional Block Diagram for the IPMI appears on the next page

Figure 2-14: IPMI Functional Block Diagram



2.9.2 IPMI Implementation on the CP620-PM

On the CP620-PM, the IPMI functionality is realized using the ZIRCON-Lite controller from QLogic, which is an ARM7TDMI core-based IPMI controller. Due to the fact that this controller can act as BMC and as PM on all versions of the CP620, the same controller can be used. All the information collected by the ZIRCON-Lite is then accessible by software through a keyboard-style Interface (see IPMI-Intelligent Platform Management Interface Specification V.1.0 for more information) whose address space is available in the I/O space of the Intel CPU's address map, or via the IPMB-Bus.

2.9.3 Measurement of Onboard Voltages

On the CP620-PM all voltages are monitored by the ZIRCON-Lite. This means 5V, 3.3V, 2.5V, VCORE, VIO, 12V and -12V.

2.9.4 Measurement of Temperatures

An onboard sensor measures the temperature in the vicinity of the CPU (positioned below the heatsink).

2.9.5 Fan Control

Four Tacho inputs and two PWM outputs are routed to the rear I/O connector. These make it possible to control the fan speed to regulate the CPU cooling.

2.9.6 Data Repositories

All the data gathered by the ZIRCON is stored in a non-volatile memory, providing the possibility to obtain information about working conditions and failure situations.

Chapter 3

Installation

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3. Installation

The CP620-PM has been designed for easy installation. However, the following standard precautions and installation information and procedures must be observed to ensure proper installation and to preclude damage to the board or injury to personnel.

3.1 Hardware Installation

The product described in this manual can be installed in any available slot of a CompactPCI bus system. However, to function as a system controller it must be installed in slot 1 (far left).

3.1.1 Safety Requirements

The board must be securely fastened to the chassis using the front panel retaining screws to avoid loosening of the board through vibration and to ensure proper grounding and operation of the board.

Caution, Electric Shock Hazard!

Switch off the CompactPCI system main power before installing the board. Ensure that there are no other external voltages being applied to system. This includes signals to all other boards within the system. Failure to comply with the above could endanger your life or health and may damage your board or system.

ESD Equipment!

This CompactPCI board contains electrostatically sensitive devices. Please observe the following precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

Do not touch components, connector pins, or conductive circuits.

If working at an anti-static workbench with professional discharging equipment, ensure compliance with its usage when handling this product.

3.1.2 Installation Procedures

To install the board proceed as follows:

Ensure that the safety requirements indicated above are observed.

Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation. Please refer to chapter 4 for configuration information.

- Ensure that the board is properly configured for operation before installing.

Note...

Care must be taken when applying the procedures below to ensure that when the board is inserted it is not damaged through contact with other boards in the system.

- Install the board in the appropriate slot and ensure that it is properly seated in the backplane (front panel is flush with the rack front).
- Fasten the front panel retaining screws.
- Connect external interfacing cables to the board as required
- Ensure that the board and interfacing cables are properly secured.

3.1.3 Removal Procedures

To remove the board proceed as follows:

- Ensure that the safety requirements indicated above are observed.
- Disconnect any interfacing cables that may be connected to the board.
- Loosen the front panel retaining screws.
- Disengage the board from the backplane by pressing down on the front panel handle and pull the board out of the slot.

3.2 Hotswap Procedure

3.2.1 Prerequisites

In order to utilize the CP620-PM's hotswap capability the operator must ensure that the system in which the CP620-PM is installed fully supports hotswap. This means that the system master, operating system, software drivers, etc. must all be hotswap capable. Otherwise, the following hotswap procedures for the CP620-PM do not apply.

3.2.1.1 Board Extraction

Warning!

Do not perform the following procedures before reading "Prerequisites" above. Failure to comply may result in personal injury or damage to equipment.

- open lower board handle - this results in an interrupt from the CPCI bridge (ENUM)
- system master identifies board to be extracted
- when safe to do so the system master disables the relevant software drivers
- system master lights blue LED on the board to signal that it may be safely removed
- board may now be removed by means of its handles

Note...

It will often take five seconds or so from the time at which the lower board handle is opened until the blue LED lights. This interval will depend on the load on the system master, data traffic, etc. In any event this interval should not exceed one minute.

3.2.1.2 Board Insertion

Warning!

Do not perform the following procedures before reading “Prerequisites” above. Failure to comply may result in personal injury or damage to equipment.

- commence insertion of the board using the handles
  - the long pins are the first to connect and power up CPCI bridge and hotswap controller and preload the CompactPCI signal pins
  - the medium pins connect leading to the power ramping of the entire board and the signals pins mate
  - the short pin connects generating an onboard reset
  - lower handle is closed, this generates an interrupt (ENUM) which signals to the system master that a board has been added to the system
  - system master identifies the board and allocates system resources to the board
  - system master activates software drivers relating to the board
  - blue LED is deactivated indicating that the process is complete

Note...

It will often take five seconds or so from the time at which the lower board handle is closed until the blue LED goes off. This interval will depend on the load on the system master, data traffic, etc. In any event this interval should not exceed one minute.

3.3 Software Installation

Software installation is a function of the Bootstrap Loader and is described in chapter 5 of this manual.

Chapter 4

Configuration

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4. Configuration

4.1 Jumper and Resistor Settings

Please see Figures 1-2 and 1-3 in Chapter 1 to view the positions of the jumpers and resistors on the board.

4.1.1 J3 - Bootstrap Loader / Socket Jumper

The jumper J3 is used to select the memory position from which the CP620-PM fetches its boot code. It establishes the address location of the onboard Flash window and the memory expansion socket 1 (DIL600, 32-pin). Refer to the Memory Configuration Register chapter for further information.

Table 4-1: J3 - Bootstrap Loader / Socket Jumper Settings

J3	DESCRIPTION	ADDRESS ASSIGNMENT	
Open	CP620-PM fetches boot code from onboard Flash	Socket 1: Onboard Flash Window:	0xFFF8 0000 - 0xFFFF FFFF 0xFFF0 0000 - 0xFFF7 FFFF
Closed	CP620-PM fetches boot code from socket 1	Socket 1: Onboard Flash Window:	0xFFF0 0000 - 0xFFF7 FFFF 0xFFF8 0000 - 0xFFFF FFFF

Note...

The IBM PPC750CX/CXE initially fetches its boot code from the address 0xFFF0 0100

4.1.2 J2 - Realtime Clock (RTC) Calibration Output

J2 is a test point for calibration measurement of the frequency of the RTC and is as such not a jumper. Refer to the datasheet of the ST M41T56 for further information on the use of this output signal.

Warning!

At NO TIME is J2 to be jumpered (short circuited). This is a test point and operation with a jumper installed will cause damage to the RTC.

4.1.3 Resistor Settings for Non-Standard Socket Devices

The default pinouts of sockets 1 and 2 are designed for use with standard DIL Flashes and M-Systems DiskOnChip. However, in order to accommodate the various possible devices it is necessary to install resistors as jumpers to configure the board for proper operation.

Table 4-2: Resistor Settings for Socket 1

USED SOCKET DEVICE	R267	R316	R320	R317	R251	R318	R321
Flash / DiskOnChip (default)	Open	Open	Open	Set	Set	Open	Set
NVSRAM	Open	Open	Set	Open	Set	Set	Open
4 Mbit EPROM	Set	Set	Open	Open	Open	Open	Set

Note...

All resistors are 0 ohm.

4.1.4 Resistor Setting for RS485/RS422 Selection

Both the SER2 and SER3 ports may be used in either RS485 or RS422 mode. Selection is made by means of the resistors detailed in the following table:

Table 4-3: Resistor Setting for RS485/RS422 Selection

MODE	R101	R117	R118	R124
SER2 and SER3 in RS485 half duplex mode (default)	Set (4k7)	Open	Set (4k7)	Open
SER2 in RS422 mode, SER3 in RS485 mode	Open	Set (0R)	Set (4k7)	Open
SER2 in RS485 mode, SER3 in RS422 mode	Set (4k7)	Open	Open	Set (0R)
SER2 and SER3 in RS422 mode	Open	Set (0R)	Open	Set (0R)

Note...

These interfaces are optional (special board version).

4.1.5 RS485/RS422 Slew Rate Limit

On versions of the board which are equipped with the RS485/RS422 transceivers, it is possible to limit the signal slew rate to enhance the EMI behaviour.

Table 4-4: Interface SER2 Slew Rate Limit Settings

Slew Rate	R89	R75
10 mb/s (default)	Open	Set (0R)
115 Kb/s	Open	Open
500 kb/s	Set (4k7)	Open

Table 4-5: Interface SER3 Slew Rate Limit Settings

Slew Rate	R54	R66
10 mb/s (default)	Open	Set (0R)
115 Kb/s	Open	Open
500 kb/s	Set (4k7)	Open

4.2 Board Address Map

The following figures illustrate the address mapping of the CP620-PM. Where the first figure describes the overall map, the second figure provides a more detailed map of the uppermost address area. The upper area address map depends on the configuration of the CP620-PM memory expansion sockets and the requirements of the application.

Figure 4-1: CP620-PM Address Map

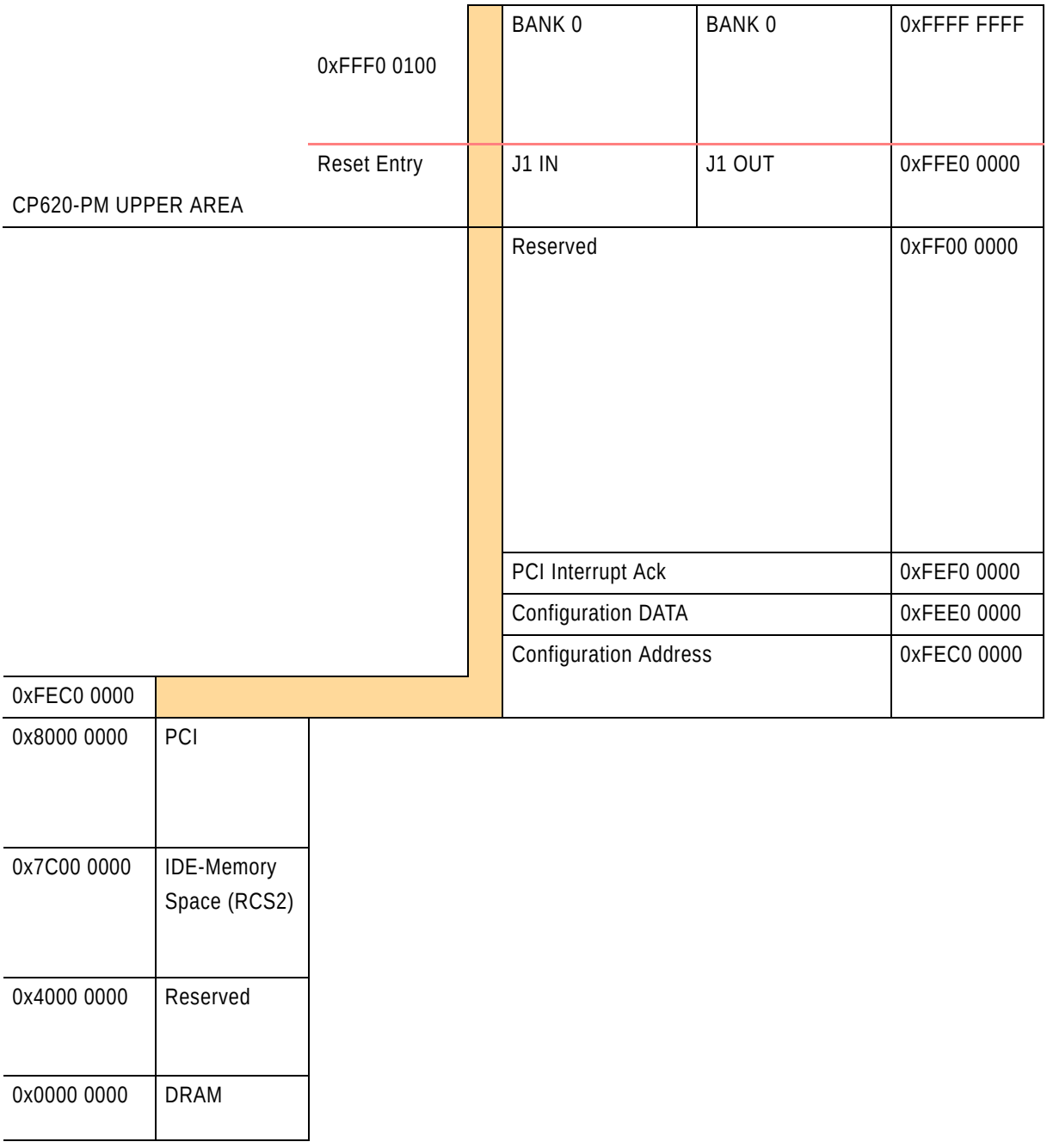

Figure 4-2: CP620-PM Upper Area Address Map

	Soldered FLASH (paged)	0xFFFF FFFF 0xFFF8 0000	Memory Expansion Socket 1	0xFFFF FFFF 0xFFF8 0000
0xFFF0 0100	Memory Expansion Socket 1		Soldered FLASH (paged)	
Reset Entry		0xFFF0 0000		0xFFF0 0000
	Reserved	0xFFE8 0000	Reserved	0xFFE8 0000
	IPMI	0xFFE0 0040	IPMI	0xFFE0 0040
	UART D	0xFFE0 0028	UART D	0xFFE0 0028
	UART C	0xFFE0 0020	UART C	0xFFE0 0020
	Onboard Register	0xFFE0 0010	Onboard Register	0xFFE0 0010
	UART B	0xFFE0 0008	UART B	0xFFE0 0008
	UART A	0xFFE0 0000	UART A	0xFFE0 0000
	Installed		Removed	

Boot Strap / Loader Jumper - J3

Note...

Write access to the upper area addresses is only possible using byte-wide write commands.

4.3 Board Control Registers

The Board Control registers may be accessed through byte-wide read and write operations to the address space 0xFFE0 0000 - 0xFFE7 FFFF

Table 4-6: Board Control Registers

REGISTER	ADDRESS	ACCESS	
		READ	WRITE
Board ID	0xFFE0 0010	X	
Software Compatibility ID	0xFFE0 0012	X	
Memory Configuration	0xFFE0 0014	X	
Flash Bank Select	0xFFE0 0016	X	X
Watchdog Control Register	0xFFE0 0018	X	X
Control Register	0xFFE0 001A	X	X
Interface Route Register	0xFFE0 001B	X	X
Event Register	0xFFE0 001C	X	X
Board/Logic Revision	0xFFE0 001E	X	
IPMI_DATA_IN (keyboard style interface)	0xFFE0 0030		X
IPMI_DATA_OUT (keyboard style interface)	0xFFE0 0030	X	
IPMI_Command Register (keyboard style interface)	0xFFE0 0031		X
IPMI Status Register	0xFFE0 0031	X	
CompactFlash Registers	7C000000 - 7C000078	for details please refer to table 4-29	

4.3.1 Board ID Register

The Board ID is used to identify the CP620-PM in a CompactPCI system. The value for the CP620-PM is 0x81 which is factory set and cannot be changed.

Table 4-7: Board ID Register

REGISTER NAME	BOARD ID						ACCESS	
ADDRESS	0xFFE0 0010						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	BID7	BID6	BID5	BID4	BID3	BID2	BID1	BID0
DEFAULT	1	0	0	0	0	0	0	1

4.3.2 Software Compatibility ID

The Software Compatibility ID will signal to the software when differences in hardware require different handling by the software. It starts with the value 0x00 and will be incremented with each change in hardware (software sensitive only). This register is set at the factory and is for use only by the Bootstrap Loader and BSP software, and as such, is not user relevant.

Table 4-8: Software Compatibility ID

REGISTER NAME	SOFTWARE COMPATIBILITY ID						ACCESS	
ADDRESS	0xFFE0 0012						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0
DEFAULT	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a

4.3.3 Memory Configuration Register

The Memory Configuration register provides basic information concerning the amount of installed main memory, whether or not ECC is enabled, and the location from which the operating system is to access the bootstrap loader.

Table 4-9: Memory Configuration Register

REGISTER NAME		MEMORY CONFIGURATION						ACCESS	
ADDRESS		0xFFE0 0014						R	
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		BJ	res.	res.	res.	SZ3	SZ2	SZ1	SZ0
DEFAULT		n/a	n/a	n/a	1	n/a	n/a	n/a	n/a
BIT	NAME	VAL	DESCRIPTION						
0	SZ0	0	Settings:						
		1	SZ3	SZ2	SZ1	SZ0			
1	SZ1	0	0	0	0	1	64 MB (64 Mbit chips, 1 bank equipped)		
		1	0	0	1	0	128 MB (64 Mbit chips, 2 banks equipped)		
2	SZ2	0	0	1	0	1	128 MB (128 Mbit chips, 1 bank equipped)		
		1	0	1	1	0	256 MB (128 Mbit chips, 2 banks equipped)		
3	SZ3	0	0	1	1	1	384 MB (128 Mbit chips, 3 banks equipped)		
		1	0	1	0	0	512 MB (128 Mbit chips, 4 banks equipped)		
			1	0	1	0	512 MB (256 Mbit chips, 2 banks equipped)		
			1	0	1	1	768 MB (256 Mbit chips, 3 banks equipped)		
			1	0	0	0	1 GB (256 Mbit chips, 4 banks equipped)		
4	Res.	0	Reserved						
		1							
5	Res.	0	Reserved						
		1							
6	Res.	0	Reserved						
		1							
7	BJ	0	Boot Jumper J3 closed (CP620-PM fetches boot code from onboard Flash)						
		1	Boot Jumper J3 open (CP620-PM fetches boot code from socket 1)						

4.3.4 Flash Bank Select Register

The Flash bank select register is used to select the appropriate soldered Flash bank. As 8-bit wide Flash memory may only be accessed through a 512 kB window this is the only way to address a larger size Flash memory. Using bits 0 to 3 (FBn), 16 Flash banks can be selected (16x512 kB = 8 MB). The default value on startup of the CP620-PM is 0x00.

Table 4-10: Flash Bank Select Register

REGISTER NAME	FLASH BANK SELECT						ACCESS	
ADDRESS	0xFFE0 0016						R	W
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	res.	res.	res.	res.	FB3	FB2	FB1	FB0
DEFAULT	n/a	n/a	n/a	n/a	0	0	0	0

4.3.5 Watchdog Control Register

The Watchdog Control register is the interface between applications and the operating system for controlling the functioning of the Watchdog. Together with the Event Register, bit 0 (WD) and bit 2 (PB2), the possibility is provided for either hardware (Abort switch) or software (Watchdog timer) intervention in the execution of the application.

Table 4-11: Watchdog Control Register

REGISTER NAME		WATCHDOG CONTROL						ACCESS	
ADDRESS		0xFFE0 0018						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		WD_EN	WD_R	WD_CCD	WD_TRG	res.	res.	WDT1	WDT0
DEFAULT		0	0	0	0	n/a	n/a	n/a	n/a
BIT	**NAME**	**VAL**	**DESCRIPTION**						
0	WDT0	0	Settings: WDT1 WDT0						
		1	0 0 0.5 seconds Watchdog timeout time						
1	WDT1	0	0 1 1.0 seconds Watchdog timeout time						
		1	1 0 1.5 seconds Watchdog timeout time						
2		0	1 1 2.0 seconds Watchdog timeout time						
		1	Reserved						
3		0	Reserved						
		1							
4	WD_TRG	0	When WD-EN (bit 7) set to 1, indicates that Watchdog timer has not been retriggered.						
		1	Causes the Watchdog to be retriggered (Resets Watchdog timer to value indicated by bits 0 and 1, and WD_TRG (bit 4) to 0)						
5	WD_CCD	0	Normal watchdog functionality						
		1	Cascade mode: when watchdog timout occurs, an NMI will be generated, the watchdog timer resets, a further timeout will result in a system reset						
6	WD_R	0	Causes hardware reset of system upon Watchdog timeout						
		1	Causes generation of a non-maskable interrupt upon Watchdog timeout						
7	WD_EN	0	Watchdog timer disabled						
		1	Watchdog timer enabled  ***Note...*** Once the Watchdog timer is enabled it cannot be disabled except by resetting the system.						

4.3.6 Control Register

The Control register provides access to the front panel general purpose LED's (LED1R and LED1G), allows for the generation of a software reset of the system, and is used to control the configuration of the SER 0 (UART B) either for RS-232 or RS-485 operation.

Table 4-12: Control Register

REGISTER NAME		CONTROL						ACCESS	
ADDRESS		0xFFE0 001A						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		RS_CTL	Res.	IDE_RST	S_RST	GPLED3	GPLED2	GPLED1	ind. LED
DEFAULT		n/a	n/a	0	n/a	0	0	0	0
BIT	NAME	VAL	DESCRIPTION						
0	Indicator LED,green	0	GPLED0 LED1G (green) off						
		1	GPLED0 LED1G (green) on						
1	General Purpose LED 1-3 (optional)	0	GPLED1 (optional, red) off						
		1	GPLED1 (optional, red) on						
2		0	GPLED2 (optional, yellow) off						
		1	GPLED2 (optional, yellow) on						
3		0	GPLED3 (optional, green) off						
		1	GPLED3 (optional, green) on						
4	S_RST	0	No operation						
		1	Causes a software reset (S_RST) to be initiated						
5	IDE_RST	0	Reset for CompactFlash not asserted						
		1	Reset for CompactFlash assert						
6	ETH_DIR0	0	Front IO for Ethernet interface 0 (default)						
		1	Rear IO for Ethernet interface 0						
7	ETH_DIR1	0	Front IO for Ethernet interface 1 (default)						
		1	Rear IO for Ethernet interface 1						

Note...

The direction for the Ethernet interface 0 is also determined by the status of jumper J1. The jumper has the highest priority, meaning that if J1 is closed, Ethernet interface 0 will be directed to the front IO regardless of the status of register bit 6.

4.3.7 Interface Route Register

Table 4-13: Interface Route Register

REGISTER NAME		INTERFACE ROUTE						ACCESS	
ADDRESS		0xFFE001b						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		SER3_Echo	SER2_Echo	SER3_485	SER2_485	SER3_DIR	SER2_DIR	SER1_DIR	SER0_DIR
DEFAULT		0	0	0	0	0	0	0	0
BIT	NAME	VAL	DESCRIPTION						
0	SER0_DIR	0	Front IO						
		1	Rear IO						
1	SER1_DIR	0	Front IO						
		1	Rear IO						
2	SER2_DIR	0	Front IO						
		1	Rear IO						
3	SER3_DIR	0	Front IO						
		1	Rear IO						
4	SER2_485	0	Configured for RS232						
		1	Configured for RS485						
5	SER3_485	0	Configured for RS232						
		1	Configured for RS485						
6	SER2_ECHO	0	ECHO off (RS485 mode)						
		1	ECHO on (RS485 mode)						
7	SER3_ECHO	0	ECHO off (RS485 mode)						
		1	ECHO on (RS485 mode)						

4.3.8 Event Register

The Event register is used to indicate the origin of the generation of the non-maskable interrupts caused either by a Watchdog timeout or the pressing of the Abort switch.

Table 4-14: Event Register

REGISTER NAME		EVENT						ACCESS	
ADDRESS		0xFFE0 001C						R	W
BIT POSITION		MSB 7	6	5	4	3	2	1	0 LSB
CONTENT		Res.	Res.	Res.	Res.	Res.	PB2	Res.	WD
DEFAULT		n/a	n/a	n/a	n/a	n/a	0	n/a	0
BIT	NAME	VAL	DESCRIPTION						
0	WD	0	Indicates that no Watchdog timeout has occurred						
		1	Indicates that a Watchdog timeout has occurred						
1		0	Reserved						
		1							
2	PB2	0	Indicates that the Abort switch has not been pressed						
		1	Indicates that the Abort switch has been pressed						
3		0	Reserved						
		1							
4		0	Reserved						
		1							
5		0	Reserved						
		1							
6		0	Reserved						
		1							
7		0	Reserved						
		1							

4.3.9 Board Logic / Revision Register

The Board Revision Register may be used to identify the hardware (BRn) and logic status of the board by the software (LRn). It is set at the factory and starts with the value 0x00 for the initial board prototypes and will be incremented with each redesign / logic release.

Table 4-15: Board Logic / Revision Register

REGISTER NAME	BOARD LOGIC/REVISION						ACCESS	
ADDRESS	0xFFE0 001E						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	LR3	LR2	LR1	LR0	BR3	BR2	BR1	BR0
DEFAULT	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a

4.4 UART Registers Address Mapping

4.4.1 UART A

The following tables indicate the address mapping of UART A. For a more detailed description please refer to the EXAR XR16C2850 DUART manual.

Table 4-16: UART A General Register Set

READ MODE	WRITE MODE	ADDRESS
Receive Holding	Transmit Holding	0xFFE0 0000
n/a	Interrupt Enable	0xFFE0 0001
Interrupt Status	FIFO Control	0xFFE0 0002
n/a	Line Control	0xFFE0 0007
n/a	Modem Control	0xFFE0 0004
Line Status	n/a	0xFFE0 0005
Modem Status	n/a	0xFFE0 0006
Scratchpad	Scratchpad	0xFFE0 0007

Table 4-17: UART A Baud Rate Register Set

READ MODE	WRITE MODE	ADDRESS
LSB of divisor latch	LSB of divisor latch	0xFFE0 0000
MSB of divisor latch	MSB of divisor latch	0xFFE0 0001

Table 4-18: UART A Enhanced Register Set

READ MODE	WRITE MODE	ADDRESS
Trigger Level	Trigger Level	0xFFE0 0000
Feature Control	Feature Control	0xFFE0 0001
Enhanced Feature	Enhanced Feature	0xFFE0 0002
Enhanced Mode Select	Enhanced Mode Select	0xFFE0 0007
Xon-1	Xon-1	0xFFE0 0004
Xon-2	Xon-2	0xFFE0 0005
Xoff-1	Xoff-1	0xFFE0 0006
Xoff-2	Xoff-2	0xFFE0 0007

4.4.2 UART B

The following tables indicate the address mapping of UART B. For a more detailed description please refer to the EXAR XR16C2850 DUART manual.

Table 4-19: UART B General Register Set

READ MODE	WRITE MODE	ADDRESS
Receive Holding	Transmit Holding	0xFFE0 0008
n/a	Interrupt Enable	0xFFE0 0009
Interrupt Status	FIFO Control	0xFFE0 000A
n/a	Line Control	0xFFE0 000B
n/a	Modem Control	0xFFE0 000C
Line Status	n/a	0xFFE0 000D
Modem Status	n/a	0xFFE0 000E
Scratchpad	Scratchpad	0xFFE0 000F

Table 4-20: UART B Baud Rate Register Set

READ MODE	WRITE MODE	ADDRESS
LSB of divisor latch	LSB of divisor latch	0xFFE0 0008
MSB of divisor latch	MSB of divisor latch	0xFFE0 0009

Table 4-21: UART B Enhanced Register Set

READ MODE	WRITE MODE	ADDRESS
Trigger Level	Trigger Level	0xFFE0 0008
Feature Control	Feature Control	0xFFE0 0009
Enhanced Feature	Enhanced Feature	0xFFE0 000A
Enhanced Mode Select	Enhanced Mode Select	0xFFE0 000B
Xon-1	Xon-1	0xFFE0 000C
Xon-2	Xon-2	0xFFE0 000D
Xoff-1	Xoff-1	0xFFE0 000E
Xoff-2	Xoff-2	0xFFE0 000F

4.4.3 UART C

The following tables indicate the address mapping of UART C. For a more detailed description please refer to the EXAR XR16C2850 DUART manual.

Table 4-22: UART C General Register Set

READ MODE	WRITE MODE	ADDRESS
Receive Holding	Transmit Holding	0xFFE0 0020
n/a	Interrupt Enable	0xFFE0 0021
Interrupt Status	FIFO Control	0xFFE0 0022
n/a	Line Control	0xFFE0 0027
n/a	Modem Control	0xFFE0 0024
Line Status	n/a	0xFFE0 0025
Modem Status	n/a	0xFFE0 0026
Scratchpad	Scratchpad	0xFFE0 0027

Table 4-23: UART C Baud Rate Register Set

READ MODE	WRITE MODE	ADDRESS
LSB of divisor latch	LSB of divisor latch	0xFFE0 0020
MSB of divisor latch	MSB of divisor latch	0xFFE0 0021

Table 4-24: UART C Enhanced Register Set

READ MODE	WRITE MODE	ADDRESS
Trigger Level	Trigger Level	0xFFE0 0020
Feature Control	Feature Control	0xFFE0 0021
Enhanced Feature	Enhanced Feature	0xFFE0 0022
Enhanced Mode Select	Enhanced Mode Select	0xFFE0 0027
Xon-1	Xon-1	0xFFE0 0024
Xon-2	Xon-2	0xFFE0 0025
Xoff-1	Xoff-1	0xFFE0 0026
Xoff-2	Xoff-2	0xFFE0 0027

4.4.4 UART D

The following tables indicate the address mapping of UART A. For a more detailed description please refer to the EXAR XR16C2850 DUART manual.

Table 4-25: UART D General Register Set

READ MODE	WRITE MODE	ADDRESS
Receive Holding	Transmit Holding	0xFFE0 0028
n/a	Interrupt Enable	0xFFE0 0029
Interrupt Status	FIFO Control	0xFFE0 002A
n/a	Line Control	0xFFE0 002B
n/a	Modem Control	0xFFE0 002C
Line Status	n/a	0xFFE0 002D
Modem Status	n/a	0xFFE0 002E
Scratchpad	Scratchpad	0xFFE0 002F

Table 4-26: UART D Baud Rate Register Set

READ MODE	WRITE MODE	ADDRESS
LSB of divisor latch	LSB of divisor latch	0xFFE0 0028
MSB of divisor latch	MSB of divisor latch	0xFFE0 0029

Table 4-27: UART D Enhanced Register Set

READ MODE	WRITE MODE	ADDRESS
Trigger Level	Trigger Level	0xFFE0 0028
Feature Control	Feature Control	0xFFE0 0029
Enhanced Feature	Enhanced Feature	0xFFE0 002A
Enhanced Mode Select	Enhanced Mode Select	0xFFE0 002B
Xon-1	Xon-1	0xFFE0 002C
Xon-2	Xon-2	0xFFE0 002D
Xoff-1	Xoff-1	0xFFE0 002E
Xoff-2	Xoff-2	0xFFE0 002F

4.4.5 CompactFlash

Table 4-28: CompactFlash Register

REGISTER	READ/WRITE	ADDRESS
Data Register	R/W	7c000000
Error Register	R	7c000008
Feature Register	W	7c000008
Sector Count Register	R/W	7c000010
Sector Number Register	R/W	7c000018
Cylinder Low Register	R/W	7c000020
Cylinder High Register	R/W	7c000028
Drive/Head Register	R/W	7c000030
Status Register	R	7c000038
Device Control Register	W	7c000038
Alternate Status Register	R	7c000070
Digital Output Register	W	7c000070
Card Drive Address Register		7c000078

4.4.6 IRQ Routing

The IRQ routing of the CP620-PM is serial as opposed to being parallel. Hence the IRQ names are prefixed with S_ to indicate that they are serial.

Table 4-29: IRQ Routing

IRQ NAME	SOURCE
S_IRQ0	Reserved
S_IRQ1	UART-A
S_IRQ2	UART-B
S_IRQ3	INTA# (PCI)
S_IRQ4	INTB# (PCI)
S_IRQ5	INTC# (PCI)
S_IRQ6	INTD# (PCI)
S_IRQ7	TEMP_INT (Temperature Interrupt)
S_IRQ8	IDE (CompactFlash)
S_IRQ9	Reserved
S_IRQ10	UART-C
S_IRQ11	UART-D
S_IRQ12	IPMI (optional)
S_IRQ13	Reserved
S_IRQ14	Reserved
S_IRQ15	Reserved

4.4.7 Real-time Clock

Access to the real-time clock (RTC) is effected via the I2C bus. The RTC uses address 0xD0. For more detailed information please refer to the manuals for the ST - Microelectronics M41T56 and the Motorola MPC 107 (I2C - Bus).

Table 4-30: Register Map RTC M41T56

REG. BYTE	ADDRESS BITS								FUNCTION RANGE IN BCD FORMAT
	D7	D6	D5	D4	D3	D2	D1	D0	
0	ST	10 Seconds			Seconds				Seconds: 00 - 59
1	X	10 Minutes			Minutes				Minutes: 00 - 59
2	CEB	CB	10 Hours		Hours				Century: 0 - 1 Hours: 00 - 23
3	X	X	X	X	X	Day			Day: 00 - 07
4	X	X	10 Date		Date				Date: 01 - 31
5	X	X	X	10M.	Month				Month: 01 - 12
6	10 Years				Years				Year: 00 - 99
7	OUT	FT	S	Calibraton					Control

Legend for Table 4-31:

CEB = Century enable bit
CB = Century bit
FT = Frequency test bit
OUT = Output level
ST = Stop bit
S = Sign bit

Note...

When the RTC has once been stopped due to low voltage, it is necessary to re-initialize the “Seconds” “Minutes” and “Hours” registers before it will run again.

4.5 EEPROM’s

Access to the EEPROM’s is effected via the I2C bus of the MPC107. The EEPROM’s use the I2C address 0xA0 (System) and the address 0xA2 (User). Write protection is achieved by installing 0 ohm resistors R333 (System) and R337 (User). Default is unprotected.

For more detailed information please refer to the manuals for the MICROCHIP 24C64 and the MOTOROLA MPC107 (I2C bus).

4.6 Digital Temperature Sensor, LM75

Access to the onboard digital temperature sensor (DTS) is effected via the I2C bus of the MPC107. The DTS uses the I2C address 0x90.

For more detailed information please refer to the manuals for the National Semiconductor LM75 and the MOTOROLA MPC107 (I2C bus).

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Chapter 5

Bootstrap Loader

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5. Bootstrap Loader

The CP620 Bootstrap Loader is a standalone software located in the Flash memory which allows the user to safely update the contents of the Flash and delay the boot process for a specified time.

The Bootstrap Loader has the capability to program Flash memory from “Motorola S-records” or from an absolute memory address. If the programmed image does not work, the Bootstrap Loader can be re-entered. The memory contents can be examined and another programming cycle initiated.

The Bootstrap Loader is delivered already installed in soldered Flash.

Please read this user manual before reprogramming any Flash memory.

Warning!

When programming Flash memory, please do not press the RESET button or switch off the mains power under any circumstances! Doing so may damage the Bootstrap Loader and would consequently leave the board unusable due to corrupt Flash contents.

However, the ABORT button may be used to cancel a running operation safely.

5.1 System Operation

5.1.1 Startup

After system reset, the Bootstrap Loader is started. It searches the Flash memory area for a valid start key. If this start key is found, the Bootstrap Loader checks the 'BootWaitTime' from serial EEPROM. If the entry is valid, the continuation of the boot process is delayed for a period during which the green front panel LED flashes to indicate that the system is alive but waiting for continuation. If the entry is not valid, a default of 5 seconds is used. After the BootWaitTime has passed, the program in Flash is downloaded and started.

The Bootstrap Loader has two modes of operation: non-interactive start mode as described above and the interactive command mode.

For normal board operation, only the non-interactive start mode is used to start a program in Flash. This happens automatically without any user interaction. The interactive command mode is used to re-program the Flash memory contents or change the BootWaitTime.

The serial term port operates at 9600 Baud, 8 bits / character, 1 stop bit and no parity by default.

5.1.2 Entering the Command Mode

There are two possible reasons for entering the Bootstrap Loader command mode:

- If no valid start key is found, the Bootstrap Loader command mode is entered automatically.
- If the user wants to enter the Bootstrap Loader manually, e.g. for re-programming the Flash contents, the ABORT button on the front panel must be used.

Warning!

The ABORT button must not be pushed until the green LED is lit, because this button generates an NMI, and the exception vector tables must be initialized correctly to serve this NMI.

However, the ABORT button must be pushed before the green LED stops flashing (BootWaitTime), since the system control is transferred to the downloaded binary image afterwards. The LED is cycled every 0.25 sec. so if 1 second is specified as BootWaitTime, the LED will only flash twice.

Note...

CTRL-x deletes the complete input line while CTRL-a restores the last input line on the command I/F.

5.1.3 Programming a New Binary Image to Flash Memory

5.1.3.1 Preparing the Image

The image must be compiled / linked to run from the Flash base address 0x0 of the CPU. The image must contain executable PPC code at offset 0x100, as is usual for ROM/Flash images.

5.1.3.2 Programming with Motorola S-Records

Programming is done with the *If* command.

The *If* command accepts S1, S2 and S3 records. Operation is terminated by the appropriate S9, S8 or S7 record. Other types of records are ignored.

The checksum of every record except end records is checked. Bad records are rejected by the Bootstrap Loader. The address range of every record is also checked; records that try to overwrite the Bootstrap Loader are rejected. Additionally, every record must match the programmable area exactly. To give the user an overview of the available ranges, the startup banner includes address information.

In the case of the CP620 the Flash addresses are only “virtual”. The downloaded image is copied to RAM during startup and is executed there. For this reason images which require to be programmed in should start at the address 0×0.

Note...

The image must start at the absolute address 0×0 and must contain executable PPC code at the absolute address 0×100

If S1 or S2 record input is preferred, please note that these records only include 16 and 24-bit wide addresses. If no switch to another record type is included it must be ensured that the code is not larger than the address range covered.

Note...

The ’If’ command cannot be used to program Motorola S-records to RAM areas.

For sending programming data, the lower *(term)* or upper *(ser0)* RJ45 front panel connectors can be used. The *ser0* port is preferable, because in this configuration it is possible to monitor the progress of the operation via the *term* port. In any case, the user LED flashes slowly while downloading to give feedback of the usual kind.

If not specified otherwise, sectors which are not touched by the programming operation are not erased. If you want to erase all sectors while programming, the '-c' option can be specified along with the *If* command. This is useful for software which searches memory during startup and should not find any old modules.

Make sure that the XON/XOFF protocol is used on the host side. This is a fixed setting and cannot be changed. Additionally, make sure that your host does not stop transmission after a number of lines.

Serial parameters can be modified with the *pf* command.

5.1.3.3 Monitoring the Programming Progress

In both examples, the programming can be monitored via the *term* port. The characters which are displayed have the following meaning:

- r Read S-record; valid and in range
- t Protected sector touched
- e Erase sector
- c Copy to buffer, program later
- p Program record

None of the above characters indicate an error. The first sector (which includes the first instruction to be executed) and the last sector (which includes the Bootstrap Loader itself) are protected. These sectors are not immediately programmed like the other sectors. The contents of these protected sectors are buffered in RAM and programmed at the end of the operation. This is done to limit the amount of time the Bootstrap Loader itself is not in Flash or not startable, because if the Bootstrap Loader crashes during this critical period of time, it will not start again afterwards.

Warning!

When programming Flash memory, please do not press the RESET button or switch off the mains power in any circumstances! Doing so may damage the Bootstrap Loader and would consequently leave the board unusable due to corrupt Flash contents.

However, the ABORT button may be used to cancel a running operation safely.

The parameter '-q' suppresses all messages and warnings except error messages.

Programming via the *term* port is also supported, but in this case programming of the loader is quiet by default. The progress of this process cannot be monitored directly, since only the green front panel LED (U) flashes while programming is in progress.

It is recommended that programming is undertaken via the *ser0* port.

Note...

Feedback is provided to the operator, however, please note that programming may take several minutes.

If the process must be aborted, press the ABORT button and try again. However, on CPU's without an ABORT button the process cannot be aborted.

5.1.3.4 Programming from an Absolute Address

The second way to program Flash memory is to program it from an absolute address. The image to be programmed must be located in a visible address range, for example on the VMEbus. A memory card with battery-backup, Flash or EPROM can be used to hold the image to program. If we assume that the image is located at 0x87000000 and is 0x123456 bytes large we must type the following at the command prompt of the Bootstrap Loader:

```
lf -m=87000000 -l=123456
```

The characters which are now displayed have the same meaning as if we are programming from S-records, but the time needed for each step to be completed may be longer because the loader tries to program with the largest possible block size that it can manage.

Again, '-c' can be used to clear untouched sectors.

Note...

Quiet operation is not supported, and also it is not possible to specify any offset.

Please note also that programming cannot be cancelled with ABORT.

5.1.4 BootWaitTime

The command *bw* can be used to display/change the current BootWaitTime. Available delays are 1-2-5-10-20-50 seconds. CPU's without a user LED or without an ABORT button have a BootWaitTime of at least 5 seconds. In this case, the Bootstrap Loader will reject a BootWaitTime setting of 1-2 seconds.

The BootWaitTime value is stored in the boot section of the serial EEPROM. This section is validated with a CRC code to avoid the setting of random parameters.

Note...

If the CRC of the Boot section is not valid, changing the BootWaitTime has no effect because the bw command does not validate an invalid CRC in order to avoid undesired side effects. In this case, a default timing of 5 seconds is always used.

To validate an invalid CRC, the appropriate utility from an operating system must be used or, alternatively, the line *bw -f* must be issued.

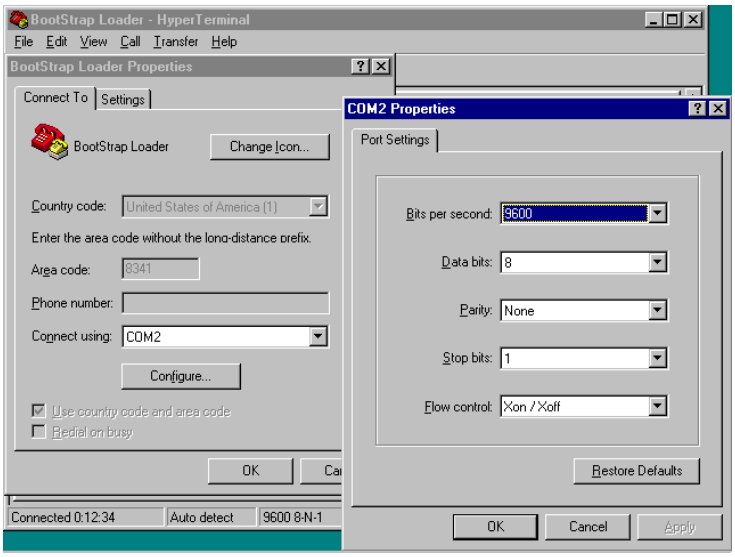
Warning!

Please note that validation with the 'bw -f' command may validate invalid entries, with adverse consequences.

5.1.5 Example Using Hyperterminal under Windows 95/Windows NT

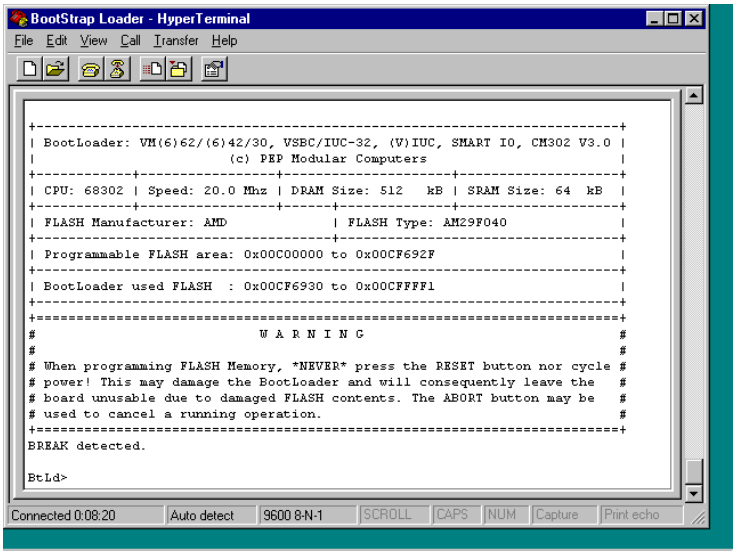
The host is assumed to be a PC with Windows 95 or Windows NT. A serial cable is used to connect the term port of the board to be programmed to COM2 of the PC. Additionally, we assume that we want to program a Motorola S-record built for the Flash address of the board. The serial connection runs at the default configuration of 9600 Baud with no parity and one stop bit. The properties should appear as follows:

Figure 5-1: Setting of COM2 Properties



After entering the Command Mode the following screen should appear:

Figure 5-2: Screen after Entering the Command Mode



Enter 'lf' on the target. The target now waits until the Motorola S-records have been transferred over the term. Select **Transfer/Send Text File** dialogue box and select the file containing the Motorola S-records.

Figure 5-3: Select Transfer/Send Text File Dialogue Box

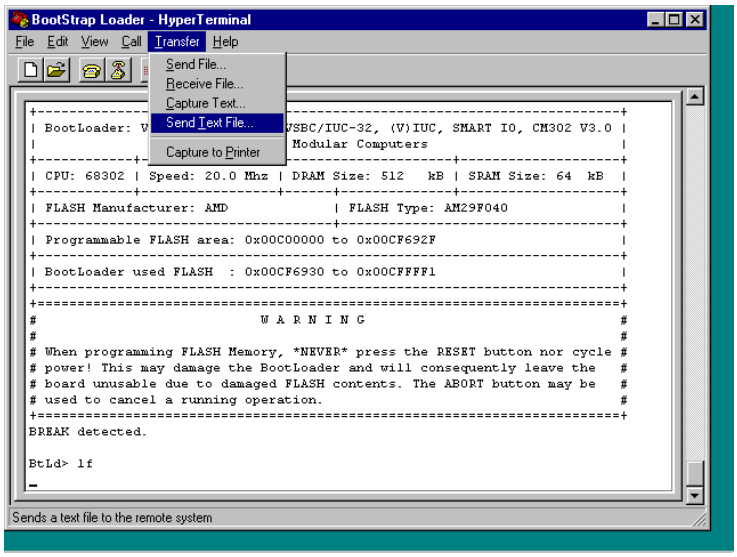
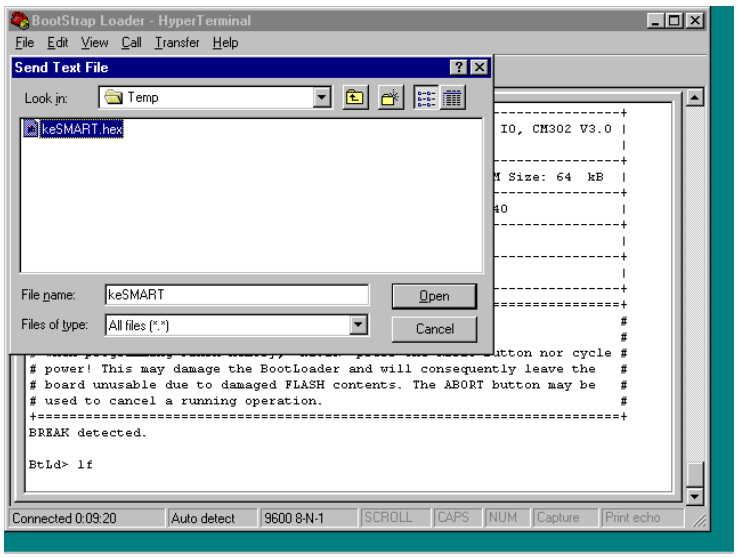


Figure 5-4: Selecting the Motorola S-Records File



After selecting Open the dialogue box disappears and the Motorola S-records are transferred. As soon as the complete file is sent, the prompt of the Bootstrap Loader appears again.

Note...

No status information is displayed.

5.2 Commands

5.2.1 Boot Wait

5.2.1.1 Syntax

```
bw [<time>| -f]
```

5.2.1.2 Description

Without parameters, *bw* displays the current setting.

The parameter <time> may be set to 1, 2, 5, 10, 20 or 50, which signifies the waiting time in seconds. No values other than these are supported, while the option '-f' has the following meaning:

'-f':- force CRC update.

Note...

CPU's without a user LED or without an ABORT button have a BootWaitTime of at least 5 seconds. The Bootstrap Loader will refuse to set a BootWaitTime of 1-2 seconds.

5.2.2 Load Flash

5.2.2.1 Syntax

```
lf [-o[=]<offset>] [-u] [-q] [-c] [-m[=]<adr> -l[=]<len>]
```

5.2.2.2 Description

Without parameters, the Flash is loaded using S-records via the *term* port.

The parameter '<offset>' is a signed 32-bit offset which is added to every record and can be used to move the S-records to the Flash position.

Note...

This option must be selected if the S1 or S2 records are used.

- '-u' must be used to download over *ser0.*
- '-q' suppresses all messages except error messages.
- '-c' clears all untouched sectors and leaves no old code fragments.

For a Load Flash from an absolute address, the -m / -l options must be used.

Note...

On CPU's without a ser0 serial connection the Bootstrap Loader will refuse a command including the '-u' option.

5.2.3 Memory Display

5.2.3.1 Syntax

```
md [<adr>]
```

5.2.3.2 Description

Without parameters specified, the Flash contents starting at the beginning of the programmable Flash area are displayed. This function is not limited to Flash and other address ranges can be specified.

Note...

The first instruction to be executed in Flash is not identical to the one to be executed first from the programming source (S-records memory block).

5.2.4 Port Format

5.2.4.1 Syntax

```
pf [<port> [<baud>][/[<bitschar>][/[<parity>][/<stops>]]]]
```

5.2.4.2 Description

Without parameters specified, the current serial port settings are displayed.

- <port> specifies the serial port. Valid values are *term* or *ser0.*
- <baud> specifies the baud rate. The values 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19200, 38400 and 115200 Baud can be specified.
- <bitschar> specifies the bits / character. Valid values are 7 or 8.
- <parity> specifies if parity should be checked / generated. The value n specifies none, o for odd and e for even parity.
- <stops> specifies the stopbits which will be generated. Valid values are 1 or 2.

Note...

No spaces are permitted between the options. Options must be separated with a slash. Not all options must be specified, but the '/' characters must be present to distinguish the different options from each other. The sequence can be aborted after every option.

On CPU's without a ser0 serial connection the Bootstrap Loader will refuse setting ser0 port parameters and will not display ser0 port parameters.

5.2.4.3 Examples

Setting *term* to 300 Baud, 7 Bits/char, odd parity and 2 stopbits:

```
pf term 300/7/o/n
```

Set the bits / character field to 7 for *ser0* only:

```
pf ser0 /7
```

Set the stopbits field to 2 for ser0:

```
pf ser0 ///2
```

5.2.5 Configure Routing

5.2.5.1 Syntax

route [<option><route>]

5.2.5.2 Description

This command is used to configure the routing of the two Ethernet and four serial channels to either the front or rear. Without parameters, the currently configured routing is displayed.

possible <option> values are as follows:-

- s0 for serial connector term
- s1 for serial channel 1
- s2 for serial channel 2
- s3 for serial channel 3
- e0 for Ethernet channel 1
- e1 for Ethernet channel 2

<route> refers to either of:-

- r for routing to serial I/O
- f for routing to front I/O

Please note that only one routing may be specified at a time.

Example:-

- route s3r

This configures serial channel 3 to the rear I/O. All other channels retain their current setting.

5.2.6 Reset System

5.2.6.1 Syntax

```
rs
```

5.2.6.2 Description

This command exits the Bootstrap Loader and resets the system. It terminates the Bootstrap Loader command mode and resets the entire system, generating a system reset with the onboard watchdog.

5.2.7 Help

5.2.7.1 Syntax

? or *help*

5.2.7.2 Description

This command prints the online help page. The display of the help text varies between the different CPU's reflecting their differences.

5.2.8 PCI Bus Configuration

5.2.8.1 Syntax

pci

5.2.8.2 Description

Displays the PCI configuration. This includes assigned addresses in memory, the I/O space and the assigned interrupt line.

5.3 Plug and Play

On the CP620 the Bootstrap Loader includes "Plug and Play" functionality. This ensures that the board is completely initialized and that all resources necessary for PCI devices (addresses, interrupts etc.) are assigned automatically. This important feature has the advantage that conflicts do not arise when PCI devices are added or removed. Furthermore, the OS itself does not include the board initialisation code.

5.4 Porting an Operating System to the CP620

The image for the absolute address 0×0 should be linked with an entry point at the absolute address at 0×100.

One should not attempt to reassign the PCI BAR registers. The assigned values should be read back and these should always be used in the drivers.

The "interrupt line" field in the PCI configuration header is initialized with the IRQ line number to which the INTA of the device is routed.

The "EUMBBAR" field in the KAHLUA (MPC 8240) configuration space MUST NOT be rewritten - a value has already been assigned by the Bootstrap Loader. The existing value must be used.

Downloaded images are never executed from the Flash due to the fact that on the CP620 it is paged . The programmed image is always downloaded to SDRAM, the absolute address 0×0 being downloaded first. There is no configuration option available to amend this process. If it is necessary to re-locate the image to another address after download, simply add a small assembly routine at the beginning of the code which will move the image to the correct address.

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