CP620

Power PC®-based 6U CPU Board
for CompactPCI Applications

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User Guide

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CE Conformity

This symbol indicates that the product described in this manual is in compliance with CE standards.

Caution, Electric Shock!

This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.

Please refer also to the section “High Voltage Safety Instructions” on the following page.

Warning, ESD Sensitive Device!

This symbol and title inform that electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Please read also the section “Special Handling and Unpacking Instructions” on the following page.

Warning!

This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your material.

Note ...

This symbol and title emphasize aspects the reader should read through carefully for his or her own advantage.

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Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

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Special Handling and Unpacking Instructions

ESD Sensitive Device!

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- Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.
- Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.
- It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

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General Instructions on Usage

- In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron Modular Computers GmbH and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.
- This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present their temperature restrictions must be taken into account.
- In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.
- Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.
- Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Chapter *1*

Introduction

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1. Introduction

1.1 System Overview

The CompactPCI board described in this manual operates with the PCI bus architecture to support additional I/O and memory-mapped devices as required by various industrial applications. For detailed information concerning the CompactPCI standard, please consult the complete Peripheral Component Interconnect (PCI) and CompactPCI Specifications. For further information regarding these standards and their use, visit the home page of the *PCI Industrial Computer Manufacturers Group (PICMG)*.

Many system-relevant CompactPCI features that are specific to Kontron Modular Computers CompactPCI systems may be found described in the Kontron CompactPCI System Manual. Due to its size, this manual cannot be downloaded via the internet. Please refer to the section "Related Publications" at the end of this chapter for the relevant ordering information.

The CompactPCI System Manual includes the following information:

- Common information that is applicable to all system components, such as safety information, warranty conditions, standard connector pinouts etc.
- All the information necessary to combine Kontron's racks, boards, backplanes, power supply units and peripheral devices in a customized CompactPCI system, as well as configuration examples.
- Data on rack dimensions and configurations as well as information on mechanical and electrical rack characteristics.
- Information on the distinctive features of Kontron CompactPCI boards, such as functionality, hot swap capability. In addition, an overview is given for all existing Kontron CompactPCI boards with links to the relating data sheets.
- Generic information on the Kontron CompactPCI backplanes, such as the slot assignment, PCB form factor, distinctive features, clocks, power supply connectors and signalling environment, as well as an overview of the Kontron CompactPCI standard backplane family.
- Generic information on the Kontron CompactPCI power supply units, such as the input/output characteristics, redundant operation and distinctive features, as well as an overview of the Kontron CompactPCI standard power supply unit family.

1.2 Kontron Double-Height PowerPC® CPU Boards

The CP620 is a high performance 64-bit/33 MHz CompactPCI system controller board designed to utilize the IBM® PowerPC® 750CX/CXe RISC microprocessors. This board is also based on the Motorola® MPC107 Bridge/Memory Controller and can support CPU speeds of 400 MHz through 700 MHz at a host bus speed of 100 MHz.

The CP620-PM is a non-system controller which is identical to the CP620 apart from having a different PCI/PCI (non-transparent) bridge at J1(CON1)/J2(CON2). This makes possible the addition of further CP620s together with a system controller CPU on one CompactPCI bus, i.e. multiprocessing.

The CP620-PCIP is a 6U CPU board without a PCI interface to the backplane. It communicates with its environment via the IEEE 802 (Ethernet) provided on J3(CON3)/P3. This is in accordance with the CompactPCI Packet Switching Backplane Specification PICMG 2.16, Revision 1.0, September 5th 2001.

1.3 Board Overview

1.3.1 Board Introduction

The design centered on realizing a board which addresses the need for extending IO capability with PMC-Modules while at the same time having a powerful CPU, a big amount of memory and an optimized power dissipation. Therefore the CP620 provides 2 PMC slots with rear I/O routing to CompactPCI P3 and P5 connectors and a powerful CPU from IBM with speeds up to 600 MHz (and even higher in the future).

Memory configurations of 128 MB to 1GB SDRAM are possible, running at 100 MHz and providing ECC error correction mechanism. This provides single-bit error correction or double-bit error detection for critical applications. In addition to the normal system memory, a choice of either 4 or 8 MB of onboard flash memory for including the initial bootloader and ROMable operating systems are provided. For extending this onboard memory, sockets for DIL-Flash/NVSRAM and CompactFlash are supported by the CP620.

The processor chip itself contains a powerful general purpose G3 processing unit, a floating point unit and a 256 kB internal second level cache which runs at the CPU clock speed. The combination of high integration within a small form factor makes it possible for a sophisticated 6U board with a comprehensive set of features to carry two additional PMC modules.

Both PMC Slots have a 32-bit/33 MHz PCI interface.

The connection to the CompactPCI bus is achieved using the Intel® transparent 21154 PCI-to-PCI bridge. The CompactPCI bus width is 64-bit at 33 MHz. The CP620-PCIP also provides the functionality of the hot swap capability. Hot swap means that the board can be installed in and removed from a hot swap compliant backplane while the rest of the system is powered up and running.

The local PCI bus runs at a 33 MHz PCI clock frequency and the bus has a 32-bit width.

The CP620 communicates with its environment using two Fast Ethernet interfaces and one RS-232 terminal interface on the front side, or by using an optional rear I/O board, which can provide the 2 Ethernet channels and 4 serial interfaces.

The CP620-PCIP provides the Ethernet channels on J3(CON3), for use with a PICMG 2.16 compliant backplane.

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The Ethernet is realized using the Intel® 82559 Fast Ethernet controller. Full duplex support at both 10 and 100 Mbps is possible.

The serial interfaces are realized with two DUAL UART 16C2850s, which include two 16550 software compatible serial interfaces in one package. They each contain 128 Bytes transmit and 128 Bytes receive FIFO buffers to increase the CPU availability for other operations. These UARTs also provide the hardware control signals for RS-422/485 transmission. If galvanic decoupling needs to be realized, the isolation will have to be effected on the rear I/O board.

The CP620 employs an OS-independent bootloader that enables the loading of any operating system available for the PowerPC®. This bootloader makes an update of the Flash contents and automatically downloads from Flash to SDRAM before booting the OS. For performance reasons, the OS and user programs are started from the SDRAM.

1.3.2 Board-Specific Information

The CP620 is a CompactPCI PowerPC®-based single-board computer specifically designed for use in highly integrated platforms with solid mechanical interfacing for a wide range of industrial environment applications.

- Processor: IBM® PowerPC® 750CX/CXe (Generation 3) with CPU speeds of up to 600 MHz and an integrated FPU
- 256 kB L2 Cache running at CPU speed
- Chipset: Motorola® MPC107
- Compliance with 64-bit CompactPCI Interface 2.0 R3.0 at 33 MHz
- CP620-PCIP with hot swap capability (PICMG 2.1, version 1.0)
- 4HP 6U CompactPCI
- Up to 512 MB SDRAM/100 MHz with ECC
- Up to 8 MB onboard Flash
- One user EEPROM (8192 x 8)/one system EEPROM (8192 x 8)
- CompactFlash expansion port
- 32-pin DIP Memory expansions socket for additional Flash/SRAM/NVSRAM/EPROM
- Two PMC PCI-Bus expansion slots (33 Mhz, 32-bit)
- PMC slots with rear I/O routing
- Onboard interfaces:
- 2 Fast Ethernet interfaces
- 4 serial interfaces/one available on the front panel/all 4 serial interfaces available on rear I/O
- ESD protected and EMI compliant
- Four counters/timer
- Programmable watchdog timer
- Real-time clock
- IPMI compliant baseboard management controller (optional)
- Temperature sensing
- Front panel LED status indicators
- Debug interface, JTAG/COP
- Operating systems: VxWorks, Linux

1.4 Extension Modules

The CP620 has been designed to hold up to two PMC modules and has rear I/O capability.

1.4.1 PMC Modules

PMC modules provide an easy, very flexible way to configure the CP620 for different interfaces. A wide range of PMC modules exists on the market (including Kontron's PMC modules; such as the PMC260, the PMC-HDD1 and PMC251) which can be connected to CP620 via the on-board PMC slots. Up to two of these modules can be placed on the CP620 at the same time.

1.4.2 Rear I/O

All interfaces on the CP620 are also available via the rear I/O connectors J3(CON3) - J5(CON5). These interfaces include four serial ports, two Fast Ethernet ports, the IPMI signals and the rear I/O signals from the PMC modules. If these interfaces are needed on the rear side of a system, a board specific rear I/O Module has to be defined, designed to meet the users' specific requirements.

1.4.3 System Relevant Information

The following system relevant information is general in nature but should still be considered when developing applications using the CP620.

Table 1-1: System Relevant Information

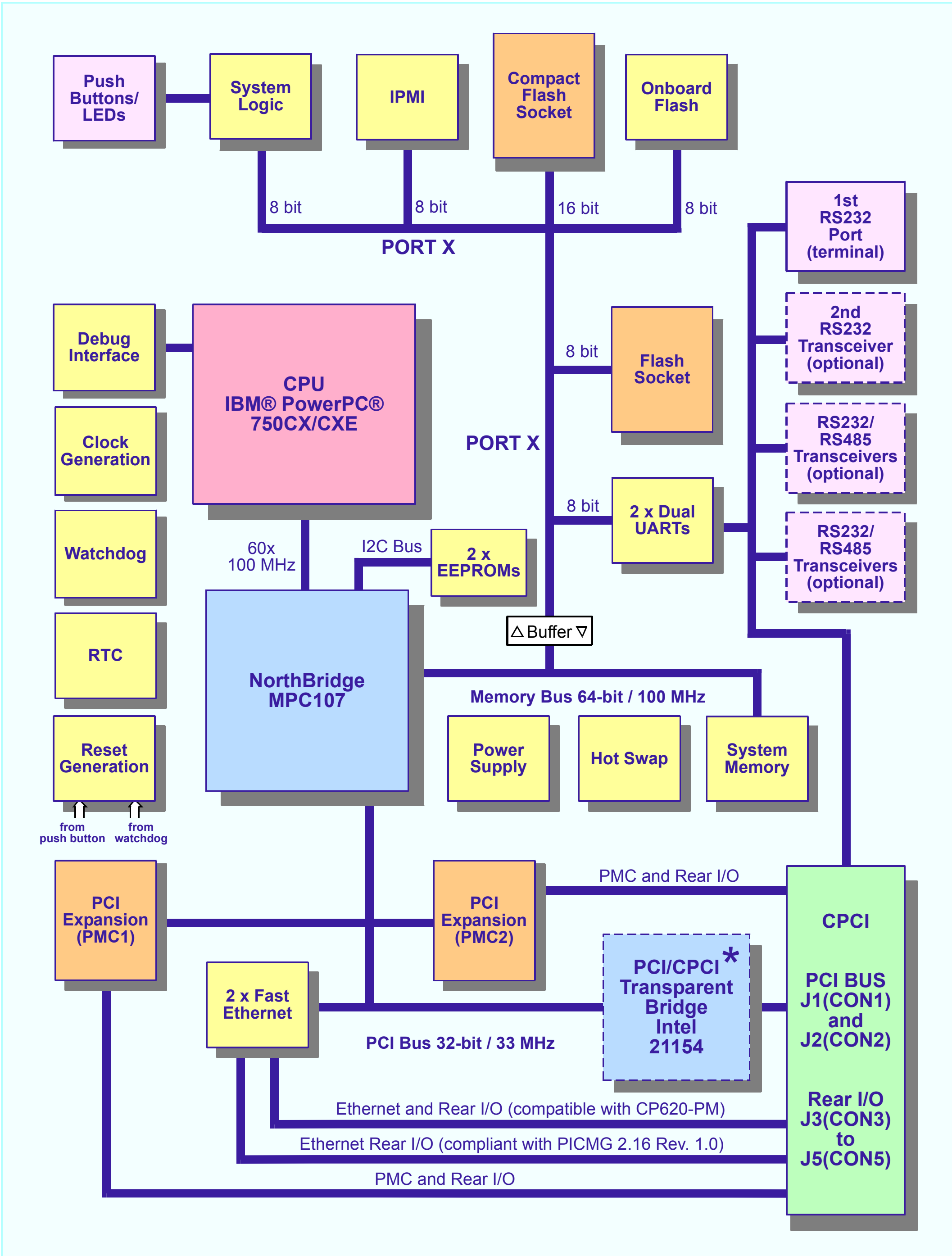
SUBJECT	INFORMATION
System Configuration	A CompactPCI system is made up of at least one system controller (for example CP620, CP603, CP604 or CP612) and up to 7 other I/O boards can be located within one system.
Master/Slave Functionality	The CP620 can operate only as a system master. The CP620-PCIP is a standalone" CPU board and communicates via "Ethernet with its environment
Board Location in the System	The CP620 board must be installed in a system slot of a CPCI backplane. The CP620-PCIP may be installed in every node slot of a PICMG 2.16 backplane
Hot Swap Compatibility	The CP620-PCIP supports all necessary signals to be removed or added while the system remains in a powered-up state.The CP620-PCIP complies with the PICMG 2.1 hot swap specification and the PICMG 2.16 Rev.1.0 specification
Hardware Requirements	The CP620 can be installed in any CompactPCI 6U rack. The CP620-PCIP can be installed in any PICMG 2.16 Rev. 1.0 compliant system.
Operating Systems	The CP620 can operate under the following operating systems: • VxWorks® • Linux Please contact Kontron Modular Computers for further information concerning other operating systems.

1.5 Board Diagrams

The following diagrams provide additional information concerning board functionality and component layout.

1.5.1 Functional Block Diagram

Figure 1-1: Functional Block Diagram



* Not present on CP620-PCIP

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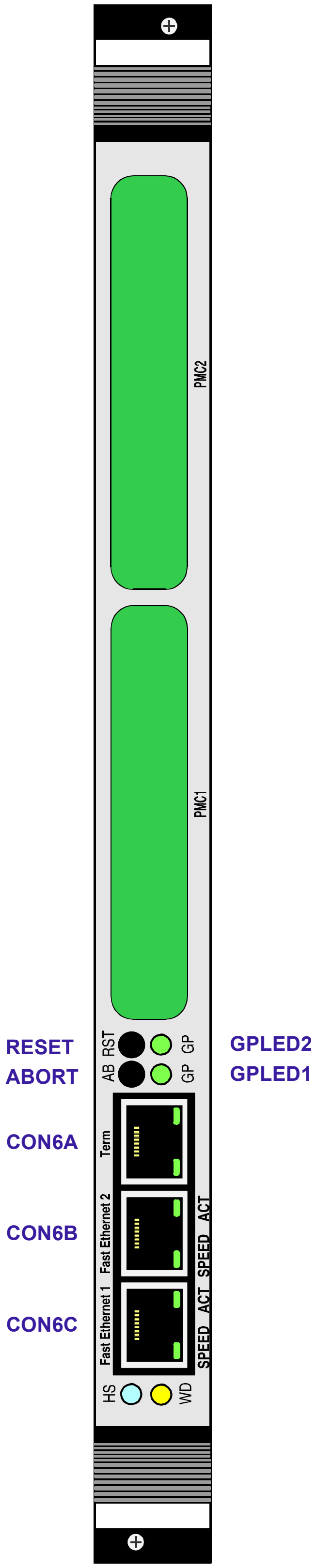
1.5.2 Front Panel

Figure 1-2: CP620 Front Panel



LEGEND:

LEDs

GP	User	(green)
HS	Hot Swap	(blue)
WD	Watchdog	(yellow)

Ethernet LEDs

ACT	Activity	(yellow)
SPEED	Speed	(green)

Switches

RST	Reset
AB	Abort

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1.5.3 Board Layout

Figure 1-3: CP620 Board (Front View)

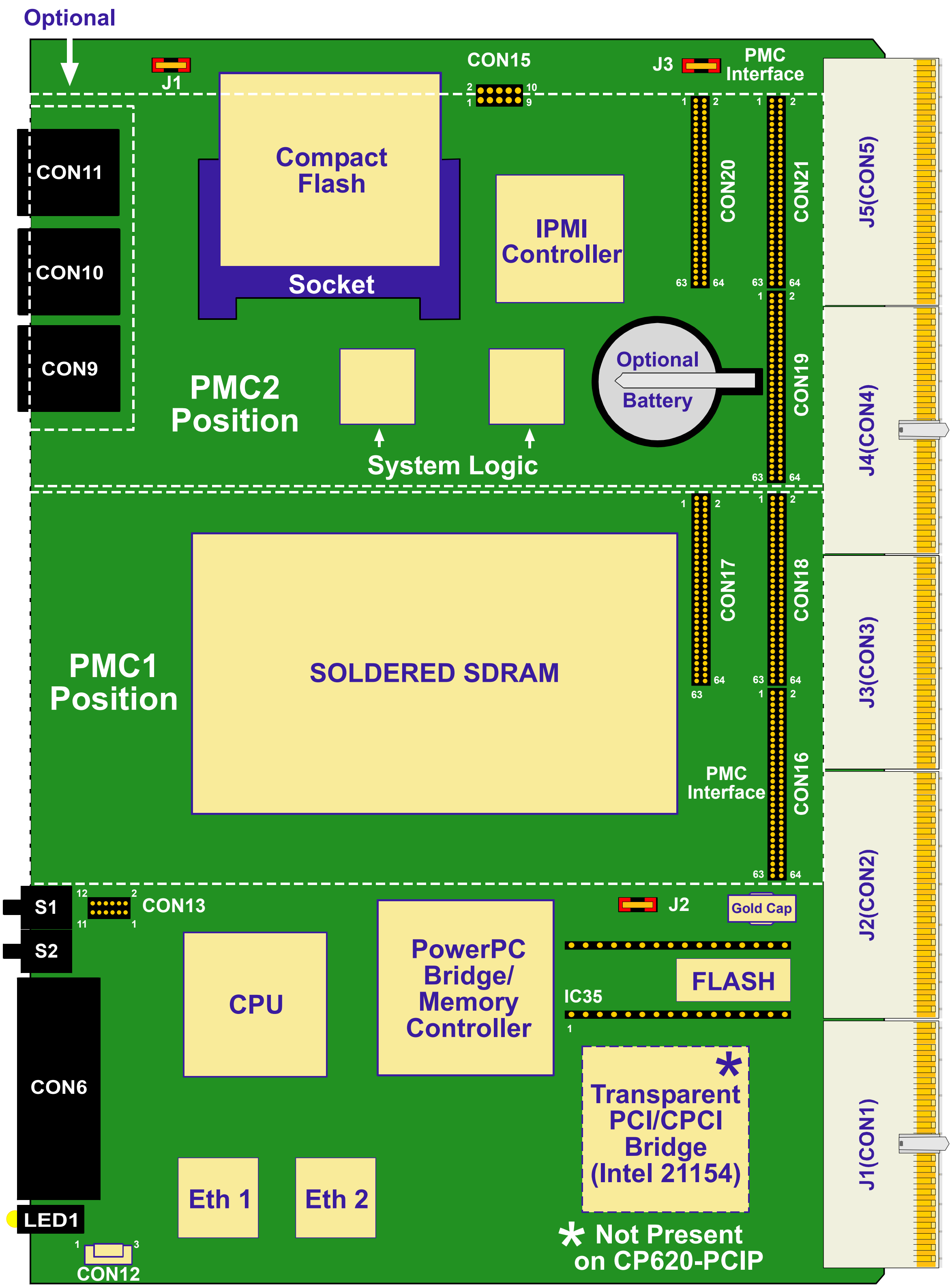

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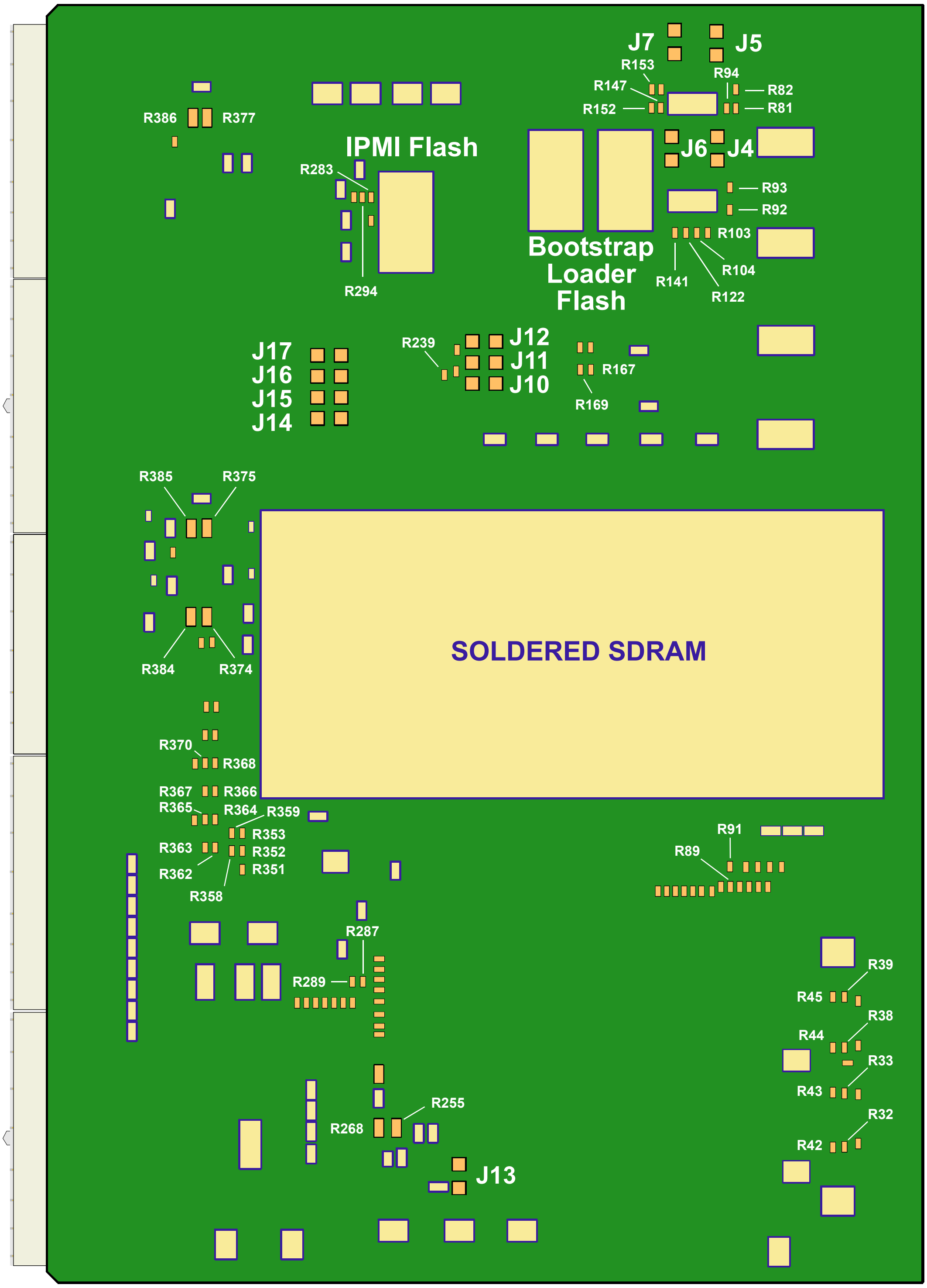
Figure 1-4: CP620 Board (Reverse View)



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1.6 Technical Specifications

Table 1-2: CP620 Main Specifications

	CP620	SPECIFICATIONS
Processor and Related	Processor	IBM® PowerPC® 750CX/CXe with integrated Level 2 cache (256 kB) Clock speed up to 600 MHz/Level 2 cache at CPU speed
	Chipset	Motorola® MPC107 PowerPC®-PCI Bridge/Memory Controller with 100 MHz CPU bus clock speed
	CompactPCI Interface	System Master, compliant with PICMG 2.0 Rev.3.0, CP620-PCIP, compliant with CompactPCI hot swap specification PICMG 2.1 version 1.0 64-bit/33 MHz master interface, universal signaling voltage (3.3V, to fit in 3.3V or 5V bus) Intel® PCI-to-PCI bridge 21154
	Main memory	128 MB to 512 MB of onboard SDRAM (soldered) with ECC support running at 100 MHz 64-bit wide
	Cache Structure	256 KB, 256-bit wide, running at CPU speed
	Watchdog	Software configurable Watchdog generates Exception-Condition/Reset or NMI
	RTC	Real-time clock backed up using Gold Cap with the data retention being about 5 days (optionally, a backup battery is available)
	Temperature Sensor	1x LM75, connected to I2C bus
Peripheral Memory	Flash/Boot device	4/8 MB soldered flash for bootloader and ROMable OS 32-pin DIP600 expansion socket
	SRAM	Support for 256 or 512 kB NVSRAM on DIP600 socket
	EEPROM (I2C)	1 x serial EEPROM for system purpose (8 x 8kB) plus 1 x serial EEPROM for general purpose (8 x 8kB) write protection possible
	Memory Expansion	1x 32-pin DIP600 socket which can be jumpered for use with Flash-, Eprom-, SRAM-Memory 1x CompactFlash Socket Type II (IDE-Mode)

Table 1-2: CP620 Main Specifications (Continued)

	CP620	SPECIFICATIONS
External Interfaces	Fast Ethernet	2 x 10Base-T / 100Base-TX realized with 2 Intel® 82559ER Fast Ethernet controllers CP620: cabling: category 5 two-pair cabling with RJ45 connectors CP620-PCIP: connection via PICMG 2.16 backplane
	CPCI Connectors	CompactPCI connectors J1(CON1), J2(CON2), J3(CON3) and J5(CON5) equipped by default. J4(CON4) optional
	Serial Ports	4 UARTs (16550 compliant) with additional RS-485 support. 128 Byte transmit and 128 Byte receive buffer each The following interfaces are available if the board is used with 2 PMCs: • all 4 UARTs connected to rear I/O, or • 1 x RS-232 interface at the front panel (TERM) + 3 UARTs connected to rear I/O The following interfaces are a#vailable when only one PMC slot is used: • all 4 UARTs connected to rear I/O, or • 1x RS-232 interface at front panel (terminal) + 3 UARTs connected to rear I/O, or • optional (special front panel version): 2x RS-232 + 2x RS-232 / RS-485 (configurable) at front panel
Internal Interfaces	PCI Expansion	2 PMC interfaces, compliant with Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards PMC, P1386.1 / Draft 2.0, 04-APR-1995. PCI master interfaces with 32-bit width and 33 MHz clock. 3.3V / 5.0V compatible. PMC-Rear-IO routing to CPCI connectors J3(CON3) and J5(CON5).
	Debug Interface	JTAG / COP interface for testing purposes (Connector type: SAMTEC FTSH-105-01-L-DV)
	Programming Interface	Second JTAG chain for logic programming
Indicators / Switches	LEDs	1 x LED blue: indicating hot swap status 1 x LED yellow: indicating that “Watchdog Counter” is active 2 x LED green: general purpose LED 2 x LED green (integrated in Ethernet RJ45 jack): Ethernet Link / Activity 2 x LED green (integrated in Ethernet RJ45 jack): Ethernet Speed
	Switches	Two, non-latching, debounced, push button type switches: one for resetting the CPU and the other for aborting the boot process
Monitor and Control	IPMI	Onboard independent IPMI compliant baseboard management (BMC) controller realized with the Qlogic Zircon LT. The Zircon LT BMC controls all onboard voltages, the CPU temperature and optional external fans connected via the rear I/O interface connectors J4(CON4).

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Table 1-2: CP620 Main Specifications (Continued)

	CP620	SPECIFICATIONS
General	Mechanical Conformance	Conforms with IEEE 1101.10
	Power Consumption	400 MHz / 128 MB: 5V / 0.6A; 3.3V / 1.5A 600 MHz / 512 MB: 5V / 0.9A; 3.3V / 1.4A
	Temperature Range	0°C to + 70°C Standard -25ºC to + 75ºC (E1) -40ºC - + 85ºC (E2) -55ºC ... +125ºC storage
	Climatic Humidity	93% RH at 40°C, non-condensing
	Dimensions	233.35mm x 160mm, double-height Eurocard (6U)
	Board Weight	400g
Software	Software / Operating System Support	Initial Boot loader, VxWorks, Linux

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1.7 Standards

The *Kontron Modular Computers'* CompactPCI systems comply with the requirements of the following standards:

Table 1-3: Standards

COMPLIANCE	TYPE	STANDARD	TEST LEVEL
CE	Emission	EN55022 EN61000-6-3	--
	Immission	EN55024 EN61000-6-2	--
	Electrical Safety	EN60950-1	--
Mechanical	Mechanical Dimensions	IEEE 1101.10	--
Environmental and Health Aspects	Vibration (sinusoidal)	IEC60068-2-6	Ruggedized version test parameters: • 10-300 (Hz) frequency range • 2 (g) accelleration • 1 (oct/min) sweep rate • 10 cycles/axis • 3 axis
	Vibration, broad-band random (digital control) and guidance	IEC 60068-2-64	Ruggedized version test parameters: • 20-500Hz, 0.05 (g^2/Hz) PSD • 500-2000Hz, 0.005 (g^2/Hz) PSD • 3,5 (g RMS) acceleration • 30 (min) test time/axis • 3 axis
	Bump	IEC60068-2-29	Ruggedized version test parameters: • 15 (g) acceleration • 11 (ms) pulse duration • 500 bumps per direction • 6 directions • 1 (s) recovery time
	Shock	IEC60068-2-27	Ruggedized version test parameters: • 30 (g) acceleration • 9 (ms) pulse duration • 3 shocks per direction • 6 directions • 5 (s) recovery time
	Climatic Humidity	IEC60068-2-78	93% RH at 40 °C, non-condensing
	WEEE	Directive 2002/96/EC	Waste electrical and electronic equipment
	RoHS	Directive 2002/95/EC	Restriction of the use of certain haz-ardous substances in electrical and electronic equipment

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1.8 Related Publications

The following publications contain information relating to this product.

Table 1-4: Related Publications

PRODUCT	PUBLICATION
CompactPCI Systems and Boards	CompactPCI Specification 2.0, Rev. 3.0 CompactPCI Packet Switching BackplaneSpecification PICMG 2.16 Rev.1.0
	Kontron Modular Computers' CompactPCI System Manual, ID 19954
PMC Add-on Modules and Carriers	Draft standard for Common Mezzanine Card Family: P1386, Draft 2.0
	Draft standard for Physical and Environment Layers for PCI Mezzanine Cards: P1386.1, Draft 2.0
Compact Flash Cards	CF+ and Compact Flash Specification Revision 1.4

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Chapter 2

Functional Description

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2. Functional Description

This chapter presents more detailed board level information about the CP620 System Master whereby the board components and their basic functionality are discussed in general.

2.1 General Information about the CP620

The CP620 is comprised basically of the following:

- CPU
  - PowerPC® G3 (IBM® PowerPC® 750CXe)
- PCI-Bridge/Memory Controller
  - Motorola® MPC107
- Memory
  - System Memory (SDRAM)
  - FLASH
  - FLASH Socket/SRAM Socket
  - FLASH expansion (CompactFlash)
  - Serial EEPROMs
- Interfaces
  - CompactPCI Interface including rear I/O
  - Ethernet Interfaces
  - Serial Interfaces
  - PCI Expansion (PMC)
  - JTAG/COP - Debug interface
- Monitor and Control
  - System Logic
  - Push Buttons/LEDs
  - Watchdog
  - RTC
  - Temperature Sensor
- Hot Swap Circuitry
- IPMI
- JTAG/COP - Debug Interface
- Software

2.2 CPU

The heart of the CP620 is the IBM® PowerPC® 750CX/CXe, a PowerPC® of the "Generation 3" hardware architecture. It combines a powerful processing unit, floating point unit and a 256 kB level 2 cache in one package and this with very low power consumption.

2.2.1 IBM® PowerPC® 750CX/CXe Key Features

This section summarizes the features of the PowerPC® 750CXe's implementation of the PowerPC® architecture. Major features of the PowerPC® 750CXe are as follows.

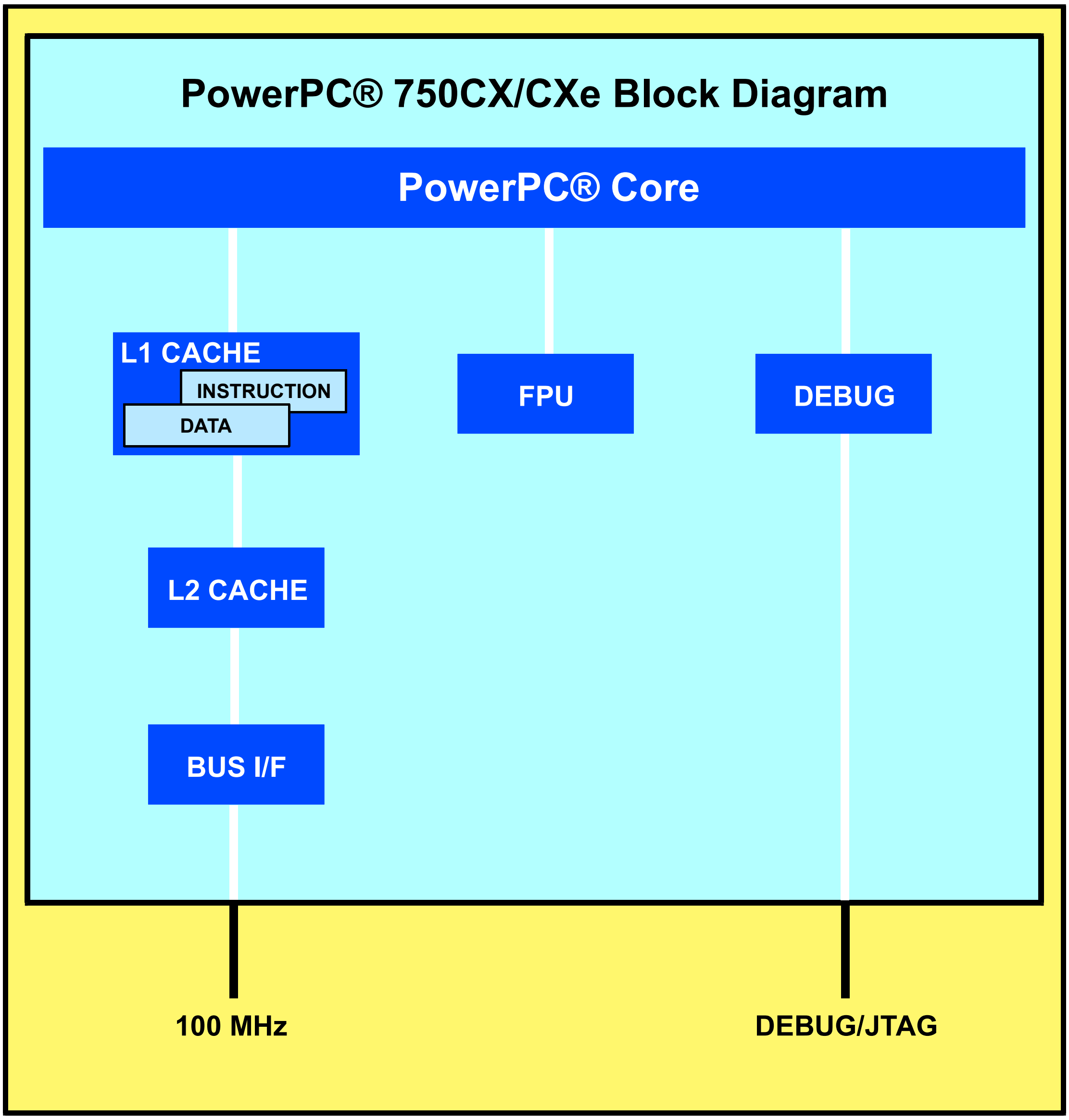
- G3 PowerPC® core
  - Branch processing unit
  - Dispatch unit
  - Decode
  - Load/store unit
  - Fixed-point units
- Floating-point unit
  - Support for IEEE-754 standard single and double precision floating-point arithmetic
  - Optimized for single-precision multiply/add
  - Thirty-two floating point registers, 64-bit wide
  - Enhanced reciprocal estimates
  - 3-cycle latency, 1-cycle throughput, single-precision multiply-add
  - 3-cycle latency, 1-cycle throughput, double-precision add
  - 4-cycle latency, 2-cycle throughput, double-precision multiply-add
  - Hardware support for division
  - Hardware support for denormalized numbers
  - Time deterministic non-IEEE mode
- L1 Cache structure
  - 32K, 32-byte line, 8-way set associative instruction cache
  - 32K, 32-byte line, 8-way set associative data cache
  - Single-cycle cache access
  - Pseudo-LRU replacement
  - Copy-back or write-through data cache (on a page per page basis)
  - 3-state (MEI) memory coherency
  - Hardware support for data coherency
  - Non-blocking instruction and data cache (one outstanding miss under hits)
  - No snooping of instruction cache
- Memory management unit
  - 128 entry, 2-way set associative instruction TLB
  - 128 entry, 2-way set associative data TLB
  - Hardware reload for TLBs
  - 4 instruction BATs and 4 data BATs
  - Virtual memory support for up to 4 exabytes (2^{52}) virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
  - Support for big/little-endian addressing
- Level 2 (L2) cache
  - Internal L2 cache controller and 4K-entry tags; 256K data SRAMs
  - Copy-back or write-through data cache on a page basis, or for all L2
  - 64-byte sectored line size
  - L2 frequency at core speed
  - Onboard ECC

- Bus interface
  - Compatible with 60X processor interface
  - 32-bit address bus
  - 64-bit data bus
- Testability
  - Powerful diagnostic and test interface through common on-chip processor (COP) and IEEE 1149.1 (JTAG) interface

2.2.2 Principal Functional Blocks of the IBM® PowerPC® 750CX/CXe

The diagram below illustrates the principal functional blocks of the IBM® PowerPC® 750CX/CXe chip.

Figure 2-1: Overview of the Main Elements of the IBM® PowerPC® 750CX/CXe



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2.3 PCI-Bridge/Memory Controller

The PCI-Bridge/Memory Controller (also named Northbridge) is used to interface the CPU to memory and a larger number of peripheral busses. On the CP620, the Motorola® MPC107 is used.

The principal features of the MPC107 are used on the CP620 as follows:

- Processor interface
  - 60x compliant bus interface
  - 32-bit address bus, 64-bit data bus supported at 100 MHz
- Memory interface
  - 64-bit 100 MHz bus
  - support of PC100 SDRAM
  - Supports one to four banks 64-, 128- or 256 Mbit SDRAM devices
  - Supports 128 MB to 512 MB SDRAM memory
  - ROM interface, 8 and 16-bits in use
  - Supports ECC
  - Low-voltage TTL logic (LVTTL) interfaces
  - Port X: 8-, 32-bit genera purpose I/O port using ROM controller interface with programmable address strobe timing
- 32-bit PCI interface operating at 33 MHz
  - PCI 2.1-compliant
  - PCI 5.0-V tolerance
  - Support for accesses to PCI memory, I/O, and configuration spaces
  - PCI bus arbitration unit (five request/grant pairs)
  - Address translation unit
- Two channel integrated DMA controller (writes to ROM/Port X not supported)
  - Local-to-local memory
  - PCI-to-PCI memory
  - PCI-to-local memory
  - PCI memory-to-local memory
- I2C controller with full master/slave support (except broadcast all)
- Embedded programmable interrupt controller (EPIC)
  - 16 serial interrupts
  - Four programmable timers
- Dynamic power management - supports 60x nap, doze, sleep, and suspend modes

2.3.1 System Memory (SDRAM)

The main memory of the CP620 consists of four memory banks, equipped with 64 Mbit/128 Mbit or 256 Mbit SDRAM chips (8-bit width), soldered onto the board. This results in a minimum memory size of 128 MB if 2 banks are equipped with 64 Mbit chips. The maximum possible Memory is 512 MB. The SDRAM is soldered onto the board for mechanical stability. It provides ECC support for data critical applications.

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2.3.2 Flash (Onboard Soldered)

Four or eight megabyte of soldered Flash memory accommodates the NetBootLoader software and can be used to store a ROMable operating system and user data. This Flash memory is 8-bit wide and windowed with window sizes of 512 kB.

2.3.3 FLASH Socket/SRAM Socket

The CP620 provides one 32-pin DIL socket on which to place Flash, SRAM, non-volatile SRAM, or other DIL600 devices on the board. Access to this memory is controlled by the on-board logic.

The following devices may be added to the CP620 via the 32-pin DIL600 socket:

- Standard EPROM devices;
- Standard Flash memory of up to 512 kB (e.g. the AMD29F010 and AMD29F040);
- The NV SRAM from Dallas Semiconductor.
- These devices are available in the temperature range -40°C to +85°C for the industrial environment and guarantee a minimum data retention of 10 years (e.g. DS1250Y-100).

2.3.4 Flash Expansion

The CP620 provides a CompactFlash Type II interface which is placed below the upper PMC slot. Its electrical interface (3.3V IDE mode) is provided by the system logic.

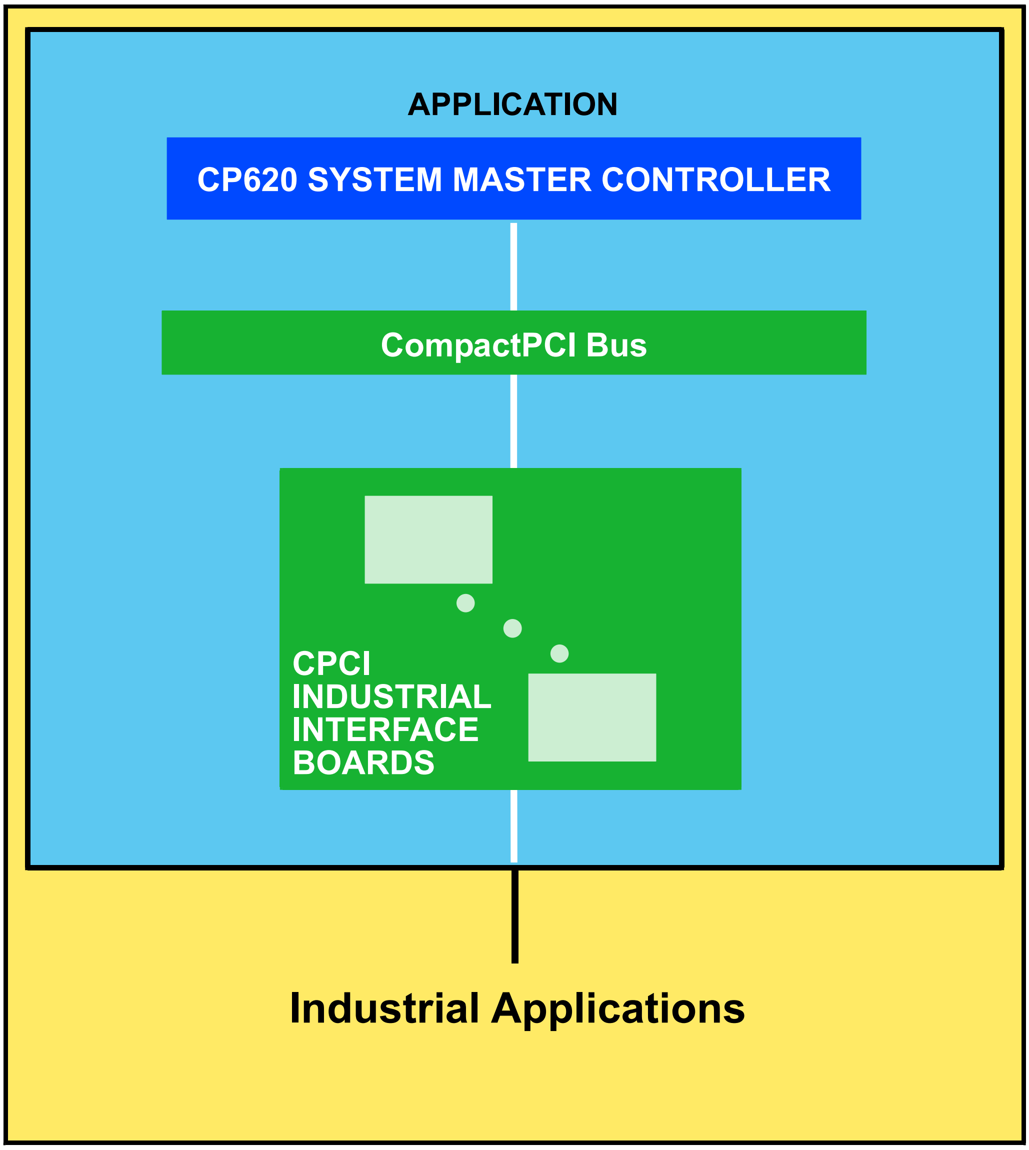
2.3.5 Serial EEPROM

Two 64-Kbit serial EEPROMs are provided, organized as 8192 x 8-bit. One EEPROM is for system purposes; the other is available to the user. Both EEPROMs may be write protected. These EEPROMs are connected to the I2C bus provided by the MPC107.

2.4 System Level Interfacing

The following illustration shows the system level dependencies of a complete CPCI system. The control of the boards on the CPCI bus is maintained by a system master CPU board. Other boards within the system may be either peripheral master CPU boards or simple I/O boards (for example, mass storage devices, field buses etc.)

Figure 2-2: System Level Interfacing



2.5 Board Level Interfacing

The following illustration shows all the possible application interfaces of the CP620.

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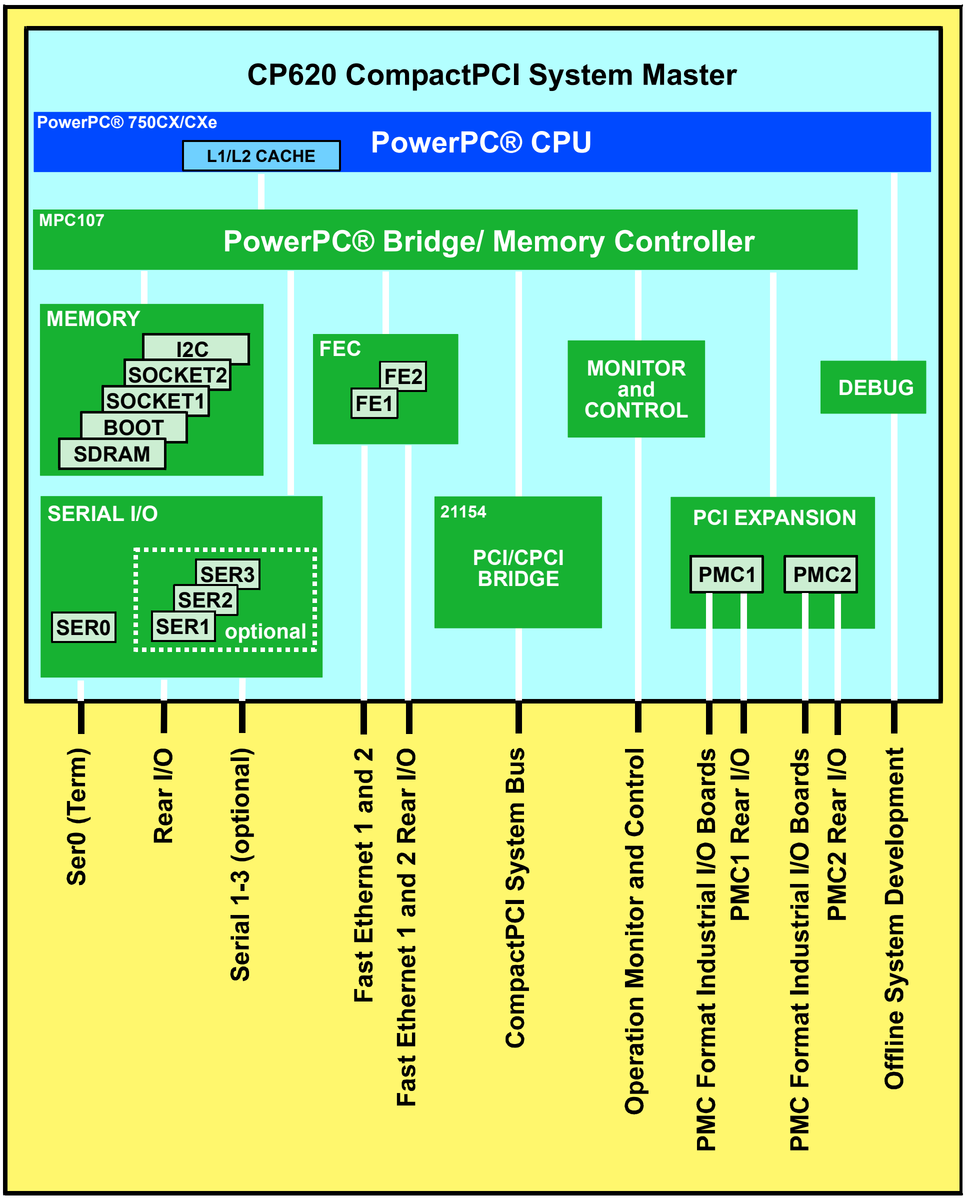
Figure 2-3: Board Level Interfacing



2.6 System Interfaces

2.6.1 CompactPCI Interface including Rear I/O

2.6.1.1 PCI-to-PCI Bridge

The Intel® 21154 bridge is a 64-bit 33 MHz PCI-to-PCI bridge device. It supports up to seven CompactPCI loads through a passive backplane.

The 21154 is a second generation PCI-to-PCI bridge and is fully compliant with the PCI Local Bus Specification Rev. 2.1. The 64-bit interface interoperates transparently with either 64-bit or 32-bit devices.

The PC-to-PCI bridge allows the primary and secondary PCI bus to operate concurrently. A master and target on the same PCI bus can communicate while the other PCI bus is busy.

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2.6.2 CompactPCI Bus Interface

2.6.2.1 CompactPCI Connector Overview

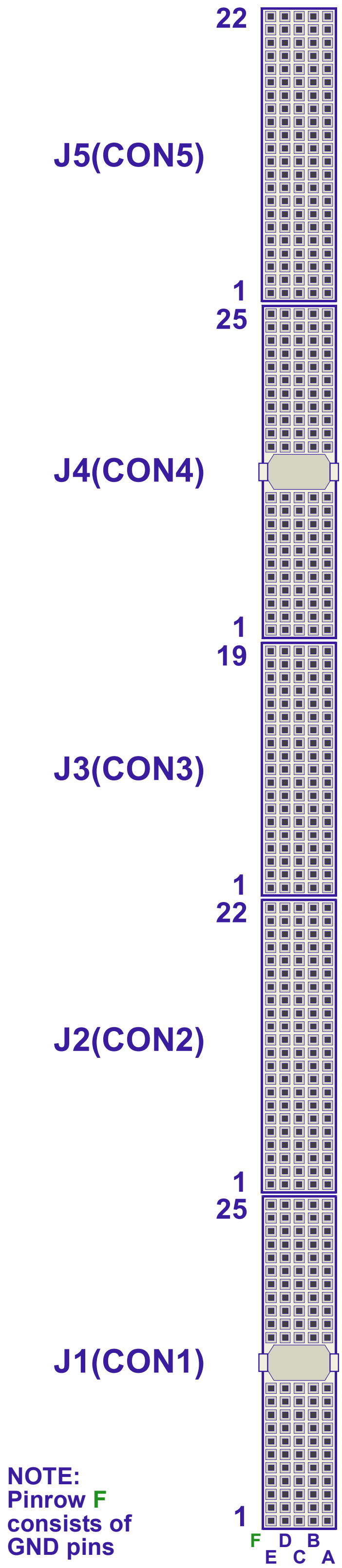
The complete CompactPCI connector configuration comprises five connectors named J1(CON1) to J5(CON5). Their functions are as follows:

- J1(CON1)/J2(CON2): 64-bit CompactPCI interface with PCI bus signals, arbitration, clock and power.
- J3(CON3) and J5(CON5) have rear I/O interface functionality.
- the optional J4(CON4) connector has rear I/O interface functionality.

The CP620 is designed for a CompactPCI bus architecture. The CompactPCI standard is electrically identical to the PCI local bus. However, these systems are enhanced to operate in rugged industrial environments and to support multiple slots.

The CP620-PCIP is hot swappable, which means it may be installed in and removed from a hot swap compliant backplane while the system is powered-up and running. The board may also be used in a standard CompactPCI system without hot swap support.

Figure 2-4: CompactPCI Connectors J1(CON1) - J5(CON5)



2.6.2.2 CompactPCI Connector Keying

CompactPCI connectors support guide lugs to ensure a correct polarized mating. A proper mating is further assured by the use of color coded keys for 3.3V and 5V operation.

Color coded keys prevent inadvertent installation of a 5V peripheral board into a 3.3V slot. The CP620 hot swap board is a 5V version. Backplane connectors are always keyed according to the signaling (VIO) level. Coding key colors are defined as follows:

Table 2-1: Coding Key Colors

SIGNALING VOLTAGE	KEY COLOR
3.3V	Cadmium Yellow
5V	Brilliant Blue
Universal board (5V and 3.3V)	None

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2.6.2.3 CompactPCI Connectors J1(CON1) and J2(CON2) Pinouts

The CP620 interfaces with the PCI bus using two 2 mm x 2 mm pitch female CompactPCI bus connectors, J1(CON1) and J2(CON2).

Table 2-2: CompactPCI Bus Connector J1(CON1) Pinout

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
25	5V	REQ64#	ENUM#	3.3V	5V	GND
24	AD[1]	5V	V(I/O)	AD[0]	ACK64#	GND
23	3.3V	AD[4]	AD[3]	5V	AD[2]	GND
22	AD[7]	GND	3.3V	AD[6]	AD[5]	GND
21	3.3V	AD[9]	AD[8]	M66EN	C/BE[0]#	GND
20	AD[12]	GND	V(I/O)	AD[11]	AD[10]	GND
19	3.3V	AD[15]	AD[14]	GND	AD[13]	GND
18	SERR#	GND	3.3V	PAR	C/BE[1]#	GND
17	3.3V	IPMB SCL	IPMB SDA	GND	PERR#	GND
16	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
15	3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
12-14	Key Area					
11	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND
10	AD[21]	GND	3.3V	AD[20]	AD[19]	GND
9	C/BE[3]#	IDSEL	AD[23]	GND	AD[22]	GND
8	AD[26]	GND	V(I/O)	AD[25]	AD[24]	GND
7	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND
6	REQ0#	PCI_PRESENT#	3.3V	CLK0	AD[31]	GND
5	NC	NC	RST#	GND	GNT0#	GND
4	IPMB PWR	HEALTHY#	V(I/O)	NC	NC	GND
3	INTA#	INTB#	INTC#	5V	INTD#	GND
2	TCK	5V	TMS	TDO	TDI	GND
1	5V	-12V	TRST#	+12V	5V	GND

(plain box)	medium-length pins on front side of backplane
(thick-bordered box)	short pins on front side of backplane
(light blue box)	long pins on front side of backplane
(pink box)	pins connected to V(I/O) via pull-up (no function)

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Table 2-3: CompactPCI Bus Connector J2(CON2) Pinout

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
22	GA4	GA3	GA2	GA1	GA0	GND
21	CLK6	GND	NC	NC	NC	GND
20	CLK5	GND	NC	GND	NC	GND
19	GND	GND	IPMI_SDA	IPMI_SCL	IPMI_ALERT	GND
18	NC	NC	NC	GND	NC	GND
17	NC	GND	PRST#	REQ6#	GNT6#	GND
16	NC	NC	DEG#	GND	NC	GND
15	NC	GND	FAL#	REQ5#	GNT5#	GND
14	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	AD[38]	GND	V(I/O)	AD[37]	AD[36]	GND
12	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	AD[45]	GND	V(I/O)	AD[44]	AD[43]	GND
10	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	AD[52]	GND	V(I/O)	AD[51]	AD[50]	GND
8	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	AD[59]	GND	V(I/O)	AD[58]	AD[57]	GND
6	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	C/BE[5]#	NC	V(I/O)	C/BE[4]#	PAR64	GND
4	V(I/O)	NC	C/BE[7]#	GND	C/BE[6]#	GND
3	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

	medium-length pins on front side of backplane

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2.6.2.4 CPCI Rear I/O Connectors J3(CON3) - J5(CON5) Pinouts

The CP620 provides all I/O signals through the rear I/O connectors J3(CON3), J4(CON4) and J5(CON5).

When the rear I/O module is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus, the rear I/O module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

For the rear I/O feature, a special backplane is necessary. The CP620 with rear I/O is compatible with all standard 6U CompactPCI passive backplanes with rear I/O support.

Table 2-4: CompactPCI Rear I/O Connector J3 (CON3) Pinout

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
19	NC	RIO_-12V	RS485_ECHO	RIO_+12V	RearBatt	GND
18	LPa_DA+	LPa_DA-	GND	NC	NC	GND
17	LPa_DB+	LPa_DB-	GND	NC	NC	GND
16	LPb_DA+	LPb_DA-	GND	NC	NC	GND
15	LPb_DB+	LPb_DB-	GND	NC	NC	GND
14	RIO_3.3V	RIO_3.3V	RIO_3.3V	RIO_VCC	RIO_VCC	GND
13	PMC1IO5	PMC1IO4	PMC1IO3	PMC1IO2	PMC1IO1	GND
12	PMC1IO10	PMC1IO9	PMC1IO8	PMC1IO7	PMC1IO6	GND
11	PMC1IO15	PMC1IO14	PMC1IO13	PMC1IO12	PMC1IO11	GND
10	PMC1IO20	PMC1IO19	PMC1IO18	PMC1IO17	PMC1IO16	GND
9	PMC1IO25	PMC1IO24	PMC1IO23	PMC1IO22	PMC1IO21	GND
8	PMC1IO30	PMC1IO29	PMC1IO28	PMC1IO27	PMC1IO26	GND
7	PMC1IO35	PMC1IO34	PMC1IO33	PMC1IO32	PMC1IO31	GND
6	PMC1IO40	PMC1IO39	PMC1IO38	PMC1IO37	PMC1IO36	GND
5	PMC1IO45	PMC1IO44	PMC1IO43	PMC1IO42	PMC1IO41	GND
4	PMC1IO50	PMC1IO49	PMC1IO48	PMC1IO47	PMC1IO46	GND
3	PMC1IO55	PMC1IO54	PMC1IO53	PMC1IO52	PMC1IO51	GND
2	PMC1IO60	PMC1IO59	PMC1IO58	PMC1IO57	PMC1IO56	GND
1	RIO_V(I/O)	PMC1IO64	PMC1IO63	PMC1IO62	PMC1IO61	GND

Warning!

The RIO_XXX signals are power supply **OUTPUTS** to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module.

Failure to comply with the above will result in damage to your board.

Table 2-5: CompactPCI Rear I/O Connector J4(CON4) Pinout

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
25	VCC	NC	JPO	RIO_3.3V	RIO_VCC	GND
24	NC	NC	NC	NC	NC	GND
23	RIO_3.3V	NC	JP1	RIO_VCC	NC	GND
22	NC	NC	NC	NC	NC	GND
21	RIO_3.3V	NC	JP2	NC	J2ALERT	GND
20	NC	NC	NC	J2SCL	J2SDA	GND
19	RIO_3.3V	NC	NC	NC	IPMIGPIO2	GND
18	NC	NC	NC	PWM1	PWM0	GND
17	RIO_3.3V	IPMI_3.3V	SPLED1	NC	Tach_IN3	GND
16	NC	NC	NC	Tach_IN2	Tach_IN1	GND
15	RIO_3.3V	IPMI_3.3V	ACLED1	NC	Tach_IN0	GND
12-14	Key Area					
11	NC	IPMI_VCC	LILED1	NC	CONN_ID_DRV	GND
10	NC	NC	NC	ID_XMIT_EN	CONN_ID1	GND
9	NC	IPMI_VCC	SPLED2	NC	CONN_ID0	GND
8	NC	GND	NC	XMIT_EN	UART0_RI	GND
7	GND	NC	ACLED2	NC	UART0_RTS	GND
6	NC	NC	NC	UART0_DCD	UART0_CTS	GND
5	GND	GND	LILED2	UART0_DOUT	UART0_DIN	GND
4	NC	NC	NC	GND	GND	GND
3	NC	NC	GND	NC	LED1	GND
2	NC	NC	GND	NC	LED2	GND
1	RIO_VCC	RIO_-12V	GND	RIO_+12V	RIO_VCC	GND

IPMI signals

Warning!

The RIO_XXX signals are power supply **OUTPUTS** to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module.

Failure to comply with the above will result in damage to your board.

Table 2-6: CompactPCI Rear I/O Connector J5(CON5) Pinout

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
22	PMC2IO5	PMC2IO4	PMC2IO3	PMC2IO2	PMC2IO1	GND
21	PMC2IO10	PMC2IO9	PMC2IO8	PMC2IO7	PMC2IO6	GND
20	PMC2IO15	PMC2IO14	PMC2IO13	PMC2IO12	PMC2IO11	GND
19	PMC2IO20	PMC2IO19	PMC2IO18	PMC2IO17	PMC2IO16	GND
18	PMC2IO25	PMC2IO24	PMC2IO23	PMC2IO22	PMC2IO21	GND
17	PMC2IO30	PMC2IO29	PMC2IO28	PMC2IO27	PMC2IO26	GND
16	PMC2IO35	PMC2IO34	PMC2IO33	PMC2IO32	PMC2IO31	GND
15	PMC2IO40	PMC2IO39	PMC2IO38	PMC2IO37	PMC2IO36	GND
14	PMC2IO45	PMC2IO44	PMC2IO43	PMC2IO42	PMC2IO41	GND
13	PMC2IO50	PMC2IO49	PMC2IO48	PMC2IO47	PMC2IO46	GND
12	PMC2IO55	PMC2IO54	PMC2IO53	PMC2IO52	PMC2IO51	GND
11	PMC2IO60	PMC2IO59	PMC2IO58	PMC2IO57	PMC2IO56	GND
10	RIO_V(I/O)	PMC2IO64	PMC2IO63	PMC2IO62	PMC2IO61	GND
9	Eth-TDN2	Eth-RDN2	S1RXD	Eth-TDN1	Eth-RDN1	GND
8	Eth-TNP2	Eth-RDP2	S1TXD	Eth-TDP1	Eth-RDP1	GND
7	RS232_2	RS232_1	S1RTS	S3RIN	RIO_3.3V	GND
6	S1DTR	S1CTS	S1DSR	S1DCD	S1RIN	GND
5	S2RXD	S2TXD	S2RTS	S2DTR	S3TXD	GND
4	S2DSR	S2DCD	S2RIN	S2CTS	S3RXD	GND
3	S4DTR	S4CTS	S4DSR	GPLED	S3DTR	GND
2	S4RTS	S4RIN	S4RXD	S3DSR	S3DCD	GND
1	S4DCD	P3RST	S4TXD	S3CTS	S3RTS	GND

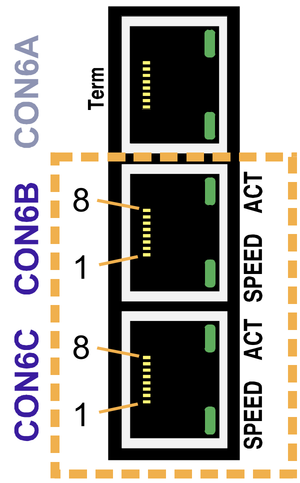
Warning!

The RIO_XXX signals are power supply **OUTPUTS** to supply the rear I/O module with power. These pins **MUST NOT** be connected to any other power source, either within the backplane itself or within a rear I/O module.

Failure to comply with the above will result in damage to your board.

2.6.3 Fast Ethernet

Figure 2-5: Ethernet/Fast Ethernet Connector



The CP620 board includes two 10BASE-T/100BASE-TX Ethernet ports based on the Intel® 82559ER Fast Ethernet PCI Bus Controller. The controller contains two receive and transmit FIFO buffers that prevent data overruns or underruns while waiting for access to the PCI bus.

The Ethernet connectors are realized as RJ45 twisted-pair connectors. The interfaces provide automatic detection and switching between 10Base-T and 100Base-TX data transmission. The two Ethernet channels may be configured via the NetBootLoader setting or the rear I/O configuration register for front I/O or rear I/O. The standard software configuration is front I/O.

Note ...

The CP620-PCIP provides the Ethernet interface only on the rear I/O connector J3(CON3)/P3. Therefore, the Ethernet connectors CON6B and CON6C must not be connected. A protective dummy plug is provided which should protect the user from incorrect usage; please do not remove this plug.

2.6.3.1 RJ45 Connectors CON6B and CON6C Pinouts

The CON6B and CON6C connectors supply the 10Base-TX/100Base-TX interfaces to the Ethernet controller.

Table 2-7: RJ45 Connectors CON6B and CON6C Pinouts

RJ45	SIGNAL	FUNCTION
1	TX+	Transmit +
2	TX-	Transmit -
3	RX+	Receive +
4	NC	--
5	NC	--
6	RX-	Receive -
7	NC	--
8	NC	--

2.6.3.2 Ethernet LED Status

The LEDs located within the Ethernet connectors have the following functions:

ACT: This LED monitors network connection and activity. The LED lights up when network packets are sent or received through the RJ45 port. When this LED is not lit it means that either the computer is not sending or receiving network data or that the cable connection is faulty.

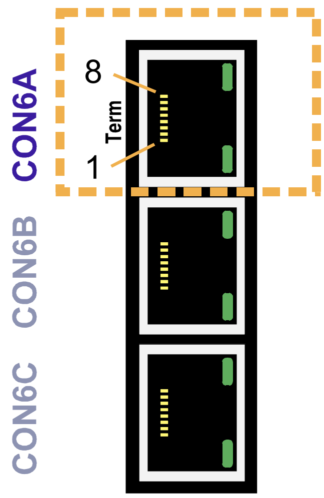
SPEED: This LED lights up to indicate a successful 100Base-TX connection. When not lit the connection is operating at 10Base-T.

2.6.4 Serial Interfaces

The CP620 provides up to four 16550 compliant serial interfaces. These interfaces are realized by two dual-UARTS from EXAR, the 16C2850, which also provide half-duplex control for RS-485 interfacing. One part of each UART pair provides 128 Bytes transmit buffer and 128 Bytes receive buffer per channel and so it reduces the bandwidth requirements of the CPU. It has independent transmit and receive UART control signals and four selectable receive FIFO interrupt trigger levels. The UARTs provide support for various character lengths (5,6,7,8) with even or odd or no parity.

The four serial interfaces on the CP620 can be divided into 3 groups:

Figure 2-6: Front Panel Serial Connector



Group 1 (serial interface 1/TERM): This interface is available with RS-232 levels (TERM) on the front panel or with TTL levels on the rear I/O connector J5(CON5). The direction of this interface can be programmed via the register-setting in the interface route register. Additionally, the interface will be routed to the front panel if the jumper J1 is set (highest priority). The default configuration is front I/O.

Group 2 (serial interface 2): This interface is available with TTL levels on the REAR-IO connector. A special board variant (1 PMC version) also provides this interface with RS-232-levels on the front panel. The direction of this interface can be programmed via the register-setting within the interface route register. The default setting is disabled.

Group 3 (serial interfaces 3 and 4): These interfaces are available with TTL level on the rear I/O connectors. A special board variant (1 PMC version) also provides these interfaces as RS-232 interfaces or RS-485/RS-422 interfaces on the front panel. The direction and type of interface can be programmed via the register setting in the interface route register.

RS-422 configuration:

The RS-422 interface uses two differential data pairs RX and TX for communication (Full-Duplex).

RS-485 configuration:

The RS-485 interface uses one differential data pair. It differs from the RS-422 mode in that it provides the ability to transmit and receive over the same wire. The RTS signal is used to distinguish between receiving and sending data.

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2.6.4.1 Serial interface 1 Pinout (TERM)

Figure 2-7: Cabling of 8-Pin CON6A and 9-Pin Connector on PC Side

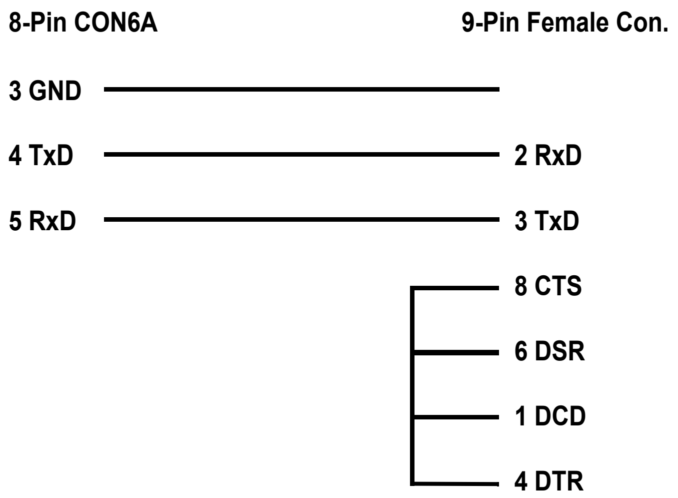


Table 2-8: RJ45 Connector CON6A Pinout

PIN	SIGNAL
1	DSR
2	RTS
3	GND
4	TXD
5	RXD
6	DCD
7	CTS
8	DTR

2.6.4.2 Serial Interfaces 2, 3 and 4 Pinout

Table 2-9: Optional CON9, CON10, CON11 (RJ45 Connector) Pinout

PIN	RS-232 SIGNALS	RS-485 HALF DUPLEX	RS-422 FULL DUPLEX
1	DSR	NC	-RxD
2	RTS	NC	NC
3	GND	GND	GND
4	TXD	+TRXD	-TxD
5	RXD	NC	NC
6	DCD	NC	+RxD
7	CTS	-TRXD	+TxD
8	DTR	NC	NC

Note ...

CON9 carries only the RS-232 signals.

If these interfaces are connected via rear I/O, the RS-232 or RS-485 transceivers must be realized on the rear I/O board.

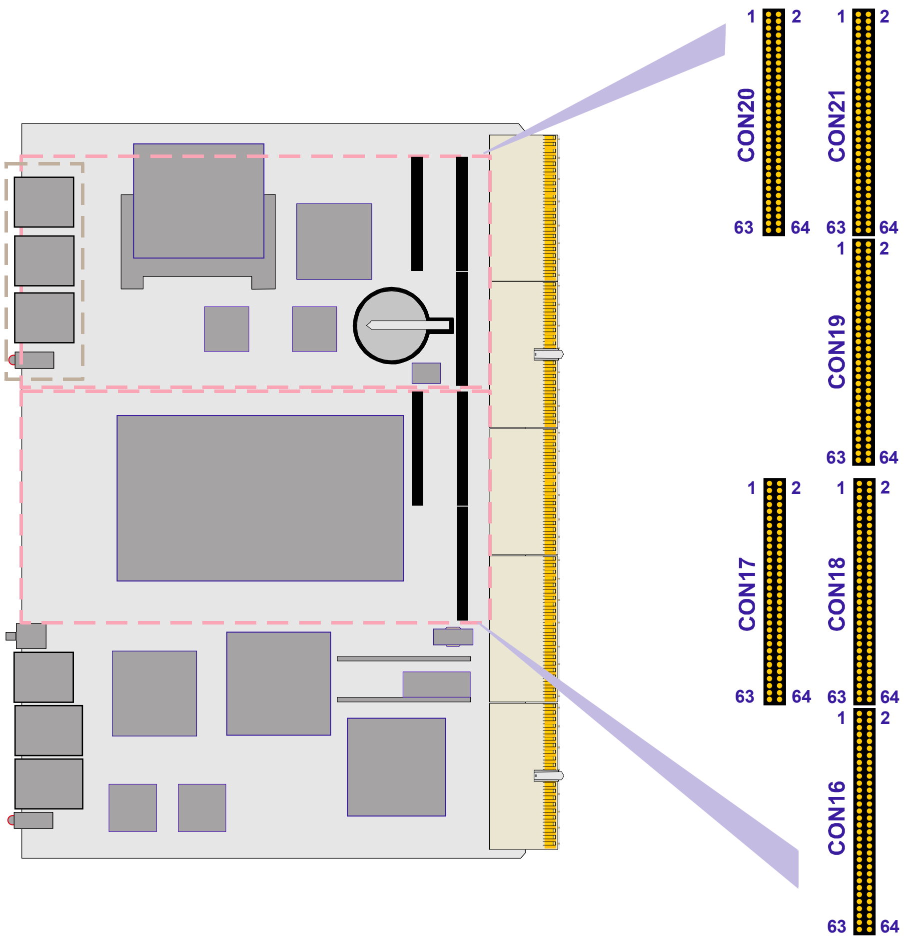
The RS-485 interfaces on the front panel or not galvanically isolated.

2.6.5 PMC Interfaces

For flexible and easy configuration two onboard PMC sockets are available. The connectors CON17, CON20 (Jn1/Pn1) and CON18, CON21 (Jn2/Pn2) provide the signals for the 32-bit PCI bus. The 64-bit interface for the PMC interface is not implemented. User defined I/O signals are supported and are connected to the CompactPCI rear I/O connectors J3(CON3) and J5(CON5).

This interface has been designed to comply with the IEEEP1386.1 specification which defines a PCI electrical interface for the CMC (Common Mezzanine Card) form factor. The CP620 provides for either a 5V or 3.3V PMC PCI signaling environment.

Figure 2-8: PMC Connectors CON16, 17 and 18 and CON19, 20 and 21



Note ...

The PMC rear I/O signals from CON16 are routed to CompactPCI connector J3(CON3), whose pinout is provided in Table 2-4.

The PMC rear I/O signals from CON19 are routed to CompactPCI connector J5(CON5), whose pinout is provided in Table 2-7.

2.6.5.1 PMC Connectors CON17/20 and CON18/21 Pinouts

Table 2-10:PMC Connectors CON17/20 and CON18/21 Pinouts

Jn1 (CON17/CON20)				Jn2 (CON18/CON21)			
SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL
Signal	1	2	-12V	+12V	1	2	Signal
Ground	3	4	Signal	Signal	3	4	Signal
Signal	5	6	Signal	Signal	5	6	Ground
BUSMODE1#	7	8	+5V	Ground	7	8	Signal
Signal	9	10	Signal	Signal	9	10	Signal
Ground	11	12	Signal	BUSMODE2#	11	12	+3.3V
Signal	13	14	Ground	Signal	13	14	BUSMODE3#
Ground	15	16	Signal	+3.3V	15	16	BUSMODE4#
Signal	17	18	+5V	Signal	17	18	Ground
V (I/O)	19	20	Signal	Signal	19	20	Signal
Signal	21	22	Signal	Ground	21	22	Signal
Signal	23	24	Ground	Signal	23	24	+3.3V
Ground	25	26	Signal	Signal	25	26	Signal
Signal	27	28	Signal	+3.3V	27	28	Signal
Signal	29	30	+5V	Signal	29	30	Ground
V (I/O)	31	32	Signal	Signal	31	32	Signal
Signal	33	34	Ground	Ground	33	34	Signal
Ground	35	36	Signal	Signal	35	36	+3.3V
Signal	37	38	+5V	Ground	37	38	Signal
Ground	39	40	Signal	Signal	39	40	Ground
Signal	41	42	Signal	+3.3V	41	42	Signal
Signal	43	44	Ground	Signal	43	44	Ground
V (I/O)	45	46	Signal	Signal	45	46	Signal
Signal	47	48	Signal	Ground	47	48	Signal
Signal	49	50	+5V	Signal	49	50	+3.3V
Ground	51	52	Signal	Signal	51	52	Signal
Signal	53	54	Signal	+3.3V	53	54	Signal
Signal	55	56	Ground	Signal	55	56	Ground
V (I/O)	57	58	Signal	Signal	57	58	Signal
Signal	59	60	Signal	Ground	59	60	Signal
Signal	61	62	+5V	Signal	61	62	+3.3V
Ground	63	64	Signal	Ground	63	64	Signal

Table 2-11: PMC Connectors CON16 and CON19 Pinouts

CON16 (J14)				CON19 (J24)			
SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL
PMC1IO1	1	2	PMC1IO2	PMC2IO1	1	2	PMC2IO2
PMC1IO3	3	4	PMC1IO4	PMC2IO3	3	4	PMC2IO4
PMC1IO5	5	6	PMC1IO6	PMC2IO5	5	6	PMC2IO6
PMC1IO7	7	8	PMC1IO8	PMC2IO7	7	8	PMC2IO8
PMC1IO9	9	10	PMC1IO10	PMC2IO9	9	10	PMC2IO10
PMC1IO11	11	12	PMC1IO12	PMC2IO11	11	12	PMC2IO12
PMC1IO13	13	14	PMC1IO14	PMC2IO13	13	14	PMC2IO14
PMC1IO15	15	16	PMC1IO16	PMC2IO15	15	16	PMC2IO16
PMC1IO17	17	18	PMC1IO18	PMC2IO17	17	18	PMC2IO18
PMC1IO19	19	20	PMC1IO20	PMC2IO19	19	20	PMC2IO20
PMC1IO21	21	22	PMC1IO22	PMC2IO21	21	22	PMC2IO22
PMC1IO23	23	24	PMC1IO24	PMC2IO23	23	24	PMC2IO24
PMC1IO25	25	26	PMC1IO26	PMC2IO25	25	26	PMC2IO26
PMC1IO27	27	28	PMC1IO28	PMC2IO27	27	28	PMC2IO28
PMC1IO29	29	30	PMC1IO30	PMC2IO29	29	30	PMC2IO30
PMC1IO31	31	32	PMC1IO32	PMC2IO31	31	32	PMC2IO32
PMC1IO33	33	34	PMC1IO34	PMC2IO33	33	34	PMC2IO34
PMC1IO35	35	36	PMC1IO36	PMC2IO35	35	36	PMC2IO36
PMC1IO37	37	38	PMC1IO38	PMC2IO37	37	38	PMC2IO38
PMC1IO39	39	40	PMC1IO40	PMC2IO39	39	40	PMC2IO40
PMC1IO40	41	42	PMC1IO42	PMC2IO41	41	42	PMC2IO42
PMC1IO43	43	44	PMC1IO44	PMC2IO43	43	44	PMC2IO44
PMC1IO45	45	46	PMC1IO46	PMC2IO45	45	46	PMC2IO46
PMC1IO47	47	48	PMC1IO48	PMC2IO47	47	48	PMC2IO48
PMC1IO49	49	50	PMC1IO50	PMC2IO49	49	50	PMC2IO50
PMC1IO51	51	52	PMC1IO52	PMC2IO51	51	52	PMC2IO52
PMC1IO53	53	54	PMC1IO54	PMC2IO53	53	54	PMC2IO54
PMC1IO55	55	56	PMC1IO56	PMC2IO55	55	56	PMC2IO56
PMC1IO57	57	58	PMC1IO58	PMC2IO57	57	58	PMC2IO58
PMC1IO59	59	60	PMC1IO60	PMC2IO59	59	60	PMC2IO60
PMC1IO61	61	62	PMC1IO62	PMC2IO61	61	62	PMC2IO62
PMC1IO63	63	64	PMC1IO64	PMC2IO63	63	64	PMC2IO64

2.6.6 CompactFlash

To enable highly flexible flash extension a CompactFlash (CF) type II socket is available.

CF is a very small removable mass storage device. It provides IDE functionality compatible with the 16-bit ATA/ATAPI-4 interface. CF cards are also available for data storage using the Microdrive harddisk from IBM with up to 1 GB capacity.

The board supports both CF types (type I and type II). The only difference between CF type I and CF type II cards is the card thickness. CF type I is 3.3 mm thick and CF type II cards are 5 mm thick. A CF type I card will operate in a CF type I or CF type II slot. A CF type II card will only fit in a CF type II slot. The electrical interfaces are identical. CompactFlash is available in both CF type I and CF type II cards. The IBM® Microdrive™ is a CF type II card.

Table 2-12: CompactFlash Connector Pinout

PIN	SIGNAL	PIN	SIGNAL
1	GND	26	NC (CD1)
2	D03	27	D11
3	D04	28	D12
4	D05	29	D13
5	D06	30	D14
6	D07	31	D15
7	IDE_CS0	32	IDE_CS1
8	GND (A10)	33	NC (VS1)
9	GND (ATASEL)	34	DIOR
10	GND (A09)	35	DIOW
11	GND (A08)	36	WE
12	GND (A07)	37	INTRQ
13	VCC	38	VCC
14	GND (A06)	39	CSEL
15	GND (A05)	40	NC (VS2)
16	GND (A04)	41	Reset
17	GND (A03)	42	IORDY
18	A02	43	INPACK
19	A01	44	VCC
20	A00	45	NC (ACTIVE)
21	D00	46	PDIAG
22	D01	47	D08
23	D02	48	D09
24	NC (IOCS16)	49	D10
25	NC (CD2)	50	GND

2.6.7 Test and Program Development

2.6.7.1 DEBUG Interface and Pinout

A JTAG/COP interface is provided on the CP620 for software debugging. The CPU can be accessed using an emulator probe via CON13. It provides all the signals required for control of the CPU via the common on-chip processor (COP).

Figure 2-9: DEBUG Connector CON13

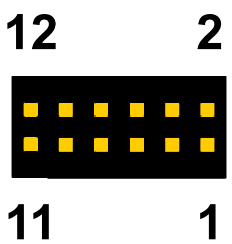


Table 2-13: DEBUG Connector CON13 Pinout

PIN	SIGNAL	DESCRIPTION	I/O
1	TDI	Input serial data	O
2	TDO	Output serial data	I
3	CKSTP_IN	Checkstop in	I
4	TRST	Test reset	I
5	TMS	Command type	I
6	TCK	Debug clock	I
7	HRESET	Hard reset	I
8	SRESET	Soft reset	I
9	GND	Ground	O
10	CHKSTP	Checkstop out	--
11	+2.5V	+2.5V	--
12	NC	--	--

2.6.7.2 JTAG/ISP Interface and Pinout

CON15 provides JTAG/ISP signals for programming the system logic chips and is reserved for factory use only. This interface utilizes a connector which is physically identical with the Debug interface.

Figure 2-10:JTAG Connector CON15

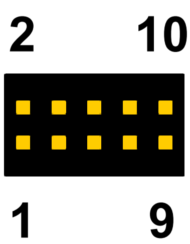


Table 2-14: JTAG Connector CON15 Pinout

PIN	SIGNAL	PIN	SIGNAL
1	TCK	2	GND
3	TDO	4	VCC
5	TMS	6	GND
7	OE_CLKS	8	N/C
9	TDI	10	GND

Note ...

This connector is reserved for factory use only. The description of this connector is provided for information purposes.

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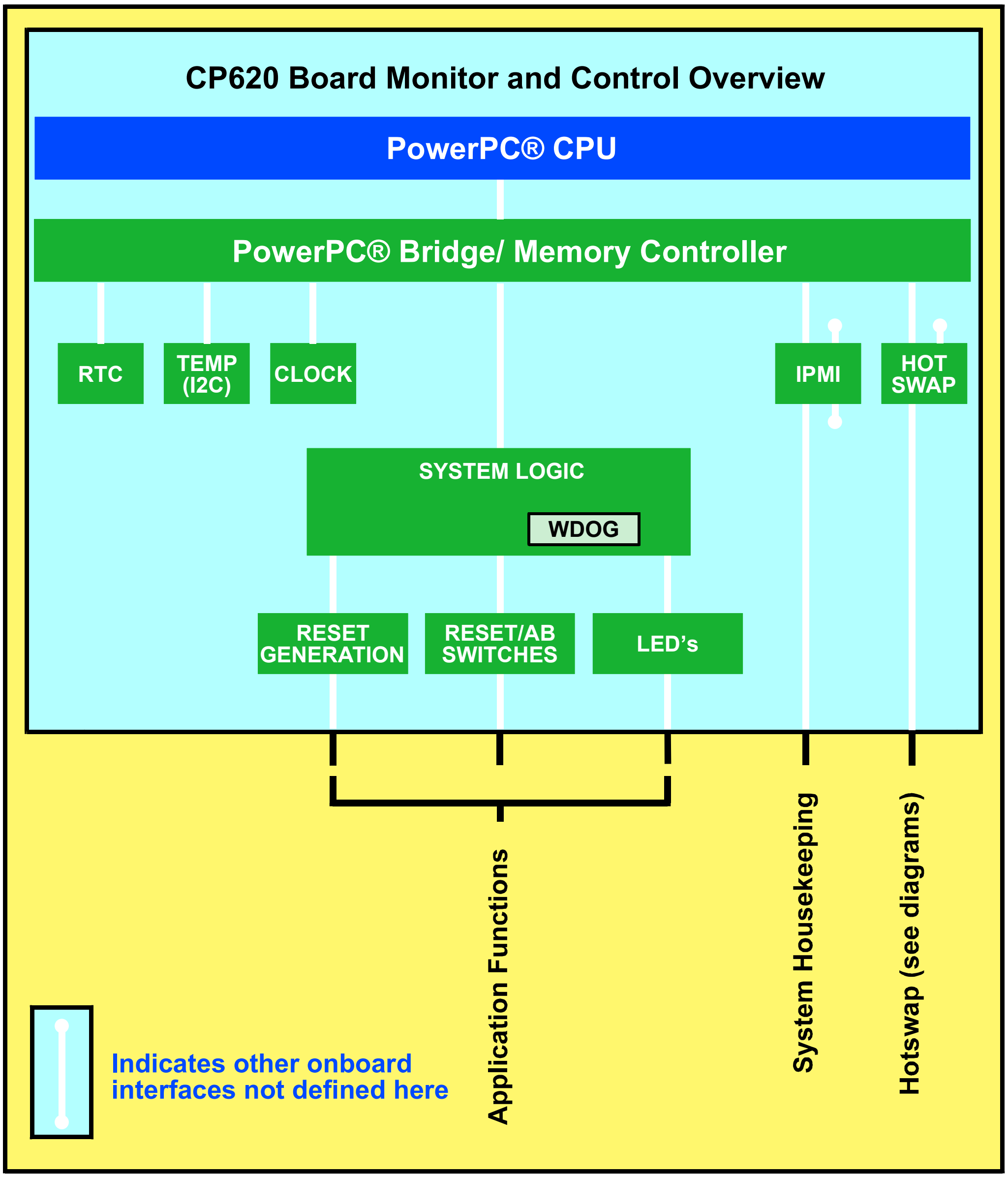
2.6.8 Non-System Relevant Connectors

CON12 is non-system relevant. It is used to connect the hot swap handle switch.

2.7 Monitor and Control (M/C)

Monitor and Control functions are divided essentially into pre-operation and operation. Pre-operation M/C deals with memory configuration aspects, board jumper configurations, and system requirements. Operation M/C covers direct operator interfaces, register handling, and the use of clocks, timers, and counters.

Figure 2-11: Monitor and Control Overview



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2.7.1 Watchdog Timer

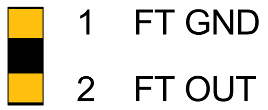
A watchdog timer is available which (when enabled) on timeout either forces a non-maskable interrupt (NMI) to be generated or causes a system reset to occur (refer to chapter 4 for configuration details). It is also possible to generate, as a first step, an NMI and then, as a second step, a system reset (in Cascade mode).The watchdog timing has four possible settings: 0.5, 1.0, 1.5, and 2.0 seconds. After selecting the timeout value and routing (NMI or reset) the watchdog can be enabled. Once enabled, the watchdog must be continuously retriggered or a timeout will occur. When the watchdog timer is enabled, it cannot be stopped or reprogrammed except by resetting the system. The yellow watchdog LED (W) indicates the enabling status of the watchdog. Prior to the watchdog being enabled it is off. After enabling it comes on and remains on until a system reset occurs.

2.7.2 Real-Time Clock (STC M41T56)

A separate hardware real-time clock (RTC) is incorporated on the CP620 board which provides clock information via the I²C bus for application use. An eight byte wide register (refer to chapter 4 for description) is available for accessing, setting, and starting the RTC. The RTC must be initialized prior to its use whereby settings are possible for seconds, minutes, hours, day, date, month, year, and calibration information. Continuous clock operation (even with system power off) is possible through the use of a rechargeable Gold Cap, or alternately, lithium battery buffering is possible. Accuracy of the RTC is 35 ppm whereby temperature compensation can be adjusted in steps of +4.068 or -2.034 ppm per software using the onboard digital temperature sensor (LM75).

For calibration purposes the RTC can also generate a 512 Hz test signal which is made available at test jack J2 (figure 1-3 indicates the location of J2 on the board). Please refer to the datasheet of the ST M41T56 for more information concerning calibration.

Figure 2-12: RTC J2 Pinout



2.7.3 Reset/Abort

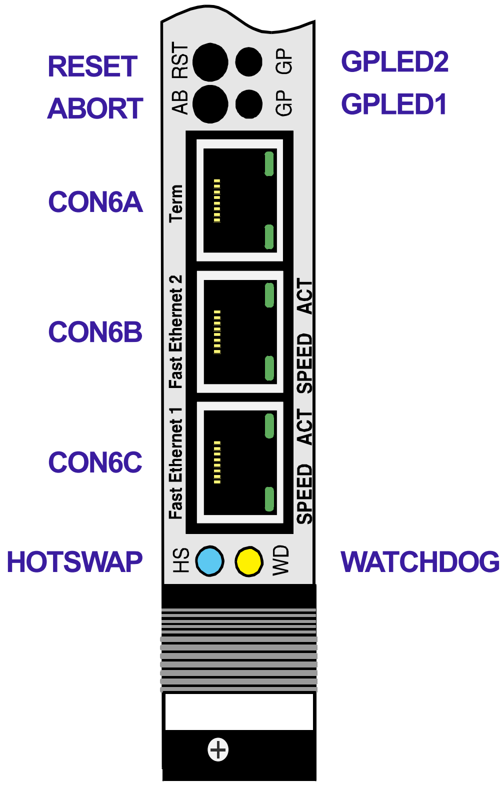
On the CP620 front panel there are two push button switches for interacting with the system: RST for reset and AB for abort.

The RST button is routed directly to the power supervisor/reset controller chip. Pressing the RST button initiates an immediate hardware reset of the system.

During normal operation pressing the AB button causes a non-maskable interrupt (NMI) to be generated. In addition, the AB button is latched into a bit in the System Logic, in order to differentiate between NMIs initiated from the ABORT Button and NMIs initiated from the Watchdog Timer.

Pressing the AB button during system startup when the lower LED (situated alongside the Abort button) is blinking causes the NetBootLoader to enter interactive command mode. Commands can then be entered for processing by the bootstrap loader. Please refer to chapter 5 for NetBootLoader information.

Figure 2-13: Front Panel LEDs and Push Buttons



2.7.4 System Status Indicators

The system status indicators can be divided into three groups. The first group (the LEDs beside the push buttons) is application oriented whereas the second group (the LEDs integrated within the Ethernet connector) is dedicated to and controlled by the Ethernet interface. The third group has dedicated functions (Hot Swap and Watchdog timer). The table below provides an overview of the functionality associated with these indicators.

Table 2-15:System Status Indicators

LED	COLOR	NAME	DESCRIPTION
HS	BLUE	LED1B	Lit when safe to extract the board from backplane.
WD	YELLOW	LED1Y	Watchdog timer: indicates that the watchdog is active

2.7.5 Digital Temperature Sensor (LM75)

The digital temperature sensor (National Semiconductor LM75) installed on the CP620 measures the board temperature. Used as a thermal watchdog, the LM75 can generate a maskable interrupt which can be used by an application. In addition, the actual temperature can be read out of the LM75 via the I²C bus. This may be used, for example, to maintain the calibration of the onboard RTC over a wide operational temperature range. Please refer to chapter 4.6, Digital Temperature Sensor, LM75, for additional information.

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2.8 Hot Swap

2.8.1 Technical Background of CompactPCI Hot Swap

In many modern application systems downtime is costly and/or unacceptable. Server applications, telecommunications networks and automated systems requiring continuous monitoring call for a system design in which a single card can be inserted or extracted without affecting the rest of the system. The ease with which a board may be removed and replaced is dependent on the mechanical design (form factor), the possibility of deactivating the software drivers for the board (operating system) and the possibility of removing and inserting the board without disturbing the signal quality on the bus.

CompactPCI hot swap is currently the most effective way to meet this need. Staggered pins on the backplane guarantee controlled power sequencing of the board, while the signals ENUM, BDSEL, HEALTHY and the hot swap control and status register bits may be used to control board access from the software side.

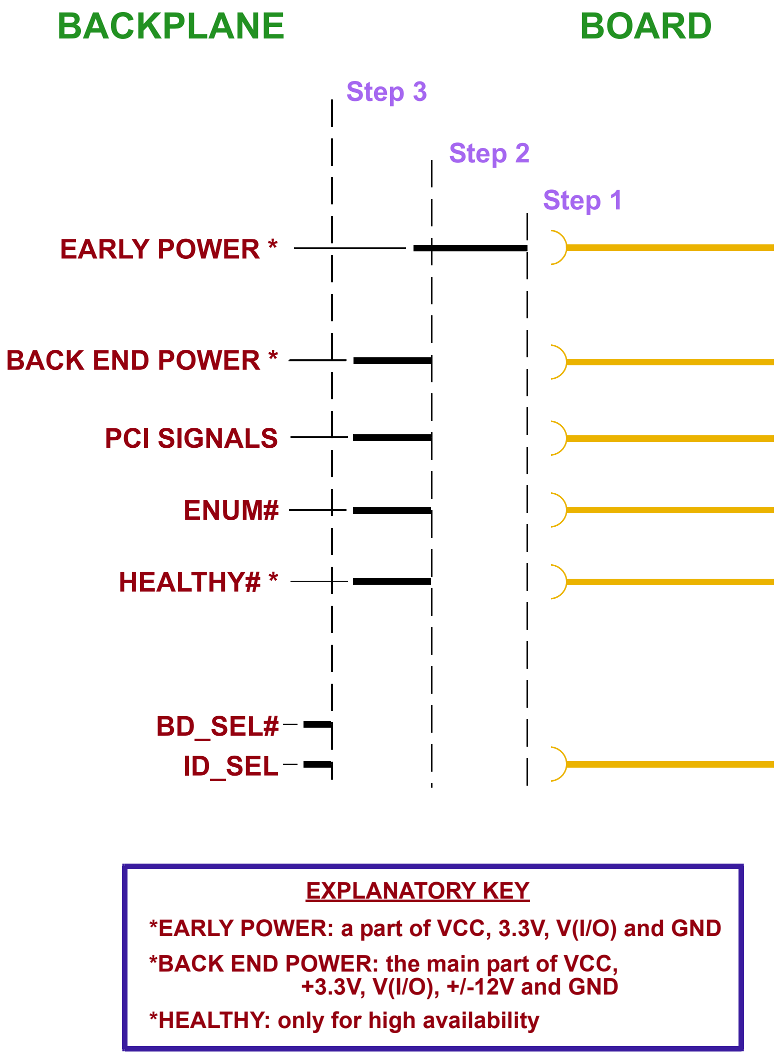
2.8.2 Hot Swap System

A hot swap system consists of a hot swap platform which comprises a hot swap backplane, the system host (CPU) with hot swap features, cooling, power supplies, etc., plus the boards to be hot swapped. Hot swapping is not possible unless the operating system has the capability to enable and disable the board specific driver during normal operation.

2.8.2.1 The Hot Swap Backplane

The hot swap backplane, illustrated on the following page, has staggered pins to ensure defined power sequencing.

Figure 2-14: Illustration of Staggered Pinning on the Hot Swap Backplane



Note ...

Some special signals (e.g. ENUM, HEALTHY, BDSEL...) have particular routing requirements.

2.8.2.2 The System Controller/Master

The System Controller must have the possibility to utilize the special signals defined by the CompactPCI hot swap specification. If a high availability system is used, it must additionally be able to control the hardware connection with the peripheral boards (Hardware Connection Control).

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2.8.2.3 The Hot Swap Board Additional Features

To ensure that a board may be removed and replaced in a working bus without disturbing the system it requires the following additional features:

- precharge
- power ramping
- hot swap control and status register bits
- automatic interrupt generation whenever a board is about to be removed or replaced
- an LED to indicate that the board may be safely removed

2.8.3 The Hot Swap Process

The hot swap process has two components; board extraction and board insertion.

2.8.3.1 Board Extraction

Start by opening (pulling down) the lower board handle; this will result in the CompactPCI bridge generating an interrupt (ENUM). The system master will now identify the board to be extracted and, when safe to do so, will disable the relevant software drivers. Next the system master lights the blue LED, which signals that it is now safe to remove the board by means of its handles.

- open lower board handle - this results in an interrupt from the CPCI bridge (ENUM)
- system master identifies board to be extracted
- when safe to do so the system master disables the relevant software drivers
- system master lights blue LED on the board to signal that it may be safely removed
- board may now be removed by means of its handles

2.8.3.2 Board Insertion

Take hold of the board by the handles and push it steadily into its slot. The long pins are the first to connect and power up the CompactPCI bridge and hot swap controller and preload the CompactPCI signal pins. Next, the medium length pins connect, leading to the power ramping of the entire board and the mating of the signal pins. Lastly, the one short pin connects, generating an onboard reset. With the board fully inserted the lower handle is now closed; this generates an interrupt (ENUM) which signals to the system master that a board has been added to the system. The system master identifies the board and allocates system resources to the board. Next the system master activates software drivers relating to the board. Finally, the blue LED is deactivated indicating that the process is complete.

- commence insertion of the board using the handles
  - the long pins are the first to connect and power up the CompactPCI bridge and hot swap controller and preload the CompactPCI signal pins
  - the medium pins connect leading to the power ramping of the entire board and the signals pins mate
  - the short pin connects generating an onboard reset
- lower handle is closed, this generates an interrupt (ENUM) which signals to the system master that a board has been added to the system
- system master identifies the board and allocates system resources to the board
- system master activates software drivers relating to the board
- blue LED is deactivated indicating that the process is complete

2.8.4 Design Implementation on CP620

The CP620 is a system master and is, therefore, not hot swappable. But as a system master, it has to monitor and analyze the ENUM# Interrupt. The ENUM# interrupt is routed to the serial IRQ9.

2.8.5 Design Implementation on CP620-PCIP

The CP620-PCIP is used to work in a PICMG 2.16 Rev 1.0 compliant environment. It communicates via Ethernet and therefore the PCI-to-PCI bridge is not populated. This means that no signals require to be precharged. Only a small subset of hot swap circuitry is therefore necessary to provide hot swap capability.

2.8.5.1 Power Ramping

On the CP620-PCIP, a special hot swap controller is used to ramp up the onboard supply voltage. The reason for this is to avoid transients on the 3.3V, 5V, +12V and -12V power supplies from the hot swap system. When the power supply is stable, the hot swap controller generates a reset onboard and on the PMC slots to put the devices into a definite state.

2.8.5.2 Precharge

Precharge is not needed on the CP620-PCIP, because there are no PCI signals present. The communication on this board version is via the Ethernet; these signals do not require a precharge during insertion.

2.8.5.3 Handle Switch

A microswitch is situated in the extractor handle (CP620-PCIP only). Opening the handle initiates the generation of serial interrupt IRQ9. This interrupt makes the execution of other commands possible before the board is extracted from the system, for example, a command to shut down the operating system. The microswitch is routed to CON12 on the board.

2.8.5.4 Blue LED

On the CP620-PCIP, a blue LED can be switched on or off by software. It may be used, for example, to indicate that the shutdown process is finished and the board is ready for extraction. It may also be used for general purposes.

2.9 Intelligent Platform Management Interface (IPMI)

2.9.1 Technical Background of IPMI

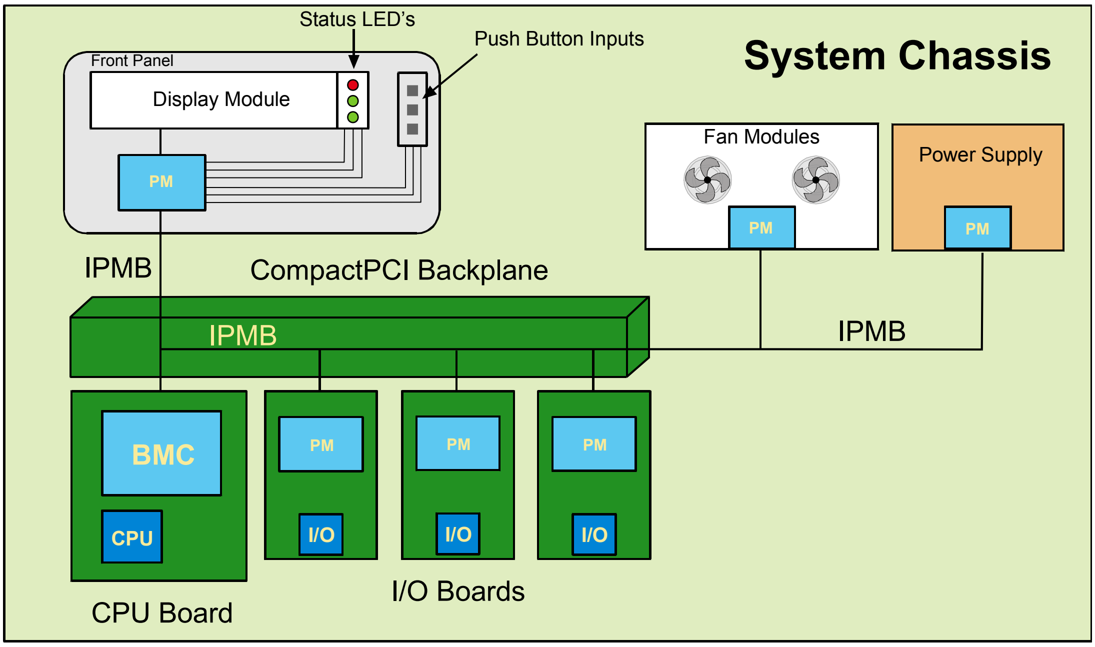
The CP620 has been configured to support the "Intelligent Platform Management Interface" (IPMI) subsystem, which is another step in providing high availability platforms. Intelligent Platform Management means monitoring the health of the entire system beyond the confines of the board itself, so that the status of the complete system is available to be used, for example, for control and intervention purposes. A range of variables is monitored on every board, to provide information on the system status, e.g. voltages, temperature, powergood signals, reset signals etc. Additionally, the IPMI Baseboard controller can intervene, regulating the operating status of the system by controlling fans, shutting down systems and generating alarm signals as and when fault conditions occur. These fault conditions are simultaneously logged in non-volatile memory for analysis and for fault recovery. IPMI also defines a protocol (software stack) for exchanging the status messages of the board, so that "IPMI ready" boards/systems from different suppliers can be monitored. In addition, a clear interface (registers, addresses etc.) is defined for guaranteeing that system management software can work with every compliant IPMI hardware.

The electrical interconnection between IPMI capable boards is an I2C interface (IPMB). On CompactPCI systems, this interface is provided on IPMI-prepared backplanes and guarantees the data path between the boards.

The devices which handle the measurements and the protocol stack are microcontrollers which are named Baseboard Management Controller (BMC) and Peripheral Management Controller (PM) depending on their position in a CompactPCI backplane. The IPMI microcontroller which is on the System Master board in a CompactPCI system is called BMC and the IPMI controller which is on a peripheral board is named PM.

The interface between the system controller CPU’s system management software and the Baseboard Management Controller can be realized in two different ways, a keyboard controller style interface (KCS) or a block transfer interface (BT), which can be found in the system master’s I/O space.

Figure 2-15: IPMI Functional Block Diagram



2.9.2 IPMI Implementation on the CP620

On the CP620, the IPMI functionality is realized using the ZIRCON-Lite controller from QLogic, which is an ARM7TDMI core-based IPMI controller. Due to the fact that this controller can act as BMC and as PM on all versions of the CP620, the same controller can be used. All the information collected by the ZIRCON-Lite is then accessible by software through a keyboard-style interface (see IPMI — Intelligent Platform Management Interface Specification V.1.0 for more information) whose address space is available in the I/O space of the Intel CPU's address map, or via the IPMB-Bus.

2.9.3 Measurement of Onboard Voltages

On the CP620 all voltages, i.e. 5V, 3.3V, 2.5V, VCORE, VIO, 12V and -12V, are monitored by the ZIRCON-Lite.

2.9.4 Measurement of Temperatures

An onboard sensor measures the temperature in the vicinity of the CPU (positioned below the heat sink).

2.9.5 Fan Control

Four Tacho inputs and two PWM outputs are routed to the rear I/O connector. These make it possible to control the fan speed in order to regulate the CPU cooling.

2.9.6 Data Repositories

All the data gathered by the ZIRCON is stored in a non-volatile memory, providing the possibility to obtain information about working conditions and failure situations.

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Chapter 3

Installation

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3. Installation

The CP620 has been designed for easy installation. However, the following standard precautions and installation information and procedures must be observed to ensure proper installation and to preclude damage to the board or injury to personnel.

3.1 Hardware Installation

The product described in this manual can be installed in any available slot of a CompactPCI bus system. However, to function as a system controller it must be installed in slot 1 (far left).

3.1.1 Safety Requirements

The board must be securely fastened to the chassis using the front panel retaining screws to avoid loosening of the board through vibration and to ensure proper grounding and operation of the board.

Caution, Electric Shock Hazard!

Switch off the CompactPCI system main power before installing the board. Ensure that there are no other external voltages being applied to system. This includes signals to all other boards within the system. Failure to comply with the above could endanger your life or health and may damage your board or system.

ESD Equipment!

This CompactPCI board contains electrostatically sensitive devices. Please observe the following precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

Do not touch components, connector pins, or conductive circuits.

If working at an anti-static workbench with professional discharging equipment, ensure compliance with its usage when handling this product.

3.1.2 Installation Procedures

To install the board proceed as follows:

Ensure that the safety requirements indicated above are observed.

Warning!

Failure to comply with the instruction below may cause damage to the board or result in improper system operation. Please refer to chapter 4 for configuration information.

- Ensure that the board is properly configured for operation before installing.

Note ...

Care must be taken when applying the procedures below to ensure that when the board is inserted it is not damaged through contact with other boards in the system.

- Install the board in the appropriate slot and ensure that it is properly seated in the backplane (front panel is flush with the rack front).
- Fasten the front panel retaining screws.
- Connect external interfacing cables to the board as required.
- Ensure that the board and interfacing cables are properly secured.

3.1.3 Removal Procedures

To remove the board proceed as follows:

- Ensure that the safety requirements indicated above are observed.
- Disconnect any interfacing cables that may be connected to the board.
- Loosen the front panel retaining screws.
- Disengage the board from the backplane by pressing down on the front panel handle and pull the board out of the slot.

3.2 Hot Swap Procedure (CP620-PCIP Only)

3.2.1 Board Extraction

Warning!

Only the CP620-PCIP is hot swap capable. The standard CP620 is a system master and must not be extracted or inserted into a powered-up system.

- open lower board handle - this results in an interrupt IRQ9*
- board may now be removed by means of its handles

Note ...

The application software may react to this interrupt (for example, by halting a running process or the storage of data etc.) When this is completed, depending on the application software, the blue LED will light to show that the board is ready for extraction.

3.2.1.1 Board Insertion

- commence insertion of the board using the handles
  - the long pins are the first to connect and power up the hot swap controller
  - the medium pins connect leading to the power ramping of the entire board
  - the short pin connects generating an onboard reset

3.3 Software Installation

Software installation is a function of the Bootstrap Loader and is described in chapter 5 of this manual.

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Chapter **4**

Configuration

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4. Configuration

4.1 Jumper and Resistor Settings

Please see Figures 1-2 and 1-3 in Chapter 1 to view the positions of the jumpers and resistors on the board.

J3 - NetBootLoader/Socket Jumper

The jumper J3 is used to select the memory position from which the CP620 fetches its boot code. It establishes the address location of the onboard Flash window and the memory expansion socket 1 (DIL600, 32-pin). Refer to the section “Memory Configuration Register” in this chapter for further information.

Table 4-1: J3 - NetBootLoader/Socket Jumper Settings

J3	DESCRIPTION	ADDRESS ASSIGNMENT	
Open	***CP620 fetches boot code from onboard Flash***	***Socket 1:*** ***Onboard Flash Window:***	***0xFFF8 0000 - 0xFFFF FFFF*** ***0xFFF0 0000 - 0xFFF7 FFFF***
Closed	CP620 fetches boot code from socket 1	Socket 1: Onboard Flash Window:	0xFFF0 0000 - 0xFFF7 FFFF 0xFFF8 0000 - 0xFFFF FFFF

The default setting is indicated by using italic bold.

Note ...

The IBM® PowerPC® 750CX/CXe initially fetches its boot code from the address 0xFFF0 0100.

4.1.1 J2 - Real-Time Clock (RTC) Calibration Output

J2 is a test point for calibration measurement of the frequency of the RTC and is as such not a jumper. Refer to the datasheet of the ST M41T56 for further information on the use of this output signal.

Warning!

At NO TIME is J2 to be jumpered (short circuited). This is a test point and operation with a jumper installed will cause damage to the RTC.

4.1.2 Resistor Settings for Non-Standard Socket Devices

The default pinouts of sockets 1 and 2 are designed for use with standard DIL Flashes and M-Systems DiskOnChip. However, in order to accommodate the various possible devices it is necessary to install resistors as jumpers to configure the board for proper operation.

Table 4-2: Resistor Settings for Socket 1

USED SOCKET DEVICE	R289	R351	R358	R352	R287	R353	R359
Flash/DiskOnChip	***Open***	***Open***	***Open***	***Set***	***Set***	***Open***	***Set***
NVSRAM	Open	Open	Set	Open	Set	Set	Open
4 Mbit EPROM	Set	Set	Open	Open	Open	Open	Set

The default setting is indicated by using italic bold.

Note ...

All resistors are 0 ohm.

4.1.3 Resistor Setting for RS485/RS422 Selection

Both the SER2 and SER3 ports may be used in either RS485 or RS422 mode. Selection is made by means of the resistors detailed in the following table:

Table 4-3: Resistor Setting for RS485/RS422 Selection

MODE	R122	R141	R147	R152
SER2 and SER3 in RS485 half duplex mode	***Set (4k7)***	***Open***	***Set (4k7)***	***Open***
SER2 in RS422 mode, SER3 in RS485 mode	Open	Set (0R)	Set (4k7)	Open
SER2 in RS485 mode, SER3 in RS422 mode	Set (4k7)	Open	Open	Set (0R)
SER2 and SER3 in RS422 mode	Open	Set (0R)	Open	Set (0R)

The default setting is indicated by using italic bold.

Note ...

These interfaces are optional (special board version).

4.1.4 RS485/RS422 Slew Rate Limit

On versions of the board which are equipped with the RS485/RS422 transceivers, it is possible to limit the signal slew rate to enhance the EMI behavior.

Table 4-4: Interface SER2 Slew Rate Limit Settings

Slew Rate	R104	R103
10 Mb/s	***Open***	***Set (0R)***
115 Kb/s	Open	Open
500 Mb/s	Set (4k7)	Open

The default setting is indicated by using italic bold.

Table 4-5: Interface SER3 Slew Rate Limit Settings

SLEW RATE	R81	R94
10 Mb/s	***Open***	***Set (0R)***
115 Kb/s	Open	Open
500 Kb/s	Set (4k7)	Open

The default setting is indicated by using italic bold.

4.2 Board Address Map

The following figures illustrate the address mapping of the CP620. Where the first figure describes the overall map, the second figure provides a more detailed map of the uppermost address area. The upper area address map depends on the configuration of the CP620 memory expansion sockets and the requirements of the application.

Figure 4-1: CP620 Address Map

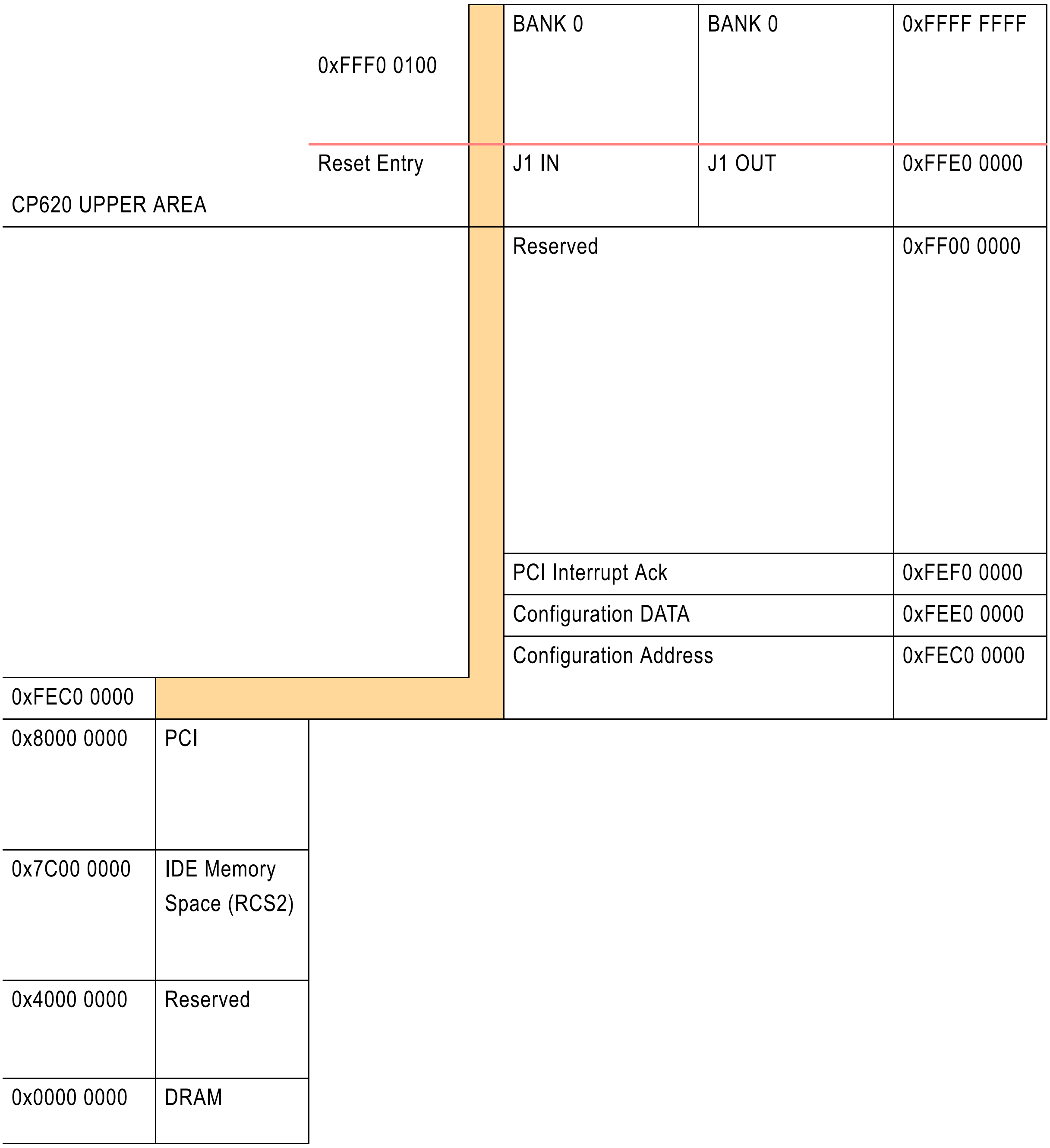

Figure 4-2: CP620 Upper Area Address Map

	Installed		Removed	
	Soldered FLASH (paged)	0xFFFF FFFF 0xFFF8 0000	Memory Expansion Socket 1	0xFFFF FFFF 0xFFF8 0000
0xFFF0 0100	Memory Expansion Socket 1		Soldered FLASH (paged)	
Reset Entry		0xFFF0 0000		0xFFF0 0000
	Reserved	0xFFE8 0000	Reserved	0xFFE8 0000
	IPMI	0xFFE0 0040	IPMI	0xFFE0 0040
	UART D	0xFFE0 0028	UART D	0xFFE0 0028
	UART C	0xFFE0 0020	UART C	0xFFE0 0020
	Onboard Register	0xFFE0 0010	Onboard Register	0xFFE0 0010
	UART B	0xFFE0 0008	UART B	0xFFE0 0008
	UART A	0xFFE0 0000	UART A	0xFFE0 0000

Boot Strap/Loader Jumper - J3

Note ...

Write access to the upper area addresses is only possible using byte-wide write commands.

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4.3 Board Control Registers

The Board Control registers may be accessed through byte-wide read and write operations to the address space 0xFFE0 0000 - 0xFFE7 FFFF.

Table 4-6: Board Control Registers

REGISTER	ADDRESS	ACCESS	
		READ	WRITE
Board ID	0xFFE0 0010	X	--
Software Compatibility ID	0xFFE0 0012	X	--
Memory Configuration	0xFFE0 0014	X	--
Flash Bank Select	0xFFE0 0016	X	X
Watchdog Control Register	0xFFE0 0018	X	X
Control Register	0xFFE0 001A	X	X
Interface Route Register	0xFFE0 001B	X	X
Event Register	0xFFE0 001C	X	X
Board / Logic Revision	0xFFE0 001E	X	--
IPMI_DATA_IN (keyboard style interface)	0xFFE0 0030		X
IPMI_DATA_OUT (keyboard style interface)	0xFFE0 0030	X	--
IPMI_Command Register (keyboard style interface)	0xFFE0 0031	--	X
IPMI Status Register	0xFFE0 0031	X	--
CompactFlash Registers	7C000000 - 7C000078	for details please refer to table 4-29	

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4.3.1 Board ID Register

The Board ID is used to identify the CP620 in a CompactPCI system. The value for the CP620 is 0x82, which is factory set and cannot be changed.

Table 4-7: Board ID Register

REGISTER NAME	BOARD ID						ACCESS	
ADDRESS	0xFFE0 0010						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	BID7	BID6	BID5	BID4	BID3	BID2	BID1	BID0
DEFAULT	1	0	0	0	0	0	0	1

4.3.2 Software Compatibility ID

The Software Compatibility ID will signal to the software when differences in hardware require different handling by the software. It starts with the value 0x00 and will be incremented with each change in hardware (software sensitive only). This register is set at the factory and is for use only by the NetBootLoader and BSP software, and as such, is not user relevant.

Table 4-8: Software Compatibility ID

REGISTER NAME	SOFTWARE COMPATIBILITY ID						ACCESS	
ADDRESS	0xFFE0 0012						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0
DEFAULT	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a

4.3.3 Memory Configuration Register

The Memory Configuration register provides basic information concerning the amount of installed main memory, whether or not ECC is enabled, and the location from which the operating system is to access the NetBootLoader.

Table 4-9: Memory Configuration Register

REGISTER NAME	MEMORY CONFIGURATION						ACCESS	
ADDRESS	0xFFE0 0014						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	BJ	res.	res.	res.	SZ3	SZ2	SZ1	SZ0
DEFAULT	n/a	n/a	n/a	1	n/a	n/a	n/a	n/a

<table>
<tr><th>BIT</th><th>NAME</th><th>VAL</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="2">0</td><td rowspan="2">SZ0</td><td>0</td><td rowspan="8">Settings:
<table>
<tr><th>SZ3</th><th>SZ2</th><th>SZ1</th><th>SZ0</th><th></th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>64 MB (64 Mbit chips, 1 bank equipped)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>128 MB (64 Mbit chips, 2 banks equipped)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>128 MB (128 Mbit chips, 1 bank equipped)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>256 MB (128 Mbit chips, 2 banks equipped)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>384 MB (128 Mbit chips, 3 banks equipped)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>512 MB (128 Mbit chips, 4 banks equipped)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>512 MB (256 Mbit chips, 2 banks equipped)</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>reserved</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>reserved</td></tr>
</table></td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">SZ1</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">SZ2</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">SZ3</td><td>0</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">Res.</td><td>0</td><td rowspan="2">Reserved</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">Res.</td><td>0</td><td rowspan="2">Reserved</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">Res.</td><td>0</td><td rowspan="2">Reserved</td></tr>
<tr><td>1</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">BJ</td><td>0</td><td>Boot Jumper J3 closed (CP620 fetches boot code from onboard Flash)</td></tr>
<tr><td>1</td><td>Boot Jumper J3 open (CP620 fetches boot code from socket 1)</td></tr>
</table>

4.3.4 Flash Bank Select Register

The Flash bank select register is used to select the appropriate soldered Flash bank. As 8-bit wide Flash memory may only be accessed through a 512 kB window this is the only way to address a larger size Flash memory. Using bits 0 to 3 (FBn), 16 Flash banks can be selected (16x512 kB = 8 MB). The default value on startup of the CP620 is 0x00.

Table 4-10: Flash Bank Select Register

REGISTER NAME	FLASH BANK SELECT						ACCESS	
ADDRESS	0xFFE0 0016						R	W
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	res.	res.	res.	res.	FB3	FB2	FB1	FB0
DEFAULT	n/a	n/a	n/a	n/a	0	0	0	0

4.3.5 Watchdog Control Register

The Watchdog Control register is the interface between applications and the operating system for controlling the functioning of the Watchdog. Together with the Event Register, bit 0 (WD) and bit 2 (PB2), the possibility is provided for either hardware (Abort switch) or software (Watchdog timer) intervention in the execution of the application.

Table 4-11: Watchdog Control Register

REGISTER NAME	WATCHDOG CONTROL						ACCESS	
ADDRESS	0xFFE0 0018						R	W
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	WD_EN	WD_R	WD_CCD	WD_TRG	res.	res.	WDT1	WDT0
DEFAULT	0	0	0	0	n/a	n/a	n/a	n/a

BIT	NAME	VAL	DESCRIPTION
0	WDT0	0	Settings: WDT1 WDT0 0 0 0.5 seconds Watchdog timeout time 0 1 1.0 seconds Watchdog timeout time 1 0 1.5 seconds Watchdog timeout time 1 1 2.0 seconds Watchdog timeout time
		1	
1	WDT1	0	
		1	
2		0	Reserved
		1	
3		0	Reserved
		1	
4	WD_TRG	0	When WD-EN (bit 7) set to 1, indicates that Watchdog timer has not been retriggered.
		1	Causes the Watchdog to be retriggered (Resets Watchdog timer to value indicated by bits 0 and 1, and WD_TRG (bit 4) to 0)
5	WD_CCD	0	Normal watchdog functionality
		1	Cascade mode: when watchdog timout occurs, an NMI will be generated, the watchdog timer resets, a further timeout will result in a system reset
6	WD_R	0	Causes hardware reset of system upon Watchdog timeout
		1	Causes generation of a non-maskable interrupt upon Watchdog timeout
7	WD_EN	0	Watchdog timer disabled
		1	Watchdog timer enabled  ***Note ...*** Once the Watchdog timer is enabled it cannot be disabled except by resetting the system.

4.3.6 Control Register

The Control register provides access to the front panel general purpose LEDs (LED1R and LED1G), allows for the generation of a software reset of the system, and is used to control the configuration of the SER 0 (UART B) either for RS-232 or RS-485 operation.

Table 4-12: Control Register

REGISTER NAME	CONTROL						**ACCESS**	
ADDRESS	0xFFE0 001A						R	W
BIT POSITION	MSB **7**	**6**	**5**	**4**	**3**	**2**	**1**	**0** LSB
CONTENT	ETH_DIR1	ETH_DIR0	Res.	S_RST	REAR_LED	HS_LED	GPLED2	GPLED1
DEFAULT	n/a	n/a	0	n/a	0	0	0	0

BIT	**NAME**	**VAL**	**DESCRIPTION**
0	GPLED1	0	GPLED1 (beside ABORT button) (green) off
		1	GPLED1 (green) on
1	GPLED2	0	GPLED2 (beside RESET button) (green) off
		1	GPLED2 (green) on
2	HS_LED	0	HS_LED (blue) off
		1	HS_LED (blue) on
3	REAR_LED	0	REAR_LED off
		1	REAR_LED on
4	S_RST	0	No operation
		1	Causes a software reset (S_RST) to be initiated
5	Res.	0	Reserved
		1	Reserved
6	ETH_DIR0	0	Front IO for Ethernet interface 0 (default)
		1	Rear IO for Ethernet interface 0
7	ETH_DIR1	0	Front IO for Ethernet interface 1 (default)
		1	Rear IO for Ethernet interface 1

Note ...

The direction for the Ethernet interface 0 is also determined by the status of jumper J1. The jumper has the highest priority, meaning that if J1 is closed, Ethernet interface 0 will be directed to the front IO regardless of the status of register bit 6.

4.3.7 Interface Route Register

Table 4-13: Interface Route Register

REGISTER NAME	INTERFACE ROUTE						ACCESS	
ADDRESS	0xFFE0001b						R	W
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	SER3_Echo	SER2_Echo	SER3_485	SER2_485	SER3_DIR	SER2_DIR	SER1_DIR	SER0_DIR
DEFAULT	0	0	0	0	0	0	0	0

BIT	NAME	VAL	DESCRIPTION
0	SER0_DIR	0	Front IO
		1	Rear IO
1	SER1_DIR	0	Front IO
		1	Rear IO
2	SER2_DIR	0	Front IO
		1	Rear IO
3	SER3_DIR	0	Front IO
		1	Rear IO
4	SER2_485	0	Configured for RS232
		1	Configured for RS485
5	SER3_485	0	Configured for RS232
		1	Configured for RS485
6	SER2_ECHO	0	ECHO off (RS485 mode)
		1	ECHO on (RS485 mode)
7	SER3_ECHO	0	ECHO off (RS485 mode)
		1	ECHO on (RS485 mode)

4.3.8 Event Register

The Event register is used to indicate the origin of the generation of the non-maskable interrupts caused either by a Watchdog timeout or the pressing of the Abort switch.

Table 4-14: Event Register

REGISTER NAME	EVENT						ACCESS	
ADDRESS	0xFFE0 001C						R	W
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	Res.	Res.	Res.	Res.	Res.	PB2	Res.	WD
DEFAULT	n/a	n/a	n/a	n/a	n/a	0	n/a	0

BIT	NAME	VAL	DESCRIPTION
0	WD	0	Indicates that no Watchdog timeout has occurred
		1	Indicates that a Watchdog timeout has occurred
1		0	Reserved
		1	
2	PB2	0	Indicates that the Abort switch has not been pressed
		1	Indicates that the Abort switch has been pressed
3		0	Reserved
		1	
4		0	Reserved
		1	
5		0	Reserved
		1	
6		0	Reserved
		1	
7		0	Reserved
		1	

4.3.9 Board Logic/Revision Register

The Board Revision Register may be used to identify the hardware (BRn) and logic status of the board by the software (LRn). It is set at the factory and starts with the value 0x00 for the initial board prototypes and will be incremented with each redesign/logic release.

Table 4-15: Board Logic/Revision Register

REGISTER NAME	BOARD LOGIC/REVISION						ACCESS	
ADDRESS	0xFFE0 001E						R	
BIT POSITION	MSB 7	6	5	4	3	2	1	0 LSB
CONTENT	LR3	LR2	LR1	LR0	BR3	BR2	BR1	BR0
DEFAULT	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a

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4.4 UART Registers Address Mapping

4.4.1 UART A

The following tables indicate the address mapping of UART A. For a more detailed description please refer to the EXAR XR16C2850 DUART manual.

Table 4-16: UART A General Register Set

READ MODE	WRITE MODE	ADDRESS
Receive Holding	Transmit Holding	0xFFE0 0000
n/a	Interrupt Enable	0xFFE0 0001
Interrupt Status	FIFO Control	0xFFE0 0002
n/a	Line Control	0xFFE0 0007
n/a	Modem Control	0xFFE0 0004
Line Status	n/a	0xFFE0 0005
Modem Status	n/a	0xFFE0 0006
Scratchpad	Scratchpad	0xFFE0 0007

Table 4-17: UART A Baud Rate Register Set

READ MODE	WRITE MODE	ADDRESS
LSB of divisor latch	LSB of divisor latch	0xFFE0 0000
MSB of divisor latch	MSB of divisor latch	0xFFE0 0001

Table 4-18: UART A Enhanced Register Set

READ MODE	WRITE MODE	ADDRESS
Trigger Level	Trigger Level	0xFFE0 0000
Feature Control	Feature Control	0xFFE0 0001
Enhanced Feature	Enhanced Feature	0xFFE0 0002
Enhanced Mode Select	Enhanced Mode Select	0xFFE0 0007
Xon-1	Xon-1	0xFFE0 0004
Xon-2	Xon-2	0xFFE0 0005
Xoff-1	Xoff-1	0xFFE0 0006
Xoff-2	Xoff-2	0xFFE0 0007

4.4.2 UART B

The following tables indicate the address mapping of UART B. For a more detailed description please refer to the EXAR XR16C2850 DUART manual.

Table 4-19: UART B General Register Set

READ MODE	WRITE MODE	ADDRESS
Receive Holding	Transmit Holding	0xFFE0 0008
n/a	Interrupt Enable	0xFFE0 0009
Interrupt Status	FIFO Control	0xFFE0 000A
n/a	Line Control	0xFFE0 000B
n/a	Modem Control	0xFFE0 000C
Line Status	n/a	0xFFE0 000D
Modem Status	n/a	0xFFE0 000E
Scratchpad	Scratchpad	0xFFE0 000F

Table 4-20: UART B Baud Rate Register Set

READ MODE	WRITE MODE	ADDRESS
LSB of divisor latch	LSB of divisor latch	0xFFE0 0008
MSB of divisor latch	MSB of divisor latch	0xFFE0 0009

Table 4-21: UART B Enhanced Register Set

READ MODE	WRITE MODE	ADDRESS
Trigger Level	Trigger Level	0xFFE0 0008
Feature Control	Feature Control	0xFFE0 0009
Enhanced Feature	Enhanced Feature	0xFFE0 000A
Enhanced Mode Select	Enhanced Mode Select	0xFFE0 000B
Xon-1	Xon-1	0xFFE0 000C
Xon-2	Xon-2	0xFFE0 000D
Xoff-1	Xoff-1	0xFFE0 000E
Xoff-2	Xoff-2	0xFFE0 000F

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4.4.3 UART C

The following tables indicate the address mapping of UART C. For a more detailed description please refer to the EXAR XR16C2850 DUART manual.

Table 4-22: UART C General Register Set

READ MODE	WRITE MODE	ADDRESS
Receive Holding	Transmit Holding	0xFFE0 0020
n/a	Interrupt Enable	0xFFE0 0021
Interrupt Status	FIFO Control	0xFFE0 0022
n/a	Line Control	0xFFE0 0027
n/a	Modem Control	0xFFE0 0024
Line Status	n/a	0xFFE0 0025
Modem Status	n/a	0xFFE0 0026
Scratchpad	Scratchpad	0xFFE0 0027

Table 4-23: UART C Baud Rate Register Set

READ MODE	WRITE MODE	ADDRESS
LSB of divisor latch	LSB of divisor latch	0xFFE0 0020
MSB of divisor latch	MSB of divisor latch	0xFFE0 0021

Table 4-24: UART C Enhanced Register Set

READ MODE	WRITE MODE	ADDRESS
Trigger Level	Trigger Level	0xFFE0 0020
Feature Control	Feature Control	0xFFE0 0021
Enhanced Feature	Enhanced Feature	0xFFE0 0022
Enhanced Mode Select	Enhanced Mode Select	0xFFE0 0027
Xon-1	Xon-1	0xFFE0 0024
Xon-2	Xon-2	0xFFE0 0025
Xoff-1	Xoff-1	0xFFE0 0026
Xoff-2	Xoff-2	0xFFE0 0027

4.4.4 UART D

The following tables indicate the address mapping of UART A. For a more detailed description please refer to the EXAR XR16C2850 DUART manual.

Table 4-25: UART D General Register Set

READ MODE	WRITE MODE	ADDRESS
Receive Holding	Transmit Holding	0xFFE0 0028
n/a	Interrupt Enable	0xFFE0 0029
Interrupt Status	FIFO Control	0xFFE0 002A
n/a	Line Control	0xFFE0 002B
n/a	Modem Control	0xFFE0 002C
Line Status	n/a	0xFFE0 002D
Modem Status	n/a	0xFFE0 002E
Scratchpad	Scratchpad	0xFFE0 002F

Table 4-26: UART D Baud Rate Register Set

READ MODE	WRITE MODE	ADDRESS
LSB of divisor latch	LSB of divisor latch	0xFFE0 0028
MSB of divisor latch	MSB of divisor latch	0xFFE0 0029

Table 4-27: UART D Enhanced Register Set

READ MODE	WRITE MODE	ADDRESS
Trigger Level	Trigger Level	0xFFE0 0028
Feature Control	Feature Control	0xFFE0 0029
Enhanced Feature	Enhanced Feature	0xFFE0 002A
Enhanced Mode Select	Enhanced Mode Select	0xFFE0 002B
Xon-1	Xon-1	0xFFE0 002C
Xon-2	Xon-2	0xFFE0 002D
Xoff-1	Xoff-1	0xFFE0 002E
Xoff-2	Xoff-2	0xFFE0 002F

4.4.5 CompactFlash

Table 4-28: CompactFlash Register

REGISTER	READ/WRITE	ADDRESS
Data Register	R/W	7c000000
Error Register	R	7c000008
Feature Register	W	7c000008
Sector Count Register	R/W	7c000010
Sector Number Register	R/W	7c000018
Cylinder Low Register	R/W	7c000020
Cylinder High Register	R/W	7c000028
Drive/Head Register	R/W	7c000030
Status Register	R	7c000038
Device Control Register	W	7c000038
Alternate Status Register	R	7c000070
Digital Output Register	W	7c000070
Card Drive Address Register	R/W	7c000078

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4.4.6 IRQ Routing

The IRQ routing of the CP620 is serial as opposed to being parallel. Hence the IRQ names are prefixed with S_ to indicate that they are serial.

Table 4-29: IRQ Routing

IRQ NAME	SOURCE
S_IRQ0	Reserved
S_IRQ1	UART-A
S_IRQ2	UART-B
S_IRQ3	INTA# (PCI)
S_IRQ4	INTB# (PCI)
S_IRQ5	INTC# (PCI)
S_IRQ6	INTD# (PCI)
S_IRQ7	TEMP_INT (Temperature Interrupt)
S_IRQ8	IDE (CompactFlash)
S_IRQ9	ENUM (CP620) / Handle Switch (CP620-PCIP)
S_IRQ10	UART-C
S_IRQ11	UART-D
S_IRQ12	IPMI (optional)
S_IRQ13	DEG (Power Supply Derating)
S_IRQ14	FAL (Power Supply Failure)
S_IRQ15	Reserved

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4.4.7 Real-Time Clock

Access to the real-time clock (RTC) is effected via the I2C bus. The RTC uses address 0xD0. For more detailed information please refer to the manuals for the ST - Microelectronics M41T56 and the Motorola MPC 107 (I2C - Bus).

Table 4-30: Register Map RTC M41T56

REG. BYTE	ADDRESS BITS								FUNCTION RANGE IN BCD FORMAT
	D7	D6	D5	D4	D3	D2	D1	D0	
0	ST	10 Seconds			Seconds				Seconds: 00 - 59
1	X	10 Minutes			Minutes				Minutes: 00 - 59
2	CEB	CB	10 Hours		Hours				Century: 0 - 1 Hours: 00 - 23
3	X	X	X	X	X	Day			Day: 00 - 07
4	X	X	10 Date		Date				Date: 01 - 31
5	X	X	X	10M.	Month				Month: 01 - 12
6	10 Years				Years				Year: 00 - 99
7	OUT	FT	S	Calibration					Control

Legend for Table 4-31:

CEB = Century enable bit
CB = Century bit
FT = Frequency test bit
OUT = Output level
ST = Stop bit
S = Sign bit

Note ...

When the RTC has once been stopped due to low voltage, it is necessary to re-initialize the "Seconds", "Minutes" and "Hours" registers before it will run again.

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4.5 EEPROMs

Access to the EEPROMs is effected via the I2C bus of the MPC107. The EEPROMs use the I2C address 0xA0 (System) and the address 0xA2 (User). Write protection is achieved by installing 0 ohm resistors R333 (System) and R337 (User). Default is unprotected.

For more detailed information please refer to the manuals for the MICROCHIP 24C64 and the MOTOROLA® MPC107 (I2C bus).

4.6 Digital Temperature Sensor, LM75

Access to the onboard digital temperature sensor (DTS) is effected via the I2C bus of the MPC107. The DTS uses the I2C address 0x90.

For more detailed information please refer to the manuals for the National Semiconductor LM75 and the MOTOROLA® MPC107 (I2C bus).

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Chapter 5

NetBootLoader

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5. NetBootLoader

This CP620 board is delivered with the NetBootLoader software already programmed into the onboard soldered Flash memory. The NetBootLoader itself is a software utility which initializes the module for operation before turning control over to either an application or to an operator. This software also provides the capability to monitor and control the operation of the NetBootLoader itself, display system status information, to program executable code and data to the Flash memory, and to load and start application software.

To attain full operational capability, the NetBootLoader FLASH must be programmed by the user with application software. Once the application has been programmed to Flash memory, the NetBootLoader will support the complete boot operation. The following chapters describe the functioning of the NetBootLoader and how to program the Flash memory.

Note ...

The following description assumes a standard CPU board with appropriate hardware. In the event such hardware is not available, disregard the text that applies to the missing hardware and proceed as appropriate.

5.1 General Operation

Upon power on or a system reset, the NetBootLoader is started. The CPU board is configured for operation and control is either passed to an application or an operator. In the event a valid application has been programmed into the Flash memory and no operator intervention takes place, the application is copied from FLASH into SDRAM and control is passed to the application. If the NetBootLoader does not find a valid application or operator intervention has occurred, control is passed to the operator. The operator now has control to determine the system status, make configuration changes, read or program the Flash memory, or to restart or shut down the system.

The operator command interfacing with the NetBootLoader is accomplished either via the TERM serial port or the Ethernet port. During the boot operation a command interpreter is started which allows the operator to input commands to the NetBootLoader. Prior to interfacing via the Ethernet port the network must be configured. This is done via the TERM port.

5.2 NetBootLoader Interfaces

There are four possibilities to interface with the NetBootLoader:

- Via the ABT (Abort) switch
- Via the TERM serial interface
- Via the SER0 serial interface
- Via the Ethernet interface

Gaining access to the NetBootLoader is a function of the contents of the Flash memory and the “BootWaitTime” setting. If there is no valid application programmed into the Flash memory, the boot operation automatically terminates after the CPU board has been initialized and control is passed to the command interpreter. If there is a valid application in the Flash memory the boot operation is delayed according to the setting of the boot wait time. The green user LED (U) on the front panel flashes indicating that the boot operation is in a wait state. During this time the operator may intervene in the boot operation either by pressing the ABT (Abort) switch, entering the “abort” command via the TERM interface, or by performing a successful telnet login via the Ethernet interface. If the operator does not intervene, the boot operation is continued after the boot wait time has been exceeded.

5.2.1 ABT (Abort) Switch

The ABT switch, located on the CPU board front panel, provides the operator with the ability to directly terminate the boot operation during the boot wait time which is indicated by the "U" LED blinking. This is the sole purpose of the ABT switch during the NetBootLoader operation.

5.2.2 TERM Serial Interface

The TERM serial port, if realized on the carrier board, is used to provide direct operator interfacing to the NetBootLoader. As soon as the CPU board has been initialized this port is activated and the operator may input commands. During the boot wait time the operator may terminate the boot operation and take control of the NetBootLoader. Once the boot wait time is exceeded the command interpreter is deactivated and the operator no longer has access to the NetBootLoader.

The TERM serial interface may either be directly connected to a terminal device or may interface with a terminal emulator.

5.2.3 SER0 Serial Interface

The SER0 serial port is used to provide the NetBootLoader with the ability to access Motorola S-Records for programming an application to FLASH. No command interpreter is available for this interface.

5.2.4 Ethernet Interface

The Ethernet interface provides the capability of remotely interfacing with the NetBootLoader. Prior to using this interface it is necessary to configure the NetBootLoader network settings. This is accomplished via the TERM interface. Once the network settings have been made, the remote operator has the same capabilities as with the TERM interface. During the boot wait time the operator gains control of the NetBootLoader by logging into it via the Ethernet interface. This causes the boot operation to be terminated and gives control to the remote operator.

The Ethernet interface uses the telnet protocol for operator interfacing with the NetBootLoader. In addition to the operator interface via Ethernet, the NetBootLoader also uses the Ethernet interface for ftp server access.

5.3 NetBootLoader Functions

In addition to initializing the CPU board for operation and the loading and starting of applications, the NetBootLoader provides the following operator monitor and control functions:

- NetBootLoader control
- system status monitoring
- ftp server access
- FLASH reading and programming operations
- Motorola S-Record acquisition

These functions are described in detail in the following chapters.

Note ...

The command title (CMD TITLE) is expressed in capital letters and is not the same as the syntax of the command. The command syntax is always written using small letters

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5.3.1 NetBootLoader Control

The NetBootLoader provides various functions for controlling the operation of the NetBootLoader itself as well as the setting of operational parameters. The following table provides an overview of available NetBootLoader control functions.

Table 5-1: NetBootLoader Control Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
ABORT	-	Terminate boot wait	
BW	Boot Wait	Set or display BootWaitTime	
HELP or ?	-	Display online HELP pages	
LOGOUT	-	Terminate telnet session	
NET	-	Set network parameters	Must be set before attempting telnet login
PASSWD	Password	Set telnet password	Must be set before attempting telnet login
PF	Port Format	Set serial port parameters	Used for both TERM and SER0 ports
RS	Reset	Resets system	

5.3.2 System Status Monitoring

The NetBootLoader provides various functions for monitoring the overall status of the system during the operation of the NetBootLoader. The following table provides an overview of available system status monitoring functions.

Table 5-2: System Status Monitoring Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
CHECK	-	Application validation	Verifies validity of user image programmed to FLASH
INFO	-	Display system information	
MD	Memory Display	Display memory contents	Applies to all visible memory
PCI	-	Display PCI device information	
PING	-	Verify network status	
VER	Version	Display version number of NetBootLoader	

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5.3.3 ftp Server Access

The NetBootLoader provides various functions for interfacing with an ftp server. The following table provides an overview of available ftp server functions.

Table 5-3: ftp Server Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
BYE	-	Terminate session with ftp server	
CD	Change Directory	Change ftp server directory	
GET	-	Download a file from ftp server	Only for executable applications. Data buffer is target.
LOGIN	-	Login to ftp server	
LS	List Directory	List ftp server directory	Lists contents of directory.
PUT	-	Upload a file to ftp server	Data buffer is source.
PWD	Print Working Directory	Display current ftp server directory	Lists name of directory

5.3.4 FLASH Operation

The NetBootLoader provides various functions for performing operations with Flash memory. The following table provides an overview of available FLASH operation functions.

Table 5-4: FLASH Operation Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
CLONE	-	Program NetBootLoader to FLASH	Uses data buffer or socket as source
LF	Load FLASH	Program application to FLASH	Uses data buffer as source
SF	Store FLASH	Reads FLASH to data buffer	Uses data buffer as target

5.3.5 Motorola S-Records

The NetBootLoader provides one function for acquiring Motorola S-Records. The following table provides an overview of this function.

Table 5-5: Motorola S-Records Commands

CMD TITLE	ALIAS	FUNCTION	REMARKS
SL	SLoad	Download Motorola S-Records	Uses data buffer as target

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5.4 Operating the NetBootLoader

5.4.1 Initial Setup

The CPU board is delivered with the NetBootLoader already installed in the onboard soldered FLASH and is ready for operation. However, in order for the CPU board to be used in a system, application software must be made available for use. This is accomplished by programming the application also to the onboard soldered Flash memory where the NetBootLoader is located.

Upon initial power up the NetBootLoader is started automatically. As soon as the NetBootLoader has completed initialization of the CPU board, it checks to see if there is a valid application programmed in FLASH and at the same time initiates a command interpreter which the operator can access either via the TERM or telnet interfaces. If there is no valid application in memory, the NetBootLoader terminates the boot operation, and waits for operator intervention. As this is the case when the CPU board is first powered up, the operator now has the opportunity to program an application.

Prior to programming an application it may be necessary to configure the NetBootLoader or perform other functions depending on the user's application development environment or application requirements. Once this has be accomplished and the application has been programmed, the CPU board is ready for operation.

The following chapters provide information on how to set up and operate the NetBootLoader itself, initiation of the telnet interface, and how to program an application to FLASH.

5.4.2 Accessing the NetBootLoader

Initial access to the NetBootLoader can only be achieved via the TERM interface. Prior to using the telnet interface, the Ethernet parameters must be set and this can only be accomplished initially via the TERM interface. Once valid Ethernet parameters and the telnet login password have be set, the telnet interface is available for operation.

Use of the TERM interface requires either a terminal or a terminal emulator. Use of the telnet interface requires a remote telnet login to the NetBootLoader.

Availability of the command interpreter depends on the system status. If there is no valid application programmed, the command interpreter is available as long as the operator requires it. If a valid application is programmed, the command interpreter is only available for the duration of the boot wait time. If the operator requires the command interpreter for a longer time he must terminate the boot operation before the boot wait time is exceeded.

Upon initiation of the command interpreter, a prompt is sent to the TERM interface and commands may be entered. To gain access to the NetBootLoader from a remote location via Ethernet a telnet login must be performed. If the boot wait time has not been exceeded, a telnet login automatically terminates the boot operation and a command prompt is sent to the telnet remote interface.

Once the operator has control of the NetBootLoader, he may perform any required action. To continue with the operation of the CPU board, the system must either be cold started or the operator must issue a "reset" command. In either event, the NetBootLoader is restarted and the boot operation begins anew.

5.4.3 NetBootLoader Configuration

There are several NetBootLoader commands which provide the operator with the capability to configure specific parameters which are used by the NetBootLoader for interfacing operations. These commands are:

- BW (BootWait)
- NET
- PASSWD
- PF (Port Format)

Default settings are available for all the above commands except for “net” which is dependent on the application environment.

5.4.3.1 BW

This command is used to display or set the actual boot wait time used by the NetBootLoader to delay the boot operation before proceeding with the loading and starting of an application. If this time is set too short it may only be possible to gain access to the NetBootLoader via the MC1 (Abort) signal.

The BootWaitTime value is stored in the boot section of the serial EEPROM. This section is validated with a CRC code to avoid the setting of random parameters.

Note ...

If the CRC of the boot section is not valid, changing the BootWaitTime will have no effect because the “bw” command does not validate an invalid CRC. In this case, a default timing of 5 seconds is always used.

To validate an invalid CRC, an operating system utility must be used, or, alternatively, the “-f” option of the “bw” command must be issued.

Warning!

Using the “bw -f” command to validate invalid entries may adversely impact the operation of the operating system.

5.4.3.2 NET

This command is used to set or display the parameters for the configuration of the Ethernet interface of the CPU board. The Ethernet interface is only available after these settings have been made. Once these settings have been made, the system must be cold started or reset for them to take effect.

5.4.3.3 PASSWD

This command is used to set the password used by the NetBootLoader for the operation of the telnet interface. No password is required for access from the TERM interface.

5.4.3.4 PF

This command is used to set the port parameters for the TERM and SER0 serial interfaces only for the current operator session. The next system restart will cause these settings to revert to the default settings of: 9600 Baud, 8 bits per character, 1 stop bit, and no parity. This is done to preclude a system lockout when restarting due to incompatible settings.

5.4.4 telnet Login

A telnet login to the NetBootLoader is only possible during the boot wait time and only after the Ethernet network parameters have been set.

To effect a telnet login the operator performs the standard telnet login procedure during the boot wait time. The NetBootLoader responds by suspending the boot wait and requests a login password. The operator then enters a password. If the password is valid, the boot wait is terminated and the operator can now access the NetBootLoader. If the password is invalid, the telnet login procedure is terminated and the boot operation continues.

In the case of an invalid password, the login procedure may be repeated as often as required within the boot wait time. Once the boot wait time is exceeded, a telnet login is no longer possible.

5.4.5 FLASH Operations

To achieve an operable system for an application, the application software must be programmed to FLASH. The NetBootLoader supports the programming of the application to FLASH. In addition to this, it also supports the updating of the NetBootLoader itself as well as data transfer from the FLASH to the data buffer and from the data buffer to an ftp server. The following chapters provide information on performing the various types of FLASH operations.

5.4.5.1 FLASH Offsets

All FLASH is treated as one uniform FLASH, regardless of the physical addresses of the devices involved. All offsets are based from the beginning of the FLASH area. This means that 0x0 is the beginning of the first FLASH bank. The NetBootLoader itself is located at the beginning of the FLASH area and for this reason this area cannot be used for application image programming. To display an overview of the current FLASH organization use the “info” command.

If the application image is an operating system (which is the default case), it must be programmed without an offset. When such an image is programmed to FLASH, the image length and CRC information is also programmed along with the image to FLASH. This information is used by the NetBootLoader to determine the validity of the image during the boot operation. During system startup, a valid image is copied to SDRAM address 0x0 and started at offset 0x100 after the boot wait time is exceeded.

If an offset is specified, the image will be programmed exactly at this offset without adding length or CRC information. This option is intended for the storing of configuration information which is required to be located in FLASH.

5.4.5.2 Programming an Application

The application image itself must be compiled and linked to run from the SDRAM base address 0x0 of the CPU. The image must contain executable PowerPC® code at offset 0x100 which is the usual case with ROM/Flash images.

Gaining access to the image for programming to FLASH depends on where it is located. The NetBootLoader can access three different sources for images:

- ftp server
- Motorola S-Records
- memory within the visible address range of the CPU board

The NetBootLoader uses a single data buffer for downloading an image from an ftp server or an image as Motorola S-Records. These images must first be downloaded to the data buffer prior to being programmed to FLASH. An image located within the visible address range of the CPU board is directly accessible for programming.

To access an image located on an ftp server, the “get” command is used. To perform Motorola S-Record acquisition, the “sl” (SLoad) command is used. Once the image is in the data buffer, the FLASH is programmed using the “lf” (Load Flash) command. For an image within visible memory, the “lf” (LoadFlash) command is used to program directly to FLASH.

5.4.5.3 ftp Server Access

To gain access to an application image file stored on an ftp server the Ethernet interface is used. Images are downloaded to the data buffer using the ftp protocol. To use this interface the Ethernet parameters must first be set and then the system must be restarted. During boot wait the operator must gain control of the NetBootLoader and perform an ftp server login. After a successful login, the operator then locates the image file required and downloads it to the data buffer. As with any type of server session, the operator should logout when the session is finished.

Note ...

The commands “get” and “ls” use the same data buffer. Therefore if an “ls” command is issued after a “get” command the data buffer will be overwritten. If an “lf” command follows the “ls” the NetBootLoader refuses to program the overwritten data buffer to the FLASH.

5.4.5.4 Motorola S-Records

The NetBootLoader will also accept Motorola S-Records as an application image. The “sl” command accepts S1, S2 and S3 records. Operation is terminated by the appropriate S9, S8 or S7 record. Other types of records are ignored.

The checksum of every record except end records is checked. Bad records are rejected by the NetBootLoader. The address range of every record is also checked. Records which fall outside of the internal buffer are rejected.

The records must be 0-based. This means that its address must correspond to the address where they will be loaded in the data buffer relative to its start. If necessary, the base address can be modified with the -o option of the “sl” command.

Note ...

If the data buffer is programmed to FLASH without the -o option (program a startable image) the downloaded image is copied to RAM during startup and is executed there. For this reason application images which require to be programmed must start at the address 0x0.

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The image must start at the absolute address 0x0 and must contain executable PowerPC® code at the absolute address 0x100. If S1 or S2 record input is preferred, please note that these records only include 16 and 24-bit wide addresses. If no switch to another record type is included it must be ensured that the code is not larger than the address range covered.

Note ...

Neither the “sl” nor “lf” command can be used to program Motorola S-Records to RAM areas.

For accessing the Motorola S-Records, both the TERM and SER0 interfaces can be used. The MC6 (LED1) signal is asserted alternately at a low rate while downloading indicating that the transfer is in progress. The transfer itself may take several minutes to complete.

Ensure that the XON/XOFF protocol is used on the host side. This is a fixed setting and cannot be changed. Additionally, ensure that the host does not stop transmission after a number of lines (e.g. OS-9: use the ‘nopause’ attribute).

The TERM and SER0 serial interface parameters can be modified with the “pf” command.

5.4.6 Updating the NetBootLoader

In addition to programming an application to FLASH, the NetBootLoader itself can be updated. The new version of the image is made available via an ftp server.

5.4.6.1 Updating With an Image Loaded Via an ftp Server

The image is downloaded in the same way as an application image (refer to chapter 5.4.5.3). The new version of NetBootLoader image is then programmed using the “clone -n” command.

5.4.7 Uploading a FLASH Area

The NetBootLoader also has the possibility to upload certain areas of the FLASH to a host using the Ethernet interface. To use this interface the Ethernet parameters must first be set and then the system must be restarted. During boot wait the operator must gain control of the NetBootLoader and perform an ftp server login. After a successful login, the operator then stores the FLASH area to be uploaded to the local data buffer using the “sf” command. Using the “put” command transfers the contents of the data buffer to the ftp server. As with any type of server session, the operator should logout when the session is finished.

5.5 Plug and Play

On the CPU board the NetBootLoader includes “Plug and Play” functionality. This ensures that the board is completely initialized and that all resources necessary for PCI devices (addresses, interrupts etc.) are assigned automatically. This important feature has the advantage that conflicts do not arise when PCI devices are added or removed. Furthermore, the operating system itself does not include the board initialization code.

5.6 Porting an Operating System to the CPU Board

The image for the absolute address 0x0 should be linked with an entry point at the absolute address 0x100.

One should not attempt to reassign the PCI BAR registers. The assigned values should be read back and these should always be used in the drivers.

The “interrupt line” field in the PCI configuration header is initialized with the IRQ line number to which the INTA of the device is routed.

It is not necessary to rewrite the “EUMBBAR” field in the KAHLUA (MPC 8240) configuration space as this has already been done by the NetBootLoader. The existing value should be used.

Downloaded images are never executed from the FLASH due to the fact that on the CPU board it is paged. The programmed image is always downloaded to SDRAM, the absolute address 0x0 being downloaded first. There is no configuration option available to amend this process. If it is necessary to relocate the image to another address after download, simply add a small assembly routine at the beginning of the code which will move the image to the correct address.

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5.7 Commands

The following commands are available with the NetBootLoader. Where an ellipsis (…) appears in the command syntax it means that the command is continued from the previous line. Observe any spaces that may be between the ellipsis and the remainder of the command.

ABORT

FUNCTION:	Terminate the NetBootLoader boot operation
SYNTAX:	`abort`
DESCRIPTION:	This command is used by the operator to terminate the boot operation during the boot wait time to allow the operator to perform other NetBootLoader operations. To be asserted it must be issued during the boot wait time which is indicated by the alternating assertion of the MC6 (LED1) signal.

BW

FUNCTION:	Set or display the parameters of the boot wait function of the NetBootLoader
SYNTAX:	`bw [<time>│ -f]` where: bw — command <time> — parameter: value: seconds 1, 2, 5, 10, 20, 50 -f — option: force CRC update

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BW

DESCRIPTION:	The command “bw” displays the parameter “<time>” setting. The parameter “<time>” stipulates the waiting time in seconds that the boot operation is delayed before the application is loaded and started. No values other than these are supported. Bear in mind when setting the boot wait time that the MC6 (LED1) signal is asserted alternately at the rate of two times a second. Therefore, if the boot wait is set to 1 second the MC6 signal will only be alternately asserted two times. The option “-f” is used to force updating of the CRC value of boot section of the EEPROM. For further information refer to chapter 5.4.3.1.
USAGE:	Display setting of “<time>” parameter COMMAND/RESPONSE: **`bw`** **`WaitTime: 20`**
	Set boot wait time to 50 seconds COMMAND/RESPONSE (none): **`bw 50`**

BYE

FUNCTION:	Terminate an ftp server session
SYNTAX:	**`bye`**
DESCRIPTION:	An ftp server session which has been established with the command “login” is terminated with the command “bye”.

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CD

FUNCTION:	Change the current ftp server directory
SYNTAX:	`cd <new-path>` where: cd — command <new-path> — parameter: string new directory path
DESCRIPTION:	If an ftp server session has been established with the “login” command, the command “cd” is used to change the current ftp server directory. The argument “<new-path>” may be an absolute or relative path. The format depends on what the server accepts. For example, UNIX hosts require that the directory names must be entered exactly in the same case.

CHECK

FUNCTION:	Verify validity of application programmed to FLASH
SYNTAX:	`check`
DESCRIPTION:	When an application is programmed to FLASH, a CRC is performed and the results are stored in FLASH along with the application. The “check” command is used to verify that the current application image in FLASH is valid.

USAGE:	Veriy valid application is stored in FLASH
	
	COMMAND/RESPONSE:
	
	`check`
	`Check userimage CRC: ok`

CLONE

FUNCTION:	Program the NetBootLoader to FLASH
SYNTAX:	`clone [-n]` where: clone command -n option: program from data buffer
DESCRIPTION:	To update the NetBootLoader itself, the command “clone” is used. The application image source for programming is the data buffer. The image must first be downloaded to the data buffer from an ftp server. To program from the data buffer, the command “clone -n” is used. The new image is checked for validity. If an image is invalid, the update is aborted. Additionally, the operation must be confirmed by typing the word “yes”. Any other or no input will cancel the operation.

USAGE:	Program NetBootLoader (normal operation)
	COMMAND/RESPONSE:
	`NetBtLd> clone -n`
	`clone: Fixup FLASH info from ftp buffer`
	`This will overwrite the current ...`
	`NetBootLoader, are you sure? [no] yes`
	`clone: System transferred; Start again, ...`
	`assure that Bootjumper is removed.`
	`NetBtLd>`
	Note: When responding to the overwrite query, “yes” must be spelled out. Any other response will terminate the cloning operation.

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CLONE

	Program NetBootLoader (image not valid)
	COMMAND/RESPONSE:
	`NetBtLd> clone -n`
	`clone: Fixup FLASH info from ftp buffer`
	`Image length invalid, image is damaged, abort.`
	`NetBtLd>`

GET

FUNCTION:	Download file from ftp server
SYNTAX:	`get <filename>` where: get — command <filename> — parameter: string name of image file to be downloaded, or path and name of image file to be downloaded
DESCRIPTION:	To download a file from the ftp server to the local data buffer, the command “get” is used. A successful ftp server login must be carried out before a file can be downloaded and the file must be in binary format. The argument “<filename>” must refer to an existing and accessible file on the server and the syntax must follow the requirements on the server, e.g. case sensitiveness. The argument may also include a path specification, if the server supports this.

HELP or ?

FUNCTION:	Display online help pages
SYNTAX:	`help` `?`
DESCRIPTION:	This command displays the online help pages. The display of the help text varies between the different CPUs reflecting their differences. The syntax of every command and a brief description is shown. The display output pauses after every page. The output can be continued with any key. Entering a “.” (period) aborts the help function.

INFO

FUNCTION:	Display system information
SYNTAX:	`info`
DESCRIPTION:	The command “info” is used to display an information summary for the running system. The CPU type, the board type, and the detected FLASH layout are displayed.

LF

FUNCTION:	Load Flash

SYNTAX:	`lf [-o[=]<offset> [-k]]`
	
	`… [-m[=]<adr> -l[=]<len>]`
	
	where:
	lf — command
	-o — option: offset
	<offset> — parameter: value: hexadecimal; program to FLASH offset of ...
	-k — option: keep; retain surrounding contents
	-m — option: memory (address)
	<adr> — parameter: value: hexadecimal; absolute address of image to be programmed
	-l — option: length
	<len> — parameter: value: hexadecimal; length of image to be programmed

DESCRIPTION:	Without parameters, the FLASH is programmed using the contents of the data buffer. If no image is available in the data buffer, the FLASH programming is terminated. If no offset option ("-o") is specified the image is considered to be valid and is therefore added along with CRC and length information. If the CRC is determined to be valid during the next startup, the image is copied to the absolute address 0x0 and started at 0x100 after the boot wait time has been exceeded. Normally, the local data buffer holds the image to be programmed. However, if the "-m" and "-l" parameters are specified, the image is programmed from the absolute address specified. If "<offset>" is specified, the contents are programmed exactly at this offset in FLASH. No length and no CRC information is added. The "-k" option can be specified to prevent deletion of the surrounding FLASH contents.

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LF

DESCRIPTION:	FLASH memory can only be erased sector-wise. If an image is programmed to a certain offset with the "-o" option, at least this sector (and maybe one or more of the following sectors depending on the size of the image) will be erased. The "-k" option can be used to retain the surrounding data, however, this slows down the operation significantly. To achieve fast programming of parameter images without destroying other FLASH contents, the data should be placed at a sector boundary and the sector(s) must not contain any other data or executable images. If organized this way, use of the "-k" option can be avoided. Note: The "lf" command cannot be used to program the NetBootLoader.
USAGE:	Program FLASH from data buffer and add CRC and image length COMMAND/RESPONSE (none): `lf`
	Program FLASH from data buffer to offset 0xF4240 COMMAND/RESPONSE (none): `lf -o=f4240`
	Program FLASH from visible address at 0x87000000 for length of 0x123456 COMMAND/RESPONSE (none): `lf -m=87000000 -l=123456`
	Program FLASH from data buffer to offset 0xF4240 and retain adjacent FLASH contents COMMAND/RESPONSE (none): `lf -o=f4240 -k`

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LOGIN

FUNCTION:	Initiate ftp server session
SYNTAX:	`login <ip-of-host> <username> [<password>]` where: login — command <ip-of-host> — parameter: value: numerical string IP address of host: nnn.nnn.nnn.nnn <username> — parameter: value: string ftp server “username” <password> — parameter: value: string user’s password
DESCRIPTION:	The command “login” is used to establish an ftp server session. The “<ip-of-host>” must be specified as four numbers separated by single dots. The “<password>” parameter is not necessary if the server does not request one.
USAGE:	Initiate ftp server session COMMAND/RESPONSE: `login 192.168.47.12 johndoe mypassword` (Response is dependent on the server accessed)

LOGOUT

FUNCTION:	Terminate telnet session with NetBootLoader
SYNTAX:	`logout`
DESCRIPTION:	A remote telnet session will be terminated with the command “logout”. No application is loaded and started if the session is terminated with “logout”. The NetBootLoader waits for a new session to be initiated or for a command entry from the serial console.

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LS

FUNCTION:	Display listing of the current ftp server directory
SYNTAX:	`ls`
DESCRIPTION:	To display a listing of the current ftp server directory the command "ls" is used. This command downloads the listing to the data buffer and then the listing is displayed. Any previously loaded image in the data buffer is overwritten. If an attempt is then made to program the FLASH after the "ls" command has been issued it will fail.

MD

FUNCTION:	Display visible memory
SYNTAX:	`md [<adr>]` where: md command <adr> parameter: value: hexadecimal starting address of a visible memory area
DESCRIPTION:	To display a visible memory area the command "md" is used. The first time the command "md" is issued, visible memory contents starting at the address 0x0 are displayed if no "<adr>" parameter is used. If issued again without the "<adr>" parameter, the display starts with the end address of the previous display. Data is displayed as hexadecimal 32-bit words and as ASCII dump.

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NET

FUNCTION:	Set or display the parameters for the Ethernet interface
SYNTAX:	**`net [<ip-addr>] [-netmask <netmask>]`** **`…[-gw <gateway>] [-f]`** where: net — command <ip-addr> — parameter: value: numerical string IP address of CPU board: nnn.nnn.nnn.nnn -netmask — option: netmask <netmask> — parameter: value: numerical string netmask of CPU board: nnn.nnn.nnn.nnn -gw — option: gateway <gateway> — parameter: value: numerical string gateway address for network: nnn.nnn.nnn.nnn -f — option: force CRC update
DESCRIPTION:	To set or display the parameters of the Ethernet interface the command “net” is used. Initially the CPU board does not have a valid Ethernet interface configuration, and, therefore, this interface is inoperable. The initial configuration must be done from the TERM interface using the command “net ... -f”. Using the “-f” option forces a CRC to be performed and stored along with the other configuration parameters in the serial EEPROM. Once the initialization of the Ethernet interface is done, the CPU board must be restarted for the parameters to take effect. Later changes to the parameters do not require the use of the “-f” option to force a CRC. This is done automatically. Only in the event that the Ethernet interface does not properly initialize, may it be necessary to re-enter the parameters using the “-f” option.

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PASSWD

FUNCTION:	Set the telnet password
SYNTAX:	`passwd [-f	-d]` where: passwd — command -f — option: if password is not known -d — option: disable disable telnet login (remote access)
DESCRIPTION:	To set the password for telnet sessions with the NetBootLoader the command "passwd" is used. This command is interactive, meaning that after it is issued, the NetBootLoader responds with an appropriate request to the operator which must be properly acknowledged or the operation fails (refer to USAGE below). To set the password in the event it is unknown, use the option "-f". This is can only be accomplished from the TERM interface and not from the Ethernet interface. With the option "-d", the remote telnet login can be disabled by invalidating the password.

USAGE:	Set password
	COMMAND/RESPONSE:
	`NetBtLd> passwd`
	`Old Password: *****`
	`New Password: *****`
	`Type again   : *****`
	`NetBtLd>`
	(The old password must be known)

	Set password when the old password is not known
	COMMAND/RESPONSE:
	`NetBtLd> passwd`
	`New Password: *****`
	`Type again   : *****`
	`NetBtLd>`

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PCI

FUNCTION:	Display PCI information
SYNTAX:	`pci`
DESCRIPTION:	The command “pci” is used to display detailed information on all detected PCI devices. The bus number, device number, function number, vendor, and device IDs are displayed together with the configured base addresses and the assigned IRQ number.

PF

FUNCTION:	Set or display the serial port parameters (format)

SYNTAX:	`pf [<port> [<baud>][/[<bitschar>]`
	`…[/[<parity>][/<stops>]]]]`
	where:
	pf — command
	<port> — parameter: string: “term” or “ser0” defines serial port to be configured
	<baud> — parameter: value: numeric: “50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19200, 38400, 115200” defines the baud rate for the port
	<bitschar> — parameter: value: numeric: “7” or “8” defines the number of bits per character
	<parity> — parameter: string: “n” (none), “o” (odd), “e” (even) defines parity to be used
	<stops> — parameter: value: number: “1”, “2” defines number of stop bits

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PF

DESCRIPTION:	To set or display the operational parameters for the available serial interfaces the command “pf” is used. At startup the settings for the “TERM” and “SER0” interfaces are always set to the default values (9600/8/n/1). This is to avoid a possible system lockout. If other settings are required during operation of the NetBootLoader they may be made. If changes are made, it must be ensured that corresponding parameters are used for the operator consle. Issuing this command without parameters being specified will display the current serial port settings. Syntax-wise, no spaces are permitted between the parameters and they must be separated with a slash. Not all parameters must be specified, but the “/” characters must be present to distinguish the different parameters from each other. The sequence can be aborted after every option.
USAGE:	Set “TERM” to 300 Baud, 7 Bits/char, odd parity, and 2 stop bits COMMAND/RESPONSE (none): `pf term 300/7/o/2`
	Set the bits per character parameter of “SER0” to 7 COMMAND/RESPONSE (none): `pf ser0 //7`
	Set the stop bits parameter of “SER0” to 2 COMMAND/RESPONSE (none): `pf ser0 ///2`

PING

FUNCTION:	Verify operability of the Ethernet interface

SYNTAX:	`ping <ip_addr> [-c <count>] [-s <size>]`
	`… [-w <wait>]`
	
	where:
	ping — command
	<ip-addr> — parameter: value: numerical string
	IP address of target: nnn.nnn.nnn.nnn
	-c — option: count
	<count> — parameter: value: numeric: “[n ...]n”
	number of packets to send
	-s — option: size
	<size> — parameter: value: numeric: “[n ...]n”: bytes
	size of packet to send
	-w — option: wait
	<wait> — parameter: value: numeric: “[n ...]n”: seconds
	wait time between packets

DESCRIPTION:	To verify the operational status of the Ethernet interface the command “ping” is used. This command tests the network connection and target server’s ability to respond. If no other parameters are specified, four requests will be sent. This can be changed with the parameter “-c”. The typical size of a ping packet can be changed with the parameter “-s” and the time between requests, which is typically one second, can be changed with the parameter “-w”. Responses to the “ping” command are dependent on the performance of the network.
USAGE:	Send four packets COMMAND/RESPONSE: `ping 192.192.158.7`
	Send ten packets, 100 bytes long, and wait two seconds between packets COMMAND/RESPONSE: `ping 192.192.158.7 -c 10 -s 100 -w 2`

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PUT

FUNCTION:	Upload contents of the data buffer to the ftp server.
SYNTAX:	`put <filename>` where: put — command <filename> — parameter: string file name to be used for contents of data buffer to be uploaded
DESCRIPTION:	To upload the contents of the data buffer to a file on an ftp server, the command “put” is used. The file indicated by the parameter “<filename>” is created on the server. In the event that a file with this name already exists, its contents will be overwritten.

PWD

FUNCTION:	Display the current ftp server directory.
SYNTAX:	`pwd`
DESCRIPTION:	If a ftp connection has been established with the “login” command, the command “pwd” is used to display the complete path of the current directory on the ftp server.

RS

FUNCTION:	Reset the system
SYNTAX:	`rs`

RS

DESCRIPTION:	To permit the operator to force a restart of the system, the command “rs” is used. This command terminates the NetBootLoader command interpreter and resets the entire system, generating a system reset with the onboard watchdog. If this command is issued over a remote telnet connection, the telnet session is terminated prior to the generation of the reset.

SF

FUNCTION:	Store FLASH contents to data buffer
SYNTAX:	`sf -o[=]<offset> -l[=]<length>` where: sf — command -o — option: offset <offset> — parameter: value: hexadecimal relative offset to start of FLASH contents to be stored to the data buffer -l — option: length <length> — parameter: value: hexadecimal length of FLASH contents to be stored to the data buffer
DESCRIPTION:	With the command “sf” a selected portion of the FLASH contents may be copied to the local data buffer, e.g. for a subsequent upload to the ftp server with the “put” command. The “<offset>” parameter refers to the relative offset within the FLASH area similar to the “lf” command. The parameter “<length>” specifies the length to store.
USAGE:	Store 64 kB of FLASH contents to the data buffer beginning at an offset of 1 MB COMMAND/RESPONSE (none): `sf -o=100000 -l=10000`

SL

FUNCTION:	Download Motorola S-Records to data buffer
SYNTAX:	`sl [-o[=]<offset>] [-u]` where: sl command -o option: offset <offset> parameter: value: hexadecimal: unsigned offset to be subtracted from each record's address -u option: upper
DESCRIPTION:	With the command “sl” Motorola S-Records are downloaded to the data buffer and the record addresses modified accordingly as required for SDRAM operation (for copying to 0x0). The “<offset>” parameter may be used to change the record base to 0x0. The “-u” option selects the SER0 interface as source for the S-Records.
USAGE:	Download S-Records to data buffer and reduce each record’s address by 0x10000. COMMAND/RESPONSE (none): `sl -o=10000`

VER

FUNCTION:	Display version number
SYNTAX:	`ver`
DESCRIPTION:	The command “ver” displays the actual version number of the NetBootLoader.

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Chapter 6

Power Consumption

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6. Power Consumption

6.1 System Power

The considerations presented in the ensuing chapters must be taken into account by system integrators when specifying the CP620 system environment.

6.1.1 CP620 Baseboard

The CP620 baseboard itself has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the CP620 should be carefully tested to ensure compliance with these ratings.

Table 6-1: Maximum Input Power Voltage Limits

SUPPLY VOLTAGE	MAXIMUM PERMITTED VOLTAGE
+3.3 V	+3.6 V
+5 V	+5.5 V
+12 V	+14.0 V
-12 V	-14.0 V

Warning!

The maximum permitted voltage indicated in the table above must not be exceeded. Failure to comply with the above may result in damage to your board.

The following table specifies the ranges for the different input power voltages within which the board is functional. The CP620 is not guaranteed to function if the board is not operated within the prescribed limits.

Table 6-2: DC Operational Input Voltage Ranges

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE	RECOMMENDED RANGE
+3.3 V	3.2 V min. to 3.47 V max.	3.3 V min. to 3.47 V max.
+5 V	4.85 V min. to 5.25 V max.	5.0 V min. to 5.25 V max.
+12 V	11.4 V min. to 12.6 V max.	12 V min. to 12.6 V max.
-12 V	-11.4 V min. to -12.6 V max.	Only for PMC

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6.1.2 Backplane

Backplanes to be used with the CP620 must be adequately specified. The backplane must provide optimal power distribution for the +3.3 V, +5 V and +12 V power inputs. If a PMC module is used on the CP620, an additional power input of -12 V is required.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided. It is recommended to use POSITRONIC or M-type connector backplanes and power supplies where possible.

6.1.3 Power Supply Units

Power supplies for the CP620 must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

As the design of the CP620 has been optimized for minimal power consumption, the power supply unit shall be stable even without minimum load.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for die resistance variations.

Note ...

Non-industrial ATX PSUs require a greater minimum load than a single CP620 is capable of creating. When a PSU of this type is used, it will not power up correctly and the CP620 may hangup. The solution is to use an industrial PSU or to add more load to the system.

If DC/DC power supplies are used, please ensure that the external main supply provides sufficient power in order to start-up the system properly. The external main supply should provide at least as much power as the system power supply is able to provide taking into consideration the inrush current.

Warning!

An underdimensioned power supply may cause damage to system components.

The start-up behavior of CPCI and PCI (ATX) power supplies is critical for all new CPU boards. These boards require a defined power of sequence and start-up behavior of the power supply. The required behavior is described in the ATX (http://www.formfactors.org/FFDetail.asp?FFID=1&CatID=2) and the CPCI (PICMG, http://www.picmgeu.org/) specification.

6.1.3.1 Start-Up Requirement

Power supplies must comply with the following guidelines, in order to be used with the CP620.

- Beginning at 10% of the nominal output voltage, the voltage must rise within > 0.1 ms to < 20 ms to the specified regulation range of the voltage. Typically: > 5 ms to < 15 ms.
- There must be a smooth and continuous ramp of each DC output voltage from 10% to 90% of the regulation band.
- The slope of the turn-on waveform shall be a positive, almost linear voltage increase and have a value from 0 V to nominal Vout.

6.1.3.2 Power-Up Sequence

The +5 VDC output level must always be equal to or higher than the +3.3 VDC output during power-up and normal operation.

The time from +5 VDC until the output reaches its minimum in regulation level and from +3.3 VDC until the output reaches its minimum in regulation level must be < 20 ms.

6.1.3.3 Tolerance

The tolerance of the voltage lines is described in the CPCI specification (PICMG 2.0 R3.0).The recommended measurement point for the voltage is the CPCI connector on the CPU board.

The following table provides information regarding the required characteristics for each board input voltage.

Table 6-3: Input Voltage Characteristics

VOLTAGE	NOMINAL VALUE	TOLERANCE	MAX. RIPPLE (p-p)	REMARKS
5 V	+5.0 VDC	+5%/-3%	50 mV	Main voltage
3.3 V	+3.3 VDC	+5%/-3%	50 mV	--
+12 V	+12 VDC	+5%/-5%	240 mV	Required
-12 V	-12 VDC	+5%/-5%	240 mV	Only for PMC
V I/O (PCI) voltage	+3.3 VDC or +5 VDC	+5%/-3%	50 mV	Standard Version +5.0V
GND	Ground, not directly connected to potential earth (PE)			

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

6.1.3.4 Regulation

The power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

Note ...

Non-industrial ATX PSUs require a greater minimum load than a single CP620 is capable of creating. When a PSU of this type is used, it will not power up correctly and the CP620 may hang up. The solution is to use an industrial PSU or to add more load to the system.

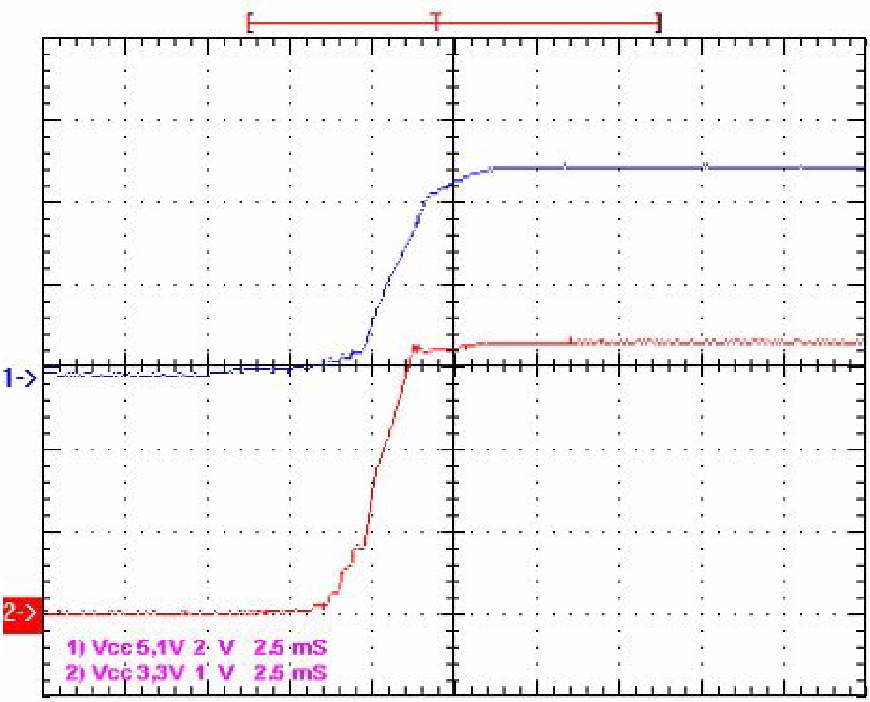
Note ...

If the main power input is switched off, the 3.3V supply voltage will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it went below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

6.1.3.5 Rise Time Diagram

The following figure illustrates an example of the recommended start-up ramp of a CPCI power supply for all Kontron boards delivered up to now.

Figure 6-1: Start-Up Ramp of the CP3-SVE180 AC Power Supply



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6.2 Power Consumption

The goal of this description is to provide a method to calculate the power consumption for the CP620 baseboard and for additional configurations. The processor dissipates the majority of the thermal power.

The power consumption table lists the voltage and current specifications for the CP620 board and the CP620 accessories. The values were measured with an 8-slot passive CompactPCI backplane. During measurement the power consumption of the backplane was ignored. Measurements were taken using the NetBootLoader (no OS) and under the operating system VxWorks. All measurements were conducted at a temperature of 25°C. The measured values varied, because power consumption was dependent on processor activity. All PPC750CXe processors are powered with 1.8V core voltage.

Table 6-4: Power Consumption Table with NetBootLoader

POWER	IBM® PowerPC® 750CX 400 MHz / 128 MB	IBM® PowerPC® 750 CXe 600 MHz / 512 MB
5 V	3.0W	3.9W
3.3 V	5.08W	5.48W
Total	8.08W	9.38W

Table 6-5: Power Consumption Table with VxWorks Running

POWER	IBM® PowerPC® 750CX 400 MHz / 256 MB	IBM® PowerPC® 750 CXe 600 MHz / 512 MB
5 V	5.5W	5.7W
3.3 V	3.63W	3.7W
Total	9.13W	9.4W

6.2.1 Power Requirement for the CP620

The following table indicates the start-up current of the CP620 during the first 2-3 seconds after the power supply has been switched on. The power consumption of the CP620 during operation is indicated in tables 6-4 and 6-5.

Table 6-6: Start-Up Current of the CP620

POWER		IBM® PowerPC® 750CX 400 MHz / 128 MB	IBM® PowerPC® 750 CXe 600 MHz / 512 MB
5 V	peak	8.5 A	4.0 A
	average	1.0 A	1.2 A
3.3 V	peak	9.0 A	6.0 A
	average	2.5 A	2.8 A
12 V	average	0.1 A	0.1 A

For further information on the start-up current, contact Kontron Modular Computers' Technical Support.

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Chapter 7

System Considerations

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7. System Considerations

The following chapters provide system integrators with the necessary information to satisfy thermal requirements when implementing CP620 applications.

7.1 Temperature Range and Air Flow

The CP620 has been designed to operate at an extended temperature range from -40°C up to + 85°C. All onboard components are specially selected for the higher temperature range. The processors used here are produced with the new 0.18-micron copper process which have lower power consumption and support high die temperatures (105°C).

These values have been measured with typical applications under Linux and VxWorks. In worst case situations the values and the temperature range must be reduced accordingly. For all situations the maximum case temperature of the PowerPC® 750CXe processor must not exceed 105°C. This temperature value can be measured using the on-chip thermal management unit of the PowerPC® 750CXe processor. In instances of overtemperature, the thermal management unit will reduce the processor clock speed in order to reduce power generation.

Table 1-1: Typical Temperature Range and Required Air Flow

HEAT SINK VERSION	RANGE	400 MHz	600 MHz
4HP	0°C to +70°C	natural convection	natural convection
	-25°C to +75°C	natural convection	natural convection
	-40°C to +85°C	TBD	TBD

When developing applications using the CP620, the system integrator must be aware of the overall system thermal requirements. System chassis must be provided which satisfy these requirements.

0.2 m/s air flow means standard convection cooling with the board in an upright position. An airflow of 1 m/s to 1.5 m/s is a typical value for a standard Kontron ASM 4 rack (6U CompactPCI rack with 1U cooling fans). For other racks or housings the available airflow will be different. The maximum ambient temperature must be recalculated and/or measured for such environments. For the calculation of the maximum ambient temperature the processor temperature must never exceed 105°C.

The CP620 is fitted with an optimally designed heat sink. The physical size, shape, and construction ensures the best possible thermal resistance (R_{th}) coefficients. To ensure that the heat sink temperature does not exceed its limits, an airflow may be needed for a given ambient temperature.

Warning!

It is the responsibility of the end user to ensure that the processor die temperature never exceeds 105°C in order to protect the board against overheating. Permanent overheating can damage the board.

If the temperature on the processor die is greater than 105°C, the maximum ambient temperature must be reduced or an external airflow must be provided by means of an additional fan.

7.1.1 Peripherals

When determining the thermal requirements for a given application, peripherals to be used with the CP620 must also be considered. Devices such as hard disks, PMC modules, etc. which are directly attached to the CP620 must also be capable of being operated at the temperatures foreseen for the application. It may very well be necessary to revise system requirements to comply with operational environment conditions. In most cases, this will lead to a reduction in the maximum allowable ambient operating temperature or even require active cooling of the operating environment.

Warning!

As Kontron assumes no responsibility for any damage to the CP620 or other equipment resulting from overheating of the CPU, it is highly recommended that system integrators as well as end users confirm that the operational environment of the CP620 complies with the thermal considerations set forth in this document.

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Appendix **A**

PMC-HDD1 Module (Optional)

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A. PMC-HDD1 Module (Optional)

A.1 Board Description

The PMC-HDD1 provides the Kontron PowerPC-based CPU boards with a cost-effective way to add substantial mass storage capacity. It is designed to connect a 2.5” IDE hard disk drive to the PCI bus of those boards. It is based on the silicon image IDE controller SiI0680, which provides the interface between the 32 bit wide, 33 MHz PCI bus and a standard IDE hard disk drive. It is able to handle transfer rates up to the ATA-133 speed standard.

Note ...

- The maximum transfer rate which can be achieved with this module is restricted by the hard drive in use.
- The capacity of the module is defined by the hard drive in use.

Figure A-1: PMC-HDD1 Module with Hard Disk Drive Attached

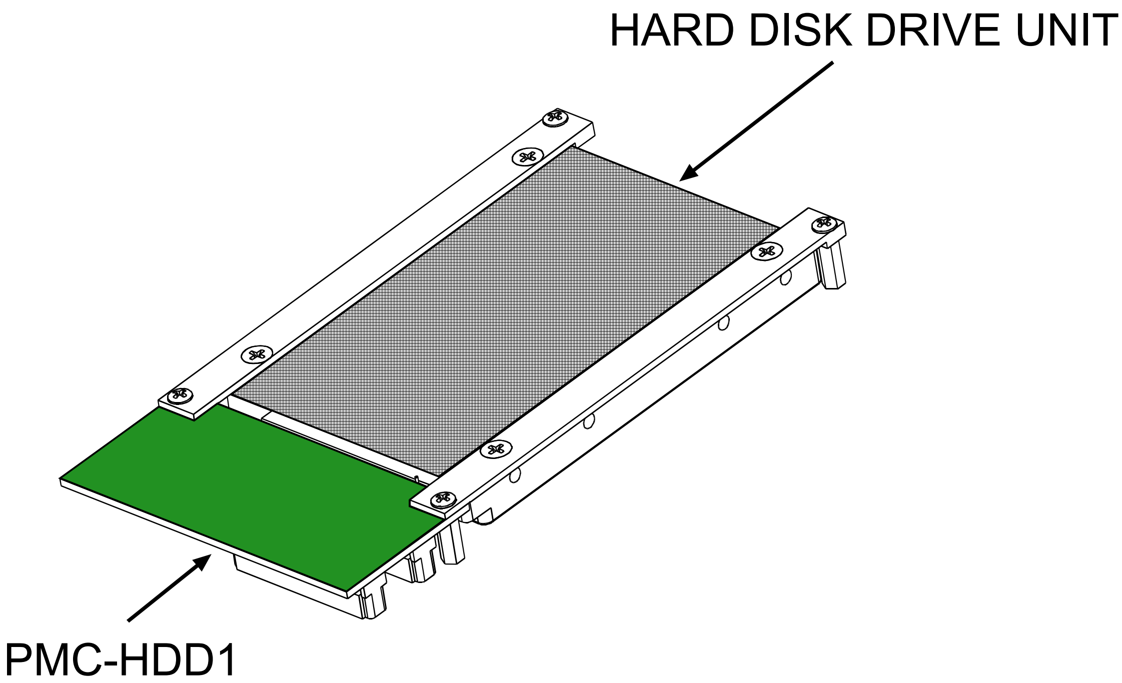

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Table A-1: Pinout of the PMC Connectors

Pn1 / Jn1 (CON1)				Pn2 / Jn2 (CON2)			
SIGNAL	PIN	PIN	SIGNAL	SIGNAL	PIN	PIN	SIGNAL
TCK	1	2	-12V	+12V	1	2	TRST#
Ground	3	4	INTA#	TMS	3	4	TDO
INTB#	5	6	INTC#	TDI	5	6	Ground
BUSMODE1#	7	8	+5V	Ground	7	8	PCI-RSVD
INTD#	9	10	PCI-RSVD	PCI-RSVD	9	10	PCI-RSVD
Ground	11	12	PCI-RSVD	BUSMODE2#	11	12	+3.3V
CLK	13	14	Ground	RST#	13	14	BUSMODE3#
Ground	15	16	GNT#	+3.3V	15	16	BUSMODE4#
REQ#	17	18	+5V	PCI-RSVD	17	18	Ground
V (I/O)	19	20	AD[31]	AD[30]	19	20	AD[29]
AD[28]	21	22	AD[27]	Ground	21	22	AD[26]
AD[25]	23	24	Ground	AD[24]	23	24	+3.3V
Ground	25	26	C/BE[3]#	IDSEL	25	26	AD[23]
AD[22]	27	28	AD[21]	+3.3V	27	28	AD[20]
AD[19]	29	30	+5V	AD[18]	29	30	Ground
V (I/O)	31	32	AD[17]	AD[16]	31	32	C/BE[2]#
FRAME#	33	34	Ground	Ground	33	34	PMC-RSVD
Ground	35	36	IRDY#	TRDY#	35	36	+3.3V
DEVSEL#	37	38	+5V	Ground	37	38	STOP#
Ground	39	40	LOCK#	PERR#	39	40	Ground
SDONE#	41	42	SBO#	+3.3V	41	42	SERR#
PAR	43	44	Ground	C/BE[1]#	43	44	Ground
V (I/O)	45	46	AD[15]	AD[14]	45	46	AD[13]
AD[12]	47	48	AD[11]	Ground	47	48	AD[10]
AD[09]	49	50	+5V	AD[08]	49	50	+3.3V
Ground	51	52	C/BE[0]#	AD[07]	51	52	PMC-RSVD
AD[06]	53	54	AD[05]	+3.3V	53	54	PMC-RSVD
AD[04]	55	56	Ground	PMC-RSVD	55	56	Ground
V (I/O)	57	58	AD[03]	PMC-RSVD	57	58	PMC-RSVD
AD[02]	59	60	AD[01]	Ground	59	60	PMC-RSVD
AD[00]	61	62	+5V	ACK64#	61	62	+3.3V
Ground	63	64	REQ64#	Ground	63	64	PMC-RSVD

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Table A-2: IDE Hard Disk Drive Connector Pinout

I/O	FUNCTION	SIGNAL	PIN	PIN	SIGNAL	FUNCTION	I/O
O	Reset HD	IDERESET	1	2	GND	Ground signal	--
I/O	HD data 7	HD7	3	4	HD8	HD data 8	I/O
I/O	HD data 6	HD6	5	6	HD9	HD data 9	I/O
I/O	HD data 5	HD5	7	8	HD10	HD data 10	I/O
I/O	HD data 4	HD4	9	10	HD11	HD data 11	I/O
I/O	HD data 3	HD3	11	12	HD12	HD data 12	I/O
I/O	HD data 2	HD2	13	14	HD13	HD data 13	I/O
I/O	HD data 1	HD1	15	16	HD14	HD data 14	I/O
I/O	HD data 0	HD0	17	18	HD15	HD data 15	I/O
--	Ground signal	GND	19	20	N/C	--	--
I	DMA request	IDEDRQ	21	22	GND	Ground signal	--
O	I/O write	IOW	23	24	GND	Ground signal	--
O	I/O read	IOR	25	26	GND	Ground signal	--
I	I/O channel ready	IOCHRDY	27	28	GND	Ground signal	--
O	DMA Ack	IDEDACKA	29	30	GND	Ground signal	--
I	Interrupt request	IDEIRQ	31	32	N/C	--	--
O	Address 1	A1	33	34	N/C	--	--
O	Address 0	A0	35	36	A2	Address 2	O
O	HD select 0	HCS0	37	38	HCS1	HD select 1	O
I	--	NC	39	40	GND	Ground signal	--
--	5V power	VCC	41	42	VCC	5V power	--
--	Ground signal	GND	43	44	N/C	--	--

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