Errata 2

Manual: 20817

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1. Reference: Page 4-5, Chapter 4.2.1, Figure 4-1

The referenced information (figure) is superseded by the following replacement figure.

Figure 4-1: IUC-32(E) Memory Map

Address	Memory Device	MC68(EN)360
0x 00 xx xx xx	DRAM on DRAM/Flash piggyback	CS1
0x 04 xx xx xx	FLASH on DRAM/Flash piggyback	CS0
0x 07 00 0x xx	MC68(EN)360 internal RAM register	—
0x 09 xx xx xx	Flash/EPROM sockets[1]	CS3
0x 0A xx xx xx	SRAM	CS4
0x 0B F7 xx xx	CXC[2]	CS5
0x 0C xx xx xx	Real-time clock	CS6
0x 0D xx xx x7	Board control / status register	CS7+7
0x 1x xx xx xx	eCXC[2]	CS5

1 If the ROM sockets are selected as the default boot device, then the address 0x 09 xx xx xx, i.e. CS3 of the MC68[EN[360, is automatically selected as the base address for the flash on the memory piggyback.

2 See the “CXC” appendix of this manual for further addressing information.

2. Reference: Page B-8, Chapter B.5.1, Table B-7

The referenced information (table) is revised as follows.

The table row:

1	DSR

is changed to read:

1	N/C

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