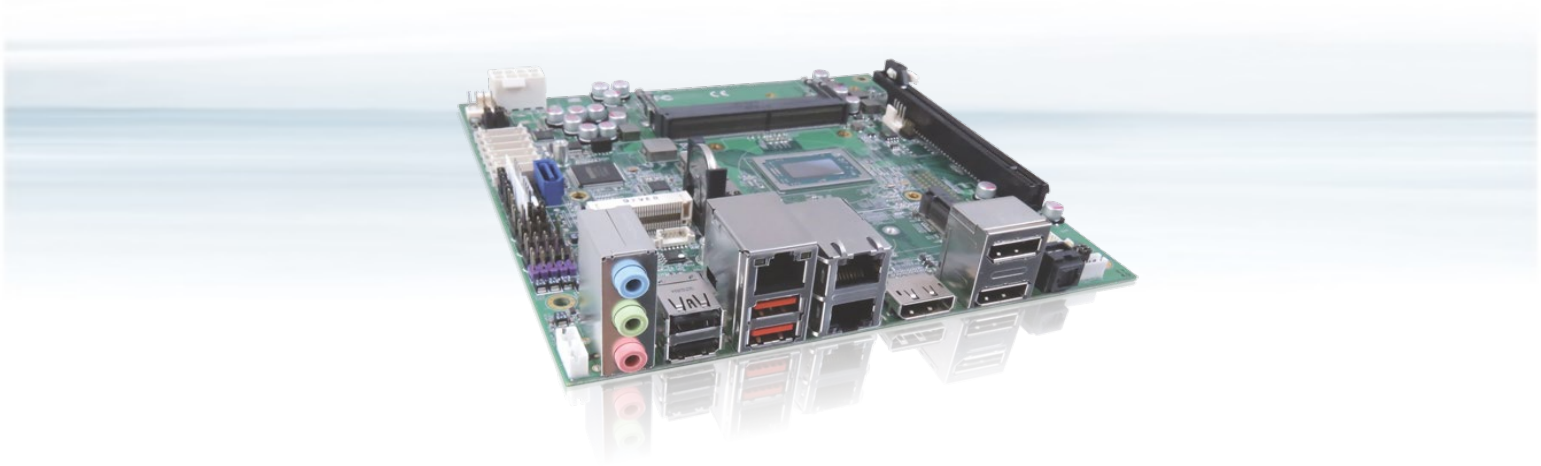
USER GUIDE



mITX-VR1000 V2.0

Doc. User Guide, Rev. 1.2

Doc. ID: [To be Determined]

POSSIBILITIES START HERE kontron S&T Group

www.kontron.com

This page has been intentionally left blank

MITX-VR1000 V2.0 - USER GUIDE

Disclaimer

Kontron would like to point out that the information contained in this user guide may be subject to alteration, particularly as a result of the constant upgrading of Kontron products. This document does not entail any guarantee on the part of Kontron with respect to technical processes described in the user guide or any product characteristics set out in the user guide. Kontron assumes no responsibility or liability for the use of the described product(s), conveys no license or title under any patent, copyright or mask work rights to these products and makes no representations or warranties that these products are free from patent, copyright or mask work right infringement unless otherwise specified. Applications that are described in this user guide are for illustration purposes only. Kontron makes no representation or warranty that such application will be suitable for the specified use without further testing or modification. Kontron expressly informs the user that this user guide only contains a general description of processes and instructions which may not be applicable in every individual case. In cases of doubt, please contact Kontron.

Kontron S&T AG

Lise-Meitner-Str. 3-5
86156 Augsburg
Germany
www.kontron.com

Intended Use

THIS DEVICE AND ASSOCIATED SOFTWARE ARE NOT DESIGNED, MANUFACTURED OR INTENDED FOR USE OR RESALE FOR THE OPERATION OF NUCLEAR FACILITIES, THE NAVIGATION, CONTROL OR COMMUNICATION SYSTEMS FOR AIRCRAFT OR OTHER TRANSPORTATION, AIR TRAFFIC CONTROL, LIFE SUPPORT OR LIFE SUSTAINING APPLICATIONS, WEAPONS SYSTEMS, OR ANY OTHER APPLICATION IN A HAZARDOUS ENVIRONMENT, OR REQUIRING FAIL-SAFE PERFORMANCE, OR IN WHICH THE FAILURE OF PRODUCTS COULD LEAD DIRECTLY TO DEATH, PERSONAL INJURY, OR SEVERE PHYSICAL OR ENVIRONMENTAL DAMAGE (COLLECTIVELY, "HIGH RISK APPLICATIONS").

You understand and agree that your use of Kontron devices as a component in High Risk Applications is entirely at your risk. To minimize the risks associated with your products and applications, you should provide adequate design and operating safeguards. You are solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning your products. You are responsible to ensure that your systems (and any Kontron hardware or software components incorporated in your systems) meet all applicable requirements. Unless otherwise stated in the product documentation, the Kontron device is not provided with error-tolerance capabilities and cannot therefore be deemed as being engineered, manufactured or setup to be compliant for implementation or for resale as device in High Risk Applications. All application and safety related information in this document (including application descriptions, suggested safety measures, suggested Kontron products, and other materials) is provided for reference only.

Revision History

Revision	Brief Description of Changes	Date of Issue	Author/ Editor
1.0	Initial Issue	2019-Sep-24	YS
1.1	Add a LPS power supply notice in Sec. 2.1	2020-Apr-10	YS
1.2	Remove UL certification	2021-May-25	YS

Terms and Conditions

Kontron warrants products in accordance with defined regional warranty periods. For more information about warranty compliance and conformity, and the warranty period in your region, visit http://www.kontron.com/terms-and-conditions.

Kontron sells products worldwide and declares regional General Terms & Conditions of Sale, and Purchase Order Terms & Conditions. Visit http://www.kontron.com/terms-and-conditions.

For contact information, refer to the corporate offices contact information on the last page of this user guide or visit our website CONTACT US.

Customer Support

Find Kontron contacts by visiting: http://www.kontron.com/support.

Customer Service

As a trusted technology innovator and global solutions provider, Kontron extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly-experienced support enables Kontron to provide exceptional peace of mind to build and maintain successful products.

For more details on Kontron's service offerings such as: enhanced repair services, extended warranty, Kontron training academy, and more visit http://www.kontron.com/support-and-services/services.

Customer Comments

If you have any difficulties using this user guide, discover an error, or just want to provide some feedback, contact Kontron support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user guide on our website.

Symbols

The following symbols may be used in this user guide

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
NOTICE	NOTICE indicates a property damage message.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
	Electric Shock! This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	ESD Sensitive Device! This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	HOT Surface! Do NOT touch! Allow to cool before servicing.
	Laser! This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!

Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

⚠CAUTION

Danger of explosion if the battery is replaced incorrectly.

- Replace only with same or equivalent battery type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer's instructions.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Quality and Environmental Management

Kontron aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding Kontron's quality and environmental responsibilities, visit http://www.kontron.com/about-kontron/corporate-responsibility/quality-management.

Disposal and Recycling

Kontron's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Environmental protection is a high priority with Kontron.

Kontron follows the WEEE directive

You are encouraged to return our products for proper disposal.

Table of Contents

List of Tables

List of Figures

1/ Introduction

This user guide describe the mITX-VR1000 V2.0 board made by Kontron. This board will also be denoted mITX-VR1000 V2.0 within this user guide.

Use of this user guide implies a basic knowledge of PC-AT hardware and software. This user guide focuses on describing the mITX-VR1000 V2.0 board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in the following chapter before switching on the power.

All configuration and setup of the CPU board is either carried out automatically or manually by the user via the BIOS setup menus.

Latest revision of this user guide, datasheet, thermal simulations, BIOS, drivers, BSP's (Board Support Packages), mechanical drawings (2D and 3D) can de download from Kontron's Web Page.

2/ Installation Procedures

2.1. Installing the Board

NOTICE

ESD Sensitive Device

Electrostatic discharge (ESD) can damage equipment and impair electrical circuitry.

- Wear ESD-protective clothing and shoes
- Wear an ESD-preventive wrist strap attached to a good earth ground
- Check the resistance value of the wrist strap periodically (1 MΩ to 10 MΩ)
- Transport and store the board in its antistatic bag
- Handle the board at an approved ESD workstation
- Handle the board only by the edges

To get the board running follow these steps. If the board shipped from Kontron already has components like RAM and CPU cooler mounted, then skip the relevant steps below.

1. **Turn off the PSU (Power Supply Unit)**

NOTICE

Turn off PSU (Power Supply Unit) completely (no mains power connected to the PSU) or leave the Power Connectors unconnected while configuring the board. Otherwise, components (RAM, LAN cards etc.) might get damaged. Make sure to use a standard ATX12V PSU with suitable cable kits and PS-ON# active.

NOTICE

The power supply unit shall comply with the requirements as defined in IEC 62368-1 according Clause 6.2.2 to power source category PS2 "Limited Power Source".

2. **Insert the DDR4 SO-DIMM 260-pin module(s)**
   Be careful to push the memory module in the slot(s) before locking the tabs. For a list of approved SO-DIMMs contact your Distributor or FAE. See also chapter "System Memory Support". Use SO-DIMM with the same memory density in both sockets!
3. **Cooler installation**
   You can connect the cooler fan electrically to the CPU FAN connector.
4. **Connecting interfaces**
   Insert all external cables for hard disk, keyboard etc. A monitor must be connected in order to change BIOS settings.
5. **Connect and turn on PSU**
   Connect PSU to the board by the 2x4-pin ATX wafer connector.
6. **BIOS setup**
   Enter the BIOS setup by pressing the <DEL> key during boot up.

   Enter "Exit Menu" and Load Setup Defaults.

   Refer to the "BIOS Configuration / Setup" section of this manual for details on BIOS setup.

To clear all BIOS setting, including Password protection, activate "Clear CMOS Jumper" for 10 sec (without power connected).

7. Mounting the board in chassis

NOTICE

When mounting the board to chassis etc. please note that the board contains components on both sides of the PCB that can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.

When fixing the board on a chassis, it is recommended to use screws with an integrated washer and a diameter of > 7 mm. Do not use washers with teeth, as they can damage the PCB and cause short circuits.

2.2. Chassis Safety Standards

Before installing the mITX-VR1000 V2.0 in the chassis, users must evaluate the end product to ensure compliance with the requirements of the IEC60950-1 safety standard:

- The board must be installed in a suitable mechanical, electrical and fire enclosure.
- The system, in its enclosure, must be evaluated for temperature and airflow considerations.
- The board must be powered by a CSA or UL approved power supply that limits the maximum input current.
- For interfaces having a power pin such as external power or fan, ensure that the connectors and wires are suitably rated. All connections from and to the product shall be with SELV circuits only.
- Wires have suitable rating to withstand the maximum available power.
- The peripheral device enclosure fulfils the IEC60950-1 fire protecting requirements.

2.3. Lithium Battery Replacement

If replacing the lithium battery follow the replacement precautions stated in the notification below:

⚠CAUTION

Danger of explosion if the lithium battery is incorrectly replaced.

- Replace only with the same or equivalent type recommended by the manufacturer
- Dispose of used batteries according to the manufacturer's instructions

VORSICHT! Explosionsgefahr bei unsachgemäßem Austausch der Batterie.

- Ersatz nur durch denselben oder einen vom Hersteller empfohlenen gleichwertigen Typ
- Entsorgung gebrauchter Batterien nach Angaben des Herstellers

ATTENTION! Risque d'explosion avec l'échange inadéquat de la batterie.

- Remplacement seulement par le même ou un type équivalent recommandé par le producteur
- L'évacuation des batteries usagées conformément à des indications du fabricant

PRECAUCION! Peligro de explosión si la batería se sustituye incorrectamente.

- Sustituya solamente por el mismo o tipo equivalente recomendado por el fabricante

- Disponga las baterías usadas según las instrucciones del fabricante

ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering.

- Udskiftning må kun ske med batteri af samme fabrikat og type
- Levér det brugte batteri tilbage til leverandøren

ADVARSEL! Eksplosjonsfare ved feilaktig skifte av batteri.

- Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten
- Brukte batterier kasseres i henhold til fabrikantens instruksjoner

VARNING! Explosionsfara vid felaktigt batteribyte.

- Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren
- Kassera använt batteri enligt fabrikantens instruktion

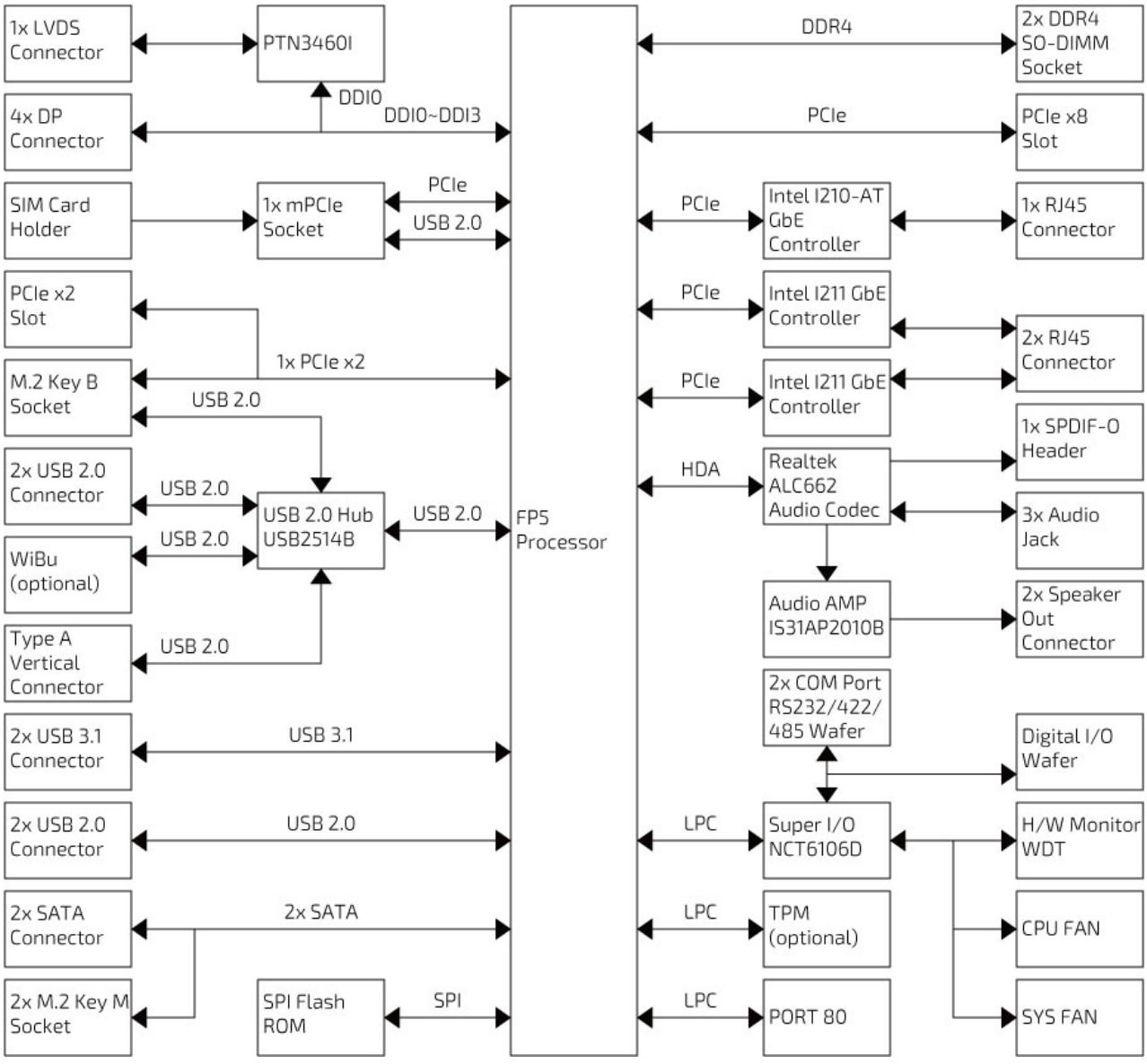
VAROITUS! Paristo voi räjähtää, jos se on virheellisesti asennettu.

- Vaihda paristo ainoastaan lalteval- mistajan suosittelemaan tyyppiln
- Hävitä käytetty paristo valmistajan ohjeiden mukaisesti

3/ System Specifications

3.1. System Block Diagram

Figure 1: System Block Diagram mITX-VR1000 V2.0



3.2. Scope of Delivery

The table below summarizes the features of the mITX-VR1000 V2.0 motherboard.

Table 1: Component Main Data

System	
Processor	AMD Embedded V-Series V1000 APU (TDP up to 54 W)
Memory	2x DDR4 SO-DIMM memory socket
Video	
Display Interface	Configuration 1: 1x LVDS + 1x DP++ (on rear) + 2x DP (on rear) Configuration2: 2x DP++ (on rear) + 2x DP (on rear)
Multiple Display	Quadruple
Audio	
Audio Codec	Realtek ALC662
Audio Interface	2x Speaker-out (3 W) 1x Line-in (on rear) 2x Line-out (1x on rear, 1x by header) 2x Mic-in (1x on rear, 1x by header) 2x S/PDIF (1x on rear, 1x by header)
Network Connection	
Ethernet	3x GbE LAN (RJ45 on rear, 2x Intel® I211-AT, 1x Intel® I210-AT)
Peripheral Connection	
USB	2x USB 3.1 (Type A on rear) 5x USB 2.0 (2x Type A on rear, 3x by header)
Serial Port	2x RS232/422/485 (by header) 4x RS232 (by header)
Other I/Os	8-bit DIO (by header)
Storage & Expansion	
Storage & Expansion	1x SATA 3.0 1x mPCIe (full size, mixed w/ PCIe x1, USB 2.0) 1x M.2 Key B (type 2242/ 2280, mixed w/ USB 2.0/PCIe x2, NVMe support) 1x M.2 Key M (type 2280) 1x PCIe x16 (x8 signal) 2x SIM Cage (1x Micro type connected to M.2 Key B, 1x by wafer connected to mPCIe)
Power	
Input Voltage	DC 12 V
Connector	2x4-pin ATX Connector
Firmware	
BIOS	AMI uEFI BIOS w/ SPI Flash
Watchdog	Programmable WDT to generate system reset event
H/W Monitor	Voltages

System	
	▶ Temperatures
Real Time Clock	▶ SoC integrated RTC
TPM	▶ Supported (Infineon SLB 9665 TPM 2.0)
WiBU	▶ Optional
System Control & Monitoring	
Front Panel Header	▶ 1x Header for Reset button, HDD LED & External Speaker ▶ 1x Header for Power button, Power LED & SM bus ▶ 1x Header for mPCIe activity LED ▶ 1x Header for M.2 Key B activity LED
Cooling	
Cooling Method	▶ 1x Wafer for CPU Smart Fan ▶ 1x Wafer for System Smart Fan
Software	
OS Support	▶ Windows 10
Mechanical	
Dimension (L x W)	▶ Mini-ITX (170 mm x 170 mm / 6.70" x 6.70")

3.3. Environmental Conditions

The mITX-VR1000 V2.0 is compliant with the following environmental conditions. It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within the allowed temperature range.

Table 2: Environmental Conditions

Operating Temperature	▶ 0 °C ~ 60 °C / 32 °F ~ 140 °F
Storage Temperature	▶ -20 °C ~ 80 °C / -4 °F ~ 176 °F
Humidity	▶ 0 % ~ 95 %

3.4. Standards and Certifications

The mITX-VR1000 V2.0 meets the following standards and certification tests.

Table 3: Standards and Certifications

CE Class B	▶ TBD
FCC Class B	▶ TBD
RoHS	▶ TBD
REACH	▶ TBD

3.5. Processor Support

The mITX-VR1000 V2.0 is designed to support AMD Ryzen™ Embedded V1000 Processors. The BGA APU is remounted from factory. Kontron has defined the board versions as listed in the following table, so far all based on Embedded APUs. Other versions are expected at a later date.

Table 4: Processor Support

Name	Core #	Speed	Turbo	Embedded	Cache	Socket	TDP	Tj
Ryzen™ V1807B	4	3.35 GHz	3.80 GHz	Yes	4M	FP5	45 W	105 °C
Ryzen™ V1756B	4	3.25 GHz	3.60 GHz	Yes	4M	FP5	45 W	105 °C
Ryzen™ V1605B	4	2.00 GHz	3.60 GHz	Yes	4M	FP5	15 W	105 °C
Ryzen™ V1202B	2	2.30 GHz	3.20 GHz	Yes	4M	FP5	15 W	105 °C

Sufficient cooling must be applied to the APU in order to remove the effect defined as TDP (Thermal Design Power). The sufficient cooling is also depending on the worst case maximum ambient operating temperature and the actual worst case load of processor.

3.6. System Memory Support

The mITX-VR1000 V2.0 has two DDR4 SO-DIMM sockets. The sockets support the following memory features:

- 2x DDR4 SO-DIMM, 1.2 V
- Up to 32 GB (2x 16 GB)
- Dual channel, 260-pin, 3200 MT/s (V1807B and V1756B) or 2400 MT/s (V1605B and V1202B)
- SPD timing supported
- ECC supported

The installed DDR4 SO-DIMM should support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read and configure the memory controller for optimal performance. If non-SPD memory is used, the BIOS will attempt to configure the memory settings, but performance and reliability may be impacted, or the board may not be able to boot totally.

3.6.1. Memory Operating Frequencies

In all modes, the frequency of system memory is the lowest frequency of all the memory modules placed in the system. Each memory module's frequency can be determined through the SPD registers on the memory modules.

The table below lists the resulting operating memory frequencies based on the combination of SO-DIMMs and processor.

Table 5: Memory Operating Frequencies

SO-DIMM Type	Module Name	Memory Data Transfer (MT/s)	Processor System Bus Frequency (MHz)	Resulting Memory Clock Frequency (MHz)	Peak Transfer Rate (MB/s)
DDR4 3200	PC4-25600	3200	1600	400	25600
DDR4 2400	PC4-19200	2400	1200	300	19200

Memory modules have in general a much lower longevity than embedded motherboards, and therefore EOL of modules can be expected several times during lifetime of the motherboard.

As a minimum it is recommend using Kontron memory modules for prototype system(s) in order to prove stability of the system and as for reference.

For volume production you might request to test and qualify other types of RAM. In order to qualify RAM it is recommend configuring 3 systems running RAM Stress Test program in heat chamber at 60° C for a minimum of 24 hours.

3.7. On-board Graphics Subsystem

The mITX-VR1000 V2.0 supports AMD Radeon™ Vega technology for high quality graphics capabilities. All mITX-VR1000 V2.0 versions support four displays pipes.

Up to four displays can be used simultaneously and be used to implement independent or cloned display configuration.

Table 6: Four-displays Configurations

Display 1	Display 2	Display 3	Display 4	Max. Resolution (Px) at 60 Hz			
				Display 1	Display 2	Display 3	Display 4
LVDS	DP++	DP	DP	1920 x 1200	4096 x 2160	4096 x 2160	4096 x 2160
DP++	DP++	DP	DP	4096 x 2160	4096 x 2160	4096 x 2160	4096 x 2160

3.8. Power Supply Voltage

In order to ensure safe operation of the board, the input power supply must monitor the supply voltage and shut down if the supply is out of range – refer to the actual power supply specification. Please note, in order to keep the power consumption to a minimal level, boards do not implement a guaranteed minimum load. In some cases, this can lead to compatibility problems with ATX power supplies that require a minimum load to stay in regulation. The mITX-VR1000 V2.0 board must be powered through the ATX+12V-8p (8-pole) connector using standard ATX12V power supply.

ATX12V supply: ATX+12V-8p connector must be used in according to the ATX12V PSU standard.

NOTICE

Hot Plugging power supply is not supported. Hot plugging might damage the board.

The requirements to the voltages of ATX power supply are as follows:

Table 7: Supply Voltages

Supply	Min.	Max.	Note
+12 V	11.4 V	12.6 V	Should be ±5% for compliance with the ATX specification

4/ Connector Locations

4.1. Top Side

Figure 2: Top Side

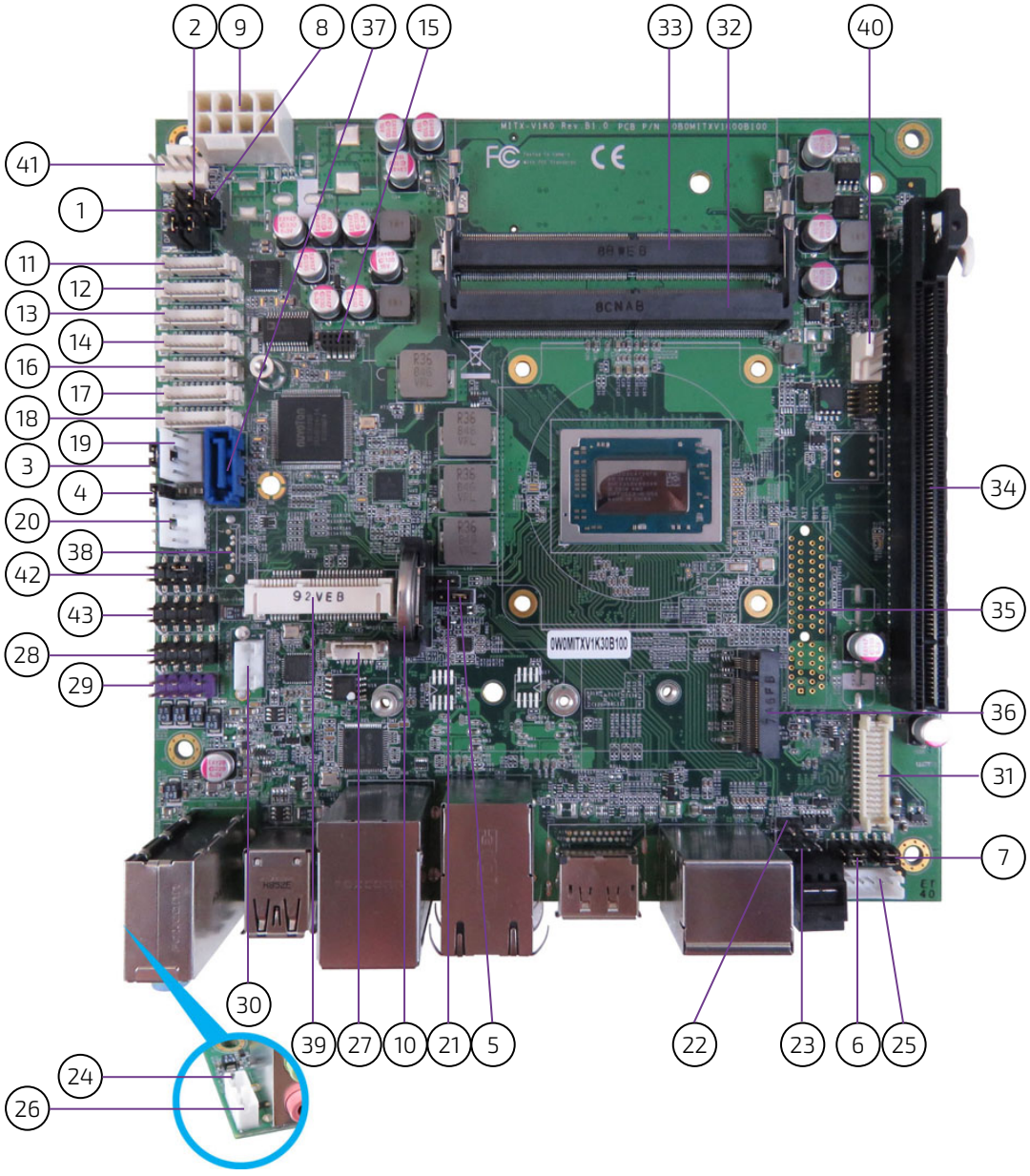


Table 8: Jumper List

Item	Designation	Description	See Chapter
1	JP1	Pin-9 Selection for COM1	7.20.1
2	JP2	Pin-9 Selection for COM2	7.20.1
3	JP3	AT / ATX Power Mode Selection	7.20.2
4	JP4	USB Power Selection	7.20.3

Item	Designation	Description	See Chapter
5	JP6	Clear CMOS Selection	7.20.4
6	JP7	Backlight Power Enable Selection for LVDS1	7.20.5
7	JP8	Panel & Backlight Power Selection for LVDS1	7.20.6
8	JP9	LVDE_EDID Selection	7.20.7

Table 9: Top Side Internal Connector Pin Assignment

Item	Designation	Description	See Chapter
9	ATX1	DC 12 V (BOM option for 24 V support) Power Input Wafer	7.1.1
10	BAT2	CR2032 Battery Holder	7.1.2
11	CN2	Digital Input / Output Wafer	7.13
12	CN3	RS232/422/485 Port 1 Wafer	7.10
13	CN4	RS232/422/485 Port 2 Wafer	7.10
14	CN5	RS232 Port 3 Wafer	7.10
15	CN6	P80 Header	
16	CN7	RS232 Port 4 Wafer	7.10
17	CN8	RS232 Port 5 Wafer	7.10
18	CN10	RS232 Port 6 Wafer	7.10
19	CN11	HDD Power Output Wafer 1	7.4
20	CN12	HDD Power Output Wafer 2	7.4
21	CN13	mPCIe Activity LED Pin Header	7.19
22	CN14	M.2 Key B LED Pin Header	7.19
23	CN15	S/PDIF Output Pin Header	7.9
24	CN19	Right Channel 3W Audio AMP Output Wafer	7.6
25	CN23	Panel Backlight Wafer for LVDS1	7.12
26	CN25	Left Channel 3W Audio AMP Output Wafer	7.6
27	CN26	SIM Interface Wafer for MPCIE1	7.16
28	CN27	USB 2.0 Port DN_1, DN_2 Pin Header	7.5
29	CN28	Front Panel Audio Pin Header	7.7
30	CN29	USB 2.0 Port 5 Wafer	7.5
	USB1	USB 2.0 Port 3 Type A 90 degrees Connector	
31	LVDS1	Primary 24-bit, 2-channel LVDS Panel Connector (BOM option)	7.11
32	DIMM1	DDR4 Memory SO-DIMM Socket	3.6
33	DIMM2	DDR4 Memory SO-DIMM Socket	3.6
34	PCIE2	PCIe x16 Slot (signal for PCIe x8 only)	7.17
35	PCIE1	PCIe x4 Slot (signal for PCIe x2 only) (BOM option)	7.18
36	M2B1	M.2 Key B Socket (BOM option)	7.15
37	SATA1	Serial ATA Port-0 Connector (for M2M1) (BOM option)	7.3
38	SATA2	Serial ATA Port-1 Connector (for M2M2) (BOM option)	7.3
39	MPCIE1	Mini-PCI Express v1.2 Socket	7.14
40	FAN1	CPU FAN Wafer	7.2
41	FAN2	System FAN Wafer	7.2
42	FP1	Front Panel 1 Pin Header	7.8

Item	Designation	Description	See Chapter
43	FP2	Front Panel 2 Pin Header	7.8

4.2. Bottom Side

Figure 3: Bottom Side

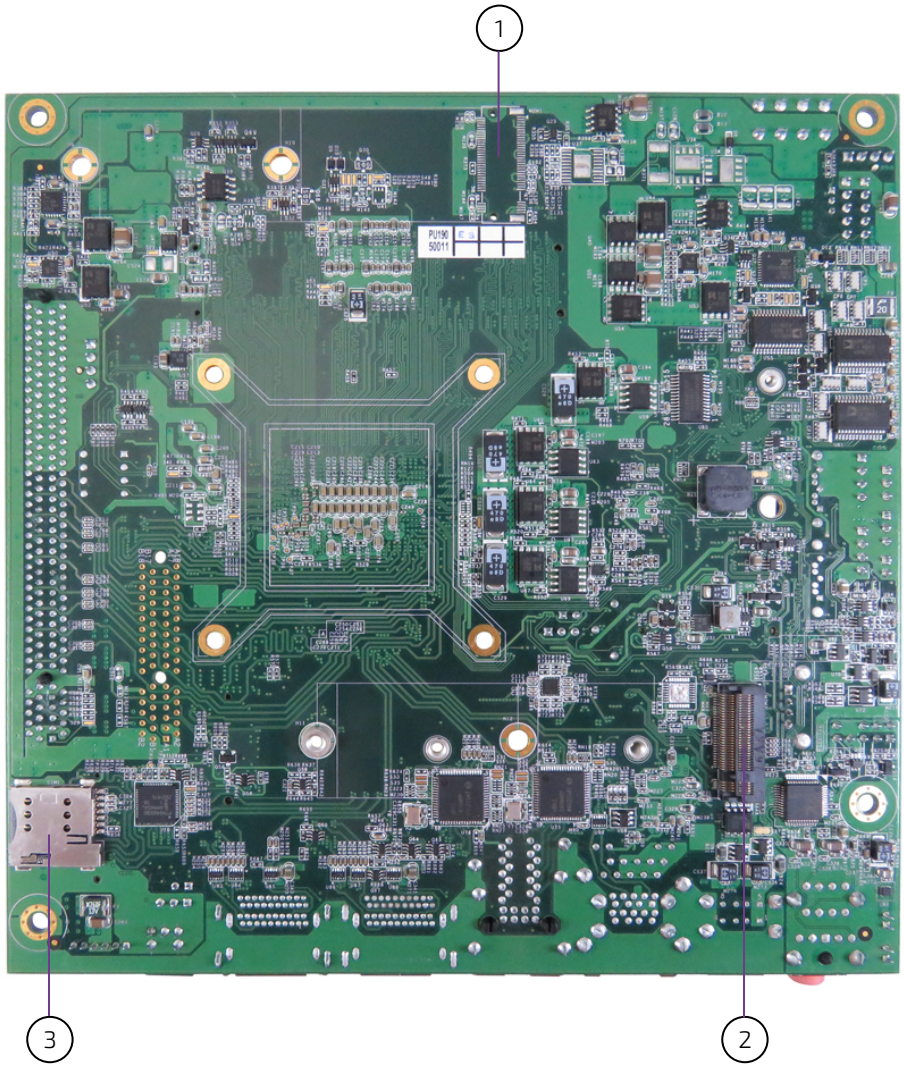


Table 10: Bottom Side Internal Connector Pin Assignment

Item	Designation	Description	See Chapter
1	M2M1	M.2 Key M Socket (for SATA1) (BOM option)	7.15
2	M2M2	M.2 Key M Socket (for SATA2) (BOM option)	7.15
3	SIM1	SIM Card Connector, Push-Push Type	7.16

4.3. Connector Panel Side

Figure 4: Connector Panel Side

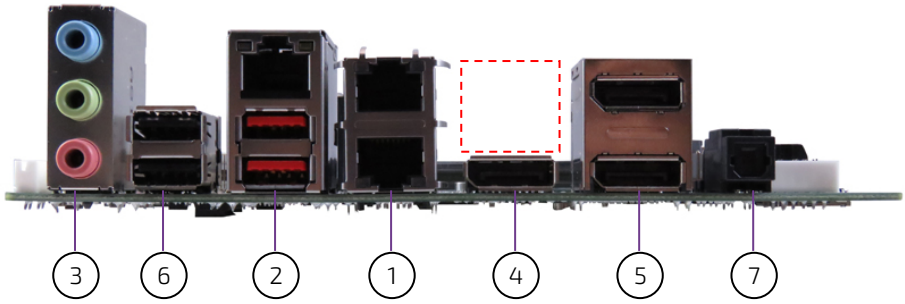


Table 11: Connector Panel Side Connector List

Item	Designation	Description	See Chapter
1	CN16	GbE LAN2 & GbE LAN3 Connector	6.2
2	CN17	GbE LAN1 & USB 3.1 Port-0, 1 Connector	6.2 & 6.3
3	CN18	3 Stack-up Azalia Audio Phone Jack	6.4
4	CN20B	Single DisplayPort Connector (Configuration 1)	6.1
	CN20A & CN20B	Dual DisplayPort Connector (Configuration 2)	
5	CN21C & CN21D	Dual DisplayPort Connector	6.1
6	CN22	USB 2.0 Port 4, 5	6.3
7	CN24	Optical S/PDIF Output Connector	

5/ Connector Definitions

The following defined terms are used within this user guide to give more information concerning the pin assignment and to describe the connector's signals.

Defined Term	Description
Pin	Shows the pin numbers in the connector
Signal	The abbreviated name of the signal at the current pin The notation "XX#" states that the signal "XX" is active low
Note	Special remarks concerning the signal
Designation	Type and number of item described
See Chapter	Number of the chapter within this user guide containing a detailed description

The abbreviation TBD is used for specifications that are not available yet or which are not sufficiently specified by the component vendors.

6/ I/O-Area Connectors

6.1. DP Connector (CN20 Port A, CN20 Port B, CN21 Port C & CN21 Port D)

The DP (DisplayPort) connector is based on standard DP female port.

Port A and Port B support DP++, allowing users to use a passive adapter to convert DP signals to single-link DVI or HDMI.

Port A is a BOM option to replace LVDS (LVDS1).

Figure 5: DP Connector CN20 Port A, CN20 Port B, CN21 Port C, CN21 Port D

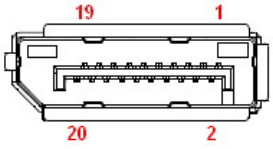


Table 12: Pin Assignment DP Connector CN20 Port A, CN20 Port B, CN21 Port C, CN21 Port D

Pin	Signal	Description	Note
1	TX0+	DisplayPort Lane 0 transmitter differential pair (+)	
2	GND	Ground	
3	TX0-	DisplayPort Lane 0 transmitter differential pair (-)	
4	TX1+	DisplayPort Lane 1 transmitter differential pair (+)	
5	GND	Ground	
6	TX1-	DisplayPort Lane 1 transmitter differential pair (-)	
7	TX2+	DisplayPort Lane 2 transmitter differential pair (+)	
8	GND	Ground	
9	TX2-	DisplayPort Lane 2 transmitter differential pair (-)	
10	TX3+	DisplayPort Lane 3 transmitter differential pair (+)	
11	GND	Ground	
12	TX3-	DisplayPort Lane 3 transmitter differential pair (-)	
13	GND	Ground	
14	GND	Ground	
15	AUX+	DisplayPort Auxiliary channel differential pair (+)	
16	GND	Ground	
17	AUX-	DisplayPort Auxiliary channel differential pair (-)	
18	HPD	DisplayPort hot plug detect	
19	GND	Ground	
20	PWR	Power for connector	

6.2. Ethernet Connectors (CN17 - LAN1, CN16 - LAN2 & CN16 - LAN3)

The mITX-VR1000 V2.0 supports three channels of 10/100/1000 Mbit Ethernet, which are based Intel® I210-AT and Intel® I211-AT controllers.

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100 MByte and Category 5E, 6 or 6E with 1 Gbit LAN networks.

The signals for the Ethernet ports are as follows:

Figure 6: Ethernet Connectors CN17 - LAN1, CN16 - LAN2, CN16 - LAN3

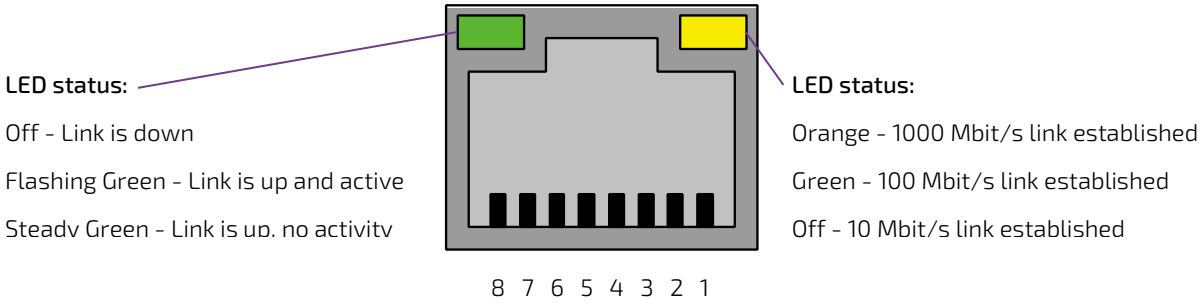


Table 13: Pin Assignment Ethernet Connectors CN17 - LAN1, CN16 - LAN2, CN16 - LAN3

Pin	Signal	Note
1	TX1+	
2	TX1-	
3	TX2+	
4	TX3+	
5	TX3-	
6	TX2-	
7	TX4+	
8	TX4-	

Signal Description

Signal	Description
TX1+ / TX1-	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
TX2+ / TX2-	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
TX3+ / TX3-	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
TX4+ / TX4-	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair.In MDI crossover mode, this pair acts as the BI_DC+/- pair.

'MDI' – media dependent Interface

6.3. USB Connectors (I/O Area)

The external I/O connector panel supports one dual USB 2.0 connector and one dual USB 3.1 connector.

USB 3.1 ports are backward compatible with USB 2.0.

Figure 7: USB 2.0 Connectors CN22 - USB 2.0 Port 4 / 5

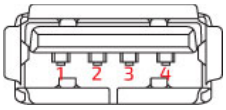


Table 14: Pin Assignment USB 2.0 Connectors CN22 - USB 2.0 Port 4 / 5

Pin	Signal	Description	Note
1	+USBVCC*	+5 V power supply for USB device	
2	USB_D-	USB 2.0 differential pair (-)	
3	USB_D+	USB 2.0 differential pair (+)	
4	GND	Ground	

Figure 8: USB 3.1 Connector CN17 - USB 3.1 Port 0 / 1

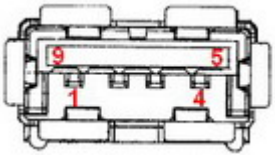


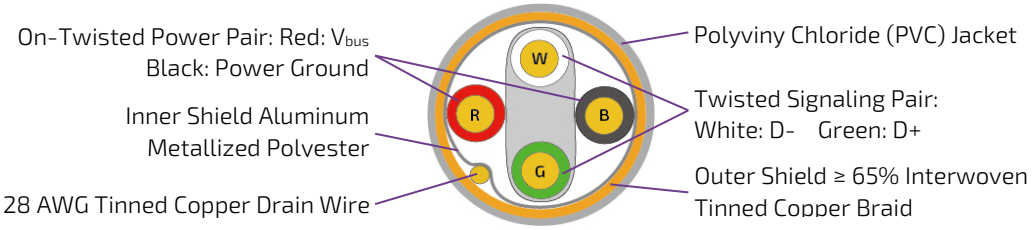
Table 15: Pin Assignment USB 3.1 Connector CN17 - USB 3.1 Port 0 / 1

Pin	Signal	Description	Note
1	+USBVCC	+5 V power supply for USB device	
2	USB_D-	USB 2.0 differential pair (-)	
3	USB_D+	USB 2.0 differential pair (+)	
4	GND	Ground	
5	USB3_SSRX-	USB 3.1 receiver differential pair (-)	
6	USB3_SSRX+	USB 3.1 receiver differential pair (+)	
7	GND	Ground	
8	USB3_SSTX-	USB 3.1 transmitter differential pair (-)	
9	USB3_SSTX+	USB 3.1 transmitter differential pair (+)	

* The power source of +USBVCC can be selected by JP4.

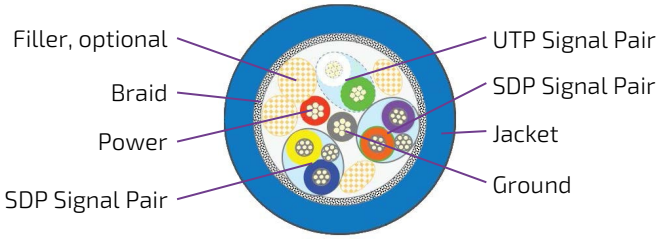
For HiSpeed rates it is required to use a USB cable, which is specified in USB 2.0 standard:

Figure 9: USB 2.0 High Speed Cable



For USB 3.0 cabling it is required to use only HiSpeed USB cable, specified in USB3.0 standard:

Figure 10: USB 3.0 High Speed Cable



6.4. 3 Stack-up Azalia Audio Phone Jack (CN18)

The external I/O connector panel supports one 3.5 mm triple-port Azalia audio phone jack for headset, microphone and audio input devices. The audio output signals are shared with those of the speaker connectors CN19 & CN25.

Figure 11: Audio Jack CN18

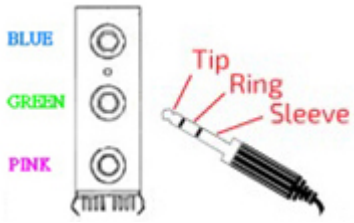


Table 16: Pin Assignment Audio Jack CN18

Pin	Signal	Description	Note
Top			
Tip	Line-In_L	Audio input left channel signal	
Ring	Line-In_R	Audio input right channel signal	
Sleeve	GND	Ground	
Middle			
Tip	Line-Out_L	Audio output left channel signal	
Ring	Line-Out_R	Audio output right channel signal	
Sleeve	GND	Ground	
Bottom			
Tip	Mic-In_L	Microphone input left channel signal	
Ring	Mic-In_R	Microphone input right channel signal	
Sleeve	GND	Ground	

7/ Internal Connectors

7.1. Power Connector

The mITX-VR1000 V2.0 is designed to be supplied from a 2x4-pin +12 VDC power supply.

NOTICE

Hot plugging any of the power connector is not allowed.

Hot plugging might damage the board. In other words, turn off main supply etc. to make sure all the power lines are turned off when connecting to the motherboard.

7.1.1. 2x4-pin ATX Power Supply Wafer (ATX1)

The 2x4-pin ATX power supply wafer provides +12 V DC to the board.

Figure 12: 2x4-pin ATX Power Supply Wafer ATX1

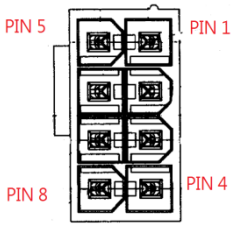


Table 17: Pin Assignment ATX1

Pin	Signal	Description	Note
1	GND	Ground	
2	GND	Ground	
3	GND	Ground	
4	GND	Ground	
5	+12V	Power +12 V	
6	+12V	Power +12 V	
7	+12V	Power +12 V	
8	+12V	Power +12 V	

7.1.2. CR2032 Battery Holder (BAT2)

The holder is intended to be accommodate the CR2032 battery. The battery provides power to the system clock to retain the time when power is turn off.

Figure 13: CR2032 Battery Holder BAT2

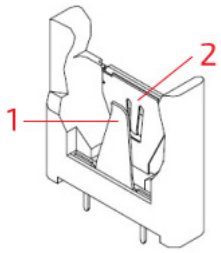


Table 18: Pin Assignment BAT2

Pin	Signal	Description	Note
1	Battery+	RTC Battery+	
2	Battery-	RTC Battery-	

7.2. Fan Wafers (FAN1 & FAN2)

The CPU FAN Wafer (FAN1) is used for the connection of the FAN for the CPU while the System FAN Wafer (FAN2) for the connection of the FAN for the system.

Figure 14: Fan Wafer FAN1, FAN2

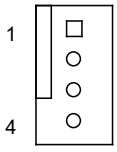


Table 19: Pin Assignment FAN1, FAN2

Pin	Signal	Description	Note
1	GND	Power supply ground signal	
2	+12V	+12 V power supply for fan	
3	SENSE	Sense input signal from the fan, for rotation speed supervision RPM (Rotations Per Minute).	
4	PWM	PWM output signal for FAN speed control	

7.3. SATA (Serial ATA) Port 0 & Port 1 Connector (SATA1 & SATA2)

The SATA connectors (SATA1 & SATA2) supply the data connection for the SATA hard disk and are SATA 3.0 compatible. They share the same SATA signals with M.2 Key M sockets (M2M1 & M2M2 respectively). The default assembly configuration is the SATA connector SATA1 and M.2 Key M socket M2M2.

Figure 15: SATA Connector SATA1, SATA2

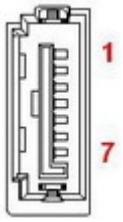


Table 20: Pin Assignment SATA1, SATA2

Pin	Signal	Description	Note
1	GND	Ground	
2	TX+	Host transmitter differential signal pair (+)	
3	TX-	Host transmitter differential signal pair (-)	
4	GND	Ground	
5	RX-	Host receiver differential signal pair (-)	
6	RX+	Host receiver differential signal pair (+)	
7	GND	Ground	

7.4. HDD Power Output Wafer 1 & Wafer 2 (CN11 & CN12)

The 1x4-pin 2.5 mm pitch HDD power output wafer provides power to the SATA hard disk.

Figure 16: HDD Power Output Wafer CN11, CN12

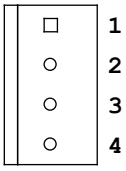


Table 21: Pin Assignment CN11, CN12

Pin	Signal	Description	Note
1	+12V	+12 V power supply for HDD	
2	GND	Ground	
3	GND	Ground	
4	+5V	+5 V power supply for HDD	

7.5. USB Connectors (Internal) (CN27 & CN29 / USB1)

The USB port pin header CN27 supports two USB 2.0 ports and the USB port wafer CN29 supports one USB 2.0 port. The wafer CN29 can be replaced with an onboard USB 2.0 Type A 90° connector (USB1). The default assembly configuration is the wafer CN29.

Figure 17: USB 2.0 Port DN_1, DN_2 Pin Header CN27

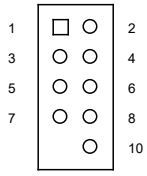


Table 22: Pin Assignment CN27

Pin	Signal	Description	Note
1	+USBVCC	5 V supply. SB5V is supplied during power down to allow wakeup.	
2	+USBVCC	5 V supply. SB5V is supplied during power down to allow wakeup.	
3	USB_A-	USB 2.0 differential pair (-) for channel A	
4	USB_B-	USB 2.0 differential pair (-) for channel B	
5	USB_A+	USB 2.0 differential pair (+) for channel A	
6	USB_B+	USB 2.0 differential pair (+) for channel B	
7	GND	Ground	
8	GND	Ground	
9	KEY		
10	GND	Ground	

Figure 18: USB 2.0 Port 5 Wafer CN29

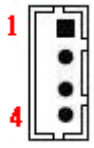


Table 23: Pin Assignment CN29

Pin	Signal	Description	Note
1	+USBVCC	5 V power supply	
2	USB_-	USB 2.0 differential pair (-)	
3	USB_+	USB 2.0 differential pair (+)	
4	GND	Ground	

Figure 19: USB 2.0 Connector USB1

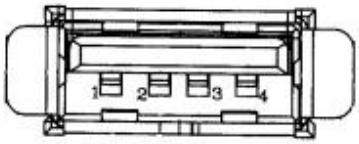


Table 24: Pin Assignment USB1

Pin	Signal	Description	Note
1	+USBVCC	5 V power supply	
2	USB_-	USB 2.0 differential pair (-)	
3	USB_+	USB 2.0 differential pair (+)	
4	GND	Ground	

7.6. Speaker Connector (CN19 & CN25)

The Speaker audio-out interface is available through the wafers CN19 and CN25. These outputs are shared with the audio output (Line-out) signals of the audio jack CN18.

Figure 20: 3W Audio AMP Output Wafer CN19 (Right Channel), CN25 (Left Channel)

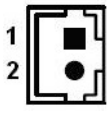


Table 25: Pin Assignment CN19, CN20

Pin	Signal	Description	Note
1	Speaker+	Speaker output (+)	
2	Speaker-	Speaker output (-)	

7.7. Front Panel Audio Pin Header (CN28)

The front panel audio pin header provides audio output (Line-Out) and microphone (Mic-In) signals through the wafer CN28. The audio output signals are shared with those of the speaker connectors CN19 & CN25.

Figure 21: Front Panel Audio Pin Header CN28

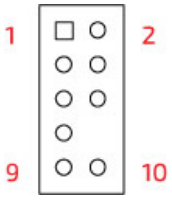


Table 26: Pin Assignment CN28

Pin	Signal	Description	Note
1	MIC2-L	Microphone input left channel signal	
2	Audio GND	Audio ground	
3	MIC2-R	Microphone input right channel signal	
4	Audio GND	Audio ground	
5	Line2-R	Audio output right channel signal	
6	MIC2_JD	Microphone jack detection	
7	Audio GND	Audio ground	
8	Key		
9	Line2-L	Audio output left channel signal	
10	Line2_JD	Audio output jack detection	

7.8. Front Panel Pin Header (FP1 & FP2)

The front panel connector FP1 supplies signals for the reset button, storage LED and system warning speaker.

The front panel connector FP2 supplies signals for the power button, power LED and SM Bus.

Figure 22: Front Panel 1 Pin Header FP1

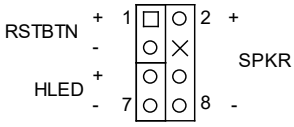


Table 27: Pin Assignment FP1

Pin	Signal	Description	Note
1	Reset Button +	System reset button (+)	
2	Speaker +	External system warning speaker (+)	
3	Reset Button -	System reset button (-)	
4	NC	No connection	
5	HDD LED +	HDD activity LED (+). The LED lights up or flashes when data is ready from or written to the HDD.	
6	Internal Speaker -	Internal system warning speaker (-)	
7	HDD LED -	HDD activity LED (-).	
8	Speaker -	External system warning speaker (-)	

Internal Buzzer is enabled when Pin6-8 is shorted.

Figure 23: Front Panel 2 Pin Header FP2

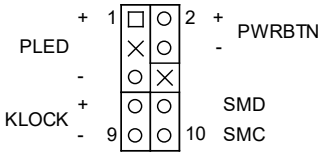


Table 28: Pin Assignment FP2

Pin	Signal	Description	Note
1	Power LED +	System Power LED (+). The LED lights up when users turn on the system power, and blinks when the system is in sleep mode.	
2	Power Button +	System power button (+). Pressing the power button turns the system on or puts the system in sleep or soft-off mode depending on the operating system settings. Pressing the power switch for more than four seconds while the system turns from ON to OFF.	
3	NC	No connection	

Pin	Signal	Description	Note
4	Power Button -	System power button (-).	
5	Power LED -	System Power LED (-).	
6	SMB_ALERT#	System management bus alert	
7	BATLOW#	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low. It also can be used to signal some other external power management event.	
8	SMBus Data	System management bus bidirectional data line	
9	GND	Ground	
10	SMBus Clock	System management bus bidirectional clock line	

7.9. S/PDIF Out Pin Header (CN15)

The S/PDIF audio output jack is supplied via the internal pin header (CN15).

Figure 24: S/PDIF Out Pin Header CN15

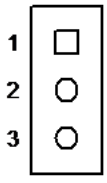


Table 29: Pin Assignment CN15

Pin	Signal	Description	Note
1	SPDIF-O	S/PDIF digital output	
2	+5V	+5 V power supply	
3	GND	Ground	

7.10. Serial COM1 - COM6 Ports (CN3, CN4, CN5, CN7, CN8 & CN10)

The serial connectors CN3 and CN4 provide RS232/422/485 connections.

The serial connections CN5, CN7, CN8 and CN10 provide RS232 connections.

Figure 25: Serial COM CN3, CN4, CN5, CN7, CN8, CN10

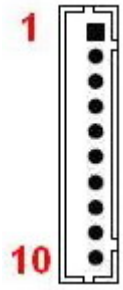


Table 30: Pin Assignment CN3, CN4

Pin	RS232 Signal	RS422 Signal	Half Duplex RS485 Signal	Full Duplex RS485 Signal	Note
1	DCD	TX-	DATA-	TX-	
2	DSR	N/A	N/A	N/A	
3	RXD	TX+	DATA+	TX+	
4	RTS	N/A	N/A	N/A	
5	TXD	RX+	N/A	RX+	
6	CTS	N/A	N/A	N/A	
7	DTR	RX-	N/A	RX-	
8	RI	N/A	N/A	N/A	
9	GND	GND	GND	GND	
10	+5V	+5V	+5V	+5V	

Table 31: Pin Assignment CN5, CN7, CN8, CN10

Pin	RS232 Signal	Note
1	DCD	
2	DSR	
3	RXD	
4	RTS	
5	TXD	
6	CTS	
7	DTR	
8	RI	
9	GND	
10	+5V	

The COM ports need to install an OS patch from ITE. The patch is only available for Windows and is not available Linux.

Table 32: Serial COM Signal Description

Signal	Description
TXD	Transmitted Data, sends data to the communications link. The signal is set to the marking state (-12 V) on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RXD	Received Data, receives data from the communications link.
DTR	Data Terminal Ready, indicates to the modem etc. that the on-board UART is ready to establish communication link.
DSR	Data Set Ready, indicates that the modem etc. is ready to establish a communications link.
RTS	Request To Send, indicates to the modem etc. that the on-board UART is ready to exchange data.
CTS	Clear To Send, indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator, indicates that the modem has received a ringing signal from the telephone line.
TX+/-	Transmitted Data differential pair sends data to the communications link.
RX+/-	Received Data differential pair receives data from the communications link.
GND	Power Supply GND signal

7.11. LVDS Panel Connector (LVDS1)

The 24-bit, 2-channel LVDS connector is based on 2x15-pin 1.25 mm pitch connector.

Figure 26: LVDS Connector LVDS1

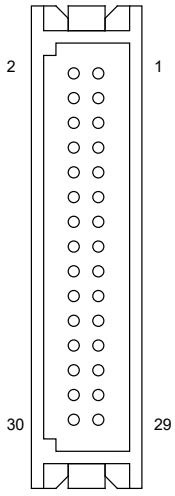


Table 33: Pin Assignment LVDS1

Pin	Signal	Description	Note
1	VDD_EN	Output Display Enable	
2	GND	Ground	
3	+3.3V / +5V *	+3.3 V / +5 V power supply	
4	+3.3V / +5V *	+3.3 V / +5 V power supply	
5	TxclkA-	LVDS Channel A clock differential pair (-)	
6	TxclkB-	LVDS Channel B clock differential pair (-)	
7	TxclkA+	LVDS Channel A clock differential pair (+)	
8	TxclkB+	LVDS Channel B clock differential pair (+)	
9	GND	Ground	
10	GND	Ground	
11	TxoutA0-	LVDS Channel A Data 0 differential pair (-)	
12	TxoutB0-	LVDS Channel B Data 0 differential pair (-)	
13	TxoutA0+	LVDS Channel A Data 0 differential pair (+)	
14	TxoutB0+	LVDS Channel B Data 0 differential pair (+)	
15	TxoutA1-	LVDS Channel A Data 1 differential pair (-)	
16	TxoutB1-	LVDS Channel B Data 1 differential pair (-)	
17	TxoutA1+	LVDS Channel A Data 1 differential pair (+)	
18	TxoutB1+	LVDS Channel B Data 1 differential pair (-)	
19	TxoutA2-	LVDS Channel A Data 2 differential pair (-)	
20	TxoutB2-	LVDS Channel B Data 2 differential pair (-)	
21	TxoutA2+	LVDS Channel A Data 2 differential pair (+)	
22	TxoutB2+	LVDS Channel B Data 2 differential pair (+)	

Pin	Signal	Description	Note
23	TxoutA3-	LVDS Channel A Data 3 differential pair (-)	
24	TxoutB3-	LVDS Channel B Data 3 differential pair (-)	
25	TxoutA3+	LVDS Channel A Data 3 differential pair (+)	
26	TxoutB3+	LVDS Channel B Data 3 differential pair (+)	
27	GND	Ground	
28	GND	Ground	
29	DDC_Data	DDC channel Data	
30	DDC_Clock	DDC Channel Clock	

* **Panel power can be selected by JP3.**

7.12. Backlight Power Output Wafer for LVDS1 (CN23)

The wafer CN23 provides power supply for flat panel and its backlight inverter.

Figure 27: Backlight Power Output Wafer CN23

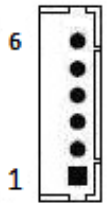


Table 34: Pin Assignment CN23

Pin	Signal	Description	Note
1	BL_EN**	Backlight Enable signal	
2	BL_ADJ_PWM	Backlight Adjustment PWM (Pulse Width Modulation) signal	
3	+5V / +12V*	+5 V / +12 V power supply	
4	+5V / +12V*	+5 V / +12 V power supply	
5	GND	Ground	
6	GND	Ground	

* Backlight Power can be selected by JP8.

** BL_EN can be selected by JP7.

7.13. Digital Input / Output Wafer (CN2)

The wafer CN2 supports 8-bit digital input / output signals to provide powering-on function of the connected devices.

Figure 28: Digital Input / Output Wafer CN2

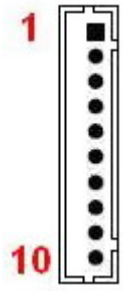


Table 35: Pin Assignment CN2

Pin	Signal	Description	Note
1	+5V	+5 V power supply	
2	DIO_0	Digital input / output channel 0	
3	DIO_1	Digital input / output channel 1	
4	DIO_2	Digital input / output channel 2	
5	DIO_3	Digital input / output channel 3	
6	DIO_4	Digital input / output channel 4	
7	DIO_5	Digital input / output channel 5	
8	DIO_6	Digital input / output channel 6	
9	DIO_7	Digital input / output channel 7	
10	GND	Ground	

7.14. mPCIe Socket (MPCIE1)

Full-sized Mini-PCI Express V1.2 socket (MPCIE1). Socket MPCIE1 supports mPCIe, USB 2.0 and SIM-card socket. The SIM-card socket makes it possible to use a WWAN wireless modem in this mPCIe slot. The USB does support WAKE function.

Figure 29: mPCIe Slot Connector MPCIE1

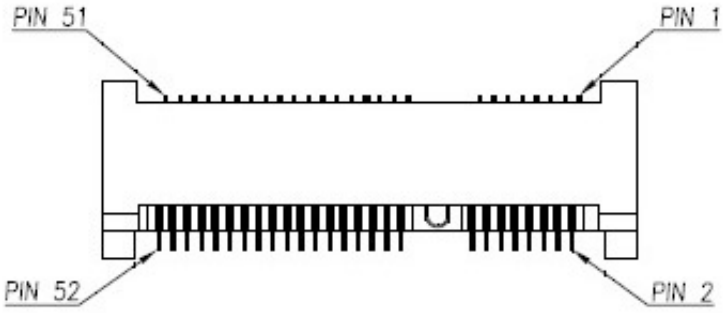


Table 36: Pin Assignment MPCIE1

Pin	Signal	Description	Note
1	WAKE#	Requests the host interface to return to full operation and respond to PCIe	
2	+3.3VSB	+3.3 V standby power supply	
3	Reserved		
4	Ground		
5	Reserved		
6	+1.5V	+1.5 V power supply	
7	CLKREQ#	Reference clock request signal	
8	UIM_PWR*	Power source for User Identity Modules (UIM)	
9	Ground		
10	UIM_DATA*	Data signal for User Identity Modules (UIM)	
11	REFCLK-	Reference clock differential pair (-)	
12	UIM_CLK*	Clock signal for User Identity Modules (UIM)	
13	REFCLK+	Reference clock differential pair (+)	
14	UIM_RESET*	Reset signal for User Identity Modules (UIM)	
15	Ground		
16	UIM_VPP*	Variable supply voltage for User Identity Module (UIM)	
17	Reserved		
18	Ground		
19	Reserved		
20	W_Disable#	Wireless disable signal	
21	Ground		
22	PERST#	PCI Express reset	
23	PERn0	PCIe Lane 0 receiver differential pair (-)	
24	+3.3VSB	+3.3 V standby power supply	

Pin	Signal	Description	Note
25	PERp0	PCIe Lane 0 receiver differential pair (+)	
26	Ground		
27	Ground		
28	+1.5V	+1.5 V power supply	
29	Ground		
30	SMB_CLK	System management bus clock	
31	PETn0	PCIe Lane 0 transmitter differential pair (-)	
32	SMB_DATA	System management bus data	
33	PETp0	PCIe Lane 0 transmitter differential pair (+)	
34	Ground		
35	Ground		
36	USB_D-	USB 2.0 differential pair (-)	
37	Ground		
38	USB_D+	USB 2.0 differential pair (+)	
39	+3.3VSB	+3.3 V standby power supply	
40	Ground		
41	+3.3VSB	+3.3 V standby power supply	
42	LED_WWAN#	LED status indicator signal for WWAN	
43	Ground / NC		
44	LED_WLAN#	LED status indicator signal for WLAN	
45	Reserved		
46	LED_WPAN#	LED status indicator signal for WPAN	
47	Reserved		
48	+1.5V	+1.5 V power supply	
49	Reserved		
50	Ground		
51	Reserved		
52	+3.3VSB	+3.3 V standby power supply	

* **These pins are connected to CN26 SIM Interface directly.**

7.15. M.2 Socket (M2B1, M2M1 & M2M2)

The mITX-VR1000 V2.0 supports up to three M.2 modules: one in format 2242 / 2280 with Key B and the other two in format 2280 with Key M.

The M.2 Key B socket (M2B1) shares the same PCIe x2 signals with the PCIe x2 slot (PCIE1). The default assembly configuration is the M.2 Key B socket M2B1. The specifications supports USB 2.0 and PCIe x2 / PCIe x1 + USB 3.0 (default assembly configuration is PCIe x2) signals as well as a SIM card socket. The SIM card socket makes it possible to use a WWAN wireless modem in this M.2 socket.

The M.2 Key M sockets (M2M1 & M2M2) supports SATA signals. They share the same SATA signals with the SATA connectors (SATA1 & SATA2 respectively). The default assembly configuration is the M.2 Key M socket M2M2 and SATA connector SATA1.

Figure 30: M.2 Key B Slot Connector M2B1

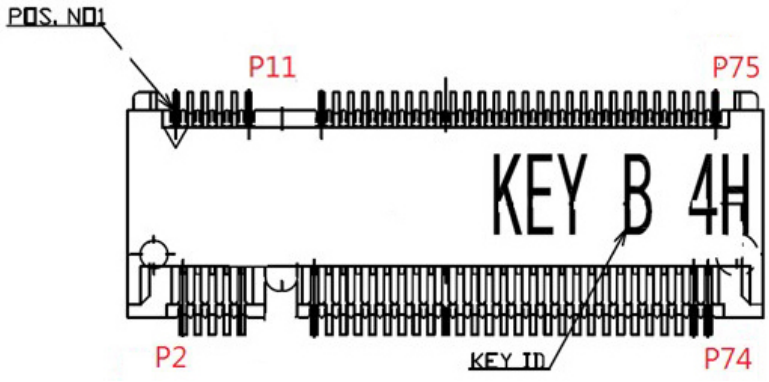


Table 37: Pin Assignment M2B1

Pin	Signal	Description	Note
1	NC		
2	+3.3V	+3.3 V power supply	
3	GND	Ground	
4	+3.3V	+3.3 V power supply	
5	GND	Ground	
6	M2B_ PWROFF#	M.2 module power off active low	
7	USB-D+	USB 2.0 differential pair (+)	
8	M2B_WDIS1#	Wireless disable signal	
9	USB-D-	USB 2.0 differential pair (-)	
10	M2B_LED1#	Device active signal	
11	GND	Ground	
12	KEY B		
13	KEY B		
14	KEY B		
15	KEY B		
16	KEY B		
17	KEY B		
18	KEY B		

Pin	Signal	Description	Note
19	KEY B		
20	NC		
21	NC		
22	NC		
23	NC		
24	NC		
25	NC		
26	NC		
27	GND	Ground	
28	NC		
29	M2B1_RXN / USB3.0 RX-**	PCIe Lane 1 / USB 3.0 receiver differential pair (-)	
30	UIM RESET*	Reset signal for User Identity Modules (UIM)	
31	M2B1_RXP / USB3.0 RX+**	PCIe Lane 1 / USB 3.0 receiver differential pair (+)	
32	UIM CLK*	Clock signal for User Identity Modules (UIM)	
33	GND	Ground	
34	UIM DATA*	Data signal for User Identity Modules (UIM)	
35	M2B1_TXN / USB3.0 TX-**	PCIe Lane 1 / USB 3.0 transmitter differential pair (-)	
36	UIM PWR*	Power source for User Identity Modules (UIM)	
37	M2B1_TXP / USB3.0 TX+**	PCIe Lane 1 / USB 3.0 transmitter differential pair (+)	
38	NC		
39	GND	Ground	
40	NC		
41	M2B0_RXN	PCIe Lane 0 receiver differential pair (-)	
42	NC		
43	M2B0_RXP	PCIe Lane 0 receiver differential pair (+)	
44	NC		
45	GND	Ground	
46	NC		
47	M2B0_TXN	PCIe Lane 0 transmitter differential pair (-)	
48	NC		
49	M2B0_TXP	PCIe Lane 0 transmitter differential pair (+)	
50	PCIE_RST#	PCI Express reset	
51	GND	Ground	
52	M2B_CLKREQ#	Reference clock request signal	
53	REFCLKN	Reference clock differential pair (-)	
54	PCIE_WAKE#	PCIe wake	
55	REFCLKP	Reference clock differential pair (+)	
56	NC		
57	GND	Ground	
58	NC		
59	NC		
60	NC		

Pin	Signal	Description	Note
61	NC		
62	NC		
63	NC		
64	NC		
65	NC		
66	M2B_SIM_DETECT	SIM card detect	
67	M2B_RESET#	M.2 module reset active low	
68	M2B_SUSCLK	32.768 kHz clock supply input	
69	NC		
70	+3.3V	+3.3 V power supply	
71	GND	Ground	
72	+3.3V	+3.3 V power supply	
73	GND	Ground	
74	+3.3V	+3.3 V power supply	
75	NC		

* These pins are connected to SIM card connector SIM1 directly.

* These pins are BOM option.

Figure 31: M.2 Key M Slot Connector M2M1, M2M2

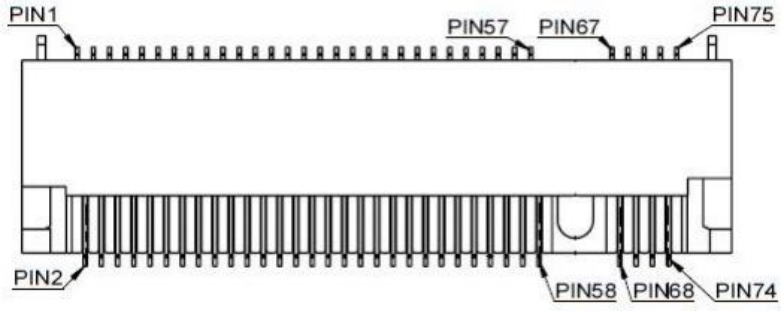


Table 38: Pin Assignment M2M1, M2M2

Pin	Signal	Description	Note
1	GND	Ground	
2	+3.3V	+3.3 V power supply	
3	GND	Ground	
4	+3.3V	+3.3 V power supply	
5	NC		
6	NC		

Pin	Signal	Description	Note
7	NC		
8	NC		
9	GND	Ground	
10	NC		
11	NC		
12	+3.3V	+3.3 V power supply	
13	NC		
14	+3.3V	+3.3 V power supply	
15	GND	Ground	
16	+3.3V	+3.3 V power supply	
17	NC		
18	+3.3V	+3.3 V power supply	
19	NC		
20	NC		
21	GND	Ground	
22	NC		
23	NC		
24	NC		
25	NC		
26	NC		
27	GND	Ground	
28	NC		
29	NC		
30	NC		
31	NC		
32	NC		
33	GND	Ground	
34	NC		
35	NC		
36	NC		
37	NC		
38	DEVSLP	Device sleep	
39	GND	Ground	
40	NC		
41	SATAB+	SATA transmitter differential pair (+)	
42	NC		
43	SATAB-	SATA transmitter differential pair (-)	
44	NC		
45	GND	Ground	
46	NC		
47	SATAA-	SATA receiver differential pair (-)	
48	NC		

Pin	Signal	Description	Note
49	SATAA+	SATA receiver differential pair (+)	
50	NC		
51	GND	Ground	
52	NC		
53	NC		
54	NC		
55	NC		
56	NC		
57	GND	Ground	
58	NC		
59	KEY M		
60	KEY M		
61	KEY M		
62	KEY M		
63	KEY M		
64	KEY M		
65	KEY M		
66	KEY M		
67	NC		
68	NC		
69	GND	Ground	
70	+3.3V	+3.3 V power supply	
71	GND	Ground	
72	+3.3V	+3.3 V power supply	
73	GND	Ground	
74	+3.3V	+3.3 V power supply	
75	GND	Ground	

7.16. SIM Interface for M.2 Key B and mPCIe (SIM1 & CN26)

The push-push type Micro SIM card cage SIM1 is connected to M.2 Key B socket for Micro SIM card installation.

The wafer CN26 is intended to be connected to a SIM card cage for SIM card installation. It is connected to mPCIe socket.

Figure 32: Micro SIM Card Cage SIM1

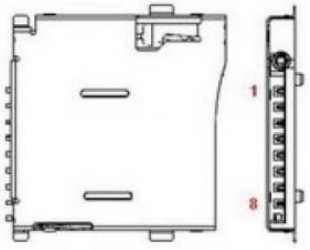


Table 39: Pin Assignment SIM1

Pin	Signal	Description	Note
1	UIM_PWR	Power +5V or +3.3V	
2	UIM_RESET	Reset signal	
3	UIM_CLK	Clock signal	
4	GND	Ground	
5	UIM_VPP	Programming voltage input	
6	UIM_DATA	Input or Output for serial data	
7	SIM_DETECT	SIM card detect signal	

Figure 33: SIM Interface Wafer CN26

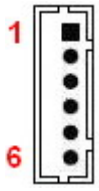


Table 40: Pin Assignment CN26

Pin	Signal	Description	Note
1	UIM_PWR	Power +5V or +3.3V	
2	UIM_DATA	Input or Output for serial data	
3	UIM_RESET	Reset signal	
4	UIM_VPP	Programming voltage input	
5	UIM_CLK	Clock signal	
6	GND	Ground	

7.17. PCI Express x16 Slot (PCIE2)

The mITX-VR1000 V2.0 supports PCI Express x16 via slot PCIE2 which supports PCIe x8 signal only.

Figure 34: PCIe x16 Slot Connector PCIE2

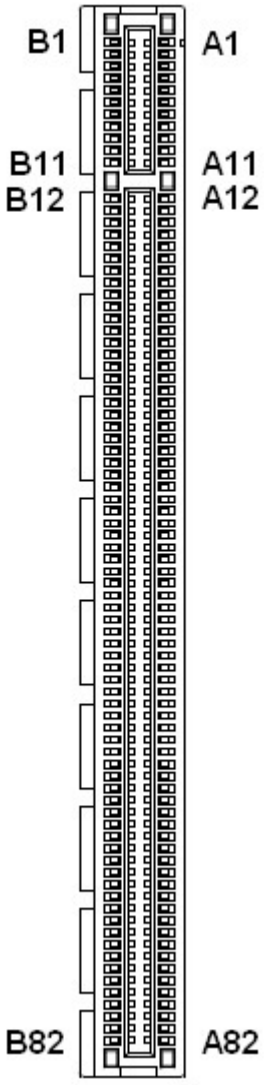


Table 41: Pin Assignment PCIE2

Pin	Side B		Side A	
	Signal	Description	Signal	Description
1	+12V	+12 V power	PRSNT1#	Hot plug presence detect
2	+12V	+12 V power	+12V	+12 V power
3	Reserved		+12V	+12 V power
4	Ground		Ground	
5	SMCLK	SMBus clock	Reserved	
6	SMDAT	SMBus data	Reserved	

Pin	Side B		Side A	
	Signal	Description	Signal	Description
7	Ground		Reserved	
8	+3.3V	+3.3 V power	Reserved	
9	Reserved		+3.3V	+3.3 V power
10	+3.3VSB	+3.3 V standby power	+3.3V	+3.3 V power
11	WAKE#	Link reactivation	PERST#	PCI Express reser
Mechanical Key				
12	Reserved		Ground	
13	Ground		REFCLK+	Reference clock differential pair (+)
14	HSOP0	Lane 0 transmitter differential pair (+)	REFCLK-	Reference clock differential pair (-)
15	HSON0	Lane 0 transmitter differential pair (-)	Ground	
16	Ground		HSIP0	Lane 0 receiver differential pair (+)
17	PRSNT2#	Hot plug presence detect	HSIN0	Lane 0 receiver differential pair (-)
18	Ground		Ground	
19	HSOP1	Lane 1 transmitter differential pair (+)	Reserved	
20	HSON1	Lane 1 transmitter differential pair (-)	Ground	
21	Ground		HSIP1	Lane 1 receiver differential pair (+)
22	Ground		HSIN1	Lane 1 receiver differential pair (-)
23	HSOP2	Lane 2 transmitter differential pair (+)	Ground	
24	HSON2	Lane 2 transmitter differential pair (-)	Ground	
25	Ground		HSIP2	Lane 2 receiver differential pair (+)
26	Ground		HSIN2	Lane 2 receiver differential pair (-)
27	HSOP3	Lane 3 transmitter differential pair (+)	Ground	
28	HSON3	Lane 3 transmitter differential pair (-)	Ground	
29	Ground		HSIP3	Lane 3 receiver differential pair (+)
30	Reserved		HSIN3	Lane 3 receiver differential pair (-)
31	PRSNT2#	Hot plug presence detect	Ground	
32	Ground		Reserved	
33	HSOP4	Lane 4 transmitter differential pair (+)	Reserved	
34	HSON4	Lane 4 transmitter differential pair (-)	Ground	
35	Ground		HSIP4	Lane 4 receiver differential pair (+)
36	Ground		HSIN4	Lane 4 receiver differential pair (-)
37	HSOP5	Lane 5 transmitter differential pair (+)	Ground	
38	HSON5	Lane 5 transmitter differential pair (-)	Ground	
39	Ground		HSIP5	Lane 5 receiver differential pair (+)
40	Ground		HSIN5	Lane 5 receiver differential pair (-)
41	HSOP6	Lane 6 transmitter differential pair (+)	Ground	
42	HSON6	Lane 6 transmitter differential pair (-)	Ground	
43	Ground		HSIP6	Lane 6 receiver differential pair (+)
44	Ground		HSIN6	Lane 6 receiver differential pair (-)
45	HSOP7	Lane 7 transmitter differential pair (+)	Ground	
46	HSON7	Lane 7 transmitter differential pair (-)	Ground	

Pin	Side B		Side A	
	Signal	Description	Signal	Description
47	Ground		HSIP7	Lane 7 receiver differential pair (+)
48	PRSNT2#	Hot plug presence detect	HSIN7	Lane 7 receiver differential pair (-)
49	Ground		Ground	
50	NC		Reserved	
51	NC		Ground	
52	Ground		NC	
53	Ground		NC	
54	NC		Ground	
55	NC		Ground	
56	Ground		NC	
57	Ground		NC	
58	NC		Ground	
59	NC		Ground	
60	Ground		NC	
61	Ground		NC	
62	NC		Ground	
63	NC		Ground	
64	Ground		NC	
65	Ground		NC	
66	NC		Ground	
67	NC		Ground	
68	Ground		NC	
69	Ground		NC	
70	NC		Ground	
71	NC		Ground	
72	Ground		NC	
73	Ground		NC	
74	NC		Ground	
75	NC		Ground	
76	Ground		NC	
77	Ground		NC	
78	NC		Ground	
79	NC		Ground	
80	Ground		NC	
81	PRSNT2#	Hot plug presence detect	NC	
82	Reserved		Ground	

7.18. PCI Express x4 Slot (PCIE1)

The mITX-VR1000 V2.0 supports PCI Express x4 via slot PCIE1 which supports PCIe x2 signal only.

The PCIe x4 slot (PCIE1) shares the same PCIe x2 signals with the M.2 Key B socket (M2B1). The default assembly configuration is the M.2 Key B socket M2B1.

Figure 35: PCIe x4 Slot Connector PCIE1

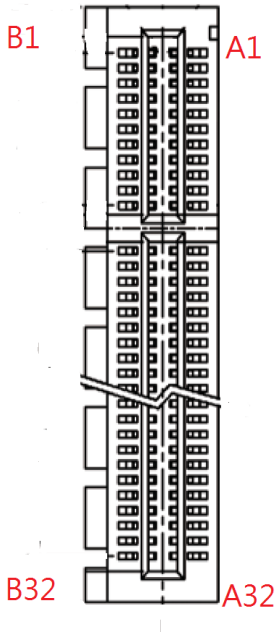


Table 42: Pin Assignment PCIE1

Pin	Side B		Side A	
	Signal	Description	Signal	Description
1	+12V	+12 V power	PRSNT1#	Hot plug presence detect
2	+12V	+12 V power	+12V	+12 V power
3	NC		+12V	+12 V power
4	Ground		Ground	
5	SMB_CLK	SMBus clock	NC	
6	SMB_DAT	SMBus data	NC	
7	Ground		NC	
8	+3.3V	+3.3 V power	NC	
9	NC		+3.3V	+3.3 V power
10	+3.3VSB	+3.3 V standby power	+3.3V	+3.3 V power
11	WAKE#	Link reactivation	RST#	PCI Express reser
Mechanical Key				
12	NC		Ground	
13	Ground		REFCLK+	Reference clock differential pair (+)
14	PETX0+	Lane 0 transmitter differential pair (+)	REFCLK-	Reference clock differential pair (-)

Pin	Side B		Side A	
	Signal	Description	Signal	Description
15	PETX0-	Lane 0 transmitter differential pair (-)	Ground	
16	Ground		PERX0+	Lane 0 receiver differential pair (+)
17	PRSNT2#1	Hot plug presence detect	PERX0-	Lane 0 receiver differential pair (-)
18	Ground		Ground	
19	PETX1+	Lane 1 transmitter differential pair (+)	NC	
20	PETX1-	Lane 1 transmitter differential pair (-)	Ground	
21	Ground		PERX1+	Lane 1 receiver differential pair (+)
22	Ground		PERX1-	Lane 1 receiver differential pair (-)
23	NC		Ground	
24	NC		Ground	
25	Ground		NC	
26	Ground		NC	
27	NC		Ground	
28	NC		Ground	
29	Ground		NC	
30	NC		NC	
31	NC		Ground	
32	Ground		NC	

7.19. mPCIe / M.2 Key B LED Pin Header (CN13 & CN14)

The pin header CN13 is intended to connect mPCIe activity LED cable.

The pin header CN14 is intended to connect M.2 Key B activity LED cable.

Figure 36: mPCIe / M.2 Key B LED Pin Header CN13, CN14

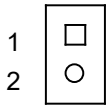


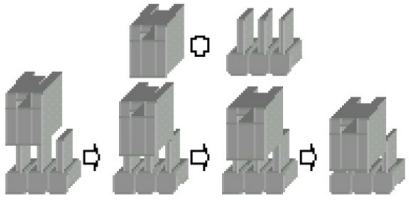
Table 43: Pin Assignment CN13, CN14

Pin	Signal	Description	Note
1	LED+		
2	LED-		

7.20. Switches and Jumpers

The product has several jumpers which must be properly configured to ensure correct operation.

Figure 37: Jumper Connector



For a three-pin jumper (see Figure 37), the jumper setting is designated "1-2" when the jumper connects pins 1 and 2. The jumper setting is designated "2-3" when pins 2 and 3 are connected and so on. You will see that one of the lines surrounding a jumper pin is thick, which indicates pin No.1.

To move a jumper from one position to another, use needle-nose pliers or tweezers to pull the pin cap off the pins and move it to the desired position.

7.20.1. Pin-9 Selection for COM1 & COM2 (JP1 & JP2)

The jumper JP1 and JP2 can be used to select the power voltage of Pin 9 of the serial COM port COM1 and COM2 respectively.

Figure 38: Pin-9 Selection (JP1, JP2)

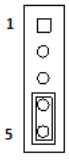


Table 44: Pin Assignment JP1, JP2

Jumper Position				Description
Pin 1-2	Pin 2-3	Pin 3-4	Pin 4-5	
X	-	-	-	Pin-9 = +12 V
-	X	-	-	Pin-9 = +5 V
-	-	X	-	Pin-9 = +5 V
-	-	-	X	Pin-9 = RI

"X" = Jumper set (short) and "-" = jumper not set (open)

7.20.2. AT / ATX Power Mode Selection (JP3)

The jumper JP3 can be used to select AT power mode or ATX power mode.

Figure 39: AT / ATX Power Mode Selection JP4

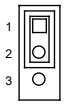


Table 45: Pin Assignment JP4

Jumper Position		Description
Pin 1-2	Pin 2-3	
X	-	ATX Mode
-	X	AT Mode

“X" = Jumper set (short) and “-” = jumper not set (open)

7.20.3. USB Power Selection (JP4)

The "USB Power Selection" jumper (JP4) can be used to determine whether the USB ports are powered in the S4 / S5 state.

Figure 40: USB Power Selection JP4

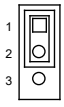


Table 46: Pin Assignment JP4

Jumper Position		Description
Pin 1-2	Pin 2-3	
X	-	USB power will be cut off in S4 & S5 state
-	X	USB power is always supplied

“X" = Jumper set (short) and “-” = jumper not set (open)

7.20.4. Clear CMOS Selection (JP6)

The jumper JP6 can be used to clear CMOS RTC content.

The jumper has two positions: Pin 1-2 mounted is the default configuration.

Figure 41: Clear CMOS Selection JP6

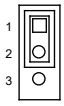


Table 47: Pin Assignment JP6

Jumper Position		Description
Pin 1-2	Pin 2-3	
X	-	Normal operation (default position)
-	X	Enable Clear CMOS RTC content (board does not boot with the jumper in this position)

"X" = Jumper set (short) and "-" = jumper not set (open)

Do not leave the jumper in position 2-3, otherwise if the power is disconnected, the battery will fully deplete within a few weeks.

7.20.5. Backlight Power Enable Selection for LVDS1 (JP7)

The jumper JP7 can be used to select voltage level of backlight enable signal for LVDS1.

Figure 42: Backlight Enable Selection JP7

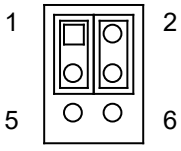


Table 48: Pin Assignment JP7

Jumper 1 Position		Description
Pin 1-3	Pin 3-5	
X	-	Backlight Enable Level = +3.3 V
-	X	Backlight Enable Level = +5 V
Jumper 2 Position		Description
Pin 2-4	Pin 4-6	
X	-	Backlight Enable High Active
-	X	Backlight Enable Low Active

"X" = Jumper set (short) and "-" = jumper not set (open)

7.20.6. Panel & Backlight Power Selection for LVDS1 (JP8)

The jumper JP8 can be used to select LVDS panel and backlight power voltage for LVDS1.

Figure 43: Panel & Backlight Power Selection JP8

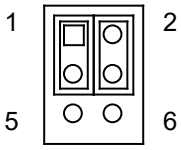


Table 49: Pin Assignment JP8

Jumper 1 Position		Description
Pin 1-3	Pin 3-5	
X	-	Backlight Power = +12 V
-	X	Backlight Power = +5 V
Jumper 2 Position		Description
Pin 2-4	Pin 4-6	
X	-	Panel Power = +3.3 V
-	X	Panel Power = +5 V

"X" = Jumper set (short) and "-" = jumper not set (open)

7.20.7. LVDE_EDID Selection (JP9)

Figure 44: LVDE_EDID Selection JP9

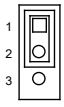


Table 50: Pin Assignment JP9

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	Normal
-	X	LVDE_EDID Write

"X" = Jumper set (short) and "-" = jumper not set (open)

8/ BIOS

8.1. Starting the uEFI BIOS

The mITX-VR1000 V2.0 is provided with a Kontron-customized, pre-installed and configured version of AMI Aptio® V uEFI BIOS. AMI BIOS firmware is based on the Unified Extensible Firmware Interface (UEFI) specification and the AMD Platform Innovation Framework for EFI. This uEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the mITX-VR1000 V2.0.

The uEFI BIOS comes with a setup program that provides quick and easy access to the individual function settings for control or modification of the uEFI BIOS configuration. The setup program allows the accessing of various menus that provide functions or access to sub-menus with more specific functions of their own.

To start the uEFI BIOS setup program, follow the steps below:

1. Power on the board.
2. Wait until the first characters appear on the screen (POST messages or splash screen).
3. Press the <DEL> key.
4. If the uEFI BIOS is password-protected, a request for password will appear. Enter either the User Password or the Supervisor Password (see Security menu), press <RETURN>, and proceed with step 5.
5. A setup menu will appear.

The mITX-VR1000 V2.0 uEFI BIOS setup program uses a hot key-based navigation system. A hot key legend bar is located on the bottom of the setup screens.

The following table provides information concerning the usage of these hot keys.

Table 51: Hotkeys Table

Signal	Description
<F1>	The <F1> key invokes the General Help window.
<->	The <Minus> key selects the next lower value within a field.
<+>	The <Plus> key selects the next higher value within a field.
<F2>	The <F2> key loads the previous values.
<F3>	The <F3> key loads the standard default values.
<F4>	The <F4> key saves the current settings and exit the uEFI BIOS setup.
<→> or <←>	The <Left/Right> arrows selects major setup menus on the menu bar. For example: Main, Advanced, Security, etc.
< ↑ > or < ↓ >	The <Up/Down> arrows selects fields in the current menu. For example: A setup function or a sub-screen.
<ESC>	The <ESC> key exits a major setup menu and enter the Exit setup menu. Pressing the <ESC> key in a sub-menu displays the next higher menu level.
<RERURN>	The <RETURN> key executes a command or select a submenu.

8.2. Starting the uEFI BIOS

The Setup utility features shows six menus in the selection bar at the top of the screen:

- Main
- Advanced
- Power
- Boot
- Security
- Save & Exit

The Setup menus are selected via the left and right arrow keys. The currently active menu and the currently active uEFI BIOS Setup item are highlighted in white. Each Setup menu provides two main frames. The left frame displays all available functions. Functions that can be configured are displayed in blue. Functions displayed in gray provide information about the status or the operational configuration. The right frame displays an Item Specific Help window providing an explanation of the respective function.

8.2.1. Main Setup Menu

Upon entering the uEFI BIOS Setup program, the Main Setup menu is displayed. This screen lists the Main Setup menu sub-screens and provides basic system information. Additionally functions for setting the system time and date are offered.

Table 52: Main Setup Menu Sub-Screens and Functions

Function	Description
BIOS Information	Read only field. Displays information about the system BIOS
Memory Information	Read only field. Displays information about total memory
Firmware Information	Code version and firmware information
System Date	Set System Date
System Time	Set System Time

Figure 45: BIOS Main Menu Screen System Data and Time

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Product Information					
Product Name		mITX-VR1000 V2.0-V1202			
BIOS Version		R0.08 (x64)			
BIOS Build Date		04/23/2019			
CPU Information					
AMD Ryzen Embedded V1202B with Radeon Vega Gfx 2300 Mhz, 2 Core(s), 4 Logical Processor(s)					
Processor ID		810F10h			
Memory Information					
Total Size		8192 MB (DDR4)		→ ←: Select Screen	
Frequency		2400 MHz		↑ ↓: Select Item	
				Enter: Select	
> AMD Firmware Version				+/-: Change Opt.	
				F1: General Help	
System Date		[Mon 09/23/2019]		F2: Previous Values	
System Time		[21:51:51]		F3: Optimized Defaults	
				F4: Save & Exit	
Access Level		Administrator		ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Feature	Option	Description
System Date	[dd/mm/yyyy]	Set the Date. Use Tab to switch between Data elements.
System Time	[hh:mm:ss]	Set the Time. Use Tab to switch between Time elements.

Figure 46: BIOS Main Menu Screen System Data and Time - AMD Firmware Version

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
AMD Firmware Version					
AGESA Version		RavenPI-FP5-AM4 1.1.0.8			
PSP BootLoader Version		0.8.0.5C			
PSP SecureOS Version		0.8.0.5C			
ABL Version		18120420			
APCB Version		0029			
APOB Version		0012			
Ucode Patch Version		810100B			

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
SMU FW Version		0.30.79.0			
DXIO FW Version		001E.011D			
MP2 FW Version		1.0.24		→ ←: Select Screen	
				↑ ↓: Select Item	
XHCI FW Version		FF.FF.FF.FF		Enter: Select	
VBIOS FW Version		0113		+/-: Change Opt.	
GOP Driver Version		0		F1: General Help	
				F2: Previous Values	
EC FW Version		0CFF		F3: Optimized Defaults	
USB PD Section 1 FW Version		00FF		F4: Save & Exit	
USB PD Section 2 FW Version		00FF		ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

8.2.2. Advanced Setup Menu

The Advanced setup menu provides sub-screens and functions for advanced configurations. The following sub-screen functions are included in the menu:

- LAN Configuration
- Display Configuration
- CPU Chipset Configuration
- NVMe Configuration
- SATA Configuration
- USB Configuration
- Trusted Computing
- Network Stack Configuration
- DIO Configuration
- Super IO Configuration
- H/W Monitor
- Tls Auth Configuration

NOTICE

Setting items on this screen to incorrect values may cause the system to malfunction.

Figure 47: BIOS Advanced Menu

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Onboard LAN1 Controller		[Enabled]			
Onboard LAN2 Controller		[Enabled]			
Onboard LAN3 Controller		[Enabled]			
> Display Configuration					
> CPU Chipset Configuration					
> NVMe Configuration					
> SATA Configuration				→←: Select Screen	
> USB Configuration				↑ ↓: Select Item	
> Trusted Computing				Enter: Select	
> Network Stack Configuration				+/-: Change Opt.	
> DIO Configuration				F1: General Help	
> Super IO Configuration				F2: Previous Values	
> H/W Monitor				F3: Optimized Defaults	
				F4: Save & Exit	
> Tls Auth Configuration				ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Feature	Option	Description
Onboard LAN1 Controller	[Disabled], [Enabled]	Select whether to enable or disable Onboard LAN1 Controller. I211-AT-1
Onboard LAN2 Controller	[Disabled], [Enabled]	Select whether to enable or disable Onboard LAN2 Controller. I211-AT-2
Onboard LAN3 Controller	[Disabled], [Enabled]	Select whether to enable or disable Onboard LAN3 Controller. I210-AT

Figure 48: BIOS Advanced Menu - Display Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Display Configuration					
Integrated Graphics Controller		[Enabled]		→ ←: Select Screen	
Primary Video Adaptor		[Int Graphics (IGD)]		↑ ↓: Select Item	
UWA Frame Buffer Size		[512M]		Enter: Select	
				+/-: Change Opt.	
Active LVDS		[Disabled]		F1: General Help	
LVDS Panel Type*		[1366x768 1CH]		F2: Previous Values	
LVDS Panel Color Depth*		[18Bit]		F3: Optimized Defaults	
PWM Backlight Control*		[By External]		F4: Save & Exit	
LVDS Backlight Control - PWM*		127		ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

* These items appear only when enabling Active LVDS.

Feature	Option	Description
Integrated Graphics Controller	[Disabled], [Enabled]	Select whether to enable or disable Integrated Graphics controller
Primary Video Adaptor	[Int Graphics (IGD)], [Ext Graphics (PEG)]	Select which graphic controller to be used as the primary display device.
UWA Frame Buffer Size	[64M], [128M], [256M], [384M], [512M], [1G], [2G], [3G]	Configure the memory size for internal graphic.
Active LVDS	[Disabled], [Enabled]	Select the Active LVDS Configuration. [Disabled]: VBIOS does not enable LVDS. [Enabled]: VBIOS will enable LVDS.
LVDS Panel Type	[800x600 1CH], [1024x768 1CH], [1280x1024 2CH], [1366x768 1CH], [1366x768 2CH], [1600x1200 2CH], [1920x1080 2CH]	Select the appropriate setup item for LVDS panel type.
LVDS Panel Color Depth	[18Bit], [24Bit]	Select the appropriate setup item for LVDS panel color depth.
PWM Backlight Control	[By External], [By Internal]	Select the appropriate setup item for PWM Backlight Control. [By External]: Control by external HW circuit. [By Internal]: Control by LBKLT_CTL on the AMD Chipset.

Figure 49: BIOS Advanced Menu - CPU Chipset Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
CPU Chipset Configuration					
SVM Mode		[Enabled]		→←: Select Screen	
NX Mode		[Enabled]		↑ ↓: Select Item	
IOMMU		[Enabled]		Enter: Select	
				+/-: Change Opt.	
				F1: General Help	
				F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Feature	Option	Description
SVM Mode	[Disabled], [Enabled]	Select whether to enable or disable CPU Virtualization.
NX Mode	[Disabled], [Enabled]	Select whether to enable or disable No-execute page protection function.
IOMMU	[Disabled], [Enabled]	Select whether to enable or disable IOMMU.

Figure 50: BIOS Advanced Menu - NVMe Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
NVMe Configuration					
No NVMe Device Found				→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Figure 51: BIOS Advanced Menu - SATA Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
SATA Configuration					
SATA Controller		[Enabled]		→←: Select Screen	
				↑ ↓: Select Item	
Serial ATA Port-0		Not Present		Enter: Select	
Serial ATA Port-1		Not Present		+/-: Change Opt.	
				F1: General Help	
				F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Feature	Option	Description
SATA Controller	[Enabled], [Disabled]	Select whether to disable or enable OnChip SATA Controller.

Figure 52: BIOS Advanced Menu - USB Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
USB Configuration					
USB Devices:				→ ←: Select Screen	
1 Keyboard, 1 Hub				↑ ↓: Select Item	
				Enter: Select	
Legacy USB Support		[Enabled]		+/-: Change Opt.	
XHCI Hand-off		[Enabled]		F1: General Help	
USB Mass Storage Driver Support		[Enabled]		F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Feature	Option	Description
Legacy USB Support	[Enabled], [Disabled], [Auto]	Select whether to enable or disable Legacy USB support. AUTO option disables legacy support if no USB devices are connected.
XHCI Hand-off	[Enabled], [Disabled]	Select whether to enable or disable XHCI Hand-off function. This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	[Disabled], [Enabled]	Select whether to enable or disable USB Mass Storage Driver Support.

Figure 53: BIOS Advanced Menu - Trusted Computing

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
TPM20 Device Found					
Firmware Version:		5.62			
Vendor:		IFX			
Security Device Support		[Enable]			
Active PCR banks*		SHA-1, SHA256			
Available PCR banks*		SHA-1, SHA256			
SHA1 PCR Bank*		[Enabled]			
SHA256 PCR Bank*		[Enabled]		→←: Select Screen	
				↑ ↓: Select Item	
Pending operation*		[None]		Enter: Select	
Platform Hierarchy*		[Enabled]		+/-: Change Opt.	
Storage Hierarchy*		[Enabled]		F1: General Help	
Endorsement Hierarchy*		[Enabled]		F2: Previous Values	
TPM2.0 UEFI Spec Version*		[TCG_2]		F3: Optimized Defaults	
Physical Presence Spec Version*		[1.3]		F4: Save & Exit	
TPM 20 Interface Type*		[TIS]		ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

* These items appear only when enabling Security Device Support.

Feature	Option	Description
Security Device Support	[Disable], [Enable]	Select whether to enable or disable BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.
SHA-1 PCR Bank	[Disabled], [Enabled]	Select whether to enable or disable SHA-1 PCR Bank.
SHA256 PCR Bank	[Disabled], [Enabled]	Select whether to enable or disable SHA256 PCR Bank.
Pending operation	[None], [TPM Clear]	Schedule an Operation for the Security Device. NOTE: Your Computer will reboot during restart in order to change State of Security Device.
Platform Hierarchy	[Disabled], [Enabled]	Select whether to enable or disable Platform Hierarchy.
Storage Hierarchy	[Disabled], [Enabled]	Select whether to enable or disable Storage Hierarchy.
Endorsement Hierarchy	[Disabled], [Enabled]	Select whether to enable or disable Endorsement Hierarchy.
TPM2.0 UEFI Spec Version	[TCG_1_2], [TCG_2]	Select the TCG2 Spec Version Support. [TCG_1_2]: the Compatible mode for Win8 / Win10. [TCG_2]: Support new TCG2 protocol and event format for Win10 or later.
Physical Presence Spec Version	[1.2], [1.3]	Select to Tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.

Figure 54: BIOS Advanced Menu - Network Stack Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Network Stack Configuration					
Load Intel I211 / I210 UNDI		[Disabled]		→ ←: Select Screen	
				↑ ↓: Select Item	
LAN Boot I211-AT-1		[Disabled]		Enter: Select	
LAN Boot I211-AT-2		[Disabled]		+/-: Change Opt.	
LAN Boot I210-AT		[Disabled]		F1: General Help	
				F2: Previous Values	
Ipv4 PXE Support		[Enabled]		F3: Optimized Defaults	
Ipv6 PXE Support		[Disabled]		F4: Save & Exit	
				ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Feature	Option	Description
Load Intel I211 / I210 UNDI	[Disabled], [Enabled]	Select whether to enable or disable load onboard UNDI (Universal Network Driver Interface) for Intel I211 / I210.
LAN Boot I211-AT-1	[Disabled], [Load PXE]	Select whether to enable or disable load onboard PXE (Preboot Execution Environment) or uEFI-SNP (Simple Network Protocol). Intel I211-AT-1.
LAN Boot I211-AT-2	[Disabled], [Load PXE]	Select whether to enable or disable load onboard PXE (Preboot Execution Environment) or uEFI-SNP (Simple Network Protocol). Intel I211-AT-2.
LAN Boot I210-AT	[Disabled], [Load PXE]	Select whether to enable or disable load onboard PXE (Preboot Execution Environment) or uEFI-SNP (Simple Network Protocol). Intel I210-AT.
Ipv4 PXE Support	[Disabled], [Enabled]	Select whether to enable or disable IPv4 PXE Boot Support. If disabled, IPv4 PXE boot support will not be available.
Ipv6 PXE Support	[Disabled], [Enabled]	Select whether to enable or disable IPv6 PXE Boot Support. If disabled, IPv6 PXE boot support will not be available.

Figure 55: BIOS Advanced Menu - DIO Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
DIO Configuration					
User Configuration		[Disabled]			
DIO_0*		[Output High]			
DIO_1*		[Output High]			
DIO_2*		[Output High]			
DIO_3*		[Output High]			
DIO_4*		[Output High]			
DIO_5*		[Output High]			
DIO_6*		[Output High]			
DIO_7*		[Output High]			
DIO_0 Value		1		→←: Select Screen ↑ ↓: Select Item	
DIO_1 Value		1		Enter: Select	
DIO_2 Value		1		+/-: Change Opt.	
DIO_3 Value		1		F1: General Help	
DIO_4 Value		1		F2: Previous Values	
DIO_5 Value		1		F3: Optimized Defaults	
DIO_6 Value		1		F4: Save & Exit	
DIO_7 Value		1		ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

* These items appear only when enabling User Configuration.

Feature	Option	Description
User Configuration	[Enabled], [Disabled]	Select whether to allow users to set the DIO pin output value.
DIO_0..7	[Output Low], [Output High], [Input]	Set the DIO pin output value.

Figure 56: BIOS Advanced Menu - Super IO Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Super IO Configuration					
Serial Port UART Protection		[No Protection]			
				→ ←: Select Screen	
> Serial Port 1 Configuration				↑ ↓: Select Item	
> Serial Port 2 Configuration				Enter: Select	
> Serial Port 3 Configuration				+/-: Change Opt.	
> Serial Port 4 Configuration				F1: General Help	
> Serial Port 5 Configuration				F2: Previous Values	
> Serial Port 6 Configuration				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Feature	Option	Description
Serial Port UART Protection	[No Protection], [Keep Device On]	Set Super IO Serial Port into Device D3 or not. [No Protection]: UART device have be entry D3 for OS control. [Keep Device On]: Protection UART device not entry D3 state.

Figure 57: BIOS Advanced Menu - Super IO Configuration - Serial Port 1 Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Super Port 1 Configuration					
				→ ←: Select Screen	
Serial Port		[Enabled]		↑ ↓: Select Item	
Device Settings		IO=3F8h; IRQ=4;		Enter: Select	
Change Setting		[Auto]		+/-: Change Opt.	
Serial Port 1 Type		[RS232]		F1: General Help	
RS485 Deplux Mode*		[Half Duplex]		F2: Previous Values	
RS485 Auto Flow Control*		[Disabled]		F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

* These items appear only when selecting RS485 for the Serial Port 1 Type.

Feature	Option	Description
Serial Port	[Disabled], [Enabled]	Select whether to enable or disable Serial Port (COM).
Change Settings	[Auto], [IO=3F8h; IRQ=4;], [IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10,	Select an optional setting for Super IO device.

Feature	Option	Description
	11, 12;], [IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;]	
Serial Port 1 Type	[RS232], [RS422], [RS485]	Select an appropriate type for Serial Port 1.
RS485 Duplex Mode	[Half Duplex], [Full Duplex]	Select an appropriate RS485 Duplex Mode.
RS485 Auto Flow Control	[Disabled], [Enabled]	Select whether to enable or disable RS485 Auto Flow Control.

Figure 58: BIOS Advanced Menu - Super IO Configuration - Serial Port 2 Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Super Port 2 Configuration					
Serial Port		[Enabled]		→ ←: Select Screen	
Device Settings		IO=2F8h; IRQ=3;		↑ ↓: Select Item	
				Enter: Select	
Change Setting		[Auto]		+/-: Change Opt.	
Serial Port 2 Type		[RS232]		F1: General Help	
RS485 Deplux Mode*		[Half Duplex]		F2: Previous Values	
RS485 Auto Flow Control*		[Disabled]		F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

* These items appear only when selecting RS485 for the Serial Port 2 Type.

Feature	Option	Description
Serial Port	[Disabled], [Enabled]	Select whether to enable or disable Serial Port (COM).
Change Settings	[Auto], [IO=2F8h; IRQ=3;], [IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;]	Select an optional setting for Super IO device.
Serial Port 2 Type	[RS232], [RS422], [RS485]	Select an appropriate type for Serial Port 2.
RS485 Duplex Mode	[Half Duplex], [Full	Select an appropriate RS485 Duplex Mode.

Feature	Option	Description
	Duplex]	
RS485 Auto Flow Control	[Disabled], [Enabled]	Select whether to enable or disable RS485 Auto Flow Control.

Figure 59: BIOS Advanced Menu - Super IO Configuration - Serial Port 3 Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Super Port 3 Configuration					
Serial Port		[Enabled]		→←: Select Screen	
Device Settings		IO=3E8h; IRQ=5;		↑ ↓: Select Item	
				Enter: Select	
Change Setting		[Auto]		+/-: Change Opt.	
				F1: General Help	
				F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Feature	Option	Description
Serial Port	[Disabled], [Enabled]	Select whether to enable or disable Serial Port (COM).
Change Settings	[Auto], [IO=3E8h; IRQ=7;], [IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2F0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;]	Select an optional setting for Super IO device.

Figure 60: BIOS Advanced Menu - Super IO Configuration - Serial Port 4 Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Super Port 4 Configuration					
Serial Port		[Enabled]		→←: Select Screen	
Device Settings		IO=2E8h; IRQ=5;		↑ ↓: Select Item	
				Enter: Select	
Change Setting		[Auto]		+/-: Change Opt.	
				F1: General Help	

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
				F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Feature	Option	Description
Serial Port	[Disabled], [Enabled]	Select whether to enable or disable Serial Port (COM).
Change Settings	[Auto], [IO=2E8h; IRQ=7;], [IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2F0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;]	Select an optional setting for Super IO device.

Figure 61: BIOS Advanced Menu - Super IO Configuration - Serial Port 5 Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Super Port 5 Configuration					
Serial Port		[Enabled]		→←: Select Screen	
Device Settings		IO=2F0h; IRQ=5;		↑ ↓: Select Item	
				Enter: Select	
Change Setting		[Auto]		+/-: Change Opt.	
				F1: General Help	
				F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Feature	Option	Description
Serial Port	[Disabled], [Enabled]	Select whether to enable or disable Serial Port (COM).
Change Settings	[Auto], [IO=2F0h; IRQ=7;], [IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2F0h; IRQ=3, 4, 5, 6, 7, 9, 10,	Select an optional setting for Super IO device.

Feature	Option	Description
	11, 12;], [IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;]	

Figure 62: BIOS Advanced Menu - Super IO Configuration - Serial Port 6 Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Super Port 6 Configuration					
Serial Port		[Enabled]		→←: Select Screen	
Device Settings		IO=2E0h; IRQ=5;		↑ ↓: Select Item	
				Enter: Select	
Change Setting		[Auto]		+/-: Change Opt.	
				F1: General Help	
				F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Feature	Option	Description
Serial Port	[Disabled], [Enabled]	Select whether to enable or disable Serial Port (COM).
Change Settings	[Auto], [IO=2E0h; IRQ=7;], [IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2F0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;]	Select an optional setting for Super IO device.

Figure 63: BIOS Advanced Menu - H/W Monitor

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
PC Health Status					
> Smart FAN Configuration					
CPU Temperature - Thermistor		: +67 C			
System Temperature		: +47 C			
CPU Fan Speed		: N/A		→ ←: Select Screen	
SYS Fan Speed		: N/A		↑ ↓: Select Item	
				Enter: Select	
+VCORE		: +1.117 V		+/-: Change Opt.	
+12V		: +8.316 V		F1: General Help	
+5V		: +5.106 V		F2: Previous Values	
+VMEM		: +1.237 V		F3: Optimized Defaults	
+3.3V		: +3.344 V		F4: Save & Exit	
+VRTC		: +3.280 V		ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Figure 64: BIOS Advanced Menu - H/W Monitor - Smart FAN Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Smart FAN Configuration					
CPU FAN Setting		[Manual]			
Manual Duty*		255			
System FAN Setting		[Manual]		→ ←: Select Screen	
1st Boundary Temperature**		30		↑ ↓: Select Item	
1st FAN Speed**		50		Enter: Select	
2nd Boundary Temperature**		40		+/-: Change Opt.	
2nd FAN Speed**		100		F1: General Help	
3rd Boundary Temperature**		50		F2: Previous Values	
3rd FAN Speed**		150		F3: Optimized Defaults	
4th Boundary Temperature**		60		F4: Save & Exit	
4th FAN Speed**		200		ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

* This item appears only when selecting Manual for the CPU / System FAN Setting.

** These items appear only when selecting Smart for the CPU / System FAN Setting.

Feature	Option	Description
CPU FAN Setting	[Manual], [Smart]	Select CPU smart FAN configuration.
System FAN Setting	[Manual], [Smart]	Select system smart FAN configuration.

Figure 65: BIOS Advanced Menu - Tls Auth Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
> Server CA Configuration					
> Client Cert Configuration				→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Figure 66: BIOS Advanced Menu - Tls Auth Configuration - Server CA Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
> Enroll Cert					
> Delete Cert				→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Figure 67: BIOS Advanced Menu - Tls Auth Configuration - Server CA Configuration - Enroll Cert

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
> Enroll Cert Using File					
Cert GUID				→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help	
> Commit Changes and Exit					
> Discard Changes and Exit					

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
				F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Feature	Option	Description
Cert GUID	[11111111-2222-3333-4444-1234567890ab]	Input digit character in 11111111-2222-3333-4444-1234567890ab format.

8.2.3. Power Setup Menu

The Power setup menu provides functions and a sub-screen for power configurations. The following sub-screen function is included in the menu:

- WatchDog Timer Configuration

Figure 68: BIOS Power Setup Menu

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Power Configuration					
ACPI Sleep State		[S3 (Suspend to RAM)]			
Restore AC Power Loss		[Power Off]			
Power Saving Mode		[Disabled]			
				→ ←: Select Screen	
Resume Event Control				↑ ↓: Select Item	
ResumeLan I211-AT-1		[Disabled]		Enter: Select	
ResumeLan I211-AT-2		[Disabled]		+/-: Change Opt.	
ResumeLan I210-AT		[Disabled]		F1: General Help	
Resume By PCI-E Device		[Disabled]		F2: Previous Values	
Resume By Ring Device		[Disabled]		F3: Optimized Defaults	
Resume By RTC Alarm		[Disabled]		F4: Save & Exit	
> WatchDog Timer Configuration				ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Feature	Option	Description
ACPI Sleep State	[Suspend Disabled], [S3 (Suspend to RAM)]	Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.
Restore AC Power Loss	[Power Off], [Power On], [Last State]	Select AC power state when power is re-applied after a power failure. Select [Power Off] if you want the system to remain off after power restored. Select [Power On] if you use a power strip to turn the system on.
Power Saving Mode	[Disabled], [EUP Enabled]	Configure the Power Saving Mode configuration.
ResumeLan I211-AT-1	[Disabled], [OS-Driver], [FW-MagicPacket]	Select whether to enable Wake from LAN Device Intel I211-AT-1.
ResumeLan I211-AT-2	[Disabled], [OS-Driver], [FW-MagicPacket]	Select whether to enable Wake from LAN Device Intel I211-AT-2.
ResumeLan I210-AT	[Disabled], [OS-Driver], [FW-MagicPacket]	Select whether to enable Wake from LAN Device Intel I210-AT.
Resume By PCI-E Device	[Disabled], [Enabled]	Select whether to enable Wake from PCI-E Device.

Feature	Option	Description
Resume By Ring Device	[Disabled], [Enabled]	Select whether to enable Wake from Ring Device.
Resume By RTC Alarm	[Disabled], [Enabled]	Select whether to enable or disable Wake Up on Alarm, to turn on your system on a special day of the month.

Figure 69: BIOS Power Setup Menu - WatchDog Timer Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
WatchDog Timer Configuration					
WDT Function		[Disabled]		→ ←: Select Screen	
WDT Count Mode*		[Minute]		↑ ↓: Select Item	
WDT Timer*		3		Enter: Select	
				+/-: Change Opt.	
				F1: General Help	
				F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

* These items appear only when enbling WDT Function.

Feature	Option	Description
WDT Function	[Disabled], [Enabled]	Select whether to enable or disable WatchDog Timer function.
WDT Count Mode	[Second], [Minute]	Select the WDT Count Mode.

8.2.4. Boot Setup Menu

The boot setup menu lists the for boot device priority order, that is generated dynamically.

Figure 70: BIOS Boot Setup Menu

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Boot Configuration					
Full Screen LOGO Display		[Disabled]			
Setup Prompt Timeout		1			
Bootup NumLock State		[On]			
				→ ←: Select Screen	
CSM Support		[Enabled]		↑ ↓: Select Item	
Boot Option Filter		[UEFI and Legacy]		Enter: Select	
Load Built-in Shell*		[Enabled]		+/-: Change Opt.	
File System Drivers*		[Disabled]		F1: General Help	
				F2: Previous Values	
Boot Option Priorities				F3: Optimized Defaults	
Boot Option #1		[UEFI: Built-in EFI Shell]		F4: Save & Exit	
				ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

* These items appear only when selecting 'UEFI and Legacy' or 'UEFI only'.

Feature	Option	Description
Full Screen LOGO Display	[Disabled], [Enabled]	Select whether to enable or disable to display logo screen.
Bootup NumLock State	[On], [Off]	This field indicates the state of the NumLock feature of the keyboard after Startup. [On]: The keys on the keypad will act as numeric keys. [Off]: The keys on the keypad will act as cursor keys.
CSM Support	[Enabled], [Disabled]	Select whether to enable or disable CSM support.
Boot Option Filter	[UEFI and Legacy], [Legacy only], [UEFI only]	This option controls Legacy / UEFI ROMs priority.
Load Built-in Shell	[Enabled], [Disabled]	It controls installation of the boot option for a built-in shell.
File System Drivers	[Enabled], [Disabled]	Free Software UEFI File System Drivers, such as a read-only NTFS or exFAT EFI drivers, courtesy of the GRUB project.
Boot Option #1 / #2 / #3	[UEFI: Built-in EFI Shell], [Disabled]	Select Boot option.

8.2.5. Security Setup Menu

The Security setup menu provides information about the passwords and functions for specifying the security settings. The passwords are case-sensitive. The mITX-VR1000 V2.0 provides no factory-set passwords.

NOTICE

If there is already a password installed, the system asks for this first. To clear a password, simply enter nothing and acknowledge by pressing <RETURN>. To set a password, enter it twice and acknowledge by pressing <RETURN>.

Figure 71: BIOS Security Setup Menu

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Password Description If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights The password length must be in the following range:					
Minimum Length		3		→ ←: Select Screen	
Maximum length		20		↑ ↓: Select Item	
				Enter: Select	
Administrator Password				+/-: Change Opt.	
User Password				F1: General Help	
				F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Feature	Description
Administrator Password	Set administrator password
User Password	Set user password

If only the administrator's password is set, then only access to setup is limited. The password is only entered when entering setup.

If only the user's password is set, then the password is a power on password and must be entered to boot or enter setup. Within the setup menu the user has administrator rights.

Password length requirements are maximum 20 characters and minimum 3 characters.

8.2.5.1. Remember the password

It is highly recommended to keep a record of all passwords in a safe place. Forgotten passwords results in being locked out of the system.

If the system cannot be booted because the User Password or the Supervisor Password are not know, contact Kontron Support for further assistance.

HDD security passwords cannot be cleared using the above method.

8.2.6. Save & Exit Setup Menu

The exit setup menu provides functions for handling changes made to the UEFI BIOS settings and the exiting of the setup program.

Figure 72: BIOS Save & Exit Setup Menu

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Save Changes and Reset Discard Changes and Reset					
Save Options Save Changes Discard Changes Restore Defaults				→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
Version 2.20.1271. Copyright (C) 2019, American Megatrends, Inc.					

Feature	Description
Save Changes and Exit	Exit system setup after saving the changes. Once you are finished making your selections, choose this option from the Exit menu to ensure the values you selected are saved to the CMOS RAM. The CMOS RAM is sustained by an onboard backup battery and stays on even when the PC is turned off. When you select this option, a confirmation window appears. Select [Yes] to save changes and exit.
Discard Changes and Exit	Exit system setup without saving any changes. Select this option only if you do not want to save the changes that you made to the Setup program. If you made changes to fields other than system date, system time, and password, the BIOS asks for a confirmation before exiting.
Save Changes	Save changes done so far to any of the setup values. This option allows you to save the selections you made. After selecting this option, a confirmation appears. Select [Yes] to save any changes.
Discard Changes	Discards changes done so far to any of the setup values. This option allows you to discard the selections you made and restore the previously saved values. After selecting this option, a confirmation appears. Select [Yes] to discard any changes and load the previously saved values.
Restore Defaults	Restore Default values for all the setup values. This option allows you to load optimal default values for each of the parameters on the Setup menus, which will provide the best performance settings for your system. The F9 key can be used for this operation.

Appendix A: List of Acronyms

The following table does not contain the complete acronyms used in signal names, signal type definitions or similar. A description of the signals is included in the I/O Connector and Internal connector chapters within this user guide.

Table 53: List of Acronyms

2D	Two-Dimensional
3D	Three-Dimensional
AT	Advanced Technology
ATX	Advanced Technology eXtended
BGA	Ball Grid Array
BIOS	Basic Input / Output System
BSP	Board Support Package
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DC	Direct Current
DDC	Display Data Channel
DIO	Digital Input / Output
DP	DisplayPort
ECC	Error-Correcting Code
EEE	Electrical and Electronic Equipment
EOS	Electrical OverStress
ESD	ElectroStatic Discharge
GbE	Gigabit Ethernet
HDD	Hard Disk Drive
HDMI	High Definition Multimedia Interface
LAN	Local Area Network
LED	Light Emitting Device
LVDS	Low-Voltage Differential Signaling
ME F/W	Management Engine Firmware
mPCIe	mini Peripheral Component Interconnect express
NGFF	Next Generation Form Factor
PC-AT	Personal Computer - Advanced Technology
PCB	Printed Circuit Board
PSU	Power Supply Unit
PVC	PolyViny Chloride
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read-Only Memory
RTC	Real-Time Clock
SATA	Serial Advanced Technology Attachment
SD	Secure Digital memory card
SDP	Serial Download Protocol
SELV	Safety Extra-Low Voltage
SIM	Subscriber Identity Module
SMBus	System Management Bus
SoC	System on Chip
SO-DIMM	Small Outline Dual In-line Memory Module
SPD	Serial Presence Detect
SPI	Serial Peripheral Interface
TDP	Thermal Design Power
TPM	Trusted Platform Module
UEFI	Unified Extensible Firmware Interface
USB	Universal Serial Bus
UTP	Update Transfer Protocol
VGA	Video Graphics Array
WDT	WatchDog Timer
WEEE	Waste Electrical and Electronic Equipment

About Kontron

Kontron is a global leader in Embedded Computing Technology (ECT). As a part of technology group S&T, Kontron offers a combined portfolio of secure hardware, middleware and services for Internet of Things (IoT) and Industry 4.0 applications. With its standard products and tailor-made solutions based on highly reliable state-of-the-art embedded technologies, Kontron provides secure and innovative applications for a variety of industries. As a result, customers benefit from accelerated time-to-market, reduced total cost of ownership, product longevity and the best fully integrated applications overall. For more information, please visit: www.kontron.com

Global Headquarters

Kontron S&T AG

Lise-Meitner-Str. 3-5
86156 Augsburg
Germany
Tel.: + 49 821 4086-0
Fax: + 49 821 4086-111
info@kontron.com