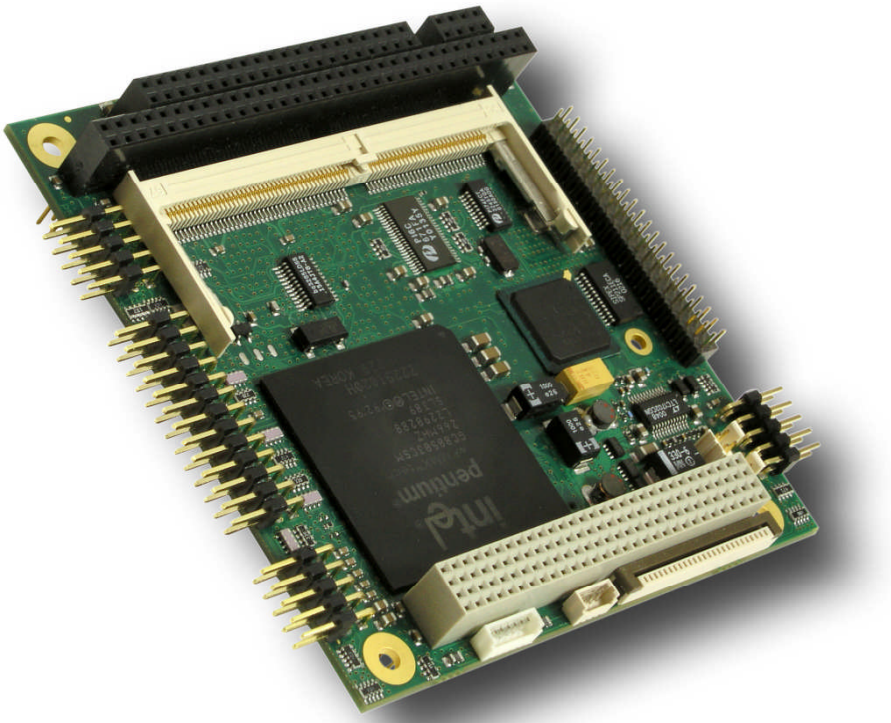


MOPSlcd6

MOPS/686+

User's Guide

Document Revision 4.3

kontron

... always a Jump ahead!

CONTENTS

1. USER INFORMATION

1.1 *About This Manual*

This document provides information about products from Kontron Embedded Modules AG and/or its subsidiaries. No warranty of suitability, purpose, or fitness is implied. While every attempt has been made to ensure that the information in this document is accurate, the information contained within is supplied "as-is" and is subject to change without notice.

For the circuits, descriptions and tables indicated, Kontron assumes no responsibility as far as patents or other rights of third parties are concerned.

1.2 *Copyright Notice*

JUMP*tec* Industrielle Computertechnik AG and Kontron Embedded Computers AG merged in July 2002. JUMP*tec* is now known as Kontron Embedded Modules GmbH. Products labeled and sold under the Kontron Embedded Modules name (formerly JUMP*tec*) are now considered Kontron products for all practical purposes, including warranty and support.

1.3 *Trademarks*

The following lists the trademarks of components used in this board.

- IBM, XT, AT, PS/2 and Personal System/2 are trademarks of International Business Machines Corp.
- Microsoft is a registered trademark of Microsoft Corp.
- Intel is a registered trademark of Intel Corp.
- All other products and trademarks mentioned in this manual are trademarks of their respective owners.

1.4 *Standards*

Kontron Embedded Modules is certified to ISO 9000 standards.

1.5 *Warranty*

This Kontron Embedded Modules product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, Kontron Embedded Modules will at its discretion decide to repair or replace defective products.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.

Kontron Embedded Modules will not be responsible for any defects or damages to other products not supplied by Kontron Embedded Modules that are caused by a faulty Kontron Embedded Modules product.

1.6 *Technical Support*

Technicians and engineers from Kontron Embedded Modules and/or its subsidiaries and official distributors are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Before contacting Kontron Embedded Modules technical support, please contact your local representative or consult our Web site for the latest product documentation, utilities, and drivers. If the information does not help to solve the problem, contact us by telephone.

Asia	Europe	North/South America
Kontron Embedded Technology (Asia Pacific)	Kontron Embedded Modules GmbH	Kontron America
Far East Science Park, 2nd Floor No. 2, Lane 50, Nan Kang Road Section 3, Nan Kang District Taipei, Taiwan	Brunnwiesenstr. 16 94469 Deggendorf – Germany	6260 Sequence Drive San Diego, CA 92121-4371
Tel: +886-2-2782-0201	Tel: +49 (0) 991-37024-0	Tel: 888-294-4558
Fax: +886-2-2782-7486	Fax: +49 (0) 991-37024-104	Fax: (858) 677-0898

2. INTRODUCTION

2.1 *MOPSlcd6 and MOPS/686+*

MOPSlcd6 and MOPS/686+ are both based on the same PCB layout. The only difference between both boards is the onboard graphic controller equipped on every MOPSlcd6. All MOPS/686+ boards come without a graphic controller. Whenever the features of the products MOPSlcd6 and MOPS/686+ are identical this document will refer to the product MOPSlcd6.

The MOPSlcd6 can be equipped with two processor versions (166MHz or 266MHz). The version with 166 MHz Intel® Pentium® MMX™ processor (fanless) offers high reliability and performance at low power consumption of typical 9 Watt—no active cooling required. The MOPSlcd6 also is available with 266 MHz processors. For this faster version, a fan for active cooling is mounted.

One SO-DIMM socket on the topside of the board enables the MOPSlcd6 to be equipped with up to 256 MB of SDRAM.

There also is a DIMM socket on the bottom side of the board, which is used as a JIPA (Intelligent Panel Adaption) interface to connect LCD flat panels. The onboard PCI Asiliant Graphic-Controller supports mono-LCD, TFT and STN displays with resolutions up to SXGA (1280x1024). This feature is not available on the MOPS/686+.

Every MOPSlcd6 comes with PC/104 standard interface (ISA signals). The PC/104-Plus interface (PCI signals) is optional and enables applications with high I/O performance requirements.

The MOPSlcd6 is a highly integrated CPU board that includes many standard interfaces, a watchdog timer and a real-time clock. It integrates the complete functionality of a Pentium motherboard and includes the following features:

- CPU
- System BIOS
- Supports up to 256MB SDRAM
- Keyboard controller
- Real-time clock
- PCI-SVGA with LCD interface (only MOPSlcd6)

Additional peripheral functions include:

- COM1 and COM2 (Both RS-232)
- LPT1 (SPP/EPP/ECP modes)
- USB interface
- Floppy interface
- EIDE hard-disk interface (Ultra33 DMA mode)
- Watchdog time (WDT)
- Ethernet controller

Attention:

This manual is describing the MOPSlcd6 new hardware revision 4. This revision is not fully compatible with older hardware revisions of this product. For Hardware Revision 4 boards, the Intel Ethernet controller 82551ER is used instead of the 82559ER. Also, a new revision of the south bridge that has an integrated watchdog timer is now on the board. In addition, smaller changes to the circuitry have been made. Parts of the manual in which this new hardware revision differs from older versions are marked in blue.

2.2 *The MOPS Family*

MOPS (**M**inimized **O**pen **P**C **S**ystem) PC/104 products represent the "Proven PC Platform for Instant Solutions." Each MOPS module is characterized by the same pinout for the keyboard, COM1 and COM2, 44-pin IDE, LPT, and 1st LAN. These homogeneous features facilitate easy upgrades within the Kontron Embedded Modules GmbH MOPS PC/104 product family.

Whenever a LCD panel is required, MOPS products with onboard graphics controllers serve as the right choice. Display connections are simplified when using these units, which come with a JUMPtec Intelligent LVDS Interface (JILI) and a JUMPtec Intelligent Panel Adapter (JIPA) interface. The two interfaces can recognize which display is connected and then independently set all video parameters. These interfaces are not available on all MOPS products.

All MOPS-PC/104 are plug-and-work enabled to further reduce time-to-market.

As part of the standard features package, all MOPS PC/104 modules come with a JUMPtec Intelligent Device Architecture (JIDA) interface, which is integrated into the BIOS of the PC/104 modules. This interface enables hardware independent access to the MOPS-PC/104 features that cannot be accessed via standard APIs. Functions such as watchdog timer, brightness and contrast of LCD backlight and user bytes in the EEPROM can be configured with ease by taking advantage of this standard MOPS PC/104 module feature.

All MOPS PC/104 products can be remote controlled by using JRC software feature. This allows you to change, update, and maintain the MOPS products from a host computer via a serial connection.

2.3 PC/104 an Embedded PC Standard

Over the past decade, PC architecture has become an accepted platform for far more than desktop applications. Dedicated and embedded applications for PCs are beginning to appear everywhere.

By standardizing hardware and software around the broadly supported PC architecture, embedded system designers can substantially reduce development costs, risks, and time-to-market.

For these reasons, companies that embed microcomputers as controllers within their products seek ways to reap the benefits of using the PC architecture. However, the standard form factor of a PC bus (12.4" x 4.8") and its associated card cages and backplanes are too bulky and expensive for most embedded control applications.

The only practical way to embed the PC architecture in space-and power-sensitive applications has been to design a PC chip by chip directly into the product. But this runs counter to growing trend away from "reinventing the wheel." Whenever possible, top management now encourages outsourcing of components and technologies to reduce development costs and accelerate product design cycles.

A need has arisen for a more compact implementation of the PC bus, satisfying the reduced space and power constraints of embedded control applications. PC/104 was developed in response to this need. It offers full architecture, hardware and software compatibility with the PC bus but in ultra-compact (3.6" x 3.8") stackable modules. PC/104 is ideally suited to the unique requirements of embedded control applications.

Although configuration and application possibilities with PC/104 modules are practically limitless, there are two ways to use them in embedded system designs:

- ***Standalone module stacks***
  PC/104 modules are self-stacking. The modules are used like ultra-compact bus boards but without a need for backplanes or card cages. Stacked modules are spaced 0.6 inches apart. (The three-module stack measures 3.6 by 3.8 by 2 inches.) Companies using PC/104 module stacks within their products frequently create one or more of their own application-specific PC/104 modules.

- ***Component-line applications***
  In this configuration, the modules function as highly integrated components, plugged into custom carrier boards that contain application-specific interfaces and logic. The modules' self-stacking bus can be useful to install multiple modules in one location. This facilitates product upgrades or options and allows temporary addition of modules during system debug or test.

3. GETTING STARTED

The easiest way to get the MOPSlcd6 board running is to use a starter kit from Kontron Embedded Modules GmbH. Take the following steps:

1. Turn off the power supply (part of the starter kit).
2. Connect the power supply to the starter kit baseboard (part of the starter kit).
3. Plug a graphics-controller board to the PC/104 bus, the ISA bus slots, the PC/104-Plus bus or the PCI bus slots on the starter kit when using the MOPS/686+. (There are starter kits available with and without PC/104 graphics boards included.)
4. Connect the CRT monitor to the graphics controller board when using the MOPS/686+. When using the MOPSlcd6 connect a CRT monitor to the CRT interface or a LCD panel to the JIPA interface by using the corresponding adapter cable.
5. Plug the MOPSlcd6 to the PC/104 bus stack on the starter kit baseboard.
6. Make all necessary connections from the MOPSlcd6 to the starter kit board. (Cables come with the starter kit). The starter kit board offers various interfaces on standard connectors.
7. Plug a keyboard to the starter kit's keyboard connector.
8. Connect the floppy drive (part of the starter kit) with the data cable (part of the starter kit) to the MOPSlcd6 floppy interface.
9. Connect the power supply to the floppy's power connector.
10. Plug a hard-drive data cable to the MOPSlcd6 hard-disk interface. Attach the hard disk to the connector at the opposite end of the cable.
11. If necessary, connect the power supply to the hard disk's power connector.
12. Make sure all your connections have been made correctly.
13. Turn on the power.
14. Enter the BIOS by pressing the F2 key during boot-up. Make all changes in the BIOS setup. See the BIOS chapter of this manual for details.

4. SPECIFICATIONS

4.1 *Functional Specifications*

- **Processor**

  Two choices:

  - Intel Pentium® with 166 MHz internal clock and 32 kByte write-back cache (fanless)
  - Intel Pentium® with 266 MHz internal clock and 32 kByte write-back cache (fan)

- **Chipset**

  - ALI M1543C B1/M1531 PCI Chipset; extended temperature

- **Power supply**

  - 5V only supply

- **Memory**

  - 32 – 256 MB SDRAM-SODIMM-Module up to 28mm length

- **Ethernet 100BaseT Twisted Pair Intel 82551ER (optional)**

  - according to the common criteria of the embedded technology market segment

- **Two serial ports, (COM1 and COM2)**

  - Standard RS232C serial ports with FIFO
  - 16550 compatible

- **Parallel port (LPT1)**

  - With SPP/ECP/EPP support

- **USB interface**

  - USB host controller integrated in Southbridge
  - Based on OHCI 1.0a specification
  - USB 1.1 compliant
  - Legacy USB-keyboard and USB-mouse support

- **Floppy interface**

- **EIDE hard-disk interface (PCI)**

  - PCI bus master IDE port (up to two IDE Devices)
  - Supports PIO Mode 3,4 IDE & ATAPI CD-ROM and UDMA33
  - Supports Kontron chipDISK

- **Watchdog integrated in chipset**

- **256KB FLASH-BIOS (Phoenix)**

- **Real-time Clock**
  - External Battery-support
- **Keyboard Controller**
- **Onboard Asiliant VGA (only on MOPSlcd6)**
  - 69000 LCD VGA Controller with PCI-Bus interface, including Burst Mode support
  - VGA-CRT and LCD Controller with integral 2 MB Video RAM
  - Resolution up to 1280x1024 on panel and CRT
  - Color depths up to 16 millions of colors
  - Simultaneous display on CRT and panel
  - Drivers for Win3.11, Win95, NT3.51, NT4.0, OS/2....
  - Plug and play panel interfacing on upper SO-DIMM-connector supports almost all LCDs
- **PC/104 and optional PC/104plus extension bus**

4.2 *Mechanical Specifications*

4.2.1. PC/104 Bus Connector (ISA part)

- **One 2 X 32 pin stackthrough and one 2 X 20 pin stackthrough connector**

4.2.2. PC/104-Plus Bus Connector (optional PCI part)

- **PC/104plus: 4 x 30 pin 2mm connector**

The PC/104plus connector does not have a connector shroud. You cannot use a PC/104plus board with a connector shroud on the top of a MOPSlcd6. This mechanical limitation does not reduce the functionality of a MOPSlcd6 board. You can order a module without a connector shroud or place the MOPSlcd6 board at the top of the stack.

4.2.3. Module Dimensions

- **95 x 90 mm (3.7" x 3.5")**

4.2.4. Height

- **23.5 mm max (including PC/104 connector pins)**

4.2.5. Weight

- **135 g (full feature version)**

4.3 *Electrical Specifications*

4.3.1. Supply Voltage

- 5V DC +/- 5%

4.3.2. Supply Voltage Ripple

- 100 mV peak to peak 0 - 20 MHz

4.3.3. Supply Current (Typical, DOS Prompt)

- MOPS/686+ with 166MHz CPU and 32MB SDRAM: 1.13A
- MOPS/686+ with 266MHz CPU and 256MB SDRAM: 1.65A:
- MOPSlcd6 with 166 MHz CPU and 32MB SDRAM: 1.31A
- MOPSlcd6 with 266 MHz CPU and 256MB SDRAM: 1.85A

4.3.4. Supply Current (Maximum)

- With 166MHz CPU: 2.65A + current SDRAM
- With 266MHz CPU: 3.4A + current SDRAM

(calculated theoretical values from all components maximum supply currents)

4.3.5. External RTC Battery

- External RTC battery voltage: 2.4-4.0V
- External RTC battery quiescent current, max 2 uA

4.4 *MTBF*

The following MTBF (Mean Time Between Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and a Bellcore calculation for the remaining parts. The Bellcore calculation used is "Method 1 Case 1". In that particular method the components are assumed to be operating at a 50 % stress level in a 40° C ambient environment and the system is assumed to have not been burned in. Manufacturer's data has been used wherever possible. The manufacturer's data, when used, is specified at 50° C, so in that sense the following results are slightly conservative. The MTBF values shown below are for a 40° C office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, salt water exposure, etc.) will lower the MTBF values.

- **System MTBF (hours) :** TO BE DONE

Notes: Fans usually shipped with Kontron Embedded Modules GmbH products have 50,000-hour typical operating life. The above estimates assume no fan, but a passive heat sinking arrangement.
Estimated RTC battery life (as opposed to battery failures) is not accounted for in the above figures and need to be considered for separately. Battery life depends on both temperature and operating conditions. When the Kontron unit has external power; the only battery drain is from leakage paths.

4.5 *Environmental Specifications*

4.5.1. Temperature

- **Operating: 0 to +60 C (*) (with appropriate airflow.)**
- **Nonoperating: -10 to +85 °C (noncondensing)**

The Intel® Pentium® MMX™ processor on 0.25 Micron is specified for proper operation when case temperature is within the specified range of 0°C to +95°C. The chipset M1531/M1543C on the backside is specified for extended temperature range 0°C to +85°C.

4.5.2. Humidity

- **Operating: 10% to 90% (noncondensing)**
- **Nonoperating: 5% to 95% (noncondensing)**

Note: (*) The maximum operating temperature is the maximum measurable temperature on any spot on the module's surface. You must maintain the temperature according to the above specification.

5. CPU AND CHIPSET

5.1 CPU

The MOPSlcd6 comes with a 166 MHz or 266MHz Intel® low-power, embedded Pentium® processor with MMX™ technology. It is a 32bit CPU with 64bit data bus and has separate 16 KByte code and data caches. The super scalar architecture has enhanced pipelines, two pipelined integer units, pipelined MMX technology, and pipelined floating point unit.

The 166MHz CPU doesn't need active cooling, while the 266MHz version is equipped with a fan.

5.2 Chipset

The MOPSlcd6 Board uses the ALI Aladdin IVPlus chipset, which provides the following features:

5.2.1. North Bridge M1531

- Supports SDRAM modules
- Fully synchronous 33Mhz 3.3V/5V tolerance PCI interface
- Enhanced power management

5.2.2. South Bridge M1543C B1

- PCI 3.3V/5V tolerance interface
- Buffers control
- Provides steerable PCI interrupts for PCI device Plug-and-Play
- Enhanced UDMA controller
- Interrupt controller
- Counters/timers
- Distributed DMA supported
- Serialized IRQ supported
- Plug-and-Play support
- Built-in keyboard controller

- Supports positive/subtractive decode for ISA device
- PMU features
- Built-in PCI IDE controller
- Built-in Watchdog
- USB interface
- Super I/O interface

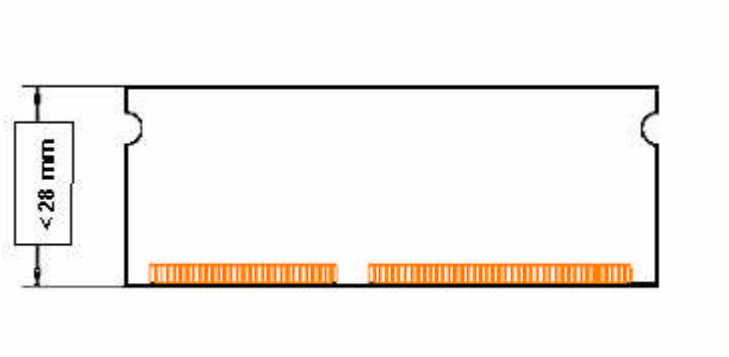
5.3 *CPU and Chipset Configuration*

See the Advanced Chipset Control Submenu section of the Appendix B: BIOS chapter for information on possible settings.

6. SYSTEM MEMORY

The MOPSlcd6 uses only small outline Dual Inline Memory Modules (SO-DIMMs). One socket is available for 3.3 Volt (power level) unbuffered Synchronous Dynamic Random Access Memory (SDRAM). SDRAM modules from 32MB up to 256MB can be used and have to be plugged into SDRAM SO-DIMM socket X4.

The SDRAM module's size is limited to 28mm length because otherwise it will collide with the fan of the processor on the 266MHz board versions. See the drawing below.



To find the location of the SDRAM socket X4 on the MOPSlcd6 board, please see the Appendix E: Connector Layout chapter.

7. ISA AND PCI BUS EXPANSION

The design of the MOPSlcd6 follows the standard PC/104 form factor and offers both ISA- and optional PCI-bus signals. The PC/104-Plus standard is downward compatible with PC/104 and enables the use of standard PC/104 and PC/104-Plus adapter cards.

7.1 *PC/104 Bus (ISA part)*

The PC/104 bus consists of two connectors that use 104 pins in total.

- XT bus connector (64 pins)
- AT bus connector (40 pins, which is optional for 16 bit-data bus system)

The pinout of the PC/104 bus connectors corresponds to the pinout of the ISA bus connectors with some added ground pins. The two PC systems with different form factors are electrically compatible.

The **XT bus connector**, Row A and B.

The corresponding 64-pin stackthrough header (ISA bus = 62pins) has two added ground pins at the end of the connector (Pin A32 and Pin B32). The pinout between PC/104 bus and XT ISA bus is identical between A1 - A31 and B1 - B31.

The **AT bus extension connector**, Row C and D.

The corresponding 40-pin stackthrough header (ISA bus = 36 pins) has four added ground pins, two on each side of the connector. To avoid confusion, the first two pins are defined as Pin C0 and Pin D0. The additional ground pins at the end of the connector are defined as C19 and D19. The pinout between PC/104 bus and AT ISA bus is identical between C1 - C18 and D1 - D18.

7.1.1. Connectors

The MOPSlcd6 features both – XT bus and AT bus extension – on two, dual-row socket connector with 2.54mm x 2.54mm grid (0.1" x 0.1").PC/104

The PC-104 XT bus is available through the X3A connector. The PC/104 AT bus is available through the X3B connector.

A detailed description of the signals including electrical characteristics and timings is beyond the scope of this document. Please refer to the official ISA bus and PC/104 specifications for more details.

7.1.2. PC/104 Configuration

When using add-on boards on the PC/104 bus, make sure that there are no resource conflicts in the system. Carefully choose hardware interrupts, DMA channels, memory and I/O address ranges to avoid resource conflicts, which are often the reason for a board or a feature not functioning correctly. See Appendix A: System Resource Allocation for information about the resources already used by the MOPSlcd6.

7.2 *PC/104-Plus (optional PCI part)*

The MOPSlcd6 is available in different versions with or without a PC/104-Plus bus. On boards with this option, a quad-row socket stack-through connector with a 2mm x 2mm (0.79" x 0.79") pitch that implements the standard 32-bit PCI bus signals is available.

The PC/104plus connector does not have a connector shroud. You cannot use a PC/104plus board with a connector shroud on the top of a MOPSlcd6. This mechanical limitation does not reduce the functionality of a MOPSlcd6 board. You can order a module without a connector shroud or place the MOPSlcd6 board at the top of the stack.

7.2.1. PCI Connector (PC/104-Plus)

The PC/104-Plus bus is available through the optional connector X5.

A description of the signals, including electrical characteristics and timings, is beyond the scope of this document. Please refer to the official PCI bus and PC/104-Plus specifications for more details.

7.2.2. PC/104-Plus Configuration

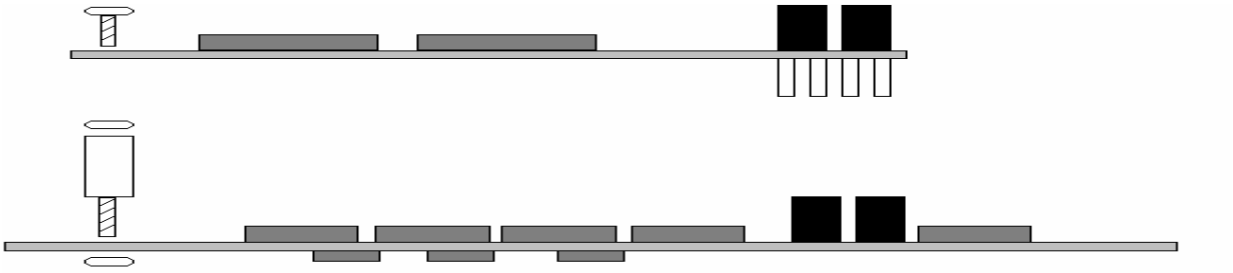
When using add-on boards on the PC/104-Plus bus, these boards have to be associated to a "PCI-slot". Make sure that there are no resource conflicts in the system. Carefully choose PCI interrupts, REQ/GNT pairs and IDSEL for the add-on board. See the technical manual of the add-on board for more details.

The MOPSlcd6 's PCI bus can be configured to optimize your system. See the PCI Configuration Submenu in Appendix B: BIOS for more information on configuration.

7.3 *PC/104 and PC/104-Plus Stack*

PC/104 and PC/104-Plus adapter cards are mounted in a stack-through manner. Adapter cards are designed with plugs on their undersides that mate with the PC/104 socket connectors of MOPSlcd6. PC/104 adapters can support the socket connector version on their topside and allow additional stacking of adapters.

Whenever possible use the MOPSlcd6 as top module of the PC/104 stack as the CPU board is normally the board with the highest heat dissipation.



8. GRAPHICS INTERFACES (MOPSLCD6 ONLY)

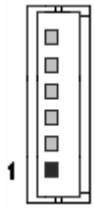
8.1 *Graphic Controller*

The MOPSlcd6 comes with a PCI graphic controller CT69000 from Asiliant. The controller features a LCD and CRT simultaneous true 64-bit graphics engine and accelerator plus integrated 2MB of video memory (SDRAM). The graphics controller supports mono-LCD, TFT, and STN displays with resolutions up to SXGA (1280x1024). The MOPSlcd6 video BIOS is integrated in the system BIOS and supports different panel types, which are identified via the configuration pins on the LCD panel connector. The MOPSlcd6 can support a variety of panel, which are all configured by a dedicated cable for each panel. Setting jumpers or changing software is not required. Because nearly all LCDs use different connectors, pinout, or LCD voltages, this is the easiest and safest way to configure different panels.

8.2 *CRT Connector*

The CRT monitor is available through the X9 connector (6 pins). To have the signals available on a standard DSUB-15 CRT monitor connector, an adapter cable is required. A 15-pin DSUB cable is available from Kontron (KAB-VGA-2, Part Number 96053-0000-00-0).

The following table shows the pinout of the CRT connector and the necessary connections for an DSUB-25 adapter.

Header	Pin	Signal Name	Function	DSUB-25
	1	RED	Analog video red	1
	2	GRN	Analog video green	2
	3	BLU	Analog video blue	3
	4	GND	Signal ground	7
	5	VSYNC	Vertical sync	14
	6	HSYNC	Horizontal sync	13

To find the location of the CRT connector on the MOPSlcd6 board, please see the Appendix E: Connector Layout chapter.

8.3 *LCD Panel Connector*

The LCD Panel interface is available through the X7 connector on the bottom of the board. This connector represents the JIPA interface (**J**UMPtec **I**ntelligent **P**anel **A**daption) and is a plug-and-play interface specified by Kontron Embedded Modules GmbH. A variety of cables for different display types are available from Kontron. Please refer to the actual cable list on the Kontron Web site for part numbers and cable names. A detailed description of the JIPA interface standard also is available in a separate document JIPAD???.PDF. The three question marks represent the documents revision number. You can download this document from the Kontron Web site, or contact your local Kontron technical support to receive it.

To find the location of the LCD Panel interface connector on the MOPSlcd6 board, please see the Appendix E: Connector Layout chapter.

8.4 *Display Power Considerations*

When using a LCD Panel in a system, additional voltages may be required to drive the displays logic, supply the backlight converter and the display contrast voltage.

The display logic may require +5V for standard or +3.3V for low-power LCDs. Contrast voltages for passive displays are normally very different and can range from –30V to +30V. Backlight converters usually are +5V or +12V types. When using a Kontron JIPA cable, you do not have to take care about all of those configurations. Display logic voltage and contrast voltage come preconfigured on the JIPA cable. Backlight voltage sometimes has to be adjusted on the cable.

Even though the MOPSlcd6 is a +5V-only board, you need to supply the +12V for the backlight converter additionally when using such a converter type.

The onboard 3.3V-circuitry of the MOPSlcd6 and the +3.3V logic voltage of low-voltage panels are powered by separate voltage regulators. The one for the LCD is mounted on the JIPA adapter cable.

8.5 Connecting a LCD Panel

To determine whether your panel display is supported, check the Kontron Web site for panel lists. We regularly update the list of panels that have been tested with the MOPSlcd6.

Many panel adapters for a wide spread variety of displays are available through Kontron. If you use one of those adapters supplied by Kontron, configuration is easy:

15. Check whether you have the correct adapter and cable for the panel you plan to use. Inspect the cable for damages.
16. Disconnect the power from your system.
17. Connect the panel adapter to the LCD Panel connector (JIPA interface) on the MOPSlcd6.
18. Connect the other end of the cable to your display.
19. Connect the backlight converter.
20. Supply power to your system.
21. If no image appears on your display, connect a CRT monitor to the CRT connector. If you still do not see improvement, consider contacting the dealer for technical support.

8.6 Configuration

You can download available drivers for the CT69000 graphic controller from the Kontron Web site. For further information read the read-me or help files or contact technical support.

8.7 Graphics Technical Support

If problems occur, you can solve some of them by using the latest drivers for the CT69000 graphic controller. Kontron provides you with the latest in house- tested drivers, which can differ from newer ones. For further technical support, contact either Kontron or get support information and downloadable software updates from Asiliant.

8.8 *Available Video Modes*

The following list shows the video modes supported by the graphic controller. When using a LCD panel on the JIPA interface, not all of the below video modes may be available. This depends on the display capabilities.

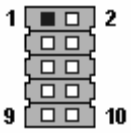
Video Mode	Display Mode	Characters/Pixels	Colors/Gray val.	Refresh Rate
00h/01h	Text	40x25	16	70
02h/03h	Text	80x25	16	70
04h/05h	Graphics	320x200	4	70
06h	Graphics	640x200	2	70
07h	Text	80x25	Mono	70
0Dh	Graphics	320x200	16	70
0Eh	Graphics	640x200	16	70
0Fh	Graphics	640x350	Mono	70
10h	Graphics	640x350	16	70
11h	Graphics	640x480	2	60
12h	Graphics	640x480	16	60
13h	Graphics	320x200	256	70
14h	Graphics	320x200	256	70
15h	Graphics	320x200	64k	70
16h	Graphics	320x200	16M	70
17h	Graphics	320x240	256	60
18h	Graphics	320x240	64k	60
19h	Graphics	320x240	16M	60
1Ah	Graphics	400x300	256	60
1Bh	Graphics	400x300	64k	60
1Ch	Graphics	400x300	16M	60
1Dh	Graphics	512x384	256	60
1Eh	Graphics	512x384	64k	60
1Fh	Graphics	512x384	16M	60
20h	Graphics	640x480	16	85
22h	Graphics	800x600	16	85
24h	Graphics	1024x768	16	85
28h	Graphics	1280x1024	16	60
30h	Graphics	640x480	256	85
31h	Graphics	640x400	256	70
32h	Graphics	800x600	256	85
34h	Graphics	1024x768	256	85
38h	Graphics	1280x1024	256	60
40h	Graphics	640x480	32k	85
41h	Graphics	640x480	64k	85
42h	Graphics	800x600	32k	85
43h	Graphics	800x600	64k	85
44h	Graphics	1024x768	32k	85
45h	Graphics	1024x768	64k	85
50h	Graphics	640x480	16M	85
52h	Graphics	800x600	16M	85
62h	Graphics	640x400	64k	70
63h	Graphics	640x400	16M	70
64h	Graphics	1024x768	16	85
68h	Graphics	1280x1024	16	60
6Ah	Graphics	800x600	16	85
70h	Graphics	640x480	256	85
71h	Graphics	640x400	256	70
72h	Graphics	800x600	256	85
74h	Graphics	1024x768	256	85
78h	Graphics	1280x1024	256	60

9. SERIAL-COMMUNICATION INTERFACES

Two fully functional serial ports (COMA and COMB) provide asynchronous serial communications. COMA and COMB support RS-232 operation modes and are compatible with the serial-port implementation used on the IBM Serial Adapter. They are 16550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 50baud to 115.2Kbaud.

9.1 *Connectors*

COMA is available through the X18 connector (10 pins) and COMB through the X19 connector (10 pins). To have the signals available on the standard serial interface connectors DSUB9 or DSUB25, an adapter cable is required. A 9-pin DSUB cable is available from Kontron (KAB-DSUB9-2, Part Number 96017-0000-00-0). The following table shows the pinouts for COMA and COMB, as well as necessary connections for DSUB adapters.

Header	Pin	Signal Name	Function	In / Out	DSUB-25	DSUB-9
	1	/DCD	Data Carrier Detect	In	8	1
	2	/DSR	Data Set Ready	In	6	6
	3	RxD	Receive Data	In	3	2
	4	/RTS	Request to Send	Out	4	7
	5	TxD	Transmit Data	Out	2	3
	6	/CTS	Clear to Send	In	5	8
	7	/DTR	Data Terminal Ready	Out	20	4
	8	/RI	Ring Indicator	In	22	9
	9	GND	Signal Ground	--	7	5
	10	VCC (*)	+5V	--	--	--

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

To find the location of the serial ports on the MOPSlcd6 board, please see the Appendix E: Connector Layout chapter.

9.2 *Configuration*

You can set the two serial input/output interfaces to a variety of I/O addresses and IRQ configurations. Refer to the I/O Device Configuration submenu in the Appendix B: BIOS Operation chapter for configuration information.

Note: Most operating systems detect the serial port with the I/O address 3F8h as COM1 and 2F8h as COM2.

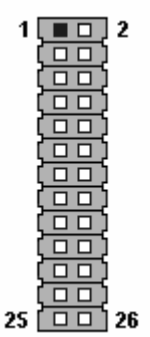
10. PARALLEL-COMMUNICATION INTERFACE

The MOPSlcd6 incorporates an IBM XT/AT compatible parallel port. It can be set to bi-directional and supports EPP and ECP operating modes. The bi-directional functions are compatible with those of an IBM PS/2 style parallel port. This functionality is always available and does not conflict with printer use.

10.1 *Connector*

The parallel port is available through the X11 connector (26 pins). To have the signals available on a standard, parallel-interface connector DSUB-25, an adapter cable is required, which is offered by Kontron (KAB-DSUB25-1, Part Number 96015-0000-00-0).

The following table shows the pinout as well as necessary connections for a DSUB-25 adapter.

Header	Pin	Signal Name	Function	In / Out	DSUB-25
	1	/STB	Strobe	Out	1
	3	PD0	Data 0	I/O	2
	5	PD1	Data 1	I/O	3
	7	PD2	Data 2	I/O	4
	9	PD3	Data 3	I/O	5
	11	PD4	Data 4	I/O	6
	13	PD5	Data 5	I/O	7
	15	PD6	Data 6	I/O	8
	17	PD7	Data 7	I/O	9
	19	/ACK	Acknowledge	In	10
	21	/BUSY	Busy	In	11
	23	PE	Paper out	In	12
	25	/SLCT	Select out	In	13
	2	/AFD	Autofeed	Out	14
	4	/ERR	Error	In	15
	6	/INIT	Init	Out	16
	8	/SLIN	Select in	Out	17
	26	VCC (*)	+ 5 V	--	NC
	10,12	GND	Signal Ground	--	18 - 25
	14,16	GND	Signal Ground	--	18 - 25
	18,20	GND	Signal Ground	--	18 - 25
	22,24	GND	Signal Ground	--	18 - 25

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

To find the location of the parallel port on the MOPSlcd6 board, please see the Appendix E: Connector Layout chapter.

10.2 *Configuration*

The parallel-port mode, I/O addresses, and IRQs are changeable in the MOPSlcd6 BIOS Setup Utility. You can program the base I/O-address 378h, 3BCh, 278h, disable the interface or set it to AUTO. You can choose IRQ5 or IRQ7 as the parallel-port interrupt. In ECP mode, you can choose DMA 1 to DMA 3.

Refer to the I/O Device Configuration Submenu in the Appendix B: BIOS Operation chapter for additional information on configuration.

11. KEYBOARD AND FEATURE INTERFACE

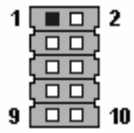
The keyboard and feature connector of the MOPSlcd6 offers five functions. The interface connects the following:

- Keyboard
- Keyboard lock switch
- Speaker
- Battery
- Reset button

11.1 *Connector*

The keyboard and feature connector is available through Connector X13 (10 pins). An adapter cable is required to connect a standard keyboard to this interface. There are two adapter cables available from Kontron. One can be used for AT-keyboard (KAB-KB-1, Part Number 96023-0000-00-0), the other for PS/2-keyboard (KAB-KB-PS2, Part Number 96060-0000-00-0). The adapter cables do not know the other functions on this interface.

The following table shows the pinout as well as necessary connections for adapters.

Header	Pin	Signal Name	Function	5-pin Din (Diode)	6-pin MiniDin (PS2)
	1	Speaker	Speaker output		
	2	GND	Ground		
	3	/RESIN	Reset input		
	4	/KBLOCK	Keyboard lock		
	5	KBDAT	Keyboard data	2	1
	6	KBCLK	Keyboard clock	1	5
	7	GND	Ground	4	3
	8	VCC (*)	+5V	5	4
	9	BATT	Battery in (3,0V)		
	10	PWRGOOD	Powergood		

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

To find the location of the keyboard and feature connector on the MOPSlcd6 board, please see the Appendix E: Connector Layout chapter.

11.2 Configuration

Refer to the Keyboard Features submenu in the Appendix B: BIOS chapter for information on configuration.

11.3 Signal Descriptions

/KBLOCK (Keyboard Lock)

- Input on CPU modules
- Output on any other module
- Input to the keyboard controller input Port 1, Bit 7

/RESIN and PWRGOOD (Reset Inputs)

- Input on CPU modules
- When POWERGOOD goes high, it starts the reset generator on the CPU module to pull the onboard reset line high after a valid reset period. You also can use this pin as a low active hardware reset for modules.

Speaker

- Open collector output on modules that drive a piezo electronic speaker.
- Input on modules that connects a 5V piezo electronic speaker to this pin.
- An 8-Ohm loudspeaker also can be connected between SPEAKER and GND, but because of current limitation the volume will be low.
- Connect only one speaker to this pin. The CPU usually drives this pin. However, other modules also can use this signal to drive the system speaker.

KBDAT (Keyboard Data)

- Bi-directional I/O pin on CPU modules
- Keyboard data signal

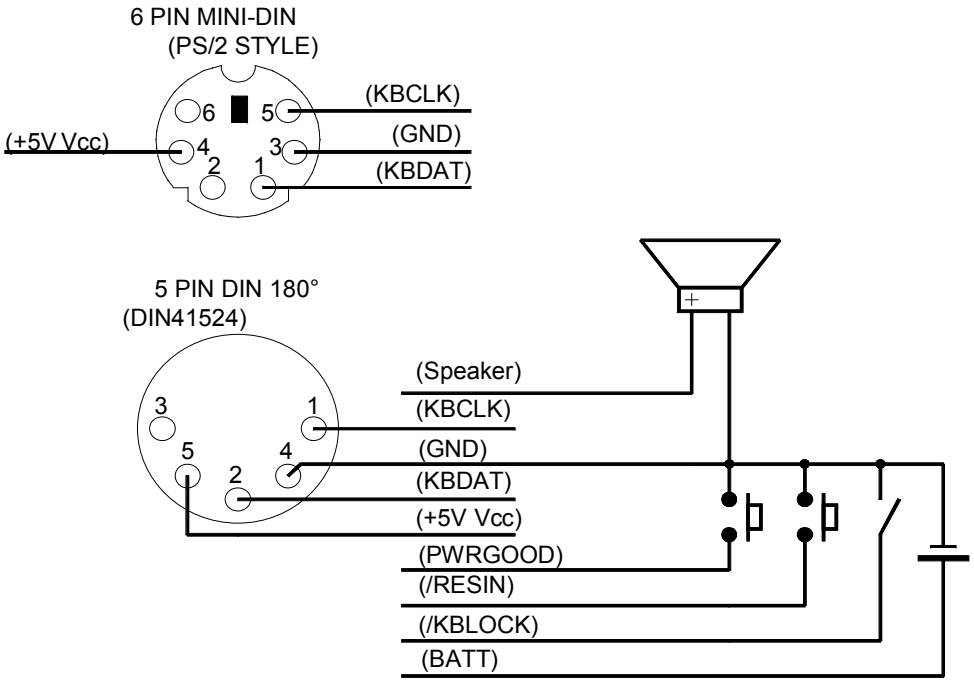
KBCLK (Keyboard Clock)

- Bi-directional I/O pin on CPU modules
- Keyboard clock signal

BATT (System Battery Connection)

- This pin connects a system battery to all modules.
- The battery voltage has to be higher than 2.4V and lower than 4.0V. A 3V battery is recommended.
- A battery is not needed to hold CMOS setup data. Your configurations for hard disks, floppy drives, and other peripherals are saved in an onboard DRAM. However, you need a battery to save the CMOS date and time when power supply is turned off.

11.3.1. Example Connection AT-keyboard and Other Functions



12. USB INTERFACE

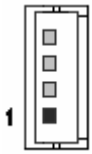
The chipset of the MOPSlcd6 has a USB host bridge integrated. It comes with one USB port, which follows the OHCI specification and is USB-1.1 compliant.

You can expand the amount of USB connections by adding external hubs. You can connect up to 127 USB peripherals to each hub.

12.1 *Connector*

The USB port is available through the X10 connector (4 pins). To have the signals available on the standard USB interface connectors, an adapter cable is required. A USB interface cable is available from Kontron (KAB-USB-1, Part Number 96054-0000-00-0).

The following table shows the pinouts for the USB connector.

Header	Pin	Signal Name	Function
	1	VCC *	+5V
	2	USB0	USB-
	3	USB1	USB+
	4	GND	Ground

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

To find the location of the USB ports on the MOPSlcd6 board, please see the Appendix E: Connector Layout chapter.

12.2 *Configuration*

Configuration entries are available for the USB ports in the BIOS Setup Utility. You can enable/disable the USB controller as well as the USB legacy support. Please refer to the PCI Device Configuration and the I/O Device Configuration submenus in the Appendix B: BIOS chapter for information.

12.3 *Limitations*

The power contacts for USB devices on Pin 1 and Pin 4 are not protected. They are suitable to supply connected USB devices with a maximum of 500mA power dissipation. Do not supply external USB devices with higher power dissipation through these pins. Always use a fuse for power on external USB connectors, otherwise a defective USB device may damage the MOPSlcd6. Kontron recommends using a resetable fuse for power on external USB connectors to follow the USB specification.

13. FLOPPY-DRIVE INTERFACE

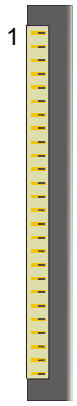
The floppy-drive interface of the MOPSlcd6 uses a 2.88MB super I/O floppy-disk controller and can support one floppy disk drive with densities that range from 360kB to 2.88MB. The controller is 100% IBM compatible.

13.1 *Connector*

The floppy disk interface is available on the flat-foil Connector X16 (26 pins). This type of connector is often internally used in notebooks to connect a slim-line floppy drive.

Accessories are available for this interface from Kontron. To connect a standard 3.5" floppy drive, use an adapter cable (ADA-FLOPPY-2, Part Number 96001-0000-00-0). If you have a slim-line 3.5" floppy drive, you may need a flat foil cable (KAB-FLOPPY/MOPS-1, Part Number 96019-0000-00-0). It also is possible to get a slim line 3.5" floppy drive with cable from Kontron (FLOPPY-MOPS-1, Part Number 96010-0000-00-0).

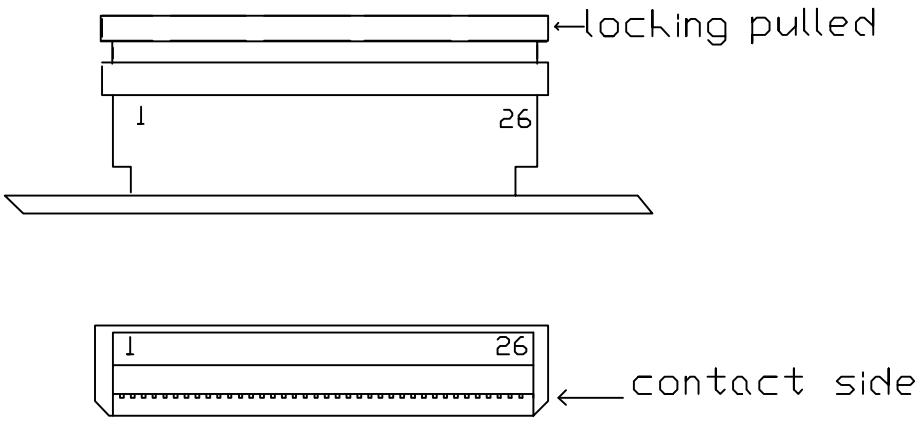
The following table shows the connector pinout.

Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	1	VCC *	+5V	2	/IDX	Index
	3	VCC *	+5V	4	/DR0	Drive Select 0
	5	VCC *	+5V	6	/DSKCHG	Disk Change
	7	NC	Not connected	8	NC	Not connected
	9	NC	Not connected	10	/MTR0	Motor on 0
	11	NC	Not connected	12	/FDIR	Direction Select
	13	NC	Not connected	14	/STEP	Step
	15	GND	Ground	16	/WDATA	Write Data
	17	GND	Ground	18	/WGATE	Write Gate
	19	GND	Ground	20	/TRK0	Track 00
	21	GND	Ground	22	/WRTPRT	Write Protect
	23	GND	Ground	24	/RDATA	Read Data
	25	GND	Ground	26	/HDSEL	Side One Select

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

To find the location of floppy-drive interface on the MOPSlcd6 board, please see the Appendix E: Connector Layout chapter.

13.1.1. Connector Diagram



13.2 *Configuration*

You can configure the floppy disk interface in the BIOS Setup Utility. You can choose the 3.5" (common) or 5.25" drive types with densities of 360kB, 720kB, 1.2MB, 1.25MB, 1.44MB or 2.88MB. Refer to the Main Menu section of the Appendix B: BIOS Operation chapter for more information on configuring the floppy drive.

You also can disable the floppy-disk interface in the I/O Device Configuration Submenu.

14. IDE INTERFACE

The MOPSlcd6 features one IDE interface (Ultra33 DMA mode) that can drive two hard disks. When two devices share a single adapter, they are connected in a master/slave, daisy-chain configuration. If only one drive is in the system, you must set it as the master.

14.1 *Connector*

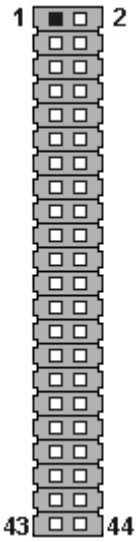
The IDE interface is available through Connector X17 (44 pins). This interface is designed in 2mm grid for optimal connectivity to a 2.5" hard disk.

There are several accessories available for IDE connectivity.

You can use two cables to directly connect a hard disk in a 2.5" form factor (KAB-IDE-2MM, Part Number 96021-0000-00-0) or a 3.5" form factor (KAB-IDE-25, Part Number 96020-0000-00-0).

You can plug a Kontron chipDISK, which is an IDE hard disk that uses Flash technology, into the IDE interface and mechanically mount it by using a mini-spacer on the chipDISK hole. You also can use a chipDISK adapter (chipDISK-ADA1, Part Number 96004-0000-00-0) or compact Flash adapter (CFC-ADA1, Part Number 96004-0000-00-2) for more disk support.

The following table shows the pinout.

Header	Pin	Signal Name	Function	Pin	Signal Name	Function
	1	/RESET	Reset	2	GND	Ground
	3	HDD7	Data 7	4	HDD8	Data 8
	5	HDD6	Data 6	6	HDD9	Data 9
	7	HDD5	Data 5	8	HDD10	Data 10
	9	HDD4	Data 4	10	HDD11	Data 11
	11	HDD3	Data 3	12	HDD12	Data 12
	13	HDD2	Data 2	14	HDD13	Data 13
	15	HDD1	Data 1	16	HDD14	Data 14
	17	HDD0	Data 0	18	HDD15	Data 15
	19	GND	Ground	20	Key (NC)	Key pin
	21	DRQ	IDE DMA Request	22	GND	Ground
	23	/IOW	I/O write	24	GND	Ground
	25	/IOR	I/O read	26	GND	Ground
	27	IOCHRDY	I/O channel ready	28	NC **	Not connected
	29	AKJ	Acknowledge	30	GND	Ground
	31	SIRQ	Interrupt	32	NC	Not connected
	33	SA1	Addr 1	34	NC	Not connected
	35	SA0	Addr 0	36	SA2	Addr 2
	37	/CS1	Chip select 1	38	CS3	Chip select 3
	39	NC	Not connected	40	GND	Ground
	41	VCC	+5V	42	VCC (Motor)	+5V
	43	GND	Ground	44	NC	Not connected

Notes: (*) To protect the external power lines of peripheral devices, make sure that:
-- the wires have the right diameter to withstand the maximum available current
-- the enclosure of the peripheral device fulfils the fire-protecting requirements of
-- IEC/EN 60950.

(**) Pin 28 is normally used as cable select signal. On the MOPSlcd6 it is not connected. IDE devices that have to use cable select will not function under all configurations.

To find the location of IDE-controller interface on the MOPSlcd6 board, please see the Appendix E: Connector Layout chapter.

14.2 *Configuration*

The IDE interface offers several configuration settings. Refer to the Main Menu and I/O Device Configuration Submenu in the Appendix B: BIOS Operation chapter for additional information on configuration.

15. ETHERNET INTERFACE

The Ethernet interface is realized with the 82551ER from Intel, a fully integrated 10BASE-T/100BASE-TX LAN solution. The 82551ER consists of both the Media Access Controller (MAC) and the physical layer (PHY) interface combined into a single component solution. A 32-bit PCI controller provides enhanced scatter-gather bus mastering capabilities and enables the 82551ER to perform high-speed data transfers over the PCI bus. Two large transmit and receive FIFOs of 3 Kbytes each help prevent data underruns and overruns while waiting for bus accesses. The 82551ER can operate in either full duplex or half duplex mode. In full duplex mode, the 82551ER adheres with the IEEE 802.3x Flow Control specification. Half-duplex performance is enhanced by a proprietary, collision-reduction mechanism. The 82551ER also includes an interface to a serial (4-pin) EEPROM. The EEPROM provides power-on initialization for hardware and software configuration parameters.

The 82551ER provides the following features:

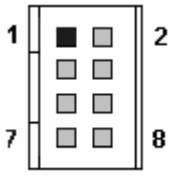
- Integrated IEEE 802.3 10BASE-T and 100BASE-TX compatible PHY
- Glueless 32-bit PCI master interface
- Improved dynamic transmit chaining with multiple priorities transmit queues
- Backward compatible software to the 82558 and 82557
- Full Duplex support at both 10 and 100Mbps
- IEEE 802.3u Auto-Negotiation support
- 3 KB transmit and 3 KB receive FIFOs
- IEEE 802.3x 100BASE-TX Flow Control support
- Adaptive Technology
- TCP/UDP checksum offload capabilities
- Low power 3.3 V device
- Clock run protocol support

Note: The Ethernet interface works according to the common criteria of the embedded technology market segment.

15.1 *Connector*

The Ethernet interface is available through Connector X6 (8 pins). To have the signals of the Ethernet connection available on a standard RJ45 connector, you need an adapter cable, which is offered by Kontron (KAB-MOPS-ETN1, Part Number 96048-0000-00-0).

The following table shows the pinout.

Header	Pin	Signal Name	Function	In/Out
	1	TXD+	10BASE-T Transmit	Differential Output
	2	TXD-	10BASE-T Transmit	Differential Output
	3	RXD+	10BASE-T Receive	Differential Input
	4	SHLDGND	Shield Ground	
	5	SHLDGND	Shield Ground	
	6	RXD-	10BASE-T Receive	Differential Input
	7	ACTLED *	Activity LED	Output
	8	LILED *	Link LED	Output

Notes: TXD+, TXD- differential-output pair drives 10 and 100Mb/s Manchester-encoded data to 100/10BASE-T transmit lines.
RXD+, RXD- differential input pair receives 10 and 100Mb/s Manchester-encoded data from 100/10BASE-T receive lines.
(*) ACTLED and LILED have an onboard 470Ohm serial resistor and can directly be connected to a LED's cathode. Connect anode to VCC.

To find the location of the Ethernet interface on the MOPSlcd6 board, please see the Appendix E: Connector Layout chapter.

15.2 *Configuration*

You can download available drivers and setup utilities from the Kontron Web site. Please refer to the corresponding readme and setup/install files. For further information contact your local technical support.

You can enable an onboard LAN RPL ROM to support the boot up of the system via Ethernet and a PXE-boot server. Refer to the Boot Menu in the Appendix B: BIOS Operation chapter.

15.3 *Ethernet Technical Support*

Many problems can be solved with the latest drivers for the 82551ER controller. In our system, the 82551ER is working in 82559ER compatibility mode; so if you already used the 82559ER on former boards no additional changes on these drivers in your system are necessary. Please use the 82559ER drivers for the 82551ER as well.

Kontron provides you with the latest tested drivers, which might be quite different from the newest ones. Therefore feel free to contact the Intel Web site for driver updates.

16. POWER CONNECTION

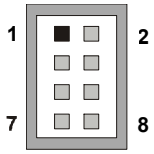
In some applications, the MOPSlcd6 is intended for use as a stand-alone module without a backplane. You need to have a power connector available on the board for direct power supply. The MOPSlcd6 is a +5V-only board. Peripherals can obtain additional voltage from the power connector next to the PC/104 bus. The additional voltages (+12V, -5V and -12V) are not generated onboard the MOPSlcd6.

The +3.3V for PC/104-Plus boards are also not generated on the MOPSlcd6 board. You must supply PC/104-Plus boards separately through the PC/104-Plus bus. Use +5V PC/104-Plus add-on cards.

16.1 *Connector*

The power connector is available as X3C (8 pins).

The following table shows the pinout.

Header	Pin	Signal Name	Function
	1	GND	Ground
	2	VCC	+5V
	3	BATT	Battery
	4	+12V	+12V
	5	-5V	-5V
	6	-12V	-12V
	7	GND	Ground
	8	VCC	+5V

To find the location of the power connector on the MOPSlcd6 board, please see the Appendix E: Connector Layout chapter.

16.2 *Power Pins*

Every power pin on the power connector as well as on the PC/104 and PC/104-Plus bus connectors is limited to a maximum current of 1A per pin.

If a system using a MOPSlcd6 is only supplied from the power connector, the following limitations apply:

Power	Number of Pins	Max. Current
VCC (+5V)	2	2A
+12V	1	1A
-12V	1	1A
-5V	1	1A
GND	2	2A

A system using the MOPSlcd6 also can be supplied from the PC/104 and PC/104-Plus bus connectors. If only those supply voltages pins are used, the following limitations apply:

Power	Number of pins on ISA part	Number of pins on PCI part	Max. Current
VCC (+5V)	4	8	4A + 8A = 12A
+12V	2	1	2A + 1A = 3A
-12V	2	1	2A + 1A = 3A
-5V	2	0	2A
+3.3V	0	10	10A
GND	8	23	8A + 23A = 31A

Modules on the PC/104 bus or PC/104-Plus bus consuming a higher supply current must provide power supply through an additional connector.

Note: The MOPSlcd6 is not a replacement for a backplane. Use all power pins on the power connector and on the PC/104 connectors for power supply to the MOPSlcd6, and also use all additional power connectors on additional I/O cards, if your system exceeds the above limitations. It is not acceptable to use only the power pins of the PC/104 connector for power supply of the full PC/104 stack.

16.3 *External Battery*

You can connect an external battery to Pin 3 (BATT) of the power connector instead of Pin 9 of the KBD connector. For more information refer to the Keyboard and Feature Interface section.

Note: The two battery inputs are not protected against each other and can only be used exclusively.

17. WATCHDOG TIMER

The watchdog timer is integrated in the chipset of the MOPSlcd6 and can issue a reset to the system or generate a nonmaskable interrupt (NMI). The watchdog timer circuit has to be triggered within a specified time by the application software. If the watchdog is not triggered because proper software execution fails or a hardware malfunction occurs, it will reset the system or generate the NMI.

17.1 *Configuration*

You can set the watchdog timer to disabled, reset or NMI mode. You can specify the delay time from 1 second to 30 minutes and timeout (trigger period) from 1 second up to 10 minutes. The delay time is the time after first initialization before the trigger period starts. The timeout is the time the watchdog has to be triggered within. You can make the initialization settings in the BIOS setup. Refer to the Watchdog Settings Submenu in the Appendix B: BIOS Operation chapter for information on configuration.

17.2 *Programming*

17.2.1. Initialization

You can initialize the watchdog timer from the BIOS setup. You also can set up the initialization from the application software with help of the JIDA (Jumptec Intelligent Device Architecture) programmer's interface or by using low-level programming.

17.2.2. Trigger

The watchdog needs to be triggered out of the application software within a specified timeout period. You can only do this in the application software by using low-level programming or with help of the JIDA programmer's interface.

For information about low-level programming for the watchdog timer, refer to Application Note WdogP588_E???.DOC, which you can request from Kontron technical support.

For information about the JIDA programmer's interface refer to the JIDA BIOS extension section in the Appendix B: BIOS chapter and separate documents available in the JIDA software packages on the Kontron Web site.

18. APPENDIX A: SYSTEM RESOURCE ALLOCATIONS

18.1 *Interrupt Request (IRQ) Lines*

Please note that Kontron PC/104 devices were designed after the draft of P996 Specification for ISA systems. Because of this, shareable interrupts are not supported. Some PC/104 add-on board manufacturers do not follow the P996 Specification and allow shareable interrupts. If you want to use such PC/104 boards with Kontron devices, contact the manufacturer of the add-on board and ask about switching to non-interrupt sharing.

IRQ #	Used for	Available	Comment
0	Timer0	No	
1	Keyboard	No	
2	Cascade	No	
3	COM B	No	Note (1)
4	COM A	No	Note (1)
5		Yes	Note (2)
6	FDC	No	Note (1)
7	LPT1	No	Note (1), Note (2)
8	RTC	No	
9		Yes	
10	COM C	Yes	Note (3)
11	COM D	Yes	Note (3)
12		Yes	
13	Numeric processor	No	
14	EIDE Channel 1	No	Note (1)
15		Yes	

Notes: (1) If the „used for"-device is disabled in setup, the corresponding interrupt is available for other devices.
(2) LPT1 can also be configured for IRQ5
(3) COM C and COM D may use these interrupts when an external SMSC 669 controller is in the system. Interrupts are free without this external controller

18.2 Direct Memory Access (DMA) Channels

DMA #	Used for	Available	Comment
0	LPT	No	Note (2)
1		Yes	Note (3)
2	FDC	No	Note (1), Note (3)
3		Yes	Note (3)
4	Cascade	No	
5		Yes	
6		Yes	
7		Yes	

Notes: (1) If the „used for"-device is disabled in setup, the corresponding DMA channel is available for other devices.
(2) The DMA channel is only used in ECP mode of LPT, in other modes it is available.
(3) Possible alternative setting of LPT in ECP mode for used DMA channel.

18.3 I/O Address Map

The I/O-port addresses of the processor module MOPSlcd6 are functionally identical to a standard PC/AT. All addresses not mentioned in this table should be available. We recommend that you do not use I/O addresses below 0110hex with additional hardware for compatibility reasons, even if available.

I/O Address (h)	Use	Available	Comment
0000 - 001F	DMA Controller 1	No	
0020 - 0021	Interrupt Controller 1	No	
0040 - 0044	Timer	No	
0060 - 0066	Keyboard controller	No	
0061	Port B Register	No	
0070	NMI Enable Register	No	
0070 – 0071	Real Time Clock	No	
0080	BIOS Post	No	
0081 - 008F	DMA Page Register 74LS612	No	
0092	Port A Register (Fast A20 Gate)	No	
0090 - 009F	System Control	No	
00A0 - 00A1	Interrupt Controller 2	No	
00A2 - 00A3	System Control	No	
00C0 - 00DF	DMA Controller 2	No	
00E0	System Control	No	
00F0 - 00FF	Math Coprocessor	No	
0100 - 010F	General Purpose I/O	No	Kontron Control Port
01F0 - 01F8	Fixed Disk	No	
0278-027Fh		Yes	Free in standard configuration, but possible address of LPT1.
02E8-02EF		Yes	Free in standard configuration, but possible address of COM.
02F8-02FF	Serial Port 2	No	
0378 - 037F	Parallel Port 1	No	
03BC - 03C4		Yes	Free in standard configuration, but possible address of LPT1.
03C0 - 03DF	Video	No	Free on boards without graphic
03E8 - 03EF		Yes	Free in standard configuration, but possible address of COM.
03F0 - 03F7	Diskette Controller	No	
03F8 - 03FF	Serial Port 1	No	
04D0 – 04D1	INT edge/level control	No	
04D6	DMA 2 extended mode register	No	
0CFC - 0CFF	Configuration Data Register	No	

18.4 Memory Map

The MOPSlcd6 processor module can support up to 256MB of memory. The first 640KB of DRAM are used as main memory.

Using DOS, you can address 1MB of memory directly. Memory area above 1MB (high memory, extended memory) is accessed under DOS via special drivers such as HIMEM.SYS and EMM386.EXE, which are part of the operating system. Please refer to the operating system documentation or special textbooks for information about HIMEM.SYS and EMM386.EXE.

Other operating systems (Linux or Windows versions) allow you to address the full memory area directly.

Upper Memory	Use	Available	Comment
A0000h – BFFFFh	VGA Memory	No	Mainly used by graphic adapter cards. If a PCI graphic card is in the system this memory area is mapped to the PCI bus.
C0000h – CBFFFh	VGA BIOS	No	Free for ISA bus or shadow RAM on board MOPS/686+ where no VGA controller is mounted. C0000h – C7FFFh is mainly used by external ISA VGA cards.
CC000h – DFFFFh		Yes	Free for ISA bus or shadow RAM in standard configurations. If onboard LAN RPL ROM is enabled, USB legacy support is enabled or JRC is used, a 16K block is shadowed for BIOS extensions, starting with first free area at CC000h or D0000h, D4000h, D8000hor DC000h. (BIOS extensions do not use the whole shadow block.)
E0000h – F0000h	System BIOS	No	OHCI Register MAP in USB Legacy Support is starting at E0000h by default setting.

18.4.1. Using Expanded Memory Managers

MOPSlcd6 extension BIOSes may be mapped to an upper memory area. (See the previous table.). Some add-on boards also have optional ROMs or use drivers that communicate with their corresponding devices via memory mapped I/O such as dual-ported RAM. These boards have to share the upper memory area with the Expanded Memory Manager's EMS frame. This often causes several problems in the system.

Most EMMs scan the upper memory area for extension BIOSes (optional ROMs) and choose a free memory area for their frame if it is not explicitly set. Normally, they are not always capable of detecting special memory-mapped I/O areas. You need to tell the EMM which memory areas are not available for the EMS frames, which is most of the time done by using special exclusion parameters.

If the Expanded Memory Manager you use cannot detect extension BIOSes (optional ROMs), make sure you excluded all areas in the upper memory, which are used by extension BIOSes, too. Your instruction in the CONFIG.SYS concerning the Expanded Memory Manager should look like this: (question marks for location of extension BIOS).

MS-DOS Example

```
DEVICE=EMM386.EXE X=????-???? X=E000-FFFF
```

Note: When booting up your system using this configuration under MS-DOS, the exclusion of area F000 to FFFF causes a warning. Microsoft reports that this message will always appear when the F000 segment lies in the shadow RAM. This is a bug of EMM386, not the MOPSlcd6.

Please read the technical manuals of add-on cards used with the MOPSlcd6 for the memory areas they use. If necessary, also exclude their memory locations to avoid a conflict with the EMM.

18.5 *Peripheral Component Interconnect (PCI) Devices*

All devices follow the PCI 2.1 specification. The BIOS and OS control memory and I/O resources. Please refer to the PCI 2.1 specification for details.

PCI Device (IDSEL)	PCI IRQ	REQ / GNT	Comment
PCI Graphic (AD17)	INTD#	-	
Ethernet (AD19)	INTC#	REQ3 / GNT3	
USB Controller	INTA#	-	Integrated in ALi chipset.

Note: (*) PC/104Plus specification allows only 3 external masters (REQ0, REQ1 and REQ2).

19. APPENDIX B: BIOS OPERATION

The MOPSlcd6 comes with Phoenix BIOS 4.0, Release 6.0, which is located in an onboard Flash EEPROM in compressed form. The device has 8-bit access. The shadow RAM feature provides faster access (16 bits). The onboard Flash EEPROM also holds some special Kontron BIOS extensions, which are loaded during boot up if the corresponding feature is enabled.

You can update the BIOS using a Flash utility.

19.1 *Determining the BIOS Version*

To determine the BIOS version of the MOPSlcd6 , immediately press the **<Pause/Break>** key on your keyboard as soon as you see the following text display in the upper left corner of your screen:

```
PhoenixBIOS 4.0 Release 6.0
Copyright 1985-2000 Phoenix Technology Ltd.
All Rights Reserved
Kontron(R) BIOS Version <P588R140>
(C)Copyright 2001 Kontron Embedded Modules GmbH
```

Whenever you contact technical support about BIOS issues, providing a BIOS version <P588R???> is especially helpful.

The system BIOS provides additional information about the board's serial number, CPU, and memory information by displaying information similar to the following:

```
S/N: XE3270122

CPU = Pentium with MMX166 MHz
637K System RAM Passed
127M Extended RAM Passed
System BIOS shadowed
Video BIOS shadowed

UMB upper limit segment address: E80F
```

The board's serial number has value to technical support. MOPSlcd6 serial numbers always start with XE and are followed by six or seven digits. The first digit represents the year of manufacturing, the next two digits stand for the lot number, and the last three or four digits are the number of the board in that lot.

In the example above, the board with the serial number XE3270122 was manufactured in year 2003, lot 27 of that year, and is board number 122 of that lot.

19.2 *Setup Guide*

The Phoenix BIOS Setup Utility changes system behavior by modifying the BIOS configuration. The setup program uses a number of menus to make changes and turn features on or off.

The BIOS setup menus documented in this section represent those found in most models of the MOPSlcd6. The BIOS setup for specific models can differ slightly.

Note: Selecting incorrect values may cause system boot failure. Load setup-default values to recover by pressing <F9>.

19.2.1. Start Phoenix BIOS Setup Utility

To start the Phoenix BIOS Setup Utility, press the **<F2>** key when the following string appears during boot up.

```
Press <F2> to enter Setup
```

The Main Menu then appears.

19.2.2. General Information

The **Setup Screen** is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top-level menus.
Legend Bar	Bottom	Lists setup navigation keys.
Item Specific Help Window	Right	Help for selected item.
Menu Window	Left Center	Selection fields for current menu.
General Help Window	Overlay (center)	Help for selected menu.

Menu Bar

The menu bar at the top of the window lists different menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window.
<Esc>	Exit menu.
← or → Arrow key	Select a menu.
↑ or ↓ Arrow key	Select fields in current menu.
<Tab> or <Shift-Tab>	Cycle cursor up and down.
<Home> or <End>	Move cursor to top or bottom of current window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F5> or <->	Select previous value for the current field.
<F6> or <+> or <Space>	Select next value for the current field.
<F9>	Load the default configuration values for this menu.
<F10>	Save and exit.
<Enter>	Execute command or select submenu.
<Alt-R>	Refresh screen.

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and - keys to select a value for that field. **Save Value** commands in the **Exit** menu save the values displayed in all menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (▸) marks all submenus.Item Specific Help Window

The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

Pressing **<F1>** or **<ALT-F1>** on a menu brings up the General Help window that describes the legend keys and their alternates. Press **<Esc>** to exit the General Help window.

19.3 Main Menu

Feature	Option	Description
System Time	HH:MM:SS	Set system time. Press <Enter> to move to MM or SS.
System Date	MM/DD/YYYY	Set system date. Press <Enter> to move to DD or YYYY.
Legacy Diskette A	360 kB, 5 ¼" 1.2 MB, 5 ¼" 720 kB, 3 ½" **1.44/1.25 MB**, 3 ½" 2.88 MB, 3 ½" Not installed Disabled	Select type of installed floppy disk drive.
Legacy Diskette B *	360 kB, 5 ¼" 1.2 MB, 5 ¼" 720 kB, 3 ½" 1.44/1.25 MB, 3 ½" 2.88 MB, 3 ½" Not installed **Disabled**	Select type of installed floppy disk drive.
▸ Primary Master	Autodetected drive	Displays results of PM autotyping.
▸ Primary Slave	Autodetected drive	Displays results of PS autotyping.
▸ Memory Shadow	Submenu	Opens Memory Shadow submenu.
▸ Memory Cache	Submenu	Opens Memory Cache submenu.
System Memory	N/A	Displays total of conventional memory detected during boot-up.
Extended Memory	N/A	Displays total of extended memory detected during boot-up.

Notes: In the Option column, bold shows default settings.
(*) Normally only one floppy drive is supported by the onboard floppy interface.

19.3.1. Master or Slave Submenus

Feature	Option	Description
Type	None User **Auto** CD-ROM ATAPI Removable Other ATAPI	None = Autotyping is not able to supply the drive type or end user has selected None, disabling any drive that may be installed. User = End user supplies the hdd information. Auto = Autotyping, the drive itself supplies the information. CD-ROM = CD-ROM drive. ATAPI Removable = Read- and writeable media e.g. LS120 and USB-ZIP Other ATAPI = for ATAPI devices not supported by other HDD features.
Cylinders	1 to 65,536	Number of cylinders in CHS format.
Heads	1 to 256	Number of read/write heads in CHS format.
Sectors	1 to 63	Number of sectors per track in CHS format.
Maximum Capacity	N/A	Displays the calculated size of the drive using CHS format.
Total Sectors*	N/A	Total number of sectors in LBA mode as reported by the drive during autotyping.
Maximum Capacity	N/A	Displays the calculated size of the drive by using the LBA format.
Multi-Sector Transfers	**Disabled** Standard 2 sectors 4 sectors 8 sectors 16 sectors	Any selection except Disabled determines the number of sectors transferred per block. The standard is 1 sector per block.
LBA Mode Control	**Disabled** Enabled	Enabling LBA uses Logical Block Addressing instead of CHS.
32-Bit I/O	**Disabled** Enabled	Enables 32-bit communication between CPU and IDE card. Requires PCI or Local Bus.
Transfer Mode	**Standard** Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4	Selects the method for transferring the data between the hard disk and system memory.
Ultra DMA Mode	**Disabled** Enabled	Enables UDMA Mode if your drive supports this. Use a quality short cable; non-additional connectors or adapters from the board connector to the hard disk are allowed.
SMART Device Monitoring	**Disabled** Enabled	Enables SMART warnings of imminent failure of drive.

Note: In the Option column, bold shows default settings.

19.3.2. Memory Shadow Submenu

Feature	Option	Description
C800 - CBFF	**Disabled** Enabled	Accesses to this upper memory region go to the ISA bus if Disabled or to local memory if Enabled. NOTE: This option is not displayed if the VGA BIOS exceeds 32kB (like on MOPSlcd6)! In that case this region is shadowed automatically.
CC00 - CFFF	**Disabled** Enabled	Accesses to this upper memory region go to the ISA bus if Disabled or to local memory if Enabled.
D000 – D3FF	**Disabled** Enabled	See above.
D400 – D7FF	**Disabled** Enabled	See above.
D800 - DBFF	**Disabled** Enabled	See above.
DC00 - DFFF	**Disabled** Enabled	See above.

Note: In the Option column, bold shows default settings.

19.3.3. Memory Cache Submenu

Feature	Option	Description
System BIOS	Disabled **Enabled**	Caches the system BIOS to improve performance.
Video BIOS	Disabled **Enabled**	Caches the video BIOS to improve performance.
C800 - CBFF	**Disabled** Enabled	Controls caching of accesses to this upper memory region. NOTE: this option is not displayed if the VGA BIOS exceeds 32k (like on MOPSlcd6). In that case, this region is handled by the option video BIOS.
CC00 - CFFF	**Disabled** Enabled	Controls caching of accesses to this upper memory region.
D000 – D3FF	**Disabled** Enabled	See above.
D400 – D7FF	**Disabled** Enabled	See above.
D800 - DBFF	**Disabled** Enabled	See above.
DC00 - DFFF	**Disabled** Enabled	See above.

Note: In the Option column, bold shows default settings.

19.4 Advanced Menu

All entries in this part of the BIOS setup utility are very vital to your system. Change settings only if you are sure of what you are doing. Some changes may not be suitable for your complete system and may lead to unwanted system behavior.

Feature	Option	Description
▸ Advanced Chipset Control	Submenu	Opens Advanced Chipset Control submenu.
Plug & Play OS	Yes **No**	If your system has a PNP OS (e.g. Win95) select Yes to let the OS configure PNP devices not required for boot. No makes the BIOS configure them.
Reset Configuration Data	**No** Yes	Yes erases all configuration data in ESCD, which stores the configuration settings for plug-in devices. Select Yes when required to restore manufacturer defaults.
Secured Setup Configuration	**Yes** No	Yes prevents a Plug and Play OS from changing system settings.
▸ PCI Configuration	Submenu	Opens PCI Advanced submenu.
▸ Keyboard Features	Submenu	Opens Keyboard Features submenu.
▸ I/O Device Configuration	Submenu	Opens I/O Device Configuration submenu.
Large Disk Access Mode	**DOS** Other	Select DOS if you have DOS. Select Other if you have another OS such as UNIX. A large disk is one that has more than 1024 cylinders, more than 16 heads or more than 63 sectors per track.
Halt On Errors	**Yes** No	Determines if post errors cause the system to halt.

Notes: In the Option column, bold shows default settings.
Blue text shows possible differences to the older hardware revisions of the MOPSlcd6.

19.4.1. Advanced Chipset Control Submenu

Feature	Option	Description
AT bus clock frequency	7.16 MHZ **PCICLK/4** PCICLK/3	Allows to select ISA bus clock frequency. Some ISA devices might not work at PCICLK/3 (11 MHz)! The max. ISA Clock in Spec IEEE P996 is 8.33 MHz
Passive Release	**Disabled** Enabled	Enables more efficient ISA Bus master cycles to PCI.
Delayed Transaction	**Disabled** Enabled	Latches PCI-to-ISA cycles into buffer to free the PCI bus.
ISA Master Line Buffer	Disabled **Enabled**	Enables ISA master line buffer to enhance performance.
DMA Line Buffer	Disabled **Enabled**	Enables DMA line buffer to enhance performance.
PCI to ISA Posted Write Buffer	Disabled **Enabled**	Enables PCI to ISA posted write buffer.
16-bit ISA Memory Wait states	0, 1, **2**, 3	Inserts wait state for 16-bit memory command.
16-bit ISA I/O Wait states	0, 1, **2**, 3	Inserts wait state for 16-bit I/O command.
Enable Memory Gap	**Disabled** Conventional Extended	Turns system RAM of and frees address space (512kB-640kB or 15MB-16MB) for use with an option card.
CAS Latency	2 **3**	Select CAS Latency time.
SDRAM Timing	**3-6-9** 3-5-8 3-4-7 2-5-7	Controls RAS pre-charge timing in HCLKIN's. tRP – tRAS – tRC
Pipe Function	Disabled **Enabled**	Enables the asserting of NA (Next Address) when the cycle is a L2 or DRAM access cycle.
Primary Frame Buffer	Disabled, 1 MB, **2 MB**, 4 MB, 8 MB, 16 MB	Select the size of the primary frame buffer and enables Host to PCI write buffer.
VGA Frame Buffer	**Disabled** Enabled	Enables burst PCI cycles for VGA fixed frame buffer at A0000h – BFFFFh.
Data Merge	**Disabled** Enabled	If enabled, only the words which address are consecutive linear can be merged into one line.
Byte Merge	**Disabled** Enabled	Enables the byte-merge feature for frame buffer cycles
Fast Back to Back	**Disabled** Enabled	Enables PCI fast back-to-back capability.
PCI Write Burst	**Disabled** Enabled	Enables PCI write burst capability.
Parity Check	**Disabled** Enabled	If enabled, south bridge issues NMI to CPU when it detects the SERR assertion, IOCHK assertion and PCI bus parity error.

Notes: In the Option column, bold shows default settings.
Blue text shows possible differences to the older hardware revisions of the MOPSlcd6.

19.4.2. PCI Configuration Submenu

Feature	Option	Description
PCI IRQ line 1	Disabled **Auto Select** IRQ3, 4, 5, 7, 9, 10, 11, 12, 14,15	Select IRQ for PIC interrupt INTA. Select Auto to let BIOS assign IRQ.
PCI IRQ line 2	See above.	Select IRQ for PIC interrupt INTB. Select Auto to let BIOS assign IRQ.
PCI IRQ line 3	See above.	Select IRQ for PIC interrupt INTC. Select Auto to let BIOS assign IRQ.
PCI IRQ line 4	See above.	Select IRQ for PIC interrupt INTD. Select Auto to let BIOS assign IRQ.
USB IRQ line	See above.	Select IRQ for embedded USB device. Select Auto to let BIOS assign IRQ.
‣ PCI/PNP ISA UMB Region Exclusion	Submenu	Opens UMB Region Exclusion submenu.
‣ PCI/PNP ISA IRQ Resource Exclusion	Submenu	Opens IRQ Exclusion submenu.
ISA graphics device installed	**No** Yes	PCI devices may need to know if an ISA graphics device is installed in the system to enable card to function correctly.
Assign IRQ to PCI VGA	**Yes** No	Actually the onboard VGA does not need an IRQ assigned, but Win98 2nd Edition does not work correctly if an IRQ is not assigned.

Notes: In the Option column, bold shows default settings.
Use the IRQ Miniport driver for ALI M1543C south bridge (download from www.ali.com.tw) on systems that run Win95.

19.4.3. PCI/PNP ISA UMB Region Exclusion Submenu

Feature	Option	Description
C800 - CBFF	**Available** Reserved	Reserves block of upper memory for use by legacy ISA devices. Don't set this option to Reserved on the MOPSlcd6, which has a video BIOS up to CBFF. This option should only be used with the MOPS/686+ (without graphic)
CC00 - CFFF	**Available** Reserved	Reserves block of upper memory for use by legacy ISA devices.
D000 – D3FF	**Available** Reserved	Reserves block of upper memory for use by legacy ISA devices.
D400 – D7FF	**Available** Reserved	Reserves block of upper memory for use by legacy ISA devices.
D800 - DBFF	**Available** Reserved	Reserves block of upper memory for use by legacy ISA devices.
DC00 - DFFF	**Available** Reserved	Reserves block of upper memory for use by legacy ISA devices.

Note: In the Option column, bold shows default settings.

19.4.4. PCI/PNP ISA IRQ Exclusion Submenu

Feature	Option	Description
IRQ3	**Available** Reserved	Reserves specified IRQ for use by legacy ISA devices.
IRQ4	**Available** Reserved	Reserves specified IRQ for use by legacy ISA devices.
IRQ5	**Available** Reserved	Reserves specified IRQ for use by legacy ISA devices.
IRQ7	**Available** Reserved	Reserves specified IRQ for use by legacy ISA devices.
IRQ9	**Available** Reserved	Reserves specified IRQ for use by legacy ISA devices.
IRQ10	**Available** Reserved	Reserves specified IRQ for use by legacy ISA devices.
IRQ12	**Available** Reserved	Reserves specified IRQ for use by legacy ISA devices.
IRQ14	**Available** Reserved	Reserves specified IRQ for use by legacy ISA devices.
IRQ15	**Available** Reserved	Reserves specified IRQ for use by legacy ISA devices.

Note: In the Option column, bold shows default settings.

19.4.5. Keyboard Features Submenu

Feature	Option	Description
NumLock	**Auto** On Off	'On' or 'Off' turns NumLock on or off at bootup. Auto turns NumLock on if it finds a numeric keypad.
Key Click	**Disabled** Enabled	Turns audible key click on.
Keyboard auto-repeat rate	**30/sec**, 26.7/sec, 21.8/sec, 18,5/sec, 13.3/sec, 10/sec, 6/sec, 2/sec	Sets the number of times to repeat a keystroke per second if you hold the key down.
Keyboard auto-repeat delay	¼ sec, **½ sec**, ¾ sec, 1 sec	Sets the delay time before auto-repeat will start.

Note: In the Option column, bold shows default settings.

19.4.6. I/O Device Configuration Submenu

Feature	Option	Description
Local Bus IDE adapter	Disabled, **Enabled**	Enables onboard PCI IDE device.
Floppy disk controller	Disabled, **Enabled**	Enables onboard FDC controller.
Base I/O address	**Primary** Secondary	Selects base address of onboard FDC controller. (Primary = 3F0h, Secondary = 370)
Floppy Drive Swap	**Disabled,** Enabled	Swap drive A and B
Serial Port A Serial Port B	Disabled Enabled **Auto** OS Controlled	Disabled turns off the port. Enabled requires end user to enter the base I/O address and the IRQ. Auto makes the BIOS configure the port. OS Controlled lets the PNP OS configure the port after boot-up.
Serial Port C * Serial Port D *	**Disabled** Enabled Auto	Disabled turns off the port. Enabled requires end user to enter the base I/O address and the IRQ. Auto makes the BIOS configure the port.
Base I/O address	**3F8h, 2F8h**, 3E8h, 2E8h	Select I/O base of port.
IRQ (Port A and B)	**IRQ 3, IRQ 4**	Select IRQ of Port A and B
IRQ (Port C and D) *	IRQ 10, IRQ 11	Select IRQ of Port C and D
Mode *	**Normal,** IrDA, Ask-IR	Selects mode of Serial Port D.
IRDA Pins *	**Standard** Alternate	Selects which pins of the SMC669 to use for the IrDA interface.
Parallel Port	Disabled Enabled **Auto** OS Controlled	Disabled turns off the port. Enabled requires end user to enter the base I/O address and the IRQ. Auto makes the BIOS configure the port. OS Controlled lets the PNP OS configure the port after boot-up.
Mode	Output only, **Bi-directional,** ECP, EPP	Set mode for the parallel port.
Base I/O address	**378h**, 278h, 3BCh	Select I/O base of port.
IRQ	IRQ 5, **IRQ 7**	Select IRQ of parallel port.
DMA	**DMA0**, 1, 2, 3	Select DMA channel of port if in ECP mode.
USB Host Controller	**Disabled,** Enabled	Enable or Disable onboard USB controller.
USB BIOS Legacy Support **	**Disabled** Enabled	Enable or Disable support for USB keyboard and mice. Please enable only for use with non-USB aware OSes such as UNIX and DOS.
OHCI Registers at ***	**E0000h**, D0000h	Choose the memory location address where the 16K block for the OHCI registers starts.
‣ Watchdog Settings	Submenu	Opens Watchdog Settings sub menu

Notes: In the Option column, bold shows default settings.
(*)These options are only visible if an additional I/O controller (SMSC669) is on the OEM backplane.
(**) If USB legacy support is enabled, the USB OHCI controller uses IRQ12. If you run a system with Win9x and without a mouse attached, set IRQ12 to reserved in the PCI/PNP ISA IRQ Exclusion submenu to prevent Win9x from allocating IRQ12 to PCI devices.
(***) Available since BIOS version P588R141

19.4.7. Watchdog Settings Submenu

Feature	Option	Description
Mode	**Disabled** Reset NMI	Select watchdog operation mode.
Delay	1s, 5s, 10s, **30s**, 1min, 5min,10min, 30min	The time until the watchdog counter starts counting. Useful to handle longer boot times.
Timeout	1s, 5s, 10s, **30s**, 1min, 5min, 10min	Max. trigger period.

Notes: In the Option column, bold shows default settings.
Blue text shows possible differences to the older hardware revisions of the MOPSlcd6.

19.5 *Security Menu*

Feature	Option	Description
Set Supervisor Password *	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives full access to setup.
Set User Password *	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives restricted access to setup.
Password on boot	**Disabled** Enabled	Enabled requires a password on boot. Requires prior setting of the supervisor password. If supervisor password is set and this option is disabled, BIOS assumes user is booting.
Fixed disk boot sector	**Normal** Write-protected	Write protect the boot sector on the hard disk for virus protection. Requires a password to format or Fdisk the hard disk.
Diskette access	User **Supervisor**	Enabled requires supervisor password to access floppy disk.

Notes: In the Option column, bold shows default settings.
(*) Enabling “Set Supervisor Password” requires a password for entering Setup.
Passwords are not case sensitive. User and Supervisor passwords are related.
You cannot have a User password without first creating a Supervisor password.

19.6 *Power Menu*

A power management system reduces the amount of energy used after specified periods of inactivity. The setup menu supports a **Full On** state, a **Standby** state with partial power reduction, and a **Suspend** state with full power reduction.
Use the Advanced Options sub menu to specify whether or not an activity can terminate a Standby or Suspend state and restore Full On.

Selecting „Power" from the menu bar displays this menu:

Feature	Option	Description
Power Savings	**Disabled** Customized Maximum Power Saving Maximum Performance	Maximum options select predefined values. Select Customized to make selections from the following fields. Disabled turns off all power management.
Standby Timeout	**Off**, 1min, 2min, 4min, 6min, 8min, 12min, 16min	Inactivity period required to put system in Standby mode (partial power shutdown).
Auto Suspend Timeout	**Off**, 5min, 10min, 15min, 20min, 30min, 40min, 60min	Inactivity period required after Standby to Suspend mode (maximum power shutdown).
Hard Disk Timeout	**Disabled**, 10 sec – 15 min	Inactivity period of hard disk required before standby (motor off).
‣ Advanced Options	Submenu	Opens advanced options submenu.
LCD Backlight Off Timer	**Disabled**, 28 sec – 14 min	If enabled, backlight is switched off after the selected period of time without video activity.

Note: In the Option column, bold shows default settings.

19.6.1. Advanced Options Submenu

Feature	Option	Description
Video IO	Yes **No**	Wakes up system on video event
Primary HDD	Yes **No**	Wakes up system on primary HDD event.
Floppy Disk Drive	Yes **No**	Wakes up system on FDD event.
Serial I/O	**Yes** No	Wakes up system on serial I/O event.
Parallel I/O	Yes **No**	Wakes up system on parallel I/O event.
Keyboard	**Yes** No	Wakes up system on keyboard event.
RTC	Yes **No**	Wakes up system on RTC alarm.

Note: In the Option column, bold shows default settings.

19.6.2. Monitored Events

Video IO	3B0h – 3DF I/O and A/B segment memory
Primary HDD	1F0h – 1F7h and 3F6h I/O access, primary IDE channel DMA request
Secondary HDD	170h – 177h and 376h I/O access, secondary IDE channel DMA request
FDD	3F0h – 3F7h I/O access
Serial I/O	3F8h – 3FFh, 2F8h – 2FFh, 3E8h – 3EFh, 2E8h – 2EFh, 338h – 33Fh, 238h – 23Fh
Parallel I/O	378h – 37Fh, 278h – 27Fh, 3BCh – 3BEh
Keyboard	60h and 64h I/O access

The following events also wakes the system from suspend state:

- IRQ[1-7], IRQ[9-15], NMI, SMI, INIT
- RTC IRQ 8

19.7 *Boot Menu*

Feature	Option	Description
Floppy Check	**Disabled** Enabled	Enabled verifies floppy type on boot. Disabled speeds up boot.
Summary Screen	**Disabled** Enabled	If Enabled, a summary screen is displayed just before booting the OS to let the end user see the system configuration.
QuickBoot Mode	Disabled **Enabled**	Allows the system to skip certain tests while booting. This will decrease the time needed to boot the system.
Dark Boot	**Disabled** Enabled	If Enabled, system comes up with a blank screen instead of the diagnostic screen during bootup.
▸ Boot Device Priority	Submenu	Opens boot device priority submenu
Onboard LAN RPL ROM	**Disabled** Enabled	Enables Remote Program Load ROM of the onboard LAN controller. Supports Intel PXE.

Note: In the Option column, bold shows default settings.

19.7.1. Dark Boot

After you turn on or reset the computer, Dark Boot displays a graphical logo (default is a blank screen) instead of the text based POST screen, which displays a number of PC diagnostic messages.

The graphical logo stays up until just before the OS loads unless:

- You press **Esc** to display the POST screen
- You press **F2** to enter Setup
- POST issues an error message
- The BIOS or an option ROM requests keyboard input

19.7.2. Boot Device Priority Submenu

Feature	Option	Description
▸ Removable Devices	Boot priority and submenu.	Sets boot priority of Removable Devices as described in the respective submenu.
▸ Hard Drive	Boot priority and submenu.	Sets boot priority of Hard Disks as described in the respective submenu.
CD-ROM Drive	Boot priority	Sets boot priority of ATAPI CD ROM Drives.
▸ Network Boot	Boot priority and submenu.	Sets boot priority of Network Adapters as described in the respective submenu.

This menu allows you to select the order of the devices from which BIOS attempts to boot the OS. If BIOS is unsuccessful at booting from one device, during POST it will try the next one on the list.

The items on this menu each may represent the first of a class of items. For example, if you have more than one hard-disk drive, Hard Drive represents the first of such drives as specified in the Hard-Drive menu described below.

To change the order, select the device you want to change and press **<->** to decrease or **<+>** to increase priority.

Removable Devices Priority Subentries

If you have more than one Removable Media drive, select Removable Devices and press **<Enter>** to display the Removable Media devices and choose which drive is represented in boot-order menu.

Note: The standard 1.44MB floppy drive is referenced as “Legacy Floppy Drives.”

Hard Drive Priority Subentries

If you have more than one bootable hard drive, select Hard Drive and press **<Enter>** to display the Fixed Disk Menu and choose the boot priority.

Network Boot Priority Subentries

If you have more than one bootable network adapter in the system, select **Network Boot** and press **<Enter>** to display the available network adapters and choose boot priority. Normally there is only one bootable network adapter in the system and no submenu is available.

19.8 *MultiBoot*

MultiBoot expands your boot options by letting you choose your boot device such as:

- Hard disk
- Floppy disk
- CD-ROM
- Network card

You can select your boot device in the Setup as described above, or you can choose a different device each time you boot by selecting your boot device in the **Boot First Menu**.

19.8.1. Boot First Menu

Display the **Boot First Menu** by pressing **<Esc>** during POST. In response, the BIOS first displays the message "Entering Boot Menu..." and then displays the **Boot Menu** at the end of POST.

Use the menu to select any of these options:

- Override the existing boot sequence (for this boot only) by selecting another boot device. If the specified device does not load the OS, BIOS reverts to the previous boot sequence.
- Enter Setup
- Press **<Esc>** to continue with the existing boot sequence.

19.9 Exit Menu

Feature	Option	Description
Exit Saving Changes	Saves selections and exits setup. The next time the system boots, the BIOS configures the system according to the Setup selection stored in CMOS.	Exit saving changes.
Exit Discarding Changes	Exits Setup without storing in CMOS any new selections you may have made. The selections previously in effect remain in effect.	Exit discarding changes.
Load Setup Defaults	Displays default values for all the Setup menus.	Load setup defaults.
Discard Changes	If, during a Setup session, you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you saved to CMOS.	Discard changes.
Save Changes	Saves all the selection without exiting Setup. You can return to the other menus to review and change your selection.	Save changes.

Note: In the Option column, bold shows default settings.

19.10 *Kontron BIOS Extensions*

Besides the Phoenix System BIOS, the MOPSlcd6 comes with a few BIOS extensions that support special features. All extensions are located in the onboard flash EEPROM. Some extensions are permanently available; some are loaded if required during boot up. Supported features include:

- JIDA standard
- Remote Control feature (JRC)
- Onboard LAN RPL ROM

All enabled BIOS extensions require shadow RAM. They will be loaded into the same 16K shadowed memory block, if possible. However, if the system memory cannot find free memory space because all the memory is already used for add-on peripherals, the BIOS extensions do not load.

19.10.1. JIDA BIOS extension

The JUMPtec Intelligent Device Architecture (JIDA) BIOS extension is not a true extension BIOS. It is part of the system BIOS and is located in the system BIOS segments after boot up. It is permanently available and supports the JIDA 16-bit standard. It is a software interrupt 15hex driven programmers interface and offers lots of board information functions. For detailed information about programming, refer to the JIDA specification and a source code example (JIDAI???.ZIP), which you can find at the Kontron Web site. The three question marks represent the revision number of the file. You also can contact technical support for this file.

For other operating systems, special drivers (JIDAIA??.ZIP) are available. You can download the zip file from the Kontron Web site.

19.10.2. Remote Control Client Extension

You can remotely control the MOPSlcd6 using software available from Kontron (JRC-1, Part Number 96047-0000-00-0). This software tool can communicate with the board via one of the serial ports. During boot up of the MOPSlcd6 , the system BIOS scans the serial ports for an available JRC connection. If detected, it loads the JRC client BIOS extension into the memory. With the JRC client loaded into the first detected free memory location between C0000hex and D8000hex, a 16K block is shadowed.

For more information on the Remote Control usage, refer to the JRC-1 technical manual or Application Note JRCUsage_E???.PDF, which you can find on the Kontron Web site.

19.10.3. LAN RPL ROM

If the onboard LAN RPL ROM is enabled in the system BIOS setup, a special optional ROM for the Ethernet controller loads into memory during boot up. This optional ROM allows you to boot the MOPSlcd6 over an Ethernet connection. A server with Intel PXE/RPL boot support is required on the other side of the Ethernet connection. The setup and configuration of the server, including PXE/RPL support, is not the responsibility of Kontron.

The RPL ROM extension is loaded into the first free memory area between C0000hex and D8000hex and a 16K block of memory is shadowed.

19.11 *Updating or Restoring BIOS*

If your MOPSlcd6 board requires a newer BIOS version or the BIOS is damaged, you may need to update or restore the BIOS.

Phoenix PHLASH allows you to update or restore the BIOS with a newer version or restore a corrupt BIOS by using a floppy disk without having to install a new ROM chip.

1) Download Phoenix Phlash as a compressed file, CRD1P58R.ZIP, from the Kontron Web site. It contains the following files:

File	Purpose
MAKEBOOT.EXE	Creates the custom boot sector on the Crisis Recovery Diskette.
CRISBOOT.BIN	Serves as the Crisis Recovery boot sector code.
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH.EXE	Programs the Flash ROM.
WINCRISIS.EXE	Creates the Crisis Recovery Diskette from Windows.
WINCRISIS.HLP	Serves as the help file of WINCRISES.EXE.
PLATFORM.BIN	Performs platform-dependent functions.
BIOS.ROM	Serves as the actual BIOS image to be programmed into Flash ROM.

2) To install Phoenix Phlash on a hard disk, unzip the content CRD1P58R.ZIP into a local directory such as C:\PHLASH.

3) To create a Crisis Recovery Diskette, insert a blank diskette into Drive A: or B: and execute WINCRISIS.EXE. This copies four files onto the Crisis Recovery Diskette.

File	Purpose
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH.EXE	Programs the Flash ROM.
PLATFORM.BIN	Performs platform-dependent functions.
BIOS.ROM	Serves as the BIOS image to be programmed into Flash ROM.

4) If the BIOS image (BIOS.ROM) changes because of an update or bug fix, copy the new BIOS.ROM image onto the diskette.

19.11.1. Running Phoenix Phlash

You can run Phoenix Phalsh in one of two modes:

- Command Line
- Crisis Recovery

Phlash can fail if the system uses memory managers. If this occurs, the utility displays this message:

```
Cannot flash when memory managers are present.
```

If you see this message after you execute Phlash, disable the memory manager.

19.12 *Preventing Problems When Updating or Restoring BIOS*

Updating the BIOS represents a potential hazard. Power failures or fluctuations that can occur during updating the Flash ROM can damage the BIOS code, making the system unbootable.

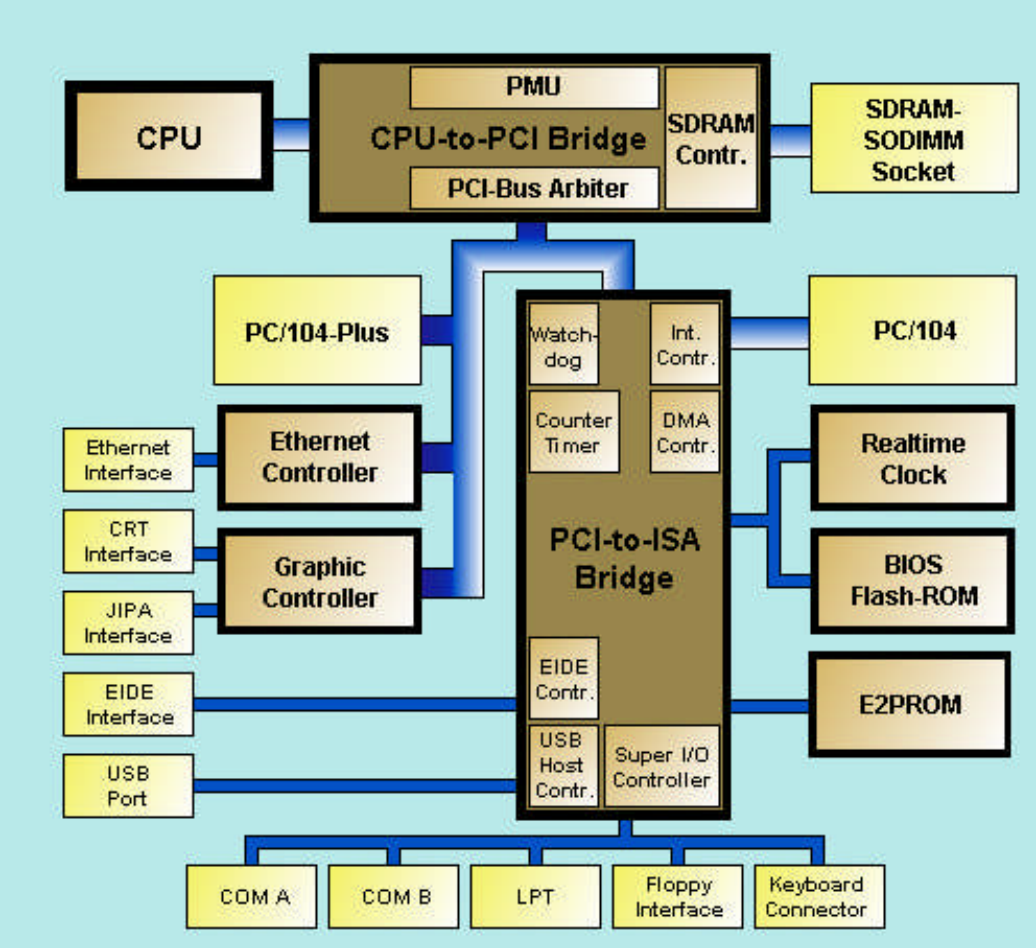
To prevent this potential hazard, many systems come with a boot-block Flash ROM. The boot-block region contains a fail-safe recovery routine. If the boot-block code finds a corrupted BIOS (checksum fails), it boots into the crisis recovery mode and loads a BIOS image from a crisis diskette (see above).

Additionally, the end user can insert an update key into the parallel port (LPT1 only) to force initiating the recovery routine for the boot block.

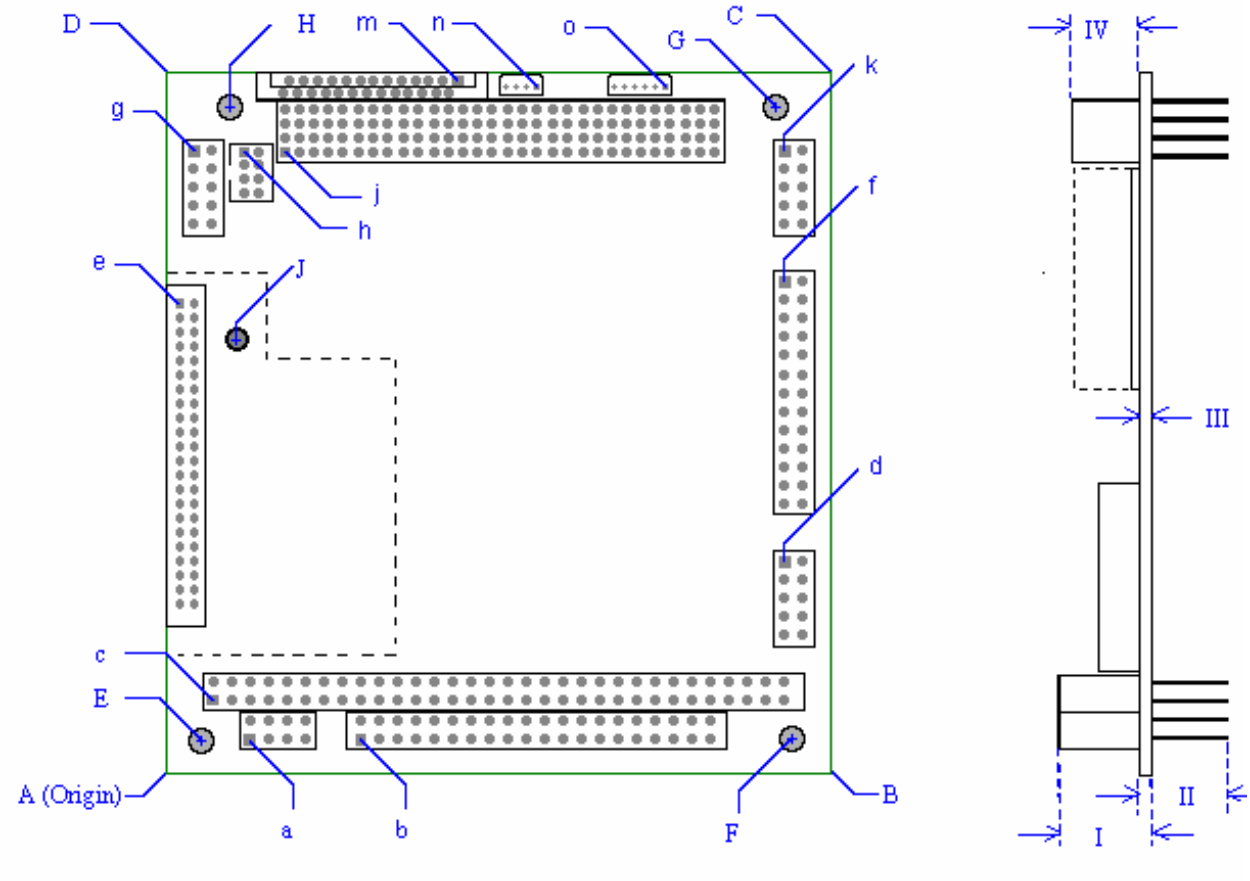
For further information on the update key and the crisis diskette, see a special application note (PHLASH_SC_E???.PDF), which is available from the Kontron Web site. (The three question marks indicate the revision number of the document.)

Note:	The file BIOS.ROM on the crisis recovery disk may not be the latest version of the ROM file. Contact Kontron technical support for the latest version. Do not flash a BIOS ROM file if you are not sure it matches your hardware because the system might become unbootable. Kontron is not obligated to recover your system free of charge if the board does not boot because flash tools were used incorrectly.

20. APPENDIX C: BLOCK DIAGRAM



21. APPENDIX D: MECHANICAL DIMENSIONS



All Dimensions in the tables below are relative to the origin location A.

Location	Horizontal (mm)	Vertical (mm)	Horizontal (mil)	Vertical (mil)
PCB Dimensions				
A (Origin)	0	0	0	0
B	90.17	0	3550	0
C	90.17	95.89	3550	3775
D	0	95.89	0	3775
Mounting Holes				
E	5.08	5.08	200	200
F	85.09	5.08	3350	200
G	82.55	90.81	3250	3575
H	8.89	90.81	350	3575
J	9.88	59.28	389	2333.84

Location	Horizontal (mm)	Vertical (mm)	Horizontal (mil)	Vertical (mil)
Interface Connectors				
a	11.43	5.08	450	200
b	26.67	5.08	1050	200
c	6.35	10.16	250	400
d	83.54	29.24	3289	1151
e	1.75	64.80	69	2551
f	83.54	67.34	3289	2651
g	4.04	85.12	159	3351
h	10.69	84.99	421	3346
j	16.51	84.81	650	3338.78
k	83.54	85.12	3289	3351
m	40.54	94.89	1596	3736
n	50.80	93.73	2000	3690
o	67.95	93.73	2675	3690

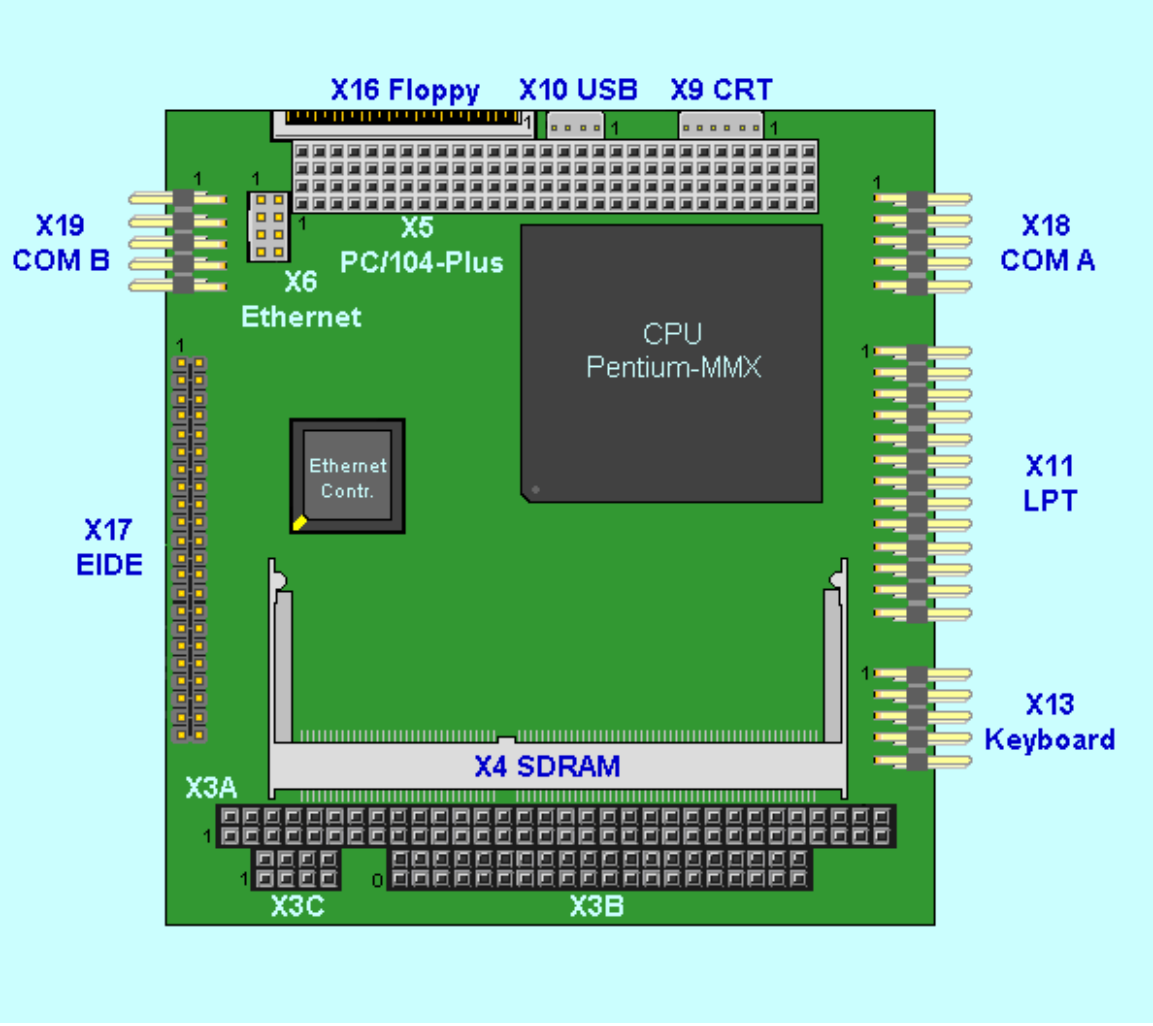
Height	Dimension (mm)	Dimension (mil)
I	13.10	515
II	10.40	410
III	1.52	60
IV	9.35	368

22. APPENDIX E: CONNECTOR LAYOUT

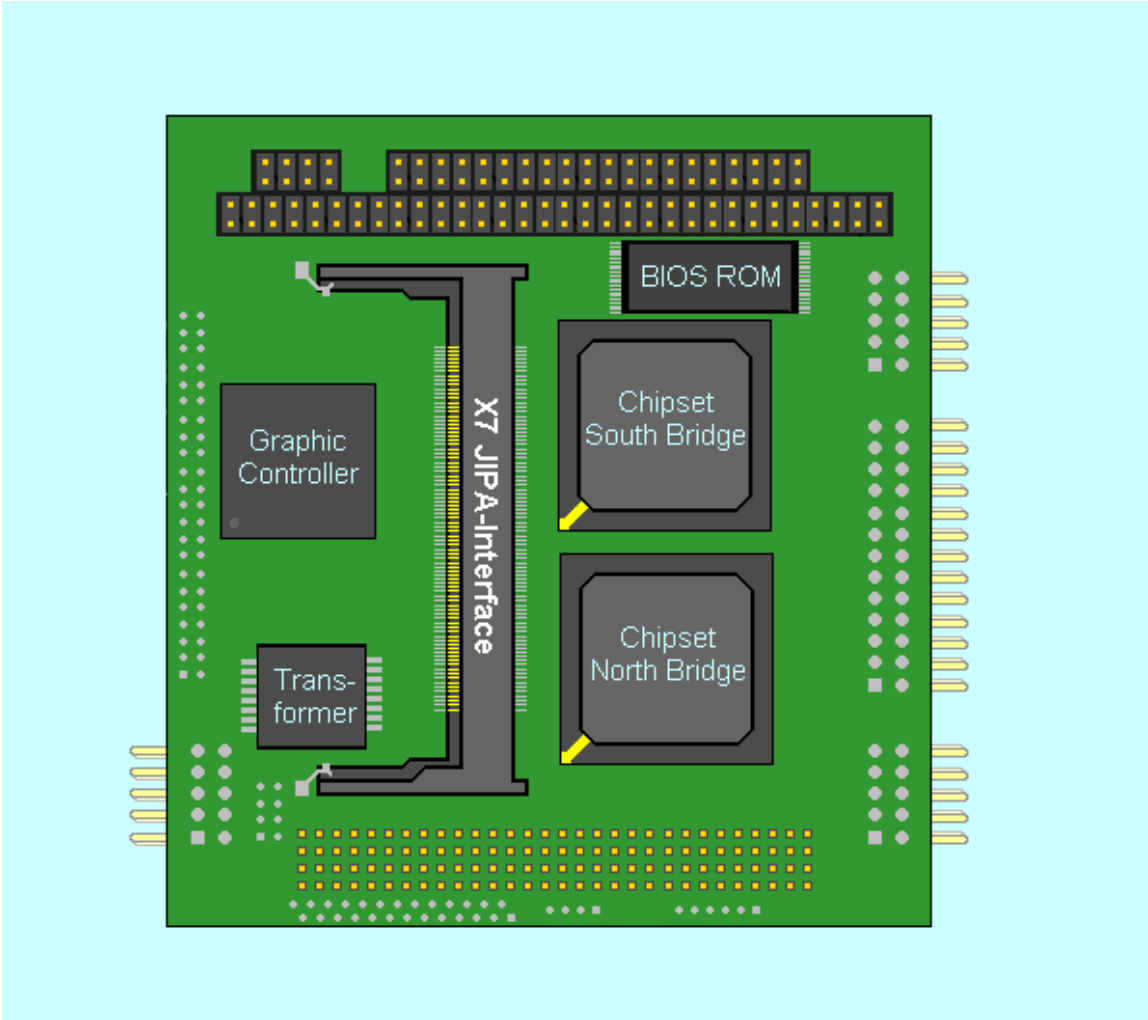
22.1 *Connector Locations*

Pin 1 of any connector is marked with "1" in this drawing and with a rectangular pad at the bottom side of the board's PCB.

22.1.1. Top Overlay



22.1.2. Bottom Overlay



22.2 Connector Functions and Interface Cables

The table notes connector functions, as well as mating connectors and available cables.

Connector	Function	Mating Connector	Available Cable	Cable Description
X3A	PC/104 Bus (XT-Bus part)	2.54mm 64 pos. (EPT 962-60323-12 or compatible for board to board connection)		
X3B	PC/104 Bus (AT-Bus part)	2.54mm 40 pos. (EPT 962-60203-12 or compatible for board to board connection)		
X3C	Power Connector	2.54mm 8 pos. (EPT 962-60043-12 or compatible for board to board connection)		
X4	SDRAM	-	-	-
X5	PC/104-Plus Bus (PCI part)	2mm 120pos. (EPT 264-60303-12)		
X6	Ethernet Interface Connector	2mm 8 pos. (Berg 90311-008 or compatible)	KAB-MOPS-ETN1 (PN 96048-0000-00-0)	For RJ45 adaptation.
X7	Display	-	KAB-JIPA-?????	Kontron JIPA cables
X9	CRT-Monitor	1.25mm 6 pos. (Molex 51021-0600 or compatible)	KAB-VGA-2 (PN 96053-0000-00-0)	For DSUB 15 adapt ion
X10	USB interface connector	1.25mm 4 pos. (Molex 51021-0400 or compatible)	KAB-USB-1 (PN 96054-0000-00-0)	For standard USB adoption
X11	Parallel Interface LPT Connector	2.54mm 26 pos. (AMP 2-215882-6 or compatible)	KAB-DSUB25-1 (PN 96015-0000-00-0)	For DSUB 25 adaptation.
X13	Keyboard and Feature Connector	2.54mm 10 pos. (AMP 1-215882-0 or compatible)	KAB-KB-1 (PN 96023-0000-00-0) or KAB-KB-PS2 (PN 96060-0000-00-0)	For AT-keyboard or PS/2 keyboard.
X16	Floppy Drive Interface Connector		ADA-FLOPPY-2 (PN 96001-0000-00-0) or KAB-FLOPPY/MOPS-1 (PN 96019-0000-00-0)	For 3.5” floppy or Slim-line floppy.
X17	IDE Hard Disk Interface Connector	2mm 44 pos. (Berg 89361-144 or compatible)	KAB-IDE-25 (PN 96020-0000-00-0) or KAB-IDE-2MM (PN 96021-0000-00-0)	For 3.5” HDD Or 2.5” HDD
X18, X19	Serial Interfaces COM A and COM B Connectors	2.54mm 10 pos. (AMP 1-215882-0 or compatible)	KAB-DSUB9-2 (PN 96017-0000-00-0)	For DSUB 9 adaptation.

22.3 Pinout Table

Pin	PC104 (A)	PC104 (B)	PC104 (C)	PC104 (D)	PC/104 Plus (A)	PC/104 Plus (B)	PC/104 Plus (C)	PC/104 Plus (D)
0			GND	GND				
1	/IOCHCK	GND	/SBHE	/MEMCS16	GND	Reserved	VCC (***)	AD00
2	SD7	RESETDRV	LA23	/IOCS16	VCC (***)	AD02	AD01	AD03
3	SD6	VCC (***)	LA22	IRQ10	AD05	GND	AD04	AD03
4	SD5	IRQ9	LA21	IRQ11	C/BE0	AD07	GND	AD06
5	SD4	-5V	LA20	IRQ12	GND	AD09	AD08	GND
6	SD3	DRQ2	LA19	IRQ15	AD11	VCC (***)	AD10	GND
7	SD2	-12V	LA18	IRQ14	AD14	AD13	GND	AD12
8	SD1	/0WS	LA17	/DACK0	VCC3 (**)	C/BE1	AD15	VCC3 (**)
9	SD0	+12V	/MEMR	DRQ0	SERR	GND	SB0	PAR
10	IOCHRDY	GND (*)	/MEMW	/DACK5	GND	PERR	VCC3 (**)	SDONE
11	AEN	/SMEMW	SD8	DRQ5	STOP	VCC3 (**)	LOCK	GND
12	SA19	/SMEMR	SD9	/DACK6	VCC3 (**)	TRDY	GND	DEVSEL
13	SA18	/IOW	SD10	DRQ6	FRAME	GND	IRDY	VCC3 (**)
14	SA17	/IOR	SD11	/DACK7	GND	AD16	VCC3 (**)	C/BE2
15	SA16	/DACK3	SD12	DRQ7	AD18	VCC3 (**)	AD17	GND
16	SA15	DRQ3	SD13	VCC (***)	AD21	AD20	GND	AD19
17	SA14	/DACK1	SD14	/MASTER	VCC3 (**)	AD23	AD22	VCC3 (**)
18	SA13	DRQ1	SD15	GND	IS0 (AD20)	GND	IS1 (AD21)	IS2 (AD22)
19	SA12	/REFRESH	GND	GND	AD24	C/BE3	VI/O	IS3 (AD23)
20	SA11	SYSCLK			GND	AD26	AD25	GND
21	SA10	IRQ7			AD29	VCC (***)	AD28	AD27
22	SA9	IRQ6			VCC (***)	AD30	GND	AD31
23	SA8	IRQ5			REQ0	GND	REQ1	VI/O
24	SA7	IRQ4			GND	REQ2	VCC (***)	GNT0
25	SA6	IRQ3			GNT1	VI/O	GNT2	GND
26	SA5	/DACK2			VCC (***)	CLK0	GND	CLK1
27	SA4	T/C			CLK2	VCC (***)	CLK3	GND
28	SA3	BALE			GND	INTD	VCC (***)	RST
29	SA2	VCC (***)			+12V	INTA	INTB	INTC
30	SA1	OSC			-12V	Reserved	Reserved	Reserved
31	SA0	GND						
32	GND	GND						

Notes:
(*) - Key pin for PC/104; GND for PC/104+ specification
(**) - Not supported on MOPSlcd6 boards.
(***) - To protect the external power lines of peripheral devices, make sure that:
- the wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

Pin	IDE	Floppy	LPT	Power	COM A	COM B
1	/RESET	VCC (***)	/STB	GND	/DCD1	/DCD2
2	GND	/IDX	/AFD	VCC (***)	/DSR1	/DSR2
3	HDD7	VCC (***)	PD0	BATT	RXD1	RXD2
4	HDD8	/DR0	/ERR	+12V	/RTS1	/RTS2
5	HDD6	VCC (***)	PD1	-5V	TXD1	TXD2
6	HDD9	/DSKCHG	/INIT	-12V	/CTS1	/CTS2
7	HDD5	VCC (***)	PD2	GND	/DTR1	/DTR2
8	HDD10	NC	/SLIN	VCC (***)	/RI1	/RI2
9	HDD4	NC	PD3		GND	GND
10	HDD11	/MTR0	GND		VCC (***)	VCC (***)
11	HDD3	NC	PD4			
12	HDD12	/FDIR	GND			
13	HDD2	NC	PD5			
14	HDD13	/STEP	GND			
15	HDD1	GND	PD6			
16	HDD14	/WDATA	GND			
17	HDD0	GND	PD7			
18	HDD15	/WGATE	GND			
19	GND	GND	/ACK			
20	KEY (NC)	/TRK0	GND			
21	DRQ	GND	/BUSY			
22	GND	/WRTPRT	GND			
23	/IOW	GND	PE			
24	GND	/RDATA	GND			
25	/IOR	GND	/SLCT			
26	GND	/HDSEL	VCC (***)			
27	IOCHRDY					
28	NC (*)					
29	AKJ					
30	GND					
31	SIRQ					
32	NC					
33	SA1					
34	NC					
35	SA0					
36	SA2					
37	/CS1					
38	/CS3					
39	NC					
40	GND					
41	VCC (***)					
42	VCC (***)					
43	GND					
44	NC					

Notes:
(*) – Pin normally used as cable select. On MOPSlcd6 it is not connected.
(***) - To protect the external power lines of peripheral devices, make sure that:
- the wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

Pin	KBD	LAN	USB
1	SPKR	TXD+	VCC (***)
2	GND	TXD-	USB00
3	/RESIN	RXD+	USB01
4	/KBLOCK	SHLDGND	GND
5	KBDAT	SHLDGND	
6	KBCLK	RXD-	
7	GND	SHLDGND	
8	VCC (***)	SHLDGND	
9	BATT		
10	PWRGOOD		

Notes:
(***) - To protect the external power lines of peripheral devices, make sure that:
- the wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

23. APPENDIX F: PC ARCHITECTURE INFORMATION

The following sources of information can help you better understand PC architecture.

23.1 *Buses*

23.1.1. ISA, Standard PS/2 - Connectors

- AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- AT IBM Technical Reference Vol 1&2, 1985
- ISA & EISA Theory and Operation, Edward Solari, Annabooks, 1992, ISBN 0929392159
- ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel
- ISA System Architecture, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989

23.1.2. PC/104, PCI - Information

- Embedded PC 104 Consortium
  The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.
- PCI SIG
  The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.
- *PCI & PCI-X Hardware and Software Architecture & Design*, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- *PCI System Architecture,* Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

23.2 General PC Architecture

- *Embedded PCs*, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- *Hardware Bible*, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- *Interfacing to the IBM Personal Computer*, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- *The Indispensable PC Hardware Book*, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9
- *The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition*, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

23.3 Ports

23.3.1. RS-232 Serial

- EIA-232-E standard
  The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.
- *RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems*, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3
- National Semiconductor
  The Interface Data Book includes application notes. Type “232” as a search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor’s Web site.

23.3.2. ATA

AT Attachment (ATA) Working Group
This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web.
We recommend you also search the Web for information on 4.2 I/O cable, if you use hard disks in a DMA3 or PIO4 mode.

23.3.3. USB

USB Specification
USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

23.4 *Programming*

- *C Programmer's Guide to Serial Communications*, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0
- *Programmer's Guide to the EGA, VGA, and Super VGA Cards*, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4
- *The Programmer's PC Sourcebook,* Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X
- *Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas*, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

24. APPENDIX G: DOCUMENT-REVISION HISTORY

Revision	Date	Edited by	Changes
P588M140	03.03.2003	WKA	Created preliminary for new HW Rev.; kill JUMPtec ☹; delete all „power through MOPS as an backplane mistakes by CE and UL considerations.
P588M141	13.02.2004	HB and JL	Updated manual throughout. Added new BIOS features. Changes for new layout. Reformatted manual.
P588M142	11.10.2004	BHO	Corrected USB mating connector information, added setup entry for OHCI memory map, corrected measurements of mounting hole H, updated technical support addresses, added PCI device configuration, minor layout changes, completed I/O address map
P588M143	07.09.2005	BHO	Added Ethernet note, changed update key for BIOS to LPT, changed connector drawings, minor changes