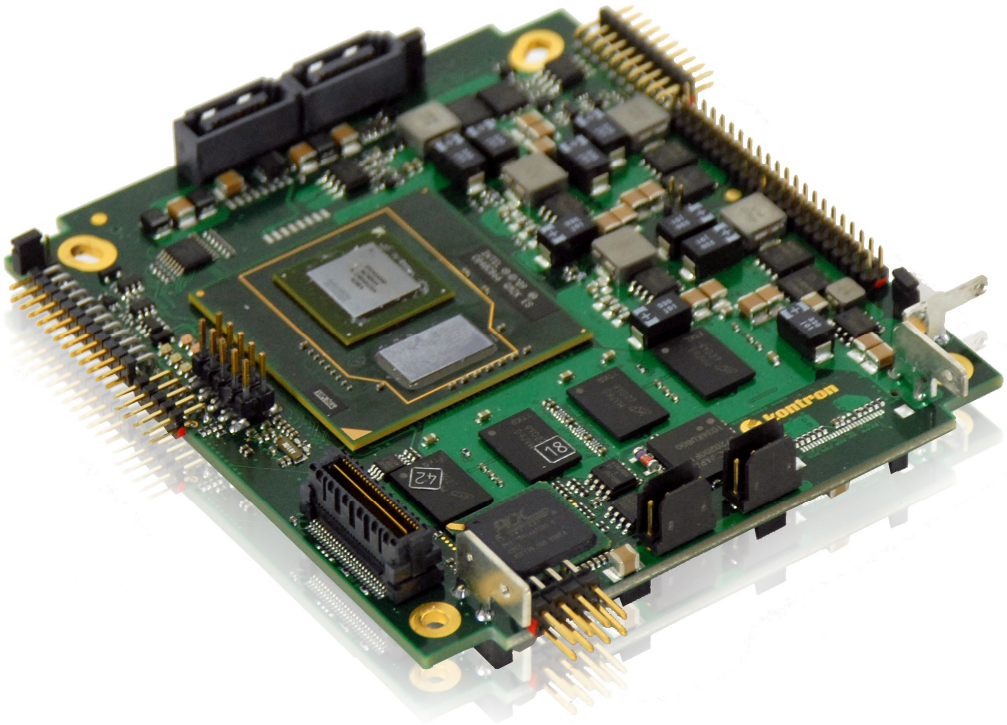
» Kontron User's Guide «



MSMST

Document Revision 109

» Table of Contents «

1 User Information

1.1 About this Document

This document provides information about products from Kontron AG and/or its subsidiaries. No warranty of suitability, purpose, or fitness is implied. While every attempt has been made to ensure that the information in this document is accurate, the information contained within is supplied "as is" and is subject to change without notice.

1.2 Copyright Notice

1.3 Trademarks

MICROSPACE®, smartModule® and smartCore® are trademarks or registered trademarks of Kontron Compact Computers AG. Kontron is a trademark or registered trademark of Kontron AG.

The following lists the trademarks of components used in this product.

- IBM, XT, AT, PS/2 and Personal System/2 are trademarks of International Business Machines Corp.
- Microsoft is a registered trademark of Microsoft Corp.
- Intel is a registered trademark of Intel Corp.

All other products and trademarks mentioned in this manual are trademarks of their respective owners. For the circuits, descriptions and tables indicated, Kontron assumes no responsibility as far as patents or other rights of third parties are concerned.

1.4 Standards

Kontron AG is certified to ISO 9000 standards.

1.5 Warranty

This Kontron AG product is warranted against defects in material and workmanship for the warranty period from the date of shipment. During the warranty period, Kontron AG will, at its discretion, decide to repair or replace defective products.

Within the warranty period, the repair of products is free of charge as long as warranty conditions are observed.

The warranty does not apply to defects resulting from improper or inadequate maintenance or handling by the buyer, unauthorized modification or misuse, operation outside of the product's environmental specifications or improper installation or maintenance.

Kontron AG will not be responsible for any defects or damages to other products not supplied by Kontron AG that are caused by a faulty Kontron AG product.

Empty batteries (external and onboard), as well as all other battery failures, are not covered by this manufacturer's limited warranty.

1.6 Technical Support

Technicians and engineers from Kontron AG and/or its subsidiaries are available for technical support. We are committed to making our products easy to use and will help you use our products in your systems.

For technical support, please consult our technical support department:

Web: http://support.kcc-ag.ch
Tel.: +41 (0) 32 681-5848
Fax: +41 (0) 32 681-5801

For the latest product documentation, utilities, drivers, additional tools and software please consult our website:

Web: http://kontron.com

1.7 Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements wherever possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations. All components within this product fulfill the requirements of the RoHS (Restriction of Hazardous Substances Directive). The product is soldered using a lead-free process.

1.8 RoHS Commitment

Kontron Compact Computers AG (Switzerland) is committed to developing and producing environmentally friendly products in accordance with the Restriction of Hazardous Substances (RoHS) Directive (2002/95/EC) and the Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) established by the European Union. The RoHS directive was adopted in February 2003 by the European Union and came into effect on 1 July 2006. It is not a law but a directive, which restricts the use of six hazardous materials in the manufacturing of various types of electronic and electrical equipment. It is closely linked with the Waste Electrical and Electronic Equipment Directive (WEEE) 2002/96/EC, which has set targets for the collection, recycling and recovery of electrical goods, and is part of a legislative initiative to solve the problem of huge amounts of toxic e-waste.

Each European Union Member State is adopting its own enforcement and implementation policies using the Directive as a guide. Therefore, there could be as many different versions of the law as there are Member States in the EU. Additionally, non-EU countries like China, Japan, or states in the U.S. such as California, may have their own regulations for green products, which are similar, but not identical, to the RoHS Directive.

RoHS is often referred to as the "lead-free" directive, but it restricts the use of the following substances:

- Lead
- Mercury
- Cadmium
- Chromium VI
- PBB and PBDE

The maximum allowable concentration of any of the above-mentioned substances is 0.1% (except for cadmium, which is limited to 0.01%) by weight of homogeneous material. This means that the limits do not apply to the weight of the finished product, or even to a component, but to any single substance that could (theoretically) be separated mechanically.

1.8.1 RoHS Compatible Product Design

All standard products from Kontron Compact Computers (KCC) AG comply with RoHS legislation.

Since July 1, 2006, there has been a strict adherence to the use of RoHS compliant electronic and mechanical components during the design-in phase of all KCC AG standard products.

1.8.2 RoHS Compliant Production Process

KCC selects external suppliers that are capable of producing RoHS compliant devices verified by:

- A confirmation from the supplier indicating that their production processes and resulting devices are RoHS compliant.
- If there is any doubt of RoHS compliancy, the concentration of the previously mentioned substances in a produced device will be measured. These measurements are carried out by an accredited laboratory.

1.8.3 WEEE Application

The WEEE Directive is closely related to the RoHS Directive and applies to the following devices:

- Large and small household appliances
- IT equipment
- Telecommunications equipment (although infrastructure equipment is exempt in some countries)
- Consumer equipment
- Lighting equipment – including light bulbs
- Electronic and electrical tools
- Toys, leisure and sports equipment
- Automatic dispensers

It does not apply to fixed industrial plants and tools. Compliance is the responsibility of the company that brings the product to market, as defined in the Directive. Components and sub-assemblies are not subject to product compliance. In other words, since Kontron Compact Computers AG does not deliver ready-made products to end users, the WEEE Directive is not applicable for KCC AG. Users are nevertheless encouraged to properly recycle all electronic products that have reached the end of their life cycle.

1.9 The Swiss Association for Quality and Management Systems

The Swiss Association for Quality and Management Systems (SQS) provides certification and assessment services for all types of industries and services. SQS certificates are accepted worldwide thanks to accreditation by the Swiss Accreditation Service (SAS), active membership in the International Certification Network, IQNet, and co-operation contracts/agreements with accredited partners.

www.sqs.ch

The SQS Certificate ISO 9001:2000 has been issued to Kontron Compact Computers AG in the field of development, manufacturing and sales of embedded computer boards, embedded computer modules and computer systems. The certification is valid for three years, after which time an audit is performed for recertification.

2 Specifications

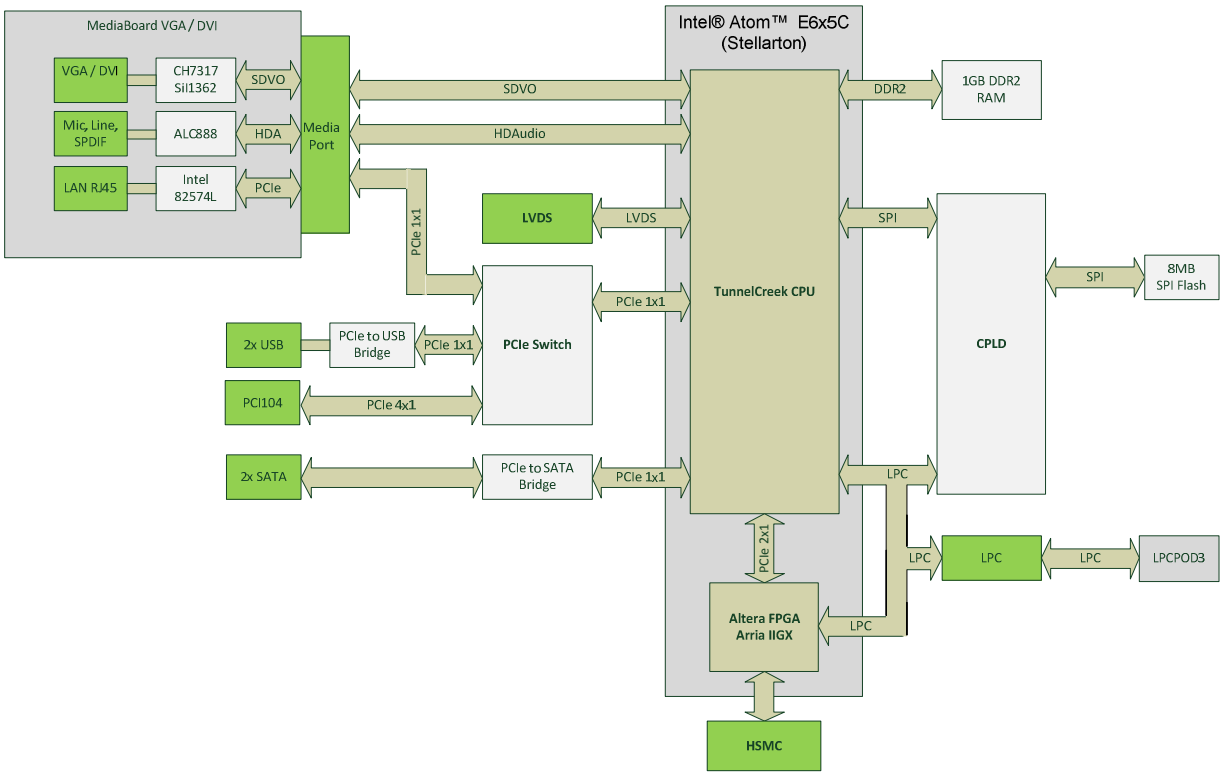
2.1 Available Modules

Part No.	Article	Soldered Memory Onboard	Intel® CPU	Remarks
802310	MSMST-13G-1.0GB	1GB	E6x5CT	
802311	MSMST-13G-2.0GB	2GB	E6x5CT	
802312	MSMST-10G-1.0GB	1GB	E6x5CT	
802313	MSMST-10G-2.0GB	2GB	E6x5CT	
802314	MSMST-06G-1.0GB	1GB	E6x5CT	
802315	MSMST-06G-2.0GB	2GB	E6x5CT	

2.2 Available Options

Part No.	Article	Remarks
802150	MSMST Mediaboard DVI	Interface: DVI, Line-In/Out or Mic-In, S/PDIF, 1Gb Ethernet. Including screw set.
802151	MSMST Mediaboard VGA	Interface: VGA, Line-In/Out or Mic-In, S/PDIF, 1Gb Ethernet. Including screw set
802315	MSMST Heat Spreader	Heat spreader, screw set included.
802316	MSMST Active Cooler	Including screw set.

2.3 Block Diagram



2.4 Functional Specifications

Processor: Intel® Stellarton Atom™ E6x5C series

» CPU: 45nm Stellarton CPU (Atom™ E6x5C series)

» Speed: 0.6 / 1.0 / 1.3GHz

Integrated Graphics: Intel®

» Graphics Memory: Up to 256MB

» Features: Integrated 2D/3D graphics engine, runs up to 400MHz, supports OpenGL ES2.0, OpenVG 1.0, DirectX 9

» Video Engine: Integrated hi-definition video decoder & encoder
Encode format: MPEG4, H.263, H.264
Decode format: MPEG2, MPEG4, VC1, WMV9, H.264

Display Interfaces

- » SDVO: Maximum resolution up to 1920x1080 @ 50Hz
- » LVDS: Single channel 18/24bit up to 1280x768 @ 60Hz

Storage

- » SATA: 2 SATA up to 300MB/s

Onboard Devices

- » TPM: TPM 1.2 connector
- » EC: Embedded controller Altera EPM1270M256, power supply supervision, and supports G3 mechanical off state with low power consumption

Additional Interfaces

- » LPC: Yes
- » SMBus: Yes

Power Management and Miscellaneous

- » HWM: Temperature monitoring for CPU and board temperatures
- » Passive Cooling: Active, passive and Critical Trip Point
- » ACPI: ACPI 1.0 / 2.0 / 3.0
- » S-States: S0, S3, S4, S5
- » C-States: C0, C1, C2, C4, Intel® Enhanced Deeper Sleep and Deep Power Down technology (code named C6) states
- » Input Voltage: Single supply support 5.0V ±5%

2.5 Mechanical Specifications

- » 90.0mm x 103.0mm
- » Height approx. 21mm

2.6 Electrical Specifications

2.6.1 Supply Voltage

- » 5.0VDC, only one single supply

2.6.2 Supply Current (Windows XP SP3)

The tested boards were mounted on a carrier board; a mouse and a keyboard were connected. The power-consumption tests were executed under Windows XP SP3 by using a tool to stress the CPU (INTEL® Thermal Analysis Tool at 100 % load). The power measurement values were acquired after 15 minutes at full load and a stable CPU die temperature. To ensure a stable die temperature, a corresponding heat sink was used to hold the temperature under the critical trip point.

MSMST-13G-1GB

Mode	[A] 5V	[W]
Full load	2.8	14

2.7 MSMST Environmental Specifications

Temperature

Operating with Kontron Compact Computers AG cooling solution:

- » Maximum operating temperature: -40 to +85°C
- » Storage temperature: -40 to +85°C

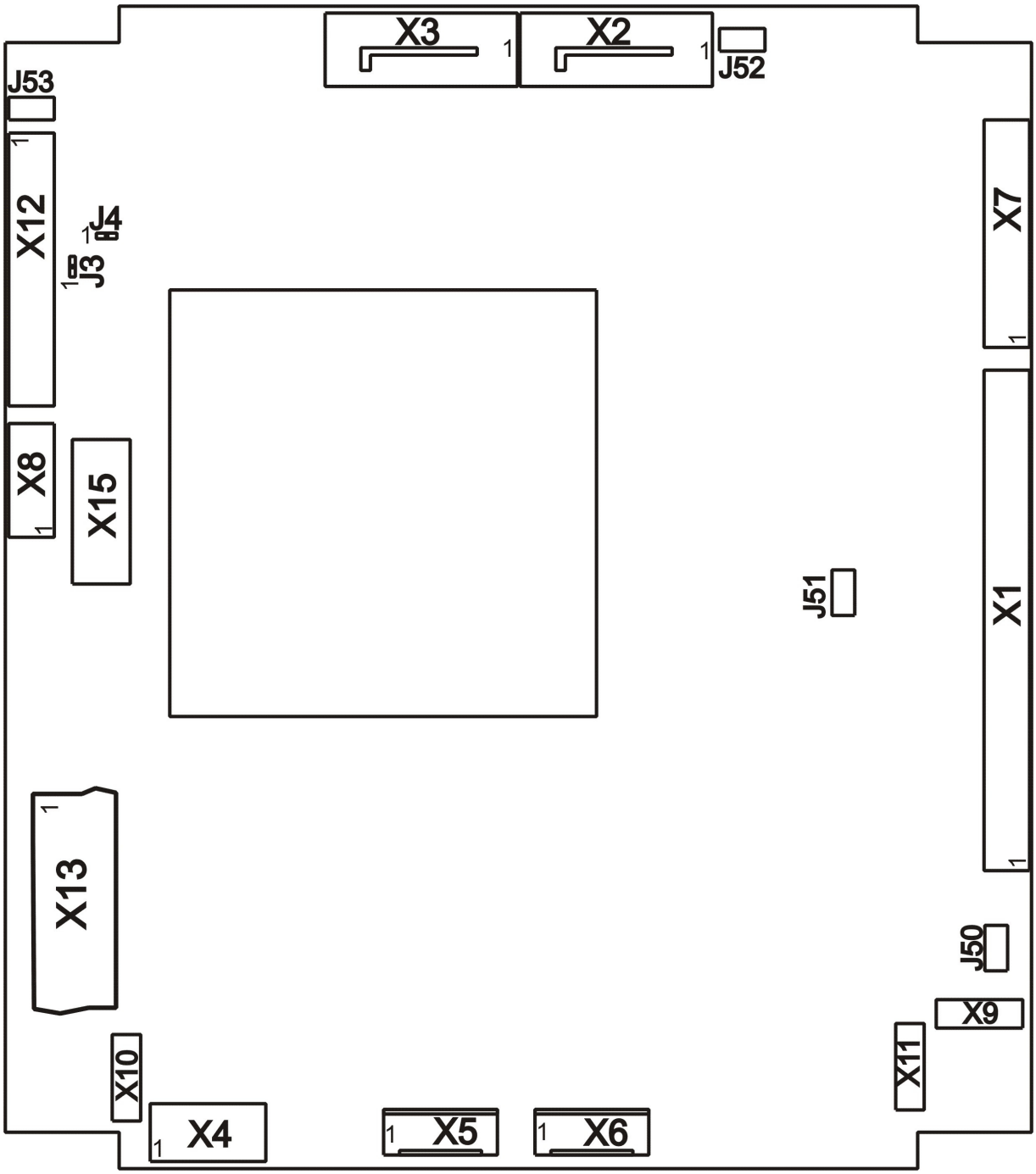
Note:	In any case, the maximum operating temperature should never be exceeded!

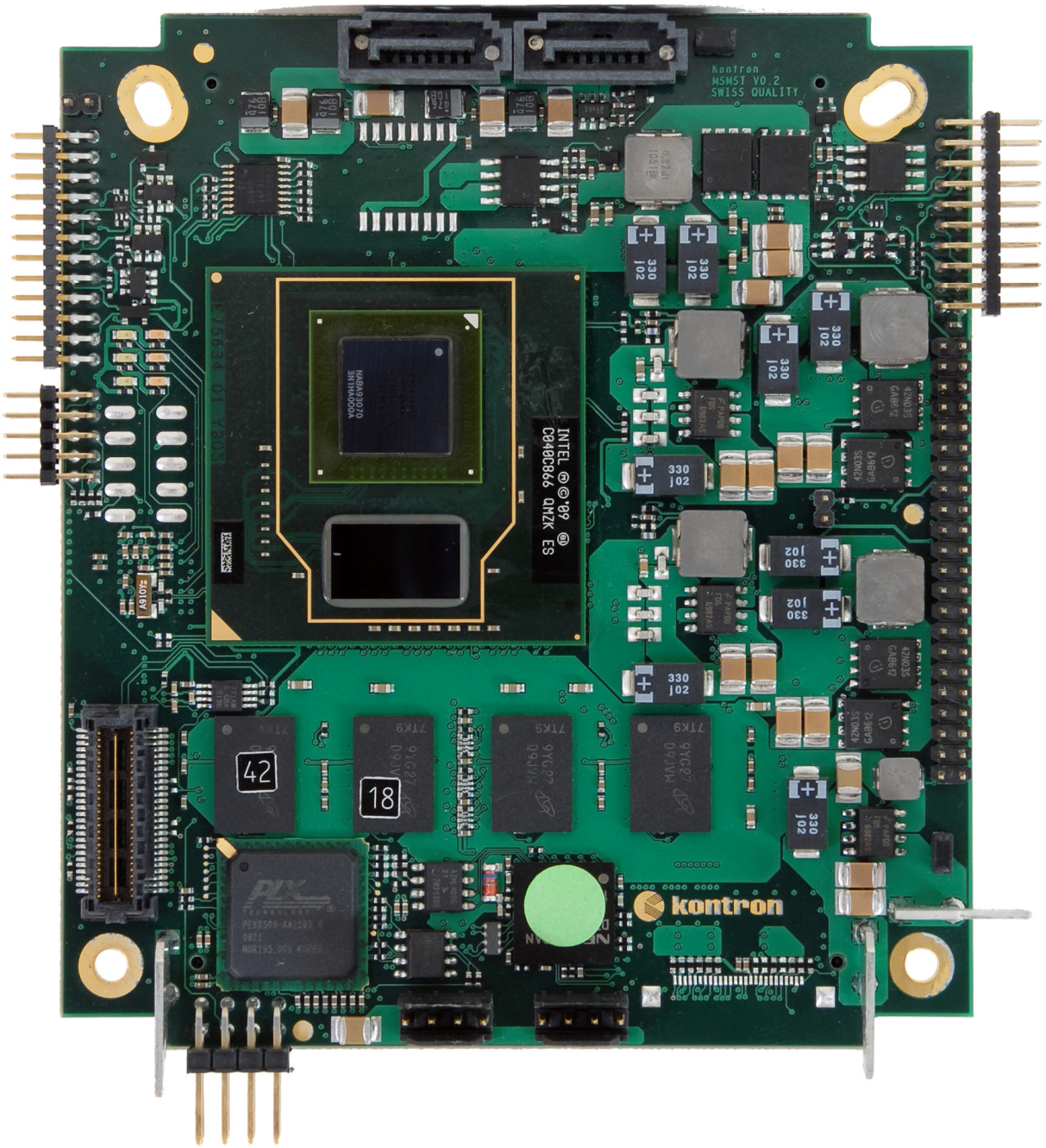
Humidity

- » Operating: 10% to 90% (non-condensing)
- » Non-operating: 5% to 95% (non-condensing)

3 MSMST Connectors & Jumpers

3.1 Assembly Layer – Top

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MSMST V0.2
SWISS QUALITY
INTEL ©©'89 ®
C0480866 QNZK ES
kontron

3.2 Connector Descriptions – Top

3.2.1 Power Input Alternative – X4

X4 is an alternative power input connector, with an additional System Management Interface. Use X9, X10 and X11 as standard power supplies.

Pin	Description	Pin	Description
1	GND	5	SMB_DAT
2	V5.0_S5	6	SMB_CLK
3	MAIN_SW	7	GND
4	VDC	8	V5.0_S5

3.2.2 Power Input – X9, X10, X11

Ref.	Description
X9	VDC (nom. 5V)
X10	V12_IN
X11	GND

3.2.3 USB2.0 – X5, X6

Pin	Description
1	VCC
2	D-
3	D+
4	GND

3.2.4 GPIO – X1

GPIOs are directly routed to the FPGA. The routing layout is not differential.

Pin	Description	Pin	Description
1	GND	23	GPIO_TX1P
2	5V	24	GPIO_TX1N
3	GPIO_RX1P	25	GPIO_TX2P
4	GPIO_RX1N	26	GPIO_TX2N
5	GPIO_RX2P	27	GPIO_TX3P
6	GPIO_RX2N	28	GPIO_TX3N
7	GPIO_RX3P	29	GPIO_TX4P
8	GPIO_RX3N	30	GPIO_TX4N
9	GPIO_RX4P	31	GND
10	GPIO_RX4N	32	3.3V
11	GND	33	GPIO_TX5P
12	3.3V	34	GPIO_TX5N
13	GPIO_RX5P	35	GPIO_TX6P
14	GPIO_RX5N	36	GPIO_TX6N
15	GPIO_RX6P	37	GPIO_TX7P
16	GPIO_RX6N	38	GPIO_TX7N
17	GPIO_RX7P	39	GPIO_TX8P
18	GPIO_RX7N	40	GPIO_TX8N
19	GPIO_RX8P	41	GND
20	GPIO_RX8N	42	3.3V
21	GND	43	GPIO_CLKOUTP
22	3.3V	44	GPIO_CLKOUTN

3.2.5 SPI and LPC (POST Code) – X7

Pin	Description	Pin	Description
1	3.3V	11	LPC_CLK_0
2	LPC_AD0	12	LPC_BIOS_EN#
3	LPC_FRAME#	13	GND
4	LPC_AD1	14	RST#_POD
5	PCIe_RST#_POD	15	3.3V_DEDIPROG
6	LPC_AD2	16	LPC_SERIRQ
7	3.3V	17	SPI_CS#
8	LPC_AD3	18	SPI_SCK
9	5.0V	19	SPI_MISO
10	PCIe_RST#_POD	20	SPI_MOSI

3.2.6 SATA – X2, X3

Pin	Description	Pin	Description
1	GND	5	RX_X-
2	TX_X+	6	RX_X+
3	TX_X-	7	GND
4	GND		

3.2.7 LVDS – X12

Pin	Description	Pin	Description
1	DATA0-	13	5.0V
2	DATA0+	14	3.3V
3	DATA1-	15	DDC_CLK
4	DATA1+	16	DDC_DAT
5	DATA2-	17	RST_LVDS#
6	DATA2+	18	BCK_ENAX
7	DATA3-	19	BKLT_CTRLX
8	DATA3+	20	LVDS_ENVCCX
9	GND	21	12V
10	GND	22	12V
11	CLK-	23	SMB_CLK0
12	CLK+	24	SMB_DAT0

3.2.8 JTAG – SC - X8

Pin	Description	Pin	Description
1	TCK	6	**NC**
2	GND	7	**NC**
3	TDO	8	**NC**
4	3.3V	9	TDI
5	TMS	10	GND

3.2.9 JTAG - X15

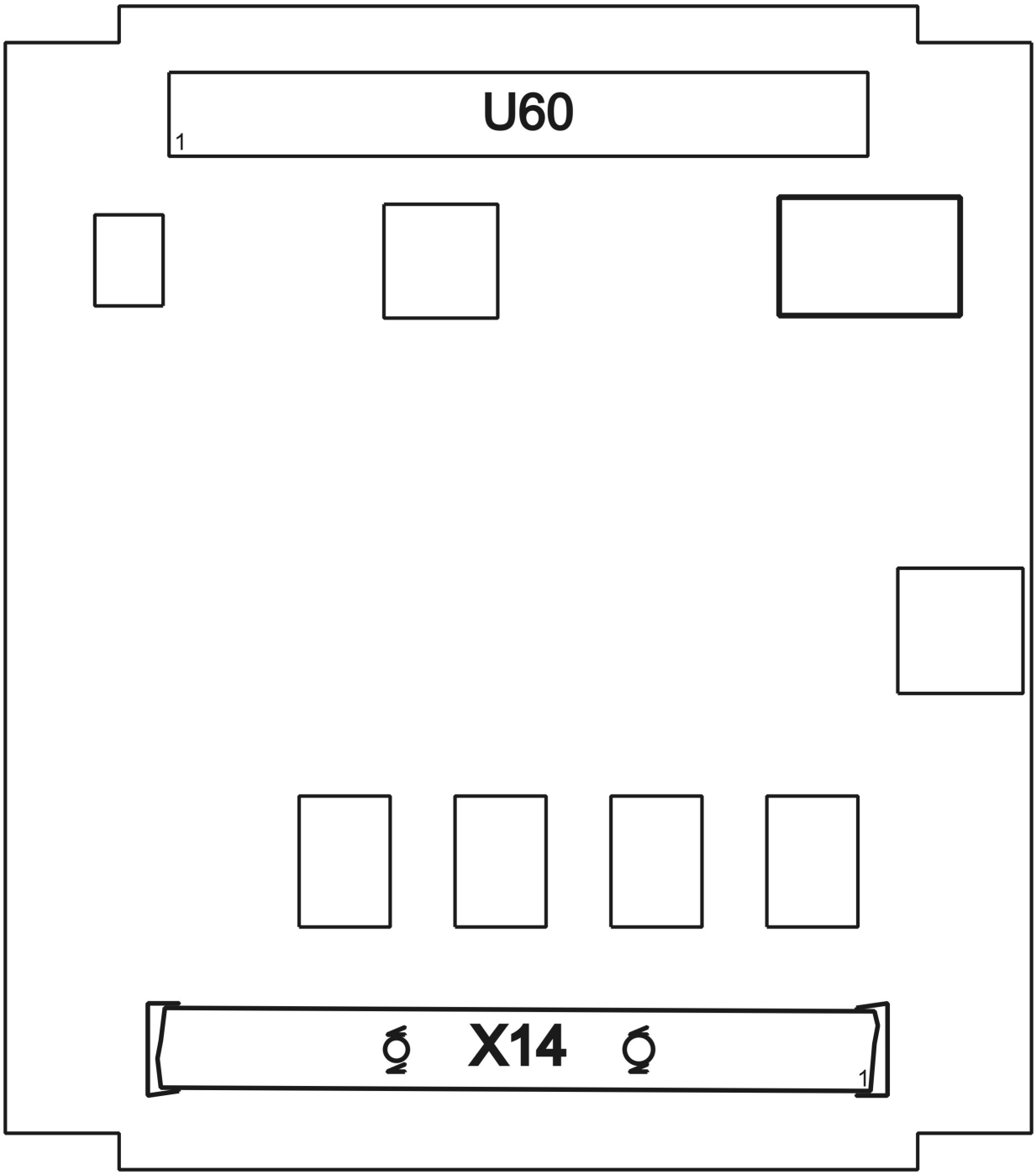
Pin	Description	Pin	Description
1	TCK	6	NC
2	GND	7	TRST#
3	TDO	8	**NC**
4	3.3V	9	TDI
5	TMS	10	GND

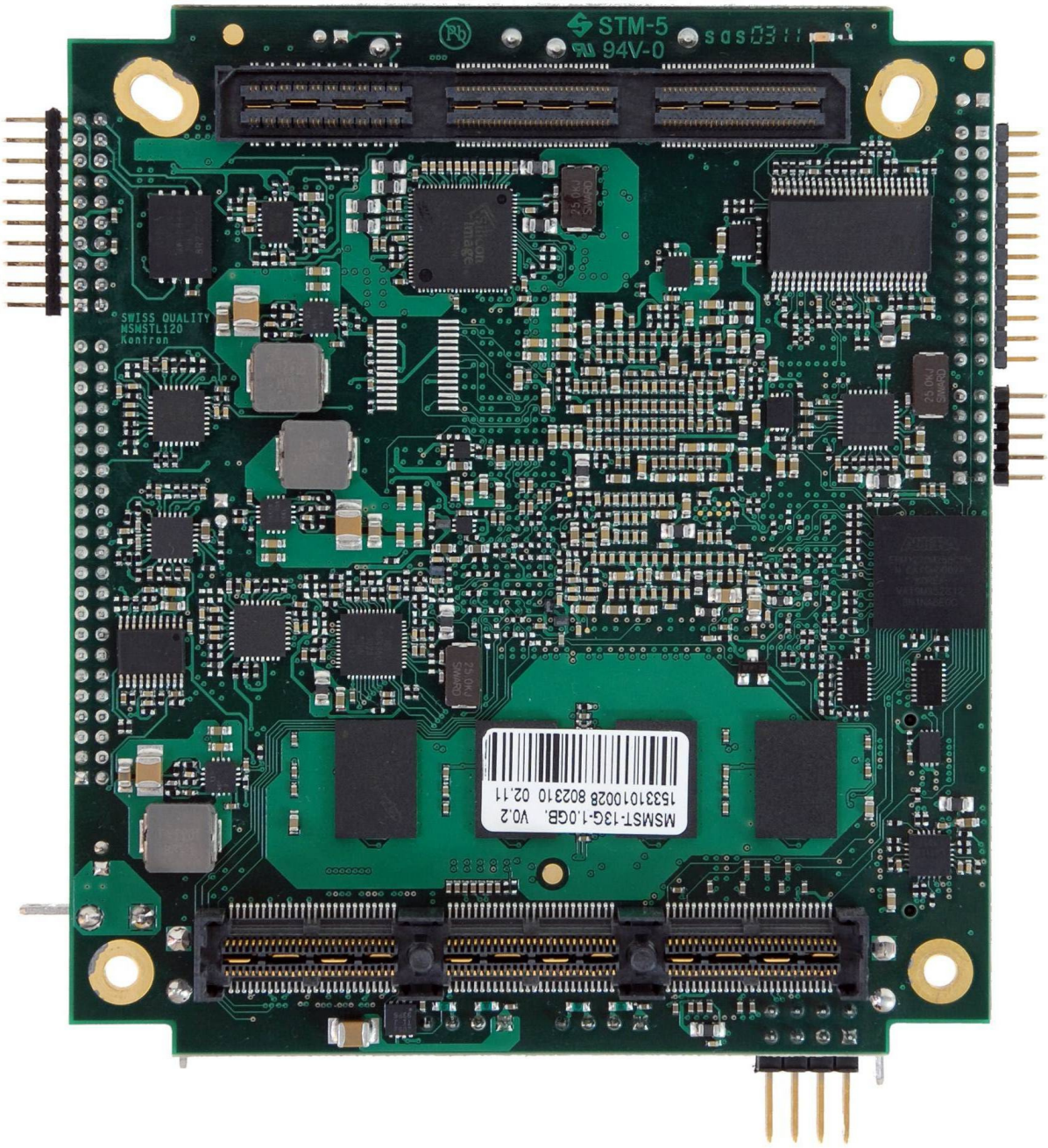
3.2.10 Media Port (PCIe, SDVO, HAD) – X13

X13 is a high-speed connector for the mediaboard interface. Media extension cards with either VGA/GbE/Audio or DVI/GbE/Audio are available.

Pin	Description		Description	Pin
1	EN_V5.0_S0		EN_V3.3_S3	2
3	GND		GND	4
5	PCIE_RX1+		CLK_PCIE2+	6
7	PCIE_RX1-		CKL_PCIE2-	8
9	GND		GND	10
11	PCIE_TX1+		PCIE_WAKE#	12
13	PCIE_TX1-		PCIE_RST#	14
15	5.0V		5.0V	16
17	SMB_CLK		SMB_ALERT#	18
19	SMB_DAT1		NC	20
21	5.0V		5.0V	22
23	NC		NC	24
25	NC		NC	26
27	HDA_CLK	3.3V	V_BAT	28
29	GND		GND	30
31	HDA_RST#		HDA_SDIN0	32
33	HDA_SYNC		HDA_SDOUT	34
35	GND		GND	36
37	SDVO_DDC_CLK		SDVO_INT+	38
39	SDVO_DDC_DAT		SDVO_INT-	40
41	GND		GND	42
43	SDVO_R+		SDVO_G+	44
45	SDVO_R-		SDVO_G-	46
47	GND		GND	48
49	SDVO_CLK+		SDVO_B+	50
51	SDVO_CLK-		SDVO_B-	52

3.3 Assembly Layer – Bottom

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1533101002B 802310 02.11

3.4 Connector Descriptions – Bottom

3.4.1 PCIe/104 – X14

These signals are in accordance with the latest PCI/104-Express specification.

3.4.2 HSMC – U60

Pin	Description	Pin	Description
BANK 1			
1	CLK_PCIE_HSMC+	21	B1_TX4+
2	**NC**	22	B1_RX0+
3	CLK_PCIE_HSMC-	23	B1_TX4-
4	**NC**	24	B1_RX0-
5	**NC**	25	B1_TX0+
6	**NC**	26	B1_RX4+
7	**NC**	27	B1_TX0-
8	**NC**	28	B1_RX4-
9	B1_TX2+	29	B1_TX1+
10	B1_RX5+	30	B1_RX3+
11	B1_TX2-	31	B1_TX1-
12	B1_RX5-	32	B1_RX3-
13	B1_TX3+	33	B1_DAT
14	B1_RX2+	34	B1_CLK
15	B1_TX3-	35	JTAG_TCK
16	B1_RX2-	36	JTAG_TMS
17	B1_TX5+	37	JTAG_TDO
18	B1_RX1+	38	JTAG_TDI
19	B1_TX5-	39	CLKOUT0
20	B1_RX1-	40	CLKIN0
BANK 2			
41	B2_D0_2+	71	B2_TX4+
42	B2_D1_3+	72	B2_RX4+
43	B2_D0_2-	73	B2_TX4-
44	B2_D1_3-	74	B2_RX4-
47	B2_TX0+	77	B2_TX5+
48	B2_RX0+	78	B2_RX5+
49	B2_TX0-	79	B2_TX5-
50	B2_RX0-	80	B2_RX5-

Pin	Description	Pin	Description
53	B2_TX1+	83	B2_TX6+
54	B2_RX1+	84	B2_RX6+
55	B2_TX1-	85	B2_TX6-
56	B2_RX1-	86	B2_RX6-
59	B2_TX2+	89	B2_TX7+
60	B2_RX2+	90	B2_RX7+
61	B2_TX2-	91	B2_TX7-
62	B2_RX2-	92	B2_RX7-
65	B2_TX3+	95	B2_CLKOUT1+
66	B2_RX3+	96	B2_CLKIN1+
67	B2_TX3-	97	B2_CLKOUT1-
68	B2_RX3-	98	B2_CLKIN1-
BANK 3			
101	B3_TX8+	132	B3_RX13+
102	B3_RX8+	133	B3_TX13-
103	B3_TX8-	134	B3_RX13-
104	B3_RX8-	137	B3_TX14+
107	B3_TX9+	138	B3_RX14+
108	B3_RX9+	139	B3_TX14-
109	B3_TX9-	140	B3_RX14-
110	B3_RX9-	143	B3_TX15+
113	B3_TX10+	144	B3_RX15+
114	B3_RX10+	145	B3_TX15-
115	B3_TX10-	146	B3_RX15-
116	B3_RX10-	149	B3_TX16+
119	B3_TX11+	150	B3_RX16+
120	B3_RX11+	151	B3_TX16-
121	B3_TX11-	152	B3_RX16-
122	B3_RX11-	155	B3_CLKOUT2+
125	B3_TX12+	156	B3_CLKIN2+
126	B3_RX12+	157	B3_CLKOUT2-
127	B3_TX12-	158	B3_CLKIN2-
128	B3_RX12-	160	PSNT#
131	B3_TX13+		
POWER			
12V	106, 112, 118, 124, 130, 136, 142, 148, 154, 46, 52, 58, 64, 70, 76, 82, 88, 94, 100		
3.3V	105, 111, 117, 123, 129, 135, 141, 147, 153, 159, 45, 51, 57, 63, 69, 75, 81, 87, 93, 99		
GND	169, 170, 171, 172, 165, 166, 167, 168, 161, 162, 163, 164		

3.5 Jumpers

Settings written in bold are defaults!

Jumper	Signal	1-2 / open	2-3 / closed
J3	LVDS_ENVCC	**V3.3_S0**	V5.0_S0
J4	BCK_ENA	**V5.0_S0**	V12_IN
J50	VDC	VDC	**V5.0_S5**
J51	V2.5_F_S0	**2.5V**	3.3V
J52	JTAG	Open loop	**Arria stand-alone**
J53	BIOS_DEFAULTS#	**Standard**	Loads the BIOS defaults

3.6 Signal Descriptions

3.6.1 PCI Express x1 Lane

PCI Express x1 Lane is a fast connection interface for many different system devices, such as network controllers, I/O controllers or express card devices.

3.6.2 USB

Two USB ports (NEC D720200 USB 3.0 controller) are available. The USB controller complies with all three versions 1.1, 2.0 and 3.0 of the USB standard and is backward compatible.

Configuration

The USB controller is a PCIe bus device. The BIOS allocates required system resources during configuration of the PCI bus.

3.6.3 SATA

The Silicon Image (SiI3132) device offers the possibility to connect 2 SATA hard disks in accordance with SATA with 150MB/s per channel, or SATA II with 300MB/s per channel in AHCI mode.

Configuration

The SATA controller is a PCIe bus device. The BIOS allocates required system resources during configuration of the PCI bus.

3.6.4 Audio

The HD audio controller is integrated in the Intel® Atom CPU.

3.6.5 Serial IRQ

The serial IRQ pin offers a standardized interface to link interrupt request lines to a single wire.

Configuration

The serial IRQ machine works in "Continuous Mode".

3.6.6 SDVO Output

The graphics subsystem is integrated in the Intel® Atom CPU.

3.6.7 LVDS Flat Panel Interface

LVDS is a part of the graphics subsystem and is also integrated in the Intel Atom® CPU.

3.6.8 Power Control

MSMST is powered by a 5.0V single supply. The 12V connector supplies HSMC and PCIe/104™ peripheral boards.

The system controller guides the whole startup and shutdown process.

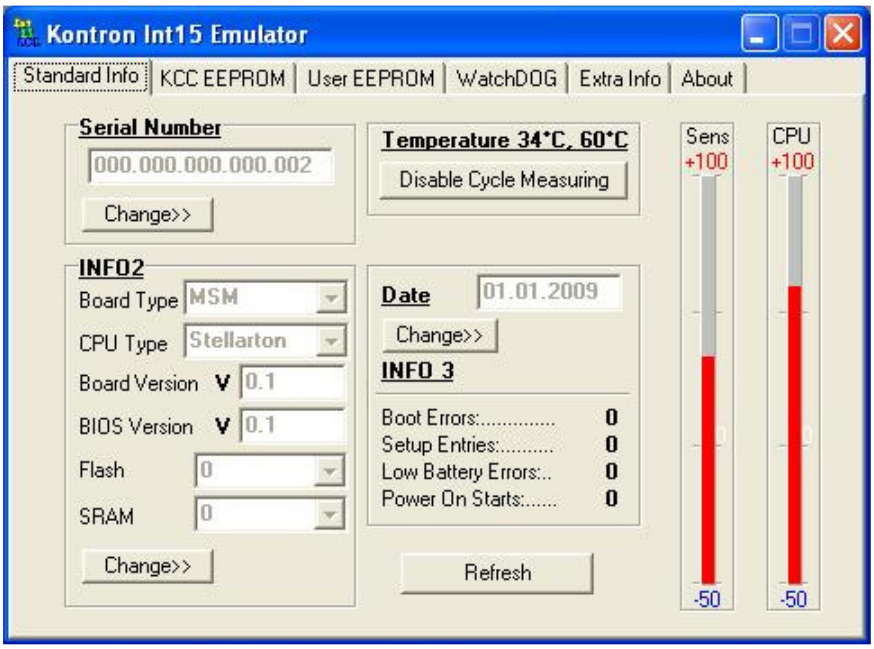
3.6.9 LPC Bus

The Low Pin Count Interface signals are connected to the LPC bus bridge, which is located in the Intel® Atom processor. The LPC low speed interface can be used for peripheral circuits such as an external Super I/O Controller which typically combine legacy-device support into a single IC.

4 Special Features

4.1 INT15 Support

The INT15 SFR (Special Function Register) functions support access to an I2C EEPROM. Addresses 0h-3FFh are reserved for manufacturer information and counters; addresses 400h-7FFh are for customer purposes.



4.2 System Controller

MSMST System Controller I/O Port Operations

- » Read the system controller version
- » Simple emulation of the keyboard controller registers
- » System Reset
- » Watchdog function

4.2.1 Special I/O Address Ranges

The special function ports of the MSMST board are I/O mapped and can be simply accessed under all operating systems. The following table shows the addresses used.

Address	Name	Type	Description
0x60	KDAT	RO	Keyboard controller emulation data register
0x64	KCTL	RW	Keyboard controller emulation control register
0xA80	VMSB	RO	System controller version MSB
0xA81	VLSB	RW	System controller version LSB
0xA82	DJMP	RO	Default jumper state
0xA83	WDOG	RW	Watchdog function

4.2.2 Functional Description

I/O PORT 0x60 – Keyboard Controller Emulation Data Register

Bit	Access	Value	Description
7:0	Read Only	0xFF (0x90)	By default, after system reset, this address does not respond and returns the value 0xFF while reading. When "responding keyboard" is enabled it returns 0x90. Write to this port is ignored.

I/O PORT 0x64 – Keyboard Controller Emulation Control Register

Bit	Access	Value	Description
7:0	Read	0xFF (0x10)	By default, after system reset, this address does not respond and returns 0xFF while reading. When "responding keyboard" is enabled it returns the value 0x10.
7:0	Write	0xFE	Writing 0xFE to this port initiates a system reset, independent of an enabled or disabled "responding keyboard".

I/O PORT 0xA80 – System Controller Version MSB

Bit	Access	Value	Description
7:0	Read Only	0x01★	System controller version MSB

★ Example valid for system controller version 1.76 and later.

I/O PORT 0xA81 – System Controller Version LSB

Bit	Access	Value	Description
7:0	Read	0x77★	System controller version LSB
7:0	Write	0x55	Enable "responding keyboard" addresses.
7:0	Write	0xAA	Disable "responding keyboard" addresses.

★ Example valid for system controller version 1.77 and later.

I/O PORT 0xA82 – Default Jumper State

Bit	Access	Value	Description
7:0	Read Only	0x00	Default jumper is set.
7:0	Read Only	0x01	Default jumper is open.

I/O PORT 0xA83 – Watchdog Function

Bit	Access	Value	Description
7	Read	0b	Watchdog reset time set up in seconds.
7	Read	1b	Watchdog reset time set up in minutes.
7	Write	0b	Set watchdog reset time value in seconds.
7	Write	1b	Set watchdog reset time value in minutes.
6:0	Read	0xNN	NN: current watchdog timer value until watchdog timer is expired.
6:0	Write	0xNN	Enable/recharge a watchdog timer with value NN (seconds/minutes, depends on Bit 7).
6:0	Read	0x00	Watchdog is disabled.
6:0	Write	0x00	Disable watchdog function.

Typical usage: write a defined value in minutes/seconds to the port 0xA83 to enable/recharge a watchdog, and recharge a watchdog periodically in a time shorter than the predefined watchdog reset time to prevent a system reset.

For example: writing the value 0x3C (60 decimal) to this port will enable and set a watchdog timer to 60 seconds.

5 Design Considerations

5.1 Board Drill-Hole Dimensions

The MSMST board follows the PCIe/104™ specification. For more information see the PCI/104-Express™ & PCIe/104™ specifications.

5.2 Thermal Management

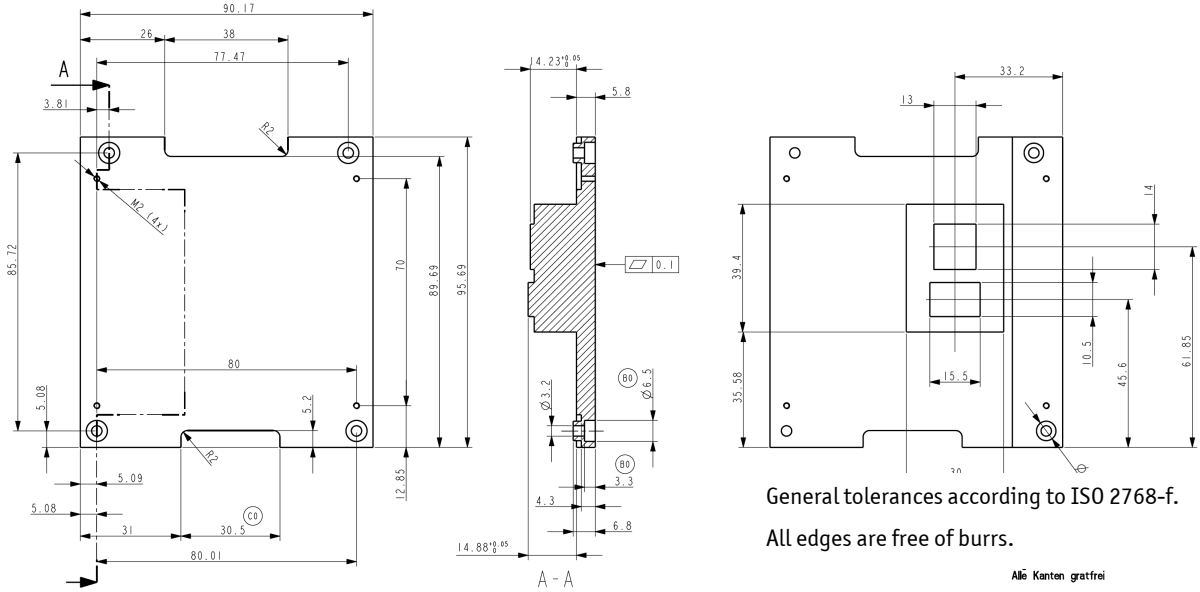
The heat-spreader plate assembly is delivered by Kontron Compact Computers AG for the MSMST. The heat-spreader plate on top of this assembly is ***not*** a heat sink. It works as a standard thermal interface to be used with a heat sink or other cooling device.

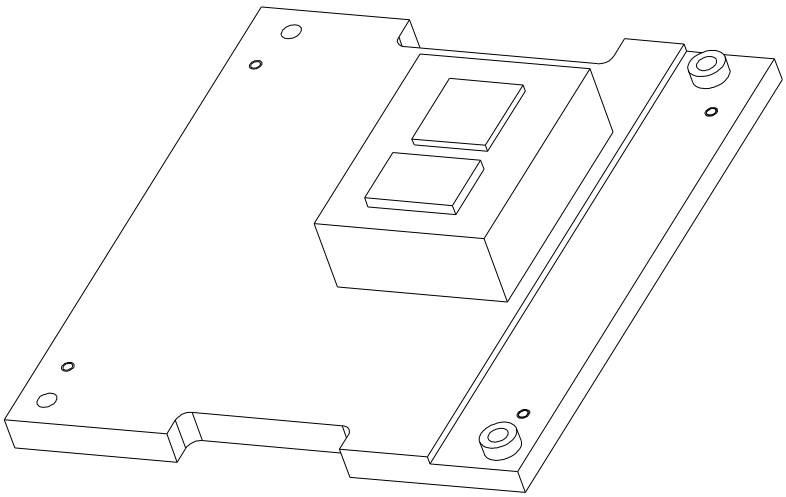
External cooling must be provided to maintain the heat-spreader plate at proper operating temperatures. Under worst case conditions, the cooling mechanism must maintain an ambient air and heat-spreader plate temperature of 85°C or less.

The aluminum blocks and thermal pads on the underside of the heat-spreader assembly serve to provide thermal interfaces between the heat-spreader plate and the major heat-generating components on the MSMST.

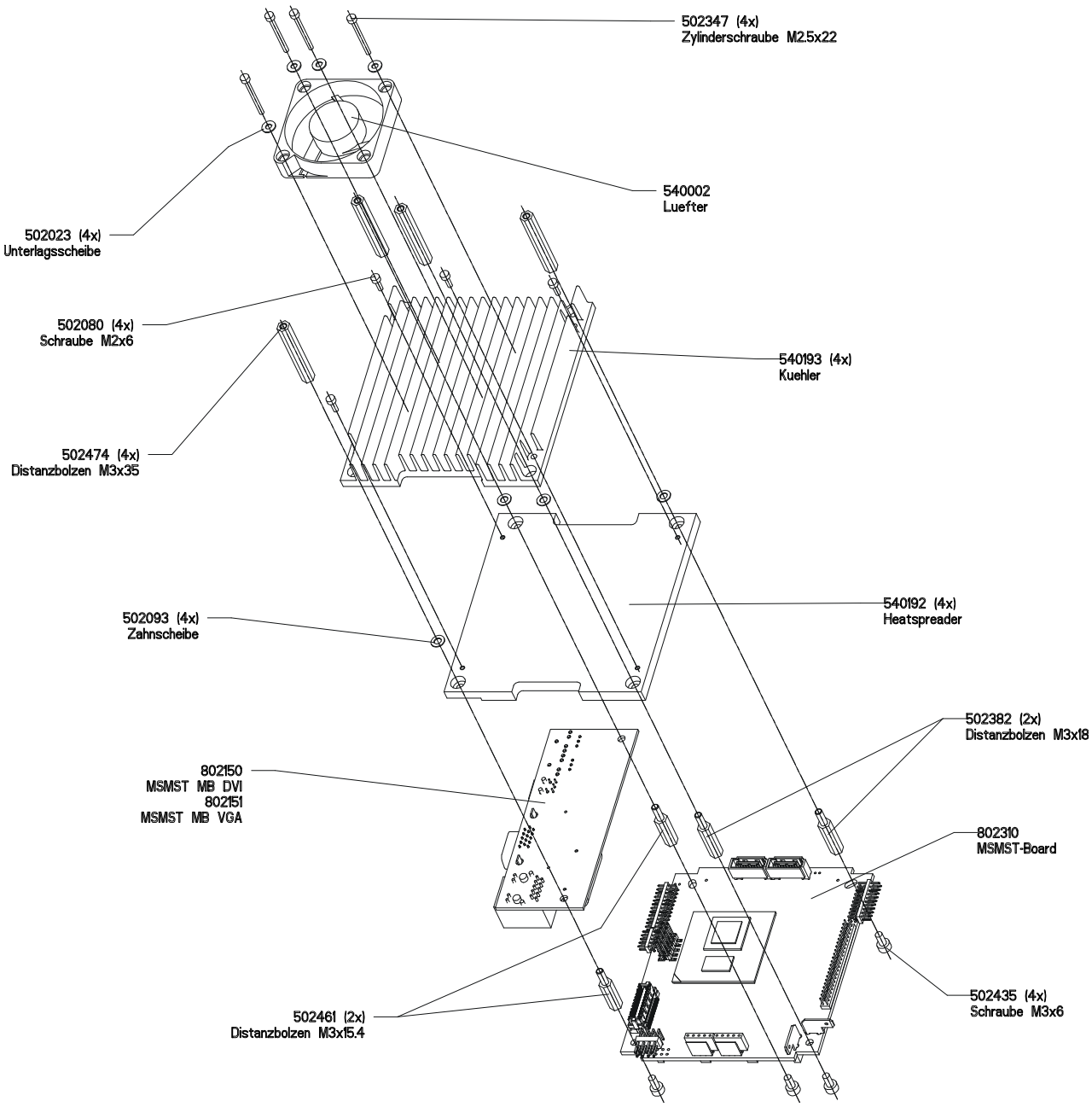
5.3 Heat-Spreader Dimensions

Figures: heat-spreader plate showing the pads for the heat-generating components of the MSMST boards.





5.4 Exploded Assembly Drawing



6 BIOS Operation

The module is equipped with the AMI Aptio® BIOS located in an onboard SPI serial flash memory. The BIOS can be updated using a flash utility.

6.1 Determining the BIOS Version

The AMI Aptio® BIOS version can be determined on the BIOS Setup screen.

6.2 Setup Guide

System behavior can be modified by changing the BIOS configuration.

Note:	Selecting incorrect values may cause system boot failure. To recover, press <**F3**> to load setup default values.

6.2.1 Start the AMI Aptio® BIOS Setup Utility

To start the AMI Aptio® BIOS setup utility, press <**DEL**> during boot-up.
Press <DEL> to enter Setup.
The Main Menu then appears.
The Setup Screen is composed of several sections:

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus.
Legend Bar	Bottom right	Lists setup navigation keys.
Item-Specific Help Window	Top right	Help for the selected item.
Menu Window	Center Left	Selection fields for the current menu.

6.3 Recovery Jumper

In the case of a bad configuration the system may not start. Use jumper **J53** to load the BIOS defaults.

To store them, enter the setup and press **F4** to save.

Temporary Boot Menu

By pressing the <**F7**> button at the beginning of the startup process the temporary boot menu will appear.

Menu Bar

The menu bar at the top of the window lists the different menus. Use the left/right arrow key to make a selection.

Legend for the Menu Bar

Key	Function
→ or ← Arrow Key	Select Screen
↑ or ↓ Arrow Key	Select Item
Enter	Select
+/-	Change Option
<F1>	General Help
<F2>	Previous Values
<F3>	Optimized Defaults
<F4>	Save
<ESC>	Exit

Selecting an Item

Use the ↑ or ↓ key to move. Use the + or – key to select a value.

Displaying Submenus

Use the ↑ or ↓ key to move the cursor to a submenu, then press <**Enter**>. The pointer (▸) marks all the submenus.

Item-Specific Help Window

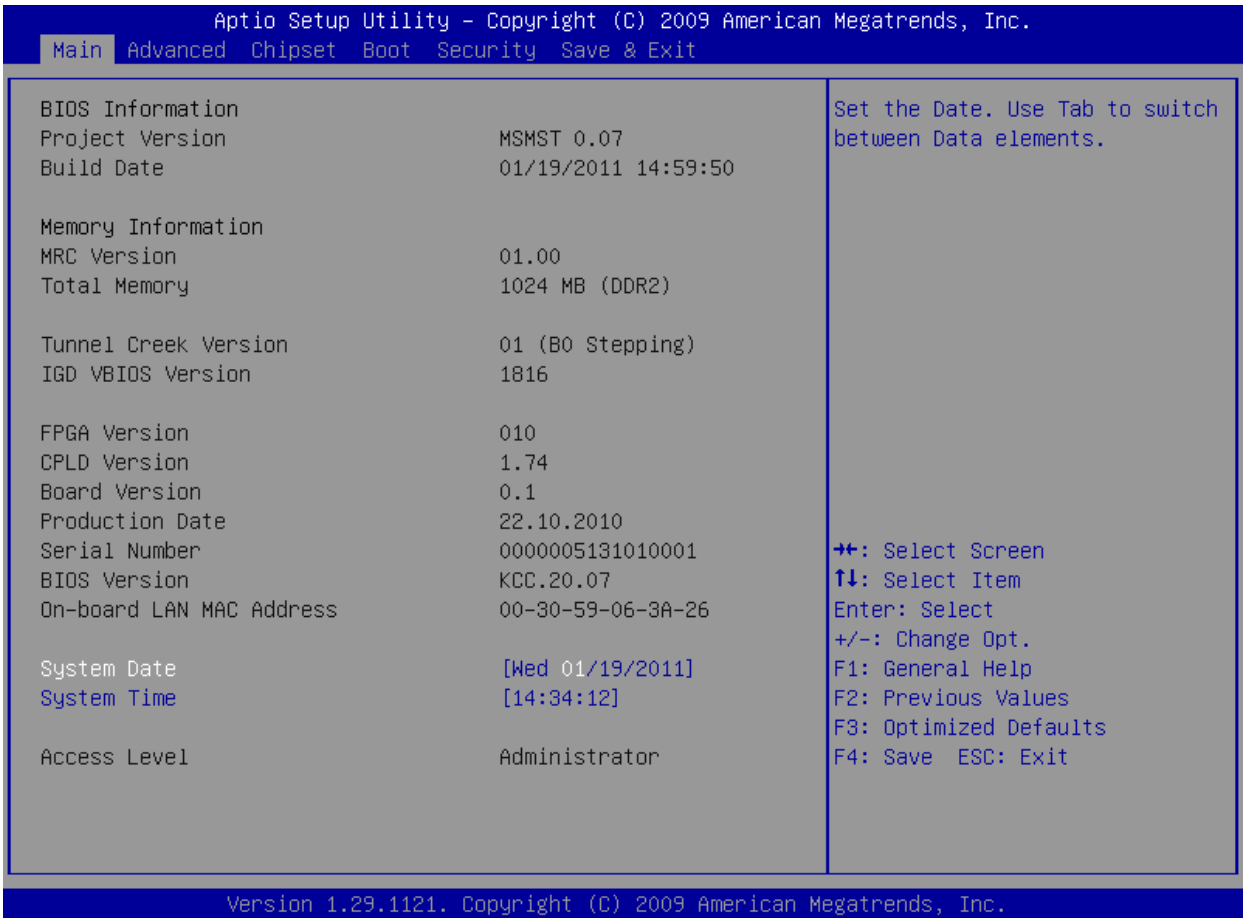
The Help window on the right side of each menu displays the Help text for the selected item.

General Help Window

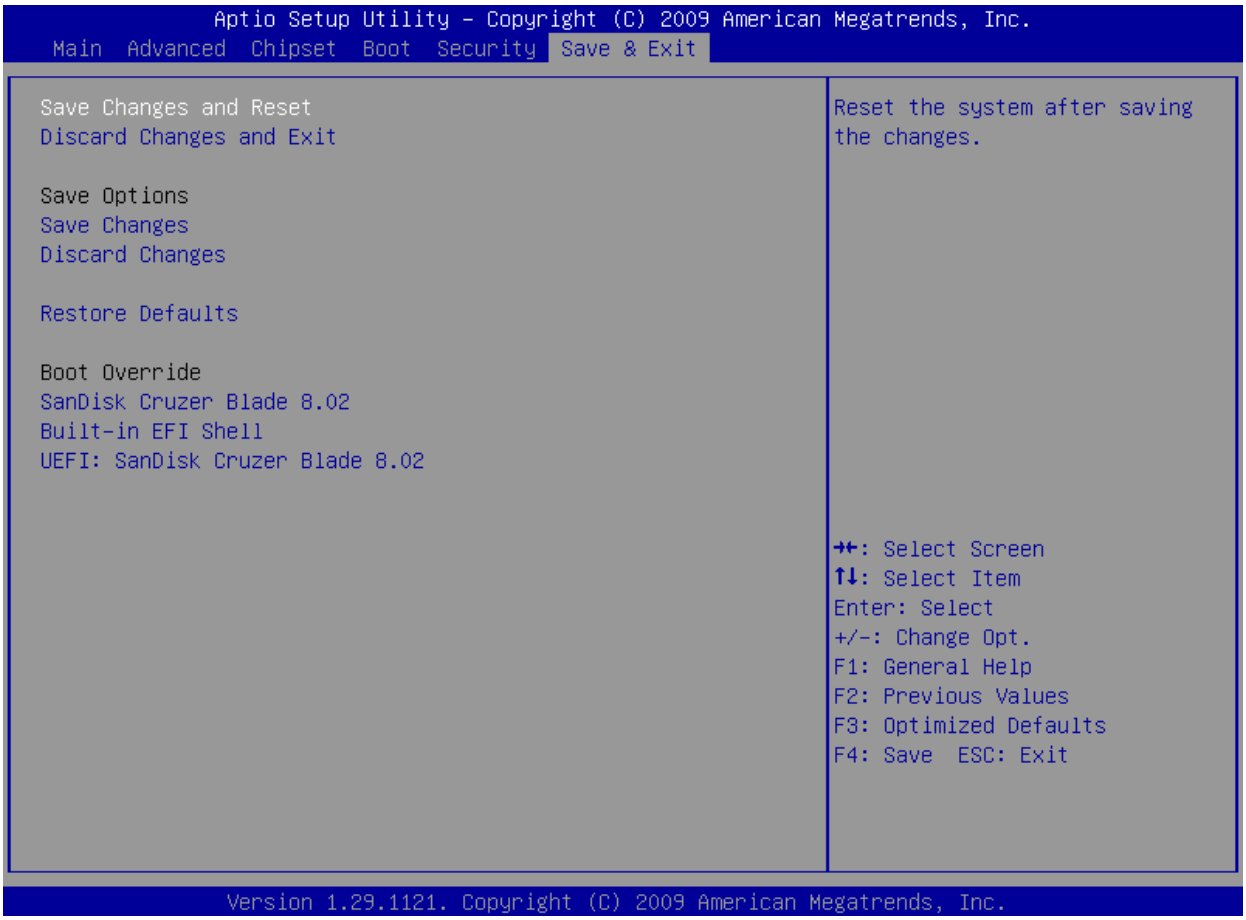
Pressing <**F1**> on a menu brings up the general Help. Press <**Esc**> to exit.

6.4 BIOS Setup

6.4.1 Main Menu



6.4.2 Exit Menu



Feature	Description
Saving Changes and Reset	Exit utility and save your changes to CMOS.
Discarding Changes and Exit	Exit utility without saving setup data to CMOS.
Save Changes	Save setup data to CMOS.
Discard Changes	Load previous values from CMOS for all setup items.
Load Setup Defaults	Load default values for all setup items.

6.5 BIOS Update

Before downloading a BIOS, please check the following:

Make a bootable diskette or USB stick which includes the following files:

- » afudos.exe
- » core BIOS (MSMSTxxx.ROM)
- » Rename the MSMSTxxx.ROM file to bios.rom

IMPORTANT: Do not use boot disks created in a Windows operating system. If you do not have an MSDOS 6.22 disk available, you can download a boot disk from www.bootdisk.com.

Notes:

- » Disable the EMM386 or other memory managers in the CONFIG.SYS of your boot disk.
- » Make sure that the AFUDOS.exe program and the BIOS are in the same path and directory!
- » Boot DOS without config.sys and autoexec.bat. (Press **F5** while starting the DOS boot).

Start the DOWNLOADING process:

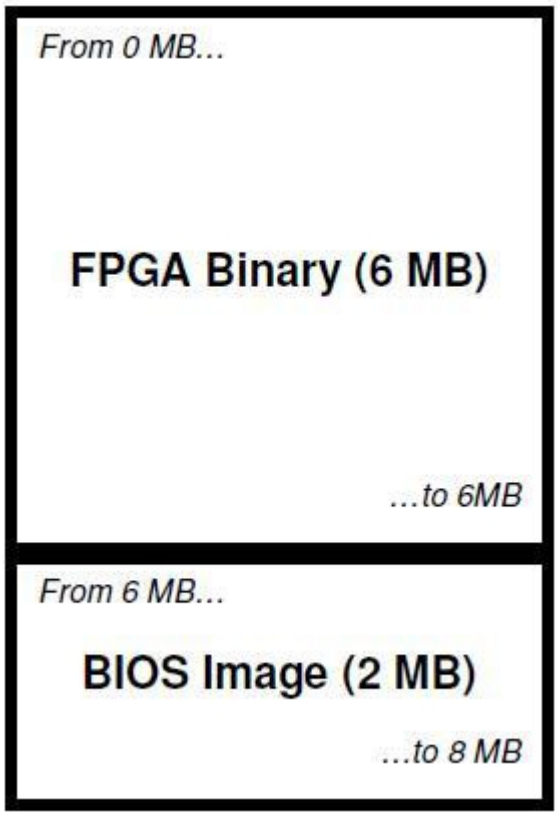
1. Start the system using the bootable diskette.

WARNING: Always use AFUDOS.EXE with option /N to be sure that NVRAM is cleared during the BIOS Update!

2. Run AFUDOS.EXE BIOS.ROM /B /P /K /X /N
3. Reboot the system and press **DEL** to enter the setup mode. Set the default values by pressing **F3**.
4. "Save and leave" the setup by pressing **F4**.
5. Reboot the system.

6.6 Permanently Programming the FPGA

1. Convert your programming file to rbf (or enable rbf file generation).
2. Pad your rbf file to 6MB (6*1024*1024 bytes); if the FPGA binary is smaller than 6MB, fill the empty space with FFs.
3. Assemble the newly combined BIOS file:
    a. the padded RBF file (0 to 5F FFFFh)
    b. BIOS (5F FFFFh to 7F FFFFh)



4. Start AFUDOS with the following parameters to update the FPGA and BIOS together:
    a. afudos bios.rom /B /P /N /X /K
5. Restart the MSMST and enter the BIOS screen with **DEL**; load the defaults with **F3** and save them **F4**.

6.7 Driver Installation Instructions

6.7.1 Windows XP SP3 Fresh Installation

Follow the instructions in this section if you are performing a new installation of Windows XP SP3. Copy all files in the TXT_DRIVER_USB_SATA folder to a diskette, and connect a USB floppy drive to the MSMST.

1. Put your Windows XP SP3 CD in the CD/DVD-ROM drive.
2. Press **F6** for third-party SCSI or driver installation at the beginning of text mode installation. Insert the SATA and USB TXT driver diskette and press '**s**' ('**z**' on the German version) when setup asks if you want to specify an additional device.
3. From the menu that is presented next, select "Renesas Electronics USB 3.0 Host Controller" and press '**Enter**'.
4. Press '**s**' when setup asks if you want to specify an additional device.
5. From the menu that is presented next, select "Renesas Electronics USB 3.0 Hub" and press '**Enter**'.
6. Press '**s**' when setup asks if you want to specify an additional device.
7. From the menu that is presented next, select "Silicon Image SiI 3132 SATALink Controller for Windows XP" and press '**Enter**'.
8. Press '**Enter**' again when prompted to continue with the text mode setup.
9. Follow the setup instructions to select your choice for partition and file system.
10. After setup has examined your disks, it will copy files from the CD to the hard drive selected above, and restart the system. After restart the setup process will resume to finish the installation.

7 Appendix A: FPGA Information

7.1 FPGA Type

The MSMST has a special combination of an Intel® Atom™ Processor and an Altera FPGA combined as a single chip solution.

Manufacturer: Altera

Family: Arria II GX

Type: EP2AGXE6XXFPGA

Datasheet for Arria II* Devices
http://edc.intel.com/Link.aspx?id=4192

EP2AGXE6XXFPGA Device Handbook Volume 1: Device Interfaces and Integration
http://edc.intel.com/Link.aspx?id=4194

EP2AGXE6XXFPGA Device Handbook Volume 2: Transceivers
http://edc.intel.com/Link.aspx?id=4195

7.2 Software

Required Software:

Altera Quartus II Subscription Edition: https://www.altera.com/download/software/quartus-ii-se

7.3 FPGA Signals

Shared Signals

Description	Schematic Signal Name	I/O Standard	FPGA Pin
PCI Reset for FPGA	ARRIA_RST#	3.3V LVCMOS	F4
25MHz Clock	CLK_25MHZ	3.3V LVCMOS	P3
75MHz Clock	CLK_REF1_QL0+	LVDS	Y29
	CLK_REF1_QL0-		Y30
75MHz Clock	CLK_REF1_QL1+	LVDS	K29
	CLK_REF1_QL1-		K30

PCI Express Interface

Description	Schematic Signal Name	I/O Standard	FPGA Pin
PCI Express Lane 0 Receive Bus	PCIE_PETN[0]	1.5V PCML	AE32
	PCIE_PETP[0]		AE31
PCI Express Lane 0 Transmit Bus	PCIE_PERN[0]		AD30
	PCIE_PERP[0]		AD29
PCI Express Lane 0 Reference Clock	CLK_100MHZ_PCIE5+	HCSL	AA31
	CLK_100MHZ_PCIE5-		AA32
PCI Express Lane 1 Receive Bus	PCIE_PETN[1]	1.5V PCML	AC32
	PCIE_PETP[1]		AC31
PCI Express Lane 1 Transmit Bus	PCIE_PERN[1]		AB30
	PCIE_PERP[1]		AB29
PCI Express Lane 1 Reference Clock	CLK_100MHZ_PCIE6+	HCSL	L31
	CLK_100MHZ_PCIE6-		L32

LPC Interface

Description	Schematic Signal Name	I/O Standard	FPGA Pin
Data Signal	LPC_AD0	3.0V PCI	D20
	LPC_AD1		C20
	LPC_AD2		B21
	LPC_AD3		A21
Frame Signal	LPC_FRAME#		D21
Serialized Interrupt	LPC_SERIRQ		B22
Clock Control	LPC_CLKRUN#		A22
Clock (25 or 33MHz)	LPC_CLK1		D17

GPIO Interface

Description	Schematic Signal Name	I/O Standard	FPGA Pin
General Purpose 3.3V I/O	GPIO_TX1P	3.3V LVTTL / 3.3V LVCMOS	D26
	GPIO_TX1N		C26
	GPIO_TX2P		J18
	GPIO_TX2N		H18
	GPIO_TX3P		K18
	GPIO_TX3N		K17
	GPIO_TX4P		J17
	GPIO_TX4N		H16
	GPIO_TX5P		K16
	GPIO_TX5N		J16
	GPIO_TX6P		D23
	GPIO_TX6N		C23
	GPIO_TX7P		D22
	GPIO_TX7N		C22
	GPIO_TX8P		D19
	GPIO_TX8N		D18
	GPIO_RX1P		K24
	GPIO_RX1N		K25
	GPIO_RX2P		C27
	GPIO_RX2N		B27
	GPIO_RX3P		A26
	GPIO_RX3N		A25
	GPIO_RX4P		A28
	GPIO_RX4N		A27
	GPIO_RX5P		C25
	GPIO_RX5N		B25
	GPIO_RX6P		D25
	GPIO_RX6N		D24
	GPIO_RX7P		C24
	GPIO_RX7N		B24
	GPIO_RX8P		A24
	GPIO_RX8N		A23
	GPIO_CLKOUTP		K23
	GPIO_CLKOUTN		K22

HSMC Interface

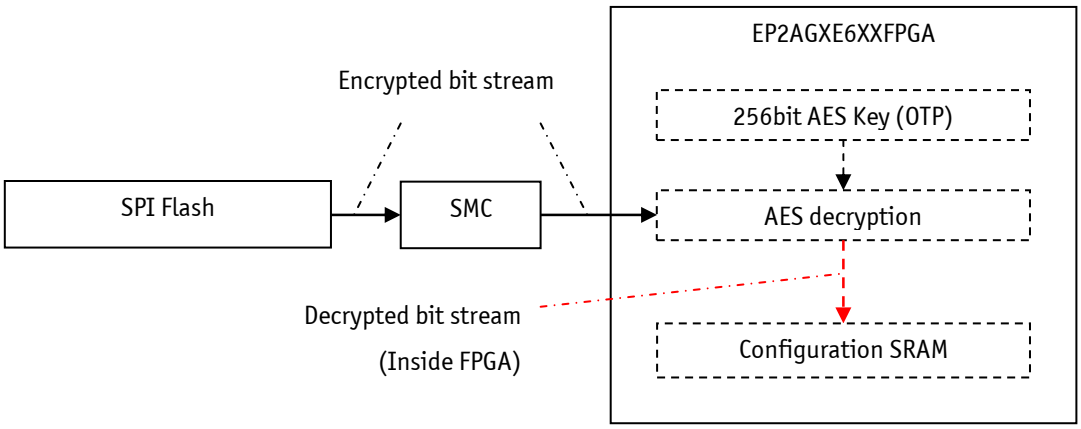
Description	Schematic Signal Name	I/O Standard	HSMC Pin	FPGA Pin
Transceiver 0 Channel 2 TX	HSMC_XCVR_TX5+	1.5V PCML	17	V29
	HSMC_XCVR_TX5-		19	V30
Transceiver 0 Channel 2 RX	HSMC_XCVR_RX5+		10	W31
	HSMC_XCVR_RX5-		12	W32
Transceiver 0 Channel 3 TX	HSMC_XCVR_TX4+		21	T29
	HSMC_XCVR_TX4-		23	T30
Transceiver 0 Channel 3 RX	HSMC_XCVR_RX4+		26	U31
	HSMC_XCVR_RX4-		28	U32
Transceiver 1 Channel 4 TX	HSMC_XCVR_TX2+		9	P29
	HSMC_XCVR_TX2-		11	P30
Transceiver 1 Channel 4 RX	HSMC_XCVR_RX3+		30	R31
	HSMC_XCVR_RX3-		32	R32
Transceiver 1 Channel 5 TX	HSMC_XCVR_TX1+		29	M29
	HSMC_XCVR_TX1-		31	M30
Transceiver 1 Channel 5 RX	HSMC_XCVR_RX1+		18	N31
	HSMC_XCVR_RX1-		20	N32
Transceiver 1 Channel 6 TX	HSMC_XCVR_TX3+		13	H29
	HSMC_XCVR_TX3-		15	H30
Transceiver 1 Channel 6 RX	HSMC_XCVR_RX0+		22	J31
	HSMC_XCVR_RX0-		24	J32
Transceiver 1 Channel 7 TX	HSMC_XCVR_TX0+		25	F29
	HSMC_XCVR_TX0-		27	F30
Transceiver 1 Channel 7 RX	HSMC_XCVR_RX2+		14	G31
	HSMC_XCVR_RX2-		16	G32
HSMC Card Management Serial Data	SMB_HSMC_DAT	2.5V	33	U1
HSMC Card Management Serial Clock	SMB_HSMC_CLK		34	U2
Dedicated CMOS Clock Out	HSMC_CLKOUT0		39	T4
Dedicated CMOS Clock In	HSMC_CLKIN0		40	D39
Dedicated CMOS I/O Bit 0	HSMC_D0_2+		41	A16
Dedicated CMOS I/O Bit 2	HSMC_D0_2-		43	A15
Dedicated CMOS I/O Bit 1	HSMC_D1_3+		42	C18
Dedicated CMOS I/O Bit 3	HSMC_D1_3-		44	B18
LVDS RX Bit 0p or CMOS Bit 5	HSMC_RX0+	LVDS or 2.5V	48	C15
LVDS RX Bit 0n or CMOS Bit 7	HSMC_RX0-		50	D15
LVDS RX Bit 1p or CMOS Bit 9	HSMC_RX1+		54	D11
LVDS RX Bit 1n or CMOS Bit 11	HSMC_RX1-		56	C11
LVDS RX Bit 2p or CMOS Bit 13	HSMC_RX2+		60	D5

Description	Schematic Signal Name	I/O Standard	HSMC Pin	FPGA Pin
LVDS RX Bit 2n or CMOS Bit 15	HSMC_RX2-		62	C5
LVDS RX Bit 3p or CMOS Bit 17	HSMC_RX3+		66	B5
LVDS RX Bit 3n or CMOS Bit 19	HSMC_RX3-		68	B4
LVDS RX Bit 4p or CMOS Bit 21	HSMC_RX4+		72	A6
LVDS RX Bit 4n or CMOS Bit 23	HSMC_RX4-		74	A5
LVDS RX Bit 5p or CMOS Bit 25	HSMC_RX5+		78	A8
LVDS RX Bit 5n or CMOS Bit 27	HSMC_RX5-		80	A7
LVDS RX Bit 6p or CMOS Bit 29	HSMC_RX6+		84	A12
LVDS RX Bit 6n or CMOS Bit 31	HSMC_RX6-		86	A11
LVDS RX Bit 7p or CMOS Bit 33	HSMC_RX7+		90	C14
LVDS RX Bit 7n or CMOS Bit 35	HSMC_RX7-		92	D14
LVDS or CMOS Clock In or CMOS Bit 37	HSMC_CLKIN1+		96	R10
LVDS or CMOS Clock In or CMOS Bit 39	HSMC_CLKIN1-		98	T10
LVDS RX Bit 8p or CMOS Bit 41	HSMC_RX8+		102	AM15
LVDS RX Bit 8n or CMOS Bit 43	HSMC_RX8-		104	AM16
LVDS RX Bit 9p or CMOS Bit 45	HSMC_RX9+		108	AM9
LVDS RX Bit 9n or CMOS Bit 47	HSMC_RX9-		110	AM10
LVDS RX Bit 10p or CMOS Bit 49	HSMC_RX10+		114	AJ9
LVDS RX Bit 10n or CMOS Bit 51	HSMC_RX10-		116	AK9
LVDS RX Bit 11p or CMOS Bit 53	HSMC_RX11+		120	AJ5
LVDS RX Bit 11n or CMOS Bit 55	HSMC_RX11-		122	AK5
LVDS RX Bit 12p or CMOS Bit 57	HSMC_RX12+		126	AJ8
LVDS RX Bit 12n or CMOS Bit 59	HSMC_RX12-		128	AK8
LVDS RX Bit 13p or CMOS Bit 61	HSMC_RX13+		132	AJ10
LVDS RX Bit 13n or CMOS Bit 63	HSMC_RX13-		134	AK10
LVDS RX Bit 14p or CMOS Bit 65	HSMC_RX14+		138	AJ12
LVDS RX Bit 14n or CMOS Bit 67	HSMC_RX14-		140	AK12
LVDS RX Bit 15p or CMOS Bit 69	HSMC_RX15+		144	AJ11
LVDS RX Bit 15n or CMOS Bit 71	HSMC_RX15-		146	AK11
LVDS RX Bit 16p or CMOS Bit 73	HSMC_RX16+		150	AJ13
LVDS RX Bit 16n or CMOS Bit 75	HSMC_RX16-	LVDS or 2.5V	152	AK13
LVDS or CMOS Clock In or CMOS Bit 77	HSMC_CLKIN2+		156	AD16
LVDS or CMOS Clock In or CMOS Bit 79	HSMC_CLKIN2-		158	AE16
LVDS TX Bit 0p or CMOS Bit 4	HSMC_TX0+		47	J11
LVDS TX Bit 0n or CMOS Bit 6	HSMC_TX0-		49	H12
LVDS TX Bit 1p or CMOS Bit 8	HSMC_TX1+		53	C9
LVDS TX Bit 1n or CMOS Bit 10	HSMC_TX1-		55	B9
LVDS TX Bit 2p or CMOS Bit 12	HSMC_TX2+		59	D6
LVDS TX Bit 2n or CMOS Bit 14	HSMC_TX2-		61	C6

Description	Schematic Signal Name	I/O Standard	HSMC Pin	FPGA Pin
LVDS TX Bit 3p or CMOS Bit 16	HSMC_TX3+		65	C8
LVDS TX Bit 3n or CMOS Bit 18	HSMC_TX3-		67	B8
LVDS TX Bit 4p or CMOS Bit 20	HSMC_TX4+		71	D8
LVDS TX Bit 4n or CMOS Bit 22	HSMC_TX4-		73	D7
LVDS TX Bit 5p or CMOS Bit 24	HSMC_TX5+		77	K11
LVDS TX Bit 5n or CMOS Bit 26	HSMC_TX5-		79	K10
LVDS TX Bit 6p or CMOS Bit 28	HSMC_TX6+		83	D10
LVDS TX Bit 6n or CMOS Bit 30	HSMC_TX6-		85	D9
LVDS TX Bit 7p or CMOS Bit 32	HSMC_TX7+		89	C13
LVDS TX Bit 7n or CMOS Bit 34	HSMC_TX7-	LVDS or 2.5V	91	B14
LVDS or CMOS Clock Out or CMOS Bit 36	HSMC_CLKOUT1+		95	A20
LVDS or CMOS Clock Out or CMOS Bit 38	HSMC_CLKOUT1-		97	A19
LVDS TX Bit 8p or CMOS Bit 40	HSMC_TX8+		101	AE12
LVDS TX Bit 8n or CMOS Bit 42	HSMC_TX8-		103	AE13
LVDS TX Bit 9p or CMOS Bit 44	HSMC_TX9+		107	AC13
LVDS TX Bit 9n or CMOS Bit 46	HSMC_TX9-		109	AD13
LVDS TX Bit 10p or CMOS Bit 48	HSMC_TX10+		113	AL8
LVDS TX Bit 10n or CMOS Bit 50	HSMC_TX10-		115	AM8
LVDS TX Bit 11p or CMOS Bit 52	HSMC_TX11+		119	AL7
LVDS TX Bit 11n or CMOS Bit 54	HSMC_TX11-		121	AM7
LVDS TX Bit 12p or CMOS Bit 56	HSMC_TX12+		125	AL10
LVDS TX Bit 12n or CMOS Bit 58	HSMC_TX12-		127	AL11
LVDS TX Bit 13p or CMOS Bit 60	HSMC_TX13+		131	AC11
LVDS TX Bit 13n or CMOS Bit 62	HSMC_TX13-		133	AD11
LVDS TX Bit 14p or CMOS Bit 64	HSMC_TX14+		137	AM11
LVDS TX Bit 14n or CMOS Bit 66	HSMC_TX14-		139	AM12
LVDS TX Bit 15p or CMOS Bit 68	HSMC_TX15+		143	AC12
LVDS TX Bit 15n or CMOS Bit 70	HSMC_TX15-	LVDS or 2.5V	145	AD12
LVDS TX Bit 16p or CMOS Bit 72	HSMC_TX16+		149	AJ14
LVDS TX Bit 16n or CMOS Bit 74	HSMC_TX16-		151	AK14
LVDS or CMOS Clock Out or CMOS Bit 76	HSMC_CLKOUT2+		155	AC15
LVDS or CMOS Clock Out or CMOS Bit 78	HSMC_CLKOUT2-		157	AC16

7.4 FPGA Design Security

To protect the FPGA configuration bit stream from tampering and reverse-engineering, the configuration can be AES encrypted. The FIPS-197 certified AES algorithm uses a 256bit security key. The security key is stored in a one-time programmable store inside the FPGA and can be programmed using the JTAG adapter. The secure key cannot be read out.



For more information visit the Altera homepage: http://www.altera.com/literature/hb/arria-ii-gx/aiigx_51009.pdf

8 Appendix B: Document Revision History

Revision	Date	Edited by	Changes
100	10.Feb.2011	SCM	Initial version.
101	20.Feb.2011	SCM	Driver installation section added.
102	01.Feb.2011	SCM	Jumper & BIOS "F7" sections added.
103	21.Feb.2011	SCM	FPGA Information (DIP) and System Controller sections (VIV) added.
104	17.Mar.2011	BAJ	Corrected language and style.
105	23.Mar.2011	WAS	Formatting and grammar check.
106	29.Mar.2011	LOM	Minor corrections.
107	12.Apr.2011	BAJ	Exploded assembly drawing & MSMST available options added.
108	29.Nov.2011	WAS/AVM	Formatting changes to Kontron CI. Bottom assembly photo rotated to match diagram; Appendix A, HSMC pins corrected.
109	02.Apr.2012	WAS	New title photo. Assembly diagrams enhanced. BIOS Update section corrected. Permanently programming the FPGA section added.

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