cPCI-MXP64

6U CompactPCI® 64-bit Peripheral Processor

Technical Reference Manual
Version 1.4, February 2003

Note: The latest releases of the Technical Reference Manuals are available at:
ftp://ftp.kontron.ca/Support

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DOCUMENTATION SURVEY

cPCI-MXP64 – Technical Reference Manual

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ADDITIONAL COMMENTS

FCC Compliance Statement

Warning

Changes or modifications to this unit not expressly approved by the party responsible for the compliance could void the user's authority to operate this equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his or her own expense.

European Statement

Warning

This is a class B product. If not installed in a properly shielded enclosure, and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his or her own expense.

Safety Standard

UL Recognized Component, File # E186339 vol. 1 section 2

Care and handling precautions for Lithium batteries

- Do not short circuit
- Do not heat or incinerate
- Do not charge
- Do not deform or disassemble
- Do not apply solder directly
- Do not mix different types or partially used batteries together
- Always observe proper polarities

READ ME FIRST

Your computer board has a standard non-rechargeable lithium battery. To preserve the battery lifetime, **the battery enable jumper is removed when you receive the board.**

EXERCISE CAUTION WHILE REPLACING LITHIUM BATTERY

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

ATTENTION

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie.

Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabriquant.

ACHTUNG

Explosionsgefahr bei falschem Batteriewechsel. Verwenden Sie nur die empfohlenen Batterietypen des Herstellers. Entsorgen Sie die verbrauchten Batterien laut Gebrauchsanweisung des Herstellers.

ATENCION

Puede explotar si la pila no este bien reemplazada.

Solo reemplazca la pila con tipas equivalentes segun las instrucciones del manifacturo. Vote las pilas usadas segun las instrucciones del manifacturo.

IMPORTANT

J1 and J2 pinout is as per PICMG standard.

J3 and J5 pinout is user-defined and varies between various manufacturers. Contact our Technical Support to verify pinout compatibility with other chassis backplane vendors.

POWERING-UP THE BOARD

If you should encounter a problem, verify the following items:

Make sure that all connectors are properly connected.

Check your boot diskette.

If the board still does not start up properly, you should try booting your system with the cPCI-MXP64 installed in the system, a monitor and a keyboard connected to the board. This is the minimum required to verify the board's operation.

If you still are not able to verify your board, please refer to the emergency Procedure in the Appendix Section.

If you still are not able to get your board up and running, contact our technical Support department for assistance.

PREVENTING VIRUSES

Kontron Inc. takes every precaution against computer viruses. To safeguard against computer viruses in general, do not freely lend your diskettes and regularly perform virus scans on all your computer systems.

ADAPTER CABLES

While adapter cables are provided from various sources, the pinout is often different. The direct crimp design offered by Kontron allows the simplest cable assembly. All cables are available from Kontron Sales Department.

UNPACKING AND SAFETY PRECAUTIONS

STATIC ELECTRICITY

Since static electricity can cause damage to electronic devices, the following precautions should be taken:

1. Keep the board in its anti-static package, until you are ready to install it.
2. Always touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
3. Handle the board by the edges.

Storage Environment

Electronic boards are sensitive devices. Do not handle or store devices near strong electrostatic, electromagnetic, magnetic or radioactive fields.

Power Supply

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

Unpacking

Follow these recommendations while unpacking:

1. After opening the box, save it and the packing material for possible future shipment.
2. Remove the board from its anti-static wrapping and place it on a grounded surface.
3. Inspect the board for damage. If there is any damage or missing items, notify Kontron immediately.

When unpacking you will find:

1. One cPCI-MXP64, 6U CompactPCI® Peripheral Processor.
2. One Quick Reference sheet
3. One CDROM containing drivers.

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1.1. PRODUCT SPECIFICATIONS

Kontron's 6U CompactPCI® peripheral processor, featuring scalable multiprocessing and the highest level of hot-swap capability, is the ideal peripheral processor for data/telecommunication, CTI, and industrial control/monitoring markets.

The cPCI-MXP64 6U CompactPCI peripheral processor brings scalable multiprocessing capability to the telecom and industrial automation markets. It is designed to operate as a "slave" processor and can be installed in any CompactPCI peripheral slot where a standard system processor, such as Kontron's cPCI-MXS64 or cPCI-CXS, drives the system slot. The cPCI-MXP64 is also stand-alone operation capable, i.e., it is capable of operation in systems were no system processor is installed.

Fully hot-swappable, the cPCI-MXP64 communicates with other processor boards using the CompactPCI backplane as the physical layer of a 1 Gb/s Ethernet.

To provide the necessary interconnect, Kontron developed IPTalky, a series of IP-Stacks that currently support local versions of the following OSs: Microsoft Windows NT, Microsoft Windows 2000, Linux, VxWorks and pSOS. Using the cPCI-MXP64's scalability, up to 15 loosely coupled x86 processors can be operated simultaneously in a single 19" CompactPCI system.

Multi-level PCI-to-PCI bridging is fully supported. Based on Intel's 21554 PCI-to–PCI non-transparent bridge, the feature set of the cPCI-MXP64 includes a rich selection of standard peripherals.

The cPCI-MXP64 offers a natural growth path to high performance, high availability as well as hot swap and scalable multiprocessing technology.

The cPCI-MXP64 can be ordered in either front I/O interfacing (video, serial port, 2xEthernet, all available on the face plate) or rear I/O interfacing through CPCI I/O connectors J3 and J5 (no interconnection capability on the face plate).

CompactPCI Connectors

Rear I/O CPCI connectors are PICMG 2.0 Rev 3.0 compliant. CompactPCI connectors are located at the rear edge of the processor board. The complete CPCI connector configuration of the cPCI-MXP64 is composed of four connectors referred to as J1, J2, J3, and J5.

Their function is described below:

J1	32 bit PCI signaling, power
J2	64 bit extension, arbitration, clocks, reset and. power
J3/J5	handle I/O signals.

CompactPCI™ connectors are also known as 2mm Hard Metric connectors.

1.2. CPCI-MXP64 TECHNICAL SPECIFICATIONS SHEET

Features	Description
CPU	• Pentium III processor Low Power 400MHz and 500MHz
Cache	• 16K/16K Instruction / Data CPU-internal Level 1 • 256KB 64-bit wide on-die Level 2 pipelined burst
Chipset	• Intel 440BX AGP set
Bus Interfaces	• Front side bus 100MHz • CompactPCI® Bus, 32-bit (33MHz) J1 and J2 • PCI-to-PCI 64-bit non-transparent bridge; Intel's 21554 • PCI Mezzanine Card (PMC) • cMC series mezzanines with PCI bus, Floppy and EIDE HD support • SMBus, IPMI compliant (for system management of CPU temperature monitoring, DRAM control, Clock buffers and power control)
Memory	• Three 168-pin latching DIMM sockets, 64/72-bit (in 4HP configuration, uses Kontron's memory module) • Up to 768MB of SDRAM with parity or ECC (for single bit error correction and double bit error detection)
Data Path	• 64-bit on CPU and video memory; 32-bit on local PCI and 32/64-bits on CompactPCI bus
Interrupts	• 11 edge/level sensitive and configurable • 4 PCI level sensitive, configurable to any interrupt vector for PnP compatibility
Flash Memory	• 512KB for BIOS field upgrade • Silicon Serial ID TAG for unique board identification accessible via software
I/O	• SMC FDC37C672 • USB Ports : Two • Serial Ports: Two (one RS-232, COM1, COM2 configurable as RS-232/422/485 • Parallel Port : One bi-directional with all IEEE 1284 protocols supported with BIOS selectable IRQs and addressing • Floppy Disk: Support for two drives (360KB to 1.44MB) • EIDE: One channel Bus Master PCI EIDE; support for two IDE drives (type 1 to 4, master/slave configuration); LBA, PIO Mode 0-4 and Ultra DMA/33

cPCI-MXP64 Technical Specifications Sheet (cont'd)

Features	Description
I/O (cont'd)	• CompactFlash™ Module: Optional bootable CompactFlash™ disk interfaces to primary EIDE channel, user upgradeable, master/slave • Ethernet: Two Ethernet, PCI 10/100Base-TX ports Intel 82559 controller) • HD/FD Mezzanine Card: Optionally onboard using Kontron's cMC series mezzanine cards
Video	• 64-bit AGP video controller (Intel 69000) with 2MB on die video memory • CRT resolutions up to 1024x768x64K colors or 1280x1024x256 colors
Clock/Calendar	• Real-time clock with (replaceable) battery backup • CMOS RAM
Connectors in "Front" configuration	• CRT (15-pin D-sub); serial COM1 (9-pin D-sub); two Ethernet ports (RJ-45 with link/activity indicators); PS/2 mouse/keyboard (6-pin mini-Din)
Rear I/O on J3 and J5	• CRT; 2x serial; 2 x USB; 1 x parallel; SMBus; I2C; speaker I/F; Reset; IR; 2 x Ethernet; PS/2 mouse; keyboard; 1 x EIDE; floppy disk interface; fan fail monitoring
BIOS Features	• Award Elite BIOS in Boot Block Flash with emergency recovery code; save CMOS in Flash option, and boot from LAN capability • Auto configuration, extended setup; • CC000-E0000 address blocking; PnP tables • Setup console redirection to serial port (VT100 mode) with CMOS setup access • Software enable/disable of onboard Ethernet; hardware enable/disable of onboard video • Diskless, keyboardless, and videoless operation extensions • System, video, and LAN BIOS shadowing system, video, LAN and option BIOS shadowing • Programmable bus and I/0 speeds and memory wait states • Advanced Configuration and Power Interface (ACPI 1.0), Advanced Power Management (APM 1.2), advanced thermal management (resume, overheat alarm and auto slow down), and Green support
Supervisory	• Two-stage software programmable Watchdog timer drives NMI on first stage and system reset on second stage • Programmable CPU temperature monitor alarm • Power failure/low battery detector • Front Panel LEDs: IDE activity, Ethernet activity and link and hot swap status.

cPCI-MXP64 Technical Specifications Sheet (cont'd)

Features	Description
OS Compatibility	• MS-DOS™, Windows® 95/98, Windows® NT, Windows2000, VxWorks™, pSOS™, QNX™, Linux, and Solaris
PICMG compliance	• Mechanical : compliant to IEEE 1101.10; compliant to PICMG 2.0 R3.0 and PICMG 2.1
Form Factor	• 233 x 160 x 41 mm / 9.2 x 6.3 , 1.6 in; 6U x 8HP (dual slot) Mechanically • 233 x 160 x 20.5 mm / 9.2 x 6.3 , 0.8 in; 6U x 4HP (single slot) Mechanically
Power Requirements	• Supply Voltages: +3.3V ±5% +5V±5% +12V±5% • Supply Current * : 3.3V: 4.5 Amps max. 5V: 3 Amps max. 12V: 0.01 Amps max. -12V: 0.01 Amps max. • Power Dissipation: 40W max. ***** *Pentium III processor Low Power 500MHz with 768MB SDRAM***.**
Environmental	**Operating** / **Storage and Transit** Temp.: 0-60°/32-140°F (w/ 150LFM airflow) / -40° to +70° / -40° to 158°F Humidity 5% to 95% @ 40°C/104°F non-condensing / 5% to 95% @ 40°C/104°F non-condensing Altitude 4,572m / 15,000ft Shock Designed to meet IEC 68-2-27 Vibration Designed to meet IEC 68-2-6
Reliability	• MTBF:> 100,000 hours 55°C/131°F (MIL-HDBK-217F) • Board serial number in EEPROM • USB, keyboard, mouse voltage protected by self-resetting fuses • 2 year limited warranty
Safety	• Designed to meet or exceed UL 1950; CSA C22.2 No 950; EN 60950; IEC950
EMI/EMC	• FCC 47 CFR Part 15/CISPR22, Class B; CE Mark to EN55022/EN50082

1.2.1 Power requirements

The power requirements for the cPCI-MXP64 are specified as follows:

CPU	VCORE	Frequency (in MHz) Int. / Ext.	Power MAX (in Watts) 3.3V/5V	Power TYP (in Watts) 3.3V/5V	Power SUS (in Watts) 3.3V/5V	Ambient temp. MAX
PIII, 400MHz	1.35 V	400 / 100	16.2 / 10.3	8.8 / 7.1	6.6 / 1.2	60°C
PIII, 500MHz	1.60 V	500 / 100	16.5 / 15.9	8.8 / 9.5	6.7 / 1.3	60°C
Where :						
Power MAX	Running memory benchmark in Windows NT for 3.3Volts Running Hiwpwr30 in Windows NT for 5Volts					
Power TYP	At DOS prompt					
Power SUS	At DOS prompt					
Test condition	256MB SDRAM, mezzanine with hard disk drive					

1.3. HOT SWAP CAPABILITY

The cPCI-MXP64 is Hot Swappable, which means it can be installed and removed under power.

Hot Swap consists of two (2) distinct elements:

1- Hardware Connection Layer,
2- Hot-Swap Services.

Upon insertion of the board the hardware connection layer will power-up and initialize the board, the Hot-Swap Services provide the means for reconfiguring the system.

High Availability: Under PICMG 2.1 Hot Swap specifications 3 levels of hot swap have been defined:

Level 1 Basic hot swap;
Level 2 Full hot swap;
Level 3 High availability.

The cPCI-MXP64 is compliant to level 3, PICMG's highest hot swap level.

Hardware Connection Layer: Electrically, 3 pins are dedicated to hot swap functionality. They are BD_SEL#, HEALTHY# and PCI_RST#.

BD_SEL# It is the shortest pins. This pin is the last to mate and the first to break contact. This ensures that the sensing of its connection takes place at a time when all other pins are reliably connected. It has two functions:

1- It is used to indicate to the CompactPCI® system that a board is properly inserted in a particular slot;
2- It allows the CompactPCI® system to power up/down a particular board.

HEALTHY# Once a CompactPCI® board is properly inserted and powered, this signal is used to indicate its readiness for operation. In cases of failure, this pin can be used to indicate such an instance to the rest of the CompactPCI® system.

PCI_RST# As defined by the CompactPCI® Specification, this is a signal on the backplane, driven by the system host. Platforms may implement this signal as a radial signal from the Hot Swap Controller to further control the electrical connection process. Platforms that do this must OR the system host's reset signal with the slot specific signal to maintain the bussed signal's function.

The Hot Swap Services interface with the rest of the system via the ENUM# signal, a switch located in the CompactPCI® insertion/extraction handle as well as a Blue LED.

Hot Swap Level 3 compliant boards use the ENUM# signal to indicate a service request to the CompactPCI® system processor. This signal is provided among other things, to notify the system processor that either a board has been newly inserted or is about to be extracted. This signal informs the system processor that the configuration of the system has changed or is about to change. The system processor is then free to perform any necessary maintenance such as installing/removing device drivers. The application that is using the resources of the particular board can also be notified of the change.

The Hot Swap Switch implemented in the CompactPCI® handle allows the operator to start the extraction sequence. A blue LED, located on the faceplate, is illuminated when it is safe to extract the board. This LED indicates that the system software has been placed in a state for orderly extraction of the board. The hardware connection layer provides protection only for the hardware during insertions and extractions.

All actions are initiated by the operator, and must be performed in the correct sequence for proper system operation.

Hot Swap level 3 complaint boards present the following resources to software executing on the system host (nominally implementing the Hot-Swap Services and Hot-Swap System Driver)

- An ENUM# signal, which is an open collector (open drain) bussed signal, to signal a change in status for the board.
- A switch actuated with the lower ejector handle, indicating the beginning of the extraction process or end of the insertion process.
- A blue LED located on the faceplate of the compliant board is used to indicate the status of the software connection process.
- A set of four control and status bits (located in the I21554 bridge chip) on each compliant board allows the system host's software to determine the source of the ENUM# signal and control the LED.

High Availability compliant boards support the full range of system capabilities.

1.4. INTERFACING WITH THE ENVIRONMENT

1.4.1 CPCI

The cPCI-MXP64 peripheral processor allows rack-mounted systems to offer a high level of modularity.

NOTE

The cPCI-MXP64 is available in two (2) base configurations: front I/O and rear I/O configuration.

A. In front I/O configuration, the following I/Os are supported on the faceplate only: SVGA, Ethernet 1 and 2, and PMC access. All other I/Os are connected to J3 and J5.

B. In Rear I/O configuration,

- All I/O signals are connected to J3 and J5
- The cPCI-MXP64 is compatible with Kontron's standard cTM80-STD2S and cTM80-STD1S transition modules.

1.4.2 Mezzanines

The cPCI-MXP64 supports two types of mezzanine cards: one industry-standard PMC mezzanine as well as Kontron's cMC series of mezzanine cards. The PMC mezzanine can be installed on single and dual slot versions of the cPCI-MXP64. The cMC series of mezzanines only fit on the dual slot versions of the cPCI-MXP64. The two mezzanines, the PMC and the cMC can be operated simultaneously on the dual-slot version of the cPCI-MXP64.

The following interfaces are provided by the cPCI-MXP64 for Kontron's cMC series of mezzanines: PCI bus, IDE and floppy.

A complete *CompactPCI* development system, the CxP0816 is also available from Kontron.

1.5. COMPATIBILITY WITH KONTRON PRODUCTS

The cPCI-MXP64 Peripheral Processor is a member of the Kontron's CompactPCI product family.

The board is fully compliant with the PICMG 2.0 Rev.3.0 and PICMG 2.1 CompactPCI specifications.

When building a basic environment around the cPCI-MXP64, the platform may be composed of any of the following devices:

- cPCI-MXS series, 6U System Processor
- cPCI-CXS 6U System Processor
- cMC Mezzanine card with hard disk and floppy disk drive for the System Processor and/or the Peripheral Processor(s).
- cMCB Mezzanine card with bridge, hard disk and floppy disk for the System Processor.
- cSM-CDHD Storage module with CD and Hard Disk
- cSM-CD Storage module with CD only
- CxP0816 including
    - 8U 19-inch enclosure
    - Front loaded hot swappable 2U fan tray
    - Power supply (300W ATX or 350W AC or DC in single or redundant configuration)
    - One of the following backplanes

        cBP-08R : 8 slots CompactPCI (PICMG 2.1)

        cBP-16R, 16 slots CompactPCI (PICMG 2.1)
- cTM80-STD2S 6Ux8HPx80mm Dual slot Rear Transition Module, standard pinout.
- cTM80-STD1S 6Ux4HPx80mm Single slot Rear Transition Module, standard pinout.

1.6. MEZZANINE CARD CONCEPT

The cPCI-MXP64 supports two type of Mezzanine cards: industry standard PCI Mezzanine Cards (PMC) as well as Kontron's cMC series of mezzanine cards.

A fully equipped cPCI-MXP64 board may appear as follows:

1.6.1 Kontron's cMC Mezzanine Concept

This is Kontron's concept to expand the I/O capability of the board. It is built around two connectors:

- Mezzanine connector handling IDE and floppy disk drive signals.
- Mezzanine connector handling a complete PCI signal set (primary bus) including the REQ/GNT arbitration signal pair.

These two connectors represent an open door for future development of expansion and I/O mezzanine cards.

Kontron developed two series of mezzanine cards: the cMC and the cMCB series. The cPCI-MXP64 supports the cMC series.

1.6.2 PMC Concept

PCI Mezzanine Card (PMC) is an industry-standard specification that allows PCI based I/O devices to be added to a number of PMC supporting devices, including Kontron's cPCI-MXP64. It conforms to the ANSI/IEEE P1386.1 specification that defines Standard Physical, Environmental and electrical Layers for PMC devices.

The cPCI-MXP64 features the PMC support onboard to provide an extra method to expand the 32-bit I/O capabilities of the cPCI-MXP64.

PMC devices connect directly to standard PMC connectors. A mechanical cutout (with its EMI proof cap) is provided to allow integrated connectors and indicators to be available directly on the front plate through PMC card.

1.6.3 CompactFlash Feature

The cPCI-MXP64 boards also support standard CompactFlash disk through a CompactFlash carrier module. CompactFlash is a widely available non-volatile memory device electrically configured in a way as to interface directly through IDE. It is supported on the board as a standard IDE drive and connects to the primary EIDE interface.

The CompactFlash disk can be set as a Master or Slave device and combined with any EIDE standard hard disk drive via W11 jumper setting (see Section .3.1., setting jumpers).

The CompactFlash module is installed using the cPCI-MXP64 on-board J13 connector. For more information on CompactFlash installation and setups, please refer to Section .2.1. – *CompactFlash Interface*.

PART 2

2. ONBOARD FEATURES

1. COMPACTFLASH INTERFACE
2. ENHANCED IDE INTERFACES
3. ETHERNET INTERFACES
4. FLOPPY DISK INTERFACE
5. PS/2 KEYBOARD AND MOUSE INTERFACE
6. PARALLEL PORT
7. POWER MANAGEMENT
8. SERIAL PORTS
9. THERMAL MANAGEMENT
10. USB INTERFACES
11. VIDEO INTERFACES

2.1. COMPACTFLASH INTERFACE

The cPCI-MXP64 board supports an IDE compatible flash disk by using a CompactFlash carrier module. CompactFlash (C-Flash) disks are the resident industry-standard ATA/IDE subsystem for application, data, image, and audio storage. They have the same functionality and capabilities as intelligent disk drives, but with the advantages of being very compact, rugged (typical M.T.B.F. is 1,000,000 hours) and low power. The cPCI-MXP64 supports all CompactFlash sizes presently available and future sizes when available.

The C-Flash disk connects on the cPCI-MXP64 via the onboard Flash Disk connector.

Related Jumpers

W11 to set the CompactFlash disk as master or slave.

BIOS Settings

Section 4.1.2 Main Menu: Hard Disk autodetect to set the type of hard disk.

The CompactFlash disk connects directly on the primary EIDE interface. It must be configured the same way as a standard hard disk using the BIOS setup program (Autodetect function).

To setup the CompactFlash disk for Master or Slave configuration, use the CompactFlash jumper (W11) located on the peripheral processor.

To locate and install this jumper, please refer to Section .3.1, *Setting Jumpers*.

NOTE

Since CompactFlash devices use the ATA/IDE interface, no specific flash disk driver is required for various operating systems.

2.2. ENHANCED IDE INTERFACES

The cPCI-MXP64 board features one channel Bus Master PCI EIDE dedicated to Primary IDE logical interface. The channel supports up to two IDE devices (including CD-ROMs, hard disks, CompactFlash) with independent timings, in Master/Slave combination.

Signal Paths

The primary IDE interface is available on the CPCI I/O connectors, the mezzanine connector and the Compact Flash connector.

Related Jumpers

None

BIOS Settings

Section 4.1.10 Integrated Peripherals.

The IDE interface supports PIO mode 4 transfers up to 14MB/sec and Bus Master IDE transfer up to 33MB/sec (Ultra-DMA 33). It does not consume any ISA DMA resources and integrates 16x32-bit buffers for optimal transfers.

CAUTION

When connecting IDE devices to the Primary IDE interface, Master and Slave devices must be shared in respect of the device allocation on both the CPCI I/O connector and the mezzanine

Two Master devices (or two Slave devices) must not be installed on the same interface at the same time.

2.3. ETHERNET INTERFACE

The Ethernet controllers are electrically connected to the Primary PCI bus. They support 10Base-T and 100Base-TX operations: 10Mbps and 100Mbps network speeds are automatically detected and switched.

Signal Path

The Ethernet interfaces are available through either the CPCI I/O connector J3 or the Front Panel connectors.

Related Jumpers

None.

BIOS Settings

Section 4.1.10 Integrated Peripherals: Enable/Disable Ethernet Controller.

2.3.1 Front I/O Configuration

The Ethernet interfaces are available on a face plate connectors only when the board is ordered for front I/O configuration. Activity and link indicators are built in the connector.

2.3.2 Rear I/O Configuration

The Ethernet signals are available on CPCI I/O connectors only when the board is ordered for rear I/O configuration. When using this configuration, a Rear Transition Module (RTM) is required to get access to Ethernet signals.

2.3.3 Boot from LAN

The Boot from LAN capability is supported. To enable the option, use the BIOS Setup program. Please refer to Section 4.1 -BIOS Setup Program.

When Enabled, the BIOS attempts to boot from a LAN boot image before it attempts to boot from a local storage device.

2.3.4 Drivers

A CDROM entitled is included with the cPCI-MXP64.

It contains network drivers for most common operating systems.

2.4. FLOPPY DISK INTERFACE

The onboard floppy disk controller is IBM PC XT/AT compatible. It handles 3.5" and 5.25", low and high density disks. Up to two drives are supported in any combination.

Signal Paths

The Floppy Disk Controller interface is available through the CPCI I/O connectors and through the Mezzanine connector (see section3.6 CPCI I/O signals and 3.3.6 Onboard Connectors and Headers).

Related Jumpers

None.

BIOS Settings

Section 4.1.4 Standard CMOS: Select type of floppy.
Section 4.1.10 Integrated Peripherals: Enable/Disable onboard FDC Controller.

2.5. PS/2 KEYBOARD / PS/2 MOUSE INTERFACE

The onboard keyboard controller is 8042 software compatible. PS/2 Keyboard and mouse signals are available through an output that supports direct connection to the interface. Since signals of both devices are combined on the same connector, a Y-cable is required to split the signals and feed a standard AT keyboard and a PS/2 mouse.

Signal Path

PS/2 keyboard and PS/2 mouse signals are available through J5 CPCI I/O connector in rear I/O configuration or on the mini-Din connector on the face plate in front I/O configuration.

Related Jumpers

None.

BIOS Settings

Section 4.1.10 Integrated Peripherals : USB Keyboard Support; PS/2 Mouse Function Control

2.6. PARALLEL PORT

The cPCI-MXP64 features one IEEE-1854 multi-mode parallel port. It is compatible with Standard Mode IBM PC/XT, PC/AT, and PS/2 compatible bi-directional parallel port, Enhanced Parallel Port (EPP), and Enhanced Capabilities Port (ECP).

Signal Path

The Parallel Port interface is only available through J5 CPCI I/O connector.

Related Jumpers

None

BIOS Settings

Section 4.1.10 Integrated Peripherals: Onboard Parallel Port; Parallel Port Mode

The differences between Standard, EPP, and ECP modes appear in the signal assignation of the pins on the connector. Differences are described as follows:

Pin Number (J5)	Standard Mode	EPP Mode	ECP Mode
A15	SLCT	-	SLCT
B15	PE	-	PERROR[1], ACKREVERS[2]
C15	BUSY	WAIT	BUSY[1], PERIPHACK[2]
D15	ACK#	INTR#	ACK#
E16	SLCTIN#	ADDRSTRB#	SLCTIN#
B17	INIT#	-	INIT[1]#, REVERSERQST[2]#
D17	ERR#	-	FAULT[1]#,PERIPHRQST[2]#
A18	ALF	DATASTB	ALF[1], HOSTACK[2]
E17	D0	D0	D0
C17	D1	D1	D1
A17	D2	D2	D2
D16	D3	D3	D3
C16	D4	D4	D4
B16	D5	D5	D5
A16	D6	D6	D6
E15	D7	D7	D7

[1] Compatible mode

[2] High Speed Mode

NOTE

To operate in EPP or ECP mode, ensure the peripheral is designed to work in this mode and the BIOS setup is configured to support it.

2.6.1 Standard Mode

The Standard mode is unidirectional. It is supported to maintain the compatibility with the IBM PC standard.

2.6.2 EPP Mode

The EPP (Enhanced Parallel Port) mode consists of a hardware independent method of accessing a parallel port configured as EPP. It provides support for single I/O cycle as well as the high performance block I/O transfers. The EPP mode always uses the most optimum method for I/O transfers. For example, if the hardware supports it, EPP mode will perform 32-bit I/O block transfers.

EPP mode assumes that the parallel port can be used to connect more than one peripheral device using multiplexor or daisy chain configurations.

A multiplexor is an external device that permits up to eight parallel port devices to share a single parallel port.

A daisy chain device has two ports: input and output. The input port is connected either to the host parallel port or the daisy chain device in front of it. The output is used to connect the next peripheral device to the daisy chain. The last device, however, can be one without daisy chain support.

2.6.3 ECP Mode

ECP (Extended Capabilities Port) works the same as EPP mode, but it will take precedence over the EPP mode when addressing multiple logical devices in a single physical product. While the EPP mode may intermix read and write operations without any overhead or protocol handshaking, the ECP mode negotiates data transfers using a request from the host and an acknowledgment from the peripheral.

> NOTE
>
> For more information on the ECP protocol, please refer to the Extended Capabilities Port Protocol and ISA Interface Standard (available from Microsoft Corporation) or contact our Technical Support department (See appendix G).

2.7. POWER MANAGEMENT

Power Management features are supported at the BIOS level. All Power Management options are described in Section 4.1.7 – *Power Management Setup*.

2.8. SERIAL PORTS

Two serial ports are provided on the board for asynchronous serial communications. They are 16C550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 50bps to 115Kbaud.

Each serial port is specified as follows:

Designation	Communication Mode	Output Path
Serial Port 1	RS-232	Front Plate DB-9, CPCI J5
Serial Port 2	RS-232, Infrared	CPCI J3

UART registers are individually addressable and fully programmable.

2.8.1 Serial Port 1

Serial Port 1 is buffered directly for RS-232 operation. Signals include the complete signal set for handshaking, modem control, interrupt generation, and data transfer. When assigned as COM1, the port is 100% compatible with the IBM-AT serial port in RS-232 mode.

Signal Path

Serial Port 1 signal path depends on the output configuration you have ordered for the board. In front I/O configuration, COM1 is available on a DB9 connector on the face plate. IN rear I/O configuration, COM1 signals are available on the CPCI connectors.

Related Jumpers

W2 – Remote reset on COM1 or COM2 is enabled or disabled

BIOS Settings

Section 4.1.10 Integrated Peripherals : Enable/Disable Onboard FDC Controller;
Select Com Port Address of COM1

2.8.2 Remote Reset

A remote hardware reset of the cPCI-MXP64 is possible by sending a break on the serial port 1 or 2 (see section 3.1 for Remote Reset jumper setting). A break is simply an abnormally long start bit (100ms or more) on the incoming data line. A break signal is embedded in the data, so no special wire is required.

Related Jumpers

W2 Selects whether the serial port 1 or 2 is used to control the remote reset or disables this option.

BIOS Settings

None

The remote reset will work in RS-232 and RS-422 modes. It will also work with a modem, since the modem will repeat the break signal over the telephone network. All major telecommunication software have the capability of sending a break signal, usually by pressing the CTRL-B keys or the ALT-B keys on the keyboard.

Only a standard telephone line and a modem in auto-answer mode are needed. The only limitation is that the communication speed must be 1200bps or more. If the communication speed is to slow, a false reset can occur.

The break signal is entirely detected by hardware.

2.8.2.1 Front I/O Configuration

For truly remote operation, use the VT-100 mode, which allows remote BIOS setup and console redirection.

The serial port 1 signals are available through a DB-9 connector located on the front plate and is labeled as COM1.

2.8.2.2 Rear I/O Configuration

The complete signal set is tied to the J5 CPCI I/O connector to be used through the Rear Transition Module (RTM).

2.8.3 Serial Port 2

The serial port 2 is buffered directly for RS-232, RS-422 or RS-485 operations and is 16C550 PC-Compatible. The interface includes the complete signal set for handshaking, modem control, interrupt generation, and data transfer.

The serial port 2 is 100% compatible with the IBM-AT serial port.

Signal Path
Serial Port 2 signals are only available through the J5 CPCI I/O connector

Related Jumpers
None

BIOS Settings
Section 4.1.10 Integrated Peripherals: Onboard Serial Port 2

Upon a power-up or reset, the serial port 2 interface circuits are automatically configured for the operation mode setup in the BIOS. The Serial Port 2 signal assignation on the J5 CPCI I/O connector depends on the operation mode (RS-232, RS-422, or RS-485) it has been set.

2.8.3.1 Infrared Mode:

Infrared (IR) interface signals are provided to drive IR module for remote operations through Serial Port 2 or CPCI I/O connector J3 (IRTX and IRRX). When set in IR mode, the IR interface supports multi-protocol infrared operations. The IR interface is IrDA 1.1 compliant.

2.8.3.2 RS-232 Protocol:

When configured for RS-232 operation mode, the Serial Port 2 is 100% compatible with the IBM-AT serial port signals.

2.8.3.3 RS-422 Protocol:

The RS-422 protocol (Full Duplex) uses both RX and TX lines during a communication session.

> **CAUTION**
>
> In RS-422 mode, W9 and W10 jumper caps must be installed to connect the 120 ohms termination resistors (See Section 3.1 *Jumper Settings*)

2.8.3.4 RS-485 Protocol:

The RS-485 protocol (Full Duplex) also uses differential signals during a communication session. It differs from the RS-422 mode as it offers the ability to transmit and receive over the same pair of wires, and allows the sharing of the communication line by multiple stations. This configuration (also known as Party Line) allows only one system to take control of the communication line at the time.

In RS-485 mode, the RX lines are used as the transceiver lines, and the RTS signal is used to control the direction of the RS-485 buffer.

When set for RS-485 mode in the BIOS, upon power-up or reset, the transceiver is by default in receiver mode to prevent unwanted perturbation on the line. Party line operation mode requires termination resistors to be installed at both ends of the network.

CAUTION

When installing the cPCI-MXP64 at one end of the network, W9 and W10 jumper caps must be installed to connect the 120 ohms termination resistors (See Section 3.1 – *Setting Jumpers*).

2.9. THERMAL MANAGEMENT

Two temperature sensors are provided to supervise the thermal environment. One is used to monitor the CPU die temperature, while the second one, located on the CPU casing, allows the monitoring of the ambient temperature around the CPU.

The temperature is controlled according to two temperature levels, the Low temperature limit, which indicates normal operating conditions, and the High temperature limit, which indicates an overheating condition.

The temperature management consists in reducing the CPU clock speed (throttling) when the temperature goes over the high limit (overheating condition) and suspending the throttling operation as soon as the temperature returns under the low temperature limit (normal condition).

The clock speed may be throttled due to CPU overheating caused by the system cooling failure. In such a case, the temperature control is triggered as soon as the temperature reaches the high temperature limit of the die.

The ambient temperature of the CPU generally raises up due to an augmentation of the temperature in the casing. In that case, the clock speed will be slowed down as soon as the ambient temperature reaches the high ambient temperature value.

Thermal management operations are controlled by the BX chipset, and settings are provided through the BIOS setup program interface, *Thermal Management Setup* option (See Section 4.1.9 *CPU Board Feature Setup, Thermal management Options).*

Signal Path
None

Related Jumpers
None

BIOS Settings
Section 4.1.9 CPU/Board Feature Setup, Thermal Management Options

2.10. USB INTERFACES

Signals for two USB ports are available through the CPCI I/O connector J5.

USB is becoming the new essential peripheral interface. The USB strengths are as follows: capability to daisy chain as many as 127 devices per interface, fast bi-directional, isochronous/asynchronous interface, 12Mbps transfer rate, and standardization of peripheral interfaces into a single format.

Signal Paths
Both USB-0 and USB-1 interface signals are available through the CPCI I/O connector J5.

Related Jumpers
None

BIOS Settings
Section 4.1.8 PnP/PCI Configuration: Assign IRQ For USB.

USB supports Plug and Play and hot swapping operations (OS level). These user-friendly features allow USB devices to be automatically attached, configured and detached, without reboot or running setup.

The cPCI-MXP64 board fully supports the standard universal host controller interface (UHCI) and uses standard software drivers that are UHCI-compatible.

2.11. VIDEO INTERFACE

The high-performance video capability of the board is based on Accelerated Graphics Port (AGP) technology. The video controller, based on Intel's 69000, with its integrated 2Meg of high performance SDRAM is capable of CRT resolutions up to 1024 x 768 x 64K colors or 1280 x 1024 x 256 colors.

The video interface features 64-bit 2D graphics engine, 64-bit GUI accelerator engine with multiple window video acceleration.

Signal Path

The VGA video signal path depends of W1 setting (Rear or Front configuration).

Related Jumpers

W7 to enable or disable onboard VGA feature.
W1 to set Rear of Front configuration.
See section 3.1 – *Jumper Settings*

BIOS Settings

Section 4.1.8 PnP/PCI Configuration: Init Display First; Assign IRQ for VGA

2.11.1 Front I/O Configuration

VGA interface signals are available on J8, standard VGA connector, located on the faceplate of the board, only when the board is ordered for front I/O access operations. This configuration allows direct connection of CRT display onto the board.

2.11.2 Rear I/O Configuration

VGA interface signals are available on the CPCI I/O connectors when the board is ordered in rear I/O configuration.

2.11.3 Supported Resolutions

The maximum video resolution and performance depend directly on the drivers running with your software application. Resolution and number of color specification are listed below:

Resolution	Number of Colors
640x480, 800x600, 1024x768, 1280x1024	256 (8 bits)
640x480, 800x600, 1024x768	65,536 (16 bits)
640x480, 800x600	16.8 million (24 bits)
640x480, 800x600	16.8 million (32 bits)

2.11.4 Major Features Description

2.11.4.1 VGA Compatibility

The video controller includes all registers and data paths required for VGA controller, and supports extensions to VGA that includes resolutions up to 800x600x16.8 million colors non-interlaced. 16-bit images are displayed at up to 1024x768 resolution.

2.11.4.2 2D Graphics Engine

The 2D graphics engine is an advanced 64-bit three-operand engine that accelerates BitBLTs as line draws, polygon draw, and polygon fill. The 2D graphics engine also performs video and bitmap scaling, and data overlay.

PART 3

3. INSTALLING THE BOARD

1. SETTING JUMPERS
2. REGISTER'S DESCRIPTION
3. ONBOARD INTERCONNECTIVITY
4. CUSTOMIZING THE BOARD
5. PUTTING A KONTRON CPCI SYSTEM TOGETHER
6. CPCI I/O SIGNALS

3.1. SETTING JUMPERS

3.1.1 Jumper Description for the cPCI-MXP64

Description		Jumper
Board Configuration	Use this jumper to configure the cPCI-MXP64 for "Front Access" or "Rear Access".	**W1**
Remote Reset	To select Serial Port 1 or Serial Port 2 as a source for the remote hardware reset.	**W2**
Bridge	Set this jumper to enable or disable the bridge (stand alone or normal mode)	**W3**
Onboard Battery	Connects or Disconnects the battery to/from the board circuitry.	**W4**
VT-100 Mode	When enabled, allows VT100 or ANSI terminal connection	**W6**
Onboard Video	Use this jumper to enable or disable the onboard video feature.	**W7**
Serial Port 2 Termination	Use these jumpers to connect or disconnect termination resistors on/from Serial Port 2 when set for RS-422/RS-485.	**W9 W10**
CompactFlash Setting	Use this connector to setup the CompactFlash device in Master or Slave configuration.	**W11**

3.1.2 cPCI-MXP64 Connector and Jumper Location

CONNECTORS

J1-J3, J5		CompactPCI	J13	CompactFlash
J4, J11		Ethernet 1, 2	J15-J17	Memory Modules
J6	*	CPU Fan	J18	Mouse / Keyboard
J8		Video (SVGA)	J19	Storage Mezzanine
J10		Serial Ports	J20,J21	PMC
J12	*	PMC Mezzanine	J22	Hot Swap Switch
			S1	Reset Switch

* Optional

JUMPER SETTINGS (* : Default Setting)

W1- Board Configuration

Rear Access	in
Front Access	out

W2 - Remote Reset

Reset by Com1 note 1	1-2
Reset by Com2	3-4
* Disable	none

W3 - Bridge

Bridge disabled, stand alone	in
* Bridge enabled, normal mode	out

W4 - Battery

Connected	in
* Disconnected	out

W6 - VT- 100 or User Defined

Enable	in
* Disable	out

W7- Video Enable

Enable	in
* Disable	out

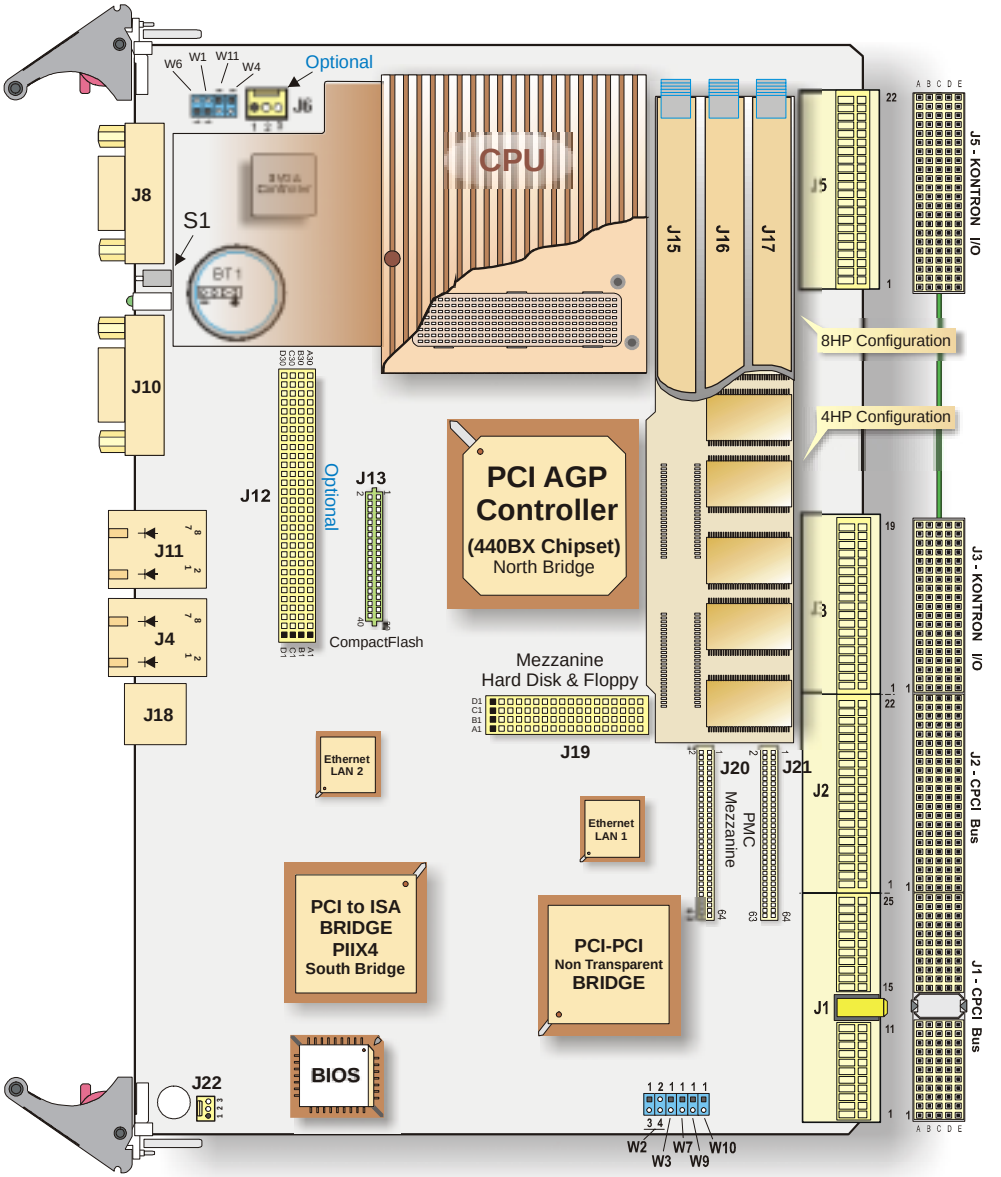
W9, W10 - COM2 Terminations

RS-422/485 modes only	W9	W10
With termination	in	in
* Without termination	out	out

W11 - Compact Flash Disk

Master	in
* Slave	out

NOTE 1 : When using Remote Reset, the jumper W2 must be at either position 1-2 or 2-3, never use both at same time.


W6
W1
W11
W4
Optional
J6
J8
S1
BT1
CPU
J15
J16
J17
J5
J10
8HP Configuration
4HP Configuration
J12
Optional
J13
PCI AGP Controller
(440BX Chipset)
North Bridge
J11
J4
CompactFlash
Mezzanine
Hard Disk & Floppy
J18
J19
J20
J21
J3
J2
J1
Ethernet LAN 2
Ethernet LAN 1
PMC Mezzanine
PCI to ISA BRIDGE PIIX4 South Bridge
PCI-PCI Non Transparent BRIDGE
BIOS
J22
W2
W3
W7
W9
W10
J5 - KONTRON I/O
J3 - KONTRON I/O
J2 - CPCI Bus
J1 - CPCI Bus

3.2. REGISTER'S DESCRIPTION

3.2.1 Serial Port 2 Configuration

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	n190h*	NU	NU	NU	RS485	RS232	ST1	NU	NU
WRITE	n190h*	NU	NU	NU	RS485	RS232	ST1	NU	NU
Power-up Default					0	1	0		

ST1 : Enable RTS2 to be used as 485TX ENABLE when in 485 mode
RS232 : Enable UART2 RS232 operation
RS485 : Enable UART2 RS422 and 485 operation

The serial port 2 mode can be controlled by setting three bits. Here are the possibilities.

Mode	Bit RS485	Bit RS232	Bit ST1
RS232	0	1	X*
RS422	1	0	0
RS485	1	0	1

X = Don't care

3.2.2 History and monitor status

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	n191h*	PBRST	NU	WDO	NU	NU	NU	NU	PFO
WRITE	n191h*	NU	NU	NU	NU	NU	NU	NU	NU
Power-up Default									

PFO : Read the external power fail flag
PBRST : When high, indicates that since the last power-up, a system reset was caused by push button reset switch
WDO : When high, indicate that since the last power-up, a system reset was caused by watchdog time out
Note : Since the history is stored in RAM memory, a loss of power will delete it.

3.2.3 History status

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	n192h*	NU	NU	NU	NU	HWD_LCK	WD_LOCK	NU	CLRHIS
WRITE	n192h*	NU	NU	NU	NU	HWD_LCK	WD_LOCK	NU	CLRHIS
Power-up Default						1	1		1

CLRHIS : When low, clear all history bits. Set this bit to 1 to enable history logging.
WD_LOCK : When high, lock the state of the enable bit for the digital watchdog

3.2.4 Monitoring status and I/O access

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	n193h*	NU	NU	NU	NU	IDCHIP	NU	I2C_CLK	I2C_DATA
WRITE	n193h*	NU	NU	NU	NU	IDCHIP	NU	I2C_CLK	I2C_DATA
Power-up Default						0		0	0

I2C_DATA : I2C data
I2C_CLK : I2C Clock
IDCHIP : One-wire clock/data for silicon ID chip

3.2.5 Digital watchdog

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	n196h*	WDEN	WDD2	WDD1	WDD0	HWDEN	HWDD2	HWDD1	HWDD0
WRITE	n196h*	WDEN	WDD2	WDD1	WDD0	HWDEN	HWDD2	HWDD1	HWDD0
Power-up Default		0	0	0	1				

WDEN : Enable/disable digital watchdog.
WDD[2..0] : Duration of digital watch dog.

The digital watchdog duration can be controlled in the following way.

WDD[2..0]	NMI(T)	RESET(T)
000	16T	NMI(T)+8T
001	64T	NMI(T)+8T
010	256T	NMI(T)+8T
011	1024T	NMI(T)+8T
100	4096T	NMI(T)+8T
101	16384T	NMI(T)+8T
110	65536T	NMI(T)+8T
111	262144T	NMI(T)+8T

Time-out selection with T = 1.08ms (TBC)

3.2.6 NMI Control

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	n197h*	BATFEN	BATFLT	NU	NU	NU	NU	WDNMIEN	WDNMI
WRITE	n197h*	BATFEN	NU	NU	NU	NU	NU	WDNMIEN	NU
Power-up Default		0						0	

WDNMI : When high, signal NMI from watchdog time-out.
WDNMIEN : Enable NMI generation from digital watchdog
BATFLT : When high, signal NMI from local RTC battery monitor
BATFEN : Enable NMI generation for bat fault.

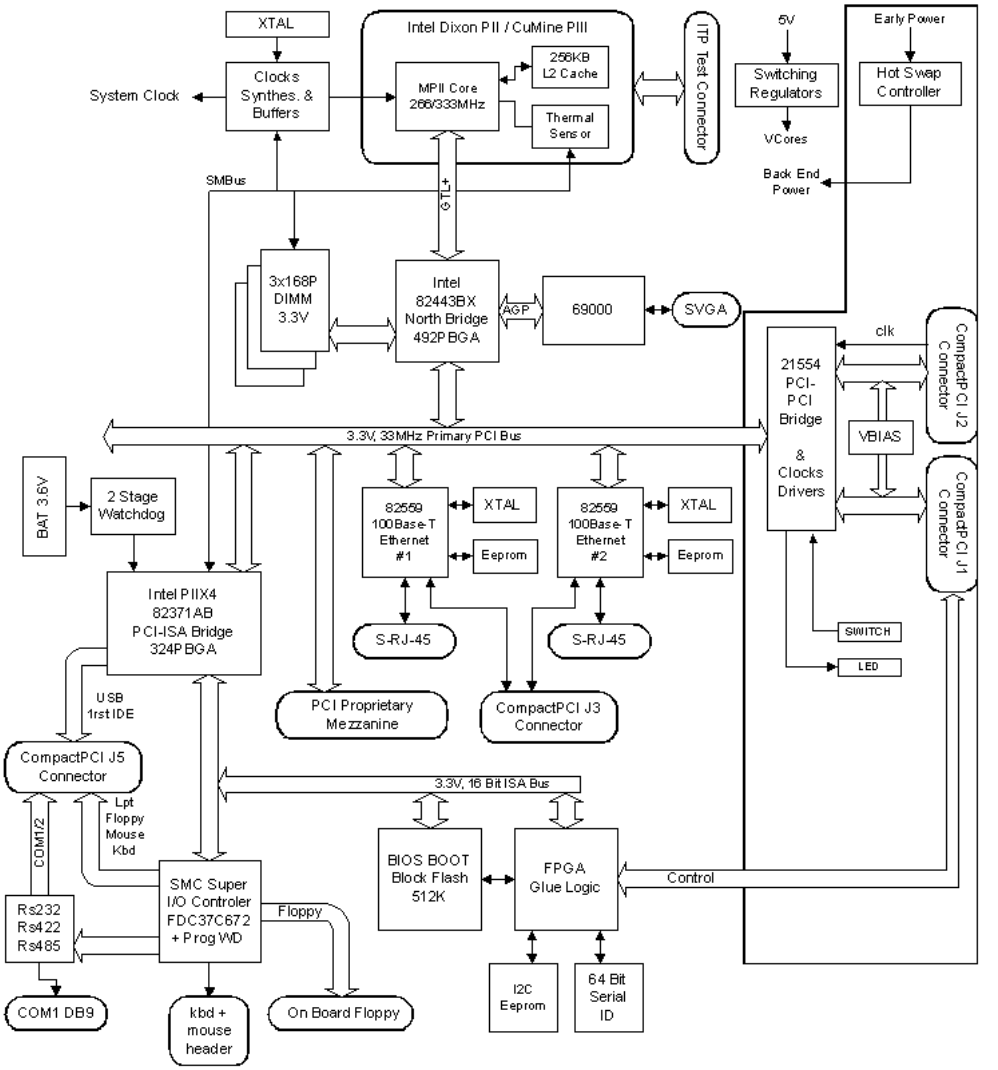
Register BITs description (summary)

FPGA	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	n190h*	NU	NU	NU	RS485	RS232	ST1	NU	NU
WRITE	n190h*	NU	NU	NU	RS485	RS232	ST1	NU	NU
READ	n191h*	PBRST	NU	WDO	NU	NU	NU	NU	PFO
WRITE	n191h*	NU	NU	NU	NU	NU	NU	NU	NU
READ	n192h*	NU	NU	NU	NU	NU	WD_LOCK	NU	_CLRHIS
WRITE	n192h*	NU	NU	NU	NU	NU	WD_LOCK	NU	_CLRHIS
READ	n193h*	NU	NU	NU	NU	IDCHIP	NU	I2C_CLK	I2C_DATA
WRITE	n193h*	NU	NU	NU	NU	IDCHIP	NU	I2C_CLK	I2C_DATA
READ	n196h*	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
WRITE	n196h*	WDEN	WDD2	WDD1	WDD0	NU	NU	NU	NU
READ	n197h*	BATFEN	BATFLT	NU	NU	NU	NU	WDNMIEN	WDNMI
WRITE	n197h*	BATFEN	NU	NU	NU	NU	NU	WDNMIEN	NU

* The base address for the Supervisor I/O Register, which is used for such functions as power fail detection and the watchdog timer can be set to 190h, 290h, and 390h (see *Chipset Features Setup*).

3.3. ONBOARD INTERCONNECTIVITY

3.3.1 cPCI-MXP64 Block Diagram



The cPCI-MXP64 is a powerful computing engine. In addition to the CPU core, it is supplemented by an extensive set of interfaces using three key components:

- Host-to-PCI bridge for PCI bus. 443BX from Intel: interface with the processor (host), system memory, video controller, and Primary PCI bus.
- PCI-to-PCI bridge - 21554 from Intel: manage the PCI bus signals on J1 and J2 CPCI connectors. When used with a CompactPCI backplane.
- PCI-to-ISA bridge - 82371AB PIIX4E from Intel: interface the ISA bus to the Primary PCI bus.

3.3.2 Mobile Pentium® III processor

The cPCI-MXP64 peripheral processor supports the Intel's Low power 400MHz Pentium® III as well as the low power 500MHz Pentium® III processor (higher clock speeds will be available when Intel releases the corresponding parts).

It consists of a Pentium® III processor core with an integrated second level cache of 256KB (on-die, full CPU speed, ECC capable) and a 64-bit high performance 100MHz front side bus.

The processor interfaces to the 440BX AGPset through the 64-bit low power GTL + data bus interface.

3.3.3 North Bridge Chipset

This chipset consist of 443BX AGPset, 64/72-bit SDRAM data interface with ECC support, Low Power GTL Bus, five PCI arbitration channels, PCI bus rev. 2.1, Accelerated Graphics Port Interface (AGP). The bus is optimized for 100MHz operation.

3.3.4 21554 PCI-to-PCI Bridge

The 21554 is a PCI peripheral chip that performs PCI bridging functions for embedded and intelligent I/O applications. The 21554 is a “non-transparent” PCI-to-PCI bridge that acts as a gateway to an intelligent subsystem. It allows a local processor to independently configure and control the local subsystem. The 21554 implements an I_2O message unit that enables any local processor to function as an intelligent I/O processor (IOP) in an I_2O-capable system.

Unlike a transparent PCI-to-PCI bridge, the 21554 is specifically designed to bridge between two processor domains. The processor domain on the primary interface of the 21554 is also referred to as the host processor. The secondary bus interfaces to the local domain and the local processor. Special features include support of independent primary and secondary PCI clocks, independent primary and secondary address spaces, and address translation between primary (host) and secondary (local) domains.

The 21554 (on cPCI-MXP64) supports a 32-bit primary PCI bus, a 64-bit secondary CPCI bus, and a maximum operation frequency of 33MHz.

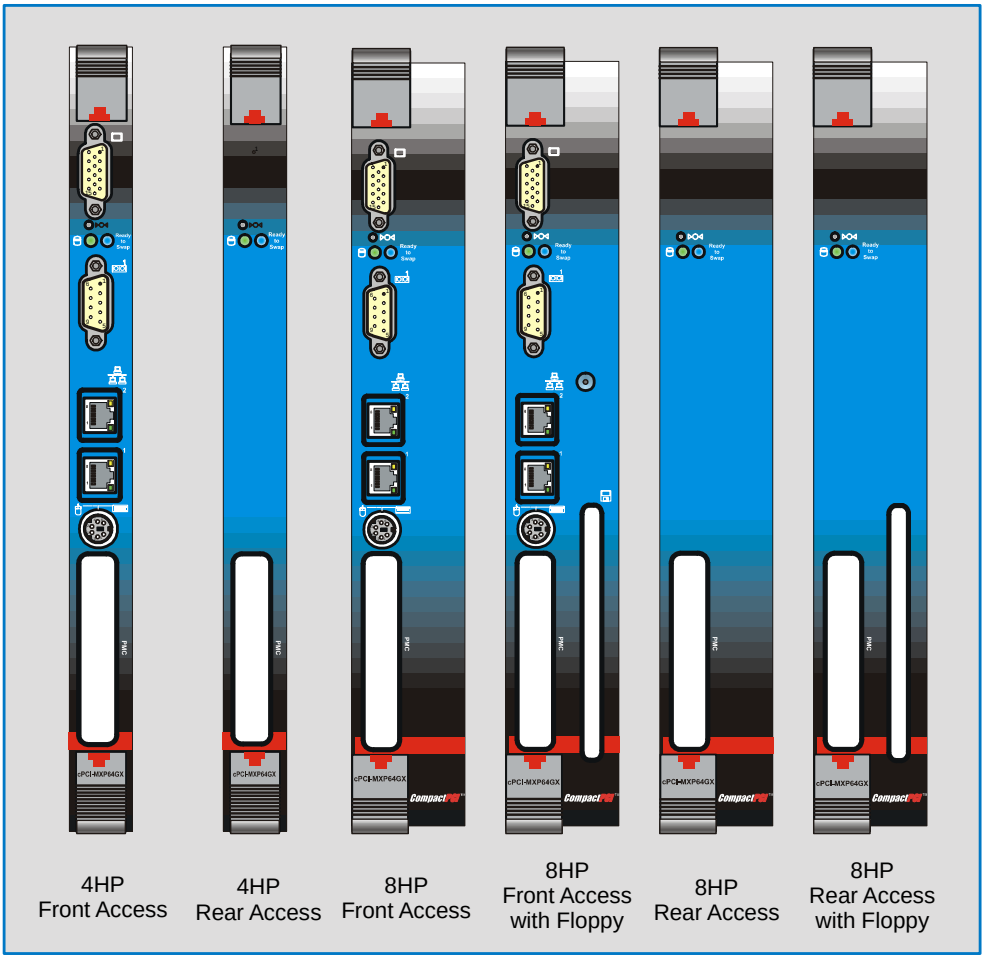
3.3.5 82371AB PCI-to-ISA Bridge / IDE Xcelerator (PIIX4)

The PCI-to-ISA bridge is configured to support signals to directly drive IDE interfaces, USB ports, and standard Serial Ports (1 and 2), floppy disk drives, mouse and keyboard through a super I/O controller (FDC37C672).

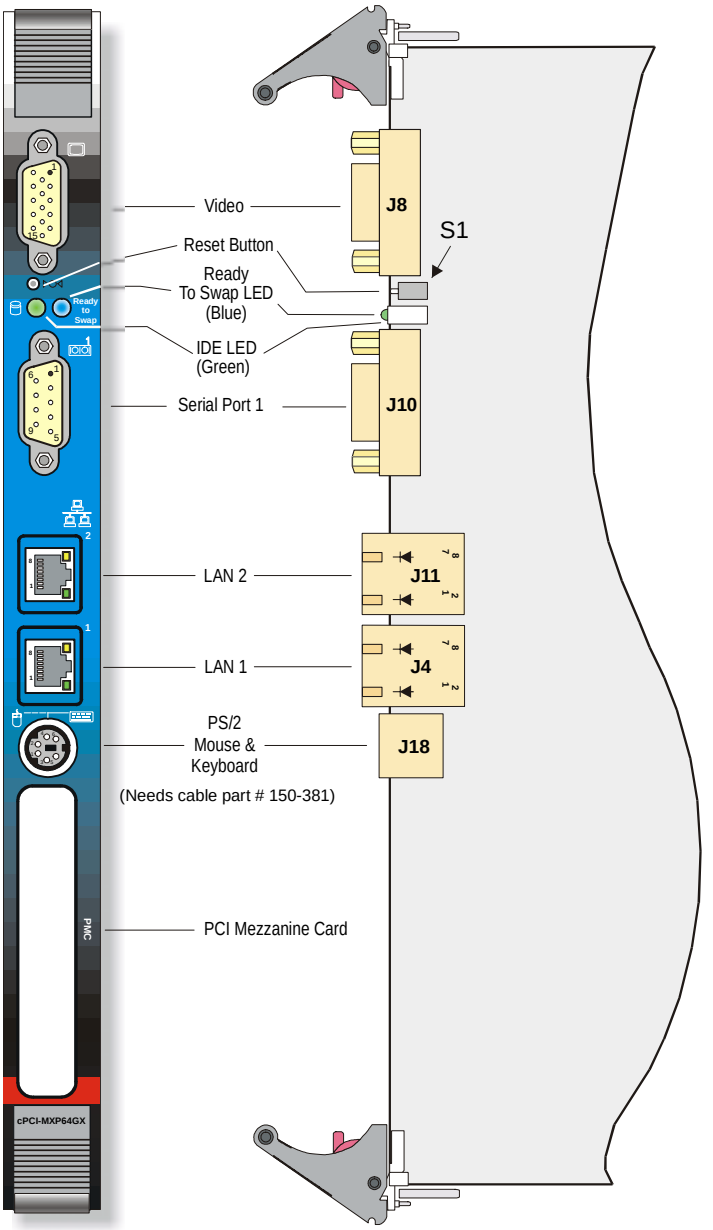
3.3.6 Onboard Connectors and Headers

Description	Comments	
CompactPCI Bus	J1/J2	J1- CPCI bus signals and power. J2 – Additional system slot signals (PCI 64 bits extension)
CompactPCI I/O	J3	Serial Port 2 (infrared), Ethernet, power.
CompactPCI I/O	J5	Supports PS/2 mouse, serial ports 1 and 2, first IDE channel, parallel port, keyboard, speaker, floppy disk, reset, USB, SMBus, and power signals.
Fan Header	J6	The +12V DC CPU fan power supply is provided through this header as well as a speed sense input for the fan
VGA	J8	Supports standard 15-pin DSUB female connector.
Processor Socket	J9	Pentium II / III connector
Serial Port 1	J10	Supports standard 9-pin DSUB male connector.
Ethernet 1 and 2	J4, J11	RJ-45 connectors with built-in activity and link indicators.
PCI Mezzanine	J12	This connector handles PCI bus signals to the mezzanine.
CompactFlash	J13	This connector is dedicated to the Kontron's CompactFlash module to support CompactFlash disk.
DIMM Sockets	J15-J17	Supports 168-pin 64/72-bit DIMMs, up to 768MB of RAM.
Keyboard/Mouse	J18	Mouse and keyboard signals are combined on a standard 6-pin DSUB female connector.
Storage Mezzanine	J19	This connector is implemented to support floppy drive and hard disk signals.
PMC	J20-J21	The PCI Mezzanine Card (PMC) connectors support one standard PMC device.
Hot Swap Switch	J22	This switch detects the removal of the cPCI-MXP64.
Battery	B1	CMOS backup battery connector.

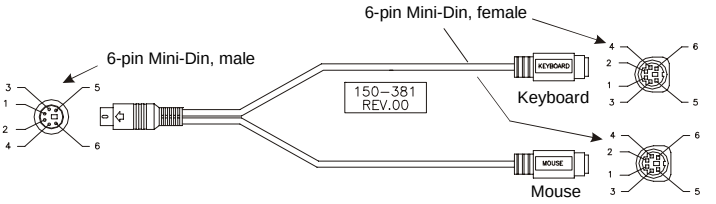
3.3.7 Front Plate Connectors and Indicators



Front Plate Connectors and Indicators (cont'd)

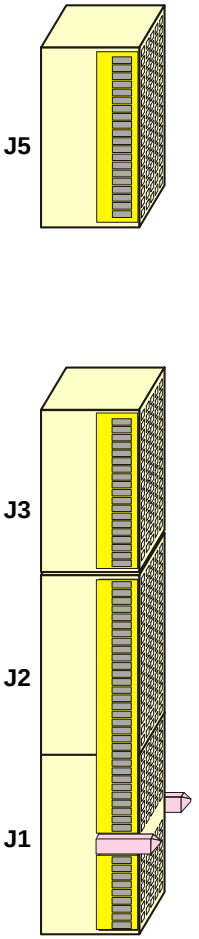


Connector	Description	Comments
J4	Ethernet 1	RJ-45 connectors with built-in activity and link indicators
J8	VGA Video	Standard 15-pin DSUB female connector
J10	Serial Port 1	Standard 9-pin DSUB male connector
J11	Ethernet 2	RJ-45 connectors with built-in activity and link indicators
J18	Keyboard and Mouse	To connect a keyboard and/or a mouse through this connector, you need a Y shaped splitter cable (Kontron part number 150-381)
DS1	IDE Activity LED	When lit, indicates an activity on IDE/SCSI devices
DS2	Ready to Swap LED	When lit, indicates that the board is ready for removal
S1	Reset Button	Use a small tool to press the button and proceed to a hardware reset of the board



The faceplate supports a PMC cutout with filler cap installed that acts as an EMI shield when there are no PMC device installed.

3.3.8 CompactPCI Connectors



- **CPCI J5 Connector**

  Supports PS/2 mouse, serial ports 1 and 2, primary IDE channel, parallel port, keyboard, speaker, floppy disk, reset, USB, SMBus and power signals.

- **CPCI J4 Connector (not installed)**

  Reserved for H110 telephony bus.

- **CPCI J3 Connector**

  Supports serial ports 2 (Infrared), 2 Ethernets and power signals.

- **CPCI J2 Connector**

  Supports additional system slot signals, PCI 64-Bit extension, and power.

- **CPCI J1 Connector**

  Supports CPCI bus signals, and power.

3.4. CUSTOMIZING THE BOARD

3.4.1 Processor

The cPCI-MXP64 is shipped with the Mobile PentiumIII processor, Low Power 400/500MHz is equipped with a passive heat sink that provides adequate cooling in a 150LFM airflow environment.

CAUTION

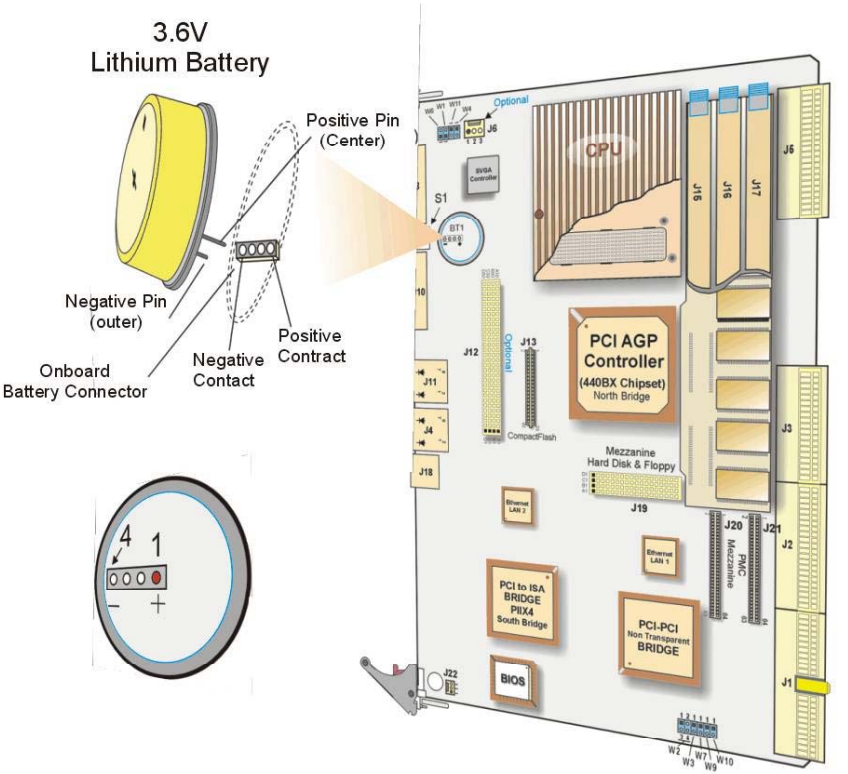
Since CPUs are very sensitive components, particular attention should be given while installing a processor on the board. Improper installation may damage the board and/or the CPU

Before installing a processor on your board, **you must contact our technical support** for the installation procedure

3.4.2 Backup Battery

An onboard 3.6V lithium battery is provided to backup BIOS setup values and the real time clock (RTC).

When replacing, the battery must be connected as follows:



WARNING

Danger of explosion if battery is incorrectly replaced

Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

3.4.3 Installing the Memory

3.4.3.1 SDRAM System Memory

The cPCI-MXP64 supports three industry standard 168-pin DIMMs (Dual In-Line Memory Module) sockets for memory configuration from 256MB to 768MB of Synchronous DRAM in 4HP configuration and from 64MB to 768MB in 8HP configuration. In single slot configuration, Kontron's memory modules supports up to 768MB.

The memory characteristics must conform to the following:

- 1.15 inch height, 168-pin DIMM
- Standard 3.3V only,
- 64-bit and 72-bit modules, single-sided or double-sided
- Unbuffered 100MHz (SDRAM),
- Serial Presence Detect (SPD) EEPROM,
- Errors Checking and Correction (ECC) capabilities or parity bit with 72-bit modules,
- Compliant with Intel's PC SDRAM Unbuffered DIMM Specification (100MHz) Rev. 1.0.

Modules can be installed in any socket and order. The total system memory is equal to the sum of the memory module size installed in the three DIMM sockets.

NOTE

When populating with more than one memory module, each socket must be populated with identical memory module.

For the latest list of tested DIMMs devices please consult our FTP site at :

ftp://ftp.kontron.ca/Support/Product_Memory_AVL_Approved%20Vendor%20List/

3.4.3.2 DIMM Installation

> **NOTE**
>
> If a Mezzanine card is installed, it must be removed before installation of DIMMs.

To install the DIMMs in the sockets, proceed as follows:

1. With the board flat on the table, turn it so that the faceplate is facing you.
2. Hold the module vertically so that the bottom connector key is at right. Install the DIMM straight down into the DIMM socket. The socket's keys will ensure a correct mating.
3. Press firmly on the top edge of the memory module to engage it into the socket. The module is fully inserted when the retaining clips snap into notches located at each end of the module.

If necessary, work your way by inserting the other modules, one by one.

To remove the DIMMs from the sockets, pull simultaneously on the retaining clips located on each side of the socket. Once the module has snapped out, pull gently on it.

3.4.4 Supervision Features

The cPCI-MXP64 provide a set of programmable I/O registers to setup the Intel PIIX4E (I/O addresses 4030h to 4037h) and the XILINX FPGA (I/O addresses programmable at 190h-19Fh, 290h-29Fh or 390h-39Fh using the AWARD Chipset Features Setup).

Only register bits needed to program the power fail detection and watchdog functions are described below.

3.4.4.1 Power Fail Monitoring

The power failure detector status can be readout from one bit of the system register located at the address n191h* Bit 0. The detection conforms to the following conditions (* = active low signal):

It always monitors the +5V power supply. When it drops below 4.65V (typical), the system is reset.
It can monitor the onboard battery. When the battery is in a low condition (below 2.9V typical), the PFO* (power fail output) signal goes low. The status of the PFO* signal can be read at I/O address 4031h, bit 1 (0 = failed, 1 = good). An interrupt handler can then service the interrupt. If you choose not to generate an NMI, you can use an algorithm to detect a low battery condition and respond accordingly.

3.4.4.2 Watchdog

The function of a watchdog is to reset the CPU board if the processor is not able to generate a trigger for longer than the watchdog time-out period. This feature is useful in embedded systems where human supervision is not required or impossible.

The cPCI-MXP64 provides a two-stage digital watchdog with software programmable time-out period.

Following a reset of any source, the watchdog is disabled. The watchdog can be enabled by software.

3.4.4.3 Dual Stage Watchdog

Enabling the Programmable Watchdog

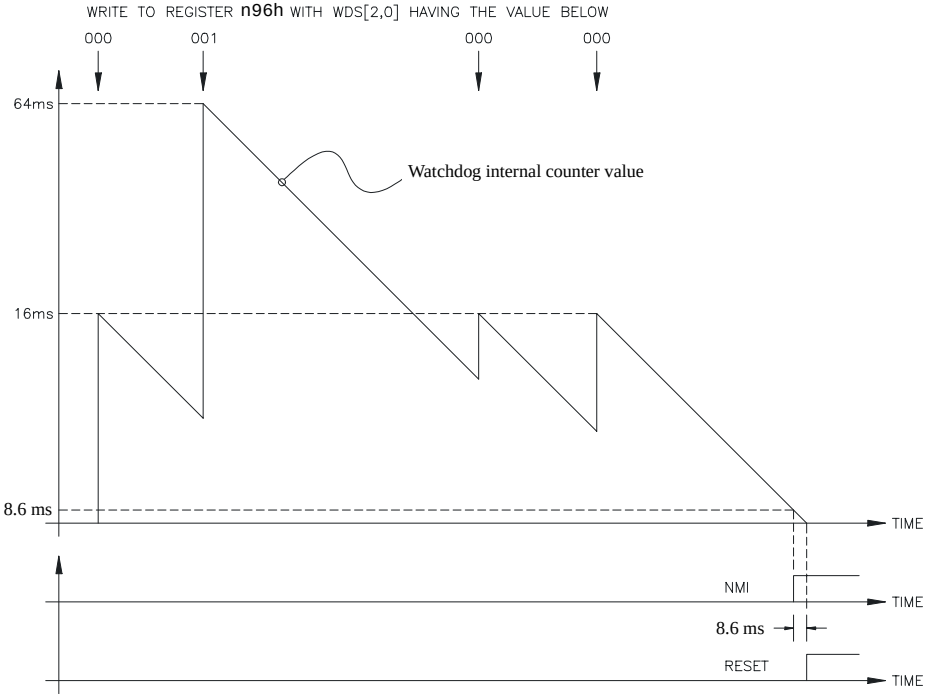
To enable the programmable watchdog, first unlock the enable bit by clearing the lock bit in register n92h (bit 2), then set the bit WDEN (bit 7) in register n96h and relock it by setting the lock bit in register n92 (bit 2). The following is an example in C language:

```
#define TekReg 0x190                    // define base address (0x190, 0x290 or 0x390)
void ArmWatchdog(void)
{
    outp(TekReg+2,  inp(TekReg+2) & 0xFB);      // unlock watchdog enable bit
    outp(TekReg+6,  inp(TekReg+6) | 0xF0);      // enable and trigger at max time-out
    outp(TekReg+2,  inp(TekReg+2) | 0x04);      // lock watchdog enable bit
}
```

3.4.4.4 Triggering the Programmable Watchdog

To trigger the programmable watchdog, the processor writes to register n96h (n=1, 2 or 3). The action of writing to the register is the trigger and the value written to the register tells the watchdog the current time-out to use (see register n96h description). For a fixed time-out, the software simply writes a constant in register n96h.

A variable refresh is possible as shown below:



The programmable watchdog can be viewed as a decrementing counter that is initialized by a write to register n96h (n = 1, 2 or 3). The processor must initialize the counter to prevent it from reaching count 0 (timeout).

The following C language procedure can be used to trigger the programmable watchdog.

```
#define TekReg 0x190                    // define base address (0x190, 0x290 or 0x390)
void TrigWatchdog(timeout)     // select timeout at runtime: 0x80 = 0.016s,
                               // 0x90 = 0.065s, 0xA0 = 0.261s, ...
{
   outp(TekReg+6,(inp(TekReg+6) & 0x0F) | (timeout & 0xF0));
}
```

Time-out

The programmable watchdog has two stages: the first stage has a variable time-out while the second stage has a fixed one.

The first stage time-out is chosen at runtime from eight preset values (see table below). The first stage time-out generates an NMI interrupt (if enabled in register n96h, bit 7). An appropriate NMI handler must be written, otherwise this will be treated as a parity error by the default BIOS NMI handler; see register n96h description for a suggestion on how to do this.
The second stage times-out 8.6ms ±10% (depending on the temperature) after the first one and generates a master reset.

WDD[2..0]	NMI(T)	RESET(T)
000	16T	NMI(T)+8T
001	64T	NMI(T)+8T
010	256T	NMI(T)+8T
011	1024T	NMI(T)+8T
100	4096T	NMI(T)+8T
101	16384T	NMI(T)+8T
110	65536T	NMI(T)+8T
111	262144T	NMI(T)+8T

Time-out selection with T = 1.08ms (TBC)

A reset from the programmable watchdog is latched for reset source identification; see reset history description in Section 3.2.2.

3.4.4.5 Thermal Management

The thermal management is built around two digital temperature sensors and a thermal watchdog. Both devices can be programmed to set their outputs when the temperature of the processor or the ambient temperature exceeds a programmable high limit, and reset its output when the temperature is under a programmable low limit. A special routine is implemented to throttle the CPU clock until the temperature falls below the programmed low limit.

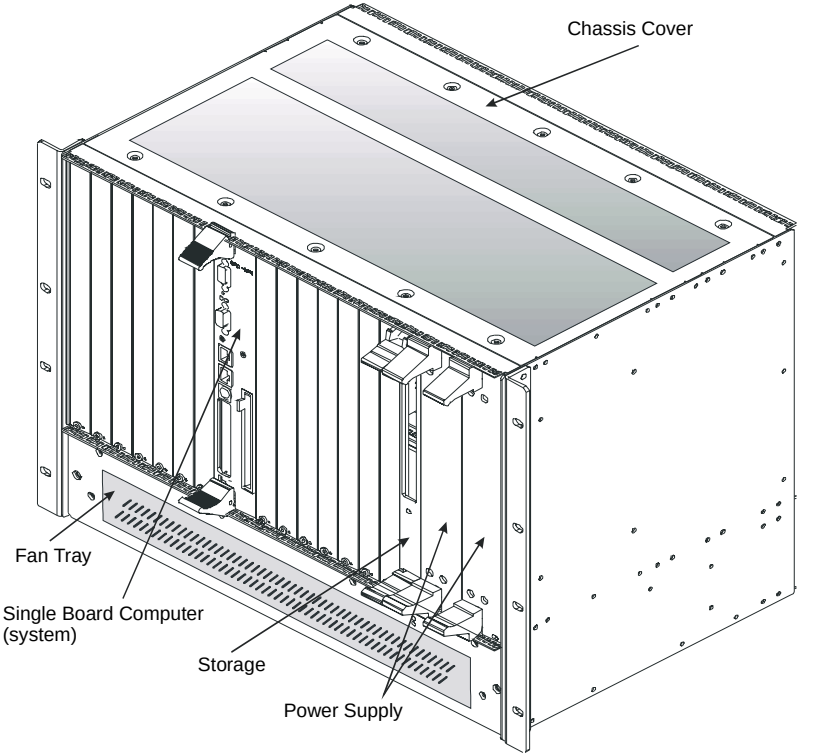
Please refer to Section 4.1.9 *CPU/Board Features Setup– Thermal Management Options* for a complete information on thermal management setups.

3.5. PUTTING A KONTRON CPCI SYSTEM TOGETHER

A typical Kontron CompactPCI system is made up of: a chassis/enclosure, a backplane, an optional storage module, a power supply unit, and a ventilation system.

AC/DC power inputs are conditioned using an off-the-shelf 2-stage filter. Protection is implemented using a replaceable fuse located in a fuse holder. A power switch allows for complete system power –up/down sequencing.

Kontron's development chassis, the CxP0816, may be used either in tabletop or rack-mount configuration.



CxP0816

3.5.1 Backplane

The entry-level backplane of the Kontron's CxP0816, referred to as the cBP-08R, is an 8 slot CPCI backplane (one PCI I/O segment), and includes P1-P5 connectors on all slots.

A 16-CPCI-slot backplane (cBP-16R) is also available from Kontron. It supports two PCI I/O segment: one is driven directly by the system processor while the other is managed through a PCI-to-PCI bridge implemented on the cMCB-2RC mezzanine card that is installed on the center-mounted system processor.

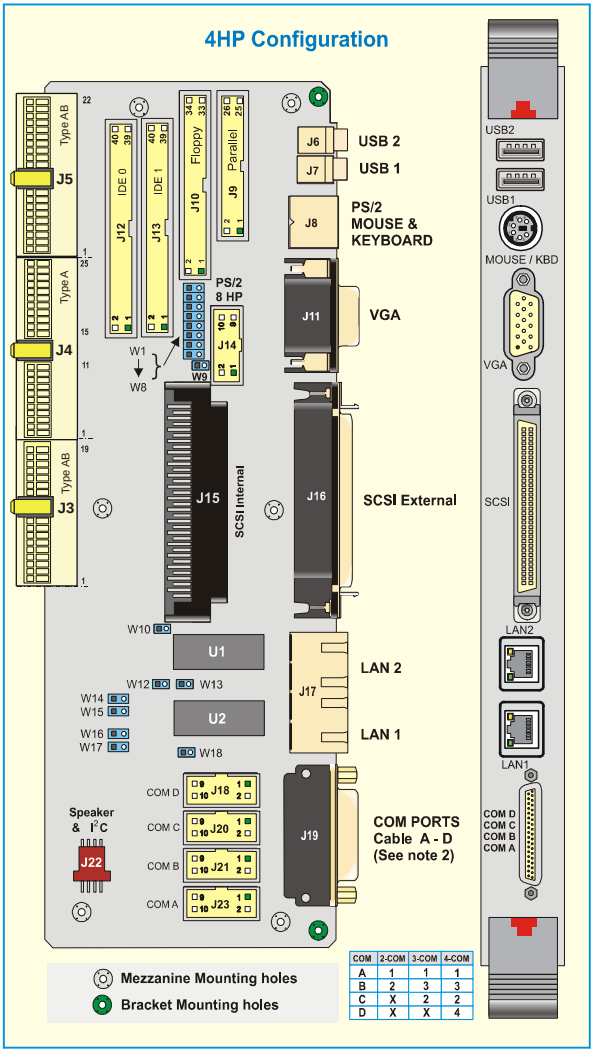
All Kontron's CompactPCI backplanes feature pass-through connectors on P3-P5 to support full Rear Panel I/O connections.

IMPORTANT

J1 and J2 connected as per PICMG 2.0 Rev 3.0 specifications.

J3 and J5 are user-defined connectors and will vary from various manufacturers. Contact our Technical Support to verify pinout compatibility with other chassis backplane vendors.

3.5.2 Rear-Transition Module

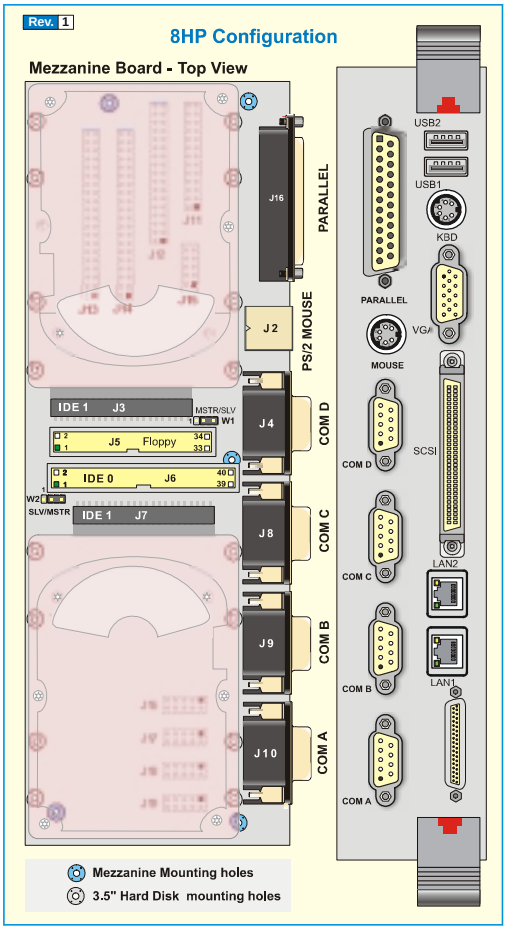


This feature is intended to extend the I/O capabilities of the system or peripheral processor to the rear of the enclosure using a Rear Transition Module.

The Transition Module gathers all the I/O signals of the CPU board and makes them easily accessible through standard headers and connectors located at the rear of enclosure.

The illustration at right shows a single slot Rear Transition Module CTM80-STD1S.

The dual slot module cTM80-STD2S is illustrated on next page.



3.5.3 Storage Devices

.

There are two ways of supplying data storage with Kontron's product line.

1. cMC : Mezzanine Card that is installed directly onto the processor board (see section 1.6 – Mezzanine Card Concept).
2. cSM-CD : 6U form factor storage module that is front loaded into the CxP0816 chassis.

3.5.4 Power Supply

Five power supply options are supported by the CxP0816. This includes 6U, dual slot front loaded 350W power supplies, in single or dual, load sharing (N+1) configurations in both AC and DC models, all hot swap capable. A standard ATX power supply unit is also supported.

3.5.5 Fan Tray

The ventilation unit of the enclosure conforms to the global requirement of the system in fully loaded configuration providing over 300CFM of airflow. The fan Tray is fully hot swap capable.

3.5.6 Installing the Board into a Bay

Due to the high-density pinout of the cPCI-MXP64's Hard Metric connectors, some precautions must be taken when inserting or removing a board in/out of a system:

1. Properly insert the board in the rail guides and slide the board until the board connectors mate to the backplane.
2. Do not use excessive force if there is any mechanical resistance while inserting the board or serious damage can be incurred to the backplane.
3. Using the extractor handle, push the board to final insertion.
4. Using the face plate bolts, firmly secure the board to the enclosure.
5. Use the extractor handles to disconnect and extract the board from its enclosure.

3.5.7 Connector Keying

CompactPCI connector supports guide lugs to ensure a correct polarized mating. A proper mating is enhanced by the use of color-coded keys for 3.3V and 5V operation.

Color-coded keys prevent inadvertent installation of a 5V peripheral board in a 3.3V slot. The cPCI-MXP64 is universal. It does not require keying. . Backplane connectors are always keyed according to the signaling (VIO) level. Coding Key Colors are defined as follows:

Signaling Voltage	Key Color
3.3V	Cadmium Yellow
5V	Brilliant Blue
Universal board (5V and 3.3V)	none
-48V	Red

3.5.8 Connection

To install the cPCI-MXP64 boards into a bay, proceed as follows:

1. Locate a 6U peripheral slot
2. Remove the blank faceplate of the slot where you intend to insert the cPCI-MXP64.
3. Proceed as per description in 3.5.6.

WARNING

1. Some mechanical parts of the guide-rail are fragile (shield contacts and clips). Do not use excessive force to insert and connect a CompactPCI board.
2. If there is any mechanical resistance while you insert a module, first ensure there is no mechanical obstacle and check for the alignment of all parts. A key might be installed preventing the installation of a CPCI board in an incompatible slot.

To remove the module from the chassis, proceed as follows:

1. Unsecure the front plate fixing bolts.
2. Unlock the bottom extractor handle. This will activate a switch a make the board aware of your intentions to remove the board.
3. Wait for the blue LED to turn ON.
4. Use the extractor handles to act as a lever to disengage the CompactPCI connector from the backplane.
5. Pull on the extractor handles and gently remove the board.

3.6. CPCI I/O SIGNALS

This section describes integrated feature signals available on the CPCI I/O connectors J3, and J5.

3.6.1 J3 Signal Specification

3.6.1.1 Ethernet LEDS

Signal	Pin Assignation	Description
LAN0, 1:SPLED	A6, E6	Speed LED signal
LAN0, 1:LINKLED	B6, D6	Link integrity LED signal
LAN0, 1:ACTLED	C6, A7	Transmit / receive activity LED signal

3.6.1.2 Ethernet 1

Signal	Pin Assignation	Description
LAN0:ETX+	A5	Ethernet High Transmit Data line
LAN0:ETX-	A3	Ethernet Low Transmit Data line
LAN0:ERX+	C5	Ethernet High Receive Data line
LAN0:ERX-	C4	Ethernet Low Receive Data line

3.6.1.3 Ethernet 2

Signal	Pin Assignation	Description
LAN1:ETX+	A9	Ethernet High Transmit Data line
LAN1:ETX-	B9	Ethernet Low Transmit Data line
LAN1:ERX+	C9	Ethernet High Receive Data line
LAN1:ERX-	D9	Ethernet Low Receive Data line

3.6.1.4 IDE LED Signals.

Signal	Pin Assignation	Description
IDE:ACT	C18	Primary IDE activity

3.6.1.5 IR COM2

Signal	Pin Assignation	Description
COM2:IRRX	D18	IR receive data line (Serial Port 2)
COM2:IRTX	E18	IR transmit data line (Serial Port 2)

3.6.1.6 Miscellaneous Signals

Signal	Pin Assignation	Description
EXT-SMI	B19	System Management Interrupt Input
PX4-NMI	C19	Non Maskable Interrupt Input
PWROK-33	E19	High when 3.3V supply is valid on the board

3.6.2 J5 Signal Specification

3.6.2.1 IDE 0 Interface

Signal	Pin Assignation	Description
IDE0:RST#	A1, B1	
IDE0:D 0-15	B4, E3, C3, A3, D2, B2, E1, C1, D1, A2, C2, E2, B3, D3, A4, D4	Prim. Disk Data – These signals are used to transfer data to or from the IDE device.
IDE0:REQ	A5	Prim. Disk DMA Request - This signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer.
IDE0:IOW#	C5	Prim. Disk I/O Write – In normal IDE mode, this is the command to the IDE device that it may latch data from SDD lines.
IDE0:IOR#	E5	Prim. Disk I/O Read – In normal IDE mode, this is the command to the IDE device that it may drive data on SDD lines.
IDE0:IORDY	B5	Prim. I/O Channel Ready – In normal mode, this input signal is driven directly by the corresponding IDE device IORDY signal.
IDE0:DACK#	D5	Prim. DMA Acknowledge – This signal directly drives the IDE device /DMACK signal. It is asserted to indicate to IDE DMA slave devices that a given data transfer cycle is a DMA data transfer cycle.
IRQ14	E4	IRQ14 line
IDE0:IO16#	A6	IOCS16 line
IDE0:A 0-2	D6, C7, E6	Prim. Disk Address – These signals indicates which byte in either the ATA command block or control block is being addressed.
IDE0:CS1#, IDE0:CS3#	A7, B7	
PRI-PD1	D7	
IDE0:DIAG#	C6	

3.6.2.2 USB 0 and 1 Interfaces

Signal	Pin Assignation	Description
USB1, 0: DATA (+/-)	B18, C18, D19, E19	USB Data – Differential data path for USB 0 and 1 ports
USB1, 0: GND	B19, D18	USB Ground – Differential ground reference for USB 0 and 1 ports
USB1, 0:VCC	C19, E18	USB Voltage – Differential power level for USB 0 and 1 ports

3.6.2.3 Floppy Disk Interface

Signal	Pin Assignation	Description
FD:DRVEN 0-1#	E7, A8	Drive 0-1 density select
FD:INDEX#	B8	Index
FD:MTR 0-1#	C8, A9	Motor 0-1 enable
FD:DS 0-1#	E8, D8	Drive 0-1 select
FD:DIR#	B9	Direction
FD:STEP#	C9	Step pulse
FD:WDATA#	D9	Write disk data
FD:WGATE#	E9	Write gate
FD:TRK0#	A10	Track 0
FD:WRPROT#	B10	Write protected
FD:RDATA#	C10	Read disk data
FD:HDSEL#	D10	Head select
FD:DSKCHG#	E10	Disk change

3.6.2.4 Serial Port 1

Signal	Pin Assignation	Description
COM1:DCD	A13	Data Carrier Detect
COM1:RXD	C13	Receive Data
COM1:DSR	D13	Data Set Ready
COM1:TXD	E13	Transmit Data
COM1:RTS	A14	Ready To Send
COM1:CTS	B14	Clear To Send
COM1:RI	C14	Ring Indicator
COM1:DTR	E14	Data Terminal Ready

3.6.2.5 Serial Port 2

Signal	Pin Assignation	Description
COM2:DCD	A11	Data Carrier Detect
COM2:RXD	C11	Receive Data
COM2:DSR	D11	Data Set Ready
COM2:TXD	E11	Transmit Data
COM2:RTS	A12	Ready To Send
COM2:CTS	B12	Clear To Send
COM2:RI	C12	Ring Indicator
COM2:DTR	E12	Data Terminal Ready

3.6.2.6 Parallel Port

Signal	Pin Assignation	Description
SLCT	A15	Printer select
PE	B15	Paper end
BUSY	C15	Busy signal
ACK#	D15	Acknowledge handshake
D 0-7	E17, C17, A17, D16, C16, B16, A16, E15	Parallel port data bus
SLCTIN#	E16	Printer select
ALF	A18	Auto line feed
INIT#	B17	Initiate output
ERR#	D17	Error at printer
STB#	A19	Strobe signal

3.6.2.7 Keyboard Interface

Signal	Pin Assignation	Description
KB:DATA	A21	Keyboard data
KB:CLK	B21	Keyboard clock
KB:VCC	C21	Keyboard power

3.6.2.8 Mouse Interface

Signal	Pin Assignation	Description
MOUSE:DATA	D21	Mouse data
MOUSE:CLK	E21	Mouse clock

3.6.2.9 CRT

Signal	Pin Assignation	Description
HSYNC	D14	Horizontal Sync.
VSYNC	B6	Vertical Sync.
RED	D20	Red signal
GREEN	B22	Green signal
BLUE	B11	Blue signal

3.6.2.10 Miscellaneous Signals

Signal	Pin Assignation	Description
SMBDATA#	B20	Onboard SMbus data
SMBALERT#	C20	Onboard SMbus Alert (CPU overheating)
SMBCLK	E20	Onboard SMbus Clock
PBRST#	A22	Reset
DIAG-OC#	C22	Reserved
SPEAKER	E22	Speaker signal

PART 4

4. SOFTWARE SETUPS

1. BIOS SETUP PROGRAM
2. BOOT UTILITIES
3. UPDATING OR RESTORING THE BIOS IN FLASH
4. VT100 MODE

4.1. BIOS SETUP PROGRAM

All relevant information for operating the board and connected peripherals is stored in the CMOS memory. A battery-backed up memory holds this information when the board is powered off, the BIOS Setup program is required to make changes to the setup.

NOTES

Make sure you setup the BIOS Setup software prior to installing your operating system and your drivers.

For systems that need the BIOS to first attempt to boot from LAN, follow these steps:

1. Set the *Boot from LAN first* option to “Enabled” in the BIOS Setup’s *BIOS Features Setup*
2. Follow the complete procedure in the Boot from LAN utility CDROM.

4.1.1 Accessing the BIOS setup program

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the cPCI-MXP64 peripheral processor. The CPCI-MXP64 uses the AWARD Setup program, a setup utility in flash memory that is accessed by pressing the DELETE key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

> CAUTION
> Before modifying CMOS setup parameters, ensure that the W4 battery selection jumper is installed to enable the CMOS battery back up (please refer to Section .3.1).

To run the AWARD Setup program incorporated in the ROM BIOS:

- Turn on or reboot the system.
- Hit the DELETE key when the message - "Press DEL to Enter SETUP" appears near the bottom of the screen.

The main menu of the AWARD BIOS CMOS Setup Utility appears on the screen.

```
                KONTRON APPPLICOM cPCI-MXP64 BIOS VERSION 2.0
                        CMOS SETUP UTILITY
                    AWARD SOFTWARE, INC. (2A69TU00)

STANDARD CMOS SETUP                 LOAD BIOS DEFAULTS (SAFE)
BIOS FEATURES SETUP                 LOAD SETUP DEFAULTS (OPTIMAL)
CHIPSET FEATURES SETUP              SUPERVISOR PASSWORD
POWER MANAGEMENT SETUP              USER PASSWORD
PNP/PCI CONFIGURATION               IDE HDD AUTO DETECTION
CPU/BOARD FEATURES SETUP            SAVE & EXIT SETUP
INTEGRATED PERIPHERALS              EXIT WITHOUT SAVING

Esc     :       Quit                ↑ ↓ → ←     :       Select Item
F10     :       Save & Exit Setup   (Shift)F2    :       Change Color

                    Time, Date, Hard Disk Type . . .
```

Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the BIOS or SETUP defaults will affect all the options in this screen (or all parameters if defaults are loaded from the Main Menu) and will reset options previously altered.

The BIOS Default settings consist of the **safest** set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.

The SETUP Default values provide **optimum performance** settings for all devices and system features.

CAUTION

These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

4.1.2 Main Menu

The Main Menu includes the following categories:

Category	Description
Standard CMOS Setup	This Setup page includes all the items in a standard, AT-compatible BIOS (date, time, hard disk type, floppy disk type, video adapter type, memory, etc.).
BIOS Features Setup	This Setup page includes all the items of AWARD's special enhanced features.
Chipset Features Setup	This Setup page includes all the items of the chipset's special features.
Power Management Setup	This Setup page sets power conservation options.
PnP/PCI Configuration	This Setup page sets Plug and Play and PCI configuration options.
CPU/Board Features Setup	This Setup page sets processor speed, thermal management and board monitoring options.
Integrated Peripherals	I/O susbsystems that depend on the integrated peripherals controller in your system.
Load Bios Defaults	The BIOS defaults are **fail safe** settings, which consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance.
Load Setup Defaults	The Setup defaults are the **optimal** settings that provide the optimum performance for all devices and system features. **If the CMOS RAM is corrupted, the Setup defaults are loaded automatically.**
Supervisor/User Password Setting	Change, set or disable the password. It allows you to limit the access to the system and the Setup, or only to the Setup.
IDE HDD Auto Detection	Forces the detection of the IDE hard disk drives parameters and puts them in the Standard CMOS Setup page.
Save & Exit	After having modified the BIOS Setup, you can save the configuration in CMOS RAM and the Flash BIOS, by selecting this option.
Exit Without Saving	This option is used to exit AWARD Setup without saving the configuration to CMOS RAM or Flash BIOS.

4.1.3 Setups

The arrow keys (↑ ↓ → ←) are used to highlight items on the menu and the PAGEUP and PAGEDOWN keys are used to change the entry values for the highlighted item. To enter in a submenu, press the ENTER key. Also, you can press the F1 key to obtain help information or the ESC key to close a menu or to quit the program.

Key	Function
↑	Moves to previous item.
↓	Moves to next item.
←	Moves to the item a the left.
→	Moves to the item at the right.
ESC	When in the Main Menu: Quits program (Answer 'Y' to save changes into CMOS). When in other screens: Exits and returns to the Main Menu.
PAGEUP or +	Increases the numeric value or changes value.
PAGEDOWN or -	Decreases the numeric value or changes value.
F1	Help Menu
F2 / <Shift>F2	At the main menu, change the color of the menu.
F5	When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup, Integrated Peripherals Setup or CPU Board Features: Restores the previous setup values for that setup screen only.
F6	When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup, Integrated Peripherals Setup or CPU Board Features: Loads the BIOS Defaults for all the BIOS parameters for that setup screen only.
F7	When in BIOS Features Setup, Chipset Features Setup, Power Management Setup, PNP/PCI Setup, Integrated Peripherals Setup or CPU Board Features: Loads the Setup Defaults for the BIOS parameters for that setup screen only. If the CMOS RAM is corrupted, the Setup defaults are loaded automatically.
F10	When in the Main Menu: Saves all the CMOS changes and exit.

4.1.4 Standard CMOS Setups

Function	Description
Date/Time	The current values for each category are displayed. Enter new values through the keyboard.
Hard Disks	Two IDE controllers are defined on the cPCI-MXP64 boards. The Primary and Secondary controllers can both have two disks: Master Disk or Slave Disk. Only three settings are available for the hard disk type: Auto, User and None. Type 1 to 46 are not predefined in the system: Use auto or enter the parameters for the type in the user-defined.
Drive A / Drive B	Select the type of floppy disk installed for drive A and drive B.
Video	This option specifies the basic type of display adapter card installed in the system.
Halt on	This option specifies the type of errors that will stop the system during the BIOS booting procedure. A message asks that you press F1 to continue or press the DELETE key to enter Setup. The settings are: All errors, No errors, All but keyboard, All but diskette, and All but disk/key (default setting).
Memory	This display-only option indicates the amount of Base, Extended and other types of memory installed in the system.

4.1.5 BIOS Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Virus Warning	Dis.	Dis.	En. / Dis.	When Enabled, you receive a warning message if a program (specifically, a virus) attempts to write to the boot sector or the partition table of the hard disk drive. You should then run an anti-virus program. Keep in mind that this feature protects only the boot sector, not the entire hard drive. **Note: Many disk diagnostic programs and OS setups (e.g., Win95 setup), that access the boot sector table, can trigger the virus warning message. If you plan to run such a program, we recommend that you first disable the virus warning.**
Quiet POST	Dis.	Dis.	En./Dis.	At the power on self-test (POST), only the AWARD logo and the "Press DEL to enter SETUP" message appears.
Quick Power On Self Test	Dis.	En.	En./Dis.	Select Enabled to reduce the amount of time required running the POST. A quick POST skips certain steps. We recommend that you enable quick POST to save time, since most major OS do their own tests
Full Screen Logo Show	Dis.	Dis.	En./Dis.	When enabled, a full screen bitmap (BMP) picture will appear during the POST or you can have your logo being displayed. Contact the technical Support (see Appendix G).
Boot from LAN First	None	None	None LAN1, LAN2, LAN1-2, LAN2-1	When "None" is selected the option is disabled, otherwise the BIOS will first attempt to boot from the LAN. If LAN1-2 is selected, the first attempt to boot is done with LAN1 and if it fails, with LAN2 (LAN2-1, first attempt with LAN2, second attempt with LAN1). The complete procedure for this function is available on the "Boot from LAN" utility CDROM.
Raid Card Boot First	Dis.	Dis.	En./Dis.	If Enabled, the BIOS will first attempt to boot from the RAID disk card.
Boot Sequence	A,C, SCSI	C,A, SCSI	A,C,SCSI; C,A,SCSI; C,CDROM,A; CDROM,C,A; D,A,SCSI; E,A,SCSI; F,A,SCSI; SCSI,A,C; SCSI,C,A; C only; LS/ZIP,C.	This option defines the searching order in the BIOS for the boot device(s). **Note: The Boot from LAN First and Raid Card Boot First options take precedence over this option.**
Repeat Boot Sequence	Dis.	Dis.	En./Dis.	If boot fails, the BIOS will restart the BOOT sequence. After each failure to boot, the BIOS will continue to restart the BOOT sequence, each sequence being separated by a delay of 1 second.
Swap Floppy Drive	Dis.	Dis.	En./Dis.	Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B.
Boot Up Floppy Seek	En.	Dis.	En./Dis.	When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360KB floppy drives have 40 tracks; drives with 720KB, 1.2MB, and 1.44MB capacity all have 80 tracks. Because very few modern PCs have 40 track floppy drives, we recommend that you set this field to "Disabled" to save time.
Drive A Boot Permit	En.	En.	En./Dis.	When Disabled, this option will not permit booting from Drive A.
Floppy Disk Access Control	R/W	R/W	R/W, Read Only	When Read Only, this option will not permit writing to the floppy disk.

BIOS Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Report No FDD For Win 95	No	No	Yes, No	Select Yes to release IRQ6 when the system contains no floppy drive, for compatibility with Windows 95 logo certification. In the Integrated Peripherals screen, select NO on the Onboard FDC Controller option.
Hard Disk Write Protect	Dis.	Dis.	En./Dis.	When Enabled, this option will not permit writing to the hard disk.
HDD S.M.A.R.T. Capability	Dis.	En.	En./Dis.	When Enabled, the Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.) features of the HDD are supported. S.M.A.R.T is used for prediction of device degradation and/or faults.
Delay For HDD (Secs)	0	0	0-15	This number of seconds inserted prior to HDD initialization. 0 is disabled.
OS Select For DRAM > 64MB	Non-OS/2	Non-OS/2	Non-OS/2, OS/2	Select OS2 only if you are running OS/2 with greater than 64MB of RAM.
Gate A20 Option	Norm.	Fast	Normal, Fast	When Fast, enables fast switching of Gate A20 via the 440BX chipset, instead of the keyboard controller.
Security Option	Setup	Setup	Setup, System	If you have set a password, select whether the password is required every time the system boots (“System” option), or only when you enter Setup (“Setup” option).
Diskette Access For	All	All	All, Supervisor	When this option is set to Supervisor and the Security option to System, all floppy disk accesses (read/write) are limited to the Supervisor (supervisor password required).
Boot Up NumLock Status	On	On	On, Off	Control the state of the NumLock key when the system boots. When set to “On”, the numeric keypad generates numbers instead of controlling cursor operations.
Typematic Rate Setting	Dis.	En.	En./Dis.	When Disabled, the following two items (Typematic Rate and Typematic Delay) are irrelevant. Keystrokes repeat at a rate determined by the keyboard controller in your system. When Enabled, you can select a typematic rate and a typematic delay.
Typematic Rate (Chars/s)	30	30	6-30 char/sec.	When the typematic rate setting is Enabled, you can select a typematic rate (the rate at which characters repeat when you hold down a key).
Typematic Delay (msec)	250	250	250-1000 ms	When the typematic rate setting is Enabled, you can select a typematic delay (the delay before keystrokes begin to repeat when you hold down a key).
VT100 Settings				
Comport	1	1	1,2	Use this option to select which COM port will be used for VT100
Speed	Auto	Auto	Auto, 2400, 9600, 19200, 38400, 57600, 115200	Select the baud rate of COM port. used in VT100 mode.
Parity	None	None	None, Odd, Mark, Even, Space	Use this option to select the parity.
Data	8	8	7, 8	Use this option to specify the number of data bits being used.
Stop	1	1	1, 2	Use this option to specify the number of stop bits being used.

4.1.6 Chipset Features Setup

This part of the setup allows you to define chipset-specific options and features.

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
CPU Internal Cache	Dis.	En.	En./Dis.	Enables or Disables the CPU Internal Cache (L1 cache).
External Cache	Dis.	En.	En./Dis.	Enables or Disables the External Cache (L2 cache).
CPU L2 Cache ECC Checking	Dis.	En.	En./Dis.	Enables or Disables ECC Checking for L2 cache. **Note: processors provided by Kontron support ECC. However, not all Pentium® II / III processors support ECC. Check Intel's website to know if your processor supports ECC:** http://developer.intel.com/support/processors/pentiumII/identify.htm.
SDRAM RAS-to-CAS Delay	3	3	2, 3	**Note: Upon boot-up, the BIOS will detect and display the optimal value for the SDRAM options, if it is different from the Setup value. You must enter the AWARD Setup, and set the options at the suggested value if you want the best performance.** This option inserts a timing delay between the CAS and RAS strobe signals, used when SDRAM is written to, read from, or refreshed. The number selected is the number of clocks to be inserted between a row activate command and either a read or write command.
SDRAM RAS Precharge Time	3	3	2, 3	Selects the number of CPU clocks for the RAS precharge. If an insufficient number of cycles is allowed for the RAS to accumulate its charge before SDRAM refresh, the refresh may be incomplete and the DRAM may fail to retain data.
SDRAM CAS Latency Time	3	3	2, 3	This option controls the number of clocks between when a read command is sampled by the SDRAMs and when the chipset samples read data from the SDRAMs. Select 3 for 3 DCLKs and 2 for 2 DCLKs. If a given row is populated with a registered SDRAM DIMM, an extra clock is inserted between the read command and when the chipset samples read data.
SDRAM Precharge Control	Dis.	Dis.	En./Dis.	When Enabled, all CPU cycles to SDRAM result in an All Banks Precharge Command on the SDRAM interface.
DRAM Data Integrity Mode	Non-ECC	ECC	ECC, Non-ECC	When set to ECC, allows auto-correction of the data read from memory. The ECC error flags' status register and the error pointer are updated if error correction occurs in this mode. When set to Non-Ecc, no error checking or error reporting is done. This option will work in ECC mode only if all installed memory banks supports ECC (Error Checking and Correction)
Memory Hole At 15M-16M	Dis.	Dis.	En./Dis.	You can reserve this area of system memory for ISA adapter ROM. When this area is reserved, it cannot be cached. The user information of peripherals that need to use this area of system memory usually discusses their memory requirements.
Video BIOS Cacheable	Dis.	En.	En./Dis.	Selecting Enabled allows caching of the video BIOS ROM at C0000h plus the VGA BIOS size, resulting in better video performance. However, in any program writes to this memory area, a system error may occur.
Video RAM Cacheable	Dis.	En.	En./Dis.	When Enabled, video memory region is cacheable. Some off-board video card drivers may behave strangely; in such a case, disable this option.
8 Bit I/O Recovery Time	3	1	1-8, NA	The I/O recovery mechanism adds bus clock cycles between PCI-originated I/O cycles to the ISA bus. This delay takes place because the PCI bus is much faster than the ISA bus. These two fields let you add recovery time (in bus clock cycles) for 8-bit and 16-bit I/O.
16 Bit I/O Recovery Time	2	1	1-4, NA	

Chipset Features Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
PCI/VGA Palette Snoop	Dis.	Dis.	En./Dis.	Palette snooping allows multiple VGA devices operating on different buses to handle data from the CPU on each set of palette registers. When set to Enabled, data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA device's palette registers, permitting the palette registers of both to be identical. When set to Disabled, data read and written by the CPU is only directed to the PCI VGA device's palette registers.
Passive Release	En.	En.	En./Dis.	When Enabled, CPU to PCI bus accesses are allowed during passive release otherwise the arbiter only accepts another PCI master access to local SDRAM.
Delayed Transaction	Dis.	Dis.	En./Dis.	The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specifications version 2.1.
Supervisor I/O Base Address	190h	190h	190h, 290h, 390h	This option determines the base address for the Supervisor I/O Register, which is used for such functions as power fail detection and the watchdog timer.
Power-Supply Type	AT	AT	AT, ATX	This option selects the type of power supply.
AGP Aperture Size (MB)	64	64	4 to 256	This option selects the size in megabytes of the AGP Aperture.
Video BIOS Shadow	Dis	Auto	Auto/Dis	Software that resides in a read-only memory (ROM) chip on a device is called *firmware*. Award permits shadowing of firmware such as the system BIOS, video BIOS, and similar operating instructions that come with some expansion peripherals. Shadowing copies from ROM into system RAM, where the CPU can read it through the 64-bit DRAM bus. Firmware not shadowed must be read by the system through the 8 or 16-bit ISA bus. Shadowing improves the performance of the system BIOS and similar firmware for expansion peripherals. Enable shadowing into each section of memory separately. Many system designers hardwire shadowing of the system BIOS and eliminate a System BIOS Shadow option. Note that on a PCI VGA card (on board or off-board), the VGA BIOS is always shadowed. Video BIOS shadows into memory area C0000 plus the VGA BIOS size. The remaining areas between C0000 and DFFFF shown on the BIOS Features Setup screen may be occupied by other expansion card firmware. If an expansion peripheral in your system contains ROM-based firmware, you need to know the address range the ROM occupies to shadow it into the correct area of RAM. When Auto, if an extension BIOS is detected the zone will be automatically shadowed. If no BIOS is deteted, the zone will remain Disabled even if mode is Auto.
C8000-CBFFF	Dis	Auto	Auto/Dis	
CC000-CFFFF	Dis	Auto	Auto/Dis	
D0000-D3FFF	Dis	Auto	Auto/Dis	
D4000-D7FFF	Dis	Auto	Auto/Dis	
D8000-DBFFF	Dis	Auto	Auto/Dis	
DC000-DFFFF	Dis	Auto	Auto/Dis	

4.1.7 Power Management Setup

This part of the setup configures power conservation options.

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
ACPI Function	Dis.	Dis	En./Dis.	The Advanced Configuration and Power Interface (ACPI) allows Operating System Direct Power Management (OSPM) and make advanced configuration architectures possible. When Enabled, the OS supports ACPI or OSPM (e.g., Win98, and Windows 2000 **Note: When Enabled, and the OS is ACPI compliant, the OS setting take precedence over all settings in this menu.**
Power Management	User Def.	User Def.	User Define, Min Saving, Max Saving	This option allows you to select the type (or degree) of power saving for Doze, Standby, and Suspend modes. Max Saving: Maximum power savings. Inactivity period is 1 minute in each mode. Min Saving: Minimum power savings. Inactivity period is the maximum setting in each mode (1 hour for Doze, Standby and Suspend). User Define: Set each mode individually. Select time-out periods in the PM Timers section (see below).
PM Control by APM	Yes	Yes	Yes, No	If Yes, the OS can control the PM by APM calls. If No, the BIOS will control the PM (Power Management)
Video Off Method	V/H SYNC + Blank	V/H SYNC + Blank	Blank Screen V/H SYNC+Blank, DPMS,	Determines the manner in which the monitor is blanked. V/H SYNC + Blank: System turns off vertical and horizontal synchronization ports and writes blanks to the video buffer. DPMS Support: Select this option if your monitor supports the Display Power Management Signaling (DPMS) standard of the Video Electronics Standards Association (VESA). Use the software supplied for your video subsystem to select video power management values. Blank Screen: System only writes blanks to the video buffer.
Video Off After	Standby	Standby	NA, Suspend, Standby, Doze,	As the system moves from lesser to greater power-saving modes, select the mode **in which you want the monitor to blank.**
Doze Mode	Dis.	Dis	Disable 1min to 1h	After the selected period of system inactivity (1 minute to 1 hour), the CPU clock runs at lower speed while all other devices still operate at full speed.
Standby Mode	Dis.	Dis.	Disable 1min to 1h	After entering Doze mode and the selected period of system inactivity (1 minute to 1 hour) has elapsed, the non-essential devices are shut off while all other devices still operate at full speed.
Suspend Mode	Dis.	Dis.	Disable 1min to 1h	After entering Standby mode and the selected period of system inactivity (1 minute to 1 hour) has elapsed, all devices including the CPU shut off and the system waits for an event to wake them up again.
HDD Power Down	Dis.	Dis.	Disable 1-15min	After the selected period of drive inactivity (1 to 15 minutes), the hard disk drive powers down while all other devices remain active. The HDD power down mode is only available if the hard drive has this capability.
HDD Down When Suspend	En.	En.	En./Dis.	When Enabled and the system goes in Suspend Mode, the hard disk is shut down.
Throttle Duty Cycle	75.0%	75.0%	12.5%-75.0%	When the system enters Doze mode, the CPU clock runs only part of the time. You may select the percentage of time that the clock **does not run.** When 12.5% is selected, the CPU is running at nearly Full Speed and if 75% is selected, the CPU will be idle 75% of time.
PCI / VGA Act-Monitor	Dis.	Dis.	En./Dis.	When Enabled, continuous video activity restarts the global timer for Standby mode.
Soft-OFF by PWR-BTTN	Instant-off	Instant-off	Instant-off, Delay 4 sec.	This option only works with an ATX power supply. It allows two configurations for the power button: Instant-off for power supply on/off switch, or Delay 4 sec. for entering Suspend Mode after pressing the button at least 4 seconds.

Power Management Setup (Continued)

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Resume by Ring	Dis.	En.	En./Dis.	When Enabled and a modem is connected to a serial port, allows a modem ring to re-activate the CPU when in Suspend mode.
IRQ 8 Break Suspend	Dis.	En.	En./Dis.	When Enabled, the RTC alarm interrupt is monitored to allow an interrupt to awaken the system when in Doze, Standby or Suspend Mode.
Resume by Alarm	Dis.	Dis.	En./Dis.	When Enabled, allows setup of a time to re-activate the CPU when in Suspend mode with the options Date (of Month) Alarm and Time (hh:mm:ss) Alarm. **Note: The IRQ 8 Break Suspend option in this setup screen must be Enabled to use the RTC alarm.**
Reload Global Timer Events:				
IRQ[3-7,9-15], NMI	Dis.	En.	En./Dis.	When any of the options below is Enabled, monitoring of the interrupt will occur to allow an interrupt to awaken the system when in Doze, Standby or Suspend Mode.
Primary IDE 0	Dis.	En.	En./Dis.	
Primary IDE 1	Dis.	En.	En./Dis.	
Secondary IDE 0	Dis.	En.	En./Dis.	
Secondary IDE 1	Dis.	En.	En./Dis.	
Floppy Disk	Dis.	En.	En./Dis.	
Serial Port	En.	En.	En./Dis.	
Parallel Port	Dis.	En.	En./Dis.	

4.1.8 PnP/PCI Configuration

This part of the setup configures PnP/PCI options.

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
PNP OS Installed	Yes	No	Yes, No	If the operating system (OS) is Plug and Play (for example Windows 95), select "**Yes**" if you want the OS to allocate resources according to Plug and Play standards, or "**No**" if you want the same resource allocations at every system boot-up. Select "**No**" when the OS is **not** Plug and Play (for example, DOS). **Note: When set to "Yes", only the boot devices will get Resources.**
Resources Controlled By	Auto	Man.	Auto, Man.	The Award Plug and Play BIOS can automatically configure all the boot and Plug and Play-compatible devices. If you select Auto, all the interrupt requests (IRQs) and DMA assignment fields disappear as well as Used Mem Base Address and Lenght as the BIOS automatically assigns them.
Reset Configuration Data	Dis.	Dis.	En./Dis.	Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.
IRQ *n* Assigned To (n = 3, 4, 5, 7, 9, 10, 11, 12, 14, 15)	PCI/ISA PnP	PCI/ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific interrupt. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for an IRQ line, this resource will not be available for PCI/ISA PnP.
DMA *n* Assigned To (n = 0, 1, 3, 5, 6, 7)	PCI/ISA PnP	PCI/ISA PnP	PCI/ISA PnP, Legacy ISA	When resources are controlled manually, assign each system DMA channel as one of the following types, depending on the type of device using the interrupt: Legacy ISA: Devices compliant with the original PC AT bus specification, requiring a specific DMA channel. PCI/ISA PnP: Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture. When Legacy ISA is selected for a DMA channel, this resource will not be available for PCI/ISA PnP.
Init Display First	Onboard	Onboard	PCI Slot, Onboard, AGP	Initializes the specified video display. The chosen display becomes the primary display. Other display devices are ignored by the BIOS and configured by the OS.
Assign IRQ For VGA	Dis.	Dis.	En./Dis.	When Enabled, the video card is assigned an IRQ.
Assign IRQ For USB	En.	En.	En./Dis.	When Enabled, the USB is assigned an IRQ. When Disabled, the IRQ is freed up for another purpose.
PCI Latency Timer	32	32	0-255 (integers)	This option specifies the value of the Latency Timer for the PCI bus master, in units of PCI bus clocks.
Bridge Init Delay	150ms	150ms	150, 300, 600, and 1200 ms	Each time the Bios finds a bridge, it resets the bridge and wait for a duration of the chosen delay. After this delay, it scans the devices behind the bridge.
Used MEM Base Address	N/A	N/A	N/A, C800, CC00, D000, D400, D800	Select a base address for the memory area used by any peripheral that requires high memory.

4.1.9 CPU/Board Features Setup

Option	BIOS Defaults	Setup Defaults	Possible Settings	Description
Processor Speed	nnn	nnn	nnn	This option displays the processor speed.
Front Side Bus Speed	nnn	nnn	nnn	This option displays the current Front Side Bus speed. This speed is selected by the CPU auto-detection logic.
Thermal Management Options:				
Thermal Management	Dis.	Dis.	En./Dis.	When this option is enabled, the CPU temperature is monitored. Whenever the CPU overheats, the CPU slows down to lower the temperature.
Thermal Audio Alarm	Dis.	Dis.	En./Dis.	When the Thermal Management option and this option are enabled, a continuous audible alarm is sounded when the temperature specified in the Overheat Alarm options is reached. Such an alarm may not be supported by the Operating System.
CPU Die Temperature	-	-	Varies	Displays the current die (internal) CPU temperature, when Thermal Management is enabled.
Resume Alarm (°C)	50	50	10-70	The CPU will be slowed down when it reaches the selected Overheat Alarm (°C) temperature. Full speed will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 4° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm.
Overheat Alarm (°C)	70	70	30-90	The CPU will be slowed down when it reaches the selected Overheat Alarm (°C) temperature. Full speed will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 4° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm
CPU Local Temperature	-	-	Varies	Displays the current case (external) CPU temperature, when Thermal Management is enabled.
Resume Alarm (°C)	42	42	10-70	The CPU will be slowed down when it reaches the selected Overheat Alarm (°C) temperature. Full speed will be resumed when the temperature comes down to the selected Resume Alarm (°C) temperature. A minimum of + 4° is automatically ensured for the Overheat Alarm temperature with reference to the Resume Alarm.
Overheat Alarm (°C)	50	50	30-90	
Save CMOS in Flash	Dis.	Dis.	En./Dis.	Saving CMOS memory content into Flash Memory will prevent to loose CMOS options when battery fails.
Watchdog Timer	Dis	Dis	En./Dis.	This option enables the Watchdog option when the POST is running.
Watchdog After POST	Ds	Dis	En./Dis.	This option enables Watchdog circuit after the POST sequence
Watchdog Duration (ms)	262144	262144	64 to 262144	Use this option to setup duration time (in ms) of the Watchdog timing circuitry.
CPU Fan speed	-	-	Varies	Speed sensing device sets this value according to the fan speed. If no fan is installed or if a fan has no tachymetric capability, this value will be 0.
Current Vcpp1 and 2	-	-	Varies	This value is set according to the actual value of Vcpp1 & Vcpp2
Vin values : +12V, +5V, +3.3V, +2.5V	-	-	Varies	The values of these voltages are each displayed according to the current value.

4.1.10 Integrated Peripherals

Option	BIOS efault	Setup efault	Possible Settings	Description
On-Chip Primary IDE controller	En.	En.	En./Dis.	Select Enabled to activate the IDE controller. The four options below appear only if the On-Chip Primary option is enabled.
IDE Primary Master PIO IDE Primary Slave PIO	Auto	Auto	Auto, Modes 0-4	Use this option to set a PIO mode (0-4) for each of the onboard IDE devices. Modes 0 through 4 provide successively increased performance and speed. In Auto mode, the system automatically determines the best mode for each device. If you select a mode that the drive does not support, it may not work, so choose a lesser value or Auto to see the best mode for the drive.
IDE Primary Master UDMA IDE Primary Slave UDMA	Dis.	Auto	Auto, Disabled.	Ultra DMA/33 implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If your hard drive and your system software both support Ultra DMA/33, select Auto to enable BIOS support.
On-Chip Secondary IDE controller	En.	En.	En./Dis.	Select Enabled to activate the IDE controller. The four options below appear only if the On-Chip Secondary option is enabled.
IDE Secondary Master PIO IDE Secondary Slave PIO	Auto	Auto	Auto, Modes 0-4	Use this option to set a PIO mode (0-4) for each of the onboard IDE devices. Modes 0 through 4 provide successively increased performance and speed. In Auto mode, the system automatically determines the best mode for each device. If you select a mode that the drive does not support, it may not work, so choose a lesser value or Auto to see the best mode for the drive.
IDE Secondary Master UDMA IDE Secondary Slave UDMA	Dis.	Auto	Auto, Disabled.	Ultra DMA/33 implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If your hard drive and your system software both support Ultra DMA/33, select Auto to enable BIOS support.
IDE HDD Block Mode	Dis.	En.	En./Dis.	Block mode is also called block transfer, multiple commands, or multiple sector read/write. If your IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.
Ethernet Controller 1	En.	En.	En./Dis.	Enables/disables the onboard Ethernet controller 1.
Ethernet Controller 2	En.	En.	En./Dis.	Enables/disables the onboard Ethernet controller 2.
USB Keyboard Support	OS	OS	OS/BIOS	This option is for DOS and BIOS support only (Win 95 has it is own drivers). **It does not enable or disable the USB controller.**
PS/2 Mouse Function Control	Auto	Auto	Auto/Dis.	When set to Auto, the PS/2 mouse is automatically enabled, if it is present.
Onboard FDC Controller	En.	En.	En./Dis.	Select Disabled to disable the onboard floppy disk controller (FDC).
Onboard Serial Port 1	Auto	Auto	Dis, 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3 Auto	Select a COM port address and IRQ# for Serial Port 1

Integrated Peripherals (continued)

Option	BIOS efault	Setup efault	Possible Settings	Description
Onboard Serial Port 2	Auto	Auto	Dis, 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3 Auto	Select a COM port address for Serial Port 2.
Serial Port 2 Mode	RS-232	RS-232	RS-232 RS-422 RS-485	
Onboard Parallel Port	378/ IRQ7	378/ IRQ7	Disabled 3BC/IRQ7 378/IRQ7 278/IRQ5	Select a LPT address and IRQ# for the physical parallel (printer) port.
Parallel Port Mode	ECP + EPP1.9	ECP + EPP1.9	SPP, EPP1.9+SPP, ECP ECP+EPP1.9, Normal, EPP1.7+SPP, ECP+EPP1.7	Select an operating mode for the onboard parallel port. Select ECP or EPP unless you are certain both your hardware and software does not support ECP or EPP mode.
ECP Mode Use DMA	3	3	1, 3	Select a DMA channel for the parallel port.

4.2. UPDATING OR RESTORING THE BIOS IN FLASH

The BIOS update procedure can be found with the Emergency Recovery procedure on our ftp site: ftp://ftp.kontron.ca/Support in the FAQ section:

Download the FAQ# KC_0028 at location:

ftp://ftp.kontron.ca/Support/Support_FAQ - Questions & Answers/

4.3. VT100 MODE

The VT100 operating mode allows remote setups of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

4.3.1 Requirements

The terminal should emulate a VT100 or ANSI terminal. Terminal emulation programs such as Telix© or Procom© can also be used.

4.3.2 Setup & Configuration

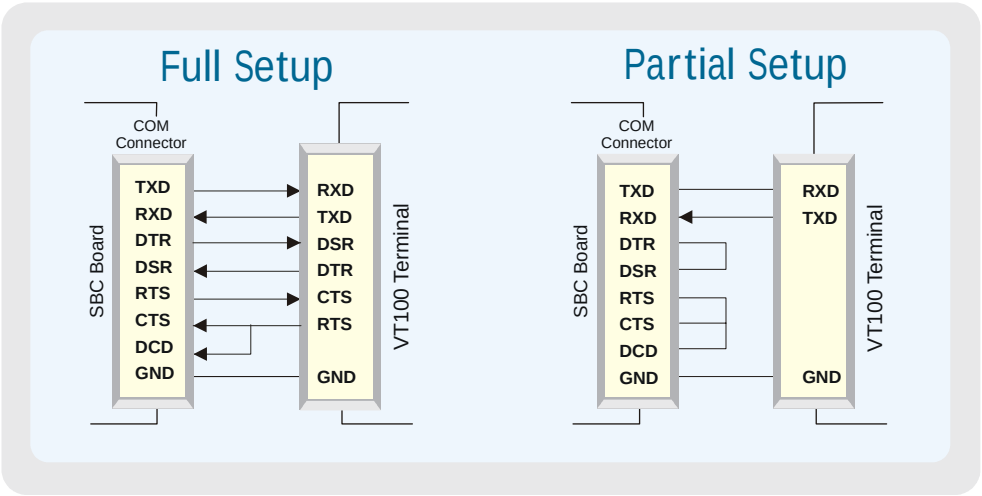
Follow these steps to set up the VT100 mode:

1. Connect a monitor and a keyboard to your board and turn on the power.
2. Enter into the CMOS Setup program in the “BIOS Feature Setup”
3. Select the VT100 mode and the appropriate COM port and save your setup.
4. Connect the communications cable as shown in the next page.

> NOTE
>
> If you do not require a full cable for your terminal, you can set up a partial cable by using only the TXD and RXD lines. To ignore control lines simply loop them back as shown in VT100 Partial Setup cable diagram.

5. Configure your terminal to communicate using the same parameters as in CMOS Setup.
6. Reboot the board.
7. Use the remote keyboard and display to setup the BIOS.

Save the setup, exit, and disconnect the remote computer from the board to operate in stand-alone configuration.



4.3.3 Running Without a Terminal

The board can boot up without a screen or terminal attached. If the speed is set to Auto and no terminal is connected, the speed is set to 115,200 bauds.

Furthermore, you can run without any console at all by simply not enabling VT100 Mode and by disabling the onboard video.

PART 5

APPENDICES

A. BOARD DIAGRAMS

B. CONNECTOR PINOUTS

C. MEMORY & I/O MAPS

D. INTERRUPT LINES

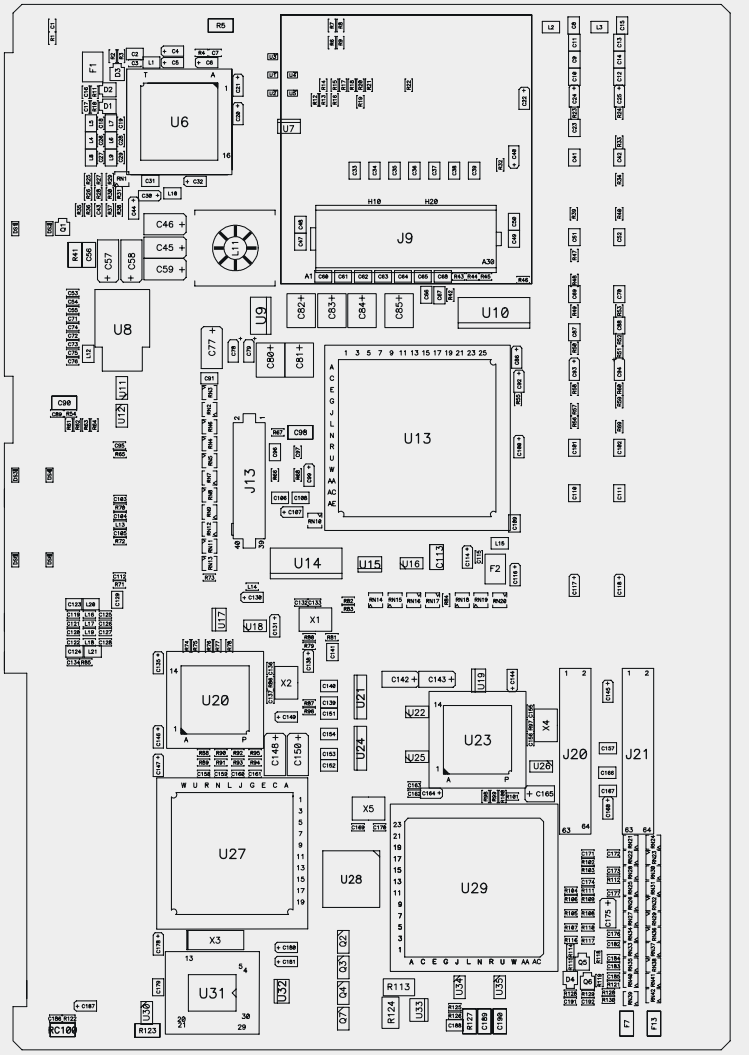
E. BIOS SETUP ERROR CODES

F. EMERGENCY PROCEDURE

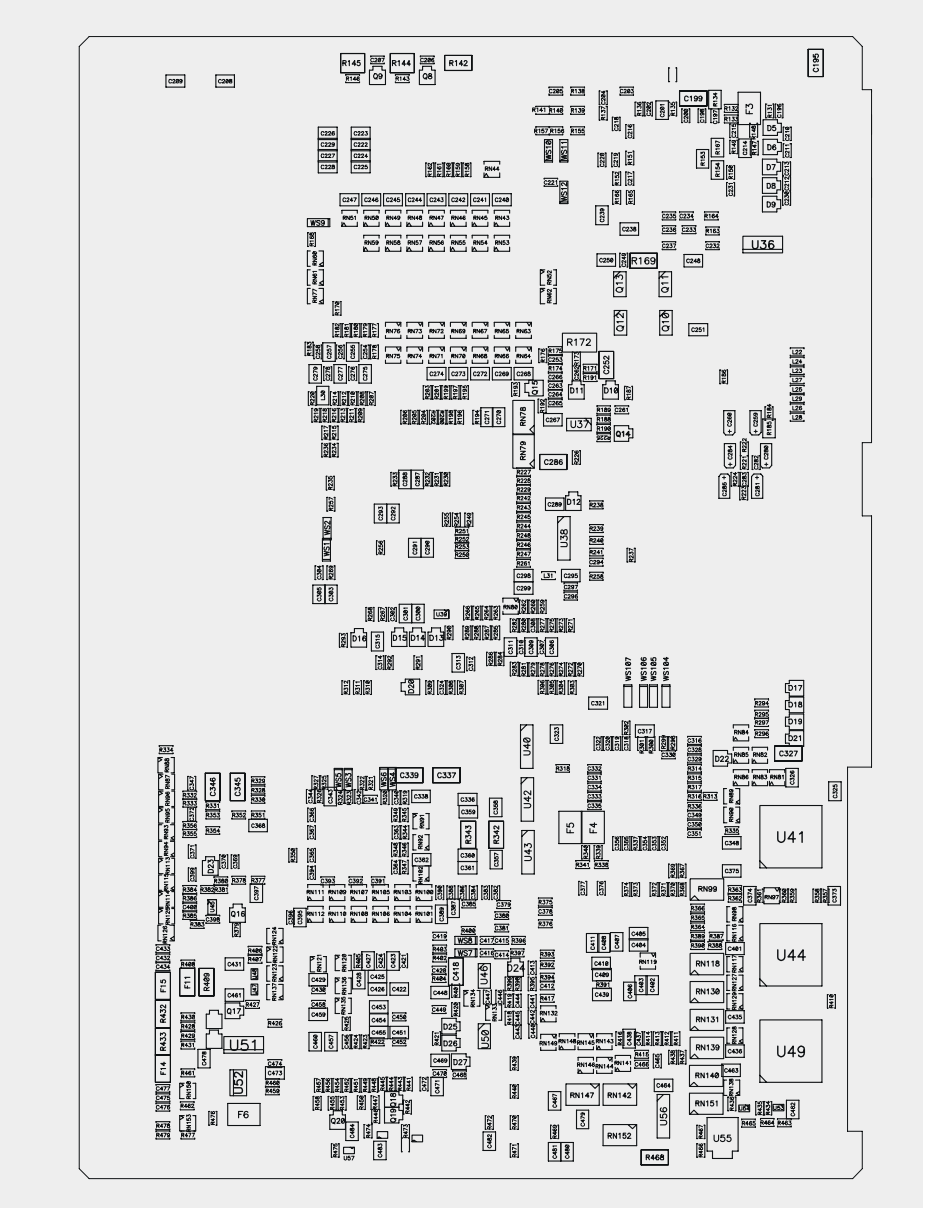
G. GETTING HELP & RMA

A. BOARD DIAGRAMS

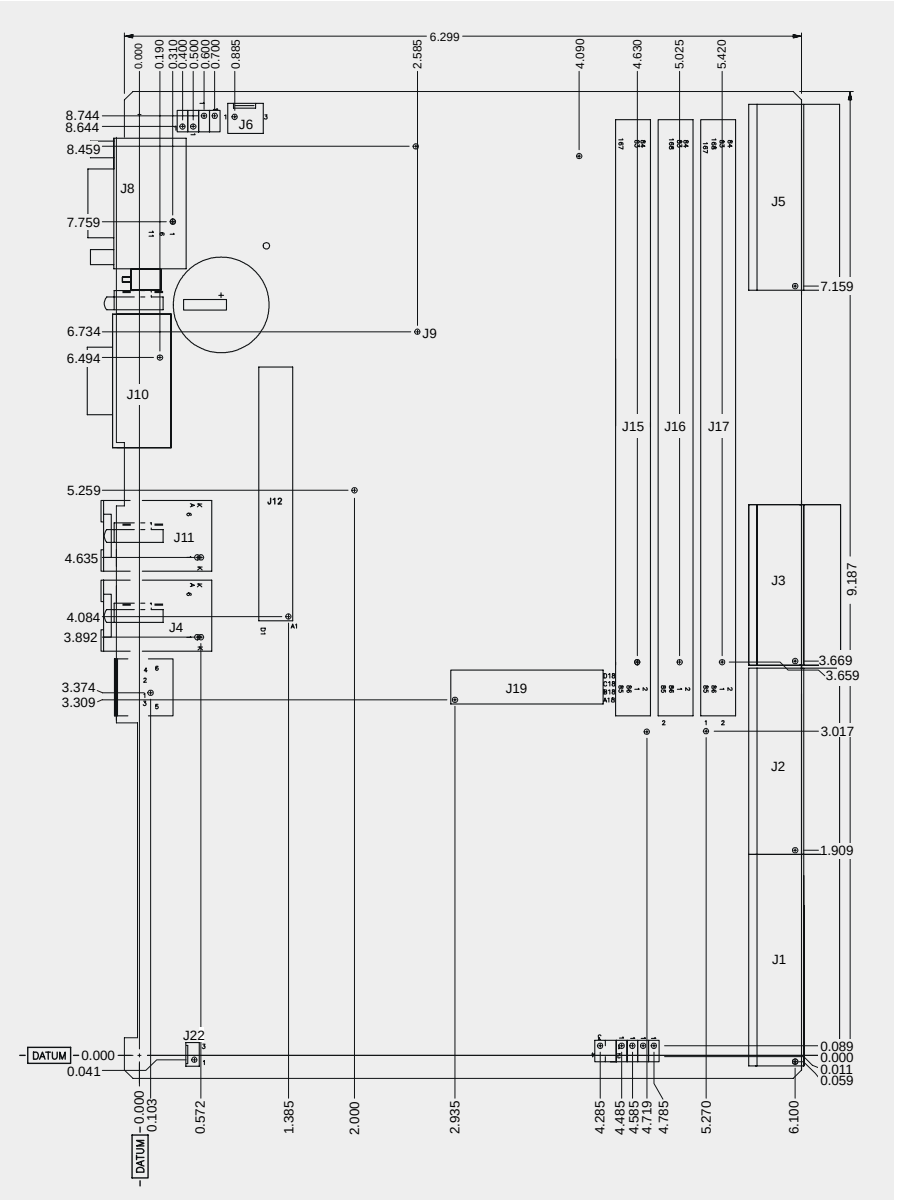
A.1 ASSEMBLY TOP DIAGRAM



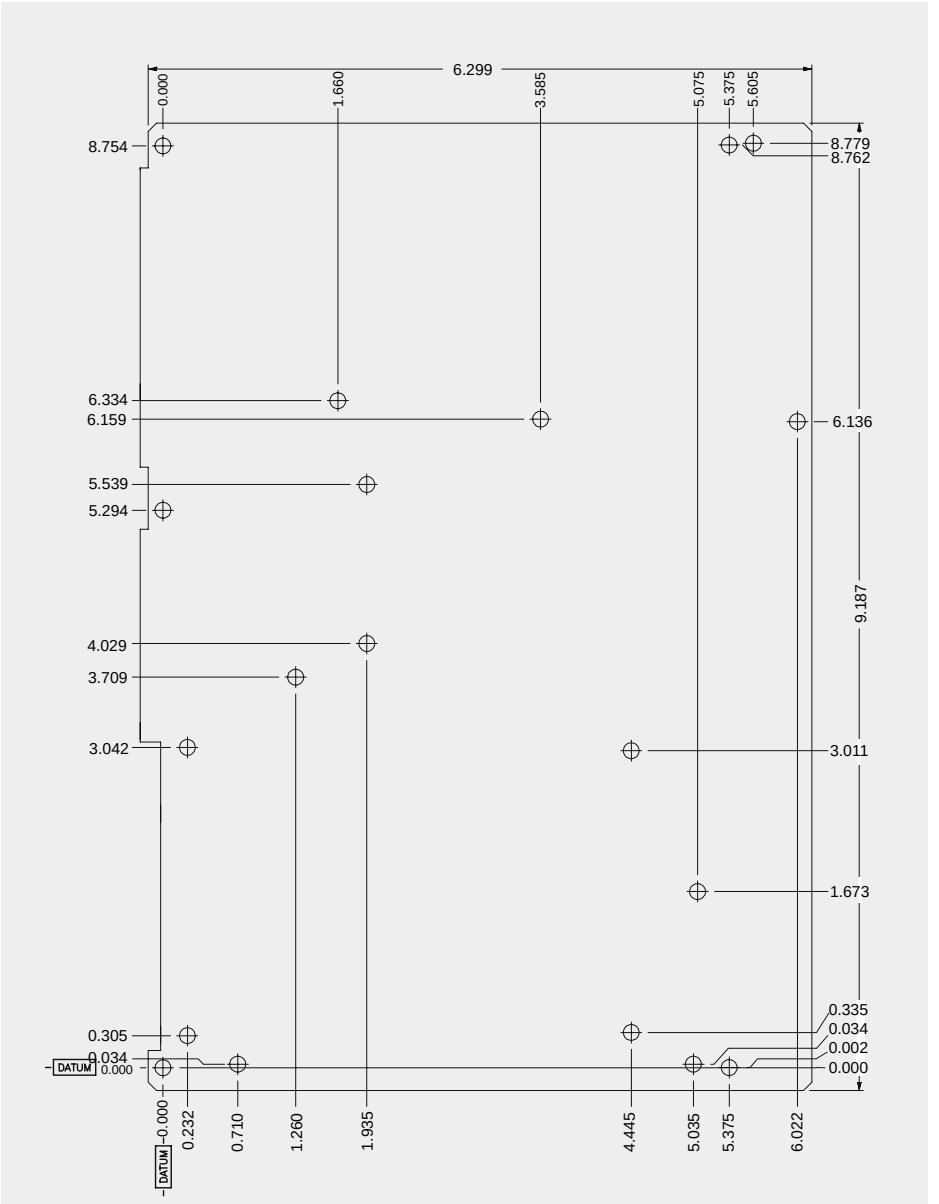
A.2 ASSEMBLY BOTTOM DIAGRAM



A.3 CONNECTOR DIMENSIONS



A.4 MOUNTING HOLES



B. CONNECTOR PINOUTS

B.1 CONNECTORS AND HEADERS ON THE CPCI-MXP64

Connectors and Headers on the cPCI-MXP64	
J1	CPCI Bus Connector
J2	CPCI Bus Connector
J3	CPCI I/O Connector
J4	Ethernet 1 Connector (Front panel configuration only)
J5	CPCI I/O Connector
J6	CPU Fan and Tachometer
J8	CRT VGA Connector (Front panel only)
J10	Serial Port 1 – RS-232 (Front panel configuration only)
J11	Ethernet 2 Connector (Front panel configuration only)
J12	Mezzanine PCI Connector
J13	CompactFLASH Disk Connector
J15-J17	Memory
J18	Keyboard/Mouse Connector
J19	Mezzanine Storage Connector
J20	PCI Mezzanine Card (PMC)
J21	PCI Mezzanine Card (PMC)
J22	Hot Swap Switch
B1	CMOS Battery Backup connector

B.2 J1 cPCI BUS CONNECTOR

Pin	Row A	Row B	Row C	Row D	Row E
1	VCC5E	-12VE	RSV.	+12VE	VCCE
2	RSV	VCCE	RSV	RSV	RSV
3	INTA#	INTB#	INTC#	**VCCE**	INTD#
4	Reserved	HEALTHY#	**VI/O**	RSV	RSV
5	BRSV	BRSV	RST#	**GND**	GNT#
6	REQ#	GND	**VCC3E**	P_CLK	AD31
7	AD30	AD29	AD28	**GND**	AD27
8	AD26	GND	VI/O	AD25	AD24
9	CBE3#	***IDSEL***	AD23	**GND**	AD22
10	AD21	GND	VCC3E	AD20	AD19
11	Ad1	AD17	AD16	**GND**	CBE2#
12	*K E Y A R E A*				
13					
14					
15	VCC3E	FRAME#	IRDY#	***BD_SEL#***	TRDY#
16	DEVSEL#	GND	VI/O	STOP#	LOCK#
17	VCC3E	I2C_SCL	I2C_SDA	**GND**	PERR#
18	SERR#	GND	VCC3E	PAR	CBE1#
19	VCC3E	AD15	AD14	**GND**	AD13
20	AD12	GND	VI/O	AD11	AD10
21	VCC3E	AD9	AD8	M66EN	CBE0#
22	AD7	GND	**VCC3E**	AD6	AD5
23	VCC3E	AD4	AD3	**VCCE**	AD2
24	AD1	VCCE	**VI/O**	AD0	ACK64#
25	VCCE	REQ64#	ENUM#	VCC3E	VCCE

Active low

(1) Short pins (front only) : **B9, D15**

(2) Long Pins (front only) : **C4, C6, C22, C24, D3, D5, D7, D9, D11, D17, D19, D22**

B.3 J2 cPCI BUS CONNECTOR

Pin	Row A	Row B	Row C	Row D	Row E
1	RSV	GND	RSV	RSV	RSV
2	RSV	RSV	SYSEN#	RSV	RSV
3	RSV	GND	RSV	RSV	RSV
4	VI/O	BRSV	CBE7	GND	CBE6#
5	CBE5#	64EN#	VI/O	CBE4#	PAR64
6	AD63	AD62	AD61	GND	AD60
7	AD59	GND	VI/O	AD58	AD57
8	AD56	AD55	AD54	GND	AD53
9	AD52	GND	VI/O	AD51	AD50
10	AD49	AD48	AD47	GND	AD46
11	AD45	GND	VI/O	AD44	AD43
12	AD42	AD41	AD40	GND	AD39
13	AD38	GND	VI/O	AD37	AD36
14	AD35	AD34	AD33	GND	AD32
15	BRSV	GND	FAL#	RSV	RSV
16	BRSV	BRSV	DEG#	GND	BRSV
17	BRSV	GND	RSV	RSV	RSV
18	BRSV	BRSV	BRSV	GND	BRSV
19	RSV	RSV	Reserved	Reserved	Reserved
20	RSV	RSV	RSV	GND	RSV
21	RSV	RSV	RSV	RSV	RSV
22	GA4	GA3	GA2	GA1	GA0

#Active low

B.4 J3 cPCI BUS CONNECTOR

Pin	Row A	Row B	Row C	Row D	Row E
1	RSV	RSV	RSV	RSV	GND
2	GND	RSV	GND	RSV	GND
3	LAN0 :ETX-	VCC	RSV	RSV	RSV
4	RSV	RSV	LAN0:ERX-	RSV	RSV
5	LAN0:ETX+	GND	LAN0:ERX+	GND	RSV
6	LAN0:SPLED	LAN0:LINKLED	LAN0:ACTLED	LAN1:LINKLED	LAN1:SPLED
7	LAN1:ACTLED	SD7	SD6	SD5	SD4
8	GND	VCC	VCC	SD3	SD2
9	LAN1 :ETX+	LAN1 :ETX-	LAN1 :ERX+	LAN1 :ERX-	GND
10	GND	WR_80#	SD1	+12V	+12V
11	RSV	GND	RSV	RSV	RSV
12	RSV	RSV	RSV	VCC	RSV
13	RSV	VCC	RSV	RSV	RSV
14	RSV	RSV	RSV	RSV	RSV
15	RSV	RSV	RSV	SD0	RSV
16	RSV	RSV	RSV	RSV	RSV
17	RSV	RSV	RSV	RSV	RSV
18	RSV	RSV	HDO_ACT#	COM2 :IRRX	COM2 :IRTX
19	RSV	RSV	RSV	RSV	RSV

#Active low

B.5 J5 cPCI BUS CONNECTOR

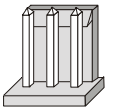
Pin	Row A	Row B	Row C	Row D	Row E
1	IDE0:RST#	IDE0:RST#	IDE0:D7	IDE0:D8	IDE0:D6
2	IDE0:D9	IDE0:D5	IDE0:D10	IDE0:D4	IDE0:D11
3	IDE0:D3	IDE0:D12	IDE0:D2	IDE0:D13	IDE0:D1
4	IDE0:D14	IDE0:D0	USB1:GND	IDE0:D15	IDE0:IRQ14
5	IDE0:REQ	IDE0:IORDY	IDE0:IOW#	IDE0:DACK#	IDE0:IOR#
6	IDE0:IO16#	VGA:VSYNC	IDE0:DIAG#	IDE0:A0	IDE0:A2
7	IDE0:CS1#	IDE0:CS3#	IDE0:A1	RSV	FD:DRVEN0#
8	FD:DRVEN1#	FD:INDEX#	FD:MTR0#	FD:DS1#	FD:DS0#
9	FD:MTR1#	FD:DIR#	FD:STEP#	FD:WDATA#	FD:WGATE#
10	FD:TRK0#	FD:WRPROT#	FD:RDATA#	FD:HDSEL#	FD:DSKCHG#
11	COM2:DCD	VGA:BLUE	COM2:RXD	COM2:DSR	COM2:TXD
12	COM2 :RTS	COM2 :CTS	COM2 :RI	H110EN#	COM2:DTR
13	COM1:DCD	VCC	COM1:RXD	COM1:DSR	COM1:TXD
14	COM1:RTS	COM1:CTS	COM1:RI	VGA:HSYNC	COM1:DTR
15	LPT:SLCT	LPT:PE	LPT:BUSY	LPT:ACK#	LPT:D7
16	LPT:D6	LPT:D5	LPT:D4	LPT:D3	LPT:SLCTIN#
17	LPT:D2	LPT:INIT#	LPT:D1	LPT:ERR#	LPT:D0
18	LPT:ALF#	USB1:DATA+	USB1:DATA-	USB0:GND	USB0:VCC
19	LPT:STB#	USB1:GND	USB1:VCC	USB0:DATA+	USB0:DATA-
20	VGA:SCL	SMBDATA	SMBALERT#	VGA:RED	SMBCLK
21	KB:DATA	KB:CLK	KB:VCC	MOUSE:DATA	MOUSE:CLK
22	PBRST#	VGA:GREEN	DIAG_OC#	VGA:SDA	SPEAKER

#Active low

B.6 J6 – CPU FAN AND TACHOMETER

Pin #	Signal
1	FANTACH
2	+12V DC
3	GND

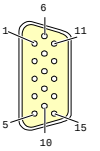
Front View



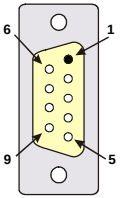
B.7 J8 - CRT VGA CONNECTORS

Signal		Signal		Signal	
RED	1	Analog GND	6	N.C.	11
GREEN	2	Analog GND	7	SDATA	12
BLUE	3	Analog GND	8	HSYNC	13
N.C.	4	N.C.	9	VSYNC	14
GND	5	GND	10	SCLK	15

Top View



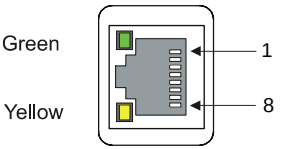
B.8 J10 – SERIAL PORT 1 - RS-232

Pin Number		Top View	Pin Number	
Signal				Signal
DSR	6		1	DCD
RTS	7		2	RXD
CTS	8		3	TXD
RI	9		4	DTR
			5	GND

B.9 J4, J11 - ETHERNET

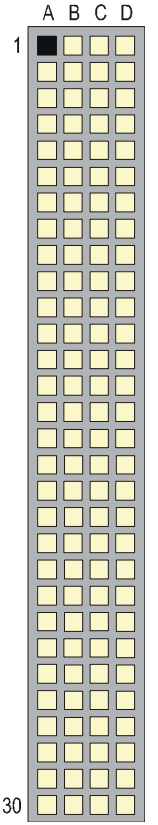
Signal	
TX+	1
TX-	2
RX+	3
N.C.	4
N.C.	5
RX-	6
N.C.	7
N.C.	8

Top View



B.10 J12 – MEZZANINE PCI CONNECTOR

	A	B	Top View	C	D	
1	5V_KEY	Reserved		VCC	AD00	1
2	VI/O (5V)	AD02		AD01	+5V	2
3	AD05	GND		AD04	AD03	3
4	C/BE0#	AD07		GND	AD06	4
5	GND	AD09		AD08	GND	5
6	AD11	VI/O (5V)		AD10	MM66EN	6
7	AD14	AD13		GND	AD12	7
8	+3.3V	C/BE1#		AD15	+3.3V	8
9	SERR#	GND		SB0#	PAR	9
10	GND	PERR#		+3.3V	SDONE	10
11	STOP#	+3.3V		LOCK#	GND	11
12	+3.3V	TRDY#		GND	DEVSEL#	12
13	FRAME#	GND		IRDY#	+3.3V	13
14	GND	AD16		+3.3V	C/BE2#	14
15	AD18	+3.3V		AD17	GND	15
16	AD21	AD20		GND	AD19	16
17	+3.3V	AD23		AD22	+3.3V	17
18	IDSEL0	GND		IDSEL1	IDSEL2	18
19	AD24	C/BE3#		VI/O (5V)	IDSEL3	19
20	GND	AD26		AD25	GND	20
21	AD29	VCC		AD28	AD27	21
22	VCC	AD30		GND	AD31	22
23	REQ0#	GND		REQ1#	VI/O (5V)	23
24	GND	REQ2#		VCC	GNT0#	24
25	GNT1#	VI/O (3V)		GNT2#	GND	25
26	VCC	CLK0		GND	CLK1	26
27	CLK	VCC		CLK3	GND	27
28	GND	INTD#		VCC	RST#	28
29	+12V	INTA#		INTB#	INTC#	29
30	-12V	Reserved		Reserved	3.3V_KEY	30



Active Low Signal

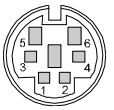
B.11 J13 - COMPACTFLASH DISK CONNECTOR

Pin Number		Top View		Pin Number	
Signal					Signal
D11	1	1	2	2	GND
D12	3			4	D3
D13	5			6	D4
D14	7			8	D5
D15	9			10	D6
CS1#	11			12	D7
DMACK#	13			14	CS0#
DMARQ#	15			16	IOR#
PDIAG#	17			18	IOW#
IRQ15	19			20	VCC
VCC	21			22	VCC
GND	23			24	GND
RESET#	25			26	GND
CSEL	27			28	A2
A01	29			30	DASP#
A0	31			32	IORDY
D0	33			34	D8
D1	35			36	D9
D2	37	39	40	38	D10
IOCS16#	39			40	GND

B.12 J18 – KEYBOARD AND MOUSE PS/2 CONNECTOR

Signal	
KB:DATA	1
MOUSE:DATA	2
GND	3
VCC	4
KB:CLK	5
MOUSE:CLK	6

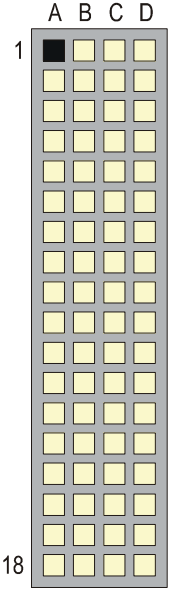
Front View



B.13 J19 – MEZZANINE STORAGE CONNECTOR

	A	B	C	D	
1	VCC	VCC	VCC	VCC	1
2	VCC	VCC	VCC	D0	2
3	MOUSE:CLK	MOUSE:DATA	D1	D2	3
4	KB:DATA	KB:CLK	D3	D4	4
5	KB:VCC	GND	D5	D6	5
6	GND	GND	D7	D8	6
7	GND	GND	D9	D10	7
8	GND	GND	D11	D12	8
9	GND	GND	D13	D14	9
10	FD:DS1#	FD-DRVEN0#	D15	BRSTDRV#	10
11	FD:DRVEN1#	FD-MTR1#	IOW#	REQ	11
12	FD:INDEX#	FD-DS0#	IORDY0	IOR#	12
13	FD:DSKCHG#	FDET	IRQ14	DACK#	13
14	FD:MTR0#	FD-DIR#	A0	A1	14
15	FD:STEP#	FD-WDATA#	A2	GND	15
16	FD:GATE#	FD-TRK0#	IDE:ACT#	CS1#	16
17	FD:WRPROT#	FD-RDATA#	CS3#	DIAG#	17
18	F:-HSEL#	+12V	IOCS16#	+12V	18

Top View

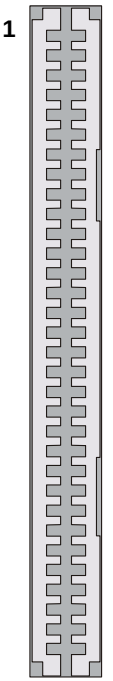


Active Low Signal

B.14 J20 PMC CONNECTOR

Pin Number		Pin Number	
Signal			**Signal**
N.C.	1	2	-12V
GND	3	4	INTA#
INTB#	5	6	INTC#
BUSMODE1#	7	8	VCC
INTD#	9	10	N.C.
GND	11	12	N.C.
PCLK-PMC	13	14	GND
GND	15	16	GNT-PMC#
REQ-PMC#	17	18	VCC
VCC	19	20	AD31
AD28	21	22	AD27
AD25	23	24	GND
GND	25	26	C/BE3#
AD22	27	28	AD21
AD19	29	30	VCC
VCC	31	32	AD17
FRAME#	33	34	GND
GND	35	36	IRDY#
DEVSEL#	37	38	VCC
GND	39	40	LOCK#
PMC-SDONE#	41	42	PMC-SB0#
PAR	43	44	GND
VCC	45	46	AD15
AD12	47	48	AD11
AD9	49	50	VCC
GND	51	52	C/BE0#
AD6	53	54	AD5
AD4	55	56	GND
VCC	57	58	AD3
AD2	59	60	AD1
AD0	61	62	VCC
GND	63	64	N.C.

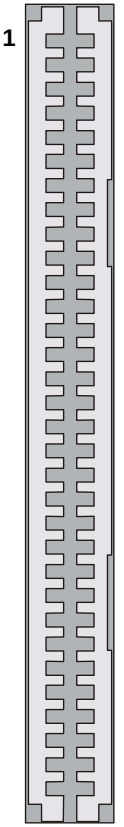
Top View



B.15 J21 PMC CONNECTOR

Pin Number	Signal
1	+12V
3	N.C.
5	N.C.
7	GND
9	N.C.
11	BUSMODE2
13	PCI RST
15	VCC
17	N.C.
19	AD30
21	GND
23	AD24
25	IDSEL_PMC
27	VCC
29	AD18
31	AD16
33	GND
35	TRDY
37	GND
39	PERR
41	VCC
43	C/BE1
45	AD14
47	GND
49	AD8
51	AD7
53	VCC
55	N.C.
57	N.C.
59	GND
61	N.C.
63	GND

Top View

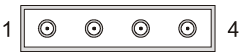


Pin Number	Signal
2	N.C.
4	N.C.
6	GND
8	N.C.
10	N.C.
12	VCC
14	BUSMODE3
16	BUSMODE4
18	GND
20	AD29
22	AD26
24	VCC
26	AD23
28	AD20
30	GND
32	C/BE2
34	N.C.
36	VCC
38	STOP
40	GND
42	SERR
44	GND
46	AD13
48	AD10
50	VCC
52	N.C.
54	N.C.
56	GND
58	N.C.
60	N.C.
62	VCC
64	N.C.

B.16 B1 - BATTERY HEADER

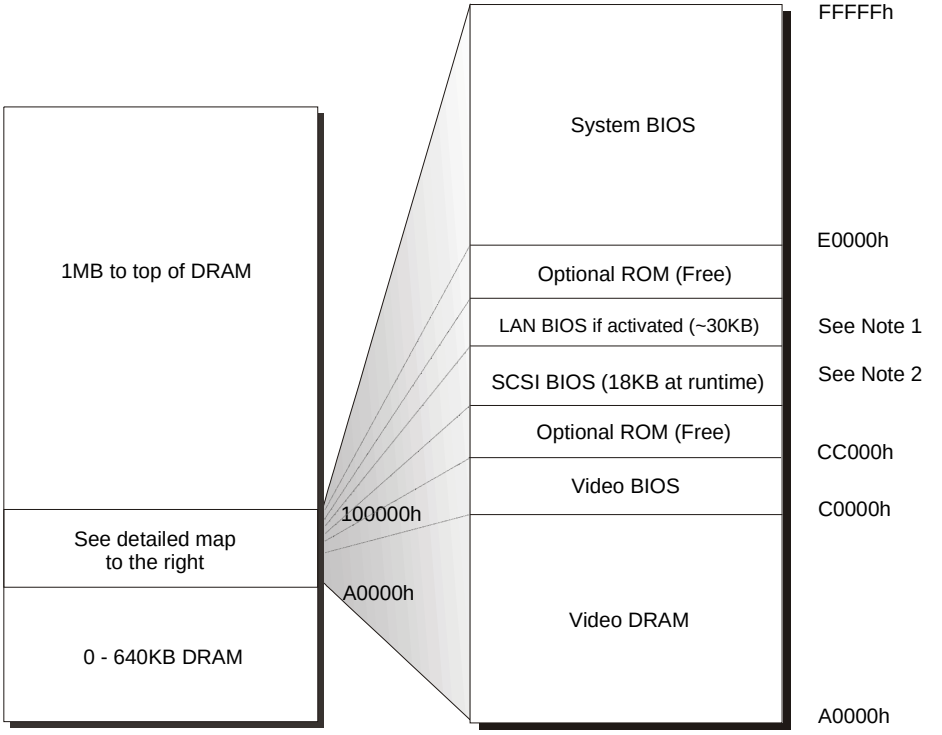
Signal	Pin
Battery (+)	1
Battery (-)	2

Top View



C. MEMORY & I/O MAPS

C.1 MEMORY MAPPING



Note 1 : LAN BIOS address may vary

Note 2 : SCSI BIOS address may vary.
Size is only 2KB if no device.

Address	Function
00000-9FFFF	0-640 KB DRAM
A0000-BFFFF	Video DRAM
C0000-CBFFF	Video BIOS
CC000-DFFFF	Optional ROM (Free)
	LAN BIOS around 30KB if activated, address may vary
	SCSI BIOS 18KB at runtime, 2KB if no device, address may vary
E0000-FFFFF	System BIOS
100000-Top of DRAM	1 MB - Top of DRAM

C.2 I/O MAPPING

Address	Optional Address	Optional Address	Optional Address	Function
000-01F				DMA Controller 1
020-03F				Interrupt Controller 1
040-05F				Timer
060-06F				Keyboard
070-07F				Real-time clock
080-09F				DMA Page Register
0A0-0BF				Interrupt Controller 2
0C0-0DF				DMA Controller 2
0F0-0F1, 0F8-0FF				Math Coprocessor
x90-x9F				Kontron Control Port
1F0-1F7, 3F6				Primary IDE
3F0-3F7	370-377			Floppy Disk
378-37A	3BC-3BE	2787-27A		Parallel Port (LPT1 by default)
3F8-3FF (COM1)	2F8-2FF (COM2)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 2 (COM2 by default)
3C0-3CF, 3D0-3DF, 3B0-3BB				Graphics Controller (I2C Port)

D. IRQ AND DMA LINES

D.1 IRQ LINES

The board is fully PC compatible with interrupt steering for PCI plug and play compatibility.

Controller # 1		Controller # 2	
IRQ 0	Timer Output 0	IRQ 8	Real-Time Clock
IRQ 1	Keyboard	IRQ 9	Available [1]
IRQ 2	Cascade Controller # 2	IRQ 10	Available [1]
IRQ 3*	Serial Port 2	IRQ 11	Available [1]
IRQ 4*	Serial Port 1	IRQ 12	PS/2 Mouse
IRQ 5*	Available [1]	IRQ 13	Coprocessor Error
IRQ 6*	Floppy Controller	IRQ 14	Primary IDE or available [1]
IRQ 7*	Parallel Port 1 or Available	IRQ 15	N/C

* :All functions marked with an asterisk (*) can be disabled or reconfigured.

1 Available lines service on board and external PCI/ISA PnP devices or a Legacy ISA device.

D.2 DMA CHANNELS

The cPCI-MXP64 integrates the functionality of two 8237 DMA controllers. Eight DMA channels are available.

According to Plug and Play standards, the system BIOS automatically allocates DMA Channel 1 or 3 for the parallel port's ECP mode. Channel 2 is reserved for the floppy controller and Channel 4 is used to cascade Channels 0 through 7 to the microprocessor.

DMA Channel	Function
DMA 0	Available
DMA 1	PnP available (ECP)
DMA 2	Floppy controller
DMA 3	PnP available (ECP)
DMA 4	Cascade controller # 1
DMA 5	PnP available
DMA 6	PnP available
DMA 7	PnP available

E. BIOS SETUP ERROR CODES

E.1 POST BEEP

POST beep codes are defined in the BIOS to provide low level tone indication when an error occurs during the BIOS initialization.

Beep codes consist of a combination of long and short beeps. They are described as follows:

Beep Codes

Post code	Beep Code	Description
41	**-*	Enterring the boot block recovery code (i.e. Main BIOS checksum error)
22	*-*-*	Error when getting the boot block flash ID code
33	*-*-*-*	Error when erasing the boot block flash
44	*-*-*-*-*	Error when programming the boot block flash
55	*-*	Success of the boot block recovery code. The board is ready to be manually reset.

Legend * = 1 Short beep code, ** = 1 Long beep code, - = Silence

E.2 POST MESSAGES

During the Power On Self Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

"PRESS F1 TO CONTINUE, DEL TO ENTER SETUP".

E.3 ERROR MESSAGES

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

CMOS BATTERY HAS FAILED

1. If it's the first boot, check for the onboard battery jumper W4. The board is shipped with W4 jumper set to OFF (onboard battery disconnected). This jumper must be shorted (ON) for proper battery operation.

2. CMOS battery is no longer functional. It should be replaced.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This indicates that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Floppy Drive A and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.
If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause BIOS to ignore the missing keyboard and continue the boot.

OFFENDING SEGMENT

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a Non Maskable Interrupt condition, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

E.4 POST CODES

POST #	Designation	Description
01	BOOT BLOCK	Boot Block in EMERGENCY : Clear Base Memory Area.
03	Initialize Chips	1. Clear CMOS shutdown byte. 2. Initialize EISA extended registers. (Not for us since we don't have EISA bus.)
04	Test Memory Refresh Toggle	RAM must be periodically refreshed in order to keep the memory from decaying.
05	Blank Video, Initialize Keyboard	1. Clear CMOS reset status byte. 2. Early Keyboard initialization. Boot Block in EMERGENCY: Initialize Keyboard Controller.
06	EPROM Checksum	1. Test F000h segment shadow readable and writeable for POST access correct. If not, show POST FE and beep continuously… 2. Autodetect Flash EPROM.
07	Test CMOS Interface and Battery Status	1. Install the Kontron segment. 2. Verifies CMOS is working correctly (walking bit test). 3. Restore CMOS from Flash if option is enabled. 4. Check for OVERRIDE KEY (INSERT key).
08	Program Chipset default	Program Chipset default (show POST BEh).
09	Early Cache Initialization	1. Check for Intel's and/or Cyrix CPU. 2. Early Cache Initialization when cache is separate from chipset. 3. Turn off Gate A20.
0A	Setup Interrupt Vector Table	1. Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize int. 00h-1Fh according to INT_TBL. 2. Early Power Management Initialization.
0B	Test CMOS RAM Checksum	1. Verify time and date for valid values. 2. If Override enabled, check for Override key. If Override key pressed, Kill CMOS checksum. 3. Check CMOS Battery (useless if save CMOS in FLASH enabled since it's already done). 4. Verify Checksum, if bad, load defaults. 5. Copy CMOS in the stack. 6. Clear CMOS Alarm date. 7. Clear HD if Hidden. 8. Clear Floppy "B" if only one drive. 9. Detect for a Math Co-processor. 10. Set Fast Gate A20 Flag in CMOS. 11. If "B" drive only is set the 2 Drive are set… 12. Program Chipset for early Power Management. 13. P6 Bios Update (if applicable). *14. Kill Onboard PnP IO.* *15. PnP Early Initialization.* *16. PnP System Resource:* *1. Get ESCD.* *2. Create default SYSTEM_MAP.* *3. Decode/Record ISA ESCD resources.* *4. Record I/O port for PnP operation.* 17. Chipset Early Shadow.

POST Codes (continued)

POST #	Designation	Description	
0C	Initialize Keyboard	1. Open Xilinx I/O Port location to x90h (X=1,2 or 3) inside the chipset (if necessary).	Boot Block 1st : Verify BIOS checksum.
		2. Disable (if necessary). Thermal Management. 3. Disable (if necessary) Ethernet Chip.Set IDE Detect counter to 0. 4. Set CD-ROM found variable to 0. 5. Initialize zone 40:0h for the keyboard buffer.	Boot Block in EMERGENCY 2nd : Init. vector 00h through 77h.
0D	Initialize Video Interface & Chipset	*1. On M1 set the cache for the memory installed.* *2. On PCI, do a PCI ROM init.* 3. On P6, Init. Apic. 4. Init. Chipset. 5. Turn ON CPU Cache. 6. Set Maximum Speed. 7. Measure CPU Clock Speed. 8. Restore Speed. 9. Turn Off CPU Cache. 10. Early Video Shadow. 11. Read CMOS location 14h to find out type of video to use. Detect and initialize Video Adapter. 12. Init. T380 if necessary.	Boot Block in EMERGENCY: Try to init. Video Card…
0E	Test Video Memory	1. If CGA or MONO, test video memory. 2. Beep the speaker. 3. Show the LOGO. 4. Install VT100 driver if necessary. 5. Write sign-on message to screen. 6. Write Copyright message to screen. 7. Write Evaluation message to screen. 8. Show CPU type and speed.	
0F	Test DMA Controller 0	Test DMA Controller 0.	
10	Test DMA Controller 1	Test DMA Controller 1.	
11	Test DMA Page Registers	Test DMA Page Registers.	
12	Reserved	Reserved for 8254 Counter 0 - Not implemented.	
13	Reserved	Reserved for 8254 Counter 1 - Not implemented.	
14	Test Timer Counter 2	Test 8254 Timer 0 Counter 2.	
15	PIC Test 8259-1 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	
16	PIC Test 8259-2 mask bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.	

POST Codes (continued)

POST #	Designation	Description
17	Test Struck 8259's Interrupt Bits	Nothing
18	Test 8259 Interrupt functionality	Force an interrupt and verify that the interrupt occurred (IRQ 0 - clock int. 8h).
19	Test Struck NMI Bits (Parity/ IO check)	Nothing.
1A-1E	Reserved	Reserved
1F	Set EISA Mode	If EISA non-volatile memory checksum is good, execute EISA initialization. If no, execute ISA test and clear EISA mode flag. Test EISA Configuration Memory integrity (checksum & communication interface).
20-2F	Enable Slots 0-15	Initialize slot 0 (System Board) to slot 15.
30	Size Base & Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB.
31	Test Base & Extended Memory	1. Test base memory from 256K to 640K and extended memory above 1MB using various patterns. 2. The last test is filling memory with 0's. 3. On a quick memory test or if user press the ESC key while testing memory, only the last test is performed.
32	Test EISA Extended Memory	If EISA Mode flag is set, then test EISA memory found in slots Initialization. NOTE 1: This will be skipped in ISA mode. NOTE 2: This POST also Detect & Report I/O PORTS and also Init. Super IO.
33-3C	Reserved	Reserved
3C	Setup Enable	
3D	Initialize & Install PS/2 Mouse	Detect if mouse is present. Initialize mouse. Install interrupt vector.
3E	Setup Cache Controller	Initialize cache controller.
3F-40	Reserved	Reserved
41	Initialize Floppy Drive & Controller	1. Verify if we should enter setup. If so, enter setup. 2. Initialize floppy disk drive controller and any drive. Boot Block in EMERGENCY: Scan for Floppy for emergency disk…
42	Initialize Hard Drive & Controller	Initialize hard drive controller and any drive. (Call HD_INSTALL).
43	Detect & Initialize Serial/Parallel/Joystick ports	Initialize any serial, parallel and game ports.
44	Reserved	Reserved
45	Detect & Initialize Math Coprocessor	Initialize Math Coprocessor.
46	Reserved	Reserved
47	Set Speed for Boot	Set Speed for Boot.
48-4C	Reserved	Reserved
4D	Init. PC-Speaker to LINE OUT	Enable access to PC-Speaker to LINE OUT and Enable/Disable it. (T934).
4^E	Manufacturing POST Loop or display Messages	1. Reboot if Manufacturing POST Loop pin is set. 2. Otherwise display any messages (i.e., any non-fatal errors that were detected during POST). 3. Enter SETUP if needed.

POST Codes (continued)

POST #	Designation	Description
4F	Security Check	*Ask password security if needed.*
50	Write CMOS	Write all CMOS values back to CMOS-RAM and clear screen.
51	Pre-Boot Enable	1. Enable Parity checker. 2. Enable NMI. 3. Enable cache before boot.
52	Initialize Option (ROM scan)	1. Call POST 81 2. Initialize any ROMs present from C8000h to DBFFFh. Disable POST code from segment E0000h. 3. Initialize any ROMs present from DC000h to E0800h. NOTE: When FSCAN option is enabled, will initialize from C8000h to F7FFFh.
53	Initialize Time Value	Initialize Time value in 40h: BIOS area.
54-5F	Reserved	Reserved
60		Store boot partition of head & cylinder.
61	Final Init	*For last µs detail before boot.*
62	Num Lock ON	Put Num Lock ON and Daylight Saving.
63	Boot Attempt	1. Call POST 82. 2. Set Low stack. 3. Boot via int 19h.
64-7F	Reserved	Reserved
80	Kontron Segment Move 1	Install the Kontron segment from Flash to DC00:0h.
81	Kontron Segment Move 2	Install the Kontron segment from DC00:0h to 7000:0h.
82	Kontron Segment Move 3	Install the Kontron segment from 7000:0h to EC00:0h.
83	Check & Program CPLD	Check & Program CPLD for valid UserCode & IDCode.
84	Kontron CRC Check	Check if Kontron block have a valid CRC. If not, the Emergency procedure is launched.
85-AF	Reserved	Reserved
B0	Spurious	If interrupt occurs in protected mode.
B1	Unclaimed NMI	If unmasked NMI occurs, display: Press F1 to disable NMI, F2 reboot.
B2-BD	Reserved	Reserved
BE	Early Prog Chipset Def.	Going to early program chipset to default values (called from POST_8s).
BF	Program Chip Set	Called early at POST 0Dh to program chipset from CT-TABLE.
C0	Turn ON/OFF Cache	OEM Specific - Cache control. / Boot Block: First POST.
C1	Memory presence	OEM Specific - Test to size on-board memory test. / Boot Block: Search for Boot Block Signature "*BBSS*".
C2	Early Memory Initialization	OEM Specific - Board Initialization.
C3	Extended Memory Initialization	OEM Specific - Turn ON extended memory DRAM select. / Boot Block: Expand compressed BIOS
C4	Special Display Switch Handling	OEM Specific - Display/Video switch handling so that display switch errors never occur.

POST Codes (continued)

POST #	Designation	Description	
C5	Early Shadow	OEM Specific - Early Shadow enable for fast boot.	Boot Block: Early Shadow System BIOS.
C6	Cache Programming	OEM Specific - Routine for programming which region are cacheable.	Boot Block: Cache Sizing
C7	Reserved	Reserved	
C8	Special Speed Switching	OEM Specific - Routine to handle speed switching.	
C9	Special Shadow Handling	OEM Specific - Normal Shadow routine.	
CA	Very Early Initialization	OEM Specific – Initialize hardware before any other hardware initialization.	
CB-CF	Reserved	Reserved	
D0	Power Management Full speed	Trying to go back or into full speed mode.	
D1	Power Management -- Doze mode	Trying to go or in Doze mode.	
D2	Power Management --Sleep mode	Trying to go or in Sleep mode.	
D3	Power Management – Suspend mode	Trying to go or in Suspend mode.	
D4-DF	Debug	Available POST codes for use by source code customers during development.	
E0	Reserved	Reserved	
E1-EE	Setup Page	Page 1 to Page 14	
EF	Shadow Error	In POST 6 to signal a Shadow Error.	
F0-FE	Reserved	Reserved	
FF	Boot	The system is now booted or waiting for an OS.	

F. EMERGENCY PROCEDURE

Symptoms:

- No POST code on a power up (when using a POST card).
- Board does not boot, even after usual hardware and connection verifications.
- At power up, there is floppy disk led activity, which is one sign that the BIOS as detected a corrupted BIOS CRC prior POST and falled back automatically to Emergency Recovery Mode looking for the floppy Emergency disk.

Please go on our FTP site in order to get the latest Emergency Recovery BIOS for that specific product.

BIOS maybe found at: Ftp://Ftp.Kontron.ca/Support/BIOS_Emergency/

Emergency Recovery Procedure is included within the Zip file of the Emergency BIOS to download. Latest Emergency Recovery procedure can be found on the FAQ section of the FTP site under FAQ # KC_0028 at location:

ftp://ftp.kontron.ca/Support/Support_FAQ - Questions & Answers/

G. GETTING HELP

At Kontron, we take great pride in our customer's successes. We strongly believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, you may contact our Technical Support department at:

CANADIAN HEADQUARTERS
Tel. (450) 437-5682
Fax: (450) 437-8053

If you have any questions about Kontron, our products or services, visit our Web site at : www.Kontron.com

You can also contact us at the following address:

Kontron inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

LIMITED WARRANTY

KONTRON INC, ("The seller") warrants its boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts, which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

Returning Defective Merchandise

If your Kontron product malfunctions, please do the following before returning any merchandise:

1) Call our Technical Support department in Canada at (450) 437-5682. Make certain you have the following at hand:

   - The Kontron Invoice number
   - Your purchase order number
   - The serial number of the defective board.

2) Give the serial number found on the back of the board and explain the nature of your problem to a service technician.

3) If the problem cannot be solved over the telephone, the technician will further instruct you on the return procedure.

4) Prior to returning any merchandise, make certain you receive an RMA number from Kontron's Technical Support and clearly mark this number on the outside of the package you are returning. To request a number, follow these steps:

   - Make a copy of the request form on the following page.
   - Fill out the form and be as specific as you can about the board's problem.
   - Fax it to us.

5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.

6) When returning a Kontron board:

   i) Make certain that the board is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.

   ii) Ship prepaid to (but not insured, since incoming units are insured by Kontron):

Kontron inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

RETURN TO MANUFACTURER AUTHORIZATION REQUEST

Contact Name : _____

Company Name : _____

Street Address : _____

City : _____ Province/State: _____

Country : _____ Postal/Zip Code: _____

Phone Number : _____ Extension : _____

Fax Number : _____

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

Fax this form to Kontron's Technical Support department in Canada at (450) 437-8053