PCI-990

Dual / Single Pentium III Processor and 64-bit bus

Technical Reference Manual
Version 1.4, February 2003

Note: The latest releases of the Technical Reference Manuals are available at:
ftp://ftp.kontron.ca/support/Product_manuals/

www.kontron.com

Ref. : M9005_TECH (Board Rev. 2)

FOREWORD

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Printed in Canada.

READ ME FIRST

Your computer board has a standard non-rechargeable lithium battery. To preserve the battery lifetime, **the battery enable jumper is not installed when you receive the board**. To enable the onboard battery, install jumper W3 to position 1-2 (see section 3.1, setting jumpers).

EXERCISE CAUTION WHILE REPLACING LITHIUM BATTERY

WARNING

Danger of explosion if battery is incorrectly replaced.

Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

ATTENTION

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie.

Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabriquant.

ACHTUNG

Explosionsgefahr bei falschem Batteriewechsel.

Verwenden Sie nur die empfohlenen Batterietypen des Herstellers. Entsorgen Sie die verbrauchten Batterien laut Gebrauchsanweisung des Herstellers.

ATENCION

Puede explotar si la pila no este bien reemplazada.

Solo reemplaza la pila con tipas equivalentes segun las instrucciones del manifacturo. Vote las pilas usadas segun las instrucciones del manifacturo.

POWERING-UP THE SYSTEM

If you should encounter a problem, verify the following items:

Make sure that all connectors are properly connected.

Verify your boot diskette.

If the system still does not start up properly, you should try booting your system with only the power cord and video monitor connected to the board; this is the minimum required to see if the board is working.

If you still are not able to start up your system, please refer to the emergency procedure in the Appendix Section.

If you still are not able to get your board up and running, contact our technical support department for assistance (see Appendix G)

ADAPTER CABLES

While adapter cables are provided from various sources, the pinout is often different. The direct crimp design offered by Kontron allows the simplest cable assembly. All cables are available from Kontron Sales Department. (see Appendix G)

UNPACKING AND SAFETY PRECAUTIONS

Static Electricity

Since static electricity can damage the board, the following precautions should be taken:

1. Keep the board in its antistatic package, until you are ready to install it.
2. Touch a grounded surface or wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
3. Handle the board by the edges.

Storage Environment

Electronic boards are sensitive devices. Do not handle or store devices near strong electrostatic, electromagnetic, magnetic or radioactive fields.

Power Supply

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.

Unpacking

Follow these recommendations while unpacking:

1. After opening the box, save it and the packing material for possible future shipment.
2. Remove the board from its antistatic wrapping and place it on a grounded surface.
3. Inspect the board for damage. If there is any damage, or items are missing, inform immediately Kontron (see Appendix G)

When unpacking you will find:

1. One PCI-990 Single Board Computer board.
2. One Quick Reference sheet
3. One CDROM containing drivers.

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APPENDICES

1 PRODUCT OVERVIEW

1. INTRODUCTION
2. PRODUCT SPECIFICATIONS

1.1 Introduction

The state-of-the-art dual CPU PCI/ISA Single Board Computer that packs new high power with two Intel® Pentium® III processors providing speed, performance, reliability and flexibility.

The Kontron PCI-990 is designed to accommodate the endless demands for a high performance engine in platforms used in the embedded datacom/telecom market. An ideal SBC for high performance Internet security and data center solutions, as well as mission-critical CTI and demanding embedded computing applications. Kontron has developed this SBC that fits perfectly into its 1U, 2U and 6U chassis such as the Kontron DreamSpeed and CoreVox families of platforms.

Key Features:

- Single/Dual Intel® processors:
  - 733 MHz, 866 MHz, 1.0GHz Pentium® III with 256KB L2 cache
  - 1.26GHz Pentium® III-S with 512KB L2 cache
  - 800MHz Low-Power Pentium III with 512KB L2 cache
- 133MHz front-side bus
- Up to 4GB of PC133 Registered SDRAM
- 64-bit backplane PCI bus
- Choice of Dual Ethernet ports:

  10/100Base-TX or

  1000Base (T or S/LX) based on Intel® 82544 Ethernet controller with copper- or optic-type interface available (only with Kontron's custom-built mezzanine)
- Dual-channel Ultra160 SCSI LVDS/SE (optional)
- Two EIDE hard disk interfaces
- Three USB ports
- Watchdog Timer
- Board and CPU temperature monitoring

1.2 Product Specifications

This board introduces the Serverworks Serverset LE III chipset, 64-bit PCI support (additional card edge connector), and registered SDRAM memory. Besides the usual basic I/O's (serial ports, IDE, etc.), this SBC offers optional dual Gigabit Ethernet or dual 10Base-T/100BaseTX Ethernet.

PCI-990 Technical Specification Sheet	
Features	**Description**
CPU	▸ PCI-990 : Dual Pentium III processor (FC-PGA) at 733MHz, 866MHz, 1.0GHz ; (FC-PGA2) at 1.26GHz and (custom adapter) 800MHz
Cache	▸ 16K/16K Instruction / Data CPU-internal Level 1 ▸ 256/512KB 64-bit wide on-die Level 2 Advanced Transfer Cache
Chipset	▸ Serverworks ServerSet III LE chipset (CNB30LE north bridge & OSB4 south bridge)
Bus Interfaces	▸ Front side bus at 133MHz ▸ PCI Bus (External 64 bit, Internal 64bit/66MHz for Gigabit, SCSI and PCI bridge, Internal 32 bit for Fast Ethernet South bridge and Video) ▸ ISA Bus (8.33MHz)
Memory	▸ Four 184-pin latching DIMM sockets, 64/72-bit ▸ Up to 4 GB of PC-133 Registered SDRAM, non-ECC/ECC mode (single bit error correction, multiple bit detection via Serverworks ServerSet III LE); all 4 GB cacheable (per CPU)
Data Path	▸ 64-bit on CPU; 32-bit and 64-bit on PCI busses, 16-bit on ISA bus
DMA Channels (ISA)	▸ Four 8-bit, three 16-bit ▸ Supports scatter / gather, Fast Type-F DMA
Interrupts	▸ 11 edge/level sensitive and software configurable ▸ 4 PCI level sensitive, configurable to any interrupt vector for PnP compatibility (DOS mode) ▸ All ISA onboard interrupts are PnP compliant
Flash Memory	▸ 512KB for BIOS field upgrade ▸ 32Kb user serial EEPROM

PCI-990 Technical Specification Sheet (cont'd)	
Features	**Description**
I/O	▸ SMSC LPC37B787 super I/O ▸ USB Ports : Three (USB 1.1 compliant) ▸ Serial Ports: Two (one RS-232 COM1, COM2 configurable as RS-232/422/485 ▸ Parallel Port : One bi-directional with all IEEE 1284 protocols supported with BIOS selectable IRQs and addressing ▸ Hard Disk : PCI EIDE Ultra DMA/33, support for four IDE drives in a master/slave configuration, PIO Mode4, Bus Master IDE or synchronous DMA mode transfers up to 33MB/s ▸ SCSI Dual-channel Ultra160 SCSI LVDS/SE (optional) ▸ Floppy Disk: Support for two drives ▸ Ethernet: • Two Ethernet, PCI 10/100Base-TX ports Intel 82559ER controllers) or • Two Intel 82544GC Gigabit Ethernet (two RJ-45 for copper; two MT-RJ SX duplex transceiver for fiber), available on mezzanine only
Video	▸ PCI video controller (Intel 69000) with 2MB on chip video memory ▸ Supports CRT with resolution up to 1280 x 1024
Clock/Calendar	▸ Real-time clock with 256 bytes of battery backup CMOS RAM
Connectors	**I/O bracket** (mounted connectors) ▸ Video (female DB-15) ▸ Ethernet: • Fast Ethernet (two RJ-45 with embedded link/activity LED's) or • Gigabit Ethernet (two RJ-45 for copper; two MT-RJ SX duplex transceiver for fiber) with link activity indicators ▸ USB port (one 4-pin USB connector)

PCI-990 Technical Specification Sheet (cont'd)	
Features	**Description**
Connectors (cont'd)	**Headers** 3-pin locking : CPU fans (2) 10-pin header : USB (1) 10-pin shrouded : Serial ports (2) 16-pin shrouded : AT keyboard, speaker, PS/2 mouse, reset, EIDE & SCSI activity LED 20-pin : ATX power supply connector (1) 20-pin shrouded : System monitor (1) 26-pin shrouded : Parallel port (1) 34-pin shrouded : Floppy (1) 40-pin shrouded : EIDE (2) 40-pin module : CompactFlash module (1) 68-pin High Density DB68 : SCSI (2) **Other** ▸ CPU module (two 370-pin PGA sockets) ▸ ISA (standard ISA edge connector) ▸ PCI (64-bit PICMG 1.0 PCI edge connector) ▸ SDRAM (4 vertical DIMM sockets)
BIOS Features	▸ Phoenix BIOS in Flash with recovery code. ▸ Save CMOS in Flash option and Boot from LAN capability. ▸ CC000-E0000 address blocking; PnP tables ▸ Setup console redirection to serial port (VT100 mode) with CMOS setup access ▸ All onboard peripherals can be enabled or disabled by software ▸ Diskless, keyboardless, and videoless operation extensions ▸ System, video and LAN BIOS shadowing ▸ Programmable I/O wait states ▸ Advanced security feature for floppy and HDD; DMI & HDD S.M.A.R.T. support ▸ Advanced Configuration and Power Interface (ACPI 1.0), **not included in BIOS version 1.5** Intelligent System Monitoring (chassis intrusion and advanced thermal management such as resume, overheat alarm and auto slow down)

PCI-990 Technical Specification Sheet (cont'd)	
Features	**Description**
Supervisory	▸ **Software monitor** • Two-stage software programmable watchdog timer, time out from 16msec to 4.5 min • Silicon Serial ID TAG for unique board identification accessible via software ▸ **Hardware system monitor** • Power failure detector • Low battery voltage detector • CPU temperature sensor / thermal management • Board temperature sensor • 12V, 5V, 3.3Vand Vcore voltage supervisor • 2 chassis error inputs accessible via software. • 1 chassis error outputs accessible through software • 6 chassis fan tachometric inputs accessible by software and with SMI generation capabilities • Chassis intrusion input with onboard battery backup accessible by software and SMI generation capability
OS Compatibility	• MS-DOS 6.22 • Microsoft Windows NT 4.0 • Microsoft Windows 98 SE • Microsoft Windows ME • Microsoft Windows XP Pro • Microsoft Windows 2000 Professional • Microsoft Windows 2000 Server • Linux • QNX RTP 6.1.0 • BSD • UNIX

PCI-990 Technical Specification Sheet (cont'd)	
Features	**Description**
PICMG compliance	▸ **Mechanical** • PICMG 1.0 Rev. 2.0
Mechanical	▸ 338 x 122 x 40 mm / 13.33 x 4.80 x 1.85 in. at CPU / fan ▸ Conforms to IEEE P996 PC/AT bus, PCI Rev. 2.1, and PICMG 1.0 Rev. 2.0 specifications
Power Requirements	▸ **Supply Voltage Vcc** • +3.3V ±5% • +5V ±5% • +12V ±5% ▸ **Current dissipation** • ICC typ.* +5V: 11.4A • ICC typ.* +3.3V: 6.6A • ICC max* +5V: 12.2A * Measured with dual CPU Tualatin 1.266 GHz, video, 2 x Gigabit Ethernet, 512MB RSDRAM, keyboard and hard disk
Environmental	**Operating** / **Storage and Transit** Temp.: 0-50°C/32-122°F (w/100LFM airflow) / -40 to +70°C/-40° to 158°F Humidity: 5% to 95% @ 40°C/104°F non-condensing / 5% to 95% @ 40°C/104°F non-condensing Altitude: 4,572m / 15,000ft / 15,240m / 50,000ft Shock: 15G, each axis / 30G Vibration: 1G, each axis / 2G
MTBF	151 130 hours (Dual CPU Tualatin 1.266GHz, SCSI, Dual Gigabit 1000 Base-TX)
Reliability	Unique silicon serial number accessible via software ▸ USB, keyboard, mouse voltage protected by self-resetting fuses ▸ 2 year limited warranty
Safety	▸ Designed to meet or exceed UL 1950; CSA C22.2 No 950; EN 60950; IEC950
EMI/EMC	▸ FCC 47 CFR Part 15/CISPR22, Class B; CE Mark to EN55022/EN55024

PART 2

2 FEATURE DESCRIPTION

1. BLOC DIAGRAM
2. SYSTEM CORE
3. ETHERNET
4. I/O DEVICES
5. PARALLEL PORT
6. POWER SUPPLY
7. SERIAL PORTS
8. STORAGE DEVICES
9. USB PORTS
10. VIDEO FEATURES

2.1 Feature Description

2.1.1 PCI-990 Block Diagram

The PCI-990 introduces the Serverworks ServerSet III LE chipset.

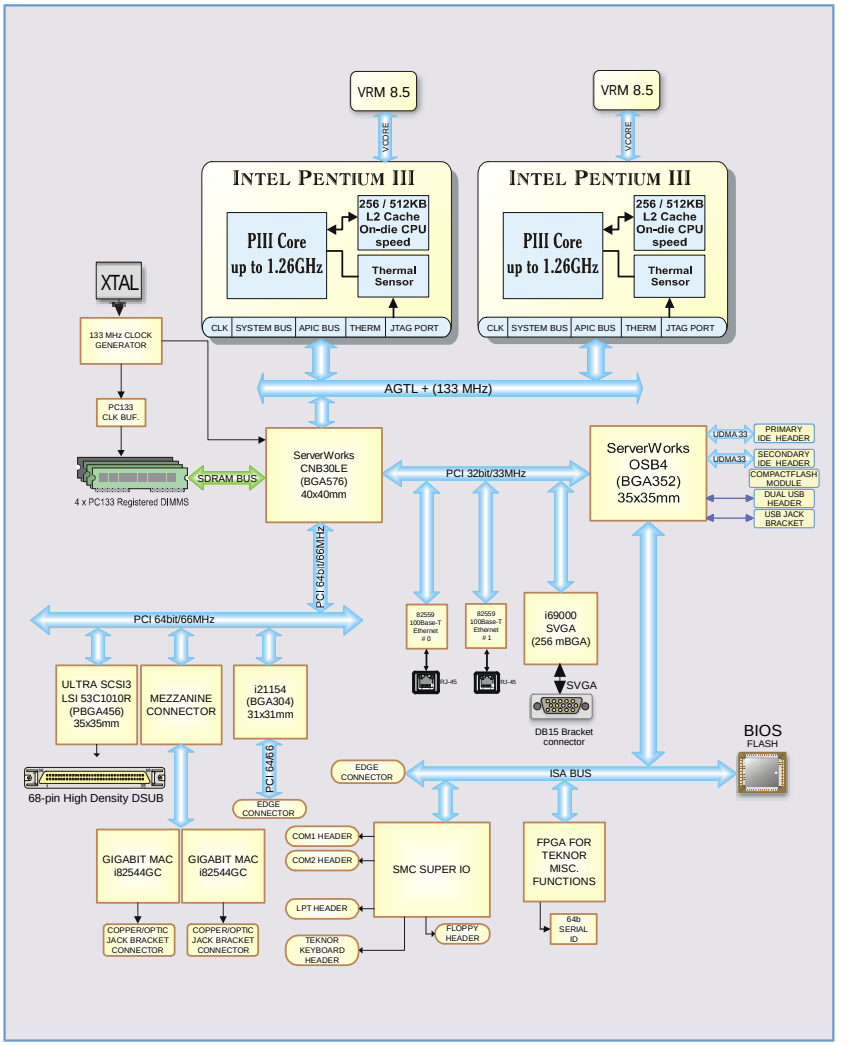

Figure 1

2.2 System Core

2.2.1 Processors

The following processor can be installed on the PCI-990

Pentium III Processor 733 MHz, 866 MHz, 1.0GHz, 1.26GHz as well as 800MHz Low-Power and future processors as technology evolves.

Related Jumpers
None

BIOS Setups
None

The fan connectors J25 for CPU2 and J26 for CPU1 provide the power voltage (+12V) for the CPU fan assemblies.

NOTE

When the board is configured for single processor operation, the CPU2 socket must be terminated with a terminator module

2.2.2 Memory

The board supports up to 4 Gigabytes of 64/72-bit PC133 Registered SDRAM (RSDRAM)

Related Jumpers
None

BIOS Setups
See 4.1.2.4 – *Phoenix Setup Program, Main Menu Selection*

NOTE

The total size of the system memory available on the board is equal to the sum of the memory module sizes installed in the SDRAM sockets. But if 4GB of memory is installed the extended memory size is 4GB minus the reserved memory space for memory mapped device.

The PCI-990 supports the industry standard 168-pin DIMM (Dual In-Line Memory Module) sockets for memory configuration from 128MB to 4GB of Synchronous DRAM.

The memory characteristics must conform to the following:

- Standard 3.3V only,
- 64-bit and 72-bit modules, single-sided or double-sided
- Serial Presence Detect (SPD) EEPROM,
- Optional Error Checking and Correction (ECC) capabilities or parity bit with 72-bit modules,
- Compliant with Intel's PC133 SDRAM Specification (133MHz) Rev. 1.7.

For the latest list of tested DIMMs devices please consult our FTP site at :
ftp://ftp.kontron.ca/Support/Product_Memory_AVL_Approved%20Vendor%20List/

2.2.2.1 DIMM Installation

To install the DIMMs in the sockets, proceed as follows:

1. With the board flat on the table, turn it so that the faceplate is facing you.
2. Hold the module vertically so that the bottom connector key is at right. Install the DIMM straight down into the DIMM socket. The socket's keys will ensure a correct mating.
3. Press firmly on the top edge of the memory module to engage it into the socket. The module is fully inserted when the retaining clips snap into notches located at each end of the module.

If necessary, work your way by inserting the other modules, one by one.

To remove the DIMMs from the sockets, pull on the retaining clip located on one side of the socket. Once the module has snapped out, pull gently on it.

2.2.3 Battery

The battery is required to keep the BIOS settings and the real-time clock stored into the CMOS RAM. The board is shipped from factory with the battery electrically disconnected from the board. Before powering the board, the battery must be connected using the W3 CMOS backup jumper.

Related Jumpers

W3: Internal CMOS backup connection
Setups are described in Section 3.1– *Setting Jumpers*

BIOS Settings

Monitoring option are available.
See sections 4.1.2.6.1.2 - Hardware Monitor Voltage Input and 4.1.2.6.1.4 - Control Voltage Events

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The battery specifications are as follows: 3.6V Lithium battery, 0.37A/h

Installation

- Connect the battery to the BT1 header. The positive pin of the battery is located at the center.
- The jumper W3 must be in position 1-2 to enable the onboard battery.

2.3 Ethernet

The Fast Ethernet interfaces are available through the RJ-45 connectors located on the edge bracket (LAN 0 : J17 on the SBC or J1/2 on the mezzanine, LAN 1 : J16 on the SBC and J3/4 on the mezzanine).

The 10Mbps or 100Mbps (10Base-T, 100Base-Tx) network speed is automatically detected and selected.

The two Gigabit Ethernet are available on the mezzanine board through J1 and J3 (RJ-45) for copper or through J2 and J4 (MT-RJ SX duplex transceiver) for fiber.

Related Jumpers

None

BIOS Settings

The onboard Ethernet feature is enabled by default.
To change settings, see Section 0 - Ethernet Controller Configuration.

The 10Base-T interface uses UTP (Unshielded Twisted Pair) cables, category 5, 4 or 3 (5 is better) while the 100Base-TX and 1000Base-T interfaces requires category 5 UTP cables.

NOTE

The Ethernet controller has specific drivers for various operating systems and software. To install these drivers, refer to the Utility CD containing the Ethernet drivers for your operating system (more detail in Section 4.3 *Installing Drivers*).

2.4 I/O Devices

2.4.1 I/O Connections

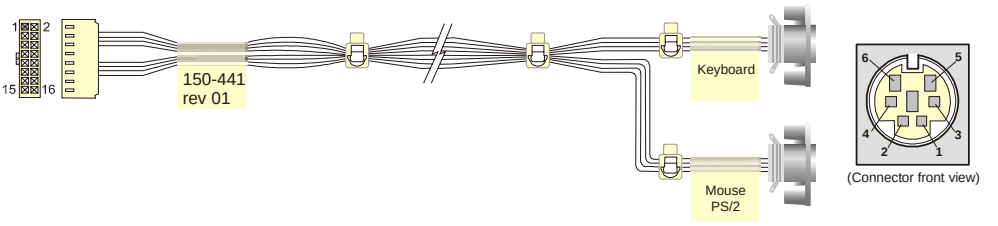
Standard AT keyboard, PS/2 Mouse, PC speaker port, reset button and hard disk LED signals are issued on the J15 multifunction header.

A 18” multifunction cable (Kontron part number 150-441-01) is provided with the board for connecting the respective devices.

Related Jumpers
None

BIOS Settings
None

Signals on the flat cable are issued as follows:



J15 Pinout description				
1	Keyboard Clock		2	GND
3	Keyboard Data		4	GND
5	VCC		6	VCC
7	Speaker		8	VCC
9	Mouse Clock		10	GND
11	Mouse Data		12	GND
13	Reset#		14	GND
15	Hard Disk Activity LED		16	VCC

Figure 2

2.4.2 Keyboard

An AT or PS/2 keyboard can be installed using the multifunction header J15 (see figure 2 for pinout).

Related Jumpers
None

BIOS Settings
None

2.4.3 PS/2 Mouse

A PS/2 mouse can be installed using the multifunction header J15 (see figure 2 for pinout).

Related Jumpers
None

BIOS Settings
The PS/2 Mouse feature is enabled by default.
To change settings, see Section 4.1.2.5 - *Advanced Menu Selection*

2.5 Parallel Port

The Parallel Port is available through the J7 26-pin connector. It is bi-directional and supports the Standard, EPP and ECP operating modes.

Related Jumpers
None

BIOS Settings
To setup the Parallel Port, refer to Section 4.1.2.5.4 - On-board Device Configuration, *Parallel Port.*

The usual way to use the parallel port is to issue signals from the J7 26-pin connector to a standard 25-pin D-Sub connector using an adapter cable (see figure 3). Such a cable is available from Kontron (Part Number: 150-172-xx).

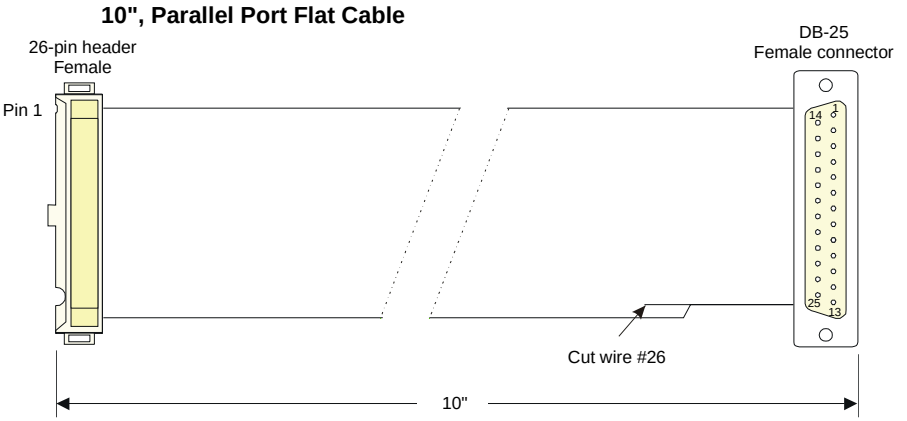


Figure 3

2.6 Power Supply

When used as a stand-alone system, the PCI-990 must be powered through the J19 Power connector. When installed on a backplane, the power is drawn to the board through the power lines of the PCI and ISA edge connectors.

Related Jumpers
None

BIOS Settings
None.

The power requirements are specified as follows:

Part	Voltage Core (V)	Frequency INT/BUS (MHz)	+5V Power Max (Watts)	+12V (Watts)	+3.3V (Watts)	Ambient Temp. °C
PCI-990	**Set by CPU**	**133**	**61**	**3.6**	**21.8**	**50**

2.7 Serial Ports

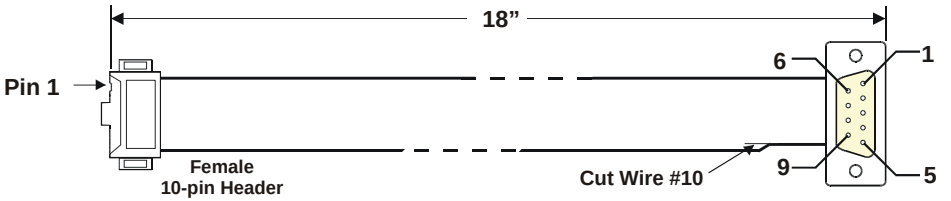
2.7.1 Serial Port 1

The Serial Port 1 is available through the J13, 10-pin connector and supports the RS-232 operation mode.

Related Jumpers
None

BIOS Settings
To setup the Serial Port 1, refer to Section 4.1.2.5.4 - On-board Device Configuration, *Serial Port A*

The usual way to use to the serial port is to issue its signals through a 10-pin header/9-pin D-Sub adapter cable. An 18 inches 10-pin header/9-pin D-Sub adapter cable is available from Kontron: Part number 150-019-xx.



RS-232 Serial Port Flat Cable (150-019)

Figure 4

CAUTION
While adapter cables are provided from various sources, the pinout is often different. The direct crimp design offered by Kontron allows the simplest cable assembly. All cables are available from Kontron by contacting the Sales Department (see Appendix G)

2.7.2 Serial Port 2

The Serial Port 2 is available through the J14 10-pin connector, and supports both RS-232 and RS-422/485 operation modes.

Related Jumpers

W1 and W2: to connect/disconnect Serial Port 2 termination resistors (in RS-422/485 mode)

Setups are described in Section 3.1 – *Setting Jumpers*

BIOS Settings

To setup the Serial Port B, refer to Section 4.1.2.5.4 - On-board Device Configuration, *Serial Port B*

The usual way to use the serial port is to issue signals through a 10-pin header/9-pin D-Sub adapter cable (see description provided for the Serial Port 1).

RS-232 Mode

By default, the Serial Port 2 is configured for RS-232 operation mode.

To change the operating mode, see Section 4.1.2.5.4 On-board Device Configuration, Serial Port B. Mode options are: RS-232, RS-422, and RS-485.

RS-422/RS-485 Modes

In RS-422 and RS-485 modes, transmitting and receiving use differential signals in either full-duplex (RS-422) or party line (RS-485) communication.

Communicating with differential signals requires one pair of wires for RS-485 and two pairs for RS-422 (one for transmission and one for reception).

For a better noise rejection, the use of twisted pair cable is highly recommended. This will enable faster serial transmissions over greater distances than with the common RS-232 cables.

If the board is installed at one end of the network and the Serial Port 2 is configured for communicating in RS-422 or RS-485 mode, use the W1 and W2 jumpers to connect the RS-485/RS-422 termination resistors (120 ohms) while the board is terminating the network.

RS-422 - Full Duplex Operation: The RS-422 protocol uses both RX and TX lines during a communication session. Upon power-up or reset, the serial port 2 interface circuits are automatically configured for full duplex operation. Pins 3 and 4 of J14 act as the receiver lines and pins 5 and 6 act as the transmitter lines.

In RS-422 mode, the software should not use the handshake signals (e.g., DSR, DTR), since they are not connected. However, software handshaking can be used (e.g., XON-XOFF).

RS-485 - Party Line Operation: The RS-485 offers to multiple stations the ability to transmit and receive over the same pair of wires (RX outputs: pins 3 and 4 of J14 and share the same communication line with multiple stations).

The RS-485 protocol offers advantages such as increased speed over long distances, improved reliability over similar RS-232 setups, the ability to share transmission line, and simpler cabling requirements than the RS-422 protocol.

In this configuration, only one system takes control of the communication at a time.

Upon power-up or reset, the transceiver is by default in "receiver mode" to avoid line perturbation.

2.8 Storage Devices

2.8.1 Floppy Disk Drives

Two floppy disk drive units can be connected to the board through the J10 Floppy Disk connector using a standard IBM 34-pin flat ribbon cable. An 18” floppy disk cable is available from Kontron: part number 150-051-xx.

Related Jumpers

None

BIOS Settings

To define the Floppy Disk installation, refer to Section 4.1.2.4 Main Menu selection.
To enable/disable the Floppy Disk controller, refer to Section 4.1.2.5.4 On-board Device Configuration*, Floppy Disk Controller.*
To enable/disable the system to boot from the floppy disk, refer to Section 4.1.2.7 PHOENIX BIOS *Setup Program, Boot Menu Selection.*

The floppy disk cable is illustrated below:

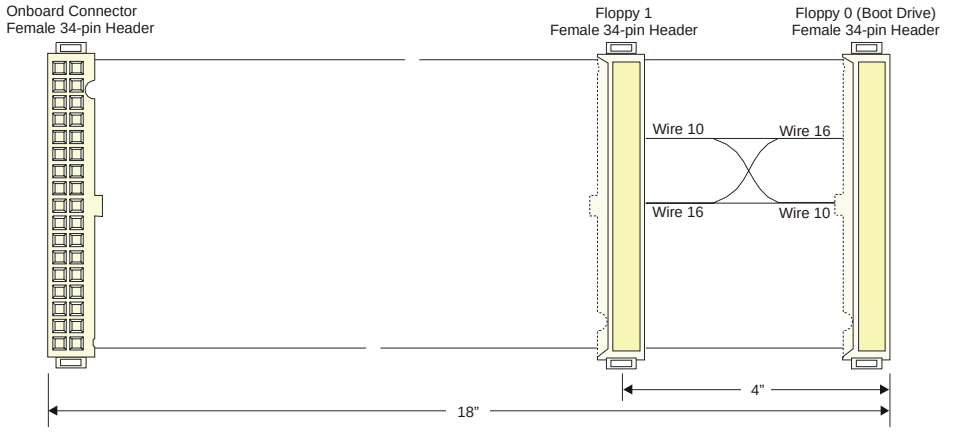


Figure 5

2.8.2 IDE Devices

Two IDE interfaces are provided to support up to four IDE devices, such as hard disks, CD-ROM, and ZIP drives. The interfaces are referred to as Primary (J5 connector) and Secondary (J6 connector). Connections are supported through 40-pin dual row headers.

Related Jumpers

None

BIOS Settings

To detect a hard disk drive type, refer to Section 4.1.2.4 PHOENIX BIOS *Setup Program, Main Menu Selection, Primary Master (or Slave), Type, and set it to "Auto".*
To enable/disable the IDE controller, refer to Section 4.1.2.5 Advanced Menu selection*, Local Bus IDE adapter.*
To enable/disable the system to boot from the floppy disk, refer to Section 4.1.2.7 PHOENIX BIOS *Setup Program, Boot Menu Selection.*

To connect one IDE interface, use a 40-pin flat ribbon cable. An 18 inches length cable is available from Kontron part number 150-259-xx.

The cable is illustrated below:

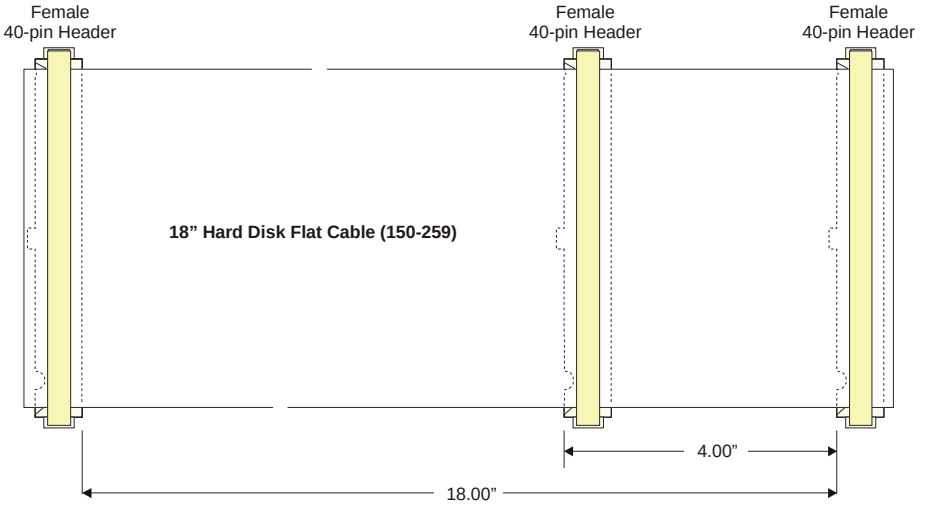


Figure 6

2.9 USB Ports

The board provides a dual-USB interface through the J12 10-pin header. You can connect a USB device by using J23 USB connector located on the faceplate.

Related Jumpers

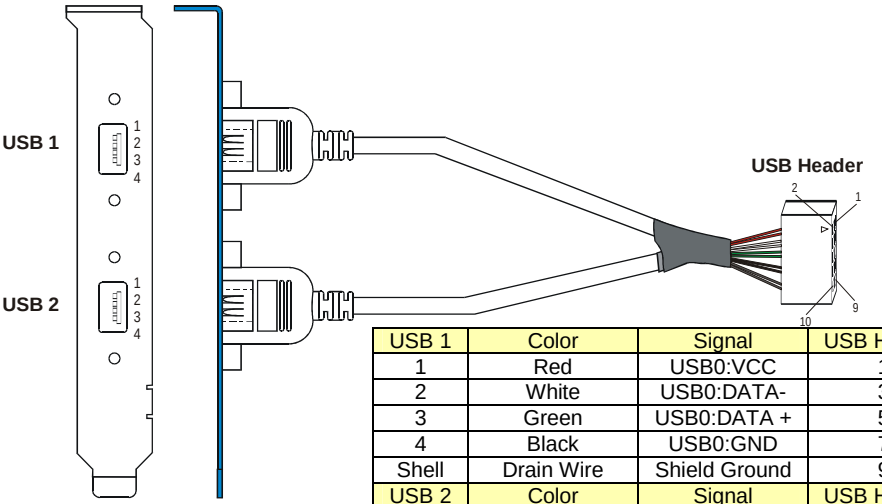
None

BIOS Settings

To enable/disable the USB Host controller, refer to Section 4.1.2.5 Advanced Menu selection*, USB Host Controller.*

To support USB keyboard, refer to Section 4.1.2.5 Advanced Menu selection*, USB BIOS Legacy Support.*

The USB cable/bracket assembly is described as follows:



USB 1	Color	Signal	USB Header
1	Red	USB0:VCC	1
2	White	USB0:DATA-	3
3	Green	USB0:DATA +	5
4	Black	USB0:GND	7
Shell	Drain Wire	Shield Ground	9
USB 2	Color	Signal	USB Header
1	Red	USB1:VCC	2
2	White	USB1:DATA -	4
3	Green	USB1:DATA+	6
4	Black	USB1:GND	8
Shell	Drain Wire	Shield Ground	10

Figure 7

2.10 Video Features

The CRT display connects directly to the J24 standard VGA 15-pin D-Sub connector located on the edge bracket.

Related Jumpers

None

BIOS Settings

Refer to Section 4.1.2.5.2.1 - PCI Device Configuration, *Onboard VGA Controller, Default Primary Video Controller and ISA graphics device installed.*

A PCI interrupt can be assigned to the video controller, the video controller will issue an interrupt request signal when the end of an active field (VSYNC pulse to the CRT monitor) is reached.

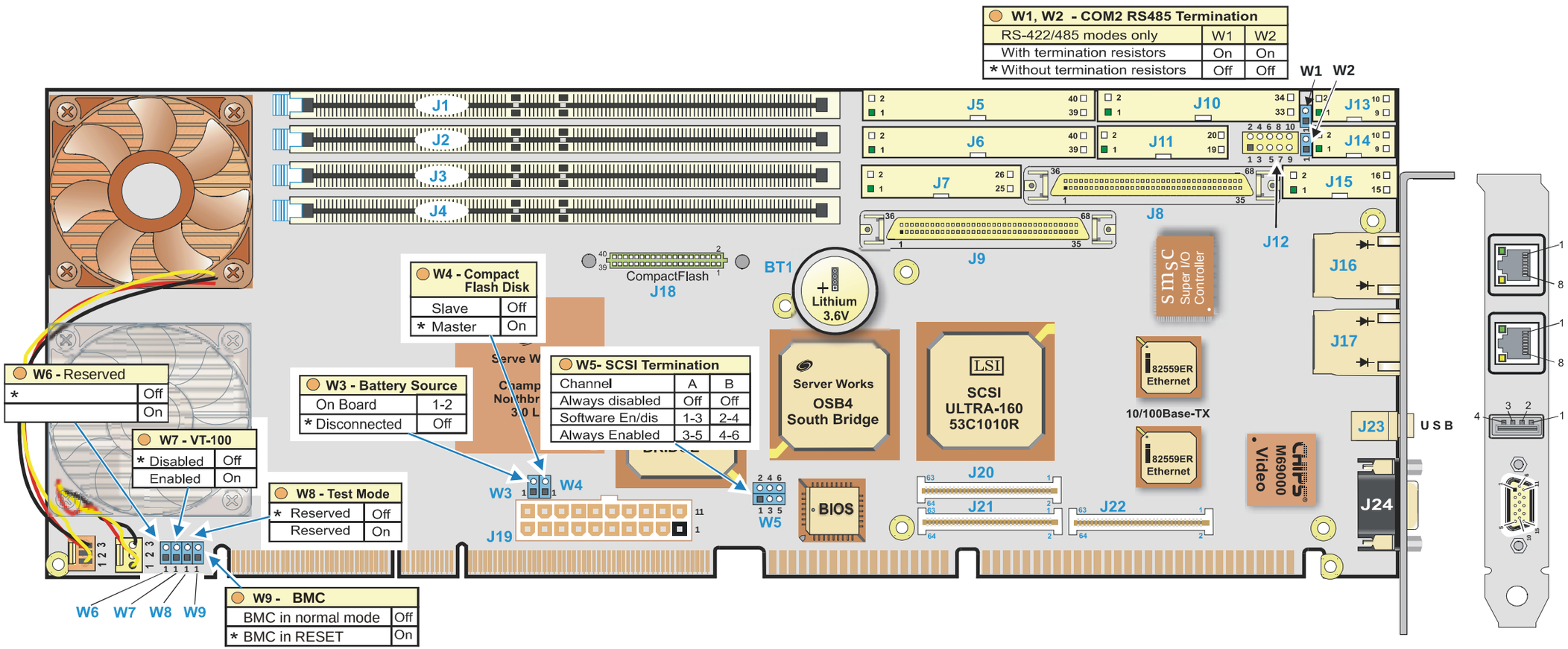
PART 3

3 INSTALLING THE BOARD

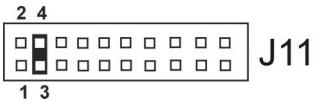
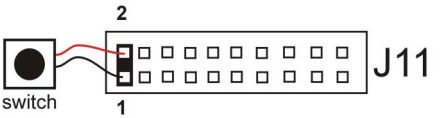
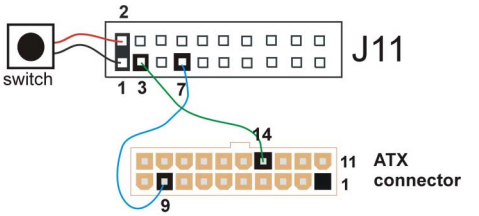
1. SETTING JUMPERS
2. POWERING UP THE BOARD
3. REGISTER'S DESCRIPTION

3.1 Setting Jumpers

PCI-990 Connector and Jumper Locations



3.2 Powering up the board

<table>
<tr><th colspan="3">To power up the board with an ATX power supply</th></tr>
<tr><th>Boot Mode</th><th>With backplane</th><th>Things to do</th></tr>
<tr><td rowspan="2">AT mode
(power up directly from the power supply main switch)</td><td>No</td><td>Short PS_ON# signal to GND
(Install a jumper between pin 3 & 4 of J11)
 
</td></tr>
<tr><td>Yes</td><td>Short PS_ON# signal of the backplane to GND
(See backplane manual for reference)</td></tr>
<tr><td rowspan="2">ATX mode
(Soft-off support & to power up the board from the remote power button connected to J11)</td><td>No</td><td>Add a momentary switch between POWER_BUTTON# and GND (Install the switch between pin 1 & 2 of J11)
 
</td></tr>
<tr><td>Yes</td><td>1 - Add a momentary switch between POWER_BUTTON# and GND (Install the switch between pin 1 & 2 of J11)
2 - Connect pin 9 (5VSB) of ATX connector of the backplane to pin 7 (VCCSB) of J11
3 - Connect pin 14 (PS_ON#) of ATX connector of the backplane to pin 3 (PS_ON#) of J11
 
</td></tr>
</table>

NOTE: Factory configuration is ATX mode with backplane where no jumper installed on Pin 3 & 4 of J11. If the board does not power up the first time, make sure that ATX support is properly configured, you may also force AT mode to power up the board by adding a jumper on pin 3 & 4 of J11 for debugging purpose.

3.3 Register's Description

3.3.1 Supervisor Registers

The Supervisor Registers consist of eight I/O registers that are used to configure and control the special features of the board and the Programmable Watchdog.

These registers are 8-bit wide and can be configured to three different I/O base addresses: 190h, 290h or 390h.

When setting Register x90h at one base address, all the other registers are located at the same base address plus one, two, three and so on. To select the base address, use the PHOENIX BIOS *Setup Program, Advanced Menu Selection*

This section includes a description of each I/O register and bit available for programming and configuring the PCI-990.

3.3.2 Register x90h: Serial port 2 configuration.

Bit	7	6	5	4	3	2	1	0
Reset				0	0	0		
Read				RS485	RS232	ST1		
Write				RS485	RS232	ST1		

Used by the BIOS, only during the POST.

Serial port 2 configuration/use

ST1 Enable RTS2 to be used as 485TX enable when in 485 mode (1: enable, 0: disable).

RS232 Enable RS-232 mode for serial port 2 (1: enable, 0: disable).

RS485 Enable RS-422/RS-485 mode for serial port 2 (1: enable, 0: disable).

> **NOTE**
>
> The RS232 and RS485 bits are initialized by the BIOS during POST (Power-On Self Test). If a modification of these bits is required, be aware that there is a hardware protection so that RS232 and RS485 buffers cannot be activated at the same time. This protection is provided at the register level. If you write to x90h register with bits 3 and 4 set, you will actually write 0 in both of these bits. This condition can be read back.

3.3.3 Register x91h: Reset History & CPU Fault

Bit	7	6	5	4	3	2	1	0
Reset				1				
Read	PBH		WDO	CPUFAULT				
Write				CPUFAULT				

CPUFAULT This bit is set by application software to indicate through the Harware Monitor connector pin 8 (see pin description in appendix) that the software is in fault status.

Reset history

PBH When high, indicates that the last system reset was caused by a Push Button Reset from the Multi-Function connector. It is cleared at power-up and when the bit CLRHIS* is "0" (see register x92h description).

WDO This bit is set when the watchdog produces a reset. It is cleared at power-up and when the bit CLRHIS* is "0" (see register x92h description).

3.3.4 Register x92h: Clearing Reset History & Lock for Watchdog

Bit	7	6	5	4	3	2	1	0
Reset						1		1
Read						LOCK		CLRHIS*
Write						LOCK		CLRHIS*

* = Active low signal

Reset history

CLRHIS* A 0-1 pulse will clear all reset history bits (refer to the x91h register described previously). In normal operation, always keep the CLRHIS* bit to "1" otherwise the reset source will not be captured (the history latch are disabled when CLRHIS* is "0").

Programmable watchdog

LOCK When set, the state of the enable bit for the programmable watchdog (WDEN) cannot be changed.

3.3.5 Register x93h: Silicon ID Chip Interface, Serial EEPROM, System Monitor Connector Interface

Bit	7	6	5	4	3	2	1	0
Reset					1		1	1
Read					IDCHIP		SCL	SDA
Write					IDCHIP		SCL	SDA

* Not used by the BIOS.

Silicon ID chip

IDCHIP Used to read the onboard silicon serial number using the Dallas Semiconductor one-wire protocol.

User EEPROM

SCL/SDA Clock and data I^2C link to user EEPROM.

3.3.6 Register x94h & x95h

These registers are reserved.

3.3.7 Register x96h: Programmable Watchdog

Bit	7	6	5	4	3	2	1	0
Reset	0	1	1	1				
Read	WDEN	WDS2	WDS1	WDS0				
Write	WDEN	WDS2	WDS1	WDS0				

Not used by the BIOS, except when the Watchdog Option is enabled in BIOS SETUP and After POST is set.

WDEN When this bit is set, the programmable watchdog is enabled with the current timeout specified by WDS[2..0] (Refers to the dual-stage programmable watchdog description in section 3.3.9.1).
To avoid accidental deactivation of the watchdog, the bit WDEN is normally locked by the bit LOCK of register x92h (see register x92h description).

WDS[2..0] Timeout selection (see section 3.3.9.1.3).

3.3.8 Register x97h: System Monitor Connector sources

Bit	7	6	5	4	3	2	1	0
Reset								
Read					EXTFLT_EN	ExtFlt	WDNMI_EN	WDNMI
Write					EXTFLT_EN		WDNMI_EN	

Not used by the BIOS.

ExtFlt External fault status: see System Monitor Connector in Appendix D. This 5V TTL input is pulled-up to +5V by a 8.2K resistor.

EXTFLT_EN	Enable NMI generations from EXTFLT input of “Monitor” connector
WDNMI_EN	Enable NMI generations from first WatchDog stage timeout
WDNMI	When low, signal NMI from watchdog time-out

All bits are active "1" regardless of the electrical state of the signal. Inversion is provided by the hardware when required.

3.3.9 Supervision Features

3.3.9.1 Watchdog

The function of a watchdog is to reset the CPU board when the processor is unable to generate a trigger for longer than the watchdog timeout period. This feature is useful in embedded systems where human supervision is not required or impossible.

The PCI-990 provides a digital watchdog with a software programmable timeout period.

The watchdog can be enabled by software or using CMOS setup option, see section 4.1.2.5.5 - Advanced Chipset Control.

3.3.9.1.1 Enabling the Programmable Watchdog

To enable the programmable watchdog, first unlock the enable bit by clearing the lock bit in register x92h, then set the bit WDEN in register x96h and re-lock it by setting the lock bit in register x92h. The following is an example in C language.

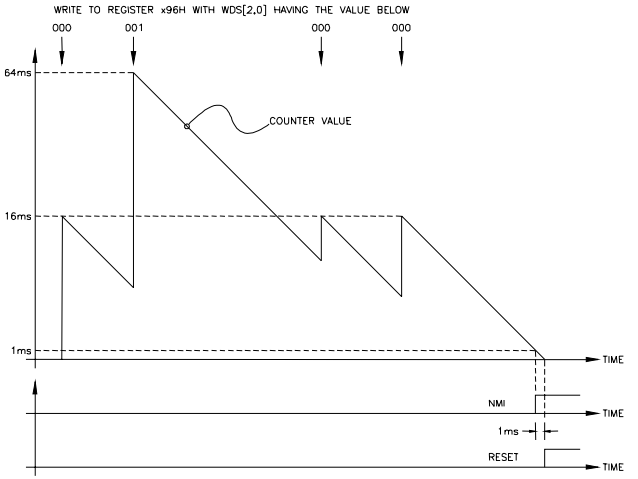
```
#define TekReg 0x190              // define base address (0x190, 0x290 or 0x390)

void ArmWatchdog(void)
{
   outp(TekReg+2,inp(TekReg+2) & 0xFB);    // unlock watchdog enable bit
   outp(TekReg+6,inp(TekReg+6) | 0xF0);    // enable & trigger at max timeout
   outp(TekReg+2,inp(TekReg+2) | 0x04);    // lock watchdog enable bit
}
```

3.3.9.1.2 Triggering the Programmable Watchdog

To trigger the programmable watchdog, the processor writes to register x96h. The result of writing to the register is the trigger and the value written to the register telling the watchdog the current timeout to use (see register x96h description). For a fixed timeout, the processor simply writes a constant in register x96h.

A variable refresh is possible as shown below:



The programmable watchdog can be viewed as a decrementing counter that is initialized by a write to register x96h. The processor must initialize the counter to prevent it from reaching count 0 (timeout).

The following C language function can be used to trigger the programmable watchdog.

```
#define TekReg 0x190       // define base address (0x190, 0x290 or 0x390)
void TrigWatchdog(timeout) // select timeout at runtime: 0x80, 0x90, 0xA0, 0xF0
{
   outp(TekReg+6,(inp(TekReg+6) & 0x0F) | (timeout & 0xF0));
}
```

3.3.9.1.3 Timeout

The timeout is chosen at runtime from eight preset values (see table below).

WDS[2,0]	RESET Timeout
000	0.015s
001	0.0625s
010	0.250s
011	1s+ 1ms
100	4s
101	16s
110	64s
111	256s

A reset from the programmable watchdog is latched for reset source identification; refer to the x92h register description in Section 3.3.4.

3.3.10 Power Failure Detection

The board has many power failure detection features (* = active low signal):

It always monitors the +5V, +3.3V and V_{CORE} power supply voltages. When one of these voltages drops below a typical threshold value, the system is reset.

3.3.11 Reset History

Following a reset, the application software can read the register x91h and examine the bit WDO. Based on the values of those bits, the following conclusions can be drawn about the reset source.

PBH	WDO	RESET Source
0	0	Power-up, Ctrl-Alt-Del or software runaway
1	0	Pushbutton reset
0	1	Programmable watchdog

For proper operation, the bit CLRHIS* of register x92h should be pulsed (0 to clear and 1 to activate monitoring) immediately after reading the history bits.

3.3.12 Thermal Management

The PCI-990 includes a user-defined temperature sensor / alarm function, which provides thermal monitoring of the processor(s).

For Thermal Management, see section 4.1.2.6 PHOENIX BIOS *Setup Program, Power Menu Selection, and Hardware Monitor Controls.*

PART 4

4 SOFTWARE SETUP

1. PHOENIX BIOS SETUP PROGRAM
2. BOOT UTILITIES
3. INSTALLING DRIVERS

4.1 PHOENIX BIOS Setup Program

All relevant information for operating the board and connected peripherals is stored in the CMOS memory. A battery-backed up memory holds this information when the board is powered off, the BIOS Setup program is required to make changes to the setup.

NOTES

Make sure you setup the BIOS Setup software prior to installing your operating system and your drivers.

For systems that need the BIOS to first attempt to boot from LAN, follow these steps:

1. Set the “Network Boot”, IBA (Intel Boot Agent) or “Landesk Service Agent II” as the first boot service in the BIOS setup (Boot Menu Selection).
2. Follow the complete procedure in the Boot from LAN utility on CDROM.

4.1.1 Accessing the BIOS setup program

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the PCI-990 peripheral processor. The PCI-990 uses the Phoenix Setup program, a setup utility in flash memory that is accessed by pressing the <DELETE> key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

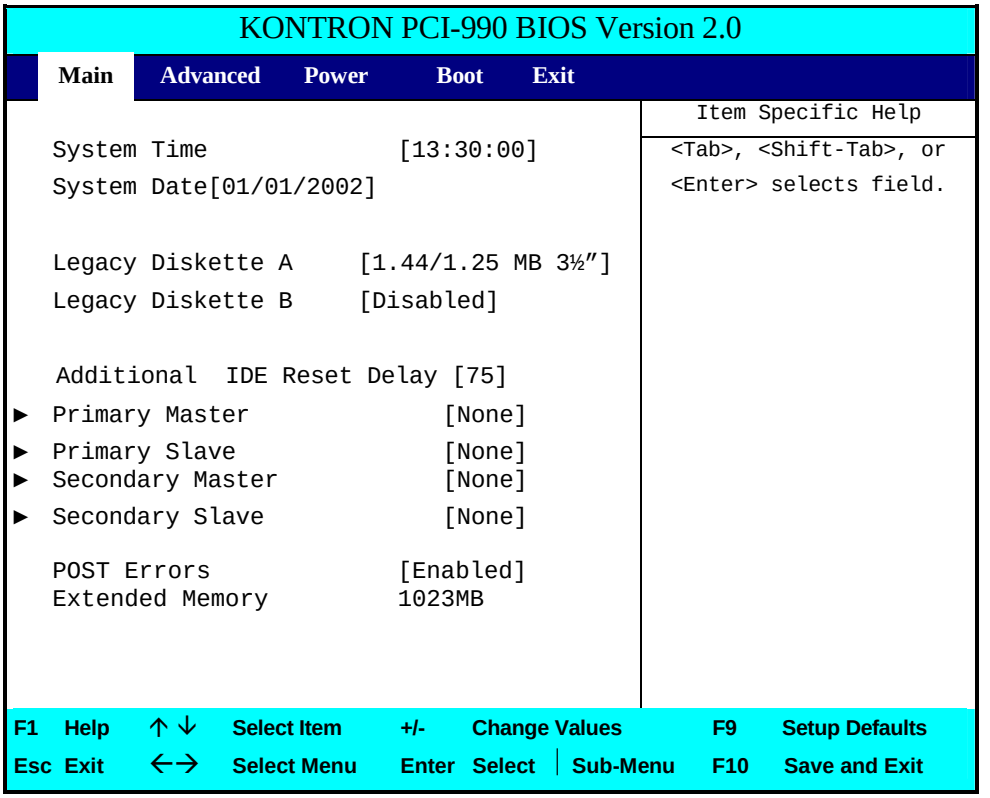
> **CAUTION**
>
> Before modifying CMOS setup parameters, ensure that the W3 battery selection jumper is installed to enable the CMOS battery back up (please refer to Section 3.1).

To run the Phoenix Setup program incorporated in the ROM BIOS:

- Turn on or reboot the system.
- When you get the following message, hit <DELETE> key to enter SETUP

```
PhoenixBIOS 4.0 Release 6.0
Copyright 1985-2000 Phoenix Technologies Ltd.
All Rights Reserved
KONTRON  PCI-990 BIOS Version 2.0
```

The main menu of the Phoenix BIOS CMOS Setup Utility appears on the screen.



Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the SETUP defaults will affect all parameters and will reset options previously altered.

The Setup Defaults values provide **optimum performance** settings for all devices and system features.

CAUTION

These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

NOTES

The CMOS setup option described in this section is based on **BIOS Version 2.0**. The options and default settings may change in a new BIOS release.

4.1.2 The Menu Bar

The Menu Bar at the top of the window lists these selections:

Menu selection	Description
Main	Use this menu for basic system configuration
Advanced	Use this menu to set the Advanced Features available on your system
Power	Use this menu to configure Power Management features and system monitoring
Boot	Use this menu to determine the booting device order.
Exit	Use this menu chose Exits option

Use the left and right ← and → arrows keys to make a selection.

4.1.2.1 The Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The chart on the following page describes the legend keys and their alternates:

Key	Function
<F1> or <Alt-H>	General Help windows (see 4.1.2.2)
<Esc>	Exit this menu.
← → arrow keys	Select a different menu
<Home> or <End>	Move cursor to top or bottom of window.
<PgUp> or <PgDn>	Move cursor to top or bottom of window.
<F5> or <->	Select the Previous Value for the field.
<F6> or <+> or <Space>	Select the Next Value for the field.
<F9>	Load the Default Configuration values for all menus
<F10>	Save and exit.
<Enter>	Execute Command, display possible value for this field or Select the Sub menu

To select an item, use the arrow keys to move the cursor to the field your want. Then use the plus-and-minus value keys to select a value for that field. To save values commands in the Exit Menu save the values currently displayed in all the menus.

To display a sub-menu, use the arrow keys to move the cursor to the sub menu your want. Then press <Enter>. A pointer (►) marks all sub menus.

4.1.2.2 The Field Help Window

The help window on the right side of each menu displays the help text for the currently selected field. It updates as you move the cursor to each field.

4.1.2.3 The General Help Windows

Pressing <F1> or <Alt-H> on any menu brings up the General Help window that describes the legend keys and their alternates:

```
                    General Help

Setup changes system behavior by modifying the BIOS
configuration. Selecting incorrect values may
cause system boot failure; load Setup Default values to
recover.

<Up/Down> arrows select fields in current menu.
<PgUp/PgDn> moves to previous/next page on scrollable menus.
<Home/End> moves to top/bottom item of current menu.

Within a field, <F5> or <-> selects next lower value and
<F6>, <+>, or <Space> selects next higher value.

<Left/Right> arrows select menus on menu bar.
<Enter> displays more options for items marked with |.

<F9> loads factory installed Setup Default values.
<F10> saves current settings and exits Setup.

<Esc> or <Alt-X> exits Setup; in sub-menus, pressing these keys returns to
the previous menu.

<F1> or <Alt-H> displays General Help (this screen).

                        [Continue]
```

4.1.2.4 Main Menu Selection

The scroll bar on the right of any windows indicates that there is more than one page of information in the windows. Use <PgUp> and <PgDn> to display all the pages. Pressing <Home> and <End> displays the first and last page. Main Menu Selection
You can make the following selections on the Main Menu itself. Use the sub menus for other selections.

Feature	Options	Description
System Time	HH:MM:SS	Set the system time.
System Date	MM/DD/YYYY	Set the system date.
Legacy Diskette A: Legacy Diskette B:	Disabled 360Kb 5.1/4” 1.2MB, 5.1/4” 720 Kb 3 1/2” 1.44/1. 25 MB 3 1/2” 2.88 MB 3 1/2	Select the type of floppy disk drive installed in your system. **Note :** 1.25MB 3 1/2” references a 1024 byte/sector Japanese media format. The 1.25MB, 3 1/2 diskette requires a 3-Mode floppy-disk drive.
Additional IDE Reset Delay	0 to 255 ms	Additional Delay after IDE soft reset for auto-detect the drives.

Feature	Options			Description
Primary Master	Type	None		None : No booting device installed.
		CD-ROM	Multi-Sector Transfers LBA Mode Control 32 BIT I/O Transfer Mode Ultra DMA Mode SMART Monitoring	**Multi-Sector Transfers** Choices : Disabled, 2,4,8, and 16 sectors Any selection except Disabled determines the number of sectors transferred per block. Standard is 16 sectors per block. **LBA Mode Control** Choices : Disabled, Enabled Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, heads, and Sectors. **32 Bit I/O** Choices : Disabled, Enabled Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus. **Transfer Mode** Choices : Standard, Fast PIO 1, Fast PIO 2, Fast PIO 3, Fast PIO 4, FPI0 3 / DMA 1, FPIO 4 / DMA2. Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform. **Ultra DMA Mode** Choices : Disabled, Mode 0, 1, 2, 3, 4. Select the Ultra DMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode. **SMART Monitoring** Display type of Monitoring. This field is a “Display Only”. This option can be changed in the Advanced Menu.
		ATAPI Removable		Same choices as CD-ROM

Main Menu Selection (continued)

Feature	Options			Description
Primary Master (Continued)	Type (continued	IDE Removable		Same choices as CD-ROM
		Other ATAPI		Same choices as CD-ROM
		(USER)	Cylinders	**Cylinders** Set the number of cylinders
			Heads	**Heads** Set the number of heads. Choices are 1 to 16
			Sectors	**Sectors** Set the number of sectors per track
			Maximum Capacity	**Maximum Capacity** Maximum capacity is displayed according to the cylinders, heads and sectors selected.
			Multi-Sector Transfers	**Multi-Sector Transfers** Choices are : Disabled, 2, 4, 8 and 16 sectors. Specify the number of sectors per block for multiple sector transfers. “MAX” refers to the size the disk returns when queried.
			LBA mode Control	**LBA Mode Control** Choices are : Enabled, Disabled Enabling LBA cause Logical Block Addressing to be used in place of Cylinders Heads and Sectors
			32 Bit I/O	**32 Bit I/O** Choices are : Enabled, Disabled. This setting enables or disables 32 bit IDE data transfers.
			Transfer Mode	**Transfer Mode** Choices are : Standard, Fast PIO 1, Fast PIO 2, Fast PIO 3, Fast PIO 4, FPI0 3 / DMA 1, FPIO 4 / DMA2. Select the method for moving data to/from the drive. Autotype the drive to select the optimum transfer mode.
			Ultra DMA Mode	**Ultra DMA Mode** Choices are: Disabled, Mode 0 to 4. Select the Ultra DMA mode used for moving data to/from the drive Autotype the drive to select the optimum transfer mode.
			SMART Monitoring	**SMART Monitoring** IDE Failure Prediction

Main Menu Selection (continued)

Feature	Options		Description
		Auto	BIOS autodetects the hard disk installed
Primary Slave	Same as Primary Master		
Secondary Master	Same as Primary Master		
Secondary Slave	Same as Primary Master		
POST Errors	Enabled Disabled		Pauses and displays SETUP entry or resume boot prompt if error occurs on boot. If disabled, system always attempts to boot.
Exended Memory	Depends on the memory installed on your computer		Displays the amount of RAM memory detected during boot up minus the base memory (1 Mbyte).

4.1.2.5 Advanced Menu Selection

You can make the following selections on the Advanced Menu. Use the sub menus for other selections.

Feature	Options	Description
Boot Setting Configuration	**This is a Sub-Menu, see section** 4.1.2.5.1	Additional setup menus to configure Boot Setting.
PCI Configuration	**This is a Sub-Menu, see section 4.1.2.5.2**	Additional setup menus to configure PCI device.
Cache Memory	**This is a Sub-Menu, see section 4.1.2.5.3**	Determines hows to configure the specified block of memory.
On-board Device Configuration	**This is a Sub-Menu, see section 4.1.2.5.4**	Pheripheral Configuration
Advanced Chipset Control	**This is a Sub-Menu, see section 4.1.2.5.5**	
DMI Event Logging	**This is a Sub-Menu, see section 4.1.2.5.6**	View and modify DMI event logs.
Console Redirection	**This is a Sub-Menu, see section 4.1.2.5.7**	Additional setup menus to configure console.

4.1.2.5.1 Boot Setting Configuration

You can make the following selections on the Boot Setting Configuration Sub-Menu. Use the sub menus for other selections.

Feature	Options	Description
Installed O/S	Other Win95 Win98 WinMe Win2000	Other : General Setting Win95/Win98/WinMe/Win2000: Specific Settings **Note :** An incorrect setting can cause some operating systems to display unexpected behavior.
Enable ACPI	No Yes	Enable/Disable ACPI BIOS (Advanced Configuration and Power Interface).
Use Multiprocessor Specification	1.1 1.4	Configures the multiprocessor specification (MPS) revision level. Some operating systems will require revision 1.1 for compatibility reasons.
Use PCI Interrupt Entries in MPS	Yes No	Configures the MPS Table with PCI interrupt entries.

Boot Setting Configuration (continued)

Feature	Options	Description
QuickBoot Mode	Enabled Disabled	Allows the system to skip certain tests while booting. This will decrease the time needed to boot the system.
Clearing Extended Memory	Enabled Disabled	Allows the system to skip Clearing Memory if QuickBoot is Enabled. This will decrease the time needed to boot the system. Some OS require Memory to be cleared.
Boot-time Diagnostic Screen	Enabled Disabled	Displays the Diagnostic Screen during Boot. Always Enabled when Console Redirection is activated.
Summary Screen Delay	None 30 seconds	Delay to display the system configuration at boot time.
Save CMOS in FLASH	Disabled Enabled	Saving CMOS memory content into Flash Memory will prevent loosing CMOS options when battery fails.
Reset Configuration Data	No Yes	Select “Yes” if you want to clear the Extended System Configuration Data (ESCD) area.
Local Bus IDE adapter	Disabled Primary Secondary Both	Enabled the integrated local bus IDE adapter.
Large Disk Access Mode	Other DOS	If you are using UNIX, Novell Netware or other operating systems, select “**Other**”. If you are installing new software and the drive fails, change this selection and try again. Different operating systems require different representations of drive geometry.
PS/2 Mouse	Disabled Enabled	"Disabled prevent any installed PS/2 mouse from functioning, but frees up IRQ 12. "Enabled forces the PS/2 mouse port to be enabled regardless if a mouse is present.

4.1.2.5.2 PCI Configuration

You can make the following selections on the PCI Configuration Sub-Menu. Use the sub menus for other selections.

Feature	Options	Description
PCI Device Configuration	**This is a Sub-Menu, see section 4.1.2.5.2.1**	Configure PCI devices
PCI/PNP ISA UMB Region Exclusion	**This is a Sub-Menu, see section 4.1.2.5.2.2**	Reserves specific upper memory blocks for use by legacy ISA devices.
PCI/PNP ISA IRQ Resource Exclusion	**This is a Sub-Menu, see section 4.1.2.5.2.3**	Reserves specific IRQs for use by legacy ISA devices.
Special PCI Routing	Enabled Disabled	Disable this option if the backplane into which the board is installed conforms to the PICMG specifications. When enabled the board will set a Special PCI Routing configuration: INTA-INTD of IDSEL 27-24 will be routed directly.
USB Host Controller	Enabled Disabled	Enables or Disable the USB hardware (Disabled resources will be freed up for other uses).
USB BIOS Legacy Support	Enabled Disabled	Enables or Disables support for USB Keyboards and Mice. (Enable for use with a non-USB aware Operating System such as DOS or UNIX)
PCI Bridges Cache Line Size	0, 2, 8 or 16	Set the Cache Line Size on DWORDS.
Default Primary Latency Timer	Default, 0020h, 0040h, 0060h, 0080h, 00A0h, 00C0h or 00E0h	Minimum guaranteed time slice allocated for bus master in units of PCI bus clocks for device not in this menu. Default = 20h for PCI bridges. Default = value based on Minimum Grant for all other PCI devices.
Default Secondary Latency Timer	None, 0020h, 0040h, 0060h, 0080h, 00A0h, 00C0h or 00E0h	Minimum guaranteed time slice allocated for bus master in units of PCI bus clocks.
Primary Host Bridge Latency Timer	None, 0020h, 0040h, 0060h, 0080h, 00A0h, 00C0h or 00E0h	Minimum guaranteed time slice allocated for bus master in units of PCI bus clocks.
Secondary Host Bridge Latency Timer	None, 0020h, 0040h, 0060h, 0080h, 00A0h, 00C0h or 00E0h	Minimum guaranteed time slice allocated for bus master in units of PCI bus clocks.

4.1.2.5.2.1 PCI Device Configuration

You can make the following selections on the PCI Device Configuration Sub-Menu. Use the sub menus for other selections.

Feature	Options	Description
Onboard VGA Controller	Enabled Disabled	Enables/Disables onboard VGA controller
Default Primary Video Adapter	Onboard External	Select "External" to have PCI video card (must be installed) to be set as boot Display Device.
ISA graphics device installed	No Yes	Enable ISA (non-VGA) graphics device to access palette data in PCI VGA device.
Ethernet Controller Configuration (Optional*)	**This is a Sub-Menu, see section 0**	Configure PCI Ethernet Device (s).
Onboard P2p64 Controller	Enabled Disabled	Enables/Disable onboard PCI-PCI Bridge Controller to Backplane.
Delay before PCI Initialization	0 to 7	Delay in seconds before PCI Initialization. Some external card may require a minimum delay after reset before they can be accessed. Card with onboard CPU that emulate a PCI Controller (ex.: RAID) are more likely to require a delay.
Onboard SCSI Controller	Enabled Disabled	Enables/Disables onboard SCSI controller.
Option ROM	Enabled Disabled	Initialize device expansion ROM
Enable Master	Enabled Disabled	Enable selected device as a PCI bus master.
Latency Timer	Default, 0020h, 0040h, 0060h, 0080h, 00A0h, 00C0h or 00E0h	Minimum guaranteed time slice allocated for bus master in units of PCI bus clocks.

*Optional: Some feature is displayed only if de option is installed on your PCI990 card.
PCI Device Configuration (continued)

4.1.2.5.2.1.1 Ethernet Controller Configuration

You can make the following selections on the Ethernet Controller Configuration Sub-Menu.

Feature	Options	Description
Mezzanine Gigabit Contr. Slot 0103	Enabled Disabled	Enables/Disables Gigabit Controller on Bus 01 and Device 03. This is the mezzanine LAN1. The LAN number is written on PCI990 back side.
Option ROM	Enabled Disabled	Initialize device expansion ROM
Mezzanine Gigabit Contr. Slot 0105	Enabled Disabled	Enables/Disables Gigabit Controller on Bus 01 and Device 05. This is the mezzanine LAN0. The LAN number is written on PCI990 back side.
Option ROM	Enabled Disabled	Initialize device expansion ROM
Onboard Ethernet Contr. Slot 0001		Enables/Disables Onboard Ethernet Controller on Bus 00 and Device 01. This is the LAN0. The LAN number is written on PCI990 back side.
Option ROM	Enabled Disabled	Initialize device expansion ROM
Onboard Ethernet Contr. Slot 0002		Enables/Disables Onboard Ethernet Controller on Bus 00 and Device 02. This is the LAN1. The LAN number is written on PCI990 back side.
Option ROM	Enabled Disabled	Initialize device expansion ROM

4.1.2.5.2.2 PCI/PNP ISA UMB Region Exclusion

You can make the following selections on the PCI/PNP ISA UMB Region Exclusion Sub-Menu. Use the sub menus for other selections.

Feature	Options	Description
C800-CBFF	Available Reserved	Reserves the specified block of upper memory for use by legacy ISA devices.
CC00-CFFF		
D000-D3FF		
D400-D7FF		
D800-DBFF		
DC00-DFFF		

4.1.2.5.2.3 PCI/PNP ISA IRQ Resources Exclusion

You can make the following selections on the PCI/PNP ISA IRQ Resources Exclusion Sub-Menu. Use the sub menus for other selections.

Feature	Options	Description
IRQ 3:	Available Reserved	Reserves the specified IRQ for use by legacy ISA devices
IRQ 4:		
IRQ 5:		
IRQ 7:		
IRQ 9:		
IRQ 10:		
IRQ 11:		

4.1.2.5.3 Cache Memory

You can make the following selections on the Cache Memory Sub-Menu.

Feature	Options	Description
Memory Cache	Enabled Disabled	Sets the state of memory cache.
Cache System BIOS area	Uncached Write Protect	Controls caching of system BIOS area.
Cache Video BIOS area	Uncached Write Protect	Controls caching of video BIOS area.
Cache Base 0-512K	Uncached Write Through Write Protect Write Back	Controls caching of 512K base memory.

Cache Memory (continued)

Feature	Options	Description
Cache Base 512K-640K	Uncached Write Through Write Protect Write Back	Controls caching of 512K-640K base memory.
Cache Extended Memory Area	Uncached Write Through Write Protect Write Back	Controls caching of system memory.
Cache A000 - AFFF Cache B000 - BFFF	Disabled USWC Caching Write Through Write Protect Write Back	Disabled - This block is not cached. USWC Caching - Uncaching Speculative Write Combined. Write Through - Write are cached and sent to main memory at once. Write Protect - Writes are ignored. Write Back - Writes are cached, but not sent to main memory until necessary.
Cache C800 - CBFF Cache CC00 - CFFF Cache D000 - D3FF Cache D400 - D7FF Cache D800 - DBFF Cache DC00 - DFFF Cache E000 - E3FF Cache E400 - E7FF Cache E800 - EBFF Cache EC00 - EFFF	Disabled Write Through Write Protect Write Back	Disabled - This block is not cached. Write Through - Write are cached and sent to main memory at once. Write Protect - Writes are ignored. Write Back - Writes are cached, but not sent to main memory until necessary.

4.1.2.5.4 On-board Device Configuration

You can make the following selections on the On-board Device Configuration Sub-Menu.

Feature	Options	Description
Serial port A	Enabled Disabled Auto	Configure serial port A using options: **Disabled :** No configuration **Enabled :** User configuration **Auto :** BIOS or OS chooses configuration
Base I/O address	3F8, 2F8, 3E8 or 2E8	Sets the base I/O address for serial port A.
Interrupt	IRQ3 or IRQ4	Sets the interrupt for serial port A.
Serial port B	Enabled Disabled Auto OS Controlled	Configure serial port B using options: **Disabled :** No configuration **Enabled :** User configuration **Auto :** BIOS or OS chooses configuration
Mode	RS-422 RS-485 RS-232	Set the mode for Serial Port B.
Base I/O address	3F8, 2F8, 3E8 or 2E8	Sets the base I/O address for serial port B.
Interrupt	IRQ3 or IRQ4	Sets the interrupt for serial port B.
Parallel port	Enabled Disabled Auto	Configure Parallel port using options: **Disabled :** No configuration **Enabled :** User configuration **Auto :** BIOS or OS chooses configuration
Mode	Output only Bi-directional EPP ECP	Set the mode for the parallel Port using option: Output only Bi-directional EPP ECP
Base I/O address	378, 278 or 3BC	Sets the base I/O address for Parallel port.
Interrupt	IRQ5 or IRQ7	Sets the interrupt for Parallel port.
DMA channel	DMA 1 or DMA 3	Sets the DMA channel for Parallel port.
Floppy Disk Controller	Enabled Disabled Auto	Configure Floppy Disk Controller using options: **Disabled :** No configuration **Enabled :** User configuration **Auto :** BIOS or OS chooses configuration
Base I/O address	Primary Secondary	Sets the base I/O address for the Floppy Disk Controller using options: Primary Secondary

4.1.2.5.5 Advanced Chipset Control

You can make the following selections on the Advanced Chipset Control Sub-Menu. Use the sub menus for other selections.

Feature	Options	Description
CNB30 Setting	**This is a Sub-Menu, see section 4.1.2.5.5.1**	CNB30 advanced chipset setup.
Error Command Setting	**This is a Sub-Menu, see section 4.1.2.5.5.2**	SERR# and PERR# enable or disable.
Frequency Ratio	Safe Mode 100/1050 133/1400 100/850 133/1133 100/950 133/1600 100/1150 133/1266 100/900 133/1533 100/550 133/1200 100/600 133/733 100/700 133/800 100/1100 133/1066 100/650 133/933 100/1000 133/1333 100/750 133/1000	Selects the internal frequency mutiplier of the CPU. Works for Engineering Sample (ES) CPU only.
Enable memory gap	Disabled Conventional Extended	If enabled, turns system RAM off to free address space for use with an option card. A 1MB extended memory gap, starting at 15MB, will be created in system RAM.
Supervisor I/O Base Address	Disabled 190h 290h 390h	Select an I/O address for Kontron FPGA.
Watchdog Timer	Disabled Enabled	Enables the Watchdog circuit when the POST is running.
Watchdog After POST	Disabled Enabled	Enables the Watchdog circuit after the POST sequence. The BIOS will hook the Timer Tick interrupt to automatically refresh the Watchdog, unless the OS replaces the interrupt service.
Watchdog Duration (ms)	16, 64, 256, 1024, 4096, 16384, 65536 or 262144	Select the duration time (in ms) of the Watchdog timing circuitry.

4.1.2.5.5.1 CNB30 Setting

You can make the following selections on the CNB30 Setting Sub-Menu.

Feature	Options	Description
Memory Write Posting	Enabled Disabled	Enable/Disable Memory write posting in CNB30.
PCI Back to Back Write	Enabled Disabled	PCI Back-to-Back write enabled or disable for Processor Bus-to-PCI posted writes.
Write Combining	Enabled Disabled	Enable/Disable Write combining for Processor Bus-to-PCI posted writes.
Posting to Non-Prefetch	Enabled Disabled	Enable/Disable posting to non-prefetch regions.
Write posting	Enabled Disabled	Enable/Disable Pentium Pro posting. See register 4B bit 1.
Defer Reads & Writes	Enabled Disabled	Enable/Disable Defer for Processor Bus-to-PCI reads and writes.
IOQ Threshold Value	Hardwired, 1, 2, 3, 4, 5, 6, or 7	Uses hardware setting if set to Hardwired. Otherwise uses the IOQ value set by the user.
Memory Timing	00h, 08h, 0Ah 48h B0h or FCh	Setup Memory Timing
CAS Latency	3 or 2	SDRAM CAS Latency
Enhanced Page Hit Timing	10-1-1-1 9-1-1-1	Select Page hit timing.

4.1.2.5.5.2 Error Command Settings

You can make the following selections on the Error Command Settings Sub-Menu.

Feature	Options	Description
ECC Config	Enabled Disabled	If all memory in the system supports ECC then use this option to enable or disable ECC support.
Scrubbing	Enabled Disabled	When enabled, CNB30 writes back the ECC corrected memory data back to the DRAM.
Correctable Error	Enabled Disabled	Enable or Disable Correctable Error settings.
Uncorrectable Error	Enabled Disabled	SERR# for Uncorrectable Error. When Enabled, the CNB30 generates SERR# when it detects a memory ECC uncorrectable error.

4.1.2.5.6 DMI Event Logging

You can make the following selections on the DMI Event Logging Sub-Menu.

Feature	Options	Description
Event log capacity	N/A	Space DMI Event Logging
Event log validity	N/A	Valid
View DMI event log	Enter	View the contents of the DMI event log
Clear all DMI event logs	Yes/NO	Setting this to yes will clear the DMI event log after rebooting
Event Logging	Enabled Disabled	Select 'Enabled' to allow logging of DMI events
ECC Event Logging	Enabled Disabled	Select 'Enabled' to allow logging of ECC events
Mark DMI events as read	Enter	Press Enter to mark all DMI events in the event log as read

4.1.2.5.7 Console Redirection

You can make the following selections on the Console Redirection Sub-Menu.

Feature	Options	Description
Com Port Address	On-board COMA On-Board COMB	If enabled, it will use a port on the motherboard. Install the VT100 jumper to use the Console Redirection.
Baud Rate	300, 1200, 2400, 9600, 19.2K, 38.4K, 57.6K, 115.2K	Enables the specified baud rate.
Console Type	PC ANSI VT-100	Enables the specified console type.
Flow Control	None XON/XOFF CTS/RTS	Enables Flow Control
Console connection	Direct Via modem	Indicate whether the console is connected directly to the system or a modem is used to connect.
Continue C.R. after POST	Off, On	Enables Console Redirection after OS has loaded.

4.1.2.6 Power Menu Selection

You can make the following selections on the Advanced Menu. Use the sub menus for other selections.

Feature	Options	Description
Intelligent System Monitoring	**This is a Sub-Menu, see section 4.1.2.6.1**	
Soft Off Support	**Enabled** **Disabled**	Enable this option to use the Power Button feature. (can set to enabled only on PCI990 rev 2)
After Power Failure	**Stay Off** **Last State** **Power ON**	[Stay Off] Keep the power off until the power button is pressed. [Last State] Restores the previous power state after power loss occurred. [Power On] Power On the system after power loss occurred. Note: Last State and Power On work only with battery.

4.1.2.6.1 Intelligent System Monitoring

You can make the following selections on the Intelligent System Monitoring Sub-Menu. Use the sub menus for other selections.

Feature	Options	Description
Intelligent System Monitoring	Disabled Enabled	Enables/Disables the Intelligent System Monitor device. When enabled, the system will monitor some system states such as temperature and power supplies.
Interrupt Generation	Disabled Enabled	Enables/Disables the generation of interrupts when an event occurs. This must be set to DISABLED when programs such as LANDesk® are loaded onto the system.
Chassis Intrusion	Disabled Enabled	Enables/Disables the detection of chassis intrusion.
Secured Chassis	Disabled Enabled	Controls the SECURE CHASSIS feature. If set to ENABLED and a chassis intrusion is detected, the user is required to enter SETUP and set the option "Reset chassis intrusion" to "Yes", before the system is allowed to complete the boot.
Reset Chassis Intrusion	No Yes	Selecting "Yes" will reset the chassis intrusion circuitry on the next boot.
Beep codes for non-thermal events	Disabled Enabled	Produces beep codes when the Intelligent System Monitoring events occur for either the chassis, the fan or the voltages. Codes are as follows: One long beep plus: 2 short beeps for chassis intrusion 3 short beeps for fan events 4 short beeps for voltage events This alarm may not be supported by the operating system.
Thermal Audio Alarm	Disabled Enabled	When the Thermal Management option and this option are enabled, a continuous audible alarm is sounded when the temperature specified in the Overheat Alarm options is reached. This alarm may not be supported by the operating system.
Hardware Monitor Temp. and Fans	**This is a Sub-Menu, see section 4.1.2.6.1.1**	
Hardware Monitor Voltage Inputs	**This is a Sub-Menu, see section 4.1.2.6.1.2**	

Intelligent System Monitoring (continued)

Feature	Options	Description
Hardware Monitor Temp. and Fans	**This is a Sub-Menu, see section 4.1.2.6.1.1**	
Hardware Monitor Voltage Inputs	**This is a Sub-Menu, see section 4.1.2.6.1.2**	

4.1.2.6.1.1 Hardware Monitor Temp. and Fans.

Feature	Options	Description
System board Temperature	**Displays a Status and limit set in other menu.**	
CPU 1 Die Temperature		
CPU 2 Die Temperature		
Fan CPU 1 (RPM)		
Fan CPU 2 (RPM)		
Fan Tach. 1 (RPM)		
Fan Tach. 2 (RPM)		
Fan Tach. 3 (RPM)		
Fan Tach. 4 (RPM)		
Fan Tach. 5 (RPM)		
Fan Tach. 6 (RPM)		

4.1.2.6.1.2 Hardware Monitor Voltage Input.

Feature	Options	Description
Vcore CPU 1	**Displays a Status and limit set in other menu.**	
Vcore CPU 2		
Vcc3 3.3V		
Vcc 5V		
Vin 2.5V		
Vtt		
Vbat		
Vin 12V		
Vin -12		
Term. Power SCSI A		
Term. Power SCSI B		

4.1.2.6.1.3 Control Temp. and Fan Events.

Feature	Options	Description
CPU 1 Temperature Interrupt	Enabled Disabled	This option enables Temperature events handling.
CPU 2 Temperature Interrupt	Enabled Disabled	This option enables Temperature events handling.
Resume Alarm (ºC)	10ºC to 70ºC with step of 4ºC	Full speed (Normal mode) will be resumed when the temperature comes down to the selected temperature.
Overheat Alarm (ºC)	30ºC to 90ºC with step of 4ºC	The CPU will be slowed down (Doze mode) When it reaches the selected temperature.
Shutdown Alarm (ºC)	60ºC to 95ºC with step of 5ºC	The CPU will be halted when it reaches the selected temperature. The system will have to be restarted.
Fan CPU 1 Interrupt	Enabled Disabled	This option enables Temperature events handling.
Fan CPU 2 Interrupt	Enabled Disabled	This option enables Temperature events handling.
Fan Tach. 1 Interrupt	Enabled Disabled	This option enables Temperature events handling.

Control Temp. and Fan Events (cont'd)

Feature	Options	Description
Fan Tach. 2 Interrupt	Enabled Disabled	This option enables Temperature events handling.
Fan Tach. 3 Interrupt	Enabled Disabled	This option enables Temperature events handling.
Fan Tach. 4 Interrupt	Enabled Disabled	This option enables Temperature events handling.
Fan Tach. 5 Interrupt	Enabled Disabled	This option enables Temperature events handling.
Fan Tach. 6 Interrupt	Enabled Disabled	This option enables Temperature events handling.

4.1.2.6.1.4 Control Voltage Events.

Feature	Options	Description
Vcore CPU 1 Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vcore CPU 2 Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vcc3 3.3V Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vcc 5V Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vin 2.5V Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vtt Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vbat Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vin 12V Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Vin -12 Voltage Interrupt	Enabled Disabled	This option enables Voltage events handling.
Term. Power SCSI A Voltage Int.	Enabled Disabled	This option enables Voltage events handling.
Term. Power SCSI B Voltage Int.	Enabled Disabled	This option enables Voltage events handling.

4.1.2.7 Boot Menu Selection

Feature	Options	Description
	Hard Drive Bootable Add-in Cards Primary Master Removable Devices Legacy Floppy Drives Hard Drive Bootable Add-in Cards * ATAPI CD-ROM Drive Network Boot	Keys used to view or configure devices: **<Enter>** expands or collapses devices with a **+** or **–** **<Ctrl+Enter>** expands all **<Shift + 1>** enables or disables a device **<+>** or **<->** moves the device up or down **<n>** May move removable device between Hard Disk or Removable Disk **<d>** Remove a device that is not installed. * Note : The hard drives and SCSI drives detected will be listed in this section and the first drive in the list will be the boot drive.

4.1.2.8 Exit Menu Selection

Feature	Options		Description
	Exit Saving Changes	Yes / No	**Exit Saving Changes** Setup and save your changes to CMOS.
	Exit Discarding Changes	Yes / No	**Exit Discarding Changes** Exit utility without saving Setup data to CMOS.
	Load Setup Defaults	Yes / No	**Load Setup Defaults** Exit utility without saving Setup data to CMOS.
	Discard Changes	Yes / No	**Load Setup Defaults** Load default values for all SETUP items.
	Saves Changes	Yes / No	**Discard Changes** Load previous values from CMOS for all SETUP items.
			Save Changes Save Setup Data to CMOS.

4.2 Boot Utilities

Phoenix Boot Utilities are : Phoenix QuietBoot™
Phoenix MultiBoot™

Phoenix QuietBoot displays a graphic illustration rather than the traditional POST messages while keeping you informed of diagnostic problems.

Phoenix MultiBoot is a boot screen that displays a selection of boot devices from which you can boot your operating system.

4.2.1 Phoenix Quiet Boot

Right after you turn on or reset the computer, Phoenix QuietBoot displays the QuietBoot Screen, a graphic illustration created by the computer manufacturer instead of the text-based POST screen, which displays a number of PC diagnostic messages.

To exit the QuietBoot screen and run Setup, display the Multiboot menu, or simply display the PC diagnostic messages, you can simply press one of the hot keys described below.

The QuietBoot Screen stays up until just before the operating system loads unless:

1. You press <ESC> to display the POST screen.
2. You press <Del> to enter Setup.
3. POST issues an error message.
4. The BIOS or an option ROM requests keyboard input.

The following explains each of these situations.

4.2.1.1 Press <ESC>

1. Pressing <ESC> switches the POST screen and The boot process continues with the text-based POST screen until the end of POST, and then displays the BootFirst Menu, with these options:
   a. Load the operating system from a boot device of your choice.
   b. Enter Setup.
   c. Exit the Boot First Menu (with <ESC>) and load the operating system from the boot devices in the order specified in Setup.

4.2.1.2 Press <Del>

Pressing < Del > at any time during POST enter Setup.

4.2.1.3 POST Error

Whenever POST detects a non-fatal error, QuietBoot switches to the POST screen and displays the errors. It then displays this message:

Press <F1> to resume, <Del> to Setup

Press <F1> to continue with the boot. Press <Del> if you want to correct the error in Setup.

4.2.1.4 Keyboard Input Request

If the BIOS or an Option ROM (add-on card) requests keyboard input, QuietBoot switches over to the POST screen and the Option ROM displays prompts for entering the information. POST continues from there with the regular POST screen.

4.2.2 Phoenix Multiboot

Phoenix Multiboot expands your boot options by letting you choose your boot device, which could be a hard disk, floppy disk, or CDROM. You can select your boot device in Setup, or you can choose a different device each time you boot during POST by selecting your boot device in **The Boot First Menu**.
Multiboot consist of :

The Setup Boot Menu
The Boot First Menu

4.3 Installing Drivers

4.3.1 Video Drivers

Various drivers are provided for different operating systems and software. To install a driver, refer to the Setup program located on the CD-ROM (provided with your board).

4.3.2 Ethernet Drivers

Various drivers are provided for different operating systems and software. To install a driver, use the Setup program and the ReadMe.bat file located on the CD-ROM (provided with your board).

4.3.3 Other Drivers

For other operating system drivers and installation instructions or for more information, contact Kontron's Technical Support department.

4.4 Console Redirection (VT100 Mode)

The VT100 operating mode allows remote setups of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

4.4.1 Requirements

The terminal should emulate a VT100 or ANSI terminal. Terminal emulation programs such as Telix© or Procom© can also be used.

4.4.2 Setup & Configuration

Follow these steps to set up the VT100 mode:

1. Connect a monitor and a keyboard to your board and turn on the power.
2. Enter into the CMOS Setup program in the "Advanced" page, "Console Redirection" menu.
3. Select the VT100 mode and the appropriate COM port and save your setup.
4. Connect the communications cable as shown in the next page.

> **NOTE**
>
> If you do not require a full cable for your terminal, you can set up a partial cable by using only the TxD and RxD lines. To ignore control lines simply loop them back as shown in VT100 Partial Setup cable diagram.

5. Configure your terminal to communicate using the same parameters as in CMOS Setup.
6. Install the VT100 jumper. Reboot the board.
7. Use the remote keyboard and display to setup the BIOS.

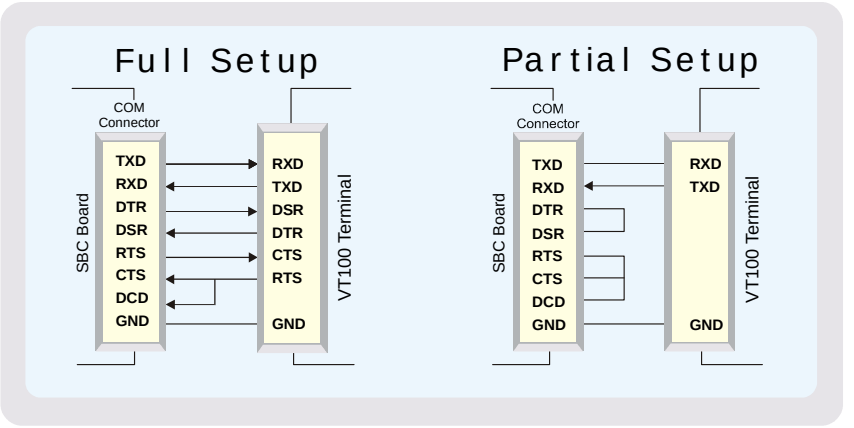
Save the setup, exit, and disconnect the remote computer from the board to operate in stand-alone configuration.

Console Redirection is done by refreshing the Video address @ B8000h at the selected BAUD rate. This means that a low baud rate refreshes the screen slowly, but the CPU time is maximized for the applications. A high BAUD rate refreshes the screen rapidly but the CPU is frequently interrupted by the Serial Port.

Console Redirection provided by Phoenix based BIOS offers various escape sequences to emulate keyboard function keys. The following table lists the escape sequences available.

Escape sequence	Function		Escape sequence	Function
Esc Del	Warm Reset		Esc [6 4 ~	(Ctrl-F1)
Esc O P	F1		Esc [6 5 ~	(Ctrl-F2)
Esc O Q	F2		Esc [6 6 ~	(Ctrl-F3)
Esc O R	F3		Esc [6 7 ~	(Ctrl-F4)
Esc O S	F4		Esc [6 8 ~	(Ctrl-F5)
Esc O w	F3		Esc [6 9 ~	(Ctrl-F6)
Esc O x	F4		Esc [7 0 ~	(Ctrl-F7)
Esc O t	F5		Esc [7 1 ~	(Ctrl-F8)
Esc O u	F6		Esc [7 2 ~	(Ctrl-F9)
Esc O q	F7		Esc [7 3 ~	(Ctrl-F10)
Esc O r	F8		Esc [7 4 ~	(Ctrl-F11)
Esc O p	F10		Esc [7 5 ~	(Ctrl-F12)

Setup & Configuration:



PART 5

APPENDICES

A. MEMORY & I/O MAPS

B. INTERRUPT LINES

C. BOARD DIAGRAMS

D. CONNECTOR PINOUTS

E. BIOS SETUP ERROR CODES

F. BIOS UPDATE & EMERGENCY PROCEDURE

G. GETTING HELP & RMA

A. MEMORY & I/O MAPS

A.1 MEMORY MAPPING

Address	Function
00000-9FFFF	0-640 KB DRAM
A0000-BFFFF	Video DRAM
C0000-C7FF	Video BIOS
C8000-DFFFF	Optional ROM (Free)
	LAN BIOS if activated, address may vary and size is not same for Gigabit Ethernet and 10/100.
	SCSI BIOS if activated, address may vary and size depend of installed SCSI drive
E0000-FFFFF	System BIOS
100000-Top of DRAM	Extended Memory

A.2 I/O MAPPING

Address	Optional Address	Optional Address	Optional Address	Function
000-01F				DMA Controller 1
020-03F				Interrupt Controller 1
040-05F				Timer
060-06F				Keyboard
070-07F				Real-time clock
080-09F				DMA Page Register
0A0-0BF				Interrupt Controller 2
0C0-0DF				DMA Controller 2
0F0-0F1, 0F8-0FF				Math Coprocessor
190-F	290-F	390-F		Kontron Control Port
1F0-1F7, 3F6				Primary IDE
3F0-3F7	370-377			Floppy Disk
378-37A	3BC-3BE	2787-27A		Parallel Port (LPT1 by default)
3F8-3FF (COM1)	2F8-2FF (COM2)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	3E8-3EF (COM3)	2E8-2EF (COM4)	Serial Port 2 (COM2 by default)
3C0-3CF, 3D0-3DF, 3B0-3BB				Graphics Controller (I2C Port)

B. IRQ AND DMA LINES

B.1 IRQ LINES

The board is fully PC compatible with interrupt steering for PCI plug and play compatibility.

Controller # 1		Controller # 2	
IRQ 0	Timer Output 0	IRQ 8	Real Time Clock
IRQ 1	Keyboard	IRQ 9	Available [1]
IRQ 2	Cascade Controller # 2	IRQ 10	Available [1]
IRQ 3*	Serial Port 2	IRQ 11	Available [1]
IRQ 4*	Serial Port 1	IRQ 12	PS/2 Mouse
IRQ 5*	Available [1]	IRQ 13	Coprocessor Error
IRQ 6*	Floppy Controller	IRQ 14	Primary IDE or available [1]
IRQ 7*	Parallel Port 1 or Available [1]	IRQ 15	secondary IDE or available [1]

* :All functions marked with an asterisk (*) can be disabled or reconfigured.

1 Available lines service on board and external PCI/ISA PnP devices or a Legacy ISA devices.

In addition to the standard ISA compatible interrupt controller (PIC) described above, the OSB4 Incorporates two Advanced Programmable Interrupt Controller (APIC). While the standard interrupt controller is intended for use in a single processor system (DOS mode), APIC can be used in either a single processor or multi-processor system (MPS or ACPI modes).

In IOAPIC mode the first IOAPIC control the standard PIC interrupt. (same as previous table). The second IOAPIC control the PCI interrupt.

Second APIC Controller (OSB4)			
PCIIRQ0	PCI VGA Interrupt	PCIIRQ8	PCI SCSIA Interrupt
PCIIRQ1	PCI LAN0 Interrupt	PCIIRQ9	PCI SCSIB Interrupt
PCIIRQ2	PCI LAN1 Interrupt	PCIIRQ10	PCI Interrupt A on Mezzanine[1]
PCIIRQ3	Not used	PCIIRQ11	PCI Interrupt B on Mezzanine[1]
PCIIRQ4	PCI Interrupt A[1]	PCIIRQ12	PCI Interrupt C on Mezzanine[1]
PCIIRQ5	PCI Interrupt B[1]	PCIIRQ13	PCI Interrupt D on Mezzanine[1]
PCIIRQ6	PCI Interrupt C[1]	PCIIRQ14	Not used
PCIIRQ7	PCI Interrupt D[1]	PCIIRQ15	Not Used

* :All functions marked with an asterisk (*) can be disabled or reconfigured.

1 Available lines service on board PCI devices.

B.2 DMA CHANNELS

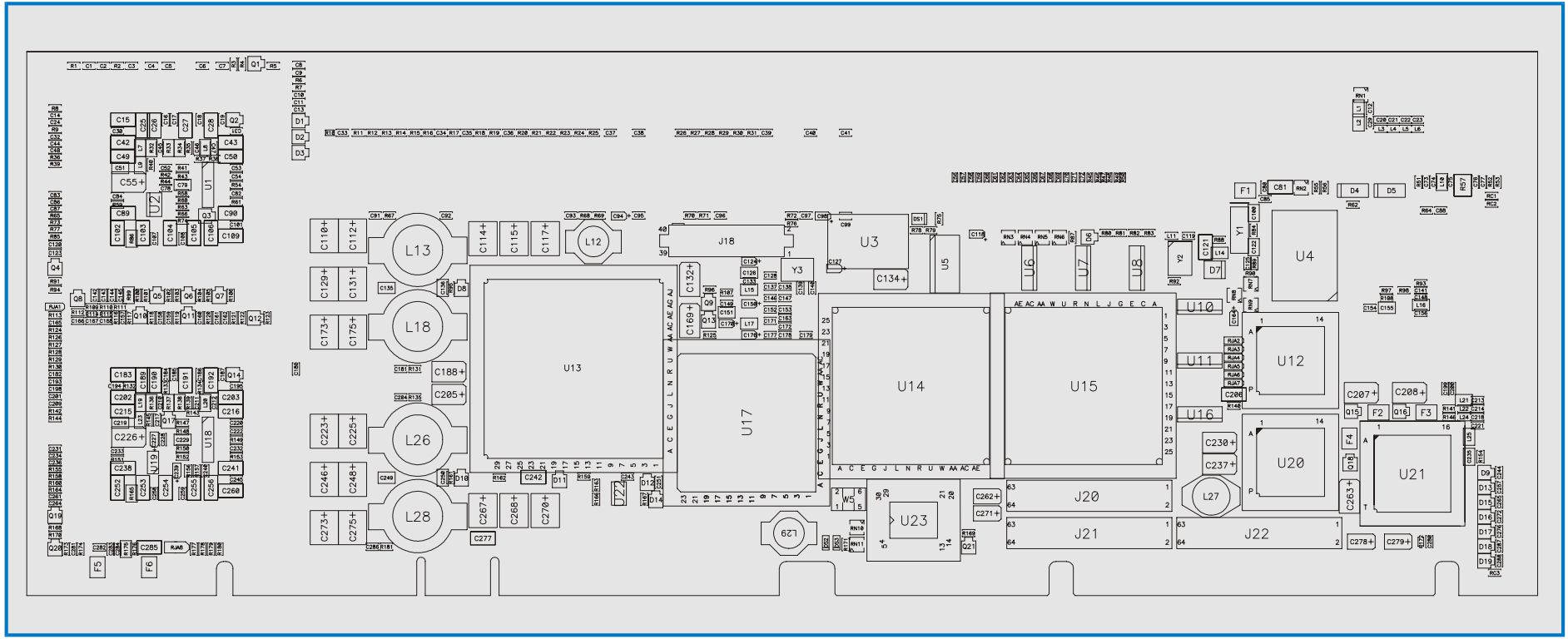
The PCI-990 integrates the functionality of two 8237 DMA controllers. Eight DMA channels are available.

According to Plug and Play standards, the system BIOS automatically allocates DMA Channel 1 or 3 for the parallel port's ECP mode. Channel 2 is reserved for the floppy controller and Channel 4 is used to cascade Channels 0 through 7 to the microprocessor.

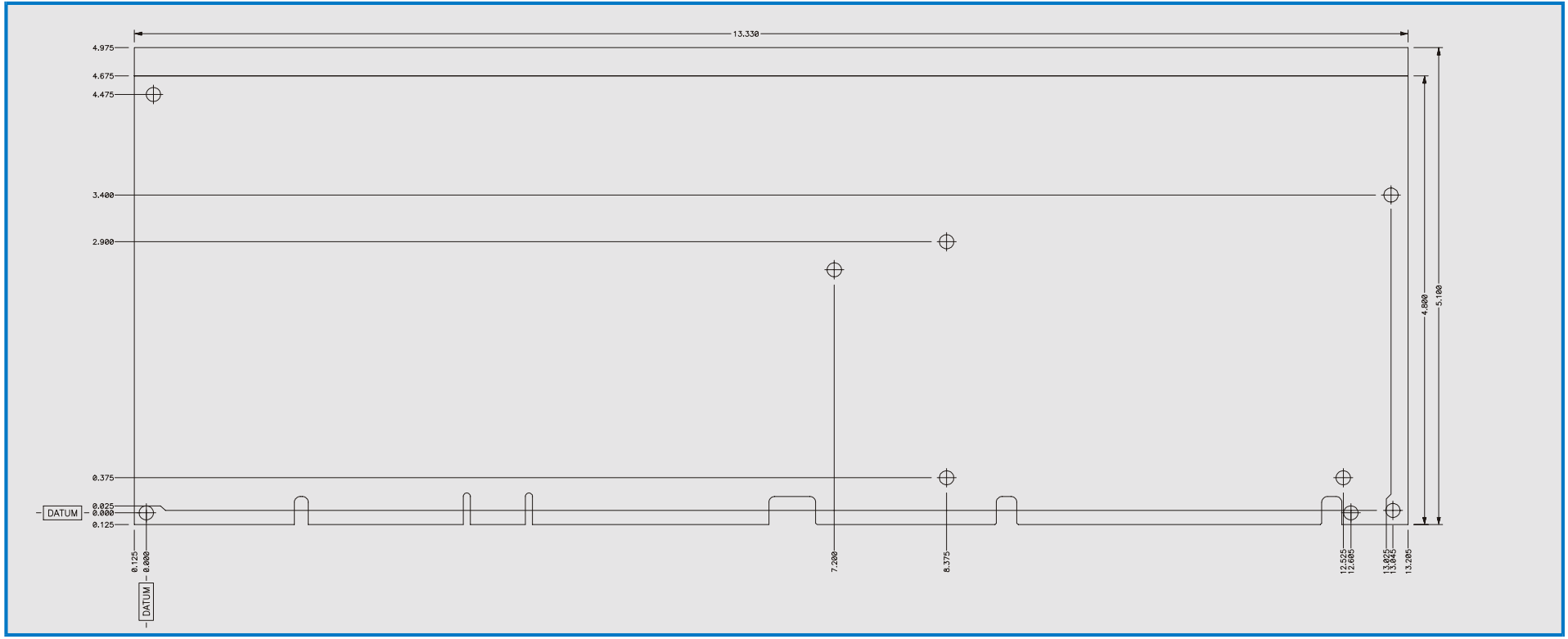
DMA Channel	Function
DMA 0	Available
DMA 1	PnP available (ECP)
DMA 2	Floppy controller
DMA 3	PnP available (ECP)
DMA 4	Cascade controller # 1
DMA 5	PnP available
DMA 6	PnP available
DMA 7	PnP available

C. BOARD DIAGRAMS

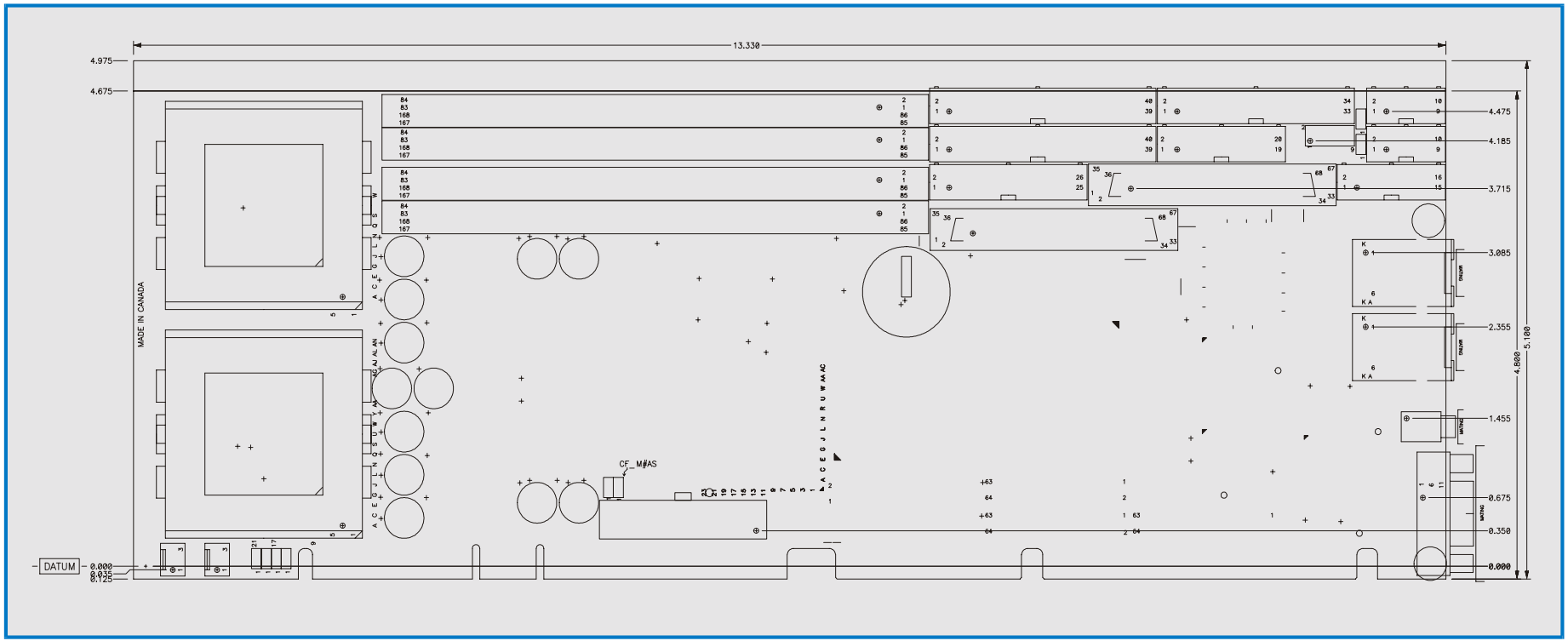
C.1 ASSEMBLY TOP DIAGRAM



C.2 MOUNTING HOLES



C.3 CONNECTOR MOUNTING HOLES



D. CONNECTOR PINOUTS

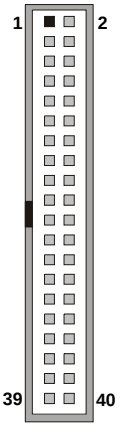
D.1 LIST OF CONNECTORS AND HEADERS

Connector	Description
J1-2-3-4	DIMM Memory
J5	EIDE Primary
J6	EIDE Secondary
J7	Parallel Port
J9	SCSI LVD Channel A
J8	SCSI LVD Channel B
J10	Floppy
J11	Hardware Monitor
J12	USB Port (header)
J13-14	Communication Ports COM 1 and COM 2
J15	Multi-Function
J17	Ethernet 10Base-T/100Base-TX – LAN0
J16	Ethernet 10Base-T/100Base-TX – LAN1
J18	CompactFlash disk
J19	External Power (ATX form factor)
J20-21-22	64-bit Mezzanine
J23	USB Port (faceplate)
J24	CRT VGA Interface
J26	CPU Fan 1
J25	CPU Fan 2

D.2 PRIMARY & SECONDARY EIDE CONNECTOR (J5 J6)

Pin Number	Signal
1	RST#
3	D7
5	D6
7	D5
9	D4
11	D3
13	D2
15	D1
17	D0
19	GND
21	RE
23	IOW#
25	IOR#
27	IORDY
29	DACK#
31	IRQ
33	A1
35	A0
37	CS0#
39	ACT#

Top View



Pin Number	Signal
2	GND
4	D8
6	D9
8	D10
10	D11
12	D12
14	D13
16	D14
18	D15
20	N.C.
22	GND
24	GND
26	GND
28	PRIMPDI
30	GND
32	N.C.
34	DIAG#
36	A2
38	CS1#
40	GND

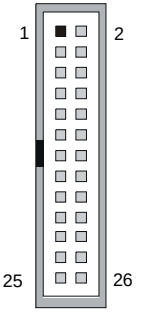
Active Low Signal

D.3 PARALLEL PORT CONNECTOR (J7)

Standard Mode

Pin Number	Signal
1	STB#
3	D0
5	D1
7	D2
9	D3
11	D4
13	D5
15	D6
17	D7
19	ACK#
21	BUSY
23	PE
25	SLCT

Top View



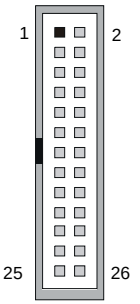
Pin Number	Signal
2	ALF#
4	ERR#
6	INIT#
8	SLCTIN#
10	GND
12	GND
14	GND
16	GND
18	GND
20	GND
22	GND
24	GND
26	GND

Active Low Signal

EPP Mode

Pin Number	Signal
1	WRITE#
3	PD0
5	PD1
7	PD2
9	PD3
11	PD4
13	PD5
15	PD6
17	PD7
19	INTR
21	WAIT#
23	N.C.
25	N.C.

Top View



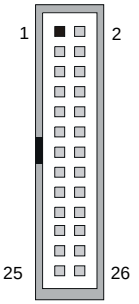
Pin Number	Signal
2	DATASTB#
4	N.C.
6	N.C.
8	ADDRSTRB#
10	GND
12	GND
14	GND
16	GND
18	GND
20	GND
22	GND
24	GND
26	GND

Active Low Signal

ECP Mode

Pin Number	Signal
1	STROBE#
3	PD0
5	PD1
7	PD2
9	PD3
11	PD4
13	PD5
15	PD6
17	PD7
19	ACK#
21	BUSY, PERIPHACK
23	PERROR, ACKREVERSE
25	SELECT

Top View



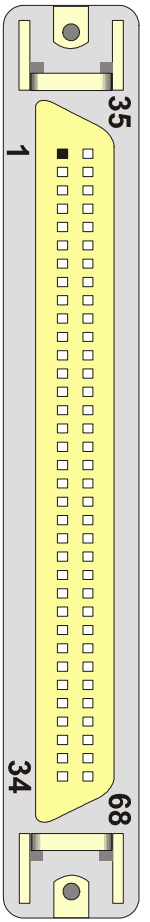
Pin Number	Signal	
	Compatible Mode	High Speed Mode
2	AUTOFD	HOSTACK
4	FAULT	PERIPHRQST
6	INIT	REVERSERQST
8	SELECTIN	SELECTIN
10	GND	
12	GND	
14	GND	
16	GND	
18	GND	
20	GND	
22	GND	
24	GND	
26	GND	

Active Low Signal,

D.4 SCSI LVD CHANNEL A,B (J9, J8)

Pin Number	Signal
1	D12+
2	D13+
3	D14+
4	D15+
5	DPH+
6	D0+
7	D1+
8	D2+
9	D3+
10	D4+
11	D5+
12	D6+
13	D7+
14	DPL+
15	GND
16	DIFFSENS
17	TERMPWR
18	TERMPWR
19	N.C.
20	GND
21	ATN+
22	GND
23	BSY+
24	ACK+
25	RESET+
26	MSG+
27	SEL+
28	CD+
29	REQ+
30	IO+
31	D8+
32	D9+
33	D10+
34	D11+

Top View



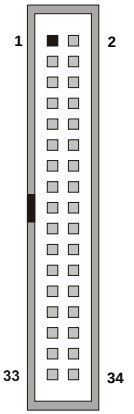
Pin Number	Signal
35	D12-
36	D13-
37	D14-
38	D15-
39	DPH-
30	D0-
41	D1-
42	D2-
43	D3-
44	D4-
45	D5-
46	D6-
47	D7-
48	DPL-
49	GND
50	GND
51	TERMPWR
52	TERMPWR
53	N.C.
54	GND
55	ATN-
56	GND
57	BSY-
58	ACK-
59	RESET-
60	MSG-
61	SEL-
62	CD-
63	REQ-
64	IO-
65	D8-
66	D9-
67	D10-
68	D11-

Active Low Signal

D.5 FLOPPY DRIVE CONNECTOR (J10)

Pin Number	Signal
1	GND
3	GND
5	GND
7	GND
9	GND
11	GND
13	GND
15	GND
17	N.C.
19	GND
21	GND
23	GND
25	GND
27	N.C.
29	FDETECT
31	GND
33	N.C.

Top View



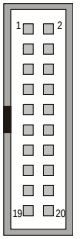
Pin Number	Signal
2	DENSEL #
4	N.C.
6	N.C
8	INDEX#
10	MTR0#
12	DSEL1#
14	DSEL0#
16	MTR1#
18	DIR#
20	STEP#
22	WDATA#
24	WGATE#
26	TRK0#
28	WRROT#
30	RDATA#
32	HDSEL#
34	DSKCHG#

Active Low Signal

D.6 HARDWARE MONITOR (J11)

Pin Number	Signal
1	GND
3	PS_ON
5	IPMB_SDA
7	VCCSB
9	EXTFLT#
11	FANFLT#
13	CHASINT#
15	FANTACH1
17	FANTACH3
19	FANTACH5

Top View



Pin Number	Signal
2	POWER BUTTON
4	GND
6	IPMB_SCL
8	CPUFLT#
10	GND
12	N.C.
14	GND
16	FANTACH2
18	FANTACH4
20	FANTACH6

Active Low Signal

D.7 USB HEADER (J12)

Pin Number		Top View	Pin Number	
Signal				Signal
USB0:VCC	1	1 2	2	USB1:VCC
USB0:DATA-	3		4	USB1:DATA-
USB0:DATA+	5		6	USB1:DATA+
USB0:GND	7		8	USB1:GND
Shield Ground	9	9 10	10	Shield Ground

D.8 COMMUNICATION PORTS COM 1 AND COM 2 (J13, J14)

Pin Number		Top View	Pin Number	
Signal				Signal
DCD	1	1 2	2	DSR
RXD	3		4	RTS
TXD	5		6	CTS
DTR	7		8	RI
GND	9	9 10	10	N.C.

Active Low Signal

D.9 SERIAL PORT 2 - (J14) RS-422/RS-485

Pin Number		Top View	Pin Number	
Signal				Signal
RSV	1	1 2	2	RSV
RX(-)	3		4	RX(+)
TX(-)	5		6	TX(+)
RSV	7		8	RSV
GND	9	9 10	10	N.C.

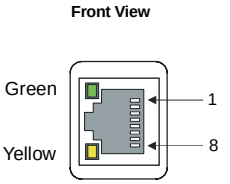
D.10 MULTI-FUNCTION CONNECTOR (J15)

Pin Number		Top View	Pin Number	
Signal				Signal
KB:CLK	1	1 2	2	GND
KB:DATA	3		4	GND
VCC	5		6	VCC
SPEAKER	7		8	VCC
MOUSE:CLK	9		10	GND
MOUSE:DATA	11		12	GND
PBRES#	13		14	GND
IDE:ACT#	15	15 16	16	VCC

Active Low Signal

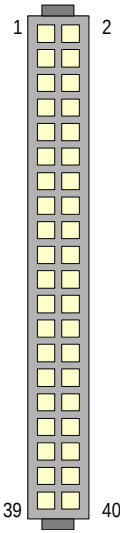
D.11 ETHERNET LAN0, LAN1 (J17, J16)

Signal	Pin Number
TX+	1
TX-	2
RX+	3
N.C.	4
N.C.	5
RX-	6
N.C.	7
N.C.	8



D.12 COMPACTFLASH™ (J18)

Signal	Pin Number
D11	1
D12	3
D13	5
D14	7
D15	9
CS1#	11
DMACK#	13
DMA RQ	15
PDIAG#	17
IRQ15	19
VCC	21
GND	23
RESET#	25
CSEL	27
A1	29
A0	31
D0	33
D1	35
D2	37
IOCS16#	39

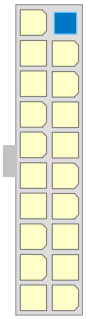


Pin Number	Signal
2	GND
4	D3
6	D4
8	D5
10	D6
12	D7
14	CS0#
16	DIOR#
18	DIOW#
20	VCC
22	VCC
24	GND
26	GND
28	A2
30	DASP#
32	IORDY
34	D8
36	D9
38	D10
40	GND

D.13 EXTERNAL POWER (ATX FORM FACTOR) (J19)

Pin Number Signal			Pin Number Signal
VCC3	11	1	VCC3
N.C.	12	2	VCC3
GND	13	3	GND
PS_ON#	14	4	VCC
GND	15	5	GND
GND	16	6	VCC
GND	17	7	GND
N.C.	18	8	PWROK
VCC	19	9	5VSB
VCC	20	10	12V

Top View

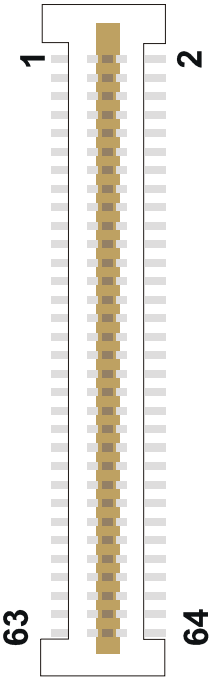


Active Low Signal,

D.14 64-BIT MEZZANINE (J20)

Pin Number	Signal
1	+12V
3	N.C.
5	TDI_BP
7	TMS_BP
9	GND
11	SMBDATA
13	IPMB0_SDA
15	PCIRST#
17	VCC3
19	AD30
21	AD24
23	EN_MEZZ_A
25	MEZZ_IDSELA
27	VCC3
29	AD18
31	PA64AD16
33	GND
35	TRDY#
37	GND
39	PERR#
41	VCC3
43	C/BE#1
45	AD14
47	MEZZ_IDSELB
49	AD8
51	AD7
53	VCC3
55	N.C.
57	M66EN
59	GND
61	N.C.
63	GND

Top View



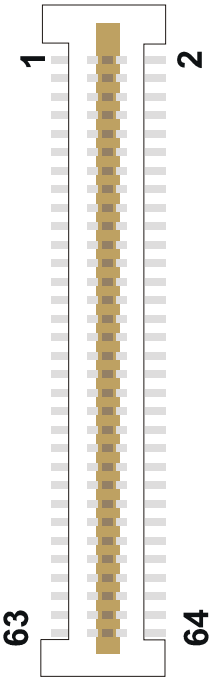
Pin Number	Signal
2	-12V
4	GND
6	TRST_BP#
8	TD0_BP
10	IPMB0_SCL
12	TCK_BP
14	EN_MEZZ_B
16	SMBCLK
18	GND
20	AD29
22	AD26
24	VCC
26	AD23
28	AD20
30	GND
32	C/BE#2
34	N.C.
36	VCC
38	STOP#
40	GND
42	SERR#
44	GND
46	AD13
48	AD10
50	VCC
52	N.C.
54	N.C.
56	GND
58	N.C.
60	MEZZ_RST#
62	VCC
64	GND

Active Low Signal

D.15 64-BIT MEZZANINE (J21)

Pin Number	Signal
1	GND
3	CLK_MEZZ1
5	GND
7	N.C.
9	VCC3
11	INTB_MEZZ#
13	INTD_MEZZ#
15	GND#_MEZZ1
17	REQ#_MEZZ1
19	VCC3
21	AD28
23	AD25
25	GND
27	AD22
29	AD19
31	VCC3
33	FRAME#
35	GND
37	DEVSEL#
39	GND
41	ACK64#
43	PAR
45	VCC3
47	AD12
49	AD9
51	GND
53	ADA6
55	AD4
57	VCC3
59	AD2
61	AD0
63	GND

Top View



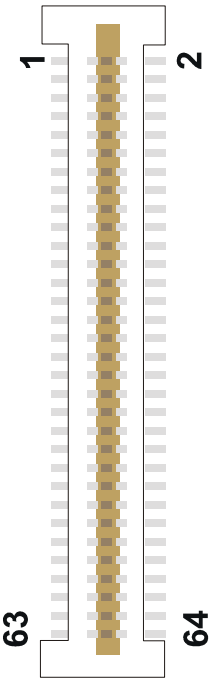
Pin Number	Signal
2	REQ#_MEZZ2
4	GND
6	CLK_MEZZ2
8	VCC
10	N.C.
12	GND
14	INTA_MEZZ#
16	INTC_MEZZ#
18	GNT#_MEZZ2
20	AD31
22	AD27
24	GND
26	C/BE#3
28	AD21
30	VCC
32	AD17
34	GND
36	IRDY#
38	VCC
40	CLOCK#
42	REQ64#
44	GND
46	AD15
48	AD11
50	VCC
52	C/BE#0
54	AD5
56	GND
58	AD3
60	AD1
62	VCC
64	N.C.

Active Low Signal

D.16 64-BIT MEZZANINE (J22)

Pin Number	Signal
AD32	1
GND	3
AD34	5
AD36	7
GND	9
AD38	11
AD40	13
GND	15
AD42	17
AD44	19
GND	21
AD46	23
AD48	25
GND	27
AD50	29
AD52	31
GND	33
AD54	35
AD56	37
GND	39
AD58	41
AD60	43
GND	45
AD62	47
PAR64	49
GND	51
C/BE#5	53
C/BE#7	55
GND	57
N.C.	59
N.C.	61
N.C.	63

Top View



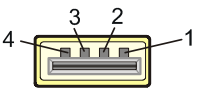
Pin Number	Signal
2	VIO
4	AD33
6	AD35
8	GND
10	AD37
12	AD39
14	GND
16	AD41
18	AD43
20	VCC3
22	AD45
24	AD47
26	GND
28	AD49
30	AD51
32	GND
34	AD53
36	AD55
38	VCC3
40	AD57
42	AD59
44	GND
46	AD61
48	AD63
50	VCC3
52	C/BE#4
54	C/BE#6
56	GND
58	N.C.
60	N.C.
62	N.C.
64	N.C.

Active Low Signal

D.17 USB CONNECTOR (J23)

Signal	Pin
USB2:VCC	1
USB2:DATA-	2
USB2:DATA+	3
USB2:GND	4

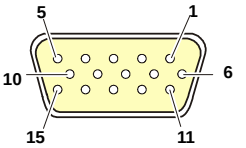
Front View



D.18 CRT VGA INTERFACE CONNECTOR (J24)

Pin Number Signal		Pin Number Signal		Pin Number Signal	
RED	1	Analog GND	6	N.C.	11
GREEN	2	Analog GND	7	SDATA	12
BLUE	3	Analog GND	8	HSYNC	13
N.C.	4	N.C.	9	VSYNC	14
GND	5	GND	10	SCLK	15

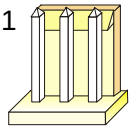
Front View



D.19 CPU1 AND CPU2 FAN AND TACHOMETER (J26, J25)

Pin #	Signal
1	Sense
2	+12V DC
3	GND

Front View



E. BIOS SETUP ERROR CODES

E.1 POST BEEP

Recoverable POST Errors
Whenever a recoverable error occurs during POST, *Phoenix* BIOS displays an error message describing the problem.
Phoenix BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (no card installed or faulty) or if an external ROM module does not properly checksum to zero.
An external ROM module (e. g. VGA) can also issue audible errors, usually consisting of one long tone followed by a series of short tones.

Terminal POST Errors
There are several POST routines that issue a **POST Terminal Error** and shut down the system if they fail. Before shutting down the system, the terminal error handler issues a beep code signifying the test point error, writes the error to port 80h, attempts to initialize the video, and writes the error in the upper left corner of the screen (using both mono and color adapters).
The routine derives the beep code from the test point error as follows:

1. The 8- bit error code is broken down to four 2- bit groups (Discard the most significant group if it is 00).
2. Each group is made one- based (1 through 4) by adding 1.
3. Short beeps are generated for the number in each group.

Example:
Testpoint 01Ah = 00 01 10 10 = 1- 2- 3- 3 beeps

Test Points and Beep Codes
At the beginning of each POST routine, the BIOS outputs the test point error code to I/ O address 80h. Use this code during trouble shooting to establish at what point the system failed and what routine was being performed.
If the BIOS detects a terminal error condition, it halts POST after issuing a terminal error beep code (See above) and attempting to display the error code on upper left corner of the screen and on the port 80h LED display.
If the system hangs before the BIOS can process the error, the value displayed at the port 80h is the last test performed. In this case, the screen does not display the error code.

E.2 POST MESSAGES

During the Power On Self Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

"PRESS F1 TO CONTINUE, DEL TO ENTER SETUP".

E.3 ERROR MESSAGES

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

CMOS BATTERY HAS FAILED

1. If it's the first boot, check for the onboard battery jumper W3. The board is shipped with W3 jumper set to OFF (onboard battery disconnected). This jumper must be shorted (ON) for proper battery operation.
2. CMOS battery is no longer functional. It should be replaced.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This indicates that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Floppy Drive A and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.
If you are purposely configuring the system without a keyboard, set the POST Errors halt condition in Setup to Disabled. This will cause BIOS to ignore all warning errors and continue the boot.

OFFENDING SEGMENT

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a Non Maskable Interrupt condition, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

PhoenixBIOS 4.0 Release 6.0 POST Tasks and Beep Codes

When you turn on or reset an IBM- compatible PC, the BIOS first performs a number of tasks, called the **Power- On- Self- Test** (**POST**). These tasks test and initialize the hardware and then boot the Operating System from the hard disk. At the beginning of each POST task, the BIOS outputs the **test- point error code** to I/ O port 80h. Programmers and technicians use this code during trouble shooting to establish at what point the system failed and what routine was being performed. Some motherboards are equipped with a seven-segment LED display that displays the current value of port 80h. For production boards which do not contain the LED display, you can purchase an installable "Port 80h" card that performs the same function. If the BIOS detects a terminal error condition, it issues a terminal- error beep code (See following), attempts to display the error code on upper left corner of the screen and on the port 80h LED display, and halts POST. It attempts repeatedly to write the error to the screen. This attempt may "hash" some CGA displays. If the system hangs before the BIOS can process the error, the value displayed at the port 80h is the last test performed. In this case, the screen does not display the error code.

Terminal POST Errors

There are several POST routines that require success to finish POST. If they fail, they issue a **POST Terminal Error** and shut down the system. Before shutting down the system, the error handler issues a beep code signifying the test point error, writes the error to port 80h, attempts to initialize the video, and writes the error in the upper left corner of the screen

(using both mono and color adapters). The routine derives the beep code from the test point error as follows:

1. The 8- bit error code is broken down to four 2- bit groups.
2. Each group is made one- based (1 through 4) by adding 1.
3. Short beeps are generated for the number in each group.

Example: **Testpoint 16h = 00 01 01 10 = 1- 2- 2- 3 beeps**

POST Task Routines

The following is a list of the Test Point codes written to port 80h at the start of each routine, the beep codes issued for terminal errors, and a description of the POST routine. Unless otherwise noted, these codes are valid for PhoenixBIOS 4.0 Release 6.0.

NOTE: The following routines are sorted by their test point numbers assigned in the BIOS code. Their actual order as executed during POST can be quite different.

02h Verify Real Mode	03h Disable Non- Maskable Interrupt (NMI)
04h Get CPU type	06h Initialize system hardware
08h Initialize chipset with initial POST values	09h Set IN POST flag
0Ah Initialize CPU registers	0Bh Enable CPU cache
0Ch Initialize caches to initial POST values	0Eh Initialize I/ O component
0Fh Initialize the local bus IDE	10h Initialize Power Management
11h Load alternate registers with initial POST values	12h Restore CPU control word during warm boot
13h Initialize PCI Bus Mastering devices	14h Initialize keyboard controller
16h 1- 2- 2- 3 BIOS ROM checksum	17h Initialize cache before memory autosize
18h 8254 timer initialization	1Ah 8237 DMA controller initialization
1Ch Reset Programmable Interrupt Controller	20h 1- 3- 1- 1 Test DRAM refresh
22h 1- 3- 1- 3 Test 8742 Keyboard Controller	24h Set ES segment register to 4 GB
26h Enable A20 line	28h Autosize DRAM
29h Initialize POST Memory Manager	2Ah Clear 512 KB base RAM
2Ch 1- 3- 4- 1 RAM failure on address line ***xxxx*** *	2Eh 1- 3- 4- 3 RAM failure on data bits ***xxxx*** * of low byte of memory bus
2Fh Enable cache before system BIOS shadow	30h 1- 4- 1- 1 RAM failure on data bits ***xxxx*** * of high byte of memory bus
32h Test CPU bus- clock frequency	33h Initialize Phoenix Dispatch Manager
36h Warm start shut down	38h Shadow system BIOS ROM
3Ah Autosize cache	3Ch Advanced configuration of chipset registers
3Dh Load alternate registers with CMOS values	42h Initialize interrupt vectors
45h POST device initialization	46h 2- 1- 2- 3 Check ROM copyright notice
48h Check video configuration against CMOS	49h Initialize PCI bus and devices
4Ah Initialize all video adapters in system	4Bh QuietBoot start (optional)

4Ch Shadow video BIOS ROM	4Eh Display BIOS copyright notice
50h Display CPU type and speed	51h Initialize EISA board
52h Test keyboard	54h Set key click if enabled
58h 2- 2- 3- 1 Test for unexpected interrupts	59h Initialize POST display service
5Ah Display prompt "Press F2 to enter SETUP"	5Bh Disable CPU cache
5Ch Test RAM between 512 and 640 KB	60h Test extended memory
62h Test extended memory address lines	64h Jump to UserPatch1
66h Configure advanced cache registers	67h Initialize Multi Processor APIC
68h Enable external and CPU caches	69h Setup System Management Mode (SMM) area
6Ah Display external L2 cache size	6Bh Load custom defaults (optional)
6Ch Display shadow- area message	6Eh Display possible high address for UMB recovery
70h Display error messages	72h Check for configuration errors
76h Check for keyboard errors	7Ch Set up hardware interrupt vectors
7Eh Initialize coprocessor if present	80h Disable onboard Super I/ O ports and IRQs
81h Late POST device initialization	82h Detect and install external RS232 ports
83h Configure non- MCD IDE controllers	84h Detect and install external parallel ports
85h Initialize PC- compatible PnP ISA devices	86h Re- initialize onboard I/ O ports.
87h Configure Motheboard Configurable Devices (optional)	88h Initialize BIOS Data Area
89h Enable Non- Maskable Interrupts (NMIs)	8Ah Initialize Extended BIOS Data Area
8Bh Test and initialize PS/ 2 mouse	8Ch Initialize floppy controller
8Fh Determine number of ATA drives (optional)	90h Initialize hard- disk controllers
91h Initialize local- bus hard- disk controllers	92h Jump to UserPatch2
93h Build MPTABLE for multi- processor boards	95h Install CD ROM for boot
96h Clear huge ES segment register	97h Fixup Multi Processor table
98h 1- 2 Search for option ROMs. One long, two short beeps on	checksum failure
99h Check for SMART Drive (optional)	9Ah Shadow option ROMs
9Ch Set up Power Management	9Dh Initialize security engine (optional)
9Eh Enable hardware interrupts	9Fh Determine number of ATA and SCSI drives
A0h Set time of day	A2h Check key lock
A4h Initialize Typematic rate	A8h Erase F2 prompt
AAh Scan for F2 key stroke	ACh Enter SETUP
AEh Clear Boot flag	B0h Check for errors
B2h POST done - prepare to boot operating system	B4h 1 One short beep before boot
B5h Terminate QuietBoot (optional)	B6h Check password (optional)
B9h Prepare Boot	BAh Initialize DMI parameters
BBh Initialize PnP Option ROMs	BCh Clear parity checkers
BDh Display MultiBoot menu	BEh Clear screen (optional)
BFh Check virus and backup reminders	C0h Try to boot with INT 19
C1h Initialize POST Error Manager (PEM)	C2h Initialize error logging
C3h Initialize error display function	C4h Initialize system error handler
C5h PnPnd dual CMOS (optional)	C6h Initialize notebook docking (optional)
C7h Initialize notebook docking late	C8h Force check (optional)
C9h Extended checksum (optional)	D2h Unknown interrupt
E0h Initialize the chipset	E1h Initialize the bridge
E2h Initialize the CPU	E3h Initialize system timer
E4h Initialize system I/ O	E5h Check force recovery boot

E6h Checksum BIOS ROM	E7h Go to BIOS
E8h Set Huge Segment	E9h Initialize Multi Processor
EAh Initialize OEM special code	EBh Initialize PIC and DMA
ECh Initialize Memory type	EDh Initialize Memory size
EEh Shadow Boot Block	EFh System memory test
F0h Initialize interrupt vectors	F1h Initialize Run Time Clock
F2h Initialize video	F3h Initialize System Management Mode
F4h 1 Output one beep before boot	F5h Boot to Mini DOS
F6h Clear Huge Segment	F7h Boot to Full DOS

* If the BIOS detects error 2C, 2E, or 30 (base 512K RAM error), it displays an additional word- bitmap (***xxxx***) indicating the address line or bits that failed. For example, "2C 0002" means address line 1 (bit one set) has failed. "2E 1020" means data bits 12 and 5 (bits 12 and 5 set) have failed in the lower 16 bits. Note that error 30 cannot occur on 386SX systems because they have a 16 rather than 32- bit bus. The BIOS also sends the bitmap to the port- 80 LED display. It first displays the check point code, followed by a delay, the high- order byte, another delay, and then the low- order byte of the error. It repeats this sequence continuously.

F. BIOS UPDATE & EMERGENCY PROCEDURE

BIOS UPDATE PROCEDURE

The BIOS update procedure can be found with the Emergency Recovery procedure on our ftp site: ftp://ftp.kontron.ca/Support in the FAQ section:

Download the FAQ# KC_0028 at location:

ftp://ftp.kontron.ca/Support/Support_FAQ - Questions & Answers/

EMERGENCY PROCEDURE

Symptoms:

- No POST code on a power up (when using a POST card).
- Board does not boot, even after usual hardware and connection verifications.
- At power up, there is floppy disk led activity, which is one sign that the BIOS as detected a corrupted BIOS CRC prior POST and falled back automatically to Emergency Recovery Mode looking for the floppy Emergency disk.

Please go on our FTP site in order to get the latest Emergency Recovery BIOS for that specific product.

BIOS maybe found at: Ftp://Ftp.Kontron.ca/Support/BIOS_Emergency/

Emergency Recovery Procedure is included within the Zip file of the Emergency BIOS to download. Latest Emergency Recovery procedure can be found on the FAQ section of the FTP site under FAQ # KC_0028 at location:

ftp://ftp.kontron.ca/Support/Support_FAQ - Questions & Answers/

G. GETTING HELP

At Kontron, we take great pride in our customer's successes. We strongly believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, you may contact our Technical Support department at:

CANADIAN HEADQUARTERS
Tel. (450) 437-5682
Fax: (450) 437-8053

If you have any questions about Kontron, our products or services, you can visit our web site at : http://www.kontron.com/ or you can write at the following address:

Kontron Canada Inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

LIMITED WARRANTY

Kontron Inc., ("The seller") warrants its boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts, which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

H. RETURNING DEFECTIVE MERCHANDISE

If your Kontron product malfunctions, please do the following before returning any merchandise:

1) Call our Technical Support department in Canada at (450) 437-5682. Make certain you have the following at hand:

   - The Kontron invoice number
   - Your purchase order number
   - The serial number of the defective board.

2) Give the serial number found on the back of the board and explain the nature of your problem to a service technician.

3) If the problem cannot be solved over the telephone, the technician will further instruct you on the return procedure.

4) Prior to returning any merchandise, make certain you receive an RMA number from Kontron's Technical Support and clearly mark this number on the outside of the package you are returning. To request a number, follow these steps:

   - Make a copy of the request form on the following page.
   - Fill out the form and be as specific as you can about the board's problem.
   - Fax it to us.

5) When returning goods, please include the name and telephone number of a person whom we can contact for further explanations if necessary. Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.

6) When returning a Kontron board:

   i) Make certain that the board is properly packed: Place it in an antistatic plastic bag and pack it in a rigid cardboard box.

   ii) Ship prepaid to (but not insured, since incoming units are insured by Kontron):

Kontron Canada Inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

RETURN TO MANUFACTURER AUTHORIZATION REQUEST

Contact Name : _____

Company Name : _____

Street Address : _____

City : _____ Province/State: _____

Country : _____ Postal/Zip Code: _____

Phone Number : _____ Extension : _____

Fax Number : _____

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

Fax this form to Kontron's Technical Support department in Canada at (450) 437-8053