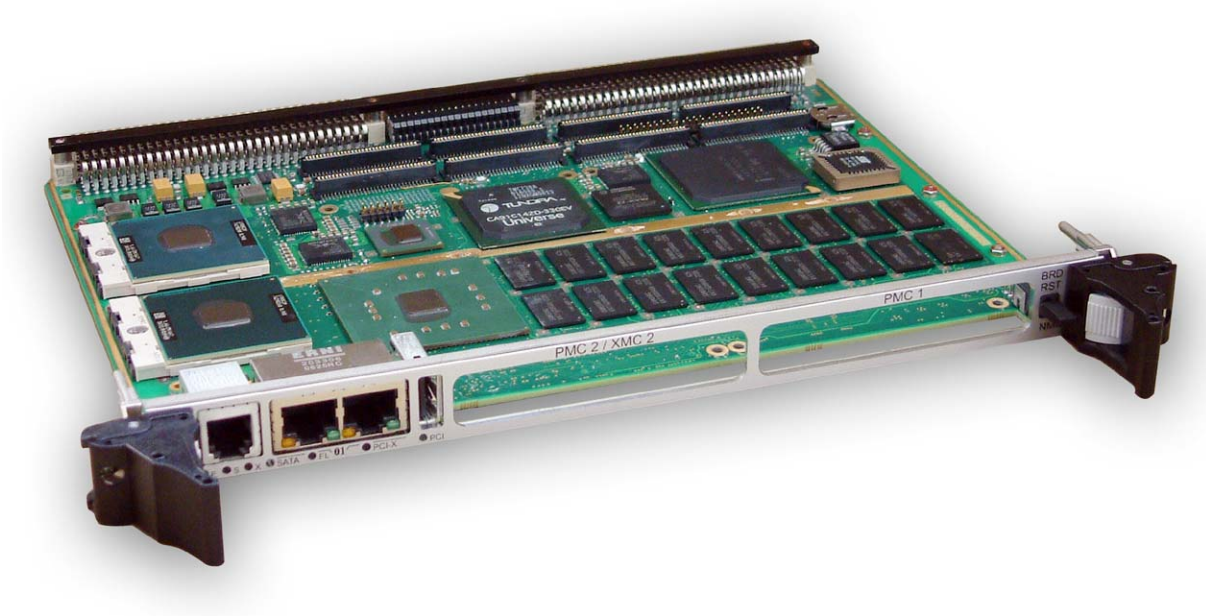
» PENTXM2 or PENTXM4 «



User's Guide

CA.DT.A07-10e - October 2010

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Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Environmental protection is a high priority with Kontron.

Kontron follows the DEEE/WEEE directive.

You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- reduce waste arising from electrical and electronic equipment (EEE)
- make producers of EEE responsible for the environmental impact of their products, especially when they become waste
- encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- improve the environmental performance of all those involved during the lifecycle of EEE

Conventions

This guide uses several types of notice: Note, Caution, ESD.

Note: this notice calls attention to important features or instructions.


Caution: this notice alert you to system damage, loss of data, or risk of personal injury.


ESD: This banner indicates an Electrostatic Sensitive Device.

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix `0x' shows a hexadecimal number, following the `C' programming language convention.

The multipliers `k', `M' and `G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when `K', `M' and `G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

When describing transfer rates, `k' `M' and `G' mean $*10^3$, $*10^6$ and $*10^9$ *not $*2^{10}$ $*2^{20}$ and $*2^{30}$.*

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and CompactPCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Signal names ending with an asterisk (*) or a hash (#) denote active low signals; all other signals are active high.

Signal names follow the PICMG 2.0 R3.0 CompactPCI Specification and the PCI Local Bus 2.3 Specification.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions


Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.


Caution, Electric Shock!
Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

Personal Injury

Be careful while handling the board, because of the cutting edges of the CPU heatsink.

Do not touch the CPU heatsink or the ruggedizer while removing the board from a rack because it can get very hot.

Do not place the board on any surface or in any form of storage container until the board and its heatsink have cooled down to room temperature.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Chapter 1 - Introduction

The Kontron PENTXM2 or PENTXM4 family of single-board computers (SBCs) uses the latest Low Power Dual-Core Intel® Xeon® processor and the Intel E7520 server class Memory Controller Hub. It offers high speed, server-class performance for advanced embedded applications. The single slot PENTXM2 or PENTXM4 SBCs is ideal for thermally constrained environments and includes all the up to date I/O standard interfaces required in a server blade PC.

Furthermore, the PENTXM2 or PENTXM4 product supports the Intelligent Platform Management Interface (IPMI) specification for easy integration in complex systems.

The Kontron PENTXM2 or PENTXM4 is therefore ideal for bandwidth intensive applications both in a standalone or in a complex cluster configuration.

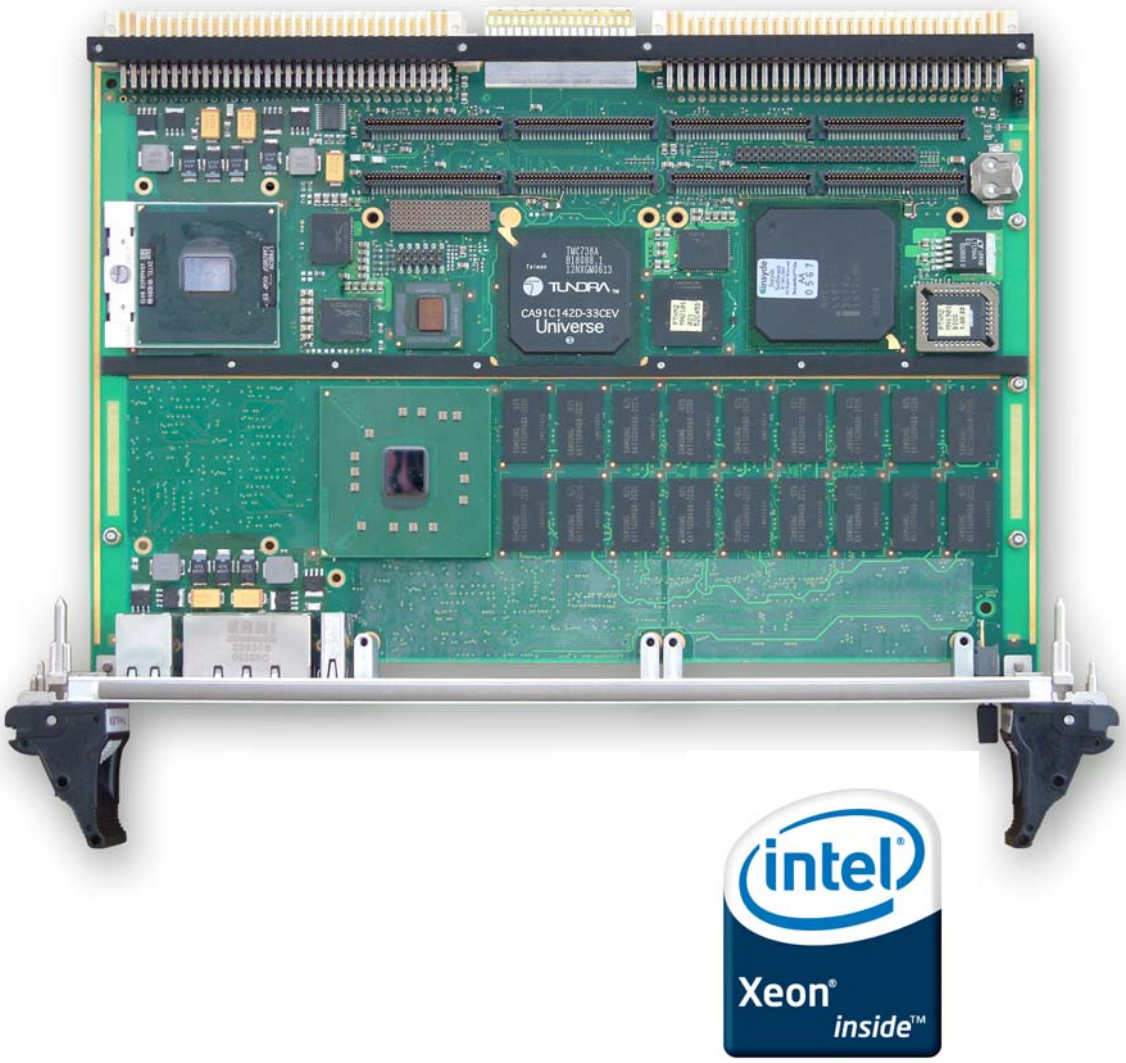


Figure 1: PENTXM2 Overview

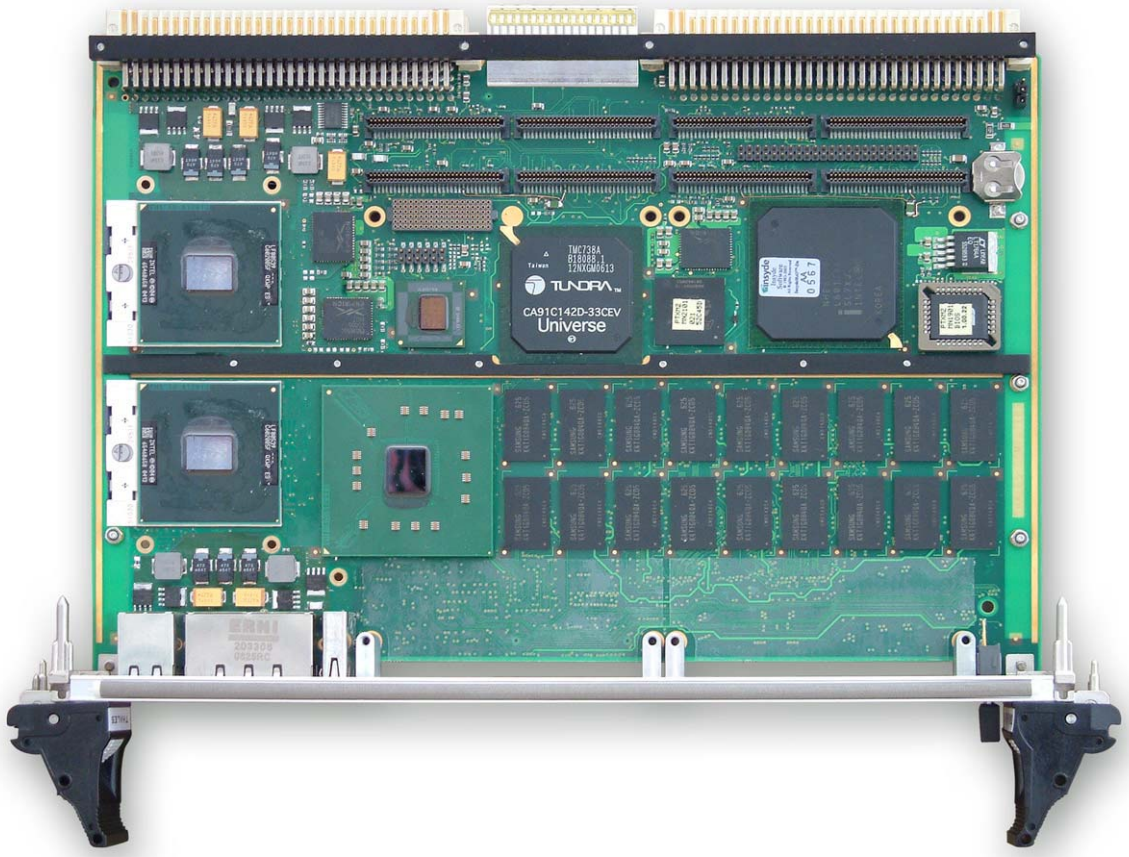


Figure 2: PENTXM4 Overview

1.1 Objectives

This guide provides general information, hardware preparation and installation instructions, operating instructions, and a functional description of the PENTXM2 or PENTXM4 board. The onboard programming, and other firmware (e.g. drivers and BSPs) are described in detail in separate guides.

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

This document applies to Kontron PENTXM2 or PENTXM4 boards.

The main differencence between a PENTXM2 and a PENTXM4 boards are:

PENTXM2	PENTXM4
Processor: One 1.67 GHz Dual-Core Intel Xeon ULV Processor	**Processor:** Two 1.67 GHz Dual-Core Intel Xeon ULV Processors

1.2 Audience

This manual is a guide and reference handbook for engineers and system integrators who wish to use Kontron's PENTXM2 or PENTXM4 single board computer. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, systems, cabling, grounding, VME, and communications. There is a glossary provided at the back of this guide that explains some of the terms used and expands all abbreviations.

1.3 Scope

This guide describes all variations of the PENTXM2 or PENTXM4. It does not cover the PENTXM2 or PENTXM4 transition modules, which are described in a separate guide: PENTXM2 or PENTXM4 Connection Guide.

1.4 Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with a brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- Chapter 1 (this chapter) - Brief introduction, this guide's objectives and audience, the structure, some warnings, conventions, and related documentation
- Chapter 2 - General Information
- Chapter 3 - Preparing Before Using
- Chapter 4 - Functional Description
- Chapter 5 - Hardware Configuration
- Chapter 6 - Connectors
- Chapter 7 - PMC Sites
- Chapter 8 - System Installation
- Chapter 9 - Operating Instructions
- Chapter 10 - BIOS Firmware
- Appendix A - Specifications

A glossary is also provided.

1.5 Related Documents

Hardware

- PENTXM2 or PENTXM4 Hardware Release Notes CA.DT.A09
- PENTXM2 or PENTXM4 Connection Guide CA.DT.A10
- PENTXM2/RC or PENTXM4/RC Supplement User's Guide CA.DT.A08
- PENTXM2/RA supplement User's Guide CA.DT.A72
- V2PMC2 - Dual Slots PCI-X/PMC VME Carrier - User's Guide CA.DT.A11

Software

- InsydeH2O Firmware for PENTXM2 and PENTXM4 - User Reference Manual SD.DT.E86
- PENTXM2 and PENTXM4 XBIT V2.xx User's Guide SD.DT.E90
- PENTXM2 and PENTXM4 IPMI BMC User Manual SD.DT.F12
- Release Notes RHEL5.2 for PENTXM2 and PENTXM4 Boards SD.DT.F34
- Release Notes RHEL5 for PENTXM2 and PENTXM4 Boards SD.DT.F28
- Release Notes RHEL4 for PENTXM2 and PENTXM4 Boards SD.DT.E82
- Release Notes Windows XP on PENTXM2 and PENTXM4 Boards SD.DT.F39

Standard

The following references will be used for the hardware design of the PENTXM2 or PENTXM4

- PCI Local Bus Specification Revision 2.2 December 18, 1998, PCI Special Interest Group.
- PCI System Design Guide Rev 1.0 9/93, PCI Special Interest Group.
- PCI to PCI Architecture Bridge Specification, rev. 1.1.
- VITA 35-199x PMC-P4 Pin Out Mapping to VME-P0 and VME64x-P2 Draft 0.4 September 19, 1999.
- VITA 42.0-2005 XMC Switched Mezzanine Card Auxiliary Standard, September 2005.
- VITA 42.3-200x XMC PCI Express Protocol Layer Standard, July 2004.
- ANSI/VITA 1-1994 VMEbus standard.
- ANSI/VITA 1.1 - 1997 VME64 Extensions Standard.
- IEEE P1386 Common Mezzanine Card Family: CMC.
- IEEE P1386.1 Physical/Environmental layer for PCI Mezzanine Cards: PMC.
- IEEE 1101-2 IEEE Standard for Mechanical Core Specifications for Conduction cooled Eurocard.
- IEC 61076-4-101 International Standard - Connectors for Electronic Equipment.

Board Components

- Intel E7520 Memory Controller Hub (MCH) Datasheet, reference 303006-002
- Intel 6300ESB I/O Controller Hub Datasheet, reference 300641-003
- Intel 82571EB/82572 Gigabit Ethernet Controller Datasheet
- Universe II™, VME-to-PCI Bus Bridge Manual, User Manual, reference 80A3010_MA001_03

1.6 World Wide Web Sites

Kontron on the world wide web site is available at http://www.kontron.com.

Manufacturers of many of the devices used on the PENTXM2 or PENTXM4 maintain world wide web sites. Useful sites:

- http://www.intel.com
- http://www.tundra.com

Chapter 2 - General Information

2.1 Overview

This chapter contains general information for the PENTXM2 or PENTXM4 product.

Chapter 4 gives a functional description, while detailing the main components of the board.

Ordering Information

Article	Part. Number	Description
Standard Air-Cooled Build		Dual-Core Intel Xeon @ 1.67 GHz
PENTXM2	PENTXM2-SA36S-10N00	2 GB DDR2-SDRAM - No User Flash Disk
PENTXM2	PENTXM2-SA34S-10N00	1 GB DDR2-SDRAM - No User Flash Disk
PENTXM2	PENTXM2-SA34S-10000	1 GB DDR2-SDRAM - 4 GB User Flash Disk
PENTXM2	PENTXM2-SA36S-10000	2 GB DDR2-SDRAM - 4 GB User Flash Disk
PENTXM2	PENTXM2-SA36S-11000	2 GB DDR2-SDRAM - 4 GB User Flash Disk - VITA 38 IPMI Management
PENTXM2	PENTXM2-SA36S-10000V	2 GB DDR2-SDRAM - 4 GB User Flash Disk - Conformal Coating
PENTXM2	PENTXM2-SA38S-10000	4 GB DDR2-SDRAM - 4 GB User Flash Disk
Rugged Air-Cooled Build		Dual-Core Intel Xeon @ 1.67 GHz
PENTXM2	PENTXM2-RA34S-10000	1 GB DDR2-SDRAM - 4 GB User Flash Disk
PENTXM2	PENTXM2-RA36S-10000	2 GB DDR2-SDRAM - 4 GB User Flash Disk
Rugged Conduction-Cooled Build		
PENTXM2	PENTXM2-RC34S-10000	1 GB DDR2-SDRAM - 4 GB User Flash Disk
PENTXM2	PENTXM2-RC36S-10000	2 GB DDR2-SDRAM - 4 GB User Flash Disk
Associated Products		
RTM	PBV36-P0-PTXM2-00	VITA 36 RTM - Standard Air-Cooled Build
RTM	PBV36-P0-PTXM2-00V	VITA 36 RTM - Standard Air-Cooled Build - Conformal Coating
Carrier Board	V2PMC2-SA-010	Dual PMC Carrier - Standard Air-Cooled Build
Carrier Board	V2PMC2-SA-010V	Dual PMC Carrier - Standard Air-Cooled Build - Conformal Coating
Carrier Board	V2PMC2-RC-010	Dual PMC Carrier - Rugged Conduction-Cooled Build
Kit Disk	KIT-DISK-PTXM2	IDE HDD onboard mounting kit
Kit Disk	ICHD-PENTXM2-080	80 GB 2.5" HDD and 2.5" IDE HDD onboard mounting kit
Kit Cable	KIT-PENTXM2-RJ12DB9	RJ12 to DB9 adaptor and RJ12-RJ12 cable
Kit PMC	KIT-RIB-PMC1	VITA 20 compliant thermal interface for Conduction-Cooled PMC

Table 1: PENTXM2 and Associated Products Ordering Information

Article	Part. Number	Description
Standard Air-Cooled Build		Twin Dual-Core Intel Xeon @ 1.67 GHz
PENTXM4	PENTXM4-SA36S-10000	2 GB DDR2-SDRAM - 4 GB User Flash Disk
PENTXM4	PENTXM4-SA36S-11000	2 GB DDR2-SDRAM - 4 GB User Flash Disk - VITA 38 IPMI Management
PENTXM4	PENTXM4-SA38S-10000	4 GB DDR2-SDRAM - 4 GB User Flash Disk
PENTXM4	PENTXM4-SA38S-11000	4 GB DDR2-SDRAM - 4 GB User Flash Disk - VITA 38 IPMI Management
PENTXM4	PENTXM4-SA38S-11000V	4 GB DDR2-SDRAM - 4 GB User Flash Disk - VITA 38 IPMI Management - Conformal Coating
Rugged Conduction-Cooled Build		
PENTXM4	PENTXM4-RC38S-10000	4 GB DDR2-SDRAM - 4 GB User Flash Disk
Associated Products		
RTM	PBV36-P0-PTXM2-00	VITA 36 RTM - Standard Air-Cooled Build
RTM	PBV36-P0-PTXM2-00V	VITA 36 RTM - Standard Air-Cooled Build - Conformal Coating
Carrier Board	V2PMC2-SA-010	Dual PMC Carrier - Standard Air-Cooled Build
Carrier Board	V2PMC2-SA-010V	Dual PMC Carrier - Standard Air-Cooled Build - Conformal Coating
Carrier Board	V2PMC2-RC-010	Dual PMC Carrier - Rugged Conduction-Cooled Build
Kit Disk	KIT-DISK-PTXM2	IDE HDD onboard mounting kit
Kit Disk	ICHD-PENTXM2-080	80 GB 2.5" HDD and 2.5" IDE HDD onboard mounting kit
Kit Cable	KIT-PENTXM2-RJ12DB9	RJ12 to DB9 adaptor and RJ12-RJ12 cable
Kit PMC	KIT-RIB-PMC1	VITA 20 compliant thermal interface for Conduction-Cooled PMC

Table 2: PENTXM4 and Associated Products Ordering Information

Simplified Block Diagram

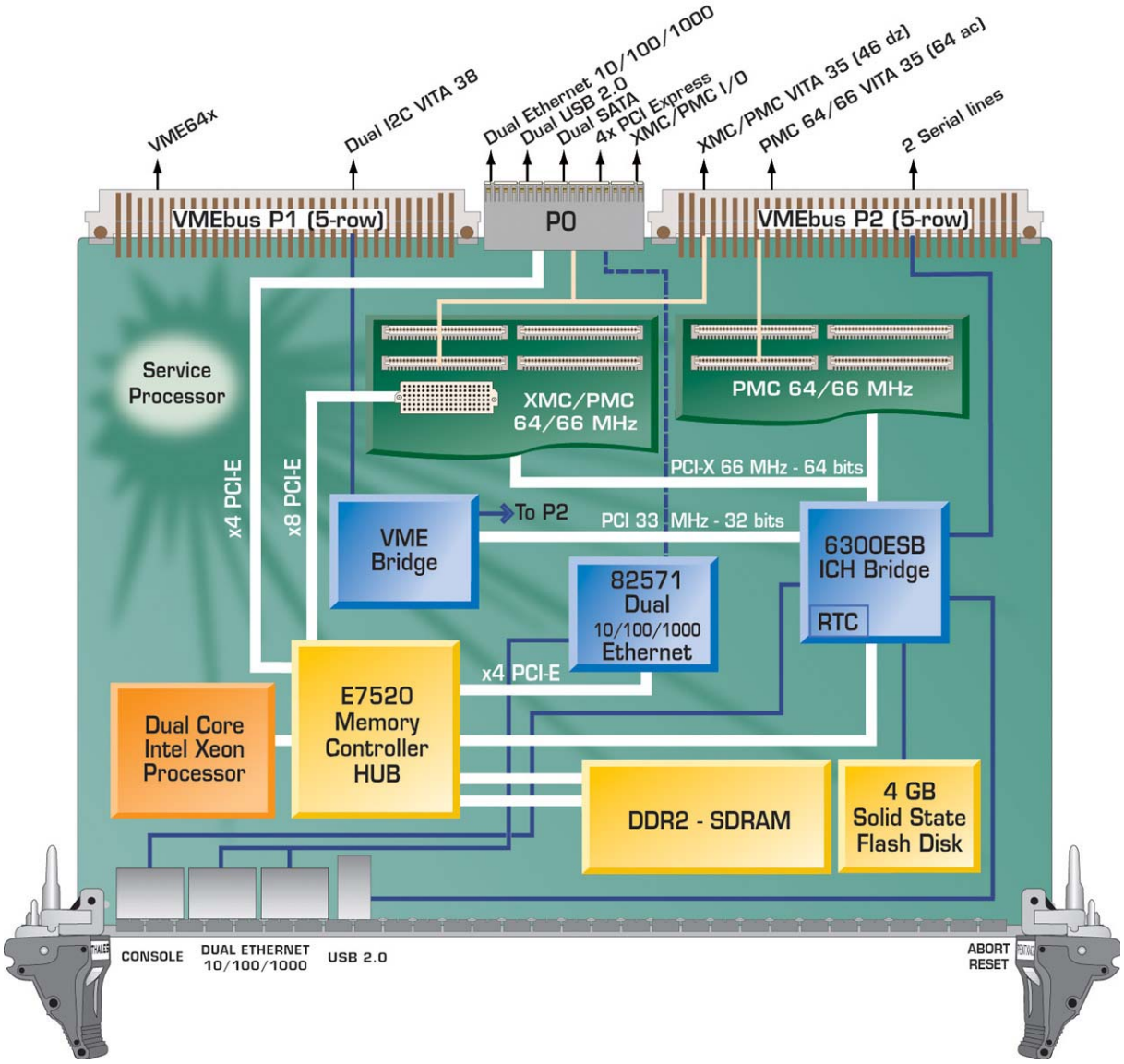


Figure 3: PENTXM2 Simplified Block Diagram

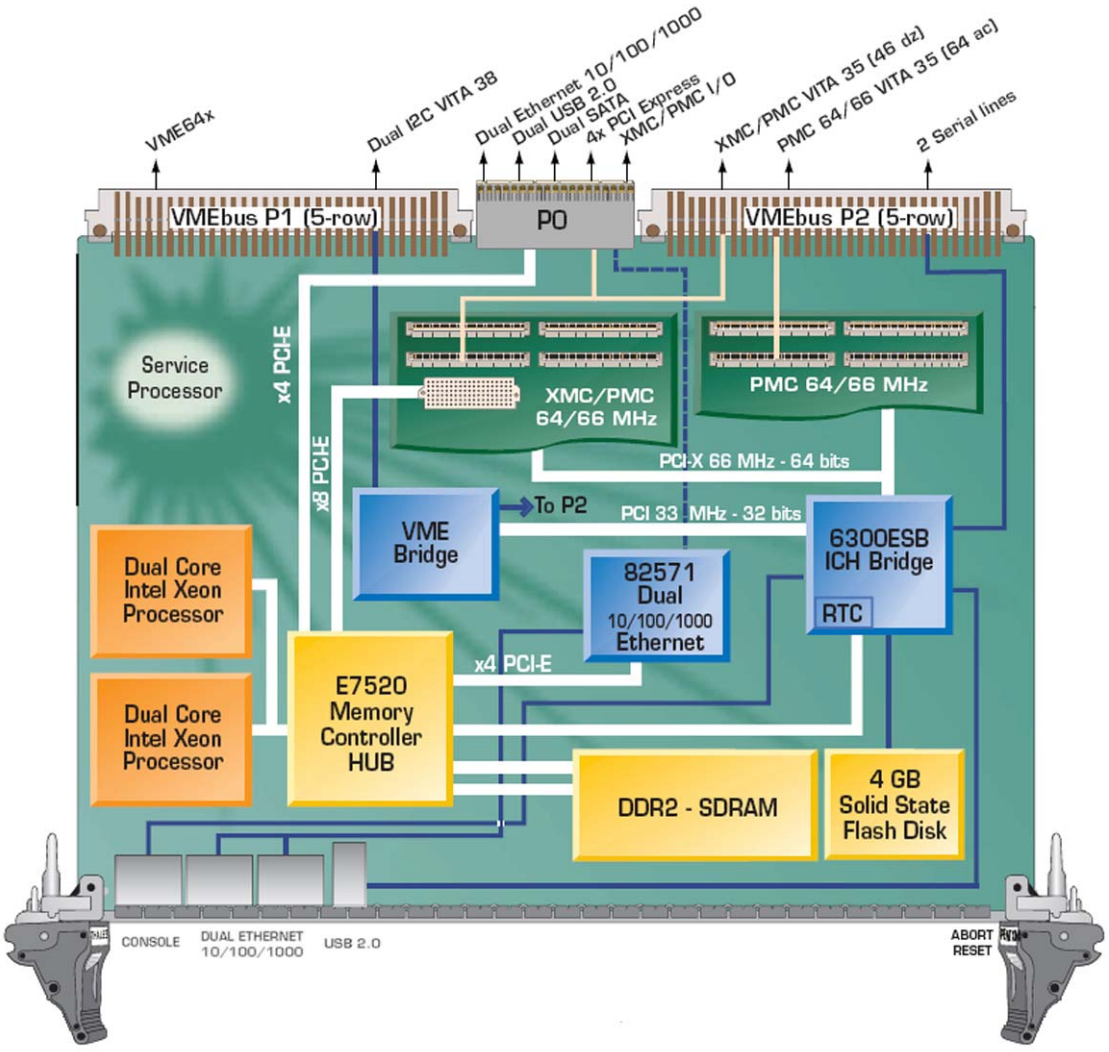


Figure 4: PENTXM4 Simplified Block Diagram

2.2 Main Features

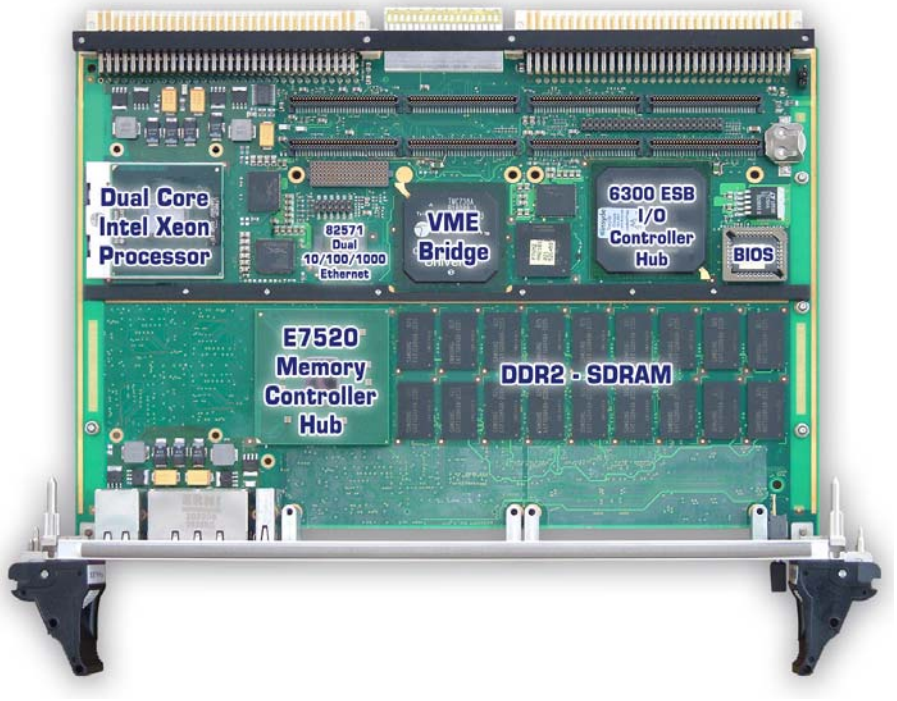


Figure 5: PENTXM2 Board Layout

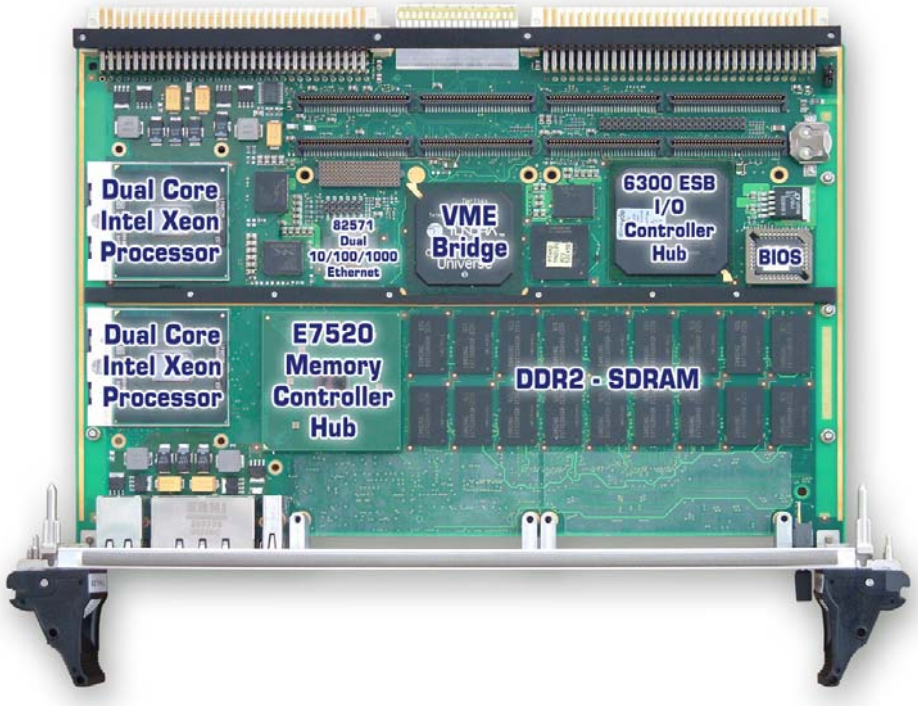


Figure 6: PENTXM4 Board Layout

Dual-Core Intel Xeon Processor

- Low voltage (LV) Dual-Core Intel Xeon Processor.
- One thread per core.
- Upwardly code-compatible with x86 family microprocessors.
- Integrate 2 MB L2 cache.
- 1.67 GHz max. processor frequency.
- Software control of the operating frequency.
- 667 MHz Front Side Bus.

Memory Controller Hub (E7520 MCH)

- Supplied by the Intel E7520 Server Class MCH
- Two channels of DDR2 SDRAM memory.
- Support of ECC memory.
- Peak bandwidth of each DDR2 branch channel: 3.2 GB/s with DDR2 400.
- One x8 PCI -Express XMC-E7520 MCH interface (maximal theorical bandwidth of 4 GB/s).
- One x4 PCI -Express P0-E7520 MCH interface (maximal theorical bandwidth of 2 GB/s).
- One x4 PCI -Express Gigabit Ethernet Controller-E7520 MCH interface.

DDR2 SDRAM memory

- 1, 2 or 4 GB of DDR2 SDRAM clocked at 400 MHz with ECC.

User Flash

- Depending on the Manufacturing Option: `User Flash Disk`, either 4 GB of User NAND-Flash on the secondary EIDE interface or no User Flash are available. Refer to 2.1 “Overview” section “Ordering Information" page 6.

I/O Controller Hub (6300ESB)

- Supplied by the Intel 6300ESB ICH.
- Three timer/counters which have fixed uses.
- Watchdog timer facility.

Serial ATA (SATA-150) interfaces

- Two independents serial ATA interfaces are provides, both of which route to the P0 connector. Each interface is supported by its own DMA controller.

USB Ports

- Three USB 2.0 interfaces are provided on the board by the 6300ESB.
- All channels can operate at 1.5 Mb/s, 12 Mb/s or 480 Mb/s.
- One channel is available on the front panel connector, two channels are connected to the P0 connector.

Dual Gigabit Ethernet Ports

- Supplied by the Intel 82571EB Gigabit Ethernet controller
- x4 PCI-Express Gigabit Ethernet Controller-MCH interface
- 10/100/1000 Mb/s
- Each port is software configurable either on front panel (RJ-45) or on rear P0.
- The P0 Ethernet routing supports VITA 31.1 backplane networking.

Serial Lines

- Two serial communication ports supplied by the 6300ESB (SP0/COM1 and SP1/COM2)
- SP0/COM1 port is available via the front panel connector or via the P2 connector.
- SP1/COM2 port is available via the P2 connector.
- Each serial port may be configured as EIA-232, EIA-422 or EIA-485.

VME Interface

- Supplied by the Tundra Universe II - PCI to VME bridge.
- A32/A24/A16/MBLT64 addressing modes.
- D64/D32/D16/D08 (E0) data widths in both user and supervisor address space.
- The board can act as system controller when in the first VME bus slot.
- Geographical addressing and Autoslot ID are both supported.

Dual Real Time Clocks (RTC)

- The 6300ESB ICH provides a RTC.
  - This includes a PC-AT clock, calendar and 242 bytes of CMOS RAM. It is used as the main RTC device when the board is on. This RTC is not powered by a battery when the board is off
- When the board is off, the date/time retention ia made by a distinct very low power RTC circuit with backup power provided by an onboard 35 mAh battery.
  - The battery provides more than ten years of power backup under normal operation.
  - This secondary RTC is accessed via the I2C bus and can generate an interrupt.
- The time can be maintened from an external supply via the VMEbus `+5VSTDBY` pin for battery free operation if required.

System Synchronization Timer (SST)

> The Software Synchronization Timer is a 32-bit timer clocked by the VME bus SYSCLK signal. It allows high accuracy software synchronization for multi-processor-based systems.

Optional Disk Drive / Mass Storage

> Onboard 44-pin header EIDE interface for use by the optional Hard Disk or CompactFlash Mass Storage kits in place of one PMC.

> Up to two EIDE peripherals may be connected to this interface.

PMC/XMC Mezzanines

> PMC Site 1
  - 64-bit / 66 MHz PCI bus
  - 3.3V PCI only signaling
  - VITA 35 - 64ac on P2 rear I/O Pn4
  - Exclusive use of PMC Site 1 and optional disk drive

> XMC/PMC Site 2
  - 64-bit / 66 MHz PCI bus
  - 3.3V PCI only signaling
  - x8 PCI-Express configurable
  - Dual x4 PCI-Express links
  - Pn4 I/O routing: 1-32 (P2-32 dz) and 45-64 (P0 PICMG 2.17) or 33-64 (P0), refer to 6.1.1 „P0 Connector Pin Assignment" Note (1)

System Management

> The PENTXM2 or PENTXM4 features a system management as outlined in the VITA 38 / PICMG 2.9 recommendation:
  - H8 microcontroller as Baseboard Management Controller (BMC),
  - Onboard System Management Bus (SMBus)
  - Power down capability when +5VSTDBY is supplied,
  - Remote communication capability via Ethernet controller,
  - Dual SMBus on backplane P1 to interface both the Intelligent Chassis Management Bus (ICMP) and the Intelligent Platform Management Bus (IPMB) in compliance with VITA 38 standard.

EFI BIOS Firmware

> The PENTXM2 or PENTXM4 supports a BIOS Firmware which complies with Extensible Firmware Interface (EFI) specification. The EFI specification defines a new model for the interface between operating systems and platform firmware. The interface consists of data tables that contain platform-related information, plus boot and runtime service calls that are available to the operating system and its loader. Together, these provide a standard environment for booting an operating system and running pre-boot applications.

Build In Test Option

> Kontron diagnostics tools for Intel-based SBCs provide a comprehensive set of Built-In Test (BIT) routines to verify the integrity of the underlying hardware. Designed for use with mission-critical software with hard real-time constraints, they simplify integration with applications running COTS software.
> The Kontron Power-on BIT (PBIT) routines run automatically at power-on, and the test results are stored in onboard Flash memory for later use by the operating system or application.

2.3 Inputs/Outputs

The PENTXM2 or PENTXM4 has a wide variety of possible I/O connectivity including Ethernet, Serial, USB, SATA, GPIOs, ...

» The PENTXM2 or PENTXM4 front panel provides:

- Two 10/100/1000/1000BASE-T Ethernet port (Ethernet channel 0 and Ethernet channel 1),
- One USB 2.0 interface,
- One Serial connector,
- One ABORT/RESET switch.

For more information about the pin assignment of the front panel connectors, refer to section 5.2 page 53.

» The PENTXM2 or PENTXM4 P0 connector provides:

- Two 10/100/1000BASE-T Ethernet interfaces (Ethernet channel 0 and Ethernet channel 1),
- Two USB 2.0 interfaces,
- Two Serial ATA (SATA-150) interfaces,
- XMC/PMC Site 2 I/O signals P24 33-64,
- x4 PCI Express Link.

For more information about the P0 pin assignment refer to section 5.1.1 page 30.

» The PENTXM2 or PENTXM4 P2 connector provides:

- XMC/PMC Site 2 I/O signals P24 01-32,
- PMC Site 1 I/O signals P14 01-64,
- Two serial lines.

For more information about the P2 pin assignment refer to section 5.1.6 page 38.

Using P0 or P2 I/O minimizes the effort needed to remove boards from a rack, improving maintainability and reliability.

For example, the rear I/Os may be attached by a VME64 Rear Transition Module (PBV36-P0-PENTXM2-00). Refer to Section 2.5 “Rear Transition Module Overview" page 16.

2.4 Board Support Packages

BSPs are available for:

- Linux 2.6

For LynxOS, VxWorks and Windows BSPs availability, please contact your Kontron representative.

2.5 Rear Transition Module

A VITA 36 style Rear Transition Module (RTM) provides P1, P2, and P0 signal routing to rear panel connectors.

The RTM plugs into the rear of the same backplane slot into which the PENTXM2 or PENTXM4 is also installed.

The P1 is installed on this RTM in order to route the SMB signals to the standard 5-pin expansion connector when this board is in slot 1 (system controller).

More I/O signals must be routed out the RTM than those that are routed out the front panel. In order to conserve rear panel space a specialty cable may need to be created or the number of available functions may need to be reduced and/or selected as build options.

The I/O requirements include:

- 2 Gigabit Ethernet ports
- 1 USB port
- 1 SMB connector
- 2 Serial ports
- 3 GPIOs and Miscellaneous signals
- 2 PIM connectors for PMC Site 1
- 2 SATA ports
- PCI Express port
- Reset
- Mechanical Ground
- Power supplies connectors

For more information about the I/O RTM pin assignments, refer to the Chapter 4 “Expanding I/O on Rear" of the “PENTXM2 or PENTXM4 Connection Guide" (CA.DT.A10).

Chapter 3 - Preparing Before Using

This chapter gives guidelines on preventing static electricity discharge, environmental protection, unpacking, inspecting and identifying the PENTXM2 or PENTXM4.

3.1 Preventing Static Electricity Discharge

During unpacking and installation of the board, it is important to follow proper procedure:

1. To avoid ESD damage don't remove the board from its antistatic packaging without wearing an antistatic wrist strap. Place the strap around your wrist and connect it to an electrical ground. An electrical ground can be a piece of metal that literally runs into the ground (such as an unpainted metal pipe) or a metal part of a grounded electrical appliance. An appliance is grounded if it has a three-prong plug and is plugged into a three-prong grounded outlet.
2. After removing the board from its protective packaging (or chassis), place the board flat on a static dissipative surface connected to a common ground by a low-resistance connection. Do not slide the board over any surface.
3. Store or ship the board into its shipping box, because it is treated to assure an antistatic protection and to be stored in a protected area (EPA).

The antistatic bag is more appropriate for a one-time use and should not be considered for repeated use.

3.2 Unpacking

Don't throw out the shipping box, it should be used to store or ship the board.

The PENTXM2 or PENTXM4 is shipped in an individual, reusable shipping box closed by an ESD stick-on label.

1. First, when you receive the shipping container, inspect it for any evidence of physical damage. If the container is damaged, request that the carrier's agent is present when the carton is opened. Keep the contents and packing materials for the agent's inspection and notify Kontron's customer service department of the incident. Retain the packing list for reference.
2. Assuming that you wear an antistatic wrist strap, you can open the shipping box by cutting the ESD stick label. If the label has already been cutting, please notify the carrier and Kontron immediately.
3. If your box contains foams, remove the first foam. Kontron board is protected by an antistatic envelope.
4. When unpacking the board, observe antistatic precautions (refer to section 3.1 page 17).
5. Closely inspect the board for any signs of shipment-related damages such as loose components or bent pins. If any evidence of damage is discovered, please notify the carrier and Kontron immediately.
6. Work at an approved antistatic workstation and a grounded bench mat.

This package has been designed for shipping and it is not suitable for long-term storage (upper than two years) nor storage under severe conditions. For more information, please visit our web site: www.kontron.com

3.3 Inspection

Assuming that the PENTXM2 or PENTXM4 is not obviously damaged, you can now go on to inspect it. It is possible for components (connectors, socketed chips etc.) to work loose or be dislodged in transit or in the process of unpacking, although this is extremely unlikely. A quick visual inspection should reveal any obviously loose components. Any defects detected should be reported to Kontron.

3.4 Board Identification

Kontron PENTXM2 or PENTXM4 boards are identified by labels fitted to the bottom and top sides.

» Labels fitted to the bottom side of the PENTXM2 or PENTXM4

- **A** “Chronological serial number" label.
- **B** “Variant" and “Engineering Change Level" (E.C. Level) label: The “Variant" number is used with the Self-Tests and manufacturing Self-Tests. In the below example the E.C. Level is eeee.
- **C** “Board Idenditification" label (Order Code) of the board.
- **D** “ETH0 Ethernet Number" label: This number is in hexadecimal.
- **E** “ETH1 Ethernet Number" label: This number is in hexadecimal.

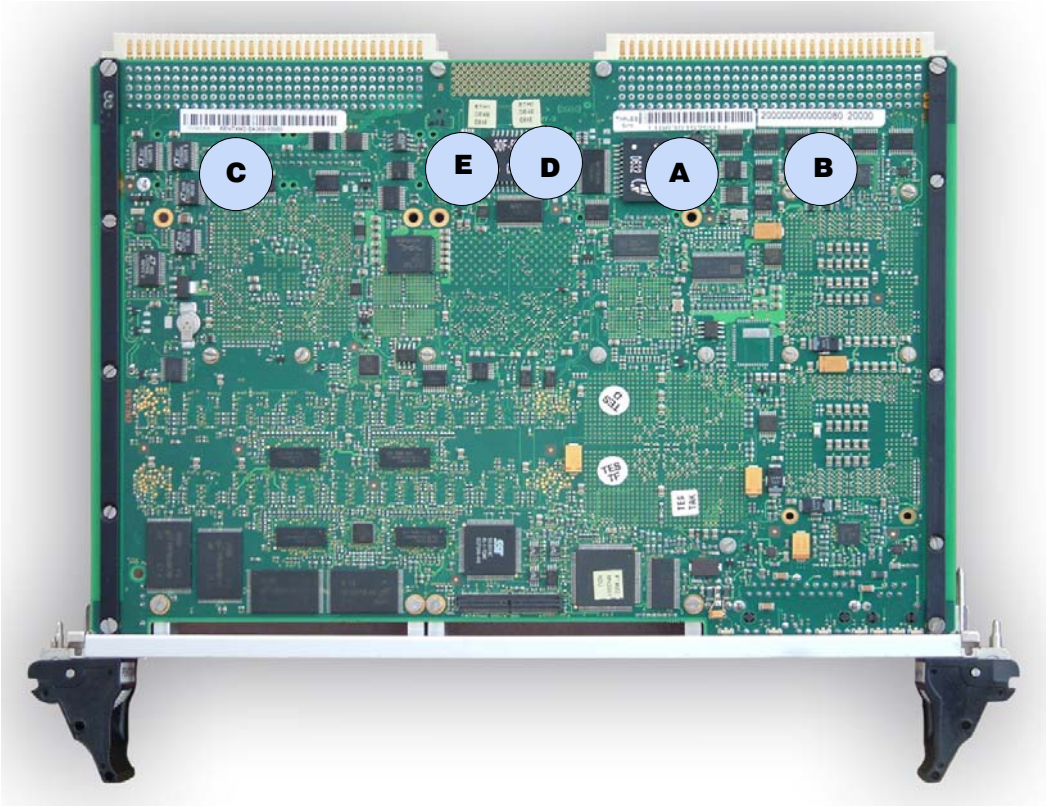


Figure 7: Bottom Side Identification Labels

Labels fitted to the top side of the PENTXM2 or PENTXM4

F Signaling level label: **no PMC voltage selection key is provided on the board.**
Only +3.3V and Universal PMCs are supported on the PMC slots.

G CPLD version.

H Insyde Software licence.

I Flash BIOS identification.

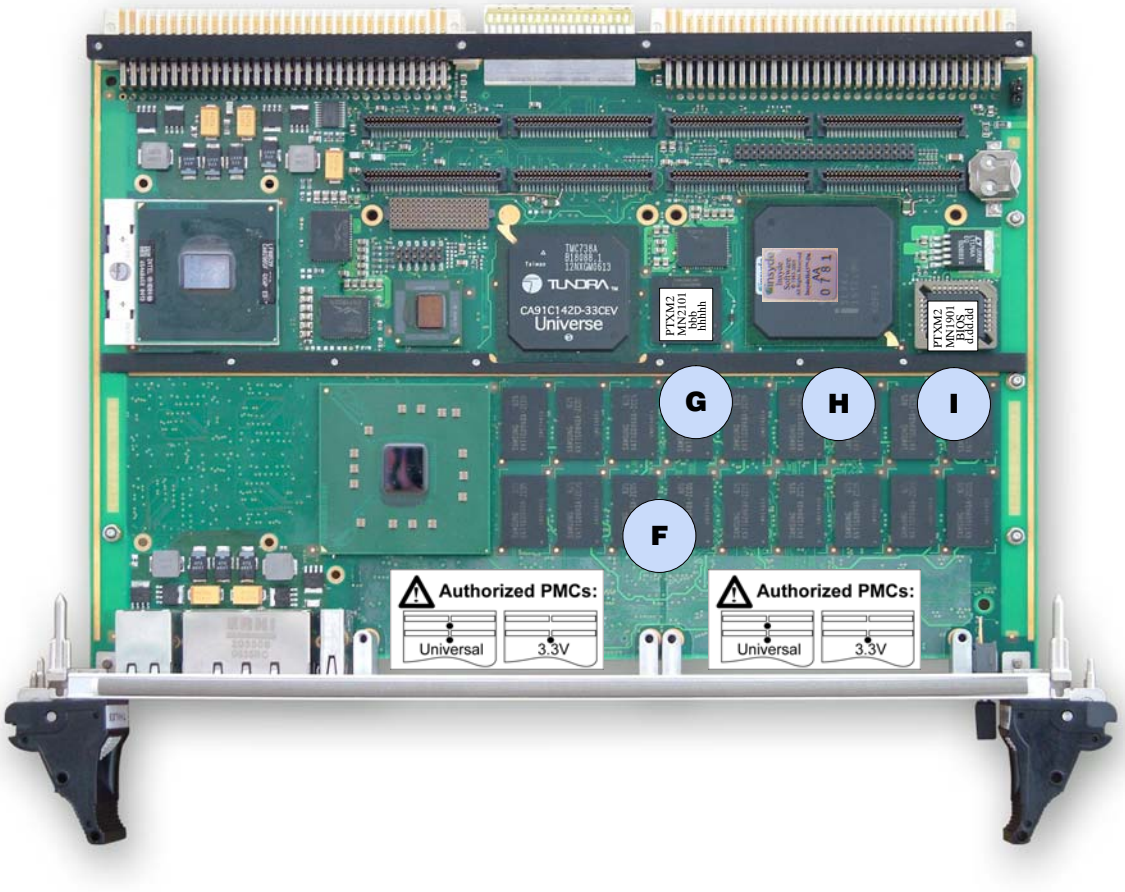


Figure 8: Top Side Identification Labels

3.5 Installing the Onboard Mass Storage

The PENTXM2 or PENTXM4 supports two onboard mass storage options:

- a 2.5 inch EIDE hard disk drive; refer to section 3.5.1 for a detailed description.
- a CompactFlash carrier module; refer to section 3.5.2 for a detailed description.

Both mass storage options are mounted in the PMC site area and connect to the EIDE header (P6 connector) that is located between the PMC connectors of PMC Site 1. This is shown in Figure 9. The following sections detail the installation procedures for the mass storage options.

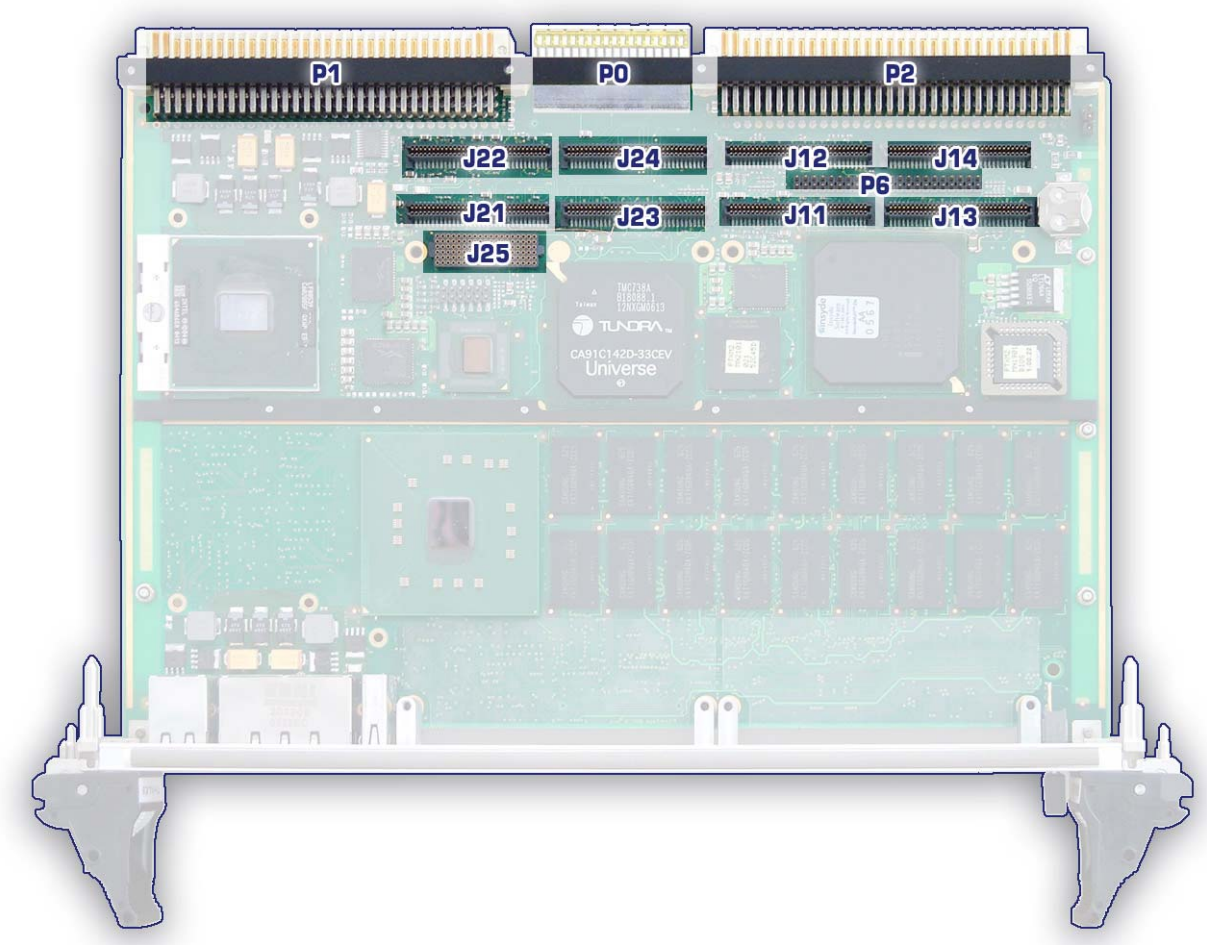


Figure 9: PENTXM2 or PENTXM4 Onboard Connector Locations

3.5.1 Hard Disk Storage Kit

Two hard disk storage references are available:

- **ICHD_PENTXM2-080**: mechanical hard disk storage mounting kit + 2.5-inch EIDE disk drive (80 GB)

The associated mechanical hard disk storage mounting kit is referenced:

- **KIT-DISK-PXTM2**: mechanical hard disk storage mounting kit only

Description of the Mechanical Hard Disk Storage Mounting Kit

Description	Quantity
Mounting Plate	1
Front Panel / EMC Gasket	1
M3x5 Torx Screw (extremely low head)	3
M2.5x10 Torx Screw	4
M2.5x4 Standoff	2
M2.5x7 Standoff	4
EIDE Disk Cable	1
Insulating Sticker	1

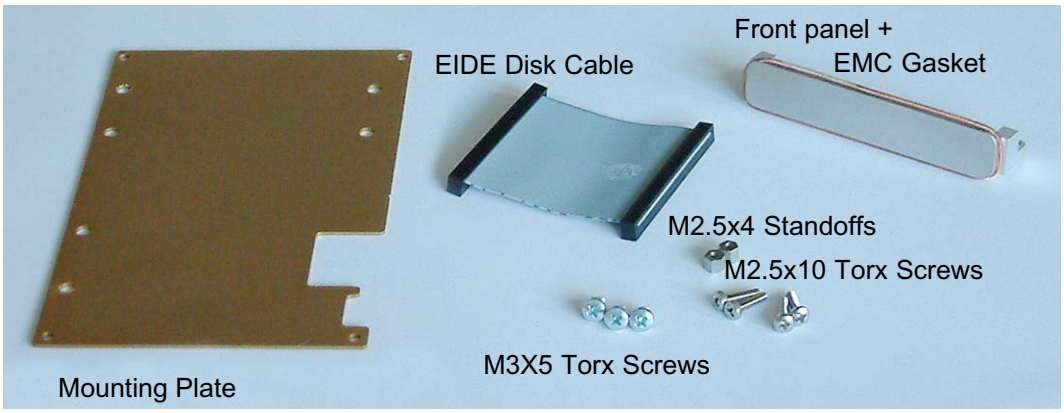


Figure 10: Hard Disk Storage Mounting Kit

Installation of the Hard Disk Storage Kit

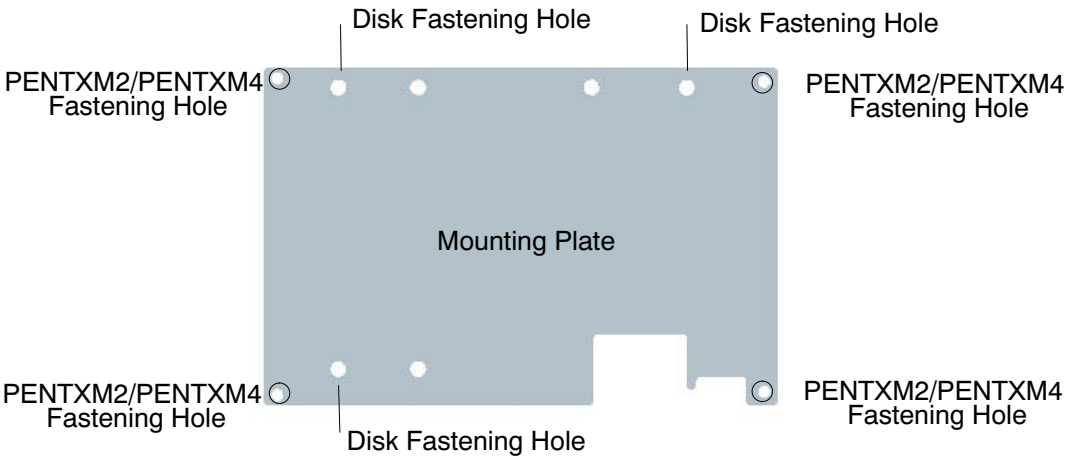


Figure 11: Hard Disk Storage Mounting Plate

1. Set up the insulating sticker on the mounting plate as shown below.

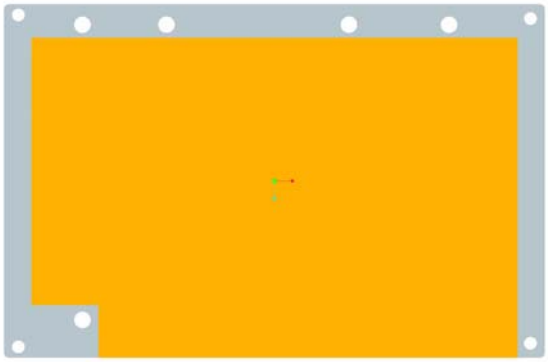


Figure 12: Setting up the Insulating Sticker

2. Fix the EIDE disk on the mounting plate using the three M3x5mm Torx screws as shown in Figure 13.

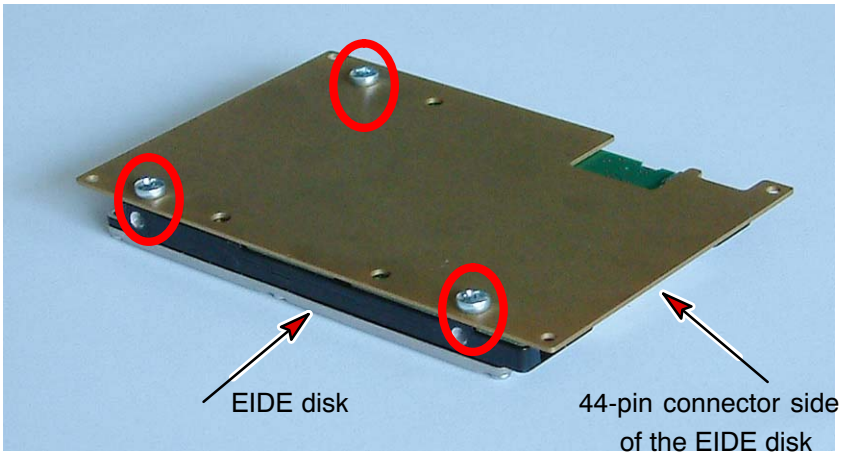


Figure 13: Fixing the EIDE Disk

Note, the lack of the pin 20 on the 44-pin EIDE connector on the disk and on the board.

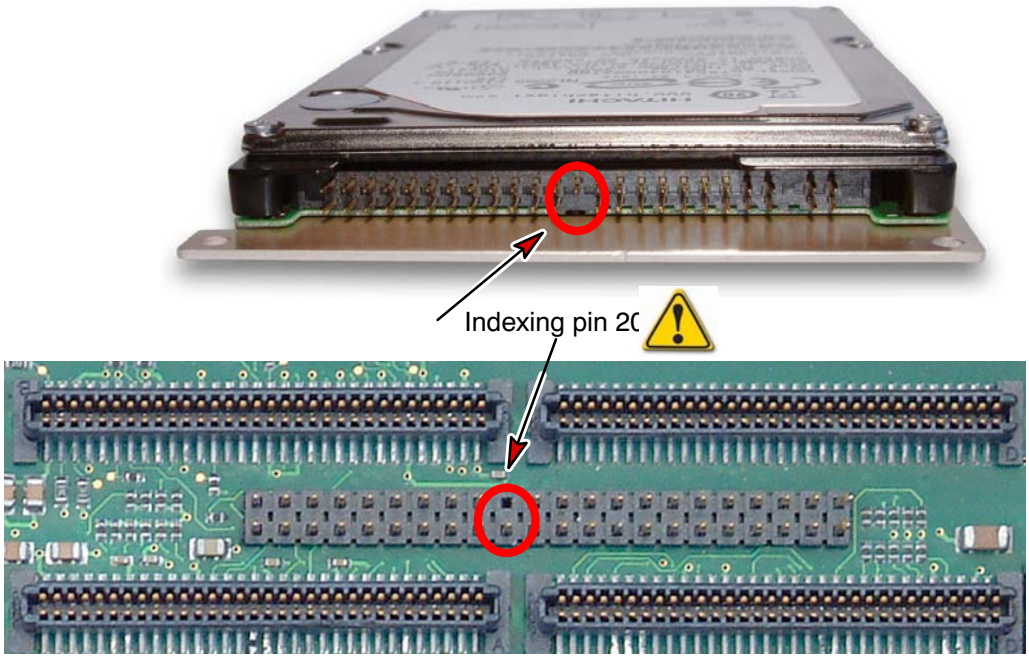


Figure 14: 44-pin EIDE connector

Note, the filling-in of the hole 20 on both sides of the ribbon cable.

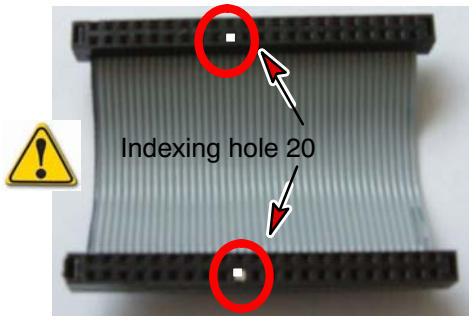


Figure 15: 44-pin EIDE cable

3. **Plug the cable on the EIDE disk as shown in Figure 16 page 25.**
   The indexing pins and indexing holes (described in Figure 14 and Figure 15 page 24) make easier the connection of the cable.

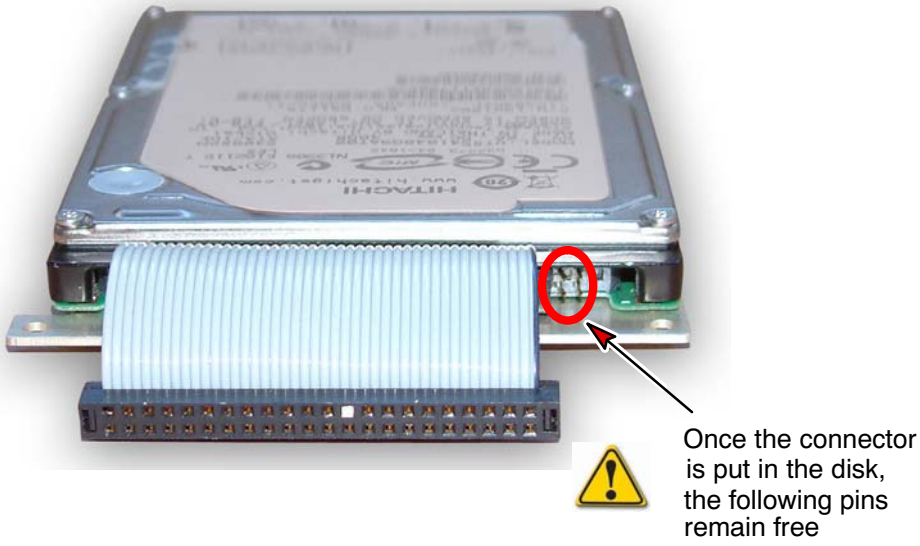


Figure 16: Plugging the cable: Disk Side

4. **Replace the standard front panel of the board by the specific front panel fitted with the EMC gasket.**
   Use two M2.5x10 Torx screws to fix it to the board (refer to areas highlighted in red in Figure 17). Do not over tighten the screws.
5. **Fix the two standoffs M2.5x4 to the board using two M2.5x10 Torx screws (refer to areas highlighted in green in Figure 17).**
   Do not over tighten the screws.

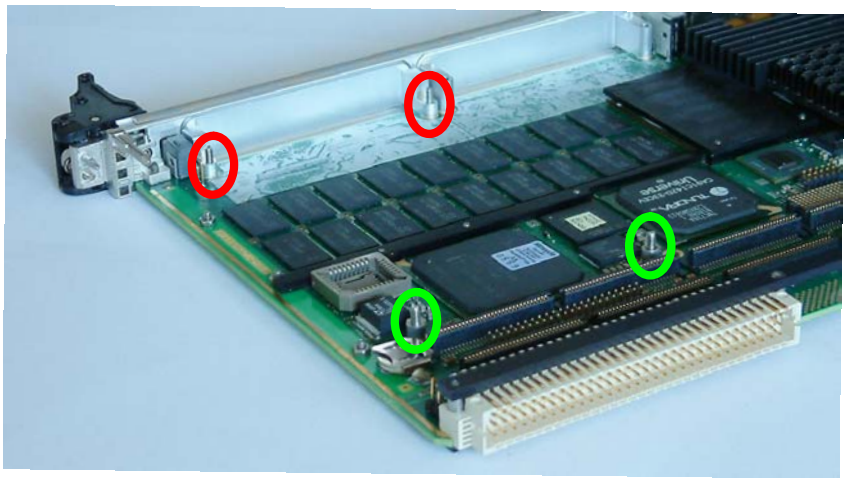


Figure 17: Preparing the EIDE Disk Installation

If the board is likely to be subjected to mechanical vibration a suitable thread lock compound applied to the screws should be considered.

6. **Plug the cable on the P6 connector of the board as shown in Figure 18 page 26.**
   The indexing pins and indexing holes (described in Figure 14 and Figure 15 page 24) make easier the connection of the cable.

   Be careful, make sure to align properly the 44-pin connector and the P6 connector.
   In case of one step shifting error (right or left side) when plugging the connector a short-circuit is generated between the 5V and the GND and between the 3V3 and the GND, and the board or the disk may be damaged.

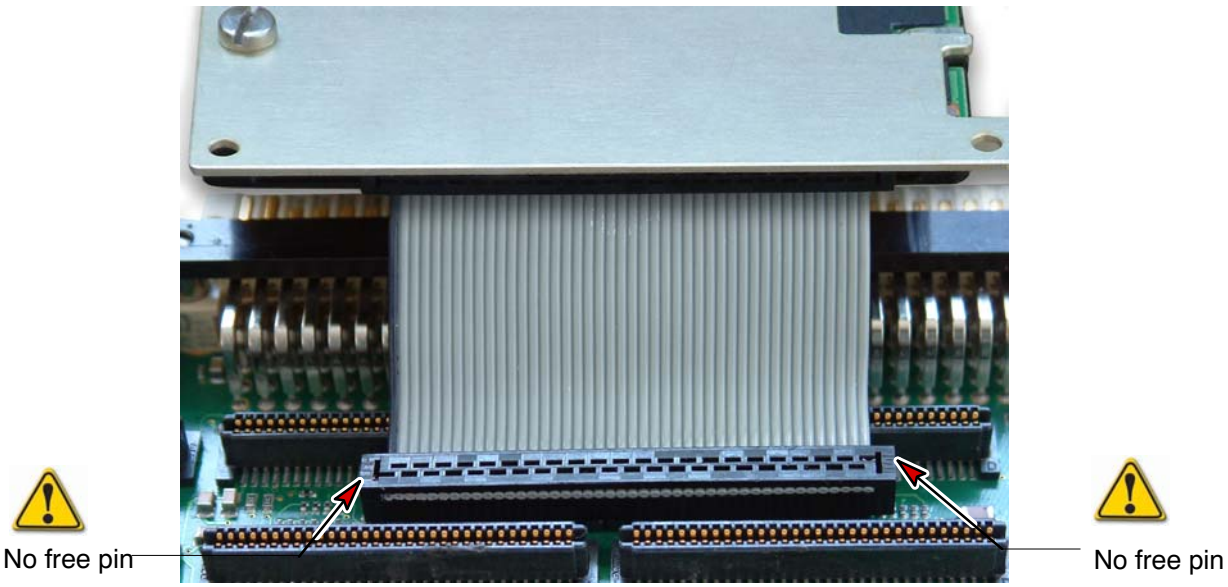


Figure 18: Plugging the cable: Board Side

7. **Fix the mounting plate in position to the board using the four M2.5x7 standoffs.**
   The mounting plate lies, on one side on the specific blank panel (refer to areas highlighted in red in Figure 19), and on the other side on the M2.5x4 standoffs installed in stage 5 (refer to areas highlighted in green in Figure 19).

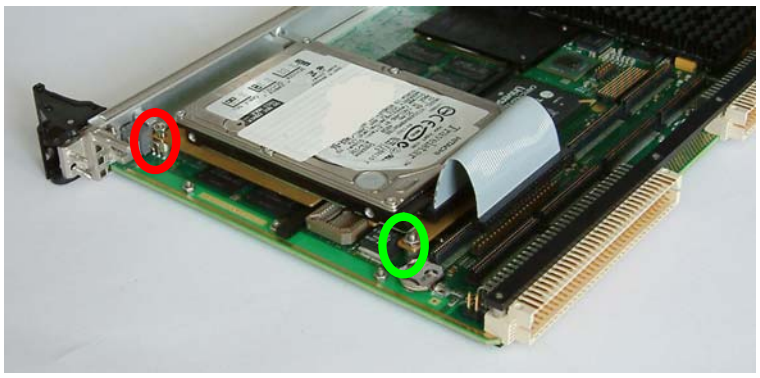


Figure 19: Fixing the Mounting Plate

3.5.2 Dual CompactFlash Storage Kit (PENTXM2-CFM)

Dual CompactFlash Kit not yet available.
Please contact your Kontron representative for a detailed information on this topic.

3.6 Installing or Removing a XMC/PMC Module

PMC modules are delivered with a full kit of parts for mounting them, and the user guide for the module normally contains instructions on how to fit the module.

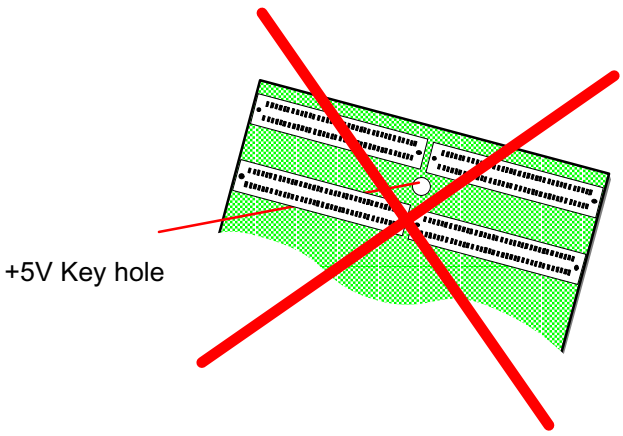
The installation of the PMC on the PENTXM2 or PENTXM4 conforms to the IEEE P1386.1 standard.

To install the XMC/PMC module, refer to Figure 20 “PMC 64 - PMC Site 1" and Figure 21 “XMC/PMC 64 - PMC Site 2" and follow the steps below:

To avoid ESD damage, wear an antistatic wrist strap to discharge static electricity while performing any part of the installation that involves touching the PENTXM2 or PENTXM4 board or the XMC/PMC. If you can't wear an antistatic wrist strap, touch one hand to the bare metal surface to provide grounding.

1. Place carefully the PENTXM2 or PENTXM4 with the backplane connectors facing you on a static dissipative surface connected to a common ground by a low-resistance connection. Do not slide the board over any surface.
2. Remove the blanking plate from the appropriate XMC/PMC slot of the PENTXM2 or PENTXM4.
3. Check that the standoffs are attached to the XMC/PMC.
4. Install the XMC/PMC, component-side down, aligning the PCI connectors with their mating connectors on the PENTXM2 or PENTXM4 and the XMC connector if available. Press them together so that the friction from the pins holds them together. Insert the standoff plug mounted on the PENTXM2 or PENTXM4 into the keyhole. The module's bezel will fill the slot and provide a connection to the module.

   As no PMC voltage selection key is provided on the board, make sure not to insert a +5V PMC on the board. Failture to observe this restriction may result in damage to the PMC or the PENTXM2 or PENTXM4.
   Refer to section 7.4 “Signaling Voltage Keying Pin" page 73 for more information on this topic.



5. Screw the XMC/PMC in place using the 4 mounting points, on the bottom side of the PENTXM2 or PENTXM4 . You need a Phillips screwdriver for this stage.
6. The XMC/PMC attachment is now complete.
7. Insert the PENTXM2 or PENTXM4 into the chassis making sure it is plugged into the backplane.

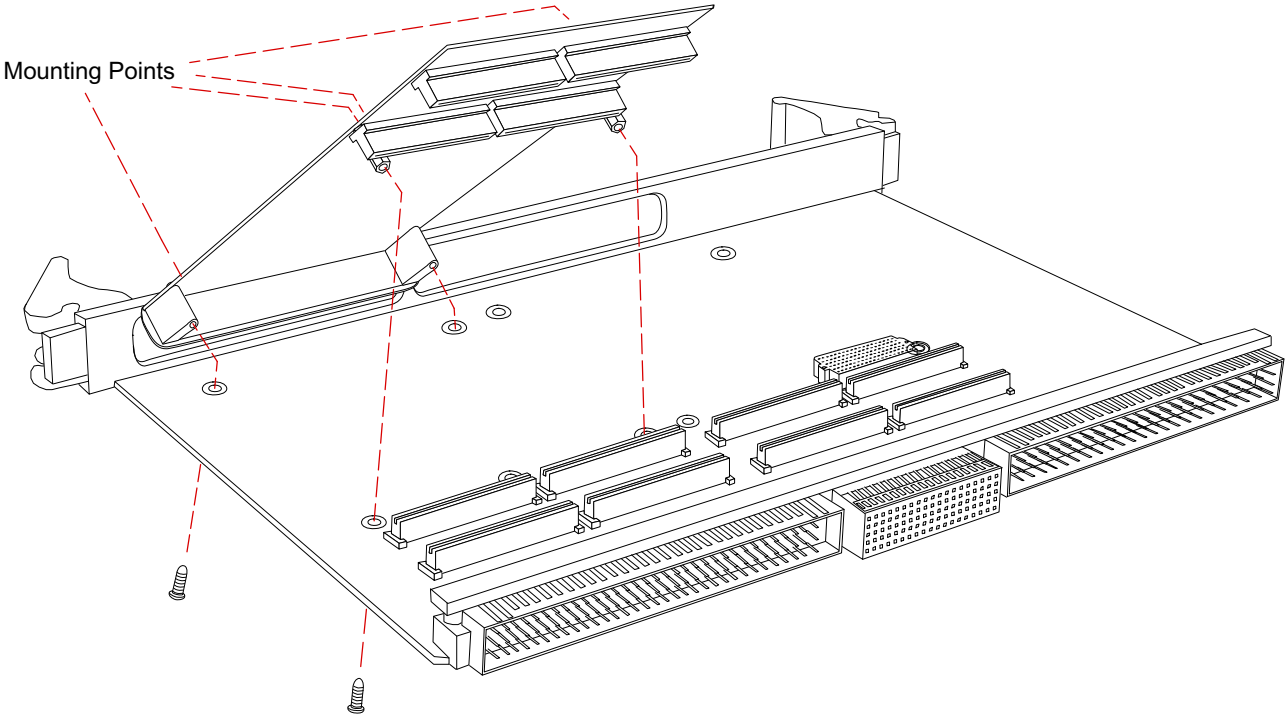


Figure 20: PMC Installation on PMC Site 1

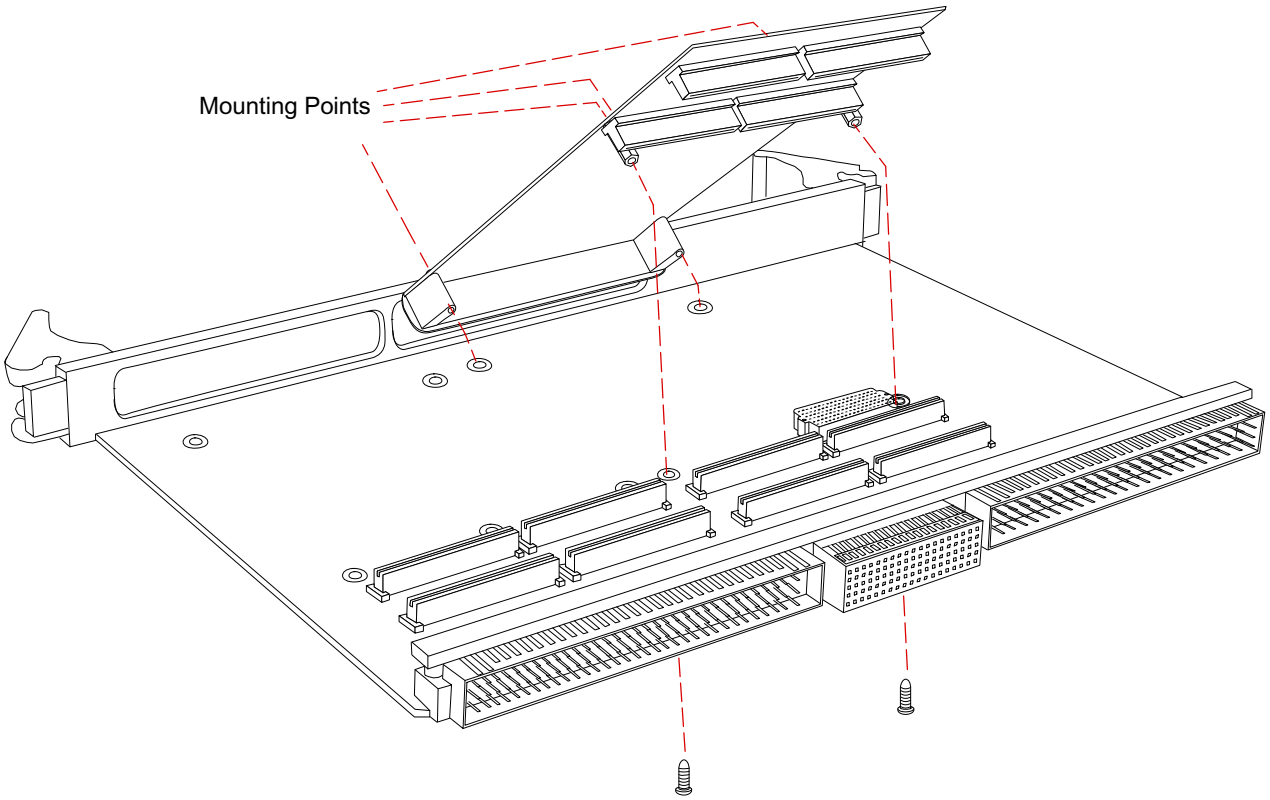


Figure 21: PMC Installation on PMC Site 2

3.6.1 XMC/PMC Specificities

The XMC board standard is based on the PMC mechanical definition, and occupies the same board area.

The XMC board add one new connector to the connectors already on a PMC. The new connectors support high-speed differential signals for fabric communications.

Figure 22 shows a XMC fitted only with the XMC connector.

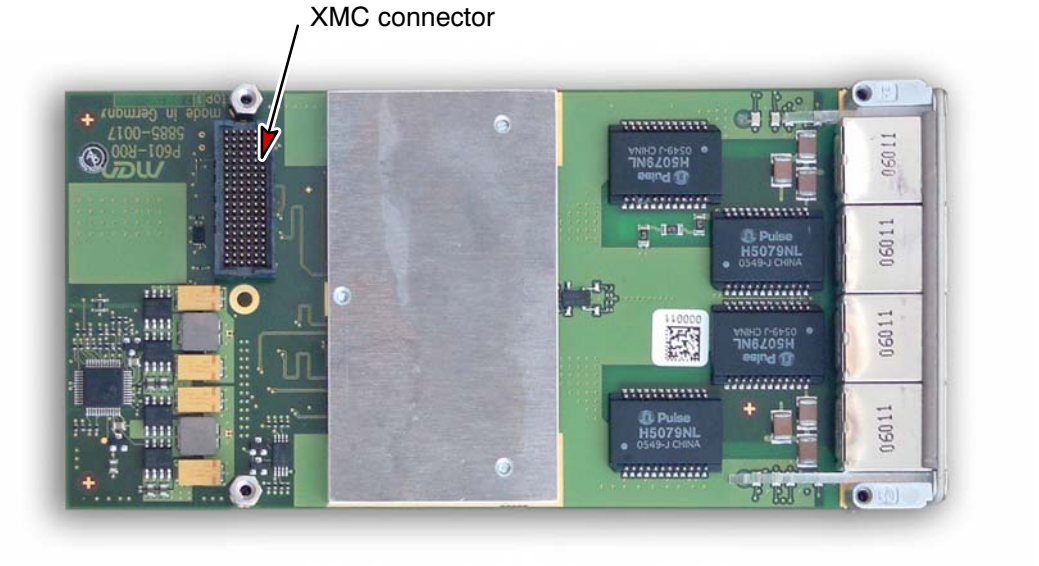


Figure 22: Example of XMC/PMC

Figure 23 shows a XMC installation on the PMC Site 2.

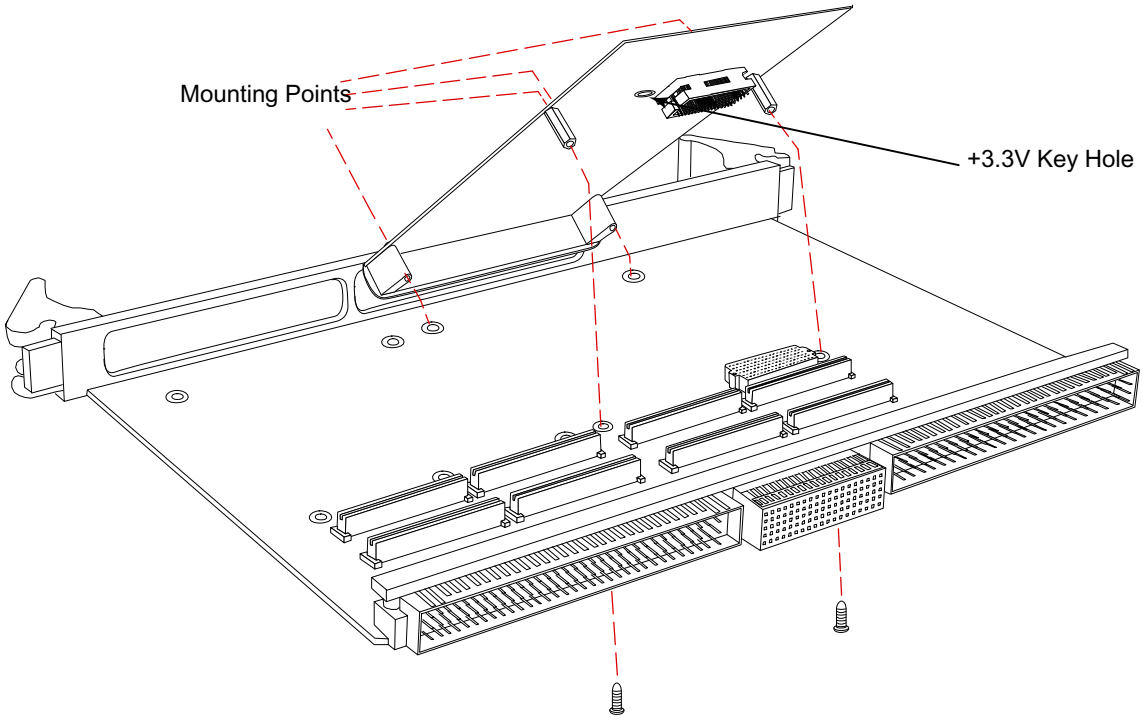


Figure 23: XMC Installation on PMC Site 2

Chapter 4 - Functional Description

This chapter describes the PENTXM2 and PENTXM4 board at a block diagram level. The general description provides an overview of the PENTXM2 and PENTXM4, followed by a detailed description of several blocks of circuitry.

The PENTXM2 and PENTXM4 is a member of Kontron's family of single board computers for the bus architecture. It has been designed as a powerful single board computer based on the dual-core Intel Xeon processor, the E7520 Memory Controller Hub (MCH) with PCI-Express interconnects as shown in Figure 24. This architecture allows up to 6.4 GB/s aggregate data throughput with the two channel DDR2 memory.

4.1 PENTXM2 and PENTXM4 Block Diagrams

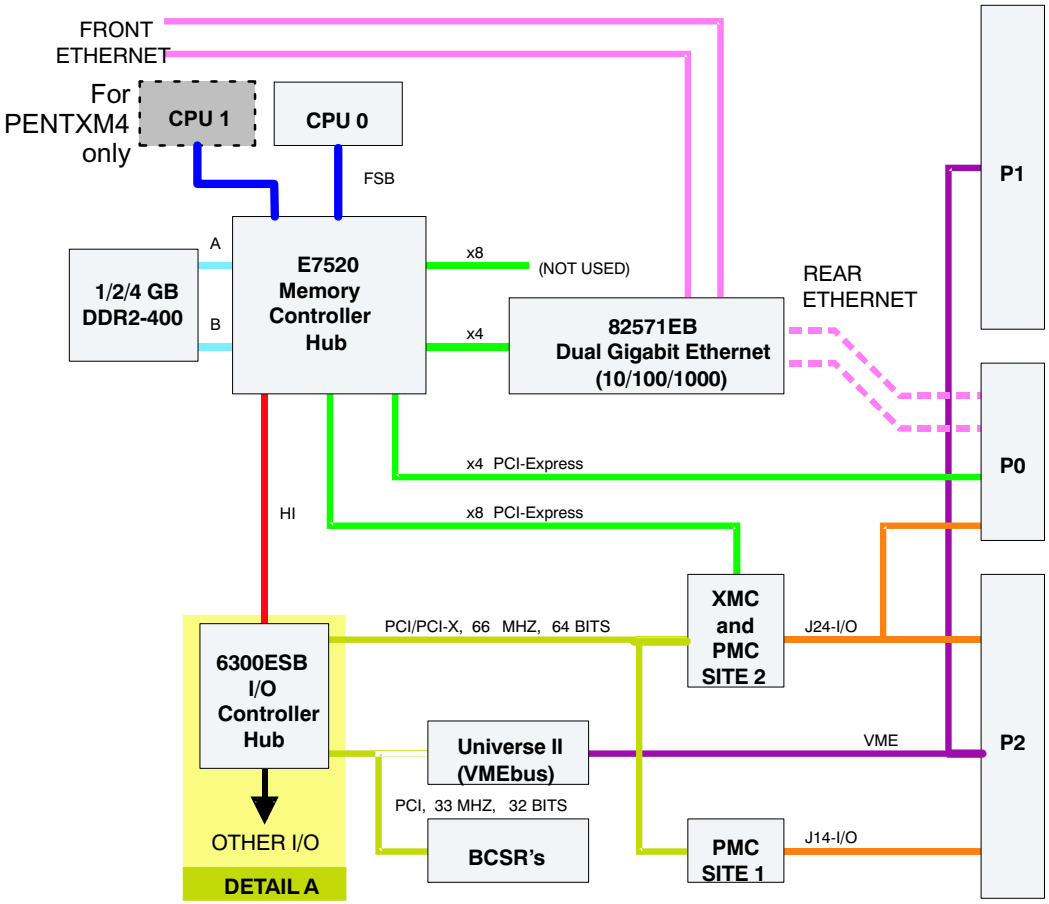


Figure 24: PENTXM2 and PENTXM4 Block Diagram

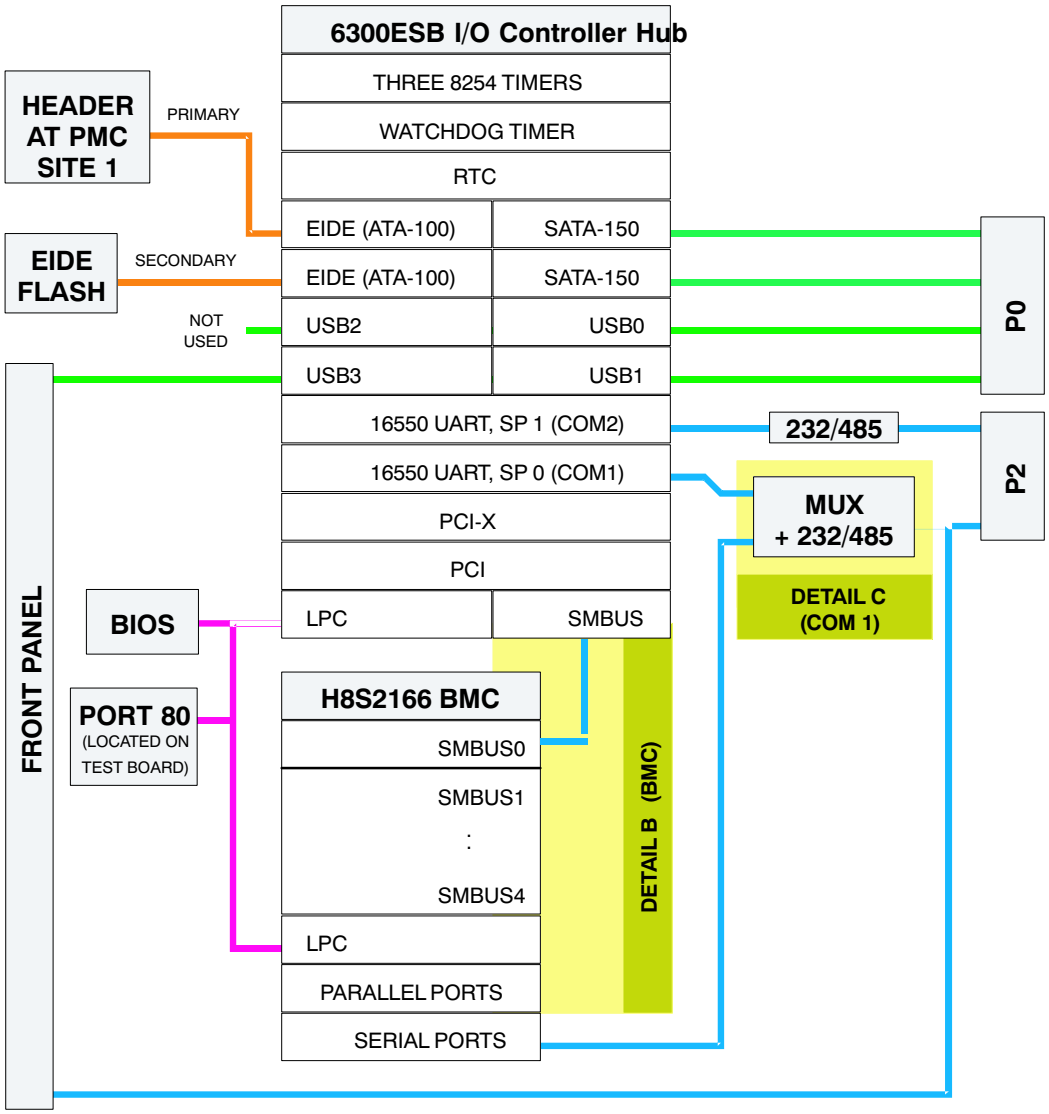


Figure 25: Detail A, I/O Block Diagram

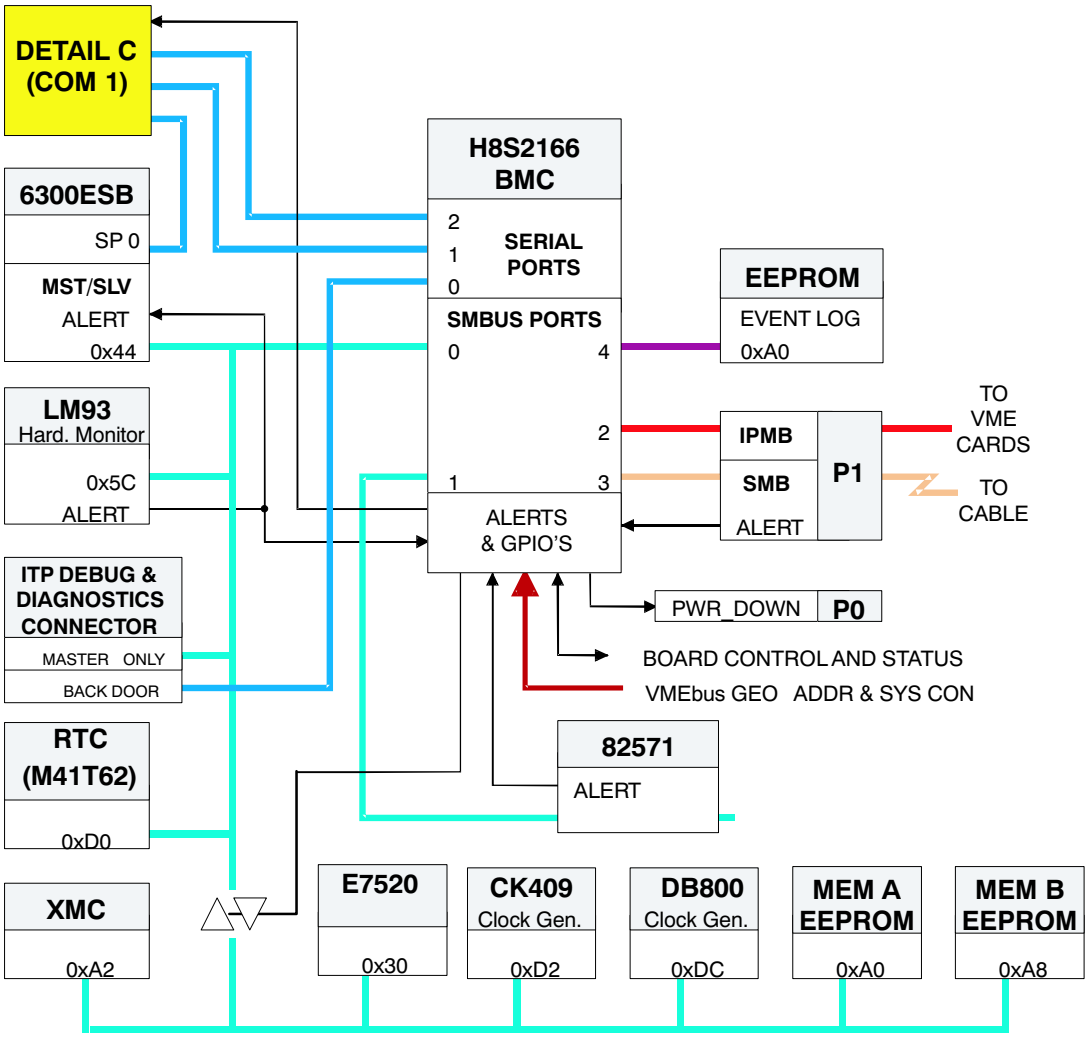


Figure 26: Detail B, BMC Block Diagram

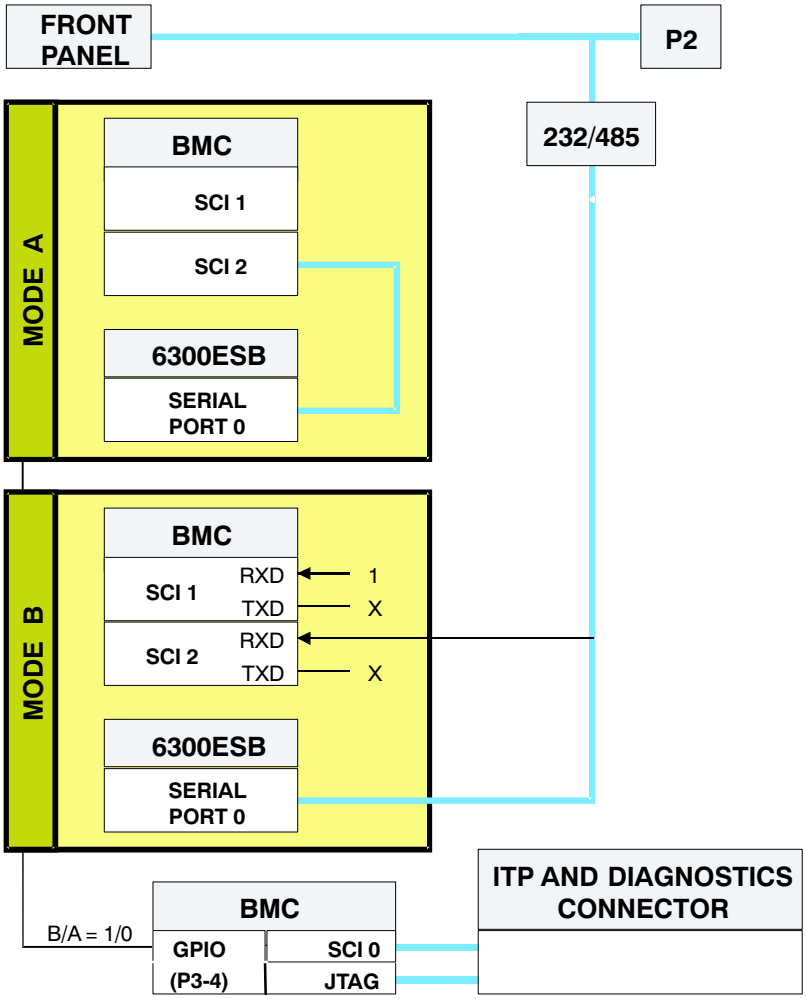


Figure 27: Detail C, COM1 Multiplexing Block Diagram

4.2 General Description

4.2.1 Central Processor

The central processor used on this board will be the low voltage (LV) version of the Sossaman dual core processor (one thread per core) which is vendor-qualified with the E7520 Memory Controller Hub (E7520 MCH).

- The PENTXM2 features one processor.
- The PENTXM4 features two processors.

This processor is upwardly code-compatible with the other members of the x86 family of microprocessors.

The Level 1 and Level 2 caches are both implemented on the processor die for maximum performance. The L2 cache is 2 MB.

The processor incorporates a mechanism for changing its operating frequencies and core voltages under software control. By making these reductions the board's maximum power consumption is also reduced. Refer to section 9.4 “Central Processor Power and Thermal Management" for a detailed presentation.

4.2.2 Memory Controller Hub (E7520 MCH)

The PENTXM2 and PENTXM4 uses the Intel E7520 Memory Controller Hub (MCH) associated with the 6300ESB chipset.

The E7520 MCH provides:

- two channel DDR2-400 SDRAM memory controller,
- the Hub Interface (HI 1.5) to the 6300ESB,
- three configurable x8 PCI Express (PCI-E) interfaces with a maximum theoretical bandwidth of 2 GB/s each.
  - One of the x8 PCI Express interfaces is configured as two independent x4 PCI Express interfaces. One x4 serves as the interconnect to the dual Ethernet Controller and the other serves as the interconnect to an external PMC Carrier board via P0.
  - One x8 PCI Express link connects the E7520 MCH to the XMC connector at PMC Site 2.
  - The remaining x8 link is unused.

Standard Air (SA) class boards power with 167 MHz base operating frequency for the Front Side Bus (FSB) (quad pumped to 667 MHz), and the appropriate gearing ratio for DDR memories.

Rugged Conduction-Cooled (RC) class boards may power up at a lower FSB frequency.

The BIOS needs to have knowledge of the PENTXM2 and PENTXM4 board FSB frequency. The BIOS can find out information about the installed SDRAM's from the installed SPD EEPROM's. After obtaining the FSB and SDRAM frequencies the BIOS can set the gear ratios to obtain DDR400 operation using the `CLKGRFM[1:0]` and `CLKGRMF[1:0]` registers of the E7520 MCH.

4.2.3 SDRAM

The E7520 MCH SDRAM controller provides two DDR2-400 channels to support a maximum transfer bandwidth of 6.4 GB/s and features ECC data protection.

The SDRAM may be accessed by the processor and any other devices that connect either directly or indirectly to the E7520 MCH.

SMBus EEPROM's, the same as those used for DIMM's, will provide memory population information for the BIOS software.

The board supports:

- A 1 GB option using 64 MB SDRAM's
- A 2 GB option of onboard memory (1GB per channel) using 128 MB SDRAM's

The board has been designed to support the stacked die option, that can double the memory capacity of the board (up to 4 GB). Please contact Kontron.

4.2.4 External PMC Carrier Interface

PMC sites may be added to the PENTXM2 and PENTXM4, beside the two onboard sites, by connecting the PENTXM2 and PENTXM4 to the Common PMC Carrier using the P0, x4 PCI Express link. The Common PMC Carrier adds two more PMC sites. Please contact Kontron fro more information on this topic.

4.2.5 Dual Ethernet Controller

A single 82571EB Gigabit Ethernet controller is used to provide two high performance PCI to Ethernet ports which are accessible via the two front panel RJ-45 connectors or via the P0 connector. Software independently selects the routing method for each port and should be part of the BIOS configuration options.

The P0 Ethernet routing allows it to support VITA 31.1 backplane networking.

For systems without backplane networking, the Ethernet ports are available as standard Ethernet ports.

The communications path to the Ethernet Controller is a x4 PCI-E link with the E7520 MCH.

The BIOS allows the board to boot via an Ethernet port.

4.2.6 I/O Controller Hub (6300ESB)

The 6300ESB provides:

- a PCI for supporting medium performance PCI and other I/O devices

  The PCI connects to the optional VMEbus Bridge and the BCSR's (Board Control and Status Registers). The PCI is 32-bits wide and operates at 33 MHz.

- a PCI-X for high speed devices.

  The PCI-X provides a 66 MHz, 64-bit wide communications path between the 6300ESB and the two PMC sites.

The 6300ESB connects to the E7520 MCH via the Hub Interface (HI 1.5).

The 6300ESB also provides a variety of peripheral functions including:

- EIDE controllers, refer to section 4.2.6.5 “EIDE Controllers"
- USB controllers, refer to section 4.2.6.7 “Universal Serial Bus"
- LPC (Low Pin Count) Bus bridge, used to connect to the BIOS, Port 80 Header, and the Board Management Controller (BMC), refer to 4.2.6.13 “LPC"
- IOAPIC interrupt controller,
- other legacy PC-AT architectural functions.

4.2.6.1 Timer/Counters

The 6300ESB provides three 8254-type timer/counters which have fixed uses. Refer to section 9.8.1 “Timer/Counters" for a detailed description of these timer/counters.

4.2.6.2 Watchdog Timer

The PENTXM2 and PENTXM4 board includes a hardware Watchdog timer that can be used by the operating software to monitor the normal operation of the system. Refer to section 9.8.2 “Watchdog Timer" for a detailed description of this timer.

4.2.6.3 Real Time Clocks (RTC's)

The 6300ESB provides a Real Time Clock (RTC)

The PENTXM2 and PENTXM4 also provides a second RTC (ST Microelectronics M41T62), with an onboard battery (Panasonic BR1225A) backup. This second RTC is accessible via the SMBus.

Refer to section 9.8.3 “Real Time Clocks (RTC's)" for a detailed description.

4.2.6.4 COM1 and COM2 Serial Ports

The 6300ESB provides two 16550-style serial communications ports, SP0 and SP1. SP0 and SP1 are also called COM1 and COM2 in PC parlance.

- COM1 and COM2 are available via the VMEbus P2 connector.
- COM1 is also available via the front panel connector.

If a video console port is not provided by a PMC, the BIOS must configure the board for operation with a Serial Console. When configured in this mode, the BIOS firmware will direct its output to COM1, and similarly will take its input from this port.

At power reset the COM2 port is disabled in order to avoid conflicts. It is the responsibility of the BIOS to configure the port.

Each serial port may be configured by the BCSR's as EIA-232 or EIA-485. The BCSR's can also independently configure each port to operate in full or half duplex mode. Slow slew rate is also BCSR-programmable when in EIA-485 mode. Refer to section 9.5.4 “COM2/1 Configuration (BCSR5)" page 87.

In EIA-485 half-duplex mode the port's DTR signal controls the data direction. Note that the signaling level of EIA-485 is compatible with EIA-422 so full duplex EIA-485 may also be used for point-to-point communications with an EIA-422 serial port. When a port is operating in EIA-485 mode software may configure the terminators for V.35, V.11, or unterminated using the BCSR's.

In EIA-232 mode the port is always unterminated.

4.2.6.5 EIDE Controllers

The 6300ESB has two EIDE/Ultra ATA100 controllers. One controller supports the Primary EIDE interface and the other supports the Secondary EIDE interface.

Primary EIDE Interface

The primary EIDE supports the onboard Mass Storage option kit. The primary EIDE interface connects to an onboard 44-pin header situated between the PMC Site 1 connectors for use by the optional Hard Disk or CompactFlash Mass Storage Kits. Up to two EIDE peripherals may be connected to this interface.

The Hard Disk kit will appear as the Secondary Master device.

The CompactFlash modules on the CompactFlash kit will appear as the Secondary Master and Secondary Slave devices.

A front panel LED indicates disk activity (see Section 9.2.3 “Other LEDs" page 79).

Secondary EIDE Interface for NAND Flash

Available or not, depending on the Manufacturing Option: `User Flash Disk.` Refer to 2.1 “Overview” section “Ordering Information" page 6.

A Silicon Storage Technologies SST55LD019 ATA/IDE to NAND Flash Interface Controller connects to the Secondary EIDE interface of the 6300ESB. Up to four NAND Flash devices are supported by the hardware.

When using 8 Gbits memories, the storage capacity is 4 GB which should be sufficient to boot WindowsXP without the need for rotating media.

`GPIO23` connects to the `WP_PD#` bit of the the SST55LD019 to invoke hardware write protection via a specific jumper (refer to section 5.4 “NAND Flash Protection" page 44).

- If the jumper is removed the entire NAND Flash is not write protected.
- If the jumper is installed and GPIO23 is logic 1 the NAND Flash is not write protected.
- If the jumper is installed and GPIO23 is logic 0 all Flash memory is protected.

A front panel LED indicates disk activity (see Section 9.2.3 “Other LEDs" page 79).

4.2.6.6 Serial ATA (SATA-150) Interface

Two independent Serial ATA interfaces are provided, both of which route to the P0 connector. Each interface is supported by its own DMA Controller.

A front panel LED indicates disk activity (see Section 9.2.3 “Other LEDs" page 79).

4.2.6.7 Universal Serial Bus (USB)

Three USB 2.0 interfaces are provided on this board by the 6300ESB:

- One channel is available on the front panel connector: USB3.
- Two channels are connected to the P0 connector: USB1 and USB0.

USB2 is not used.

All channels can operate at 1.5 Mb/s, 12 Mb/s or 480 Mb/s.

The BIOS firmware supports bootloading via any of these ports. It supports also an USB keyboard and mouse, especially if it detects the presence of a PMC video card.

Power for each USB interfaces is protected by an USB power controller. External devices that derive power from the USB ports may be used as long as the total current taken by each device is less than 500 mA. The power controller provides short circuit current limiting and fault isolation, fault detection (inputs to the 6300ESB), and power on/off control (GPIO's from the 6300ESB, see Table 28 “6300ESB GPIO Assignments").

4.2.6.8 Processor Port to SMBus

The processor software should provide its own Bus Management Controller (BMC) function using the SMBus interface of the 6300ESB.

This port is typically used by the BIOS to query the SDRAM Serial EEPROM's to determine how to configure the E7520 MCH SDRAM interface.

It should also be used to manage the clocks and various temperature and voltage alarms from the LM93.

The processor should send the status and alarms to the BMC via the LPC connection so that the BMC can maintain an event log in its private EEPROM.

Even though the BMC has a port to the SMBus of the 6300ESB, the BMC should not use that port unless the processor is powered down.

4.2.6.9 GPIO's

The 6300ESB provides General Purpose Input, Output, or I/O pins. refer to section 9.8.4 “GPIO's" page 97 for a detailed description.

4.2.6.10 PMC and XMC Sites

The 6300ESB uses its PCI/PCI X port to connect to each of the two PMC sites.

Data widths up to 64 bits, and clock speeds up to 66 MHz are supported for single function PMC's (those requiring only one IDSEL). The two sites are physically situated such that a double width PMC may be installed.

Each site provides an alternate function `IDSEL` for dual function, PCI-X capable PMC's. The `IDSEL` for the secondary function is offset by four address lines so that the interrupt binding remains consistent with the primary function. Dual function PMC's should limit the clock speed of the interface by tying `PCIX_CAP` to ground via a 10K resistor.

Both sites support the 3.3V PCI signaling environment only. **No PMC voltage selection key is provided.**

The PMC sites will also accept Processor PMC modules, but they are restricted to operating in non-Monarch mode.

PMC Site 2 can alternately be used as an XMC site with a x8 PCI Express link to the E7520 MCH. An XMC card installed in this location uses its P5 (J25 connector on the PENTXM2 and PENTXM4) for the Express Link. The installed XMC should provide either front panel I/O or utilize a P4 connector for I/O (J24 connector on the PENTXM2 and PENTXM4).

The BIOS may use the cPLD BCSR's to force protocol and clock speed restrictions for both PMC sites by forcing `PCIX_CAP` to ground or to ground through 10K ohms. It can also ground `PCIX_M66EN`. Both PMC sites utilize the same PCI/PCI-X segment so the settings affect both PMC sites. The new setting becomes effective with the next Board Reset. The default power up settings for these bits reside in the cPLD's internal Flash EPROM. The BIOS should provide the means to reprogram these bits.

4.2.6.11 VME Interface

The PENTXM2 and PENTXM4 VME interface is provided by a Tundra Universe II - PCI to VME bridge (VendorID = 10E3, DeviceID = 0000).

The VME interface supports transfers up to 64-bits wide. The onboard interconnect a 32-bit, 33 MHz PCI implementation which connects to the PCI segment of the 6300ESB.

The VME interface supports A32/A24/A16/MBLT64 addressing modes and D64/D32/D16/D08 (EO) data widths in both user and supervisor address space. The board can act as system controller when in the first VMEbus slot. Geographical addressing and Autoslot ID are both supported.

The PENTXM2 and PENTXM4 can be programmed as a VME master supporting off-board VME memory addressing accessible by any PCI bus master. The Universe II device uses the linear incrementing mode when being accessed by a PCI master. The PENTXM2 and PENTXM4 can also be programmed as a VME slave allowing other VME masters to access any PCI bus slave. This access is achieved by programming the appropriate Universe II device register. `PCI slave` registers are used for PENTXM2 and PENTXM4 master accesses and `VME slave` registers for VME accesses to the PENTXM2 and PENTXM4.

The VME interface performs auto-syscon detect at power up to provide system controller functionality, if the board is located in the lowest VME slot used. As system controller the Universe II will arbitrate VME mastership of the bus using DEMAND request mode.

The PENTXM2 and PENTXM4 can act as an Interrupt Handler for any combination of VME interrupts and can be an interrupter generating either a software interrupt or any of the Universe's internal interrupt sources on any IRQ level. All VME interrupts are directly mapped between the Universe II registers and the VMEbus backplane. Of the PCI LINT lines only LINT0 is mapped into the PCI interrupt and LINT1 is mapped to NMI. The BIOS software configures the Universe to generate a LINT1 when it encounters a VMEbus `BERR*` assertion while initiating VMEbus transfers.

VMEbus access is allowed to the full PENTXM2 and PENTXM4 memory map. Care must be taken to ensure that no accesses are made to areas that will corrupt the system memory or the configuration of any of the interfaces.

The PENTXM2 and PENTXM4 board will assert the VME SYSFAIL signal after a power-on or system reset. In some cases it may be desirable to deactivate this signal early in the boot process, while in others it can be left to the operating software to do this at a later stage. The SYSFAIL signal is controlled by the Universe II.
.

In normal operation the VMEbus SYSRESET* assertion also causes the board to be reset. A bit in the BCSR's allows this function to be inhibited.

4.2.6.12 cPLD

A custom MAX II cPLD supplements the board functionality as described in the following subsections. The cPLD becomes active while the VMEbus +5VSTDBY power rail is still coming up so the part is also used to sequence the remaining power supplies.

Note from Figure 26 “Detail B, BMC Block Diagram" 32 that the cPLD is accessed via the same 32-bit PCI segment of the 6300ESB as the Universe II. The implementation uses a PCI Target Only IP (VendorID = 184A, DeviceID = 1100) within the cPLD. This implementation prevents addressing conflicts with legacy software. The following subsections describe the cPLD functions.

» Board Control and Status Registers (BCSR)

The registers used are referred to as Board Control and Status Registers (BCSR) followed by a number. Multiply the BCSR number by 4 and add to the value of BAR0 to get the PCI address of that particular BCSR.

The BCSR's are

- BCSR0 Interrupt Status
- BCSR[1:2] Software Synchronization Timer (SST), refer to section 9.5.1 page 84 for a detailed description of BCSR[1:2]
- BCSR[3:4] Programmable Timer Module (PTM), refer to section 9.5.3 page 86 for a detailed description of BCSR[3:4]
- BCSR5 COM 1/2 Port Configuration, refer to section 9.5.4 page 87 for a detailed description of BCSR5.
- BCSR6 Reserved
- BCSR7 PMC, XMC Status/Control
- BCSR8 VME geographical Slot ID, refer to section 9.5.6 page for a detailed description of BCSR8.
- BCSR9 Test Mode, SYSRESET, and WDT Control
- BCSR[10:12] Board Test Registers
- BCSR[13:15] cPLD Flash EPROM Control, Data and Address Registers

The cPLD also provides 8Kb of Flash EEPROM that is controlled via the BCSR's. The organization is two segments of 256x16 each. Kontron reserves segment 0 for its own use. Segment 1 is available for application.

During power up, or whenever VME power is cycled, certain register bits are reloaded from the first two locations of the Kontron reserved area.

An unprogrammed Flash EEPROM returns 0xFFFF for every location read. Any Flash EPROM bit can be programmed from a 1 to a 0, but it can not be programmed from a 0 to a 1. Instead the entire segment must be erased in order to change a 0 bit to a 1. If other data in the erased segment must be preserved it should be moved from the Flash EPROM to some other memory before erasure, and rewritten to the Flash EPROM after the erasure is completed.

Power Sequencer

Refer to section 9.6.1 “Power Sequencer" for a detailed description of the power sequencer.

Reset Generator

Refer to section 9.6.2 “Reset Generator" for a detailed description of the types of resets, and the reset diagram.

4.2.6.13 LPC

The Low Pin Count bus provides the interconnect from the 6300ESB to the BIOS Flash EPROM, Port 80 and the BMC.

4.2.7 BIOS Flash EPROM

The BIOS is stored in a 32-pin, 2Mx8 Flash EPROM. This EPROM may be socketed for debug and code development. The EPROM connects directly to the LPC bus of the 6300ESB.

4.2.8 Port 80

The LPC routes to the 100-contact test connector located on the bottom of the board just behind the front panel. A test board attaches to this connector and is used to support manufacturing, debug, and maintenance.

Please contact Kontron for more information on this functionality.

4.2.9 Board and System Management Controller (BMC and SMC)

The H8S2166 microcontroller provides the BMC function using SMBus components to which it is connected, and provides a user interface using a front panel serial port. Figure 26 on page 32 shows how the microcontroller connects to the SMBus devices.

Note in Figure 26 “Detail B, BMC Block Diagram" page 32 that an SMBus connects to the 82571 Dual Ethernet Controller. This connection provides remote communications capability.

Note from Figure 26 “Detail B, BMC Block Diagram" page 32 that the microcontroller routes one of its GPIO lines to P0 and names that signal PWR_DOWN. The BMC derives its power from +5VSTDBY (see Figure 38 page 92), so if the VMEbus power supply provides +5VSTDBY the BMC will maintain PWR_DOWN while the power supply is turned off.

If the board is installed in slot 1 of the VMEbus it is also the Platform Manager Function via the IPMB and provides the SMB interface to an external System Manager. The Platform Manager monitors and controls the other VMEbus plug-in boards as outlined in the VITA 38 standard. Non-intelligent chassis and system components usually reside on the SMB since the SMB also provides the ALERT* signal. ALERT* is the equivalent of an interrupt.

Note from Figure 26 “Detail B, BMC Block Diagram" page 32 that the BMC also monitors the VMEbus geographical address and VMEbus SYSCON status. The BMC should use the geographical address signals to configure a unique address for each of its own P1-accessible IPMB ports. Each VMEbus geographical address is unique, so if each BMC uses a consistent port address assignment algorithm based on the VMEbus geographical address then no BMC port conflicts should occur. A suggested algorithm is to left shift the geographical address one bit to provide for two ports on a plug-in board. If the BMC detects that this board is the VMEbus System Controller then software for this BMC should also provide the Chassis Controller functions via the SMB.

Chassis components are typically point of measurement (POM) or point of control (POC) devices. As such they tend to be physically scattered throughout the entire physical system. The typical connection medium for such devices is a cable. The cable should connect to a VITA 38 defined 5-pin connector. The 5 pin connector is provided by the VITA 36 RTM for this board. Systems that do not use the RTM will need to provide this connection by some other means.

The BMC has three serial ports, SCI[0:2]:

- SCI0 routes to the ITP Connector,
- SCI1 and SCI2 share COM1 on the TTL side of the EIA 232/458 interface as shown in Figure 27 on page 33.

Mode selection is via GPIO bit, P34, of the BMC. A 1 (default) selects Mode B which connects the 6300ESB to COM1 and BMC SCI2 simply monitors RXD looking for the correct escape sequence to switch modes. If the BMC software detects the correct escape sequence it switches to Mode A which connects SCI1 to COM1 and the 6300ESB, SP0, to SCI2 for serial-over-LAN redirection of the BIOS or OS console.

4.2.10 Interrupts

The onboard interrupt routing is fully described in section 9.7 “Interrupts Management" page 95.

Chapter 5 - Hardware Configuration

When setting jumpers, avoid touching areas of integrated circuitry; static discharge can damage circuits.

To ensure proper operation of the PENTXM2 or PENTXM4 board, you may need to check its two jumpers configuration. Figure 28 illustrates the placement of the jumpers on the board and their default settings.

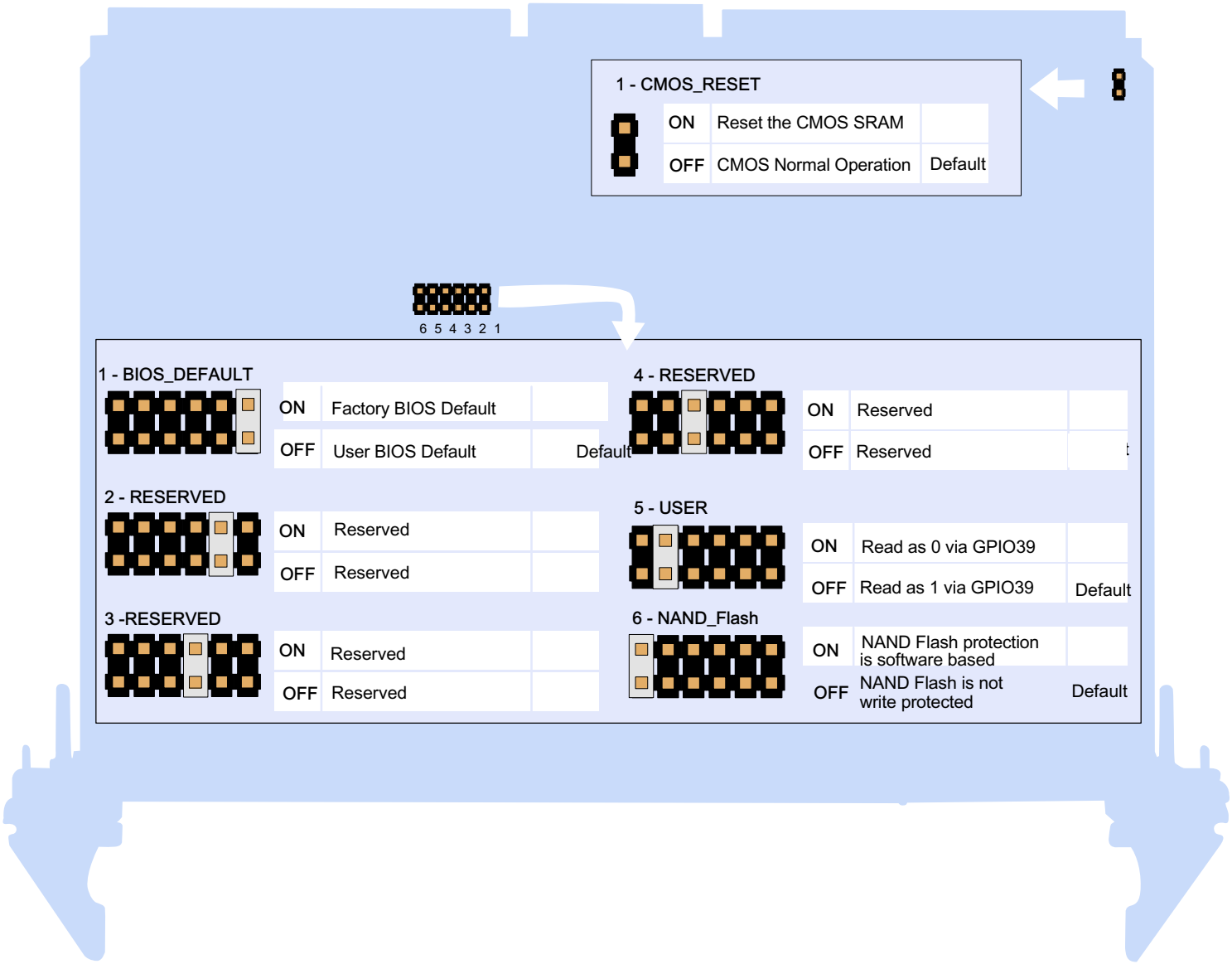


Figure 28: PENTXM2 or PENTXM4 Jumpers Locations and Default Settings

5.1 CMOS SRAM Reset

Temporarily install the jumper to reset the CMOS SRAM. Remove the jumper for normal operation.

Location	Name	Connects to	Default Setting	Description
1	CMOS_RESET	6300ESB RTCRST#	ON	Reset the CMOS SRAM
			OFF	**Default configuration:** CMOS normal operation

Table 3: Jumper Description: CMOS SRAM Reset

5.2 BIOS Defaults

This jumper (BIOS_DEFAULT) selects th BIOS defaults:

Location	Name	Connects to	Default Setting	Description
1	BIOS_DEFAULT	6300ESB GPIO2	ON	Factory BIOS defaults
			OFF	**Default configuration:** User BIOS defaults

Table 4: Jumper Description: BIOS Defaults

5.3 User Specific

This jumper (USER) is user specific, its state is read via GPIO30:

Location	Name	Connects to	Default Setting	Description
5	USER	6300ESB GPIO39	ON	Reserved for user, read as 0 via GPIO39
			OFF	**Default configuration:** Reserved for user, read as 1 via GPIO39

Table 5: Jumper Description: User Specific

5.4 NAND Flash Protection

GPIO23 connects to the WP_PD# bit of the the SST55LD019 to invoke hardware write protection via a specific jumper (NAND_Flash).

- If the jumper is removed the entire NAND Flash is not write protected.
- If the jumper is installed and GPIO23 is logic 1 the NAND Flash is not write protected..
- If the jumper is installed and GPIO23 is logic 0 all Flash memory is protected.

Location	Name	Connects to	Default Setting	Description
6	NAND-Flash	6300ESB GPIO23	ON	NAND Flash protection is software based.
			OFF	**Default configuration:** NAND Flash is not write protected.

Table 6: Jumper Description: NAND Flash Protection

The only way to control the NAND Flash write protection is to do it by software with the jumper installed, by hndling the GPIO23.

In the Linux RHEL4 BSP, a driver is provided to handle the user's GPIO: GPIO41, GPIO42 and GPIO43. The GPIO23 could be managed (output only) by adapting this driver (more detail available in section 6.5.9 “User's GPIO" in the “Release Notes RHEL4 for PENTXM2 and PENTXM4 Board - SD.DT.E82").

Chapter 6 - Connectors

This chapter gives the pin assignment and signal descriptions for the PENTXM2 or PENTXM4 connectors.

The first section 6.1 “Onboard Connectors" describes the pin assignments for the onboard connectors (P0, P1, P2, P6, J11-J14, J21-J24 and J25).

The last section 6.2 “Front Panel Connectors" gives the pin assignment and a description of the front panel connectors (SERIAL, ETH0, ETH1 and USB).

6.1 Onboard Connectors

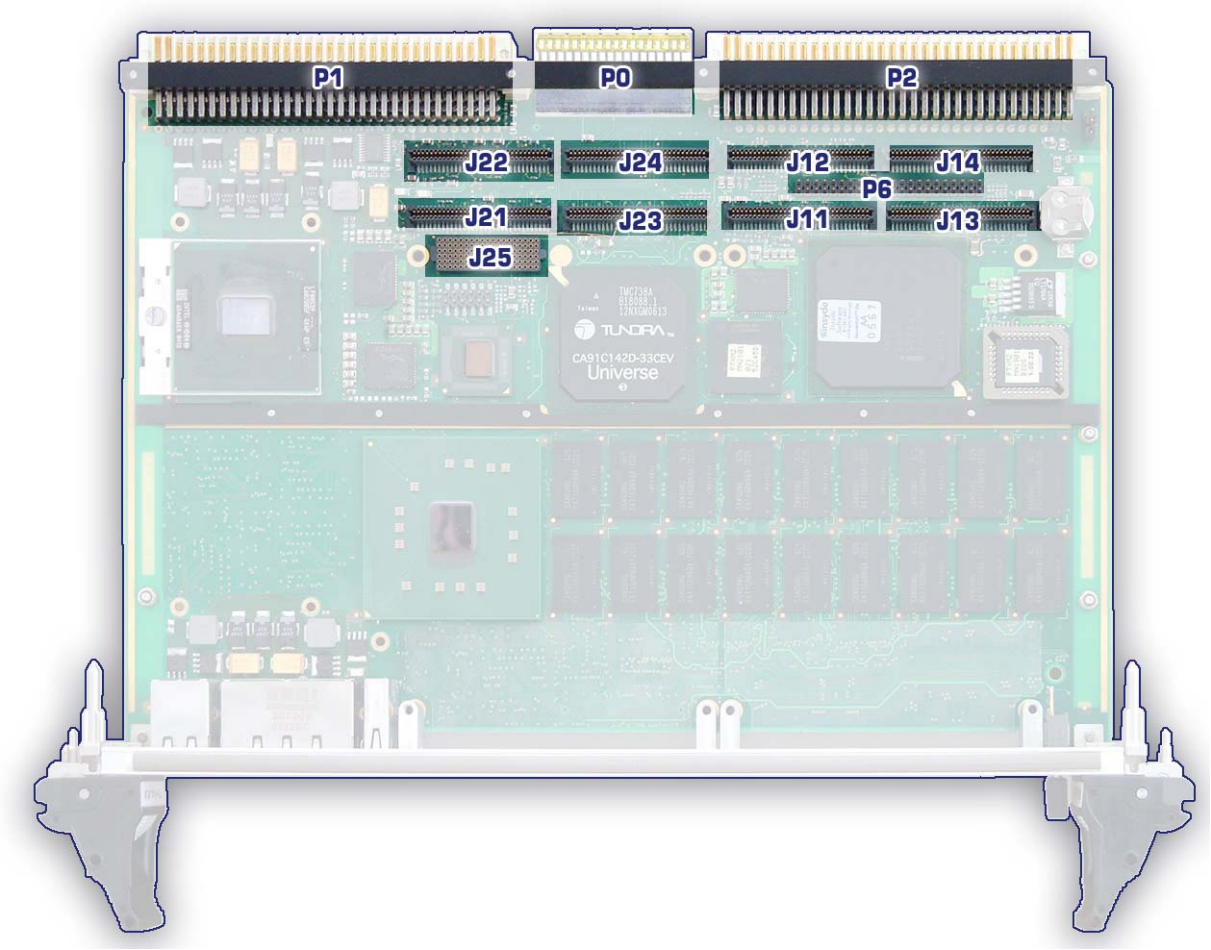


Figure 29: PENTXM2 or PENTXM4 Onboard Connector Locations

6.1.1 P0 Connector Pin Assignment

Pin	P0 connector					
	Row a	Row b	Row c	Row d	Row e	Row f (2)
1	PMC2 IO 39 (1)	PMC2 IO 38 (1)	PMC2 IO 37 (1)	PMC2 IO 36 (1)	PMC2 IO 35 (1)	GND
2	ETH1 BI_DA+	ETH1 BI_DA-	GND	ETH1 BI_DC+	ETH1 BI_DC-	GND
3	ETH1 BI_DB+	ETH1 BI_DB-	GND	ETH1 BI_DD+	ETH1 BI_DD-	GND
4	ETH0 BI_DA+	ETH0 BI_DA-	GND	ETH0 BI_DC+	ETH0 BI_DC-	GND
5	ETH0 BI_DB+	ETH0 BI_DB-	GND	ETH0 BI_DD+	ETH0 BI_DD-	GND
6	RESET#	USB1 PWR	PWR DOWN	Reserved	USB0 PWR	GND
7	USB1 DA+	USB1 DA-	GND	USB0 DA+	USB0 DA-	GND
8	SATA0 TX+	SATA0 TX-	GND	SATA0 RX+	SATA0 RX-	GND
9	SATA1 TX+	SATA1 TX-	GND	SATA1 RX+	SATA1 RX-	GND
10	PMC2 IO 34 (1)	PMC2 IO 33 (1)	6300 ESB GPIO41	6300 ESB GPIO42	6300 ESB GPIO43	GND
11	PMC2 IO 58	PMC2 IO 60	PMC2 IO 46	PMC2 IO 48	PMC2 IO 50	GND
12	PMC2 IO 62	PMC2 IO 64	PMC2 IO 45	PMC2 IO 52	PMC2 IO 54	GND
13	PMC2 IO 61	PMC2 IO 63	PMC2 IO 56	PMC2 IO 51	PMC2 IO 53	GND
14	PMC2 IO 57	PMC2 IO 59	PMC2 IO 55	PMC2 IO 47	PMC2 IO 49	GND
15	PEX RXL0+	PEX RXL0-	GND	PEX TXL0+	PEX TXL0-	GND
16	PEX RXL1+	PEX RXL1-	GND	PEX TXL1+	PEX TXL1-	GND
17	PEX RXL2+	PEX RXL2-	GND	PEX TXL2+	PEX TXL2-	GND
18	PEX RXL3+	PEX RXL3-	GND	PEX TXL3+	PEX TXL3-	GND
19	PMC2 IO 44 (1)	PMC2 IO 43 (1)	PMC2 IO 42 (1)	PMC2 IO 41 (1)	PMC2 IO 40 (1)	GND

Table 7: P0 Connector Pin Assignment

(1) In the column 1, 10 and 19, they may be signals or Not Connected (N.C.). The default is the signals listed. The N.C. option is made available by removing three, 0-ohm resistor packs. Please contact Kontron for more information on this topic.

(2) The **f** row is the metal shielded on the outside P0 connector.

6.1.2 P0 Signal Description

Mnemonic	Signal Description
6300 ESB GPIO*xx*	GPIO *xx* from 6300 ESB
ETH*x* BI_DA+/-	Ethernet *x*: First pair of Transmit/Receive data.
ETH*x* BI_DB+/-	Ethernet *x*: Second pair of Transmit/Receive data.
ETH*x* BI_DC+/-	Ethernet *x*: Third pair of Transmit/Receive data.
ETH*x* BI_DD+/-	Ethernet *x*: Fourth pair of Transmit/Receive data.
GND	Ground
N.C.	Not Connected
PEX RXL*y*+/-	x4 PCI Express Link - Receive+/- Lane *y*
PEX TXL*y*+/-	x4 PCI Express Link - Transmit+/- Lane *y*
PMC2 IO *yy*	PMC Site 2 I/o signal *yy*
PWR DOWN	Power Down from the BMC
RESET	Board Reset Signal
Reserved	Reserved. Do not use
SATA*x* RX+/RX-	Serial ATA *x* Receive +/-
SATA*x* TX+/TX-	Serial ATA *x* Transmit +/-
USB*x* DA+/-	Differential Data Pair of USB Line *x*
USB*x* PWR	USB Line *x*

Table 8: P0 Signal Description

6.1.3 P1 and P2 Row b (VMEbus) Connector Pin Assignment

Pin	P1					P2
	Row z	Row a	Row b	Row c	Row d	Row b
1	N.C.	D00	BBSY*	D08	+5V	+5V
2	GND	D01	BCLR*	D09	GND	GND
3	N.C.	D02	ACFAIL*	D10	N.C.	RETRY*
4	GND	D03	BG0IN*	D11	N.C.	A24
5	N.C.	D04	BG0OUT*	D12	N.C.	A25
6	GND	D05	BG1IN*	D13	N.C.	A26
7	N.C.	D06	BG1OUT*	D14	N.C.	A27
8	GND	D07	BG2IN*	D15	N.C.	A28
9	N.C.	GND	BG2OUT*	GND	GAP*ě	A29
10	GND	SYSCLK	BG3IN*	SYSFAIL*	GA0*ě	A30
11	N.C.	GND	BG3OUT*	BERR*	GA1*ě	A31
12	GND	DS1*	BR0*	SYSRESET*	+3.3V	GND
13	N.C.	DS0*	BR1*	LWORD*	GA2*ě	+5V
14	GND	WRITE*	BR2*	AM5	+3.3V	D16
15	N.C.	GND	BR3*	A23	GA3*ě	D17
16	GND	DTACK*	AM0	A22	+3.3V	D18
17	N.C.	GND	AM1	A21	GA4*ě	D19
18	GND	AS*	AM2	A20	+3.3V	D20
19	N.C.	GND	AM3	A19	SMB_SCL	D21
20	GND	IACK*	GND	A18	+3.3V	D22
21	N.C.	IACKIN*	IPMB_SCL	A17	SMB_SDA	D23
22	GND	IACKOUT*	IPMB_SDA	A16	+3.3V	GND
23	N.C.	AM4	GND	A15	SMB_ALERT*	D24
24	GND	A07	IRQ7*	A14	+3.3V	D25
25	N.C.	A06	IRQ6*	A13	N.C.	D26
26	GND	A05	IRQ5*	A12	+3.3V	D27
27	N.C.	A04	IRQ4*	A11	N.C.	D28
28	GND	A03	IRQ3*	A10	+3.3V	D29
29	N.C.	A02	IRQ2*	A09	N.C.	D30
30	GND	A01	IRQ1*	A08	+3.3V	D31
31	N.C.	-12V	+5V_STANDBY	+12V	GND	GND
32	GND	+5V	+5V	+5V	+5V	+5V

* VME signals active when low.

‡ Geographical address pins, refer to section 6.1.4 page 49 for more information.

Table 9: P1 and P2 (Row B) Connector Pin Assignment

Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. If such conditions occur, *toxic fumes* may be produced due to the destruction of components.

Only use the PENTXM2 or PENTXM4in VME IEEE1014x or VME64 backplanes that supply power on both P1 and P2 connectors. Failure to observe this warning may result in damage to the board.

6.1.4 Geographical Address Pin Assignment

The 6 geographical address pins (GA0*, GA1*, GA2*, GA3*, GA4* and GAP*) shall be tied to ground or left open (floating) on the backplane J1 connector as defined in the table below.

Slot Number	GAP* Pin	GA4* Pin	GA3* Pin	GA2* Pin	GA1* Pin	GA0* Pin
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
10	GND	Open	GND	Open	GND	Open
11	Open	Open	GND	Open	GND	GND
12	GND	Open	GND	GND	Open	Open
13	Open	Open	GND	GND	Open	GND
14	Open	Open	GND	GND	GND	Open
15	GND	Open	GND	GND	GND	GND
16	Open	GND	Open	Open	Open	Open
17	GND	GND	Open	Open	Open	GND
18	GND	GND	Open	Open	GND	Open
19	Open	GND	Open	Open	GND	GND
20	GND	GND	Open	GND	Open	Open
21	Open	GND	Open	GND	Open	GND

The device that samples the levels of the geographical address pins will read the inverted value of the slot number into which the board is plugged. When the board is powered on without being plugged into a VME/VME64 backplane the slot number will be zero with a parity error (GAP* open).

6.1.5 VMEbus Signal Description

The VMEbus signals occupy rows a, b and c of the P1 connector and row b of the P2 connector.

Mnemonic	Signal Description
A01 to A15	**Address Bus (bits 1 to 15)**. Address lines that are used to broadcast a short, standard or extended address.
A16 to A23	**Address Bus (bits 16 to 23)**. Address lines that are used in conjunction with A01-A15 to broadcast a standard or extended address.
A24 to A31	**Address Bus (bits 24 to 31)**. Address lines that are used in conjunction with A01-A23 to broadcast an extended address.
ACFAIL*	**AC Failure**. This signal indicates when the AC input to the power supply is no longer being provided or that the required AC input voltage levels are not being met.
AM0 to AM5	**Address Modifier (bits 0 to 5)**. These signals are used to broadcast information such as the address size, cycle type, master identification or any combination of these.
AS*	**Address Strobe**. This signal indicates when a valid address has been placed on the address bus.
BBSY*	**Bus Busy**. This signal is driven low by the requester associated with the current bus master to indicate that its master is using the bus.
BCLR*	**Bus Clear**. This signal is generated by an arbiter to indicate that there is a higher priority request for the bus than the one being processed. This signal requests the current master to release the bus.
BERR*	**Bus Error**. This signal is generated by a slave or bus timer to tell the master that the data transfer was not completed.
BG0IN* to BG3IN*	**Bus Grant (0 to 3) In**. These signals are generated by the arbiter to tell the board receiving it that if it is requesting the bus on that level, then it has been granted use of the bus. Otherwise the board should pass the signal down the daisy chain. The BGxIN*/BGxOUT* signals form the bus grant daisy chain, i.e. the BGxOUT* of one board forms the BGxIN* of the next board in the daisy chain.
BG0OUT* to BG3OUT*	**Bus Grant (0 to 3) Out**. These signals are generated by requesters to tell the next board in the daisy chain that if it is requesting the bus on that level, then it may use the bus. Otherwise the board should pass the signal down the daisy chain.
BR0* to BR3*	**Bus Request (0 to 3)**. A low level, generated by a requester, on one of these lines, shows that some master needs to use the bus.
D00 to D31	**Data Bus (0 to 31)**. These signals are used to transfer data between masters and slaves, and status/ID information from interrupters to interrupt handlers.

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Mnemonic	Signal Description
DS0*, DS1*	**Data Strobe 0, 1**. These signals are used with LWORD* and A01 to show how many byte locations are being accessed (1, 2, 3 or 4). Also, during a write cycle, the falling edge of the first data strobe shows that valid data is available on the bus. On a read cycle, the rising edge of the first data strobe shows that data has been accepted from the data bus.
DTACK*	**Data Transfer Acknowledge**. This signal is generated by a slave. The falling edge shows that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle. The rising edge shows that the slave has released the data bus at the end of a read cycle.
GA0* to GA4* and GAP*	Geographical address pins (refer to the table in section 6.1.4). These pins indicate to the VME board which one of the backplane slot it currently uses (0 to 21).
GND	The DC voltage reference for the system.
IACK*	**Interrupt Acknowledge**. This signal is used by the interrupt handler to acknowledge an interrupt request. It is routed to the IACKIN* pin of slot 1, where it is monitored by the IACK daisy chain driver.
IACKIN*	**Interrupt Acknowledge In**. This signal tells the board receiving it that board can respond to the interrupt acknowledge cycle in process or pass it down the daisy chain. IACKIN*/IACKOUT* form the interrupt acknowledge daisy chain.
IACKOUT*	**Interrupt Acknowledge Out**. This signal is sent by a board to tell the next board in the daisy chain that it can respond to the interrupt acknowledge cycle in progress.
IPMB_SCL	Intelligent Platform Management Bus - Clock I2C
IPMB_SDA	Intelligent Platform Management Bus - Data I2C
IRQ1* to IRQ7*	**Interrupt Request (1 to 7)**. These signals are driven low by interrupters to request an interrupt on the corresponding level.
LWORD*	**Longword**. This signal is used with DS0*, DS1* and A01 to select which byte location(s) within the 4-byte group are accessed during the data transfer.
N.C.	This pin is not connected.
SMB_ALERT*	System Management Bus - Alert
SMB_SCL	System Management Bus - Serial clock line from the SMBus master to SMBus slave devices.
SMB_SDA	System Management Bus - Bi-directional serial data line between the SMBus master and the SMBus slave device.
SYSCLK	**System Clock**. This signal provides a constant 16 MHz clock signal that is independent of any other bus timing.

Mnemonic	Signal Description
SYSFAIL*	**System Fail**. This signal shows that a failure has occurred in the system. It can be generated by any board in the system. It is also asserted after a reset and released when the board reset self-tests are passed successfully.
SYSRESET*	**System Reset**. When this signal is low, it causes the system to be reset.
WRITE*	**Write**. This signal is generated by a master to show whether the data transfer cycle is a read or a write.
+3.3V	+3.3 Volts DC power.
+5V	+5 Volts DC power
+12V	+12 Volts DC power.
-12V	-12 Volts DC power.
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Table 10: VME Signal Description

6.1.6 P2 Connector Pin Assignment

Pin	Row z	Row a	Row b	Row c	Row d
1	PMC2 IO 02	PMC1 IO 02	+5V	PMC1 IO 01	PMC2 IO 01
2	GND	PMC1 IO 04	GND	PMC1 IO 03	PMC2 IO 03
3	PMC2 IO 05	PMC1 IO 06	RETRY*	PMC1 IO 05	PMC2 IO 04
4	GND	PMC1 IO 08	A24	PMC1 IO 07	PMC2 IO 06
5	PMC2 IO 08	PMC1 IO 10	A25	PMC1 IO 09	PMC2 IO 07
6	GND	PMC1 IO 12	A26	PMC1 IO 11	PMC2 IO 09
7	PMC2 IO 11	PMC1 IO 14	A27	PMC1 IO 13	PMC2 IO10
8	GND	PMC1 IO 16	A28	PMC1 IO 15	PMC2 IO12
9	PMC2 IO 14	PMC1 IO 18	A29	PMC1 IO 17	PMC2 IO 13
10	GND	PMC1 IO 20	A30	PMC1 IO 19	PMC2 IO 15
11	PMC2 IO 17	PMC1 IO 22	A31	PMC1 IO 21	PMC2 IO 16
12	GND	PMC1 IO 24	GND	PMC1 IO 23	PMC2 IO 18
13	PMC2 IO 20	PMC1 IO 26	+5V	PMC1 IO 25	PMC2 IO 19
14	GND	PMC1 IO 28	D16	PMC1 IO 27	PMC2 IO 21
15	PMC2 IO 23	PMC1 IO 30	D17	PMC1 IO 29	PMC2 IO 22
16	GND	PMC1 IO 32	D18	PMC1 IO 31	PMC2 IO 24
17	PMC2 IO 26	PMC1 IO 34	D19	PMC1 IO 33	PMC2 IO 25
18	GND	PMC1 IO 36	D20	PMC1 IO 35	PMC2 IO 27
19	PMC2 IO 29	PMC1 IO 38	D21	PMC1 IO 37	PMC2 IO 28
20	GND	PMC1 IO 40	D22	PMC1 IO 39	PMC2 IO 30
21	PMC2 IO 32	PMC1 IO 42	D23	PMC1 IO 41	PMC2 IO 31
22	GND	PMC1 IO 44	GND	PMC1 IO 43	S0_TX/TX- (1)
23	S1_TX/TX- (1)	PMC1 IO 46	D24	PMC1 IO 45	S0_RX/RX- (1)
24	GND	PMC1 IO 48	D25	PMC1 IO 47	S0_RTS/TX+ (2)
25	S1_RX/RX- (1)	PMC1 IO 50	D26	PMC1 IO 49	S0_CTS/RX+ (2)
26	GND	PMC1 IO 52	D27	PMC1 IO 51	S0_DTR/DIR (2)
27	S1_RTS/TX+ (2)	PMC1 IO 54	D28	PMC1 IO 53	S0_DSR
28	GND	PMC1 IO 56	D29	PMC1 IO 55	S0_DCD
29	S1_CTS/RX+ (2)	PMC1 IO 58	D30	PMC1 IO 57	S1_DSR
30	GND	PMC1 IO 60	D31	PMC1 IO 59	S1_DCD
31	S1_DTR/DIR (3)	PMC1 IO 62	GND	PMC1 IO 61	GND
32	GND	PMC1 IO 64	+5V	PMC1 IO 63	+5V

* Signals active when low.

(1) The serial I/O Tx and Rx pins act as either single-ended signal for EIA-232 or one side differential pair for EIA-422/485.

(2) In EIA-422/485 modes, CTS and RTS act as the other side of the differental pair for Rx and Tx respectively.

(3) In EIA-485 mode, DTR acts as direction control/indicator.

Table 11: P2 Connector Pin Assignment

6.1.7 P2 Signal Description

The VME signals (row b) are described in section 6.1.5.

Mnemonic	Signal Description
GND	Ground
N.C.	Pin not connected. Reserved
PMC1 IO yy	PMC Site 1 I/O signal *yy*
PMC2 IO yy	PMC Site 2 I/O signal *yy*
S*x*_RX/RX-	Channel EIA-232 *x* Receive Data The signal acts as one side differential pair for EIA-422/485
S*x*_TX/TX-	Channel EIA-232 *x* Transmit Data The signal acts as one side differential pair for EIA-422/485
S*x*_CTS/RX+	Channel EIA-232 Clear To Send The signal acts as the other side of the differential pair for EIA-422/485
S*x*_RTS/TX+	Channel EIA-232 Ready to Send The signal acts as the other side of the differential pair for EIA-422/485
S*x*_DCD	Channel EIA-232 Data Carrier Detect
S*x*_DSR	Channel EIA-232 Data Set Ready
S*x*_DTR/DIR	Channel EIA-232 Data Terminal ready In EIA-485 mode, the signal acts as direction/control indicator.
+5V	+5 Volts DC power

Table 12: P2 Signal Description

6.1.8 PMC J11 and J21 Connector Pin Assignments

Pin	Signal	Pin	Signal
1	N.C.	2	-12V
3	GNG	4	INTA#
5*	INTB#	6	INTC#
7	BUSMODE1#	8	+5V
9	INTD#	10	N.C.
11	GND	12	+3.3V_SUS
13	CLK	14	GND
15	GND	16	GNT#
17	REQ#	18	+5V
19	V(I/0) (1)	20	AD[31]
21	AD[28]	22	AD[27]
23	AD[25]	24	GND
25	GND	26	C/BE3#
27	AD[22]	28	AD[21]
29	AD[19]	30	+5V
31	V(I/0) (1)	32	AD[17]
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	+5V
39	PCIXCAP	40	LOCK#
41	SDONE#	42	SBO#
43	PAR	44	GND
45	V(I/O) (1)	46	AD[15]
47	AD[12]	48	AD[11]
49	AD[09]	50	+5V
51	GND	52	C/BE0#
53	AD[06]	54	AD[05]
55	AD[04]	56	GND
57	V(I/O) (1)	58	AD[03]
59	AD[02]	60	AD[01]
61	AD[00]	62	+5V
63	GND	64	REQ64#

(1) V(I/O) is 3.3V only. Neither PMC site provides a 3.3V keying pin

PCI signals active when low.

Table 13: PMC J11 and J21 Connector Pin Assignment

6.1.9 PMC J12 and J22 Connector Pin Assignments

Pin	Signal	Pin	Signal
1	+12V	2	N.C.
3	Pulled to +3.3V via 10K	4	Pulled to +3.3V via 10K
5	Pulled to +3.3V via 10K	6	Ground
7	GND	8	N.C.
9	N.C.	10	N.C.
11	Pulled to +3.3V via 2.7K	12	+3.3V
13	RST#	14	GND
15	+3.3V	16	GND
17	N.C.	18	GND
19	AD[30]	20	AD[29]
21	GND	22	AD[26]
23	AD[24]	24	+3.3V
25	IDSEL	26	AD[23]
27	+3.3V	28	AD[20]
29	AD[18]	30	GND
31	AD[16]	32	C/BE2#
33	GND	34	IDSEL B (1)
35	TRDY#	36	+3.3V
37	GND	38	STOP#
39	PERR#	40	GND
41	+3.3V	42	SERR#
43	C/BE1#	44	GND
45	AD[14]	46	AD[13]
47	M66EN	48	AD[10]
49	AD[08]	50	+3.3 V
51	AD[07]	52	REQ B# (1)
53	+3.3V	54	GNT B# (1)
55	PMC-RSVD	56	GND
57	PMC-RSVD	58	EREADY
59	GND	60	N.C.
61	ACK64#	62	+3.3V
63	GND	64	N.C.

(1) IDSEL B, REQ B# and GNT B# are provided for use by dual-function PMC modules or processor-PMC modules

PCI signals active when low.

Table 14: PMC J12 and J22 Connector Pin Assignment

6.1.10 PMC J13 and J23 Connector Pin Assignments

Pin	Signal	Pin	Signal
1	N.C.	2	GND
3	GND	4	C/BE7#
5	C/BE6#	6	C/BE5#
7	C/BE4#	8	GND
9	V(I/O)	10	PAR64
11	AD[63]	12	AD[62]
13	AD[61]	14	GND
15	GND	16	AD[60]
17	AD[59]	18	AD[58]
19	AD[57]	20	GND
21	V(I/O)	22	AD[56]
23	AD[55]	24	AD[54]
25	AD[53]	26	GND
27	GND	28	AD[52]
29	AD[51]	30	AD[50]
31	AD[49]	32	GND
33	GND	34	AD[48]
35	AD[47]	36	AD[46]
37	AD[45]	38	GND
39	V(I/O)	40	AD[44]
41	AD[43]	42	AD[42]
43	AD[41]	44	GND
45	GND	46	AD[40]
47	AD[39]	48	AD[38]
49	AD[37]	50	GND
51	GND	52	AD[36]
53	AD[35]	54	AD[34]
55	AD[33]	56	GND
57	V(I/O)	58	AD[32]
59	N.C.	60	N.C.
61	N.C.	62	GND
63	GND	64	N.C.

PCI signals active when low.

Table 15: PMC J13 and J23 Connector Pin Assignment

6.1.10.1 PMC J14 and J24 Connector Pin Assignment

Pin	Signal	Pin	Signal
1	PMC IO 01	2	PMC IO 02
3	PMC IO 03	4	PMC IO 04
5	PMC IO 05	6	PMC IO 06
7	PMC IO 07	8	PMC IO 08
9	PMC IO 09	10	PMC IO 10
11	PMC IO 11	12	PMC IO 12
13	PMC IO 13	14	PMC IO 14
15	PMC IO 15	16	PMC IO 16
17	PMC IO 17	18	PMC IO 18
19	PMC IO 19	20	PMC IO 20
21	PMC IO 21	22	PMC IO 22
23	PMC IO 23	24	PMC IO 24
25	PMC IO 25	26	PMC IO 26
27	PMC IO 27	28	PMC IO 28
29	PMC IO 29	30	PMC IO 30
31	PMC IO 31	32	PMC IO 32
33	PMC IO 33	34	PMC IO 34
35	PMC IO 35	36	PMC IO 36
37	PMC IO 37	38	PMC IO 38
39	PMC IO 39	40	PMC IO 40
41	PMC IO 41	42	PMC IO 42
43	PMC IO 43	44	PMC IO 44
45	PMC IO 45	46	PMC IO 46
47	PMC IO 47	48	PMC IO 48
49	PMC IO 49	50	PMC IO 50
51	PMC IO 51	52	PMC IO 52
53	PMC IO 53	54	PMC IO 54
55	PMC IO 55	56	PMC IO 56
57	PMC IO 57	58	PMC IO 58
59	PMC IO 59	60	PMC IO 60
61	PMC IO 61	62	PMC IO 62
63	PMC IO 63	64	PMC IO 64

Table 16: PMC J14 and J24 Connector Pin Assignment

6.1.11 PMC Signal Description

Mnemonic	Signal Description
AD[00] to AD[63]	Address/Data bits. Multiplexed address and data bus. AD32 to AD63 are specifics to 64-bit bus extension.
ACK64#	Acknowledge 64-bit Transfer. Driven low by the device to indicate that the target is willing to transfer data using 64 bits.
BUSMODE1#	Bus Mode 1. Driven low by a PMC module to indicate that it supports the current bus mode
C/BE0# to C/BE7#	Command/Byte Enables. During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase the signals are byte enables that specify the active bytes on the bus. C/BE4# to C/BE7# are specifics to 64-bit bus extension.
CLK	Clock. Except RST*, the 64-bit PCI bus signals are synchronous to 33 or 66 MHz clock.
DEVSEL#	Device Select. Driven low by a PCI agent to signal that it has decoded its address as the target of the current access.
FRAME#	FRAME. Driven low by the current master to signal the start and duration of an access.
EREADY	EREADY. Output of non-monarch PPMCs that indicates it has completed its onboard initialization and can respond to PCI bus enumeration by the monarch via configuration cycles. Input to the monarch PPMC that indicates all non-monarch PPMCs have completed their onboard initialization and can respond to PCI bus enumeration by the monarch via configuration cycles.
GNT#	Grant. Driven low by the arbiter to grant PCI bus ownership to a PCI agent. GNT B# is provided for use by dual-function PMC modules or processor-PMC modules.
IDSEL	Initialization Device Select. Device chip select during configuration cycles. IDSEL B is provided for use by dual-function PMC modules or processor-PMC modules.
INTA# to INTD#	Interrupt lines. Level-sensitive, active-low interrupt requests.
IRDY#	Initiator Ready. Driven low by the initiator to signal its ability to complete the current data phase.
LOCK#	LOCK. Driven low to indicate an atomic operation that may require multiple transactions to complete.
M66EN	66 MHZ Enable. Indicates to a device if the bus segment is operating at 66 or 33 MHz. If it is high then the bus speed is 66 MHz and if it is low then the bus speed is 33 MHz.
N.C.	This pin is not connected.
PAR	Parity. Parity protection bit for AD0 to AD31 and C/BE0# to C/BE3#.
PAR64	Parity Upper DWORD. Parity protection bit for AD32 to AD63 and C/BE4# to C/BE7#.
PERR#	Parity Error. Driven low by a PCI agent to signal a parity error.
PMC IO 01 to PMC IO 64	64-bit PCI bus PMC 64 signals. Used to transmit I/O signals from PCI 64 PMC connector (J14) to P2 connector.
PMC-RSVD	Reserved. Do not connect this pin.

Mnemonic	Signal Description
REQ#	Request. Driven low by a PCI agent to request ownership of the PCI bus. REQ B# is provided for use by dual-function PMC modules or processor-PMC modules.
REQ64#	Request 64-bit Transfer. Driven low by the current bus master, indicates that it desires to transfer data using 64 bits.
RST#	Reset. Driven low to reset the PCI bus.
SBO#	Snoop Backoff. Indicates a hit of a modified line asserted.
SDONE#	Snoop Done. Indicates the status of the snoop for the current access.
SERR#	System Error. Driven low by a PCI agent to signal a system error.
STOP#	STOP. Driven low by a PCI target to signal a disconnect or target-abort.
TRDY#	Target Ready. Driven low by the current target to signal its ability to complete the current data phase.
V(I/O)	Power supply delivered by the board. On the PCI 64 PMC slots, +3.3 Volts power is supplied. +5 Volts signaling PMCs are not supported. Contact Kontron for more information.
+3.3V	+3.3 Volts DC power
+5V	+5 Volts DC power
+12V	+12 Volts DC power
-12V	-12 Volts DC power

Page 2 of 2

Table 17: PMC Signal Description

6.1.12 XMC J25 Connector Pin Assignments

One XMC site is provided to allow the installation of a VITA 42.3, PCI-Express mezzanine card. The signals assignments are as shown in the following table. The encoding for GA[2:0] should not conflict with other SMbus/IPMI devices.

VPWR is +12V with a build option for +5V.

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR (1)
4	GND	GND	TCK	GND	GND	MRSTO#
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR
6	GND	GND	TMS	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR
8	GND	GND	TDI	GND	GND	-12V
9	N.C.	N.C.	N.C.	N.C.	N.C.	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	PER0p0	PER0n0	MBIST#	PER0p1	PER0n1	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PER0p2	PER0n2	3.3V	PER0p3	PER0n3	VPWR
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	NC	PER0p5	PER0n5	VPWR
16	GND	GND	MVRMO	GND	GND	MSCL
17	PER0p6	PER0n6	N.C.	PER0p7	PER0n7	N.C.
18	GND	GND	N.C.	GND	GND	N.C.
19	REFCLK+0	REFCLK-0	N.C.	N.C.	N.C.	N.C.

(1) VPWR is connected to +12V via a 0 ohm resistor. The 5V option is available, please contact Kontron for more information on this topic.

Signals active when low.

Table 18: XMC J25 Connector Pin Assignments

6.1.13 XMC Signal Description

Mnemonic	Signal Description
MSCL	IPMI I2C serial Clock. Clock reference to the XMC mezzanine card for a two-wire serial management bus.
MSDA	IPMI I2C serial Data. Data line for a two-wire serial management bus.
GA[0..2]	I2C Channel Select. Address a specific XMC slot on an IPMI I2C bus shared by multiple XMCs
MBIST	XMC Bult In Self Test. Determine whether an XMC has completed its build-in self test.
MVMRO	XMC Write Prohibit. XMC shall disable write to non-volatile memory on the XMC when this signal is asserted high.
MRSTI#	XMC Reset In. The mezzanine card shall initiate itself into a known state when this signal is asserted low by the carrier.
MRSTO#	XMC Reset Out. This signal provides an input to the carrier's reset logic in order to support a reset button or other reset source ont the XMC.
MPRESENT#	Module Present. This signal allows the carrier to determine whether an XMC is present.
PER0p/n[0..7]	Link 0 Differential Receive. These signals are used by the XMC to receive high-speed protocol-specific data FROM the carrier over the PCI Express interface.
PET0p/n[0..7]	Link 0 Differential Transmit. These signals are used by the XMC to receive high-speed protocol-specific data TO the carrier over the PCI Express interface.
TRSRT#	JTAG Reset. This signal shall provide for asynchronous initialization of the TAP controller on the XMC.
TCK	JTAG Clock. This signal shall provide an independent clock reference for TAP controller operation.
TMS	JATG Mode Select . This signal shall provide state control of the TAP controller on the XMC.
TDI	JTAG Data In. This signal shall provide for serial writes of test data and instructions into the XMC.
TDO	JATG Data Out. This signal shall provide or serial writes of test data and instructions out of the XMC.
VPWR	Power Pins. These signals carry either 12V or 5V power from the carrier to the XMC.

Table 19: XMC Signal Description

6.1.14 Onboard Mass Storage Connector (P6) Pin Assignments

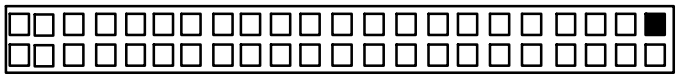


Figure 30: Mass Storage Connector

Pin	Signal	Pin	Signal
1	IDE RESET#	2	GND
3	IDE DD7	4	IDE DD8
5	IDE DD6	6	IDE DD9
7	IDE DD5	8	IDE DD10
9	IDE DD4	10	IDE DD11
11	IDE DD3	12	IDE DD12
13	IDE DD2	14	IDE DD13
15	IDE DD1	16	IDE DD14
17	IDE DD0	18	IDE DD15
19	GND	20	3.3V
21	IDE DMARQ	22	GND
23	IDE DIOW#	24	GND
25	IDE DIOR	26	GND
27	IDE IORDY	28	N.C.
29	IDE DMACK#	30	GND
31	IDE INTRQ	32	N.C.
33	IDE DA1	34	IDE PDIAG#
35	IDE DA0	36	IDE DA2
37	IDE CS0#	38	IDE CS1#
39	IDE DASP#	40	GND
41	+5V	42	+5V
43	GND	44	N.C.

Signals active when low.

Table 20: Onboard Mass Storage Connector (P6) Pin Assignments

6.1.15 Onboard Mass Storage Signal Description

Mnemonic	Signal Description
IDE CS*x*	Drive Chip Select *x*
IDE DASP	Drive active/driver 1 Present
IDE DA*x*	Drive Address Bus - *bit x*
IDE DD*x*	IDE Drive Data Bus - *bit x*
IDE DIOR	Drive I/O Read
IDE DIOW	Drive I/O Write
IDE DMACK	DMA Acknowledge
IDE DMARQ	DMA Request
IDE INTRQ	Drive Interrupt
IDE IORDY	I/O Channel Ready
IDE PDIAG	Passed Diagnostics
IDE RESET	Drive Reset

Table 21: Onboard Mass Storage Signal Description

6.1.16 ITP Debug and Diagnostics Connector Pin Assignments

This connector is reserved for a Kontron usage (manufacturing support and repairs). The connector meets the VME size restrictions. Please contact Kontron for a detailed information on this connector.

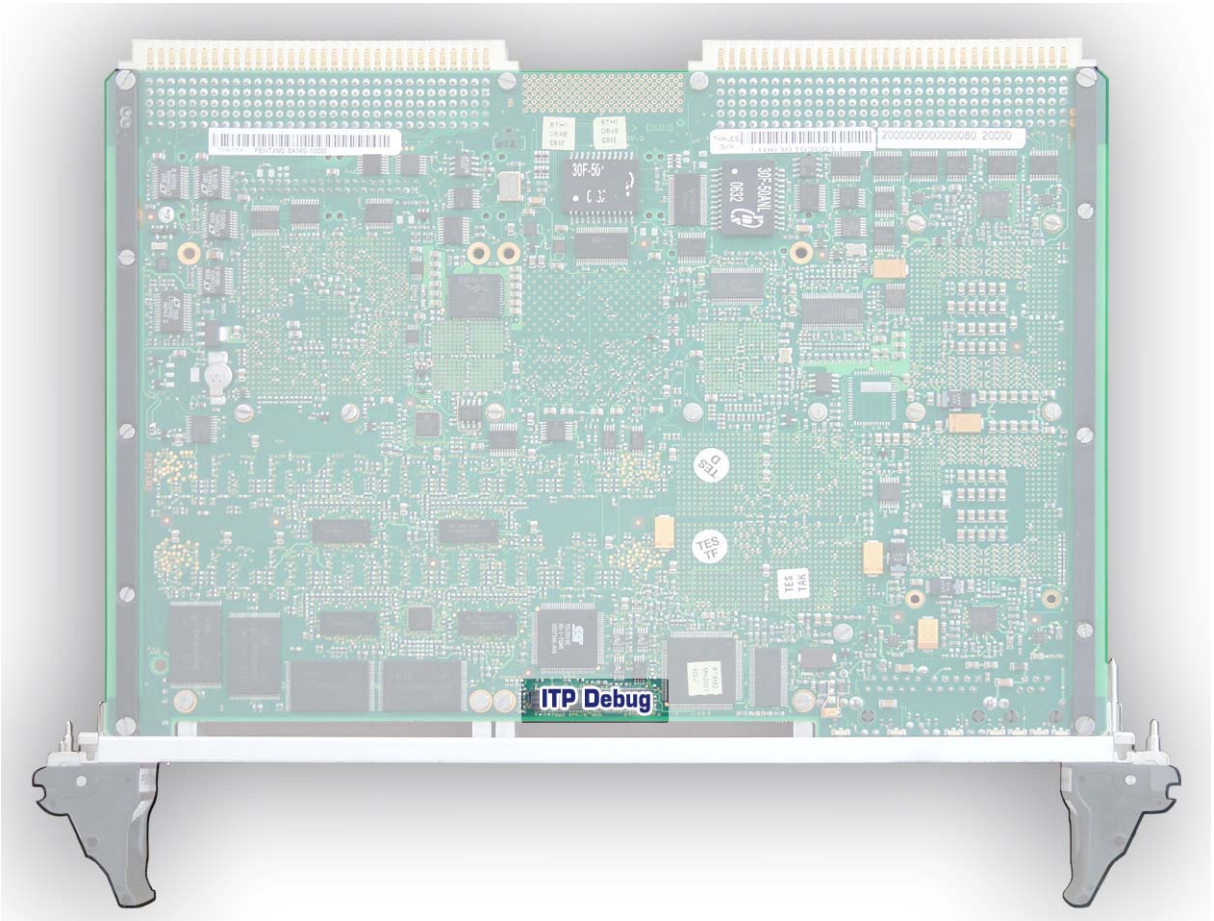


Figure 31: ITP Debug Connector Location

6.2 Front Panel Connectors

Figure 32 shows the PMC openings, connectors, LED's, and switches. The following subsections provide descriptions of the front panel connectors:

- COM1, refer to section 6.2.1 "COM1"
- ETHERNET 0 and 1, refer to section 6.2.2 "ETHERNET 0 and 1"
- USB3, refer to section 6.2.3 "USB3"

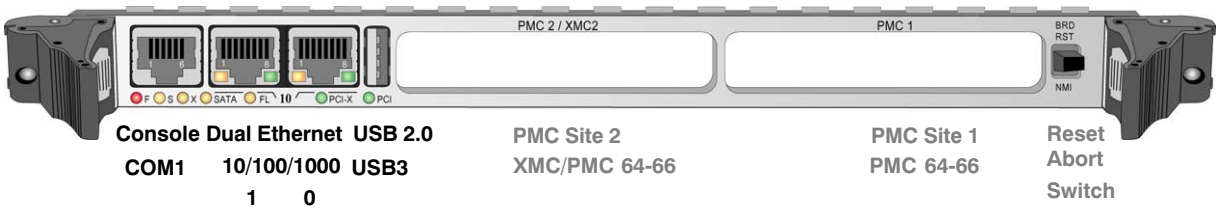


Figure 32: PENTXM2 or PENTXM4 Front Panel

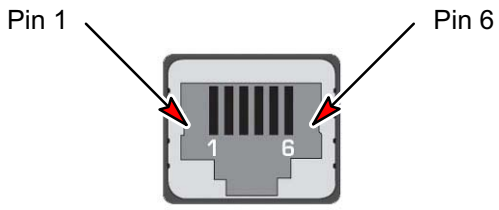
6.2.1 COM1 Serial Port

This modular connector provides the COM1 serial port. It supports RXD, TXD, signal ground, and chassis ground.

In EIA-232 mode, it also supports RTS and CTS. The front panel COM1 port may be multi dropped in EIA-485 mode.

Pin Assignment

Pin	Signal
1	RTS/TXDb
2	Shell
3	TXD/TXDa
4	RXD/RXDa
5	GND
6	CTS/RXDb



Signal Description

Mnemonic	Description
CTS/RXDb+	EIA-232 Clear-To-Send / EIA-485 Receive Data (pair b)
RTS/TXDb+	EIA-232 Ready-To-Send / EIA-485 Transmit Data (pair b)
RXD/RXDa-	EIA-232Receive Data / EIA-485 Receive Data (pair a)
TXD/TXDa-	EIA-232 Transmit Data / EIA-485 Transmit Data (pair a)
GND	Ground
Shell	Chassis Ground

Cable Designation

Serial cable is:

- RJ-14 (6 pin, 4 conductor) for a simple EIA-232 without handshake support.
- Use a RJ-12 (6 pin, 6 conductor) for EIA-232 with handshaking or EIA-485.
  A RJ-12 to DB9/DB25 male or DB9/DB25 female adapter is available from multiple sources, such as *Triangle Cable*, http://www.trianglecables.com/db9m-rj12.html

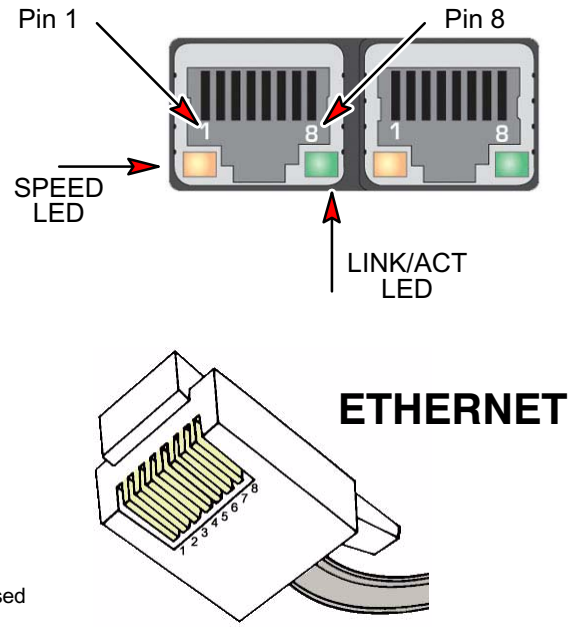
6.2.2 ETHERNET 0 and 1

A dual RJ-45 connector with integrated LED's provides the 10/100/1000 Mbps connectivity and status LED's. Both RJ-45 Ethernet ports have identical pinouts, so only one pinout is shown.

Pin Assignment

Pin	Signal
1	BI_DA+
2	BI_DA-
3	BI_DB+
4	BI_DC+ (*)
5	BI_DC- (*)
6	BI_DB-
7	BI_DD+ (*)
8	BI_DD-(*)
Shell	Chassis Ground

(*) : In 10BASE-T or 100BASE-T these signals are not used



Signal Description

Mnemonic	Description
BI_DA+/-	In 1000BASE-T: First pair of Transmit/Receive data In 10BASE-T/100BASE-T: Pair of Transmit data
BI_DB+/-	In 1000BASE-T: Second pair of Transmit/Receive data In 10BASE-T/100BASE-T: Pair of Receive data
BI_DC+/-	In 1000BASE-T: Third pair of Transmit/Receive data In 10BASE-T/100BASE-T: Unused.
BI_DD+/-	In 1000BASE-T: Fourth pair of Transmit/Receive data In 10BASE-T/100BASE-T: Unused.

Cable Designation

CABRJ45FTP5MM5M: Ethernet Cable.

Ethernet Speed LED's, Yellow

These LEDs indicate the operating speed of the Ethernet interfaces, as follows:

- Off = 10 Mbps
- Steady On = 100 Mbps
- Flashing = 1000 Mbps

Ethernet Link/Activity LED's, Green

These LEDs illuminate when connection has been made on the Ethernet interfaces. They will flash to indicate link activity. During periods of high Ethernet activity the LED's may switch off for several seconds.

6.2.3 USB3

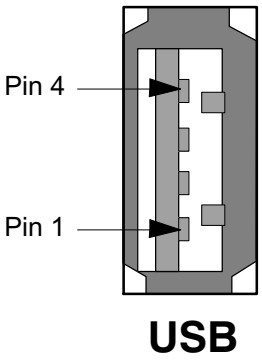
The USB connector uses switched power.

Connector Pin Assignment

The USB-type socket connector that has the following pin assignment:

Pin	Mnemonic
1	+5V Protected
2	DATA1-
3	DATA1+
4	GND
CASE	M GND

Table 22: USB Connector Pin Assignment



Signal Description

Mnemonic	Signal Description
DATA1+/-	Differential data pair of USB line 1.
+5V Protected	+5V Protected Power, up to 720 mA continuous, short circuit current limited (1.2 A) with thermal shutdown, and automatic restart when short is removed.
GND	Logical Ground.
M GND	Case Ground. Chassis Ground.

Table 23: USB Connector Signal Description

Chapter 7 - PMC Sites

The PENTXM2 or PENTXM4 provides two PMC sites:

- The PCI 64 PMC site 1, 64-bit wide, operates at 66 MHz (refer to Table 24 for more information about the PCI 64 PMC Site 1 configuration).
- The PCI 64 XMC/PMC site 2, 64-bit wide, operates at 66 MHz (refer to Table 25 for more information about the PCI 64 XMC/PMC Site 2 configuration).

Kontron products include standard PMCs such as Ethernet PMC (CPMC-ETH-xx), SCSI PMC (CPCI-SI2S). Refer to the Release Notes associated with your operating system for more information about the supported PMCs.

For EMC protection reasons, when not used, the PMC slots are fitted with a blanking plate.

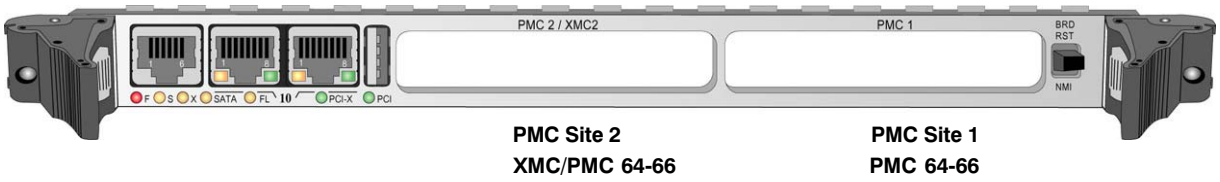


Figure 33: PENTXM2 or PENTXM4 PMC Site Location

The BIOS may use the CPLD BCSR's fo force protocol and clock speed restrictions for both PMC sites by forcing PCIX_CAP to ground or to ground through 10K ohms. It can also ground PCIX_M66EN. Both PMC sites utilize the same PCI/PCI-X segment so the settings affect both PMC sites. The new settings becomes effective with the next board reset.

The default power up settings for these bits reside in the CPLD's internal Flash EPROM. The BIOS provides the means to reprogram these bits.

7.1 PMC Installation

Refer to the section 3.6 “Installing or Removing a PMC Module" page 27.

7.2 PCI 64 PMC Site 1

Electrostatic Discharge (ESD) can damage components. To avoid ESD damage, the board should be kept in its protective antistatic packaging until it is ready to be installed. During installation make sure to wear an antistatic wrist strap to discharge static electricity.

The following table sums up all information concerning the PCI 64 PMC Site 1. It gives information needed for software and hardware configuration.

FUNCTION	VALUE	MEANING
PMC Connectors	J11	Connects the signals for the 64-bit PCI bus.
	J12	Connects the signals for the 64-bit PCI bus.
	J13	Connects the signals for the 64-bit PCI bus.
	J14	Connects the User Defines I/O signals.
V(I/O) Voltage Level	+3.3V	The signaling voltage of the 64-bit PCI bus is +3.3V. It is not +5V tolerant. The user must check that its PMC type is compatible with this signaling voltage (refer to section 7.4 page 73).
PCI Bus Mode	64 Bits	The 64-bit PCI bus is in 64-bit mode.
PCI Bus Rate	66 MHz	The 64-bit PCI bus can run at 66 MHz (refer to the Hardware Release Notes for possible restrictions).
PCI Interrupts	INTA INTB INTC INTD	Connected to the 6300ESB Interrupt Controller.
Bus Number	6	64-bit PCI bus corresponds to PCI bus number 0.
Device Number	4	PMC Site 1 is device number 1 on the 64-bit PCI bus.
REQ/GNT IDSEL	0 AD[20]	for single function PMC's
Alternate REQ/GNT Alternate IDSEL	2 AD[24]	for dual function PMC's

Table 24: PCI 64 PMC Site 1 Information

7.3 PCI 64 XMC/PMC Site 2

Electrostatic Discharge (ESD) can damage components. To avoid ESD damage, the board should be kept in its protective antistatic packaging until it is ready to be installed. During installation make sure to wear an antistatic wrist strap to discharge static electricity.

PMC Site 2 can alternately be used as an XMC site with a x8 PCI-Express link to the E7520 MCH. An XMC card installed in this location uses its P5 (J25 on the PENTXM2 or PENTXM4) for the Express Link. The installed XMC should provide either front panel I/O or utilize a P4 (J24 on the PENTXM2 or PENTXM4) for I/O.

The following table sums up all information concerning the PCI 64 XMC/PMC Site 2. It gives information needed for software and hardware configuration.

FUNCTION	VALUE	MEANING
PMC Connectors	J21	Connects the signals for the 64-bit PCI bus.
	J22	Connects the signals for the 64-bit PCI bus.
	J23	Connects the signals for the 64-bit PCI bus.
	J24	Connects the User Defines I/O signals.
XMC Connectors	J25	Connects the signals for the switched communications.
V(I/O) Voltage Level	+3.3V	The signaling voltage of the 64-bit PCI bus is +3.3V. It is not +5V tolerant. The user must check that its PMC type is compatible with this signaling voltage (refer to section 7.4 page 73).
PCI Bus Mode	64 Bits	The 64-bit PCI bus is in 64-bit mode.
PCI Bus Rate	66 MHz	The 64-bit PCI bus can run at 66 MHz (refer to the Hardware Release Notes for possible restrictions).
PCI Interrupts	INTA INTB INTC INTD	Connected to the 6300ESB Interrupt Controller.
Bus Number	6	64-bit PCI bus corresponds to PCI bus number 0.
Device Number	5	XMC/PMC Site 2 is device number 1 on the 64-bit PCI bus.
REQ/GNT IDSEL	1 AD[21]	for single function PMC's
Alternate REQ/GNT Alternate IDSEL	3 AD[25]	for dual function PMC's

Table 25: PCI 64 XMC/PMC Site 2 Information

7.4 Signaling Voltage Keying Pin

The 64-bit PCI bus of the PENTXM2 or PENTXM4 and the PMC plugged on the 64-bit PCI slot have to operate on the same signaling level.

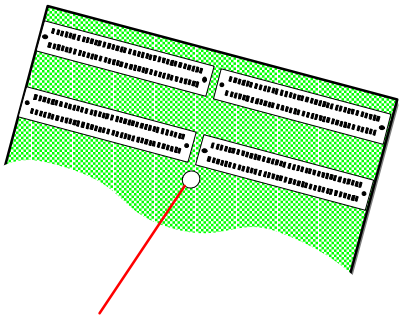
The PENTXM2 or PENTXM4 sets the signaling level for the 64-bit PCI bus to +3.3V (i.e. V(I/O)=+3.3V). The V(I/O) pins of the PCI 64 PMC are connected to +3.3V. **No PMC voltage selection key is provided on the board.**

The distinction between PMC types is the signaling level they use, not the power rails they connect to, nor the component technology they contain.

On the PENTXM2 or PENTXM4 PCI 64 PMC slot, only two PMC types must be intalled:

> +3.3V PMC:

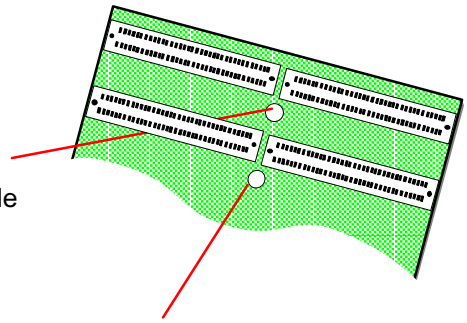
It is designed to work only in a +3.3V signaling level and will only have a keying hole.



+3.3V Key hole

> Universal PMC:

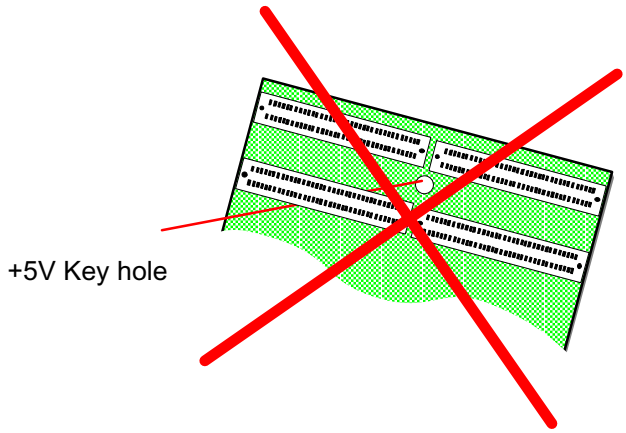
It supports both voltages (+5V and +3.3V). This PMC is capable of detecting the signaling level in use and adapting itself to that environment. It has two keying holes (+5V and +3.3.V) and can, therefore, be plugged into either signaling level.



+5V Key hole

+3.3V Key hole

As no PMC voltage selection key is provided on the board, make sure not to insert a +5V PMC on the board. Failture to observe this restriction may result in damage to the PMC or the PENTXM2 or PENTXM4



Chapter 8 - System Installation

This chapter describes the installation of the PENTXM2 or PENTXM4 board in a system.

> **WARNING**
>
> Only use the PENTXM2 or PENTXM4 in backplanes that supply power on both P1 and P2 connectors. Failure to observe this warning may result in damage to the board.

> **WARNING**
>
> Ensure that your PENTXM2 or PENTXM4 is correctly inserted into the backplane connectors.

> **WARNING**
>
> Only use the PENTXM2 or PENTXM4 into VME64x backplanes (5-row connectors) supplying 3.3V power.

8.1 System Backplane Configuration

Before plugging the PENTXM2 or PENTXM4 into a rack, you should first check the rack's backplane configuration links.

Most of the VME64 backplanes, now, have an automatic daisy chain configuration for the Interrupt Acknowledge (IACK) daisy chain and the four Bus Grant (BGx) daisy chains. If your backplane does not provide the automatic daisy chain feature, you could have to configure links on the backplane to ensure proper operations.

8.2 System Backplane Compliance

The backplane of the rack where a PENTXM2 or PENTXM4 board is inserted, must conform to the VME64X standard: **ANSI/VITA 1.1-1997**. More precisely, the P0 connectors of the backplane must conform to the level 1 of the **IEC 16076-4-101** standard (length of the pins of the [a-e] rows = 8.2 mm).

8.3 Chassis Ground

To ensure optimum operation of the PENTXM2 or PENTXM4 with regard to EMC when using I/O connections from the front panel connectors, there should always be a connection from the front panel to the chassis ground of the system.

8.4 5V Power Recommendations

The PENTXM2 or PENTXM4 draws internal +5V power from P1 and P2 connectors.

The +5V voltage rise time must be monotonic and should not last for more than 25 ms.

Power consumption and heat dissipations of each PMC (+5V and +3.3V) should not exceed 7.5W on both sides (6W on side 1), as described in the IEEE P1386 standard.

8.5 3.3 V Power Recommendations

The PENTXM2 or PENTXM4 draws internal and V(I/O) PMC +3.3V power from the P1 connector.

The +3.3V voltage rise time must be monotonic and should not last for more than 25 ms.

Power consumption and heat dissipation of each PMC (+5V and +3.3V) should not exceed 7.5W on both sides (6W on side1), as described in the IEEE P1386 standard.

8.6 V(I/O) Power Recommendations

The 64-bit PCI bus uses +3.3V for signaling bus level (to the V(I/O) pins of the PCI 64 PMC connectors. This bus is not +5V tolerant.

V(I/O) voltage is delivered by the PENTXM2 or PENTXM4.

V(I/O) current consumption must not exceed 300 mA per PMC.

8.7 System Configuration Suggestions

Check the P2 connections of the slot before powering up.

Use the PENTXM2 or PENTXM4 in a rack on its own at first, and only plug it in with other cards later (if other cards are to be used). This enables you to try basic operation before tackling any system configuration issues.

To interact with the PENTXM2 or PENTXM4's debugging monitor, you need to attach a terminal to the PENTXM2 or PENTXM4. By default, this terminal will use the serial port 0 signals either on the SERIAL front panel connector or P2 (Don't do both!).

The serial interfaces are configured as DTE (9.6 Kbaud, 8 bits/character, 1 stop bit, parity disabled). However, cables optionally supplied by Kontron permit direct connection to a terminal without use of a null-modem cable (for more information about the PENTXM2 or PENTXM4 connections, refer to the “Connection Guide").

Chapter 9 - Operating Instructions

This chapter details:

- the power-up procedure,
- the RESET switch and LEDs available on the front panel,
- the memory maps,
- power and thermal management of the central processor,
- the power sequencer and reset generator of the cPLD
- the interrupts management,
- the timers, counters, RTC and GPIO's management.

9.1 Power-up

1. Verify all necessary hardware configuration has been done: refer to Chapter 5 “Hardware Configuration",
2. Check that the connections have been made correctly: refer to Chapter 6 “Connectors" or to the “Connection Guide",
3. Verify the PMCs have been correctly plugged into the PENTXM2 or PENTXM4: refer to Chapter 3 “Preparing Before Using" section 3.6 “Installing or Removing a PMC Module" or to the “Connection Guide",
4. Verify the onboard mass storage has been correctly plugged into the PENTXM2 or PENTXM4: refer to Chapter 3 “Preparing Before Using" section 3.5 “Installing the Onboard Mass Storage" or to the “Connection Guide",
5. Verify the backplane configuration is complete and the PENTXM2 or PENTXM4 firmly secured in the rack; take care of the system configuration suggestions: refer to Chapter 8 “System Installation",
6. Power-up the system.

9.2 Abort/Reset Switch and LEDs of the Front Panel

Figure 32 shows the PMC openings, connectors, LED's, and switches. The following subsections provide descriptions of the front panel:

- Abort/Reset Switch, refer to section 9.2.1
- Ethernet LEDs, refer to section 9.2.2
- Other LEDs, refer to section 9.2.3

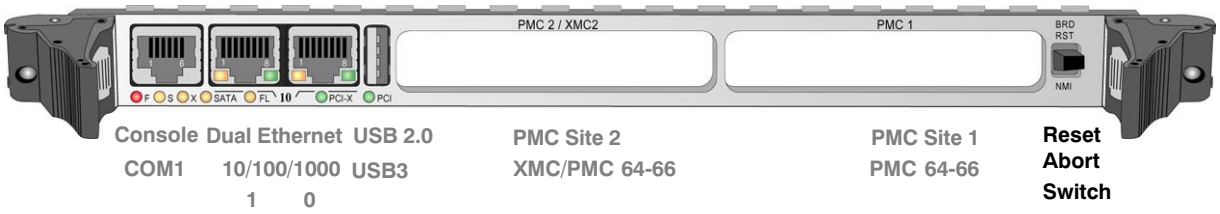


Figure 34: PENTXM2 or PENTXM4 Front Panel

9.2.1 Abort/Reset Switch

A front panel momentary action switch can be used to generate

- Board Reset (resets this board only)
- Local Non-Maskable Interrupt (NMI)
- System Reset (asserts VMEbus `SYSRESET*` resets all boards connected to the VMEbus including this board)

Using the front panel orientation shown in Figure 34:

- pressing the switch up ↑ generates a board reset,
- pressing the switch down ↓ generates a non-maskable interrupt,
- moving the switch up ↑ and then down ↓ within a half second (or down then up) will generate a VMEbus System Reset.

9.2.2 Ethernet LEDs

The connector LED's operate even if the Ethernet connection is performed via the P0 connector.

» Ethernet Speed LED's, Yellow

These LEDs indicate the operating speed of the Ethernet interfaces, as follows:

- Off = 10 Mbps
- Steady On = 100 Mbps
- Flashing = 1000 Mbps

» Ethernet Link/Activity LED's, Green

These LEDs illuminate when connection has been made on the Ethernet interfaces. They will flash to indicate link activity. During periods of high Ethernet activity the LED's may switch off for several seconds.

9.2.3 Other LEDs

Seven bi-color LEDs are situated above the Ethernet connectors, on the left side of the front panel:

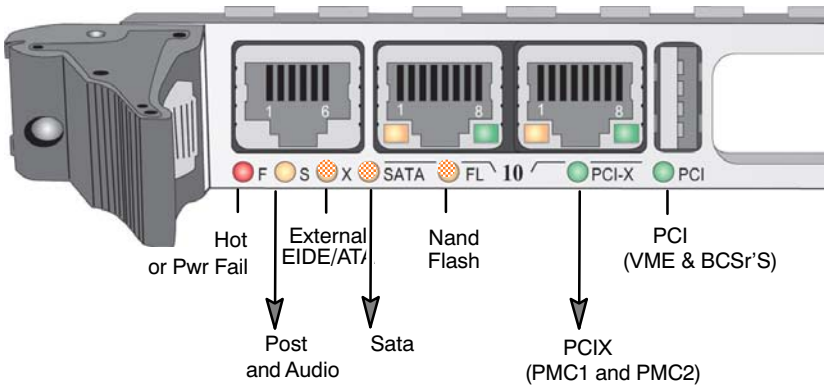


Figure 35: PENTXM2 or PENTXM4 LEDs Locations

9.2.3.1 Processor Hot / Power Fail LED (Red)

This LED will flicker at a 2 to 4 Hz rate when the processor shuts down due to an over temperature condition. A failure of either CPU's core power supply or VCCP is indicated by a steady-state-on.

9.2.3.2 POST and AUDIO LED (Yellow)

This LED should be used by test software to indicate that a power on self test has failed.

Software turns on this LED by sending a logic 1 to the 6300ESB speaker.

Creative software may also modulate this LED whenever the speaker output would normally be activated for certain functions, such as sound alerts from the operating system.

9.2.3.3 Disk Activity LED: External EIDE/ATA (Orange)

The External EIDE/ATA LED illuminates in response to activity by a device connected to the P6 connector at PMC Site 1 (primary EIDE/ATA).

9.2.3.4 Disk Activity LED: SATA (Orange)

The board provides one LED for the SATA interface. This LED illuminates whenever either of the two SATA ports is active.

9.2.3.5 Disk Activity LED: NAND Flash (Orange)

The NAND Flash LED illuminates whenever the NAND Flash is active (secondary EIDE/ATA).

9.2.3.6 Run LED: PCI-X (Green)

The board provides a run LED for the PCI-X bus.

The LED's illuminate whenever its IRDY# signal is asserted.

PMC activity is indicated by the PCIX LED.

The LED brightness provides a relative measure of activity on the PCI represented by that LED: a bright LED indicates a high level of activity and a dark LED indicates no activity.

IRDY# is a short duration signal and infrequent short bursts of activity could go unnoticed. To guard against this, each time one of these LED's illuminates it remains on for at least 8 ms.

9.2.3.7 Run LED: PCI (Green)

The board provides a run LED for the PCI bus.

The LED's illuminate whenever its IRDY# signal is asserted.

VMEbus data transfers to or from this board are indicated by the PCI LED. BCSR activity also illuminates the PCI LED.

The LED brightness provides a relative measure of activity on the PCI represented by that LED: a bright LED indicates a high level of activity and a dark LED indicates no activity.

IRDY# is a short duration signal and infrequent short bursts of activity could go unnoticed. To guard against this, each time one of these LED's illuminates it remains on for at least 8 ms.

9.3 Memory Maps

9.3.1 I/O Mapping

The PENTXM2 or PENTXM4 supports a variety of I/O functions whose addresses are summarized in Table 26.

I/O Address Range	Description
0000-001Fh	DMA Controller (6300ESB)
0020-002Dh	Interrupt Controller (6300ESB)
002E-002Fh	Legacy Super I/O Configuration Index and Data (Not Used)
0030-003Dh	Interrupt Controller (6300ESB)
0040-0043h	PIT Timers (6300ESB)
0050-0053h	PIT Timers (6300ESB)
0060h	Legacy Keyboard Controller (Not Used)
0061h	NMI Status (6300ESB)
0064h	Legacy Keyboard Controller (Not Used)
0070h	NMI Enable/RTC Address (6300ESB)
0071h	RTC Data (6300ESB)
0080h	Port 80 Debug Port (via Test Adapter Board)
0092h	Port 92 Reset Generator (6300ESB)
00A0-00A1h	Slave Interrupt Controller (6300ESB)
00C0-00DFh	Slave DMA Controller (6300ESB)
00F0h	Math Coprocessor Error
0210-021Dh	unassigned (Not Used)
02F8-02FFh	COM2 Serial (6300ESB)
031C-031Fh	unassigned (Not Used)
03BC-03BFh	Legacy Parallel Port LPT1 (Not Used)
03F0-03F7h	Legacy Floppy Controller (Not Used)
03F8-03FFh	COM1 Serial (6300ESB)
04D0-04D1h	Interrupt Control (6300ESB)
0CF8-0CFFh	PCI Configuration Registers (7520MCH)
0D00-FFFFh	PCI Free I/O Space

Table 26: I/O Address Map

9.4 Central Processor Power and Thermal Management

9.4.1 Power Management

The processor supports a number of discrete operating frequencies from about half clock speed to full clock speed.

The BIOS provides a Setup menu that allows the operating frequency of the CPU's to be set prior to booting an operating system. By default the CPU's operates at full clock speed.

This mechanism for power reduction allows the board to operate in environments where power capacity is limited (e.g. under battery power), or in systems where cooling airflow is less than adequate. In this latter case it may be wise to also consider some of the Thermal Management options available on this board.

9.4.2 Thermal Management

The maximum power dissipation of the processor may be higher than that of previous processors.

Under typical load conditions, the heatsink (and cooling airflow) will keep the processor die temperature within specification. However, if the board is running CPU-intensive or stress software, or if the airflow is inadequate, the heatsink alone may not be able to prevent the processor overheating.

To ensure that the processor always operates within its thermal specifications, it includes several thermal management and protection functions. Each of these is described in the following subsections:

- Thermal Monitor 1 (TM1), described in section 9.4.2.1,
- Thermal Monitor 2 (TM2), described in section 9.4.2.2,
- CPU Thermal Trip, described in section 9.4.2.3.

The BIOS provides a setup option to select which functions are to be enabled.

9.4.2.1 Thermal Monitor 1 (TM1)

TM1 uses a temperature sensor located near to the hottest part of the processor die. If it detects a temperature higher than 100°C, a thermal control circuit (TCC) will modulate (i.e. alternately stop and start) the processor core clocks. This causes the processor to halt for short periods and decreases its power consumption, which in turn lowers the die temperature.

The severity of the modulation will increase as the die temperature rises, up to a maximum of about 50%. The TCC will cease modulation when the die temperature has fallen to the threshold temperature value. This threshold temperature value is set to 100°C and it can not be modified.

The temperature sensor is individually calibrated by Intel. The TM1 characteristics are also fixed by Intel and cannot be modified.

TM1 is disabled after Reset and has to be enabled by the BIOS or application software.

9.4.2.2 Thermal Monitor 2 (TM2)

TM2 uses the same temperature sensor as TM1.

When the TM2 thermal control circuit is triggered, the CPU operating frequency and core voltage will be reduced, causing the power consumption to fall, which in turn lowers the die temperature.

Because a CPU under TM2 control operates continuously, the overall system performance for a given reduction in power consumption is higher than TM1.

System latency is also lower when using TM2.

The drawback of TM2 is that changes to the operating frequency will also affect the Time Stamp Counter (TSC) rate and any timing or calculations that use it.

If TM2 is used it will probably be better to use the Software Synchronization Timer SST or the Programmable Timer Module PTM (see BCSR's) for time stamping than the TSC.

TM2 is disabled after Reset and has to be enabled by the BIOS or application software.

9.4.2.3 CPU Thermal Trip

The processor chip also contains a thermal trip circuit.

This is intended to protect the processor in the event of a catastrophic cooling failure. If the die temperature reaches approximately 135ºC, it shuts down the processor core and asserts the THERMTRIP# signal. Logic on the board responds to this assertion by removing the processor core voltage within a few milliseconds. A power cycle (i.e. OFF then ON) is required to restore normal operation.

The thermal trip circuit is always operational and cannot be disabled.

9.4.2.4 Factory Settings

To cover typical use by embedded applications customers, the PENTXM2 or PENTXM4 factory settings are as such:

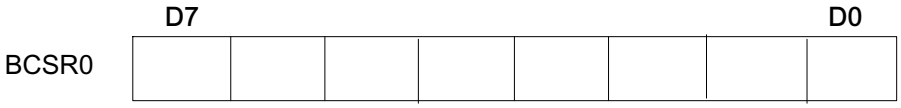
- Maximal frequency boundary for the processor(s) is set to 1.66 GHz
- TM1 management is set by default
- TM2 management is set by default
- The first throttle point is set to 100ºC (ie. processor will throttle when the core temperature goes above 100ºC)
- Thermal Trip is always set (which means the processor will shut itself if the core temperature goes beyond 135ºC)

9.5 cPLD: Description of Specific BCSRs

9.5.1 Interrupt Status (BCSR0)

Software uses BCSR0 to determine the cause of the interrupt, and provides the means for clearing some of the interrupts. A board reset clears all BCSR0 bits.

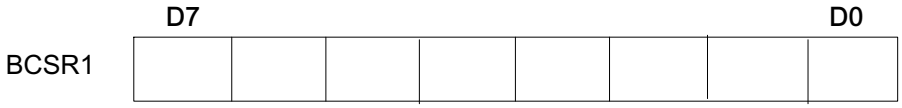
The register is 8-bits wide. D[7:5] are non-maskable (NMI) interrupts. The remaining two interrupts, D[1:0] are maskable.



D[31:8]	Not used. Write data is ignored and read returns all 0's.
D7	ABORT - sets and generates a NMI to the CPUs when the front panel switch is pressed down. Write a 1 to D7 to clear the interrupt. Writing a 0 is ignored. This bit is an edge sensitive signal in that holding the switch down will not generate continual interrupts.
D6	NMI_6300 - read only, bit follows the state of the NMI pin of the 6300ESB. The NMI from the 6300ESB must be cleared via the 6300ESB. A 1 indicates the 6300ESB is asserting NMI, which is propagated via the NMI (out) to the CPUs.
D5	LINT1 - read only. A 1 indicates the NMI is the result of the Universe II asserting LINT1#. The cause of the interrupt must be cleared via the Universe II. The LINT (in) is propagated via the NMI (out) to the CPUs.
D[4:2]	not used - always read as 0's, writes ignored.
D1	PTM - 1 indicates the PTM (Programmable Timer Module) generated INTA#. Write a 1 to this bit to clear it (removes the PTM interrupt). Writing a 0 is ignored.
D0	SST - 1 indicates the SST (Software Synchronization Timer) has generated INTA#. Write a 1 to this bit to clear it (removes the SST interrupt). Writing a 0 is ignored.

9.5.2 SST - Software Synchronization Timer (BCSR1..BCSR2)

The SST (Software Synchronization Timer) is a 32-bit timer that is intended to be used for high accuracy software synchronization for multiprocessor-based systems. BCSR1 is the 8-bit control register. BCSR2 is the 32-bit timer read register. The clock source for the timer register is the 16 MHz VMEbus SYSCLK. If the VMEbus is depopulated the clock source is the 14.31818 MHz oscillator that is used as the base frequency for the main clock generator for the board.



D[31:8] Not used. Write data is ignored and read returns all 0's.

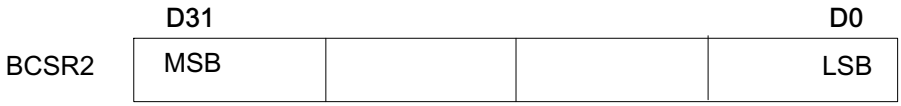
D7 IRQ MASK - 1/0 = enable/inhibit interrupt generation with return to 0.
Bit is cleared by Board Reset

D[6:3] not used - always read as 0's, writes ignored.

D2 Prescale - this bit selects the clock that is used by the SST. This bit is loaded from the cPLD internal Flash at Power Reset.
1 = Clock/16 (1 uS period in VMEbus systems)
0 = Clock/2 (125 nS period in VMEbus systems)

D1 Reset Control - this bit is used to determine how SYSRESET from the VMEbus affects the Run/Halt bit, D0. This bit is loaded from the cPLD internal Flash at Power Reset.
1 = Run/Halt is not affected by SYSRESET
0 = Run/Halt goes to 0 by SYSRESET assertion

D0 Run/Halt - controls the timer. This bit is loaded from the cPLD internal Flash at Power Reset. After that, if D1 = 0, the timer will stop running when SYSRESET is asserted (D0 goes to 0) and wait to be restarted by software writing a 1 to D0. If D1 = 1, D0 is not affected by SYSRESET. In this case, if the timer was running (D0 = 1) when a SYSRESET assertion occured it will continue to run. Note that an asserted SYSRESET always clears the timer, so as soon as SYSRESET deasserts the timer begins counting from 0. If the timer was halted (D0 = 0) it will remain halted after a SYSRESET but the counter is cleared to 0.



BCSR2 is always cleared by a VMEbus SYSRESET assertion and counts up whenever BCSR1[0] = 1. If the counter is stopped and restarted the count continues from the stop point. BCSR2 is read only and must be read as a 32-bit value or incorrect results will be obtained.

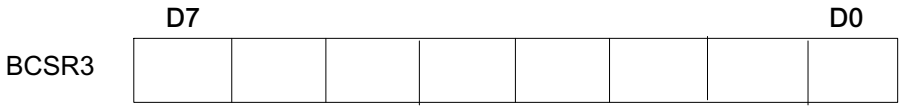
At Power Reset, the default value loaded from the cPLD internal Flash for BCSR1[0:2] = 111b; so without any particular BCSR1 re-programming, BCSR2 register contains the number of uS elapsed since the last power-on or the last SYSRESET.

9.5.3 PTM - Programmable Timer Moduler (BCSR3..BCSR4)

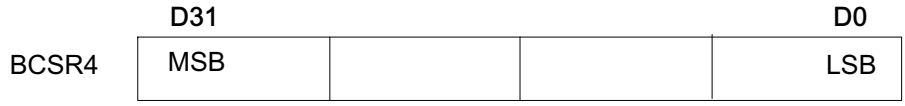
The PTM is a 32-bit preloadable down-counter that uses a 1uS clock source. Software controls the PTM using BCSR3. BCSR4 is the 32-bit preload and counter register. Writing to BCSR4 writes to the preload register. Reading from BCSR reads the current counter value. When the counter is stopped it immediately takes on the value of the preload register.

When software starts the counter it begins decrementing from the preload value. After the count decrements to 1 it synchronously preloads to the preload value with the occurrence of the next input clock period. This results in a time delay identical to that of the preload (0X100 = 256 clock periods). The longest delay possible (232) occurs with a preload value of 0x0000_0000. If the interrupt has been enabled, returning to the preload value causes an interrupt.

The counter, BCSR4, may be read at any time, but only 32-bit reads will return accurate data. BCSR4 may be written at any time (writes to the preload register) and should always be written to as a 32-bit value when the timer is running. After the timer completes decrementing from its previous preload value it will preload to the newly written preload value. If it is desired to apply the new preload immediately, stop the timer and write a new preload value to BCS4. BCSR3 and BCSR4 are cleared by a Board Reset.



D7	IRQ MASK - 1/0 = enable/inhibit interrupt generation with returns to the preload value.
D[6:2]	not used - always read as 0's, writes ignored.
D1	Pause - 1 pauses the timer. 0 allows the timer to continue decrementing without reloading
the	preload value.
D0	Run/Stop. The counter always initializes itself to the preload value while it is stopped.

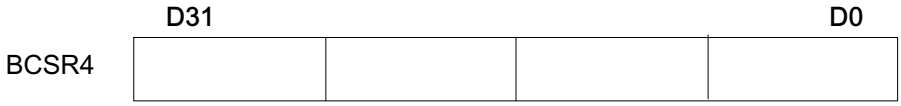


D[31:0]	Preload/Counter Register: Write: moves D[31:0] to the preload register. Read: counter register. Note that a stopped counter always assumes the value of the preload register.

9.5.4 COM2/1 Configuration (BCSR5)

- Each serial port may be configured by the BCSR5 as EIA-232 or EIA-485.
- The BCSR's can also independently configure each port to operate in full or half duplex mode.
- Slow slew rate is also BCSR-programmable when in EIA-485 mode.
- In EIA-485 half-duplex mode the port's DTR signal controls the data direction.
- The signaling level of EIA-485 is compatible with EIA-422 so full duplex EIA-485 may also be used for point-to-point communications with an EIA-422 serial port.
- When a port is operating in EIA-485 mode software may configure the terminators for V.35, V.11, or unterminated using the BCSR's.
- In EIA-232 mode the port is always unterminated.

This register controls the configuration of the COM2 and COM1 serial ports and the port terminators. COM2 configurations are cleared by a board reset which turns the port interface off. The COM1 interface remains active when main power is turned off as long as VME +5VSTDBY is applied. This is required in order for the BMC to communicate via COM1 as shown in Figure 27 on page 33. Therefore, the COM1 configurations are not affected by a board reset but are loaded from the internal Flash during Power Reset, or reloaded from Flash when +5V or +3.3V on the VMEbus is lost. The data loaded to D[5:1] is the compliment of the Flash data and D0 is loaded from the Flash without complimenting.



D[31:14] not used - always read as 0's, writes ignored.

D[13:12] COM2 Terminations - these bits determine what type of terminators are used when the port is operating in 485 mode. The terminators are hi Z when operating in 232 mode or when the port is off. The following assumes the port function is 485 mode:
00 = V.35 (driver and receiver terminated)
01 = V.11 (receiver terminated)
10 = hi Z (neither driver nor receiver is terminated, may be used for non-end point devices of a multi-drop bus)
11 = V.11 (driver and receiver terminated, assumes a communications cable is not attached)

D[11:8] COM2 Port Function
0000 = interface is off
0001-0011 = 232, full duplex
010x = 232, half duplex, RTS# controlled: 1/0 = send/receive
011x = 232, half duplex, DTR# controlled: 1/0 = send/receive
In the following, s = slew rate: 1/0 = slow/fast. Also, if the port is configured for full duplex mode the receiver is always on. If the transmit and receive wire pair are the same (ie; connected to the same wire pair) then the receiver is capable of monitoring all traffic on the pair.

100s = 485, full duplex, RTS# controlled: 1/0 = transmitter off/on
101s = 485, full duplex, DTR# controlled: 1/0 = transmitter off/on
110s = 485, half duplex, RTS# controlled: 1/0 = send/receive
111s = 485, half duplex, DTR# controlled: 1/0 = send/receive

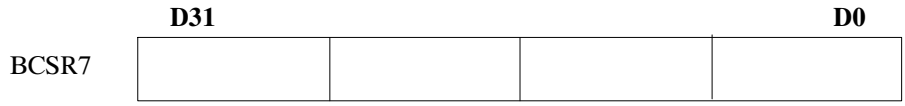
D[7:6] not used - always read as 0's, writes ignored.

D[5:4] COM1 Terminations (same as D[13:12])

D[3:0] COM1 Port Function (same as D[11:8]). An unprogrammed cPLD Flash EPROM initializes
D[5:0] to 0b00_0001.

9.5.5 PMC, XMC Status/Control (BCSR7)

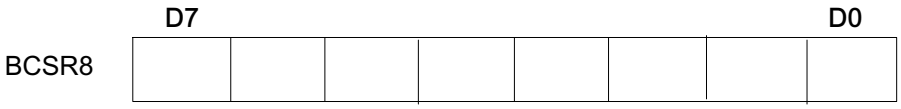
This register returns the value of the PMC and XMC status bits and allows the BIOS software to control the value of PCIX_CAP and M66EN. The control bits, D[10:8] are loaded from the internal Flash at Power Reset. D[10:8] drive open-drain outputs to their corresponding PMC/PCI-X signals. A 0 drives the corresponding signal low, a 1 results in control of the signal via the installed PMC's. D[4:0] are read only, and writes are ignored.



D[31:11]	Not used. Writes ignored, read as all 0's.
D10	PCIX_66MHz - A 0 forces PCIX_CAP low via a 10K resistor (66 MHz).
D9	PCIX_CAP - A 0 forces PMC's to PCI only (not PCIX capable)
D8	M66EN - A 0 forces PMC's to 33 MHz.
D[7:5]	not used - always read as 0's, writes ignored.
D4	XMC Site 2 presence detect. 1/0 = not present/present.
D3	XMC Site 1 presence detect. 1/0 = not present/present. Note that this board does not provide XMC Site 1 so this bit is always read as a 1.
D2	PPMC EREADY,: 1/0 = Proc PMC ready/not ready for enumeration.
D1	BMODE1#, PMC Site 2.
D0	BMODE1#, PMC Site 1.

9.5.6 VME Slot ID (BCSR8)

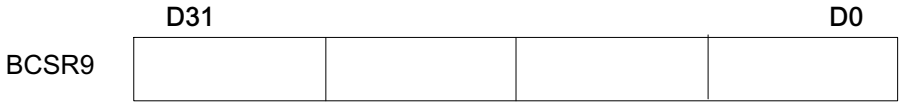
This register is read only (write data is ignored) and returns the value of the ACSEL bits of BCSR10 and the VME geographic address lines.



D[7:6]	ACSEL - Auto Configuration Select (set by BCSR10 D[7:6]) 00 = Auto-slot ID 01 = CSR's in A16 space 10 = CSR's in A32 space 11 = CSR's in A24 space If the cPLD detects a geographical address parity error, slot configuration reverts to Auto-slot ID.
D5	GAP# from VMEbus
D[4:0]	GA4#..GA0# from VMEbus

9.5.7 Test Mode, SYSRESET, and WDT Control (BSCR9)

This read/write register allows the software to control the board behaviour with respect to a VMEbus SYSRESET#, and a WDT timeout. It also allows the software to place the board in `test mode` to test the geographical address bits without interference from the geographical address bits of the VMEbus slot in which the board is installed.



D[31:10]	Not used. Writes ignored, read as all 0's.
D9	SYSRESENA[1] 1 = Universe II LRST# asserted causes a Board Reset 0 = ignore Universe II LRST# (Refer to Figure 36 “cPLD and Universe II circuitry")
D8	SYSRESENA[0] 1 = VMEbus SYRESET# asserted causes a Board Reset 0 = ignore VMEbus SYRESET# (Refer to Figure 36 “cPLD and Universe II circuitry")
D[7:4]	Always read as 0's. Writing 0xA to these bits forces D3 to 0 which forces a Power Reset via the VME Power Monitor.
D3	Forced Power Reset (read only, writes ignored) 1 = attempting to force a Power Reset. When the power monitor detects the condition the bit returns to a 0 0 = normal operation
D2	GA_EN# 1/0 = test mode/normal. This bit is loaded from the internal Flash at Power Reset and is not affected by any resets.
D1	WDT Reset Enable - this bit is cleared by a Power Reset. 1 = Board Reset when WDT_TOUT# from the 6300ESB goes low. 0 = ignore WDT_TOUT# from the 6300ESB.
D0	WDT Reset Flag - this bit is cleared by a Power Reset. 1 = Board Reset has been provided due to WDT_TOUT# activation. 0 = No Board Reset due to WDT_TOUT# activation.

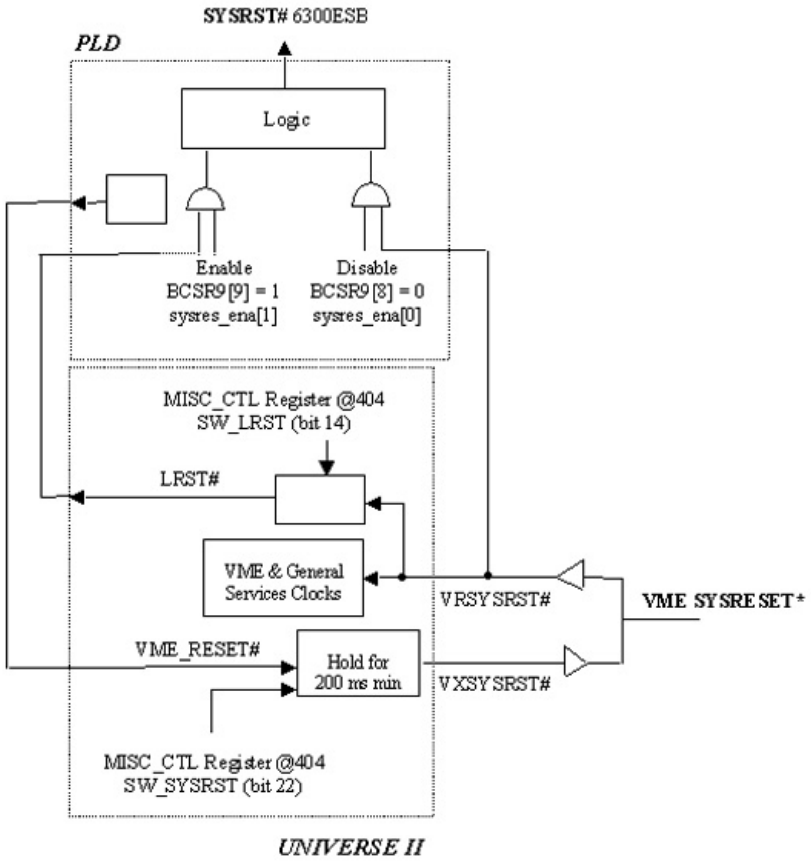


Figure 36: cPLD and Universe II Circuitry

9.5.8 Test, VME Slot ID (BCSR10..BCSR11)

BCSR10 is loaded from the internal Flash at Power Reset. The bit identifications are the same as the VME Slot ID register, BCSR8, but these bits drive open drain buffers that connect to the signals of the same name. Therefore, BCSR10 can only force a low on the corresponding bit. In order to test all the VME Slot ID bits, software should first isolate the geographic address pins by setting GA_EN# via BCSR9[2] (ACSEL bits are not affected by GA_EN#). Figure 37 shows how these circuits interact. BCSR10[31:8] ignore writes and are read as 0's.

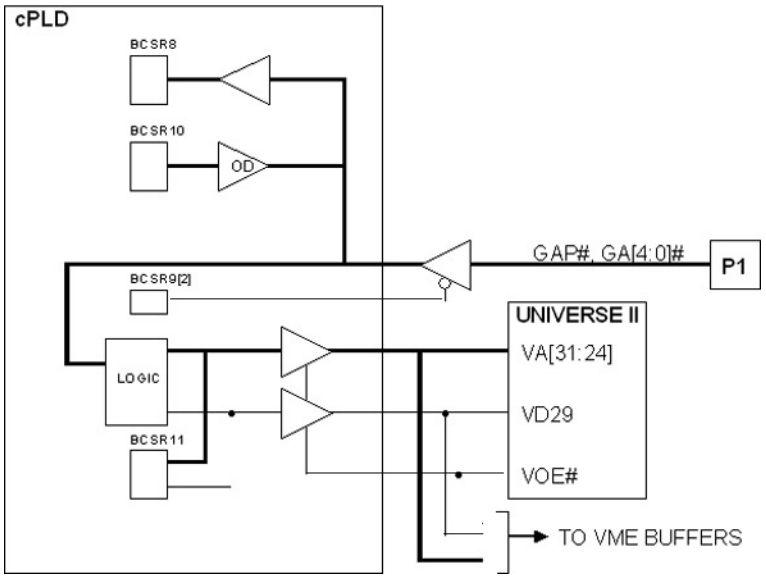
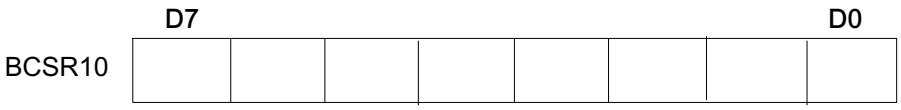
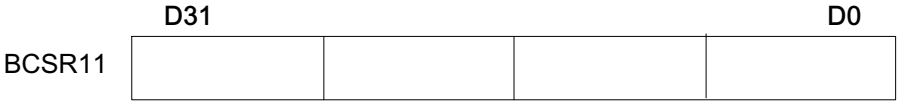


Figure 37: VME Slot ID



BCSR10 has the same bit definitions as BCSR8.



D[31:24]	VA[31:24] - these are the bit combinations that are passed to the Universe II in order to perform the geographical addressing or Auto slot ID. Note that these bits are not affected by VOE#.
D[23:6]	not used - always read as 0's.
D5	VD29 to Universe II in order to perform geographical or Auto-slot ID. Note that the bit is not affected by VOE#.
D[4:0]	not used - always read as 0's.

9.6 cPLD: Power Sequencer and Reset Generator

9.6.1 Power Sequencer

The power sequencer controls the sequencing of the board's Point Of Load (POL) power supplies. The board requires that the VMEbus provide at least the +5V and +3.3V power. After +5V comes up the power sequencer connects the VMEbus +3.3V power to the board. When these two VMEbus power rails are detected valid for a minimum time the power sequencer turns on the remaining supplies, with the exception of the CPU core. If either the +5V or +3.3V VMEbus supplies are detected low before the CPU core is switched on the sequencer turns off all the previously switched on voltages and waits for the VMEbus voltages to return to their proper operating level.

After all other power supplies are greater than their lower limits for a minimum amount of time the sequencer turns on the CPU core power supplies. After this point in time, if either of the VMEbus power supplies falls below the spec minimum or the thermal trip from the CPU occurs the sequencer will turn off VCCP, PVCPU0 and PVCPU1 supplies. The sequencer will remain in this last state until a Power Reset occurs and will light the front panel, red LED, “Processor HOT or Power Fail"

Figure 38 shows how the power routes to the major board components.

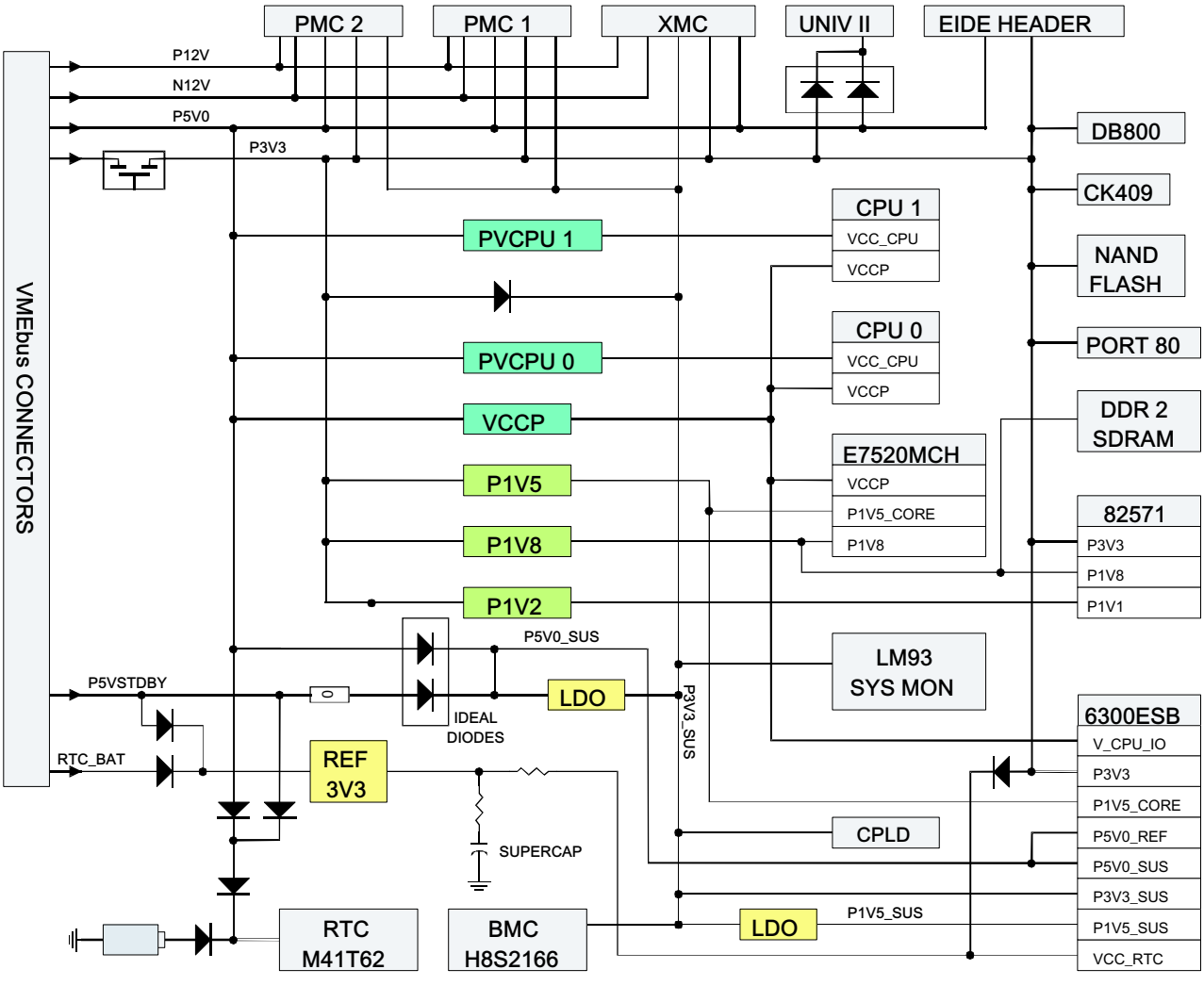


Figure 38: Power Diagram

9.6.2 Reset Generator

There are several types of resets presented to the board. These include resume Reset, Power Reset, System Reset, and Board Reset. Table 27 and Figure 39 show how the resets relate.

Reset Type	Sources	What is Reset
Resume Reset (RSMRSR#)	Voltage Monitor for +5VSTDBY of the backup power supply	CPLD and BMC. Remaining functions are mormally not powered. If VMEbus +5VSTDBY is not provided, it is generated from the VME-bus +5V supply (seeFigure 38 on page 92). In this case a Resume Reset also forces a Power Reset. At the completion of the Resume Reset the Power Sequencer of the cPLD continues to maintain the Power Reset until all the power supplies are within their operating range.
Power Reset (PWR_RST)	Power Sequencer, BMC, CPU via BCSR's	Board and VMEbus. Also forces a reload of certain BCSR register bits from the cPLD internal Flash, and renegotiation of the VME System Controller function
System Reset (SYSRESET*)	Power Sequencer, Front Panel Switch, Universe II Register, BMC	Board and VMEbus
	VMEbus SYSRESET*	If BCSR9[0] = 1, Board and VMEbus. Otherwise, SYSRESET* is ignored.
Board Reset (PCIRST#)	Front Panel Switch, 6300ESB RC Register at 0xCF9, P0 pin A6 pulled low, BMC	Board only. VMEbus SYSRESET* remains deasserted
	Watchdog Timer	Board only

Table 27: Types of Resets

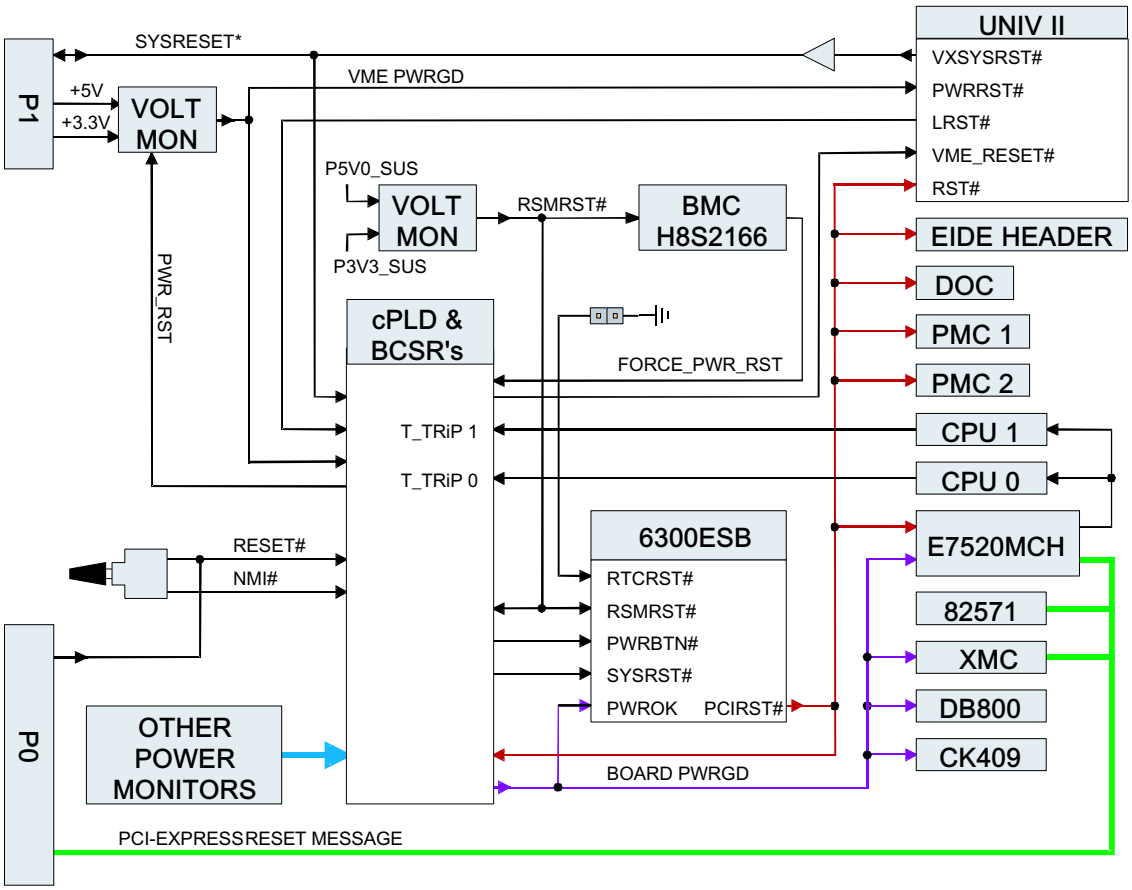


Figure 39: Reset Diagram

9.7 Interrupts Management

Figure 40 page 95 shows the onboard interrupt routing that are external to the 6300ESB.

The actual allocation of PCI bus interrupts to available interrupt controller inputs depends upon both the default “Plug-and-play" settings programmed by the BIOS, and the way in which the user has overridden them using the Setup screens. In the figure, MSI is a Message Signaled Interrupt, SMI is a System Management Interrupt, and NMI is a Non-Maskable Interrupt. Note that the source of the shared NMI may be ascertained via the BCSR's.

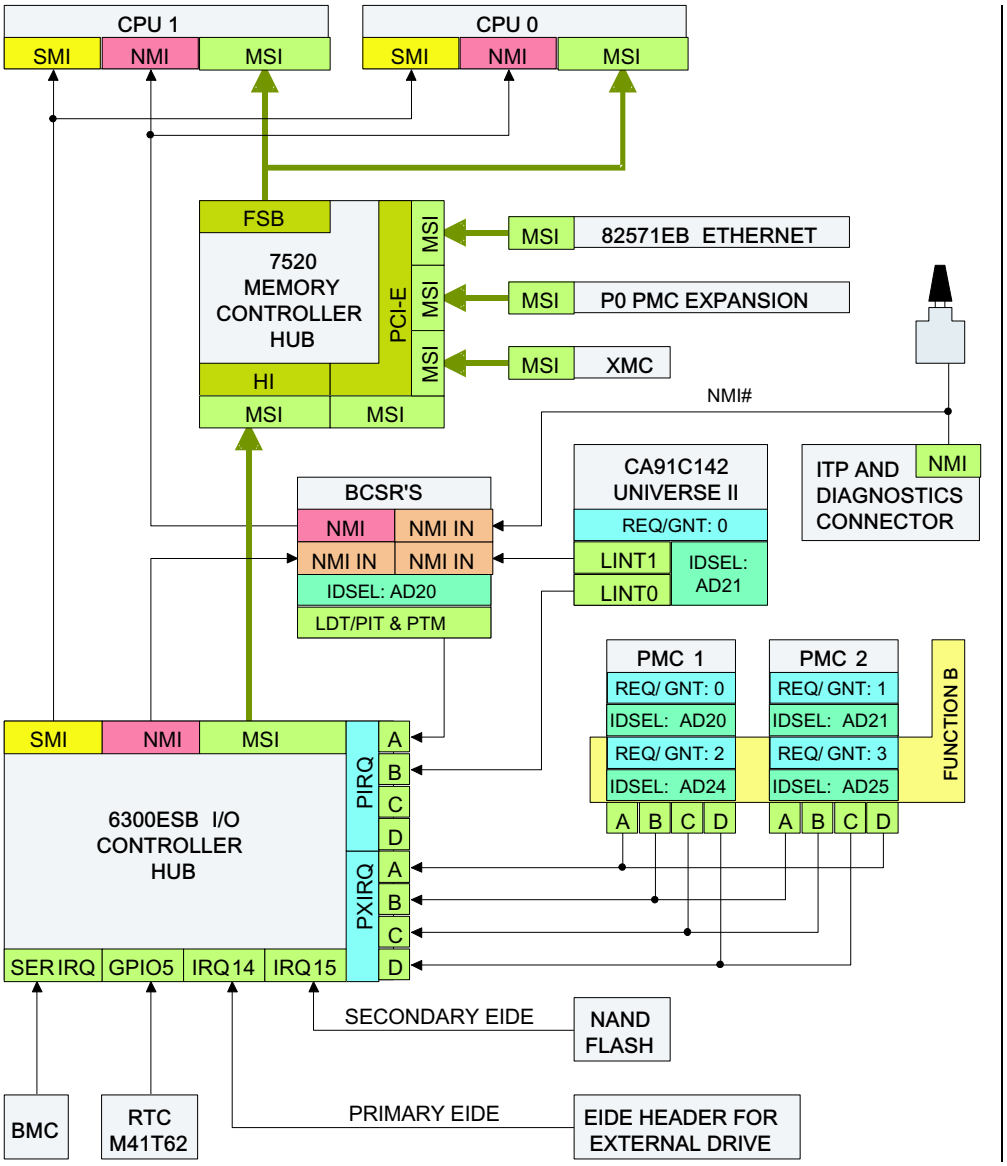


Figure 40: IRQ Routing Diagram

9.8 I/O Controller: Timers, Counters, RTC's and GPIO's

9.8.1 Timer/Counters

The 6300ESB provides three 8254-type timer/counters which have fixed uses. These timers are clocked by a 14.31818 MHz source.

> Counter 0, System Timer

This counter functions as the system timer by controlling the state of IRQ0 and is typically programmed for Mode 3 operation.

The counter produces a square wave with a period equal to the product of the counter period (838 ns) and the initial count value. The counter loads the initial count value one counter period after software writes the count value to the counter I/O address. The counter initially asserts IRQ0 and decrements the count value by two each counter period. The counter negates IRQ0 when the count value reaches zero. It then reloads the initial count value and again decrements the initial count value by two each counter period. The counter then asserts IRQ0 when the count value reaches zero, reloads the initial count value, and repeats the cycle, alternately asserting and negating IRQ0.

> Counter 1, Refresh Request

ISA platforms used to use this counter to provide the Refresh Request signal. Even though ISA is no longer used, this timer must still be programmed for Mode 2 operation and only affects the refresh toggle bit of Port 61.

The initial count is loaded one counter period after being written to at the counter address. The refresh toggle bit will exhibit a square wave behavior and toggle at the rate based on the counter value. DO NOT program this counter to other than Mode 2.

> Counter 2, Speaker Tone

This counter is usually programmed for Mode 3 operation. Some systems use the output from this timer to generate a speaker tone. No speaker is provided by this board, but a LED is provided that will illuminate when speaker tones would normally be generated (see section 9.2.3.2 “POST and Audio LED" on page 79). The intent is for software to illuminate the LED to indicate a Power reset Self Test (POST) failure.

9.8.2 Watchdog Timer

The PENTXM2 or PENTXM4 board includes a hardware Watchdog timer that can be used by the operating software to monitor the normal operation of the system.

The timer is enabled by software. Once enabled it must be restarted at regular intervals. If it is not restarted the timer will expire and cause a Non-Maskable Interrupt (NMI) or reset to the local processor.

The watchdog timer facility is provided by the 6300ESB I/O Controller Hub. Details of how it is used are provided in the Intel datasheet.

The Board Management Controller monitors the Watchdog Timeout pin of the 6300ESB.

9.8.3 Real Time Clocks (RTC's)

> RTC#1

The 6300ESB provides a RTC. This includes a PC-AT clock, calendar, and 242 bytes of CMOS RAM for BIOS configuration functions. It is used as the main RTC device when the board is on.

This RTC is not powered by a battery when the board is off.

> RTC#2

A secondary RTC is also provided and fitted on the board: ST Microelectronics M41T62, with backup power provided by an onboard 35 mAh battery: Panasonic BR1225A. The battery provides more than ten years of power backup under normal operation. The secondary RTC is accessed via the I2C bus at address 0xD0 as shown in Figure 26 on page 32, and can generate an interrupt using GPIO5 of the 6300ESB

Its main purpose is to ensure time retention: time and date are restored from the RTC#2 to the RTC#1 each time the BIOS gets started or reset.

> VMEbus +5VSTDBY

The clock and configuration RAM functions can be maintained from an external supply via the VMEbus `+5VSTDBY` pin for battery free operation if required.

9.8.4 GPIO's

The 6300ESB provides general purpose input, output, or I/O pins. Some pins are legacy PC-specific and others are available for platform-specific uses. This board uses the platform-specific pins as shown in Table 28 “6300ESB GPIO Assingments".

In this table:

- where no description is given, the pin is currently not assigned,
- the yellow shaded GPIO signals are in the suspend power well,
- the others GPIO signals are in the core power well.

GPIO	DIR	Description
0	IN	PXREQ2# (2nd Function, PMC Site 1)
1	IN	PXREQ3# (2nd Function, PMC Site 2)
2	IN	BIOS defaults to restore, 1/0 = user/factory defaults - **User-configured**
3	IN	Operating Mode, 1/0 = BIOS/VSA - **User-configured**
4	IN	Watchdog Timer, 1/0 = Enable/Inhibit - **User-configured**
5	IN	IRQ# from RTC, M41T62
6	IN	Hard Drive Header, EIDE PDIAG
7	IN	NAND Flash, PDIAG of SST55LD019
8	IN	P/U
11	I/O	SMB ALERT#
12	IN	P/U
13	IN	P/U
16	OUT	PXGNT2# (2nd Function, PMC Site 1)
17	OUT	PXGNT3# (2nd Function, PMC Site 2)
18	OUT	USB2 Power Enable (not used)
19	OUT	USB3 (front panel) Power Enable
20	OUT	USB0 (rear) Power Enable
21	OUT	USB1 (rear) Power Enable
23	OUT	NAND Flash Write Protect (WP_PD# to SST55LD019)
24	I/O	Powers up as output
25	I/O	Powers up as output
27	I/O	Powers up as output
28	I/O	DDR_RST_GATE (resets DDR Registers)
32	I/O	Watchdog Timer, WDT_TOUT#
33	IN	PXIRQA# (pulled to +3.3V, not 5V tolerant)
34	I/O	PXIRQB# (pulled to +3.3V, not 5V tolerant)
35	I/O	PXIRQC# (pulled to +3.3V, not 5V tolerant)
36	I/O	PXIRQD# (pulled to +3.3V, not 5V tolerant)
37	I/O	Ethernet 1 Location, 1/0 = Rear/Front
38	I/O	Ethernet 2 Location, 1/0 = Rear/Front
39	I/O	User Jumper, 1/0 = pins open/shunt installed
40	I/O	P/U
41	I/O	routed to P0 pin C10 - IRQ capable (pulled to +3.3V, not 5V tolerant)
42	I/O	routed to P0 pin D10 - IRQ capable (pulled to +3.3V, not 5V tolerant)
43	I/O	routed to P0 pin E10 - IRQ capable (pulled to +3.3V, not 5V tolerant)
56	OD	
57	OD	

Table 28: 6300ESB GPIO Assignments

9.9 ITP Debug and Diagnostics Support

A 100-pin high density connector located at the front edge of the board under PMC Site 2 provides the ITP connections and other functions in order to support manufacturing and debug of the board.

9.9.1 ITP

In order to support debug and test the Integrated Test Port (ITP) signal routing is identical to the Intel Allagash reference design. Please contact Kontron for more information on this functionality.

9.9.2 JTAG Ports

Three JTAG ports support the programming of the cPLD, BMC, and board testing as shown in Figure 41.

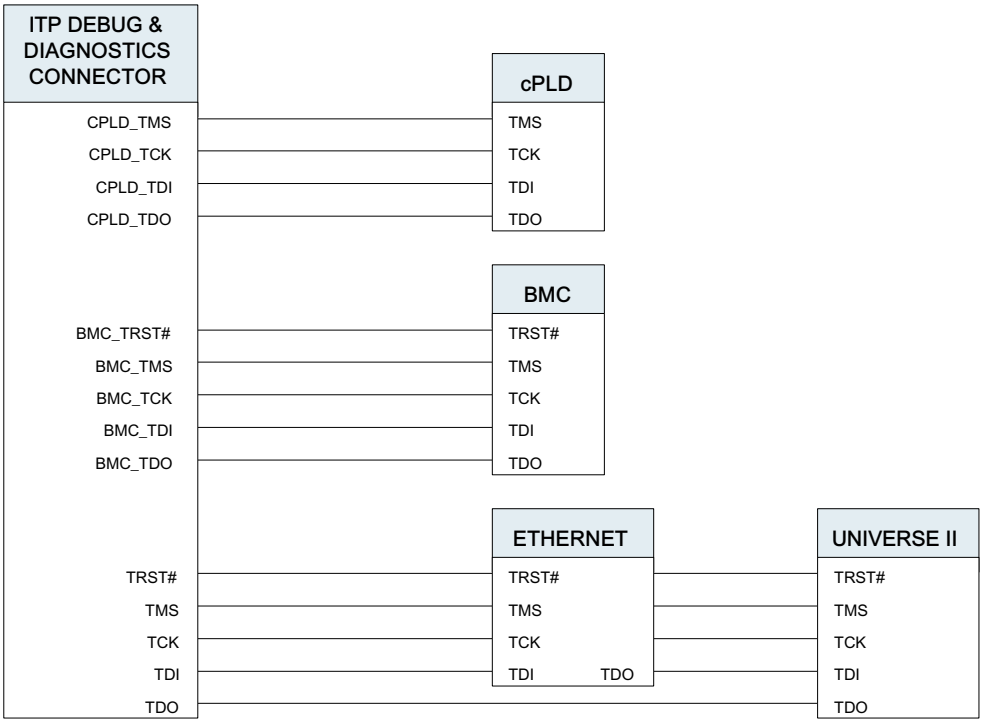


Figure 41: JTAG Simplified Schematic

Chapter 10 - BIOS Firmware

The PENTXM2 or PENTXM4 board uses a BIOS firmware that performs many of the functions of a standard desktop PC. The BIOS firmware includes additional features specifically tailored for the VMEbus environment and the board-specific features.

BIOS Associated Documentation

InsydeH2O Firmware for PENTXM2 and PENTXM4 - User Reference Manual SD.DT.E86

Saving the BIOS Parameters

The only way to save BIOS parameters is in onboard BIOS Flash EPROM.

PCI Device IDs

Each PCI bus, and each device on an individual PCI bus, has a unique ID. For the PENTXM2 or PENTXM4, the bus and device IDs are BIOS dependent and also depend upon the current devices installed in the XMC and PMC sites, and whether or not the PCIe expansion interface (at P0) is in use. The ways to obtain this list are OS-dependent.

Appendix A - Specifications

This appendix covers items such as power requirements, environment specifications, etc.

A.1 Power Requirements

Description	Pmax(1)	Ptyp.(2)
PENTXM2-SA 1.67 GHz, SDRAM 1 GB	40 W = 5V * 3.58A + 3.3V * 6.7A	24.2 W (3) = 5V * 1.1A + 3.3V * 5.67A
PENTXM4-SA 1.67 GHz, SDRAM 1 GB	68.5 W = 5V * 7.4A + 3.3V * 9.55A	40 W (3) = 5V * 3.2A + 3.3V * 7.27A

(1) Pmax = Maximum power requirements (IDE, DDR, FFT).
(2) Ptyp. = Typical power requirements at OS prompt.
(3) The power is measured at Linux prompt with no software application running.

Specification for mezzanine modules can be found in the documentation for those modules.

When a PMC or XMC module is plugged to the PENTXM2 or PENTXM4, +3.3V, +5V, +12V and -12V power consumptions of this module are directly supplied by the VME backplane. See the specifications to get additional power comsumptions.

WARNING

Only use the PENTXM2 or PENTXM4 in backplanes that supply power on both P1 and P2 connectors. Failure to observe this warning may result in damage to the board.

WARNING

Ensure that your PENTXM2 or PENTXM4 is correctly inserted into the backplane connectors.

A.2 EMC Regulatory Compliance and Safety

- CEM: compliance to CE standards EN55082 and EN55022 class A.
- FCC: compliance to Class A.

A.3 Flammability Rating

All PCBs are manufactured by UL approved manufacturers and have a flammability rating of 94V-0.

A.4 MTBF Data

Calculations are made according to the standard MIL HDBK 217F Notice 2.

Results below are given for six types of environment:

- Ground Benign GB
- Air Inhabited Cargo AIC
- Naval Sheltered NS
- Air Rotary Wing ARW
- Air Uninhabited Fighter AUF
- Ground Mobile GM

A.4.1 PENTXM2/SA

- PENTXM2-SA: DDR2-400-SDRAM 1 GB, User Flash Disk 4GB
- Order Code: PENTXM2-SA34S-*xxxxx*

Ground Benign (Hours)		Air Inhabited Cargo (Hours)	Naval Sheltered (Hours)		Air Rotary Wing (Hours)	Air Uninhabited Fighter (Hours)	Ground Mobile (Hours)
25°C	40°C	40°C	25°C	40°C	55°C	40°C	30°C
295,633	224,891	39,796	48,189	42,442	11,607	17,080	35,936

Table 29: PENTXM2/SA - MTBF Data (SDRAM 1 GB)

- PENTXM2-SA: DDR2-400-SDRAM 4 GB, User Flash Disk 4GB
- Order Code: PENTXM2-SA38S-*xxxxx*

Ground Benign (Hours)		Air Inhabited Cargo (Hours)	Naval Sheltered (Hours)		Air Rotary Wing (Hours)	Air Uninhabited Fighter (Hours)	Ground Mobile (Hours)
25°C	40°C	40°C	25°C	40°C	55°C	40°C	30°C
248,668	203,892	34,655	40,552	36,645	10,732	15,149	31,552

Table 30: PENTXM2/SA - MTBF Data (SDRAM 4 GB)

A.4.2 PENTXM4/SA

> PENTXM4-SA: **DDR2-400-SDRAM 1 GB,** User Flash Disk 4GB

> Order Code: PENTXM4-34S-*xxxxx*

Ground Benign (Hours)		Air Inhabited Cargo (Hours)	Naval Sheltered (Hours)		Air Rotary Wing (Hours)	Air Uninhabited Fighter (Hours)	Ground Mobile (Hours)
25°C	40°C	40°C	25°C	40°C	55°C	40°C	30°C
223,457	169,036	32,573	38,387	33,291	8,742	13,471	27,308

Table 31: PENTXM4/SA - MTBF Data (SDRAM 1 GB)

> PENTXM4-SA: **DDR2-400-SDRAM 4 GB**, User Flash Disk 4GB

> Order Code: PENTXM4-38S-*xxxxx*

Ground Benign (Hours)		Air Inhabited Cargo (Hours)	Naval Sheltered (Hours)		Air Rotary Wing (Hours)	Air Uninhabited Fighter (Hours)	Ground Mobile (Hours)
25°C	40°C	40°C	25°C	40°C	55°C	40°C	30°C
204,241	162,958	30, 599	35,422	31,233	8,483	12,784	25,804

Table 32: PENTXM4/SA - MTBF Data (SDRAM 4 GB)

A.5 Environmental Specifications

For operating environment exceeding the following specification, ruggedized versions of PENTXM2 or PENTXM4 board are available. Contact Kontron for further information.

A.5.1 PENTXM2/SA

	SA Standard Commercial
Conformal Coating	Optional
Airflow	1.2 m/s without throttling at 40°C
Temperature	VITA 47-Class AC1
Cooling Method Operating Storage	Convection 0 °C to +55 °C -45 °C to +85 °C
Vibration Sine (Operating)	20/500 Hz: 2g
Random	VITA 47-Class V1
Shock (Operating)	20g/11 ms Half Sine
Altitude (Operating)	-1,640 to 15,000 ft
Relative Humidity	90% without condensation

Table 33: PENTXM2 Environmental Specifications

A.5.2 PENTXM4/SA

	SA Standard Commercial
Conformal Coating	Optional
Airflow	2.7 m/s without throttling at 55°C
Temperature	VITA 47-Class AC1
Cooling Method Operating Storage	Convection 0 °C to +55 °C -45 °C to +85 °C
Vibration Sine (Operating)	20/500 Hz: 2g
Random	VITA 47-Class V1
Shock (Operating)	20g/11 ms Half Sine
Altitude (Operating)	-1,640 to 15,000 ft
Relative Humidity	90% without condensation

Table 34: PENTXM4 Environmental Specifications

A.6 Air Flow Characterisation

The PENTXM2 or PENTXM4 design is based on the Dual-Core Intel Xeon chipset (processor and host bridge). This chipset includes sophisticated temperature management technologies. It is important to understand the PENTXM2 or PENTXM4 design to be able to anticipate the board behaviour in various cooling situations.

PENTXM2 or PENTXM4 1 slot VME solution heatsinks for processor and host bridge (MCH) have been designed such as to use the processors 100% capacity (no throttling).

The following tables provide the necessary information on the required airflow to keep the PENTXM2 or PENTXM4 within its design enveloppe (processors operating at full speed and enough junction temperature margin on the host bridge).

Keeping the PENTXM2 or PENTXM4 in the **SAFE AREA** will ensure proper behaviour and performance.

Two set of measurements are provided, according to the direction of the airflow:

- from PMC slots to CPU area
- from CPU area to PMC slots

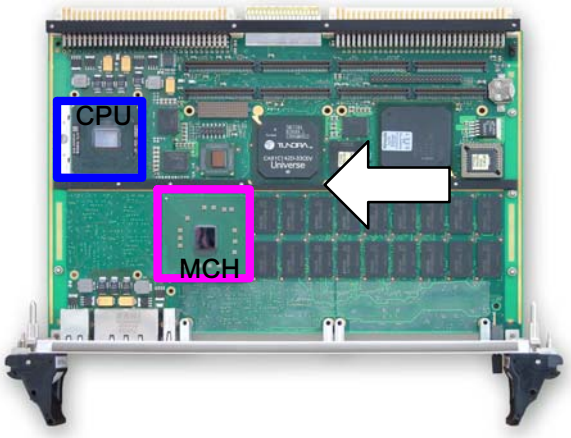
Other heatsink solutions can be evaluated for specific applications that cannot meet the airflow conditions described below. In such a case, contact your Kontron representative.

A.6.1 PENTXM2 (One Dual-Core Intel Xeon Processor)

A.6.1.1 Air Flowing from CPU Area to PMC Slots

Results non available in current release of the manual. Please contact your Kontron representative.

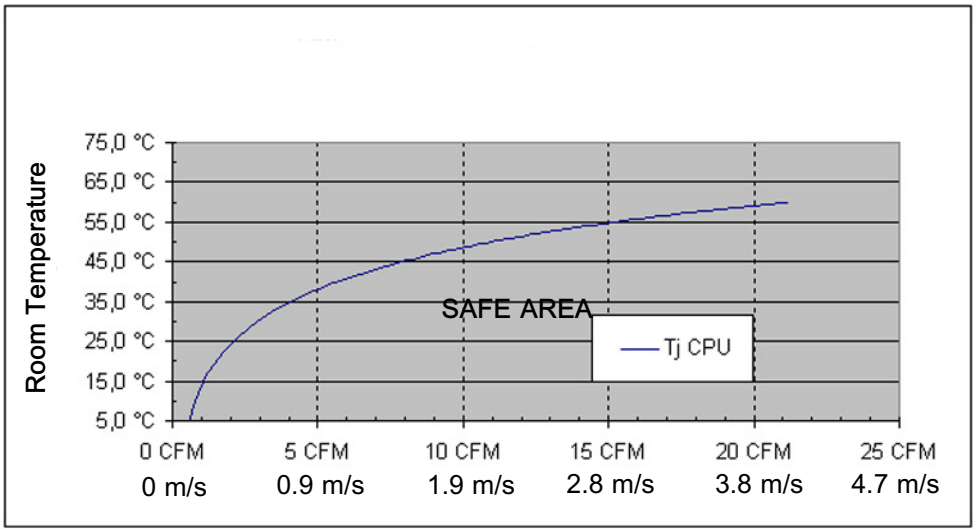
A.6.1.1 Air Flowing from PMC Slots to CPU Area



Following curve shows maximum acceptable temperature for the junction temperature of the processor.

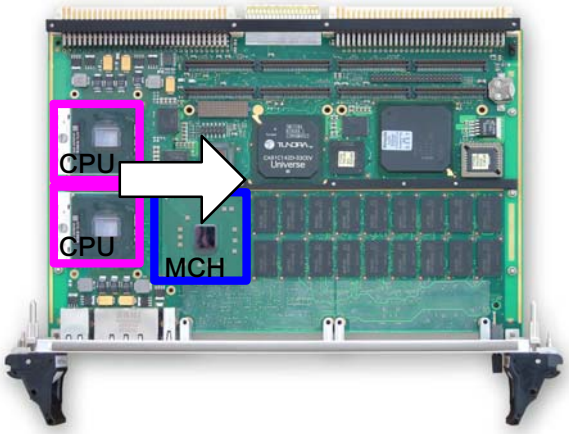
For instance, at 55°C, minimum air flow needed to cool enough the processor die is about 15 CFM (2.8 m/s).

Note The curve that shows the case temperature of the host bridge (MCH) is identical with the curve that shows the junction temperature of the processor.



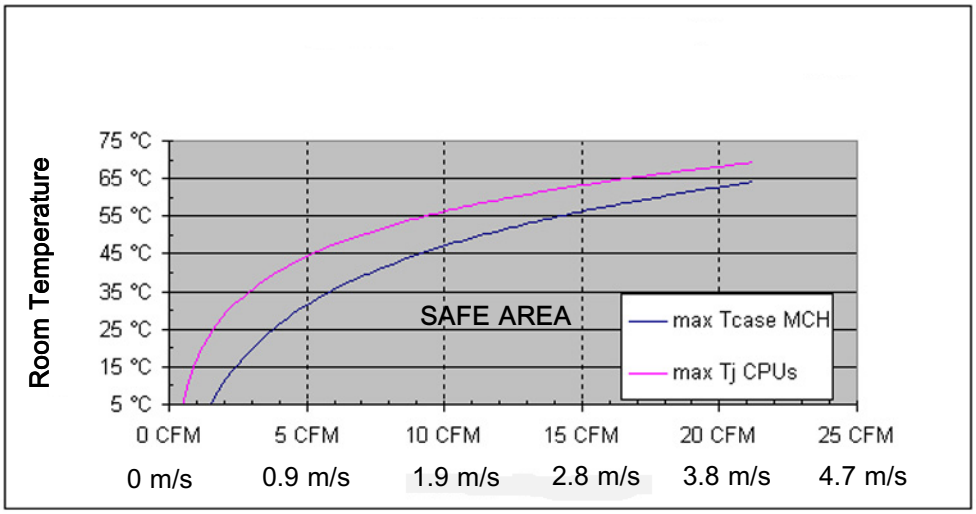
A.6.2 PENTXM4 (Twin Dual-Core Intel Xeon Processors)

A.6.2.1 Air Flowing from CPUs Area to PMC Slots

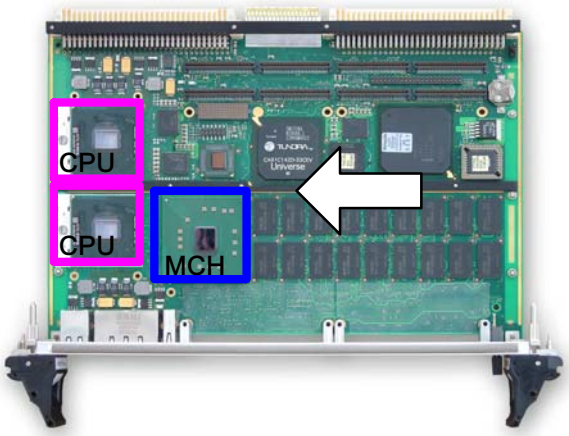


Following curves show maximum acceptable temperature for the junction temperature of both processors and the case temperature of the host bridge (MCH).

For instance, at 55°C, minimum air flow needed to cool enough the MCH device is about 14 CFM (2.6 m/s)



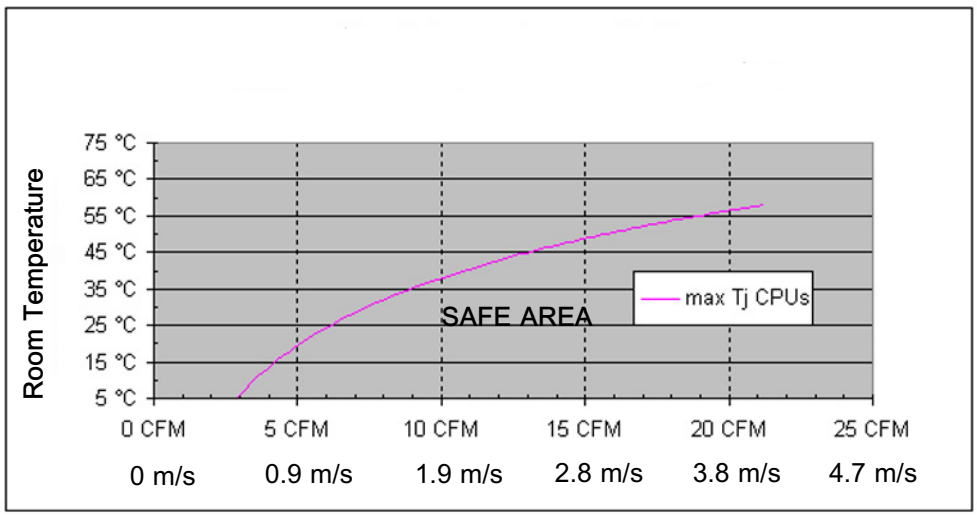
A.6.2.2 Air Flowing from PMC Slots to CPUs Area



Following curve shows maximum acceptable temperature for the junction temperature of both processors.

For instance, at 55°C, minimum air flow needed to cool enough the processor die is about 19 CFM (3.6 m/s).

Note The curve that shows the case temperature of the host bridge (MCH) is identical with the curve that shows the junction temperature of both processors.



A.7 Mechanical Construction

The PENTXM2 or PENTXM4 is build on a multi-layer double Eurocard and conforms to the dimensions specified in the ANSI/VITA VME64 1-1994. The dimensions shown below are in millimetres, with inches (in parentheses) for general guidance only.

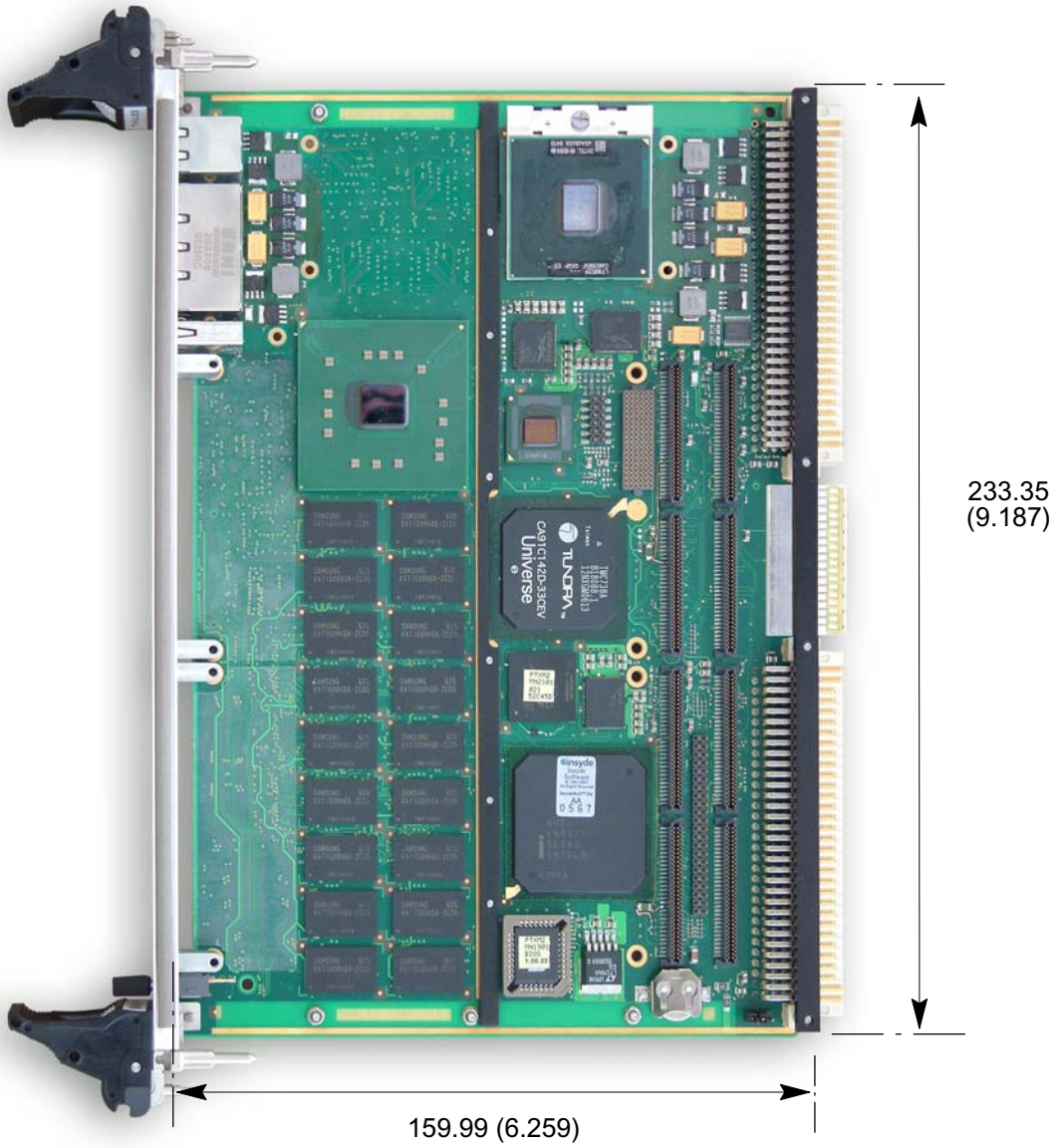


Figure 42: VME Dimensions

- **Length** : 233.35 mm
- **Depth** : 160 mm (without connectors)
- **Height** : 1 VME slot compatible
- **Weight** : 490 gr. approximately

Specifications

The VMEbus signals are detailed in Chapter 6 “Connectors”, section 6.1.3 “P1 and P2 row v (VMEbus) Connector Pin Assignment” and section 6.1.5 “VMEbus Signal Description”.

2eSST . . . . . Two edges Source Synchronous Transfer. This protocol, defined in VITA 1.5--200x draft standard, is a protocol where the source (transmitter) transmits data synchronised to both the falling and rising edge of the strobe. This performance of the 2eSST is determined by the skew (the variation of the propagation delay through drivers, backplane and receivers) not by the propagation delay itself. The 2eSST protocol provides for tranfer rates of 160 MB/s, 267 MB/s and 320 MB/S.

A16 . . . . . Providing or decoding addresses on **VMEbus** address lines A01 to A15.

A24 . . . . . Providing or decoding addresses on **VMEbus** address lines A01 to A23.

A32 . . . . . Providing or decoding addresses on **VMEbus** address lines A01 to A31.

AIX . . . . . Advanced Interactive Executive from **IBM** (UNIX).

AMD . . . . . Advanced Micro Devices. A chip manufacturer.

ANSI . . . . . American National Standards Institute.

API . . . . . Application Program Interface.

Arbiter . . . . . An arbiter accepts requests and grants control to one **requester** at a time.

ARPA . . . . . The US Defence Advanced Research Projects Agency.

ASCII . . . . . American Standard Code for Information Interchange. A 7-bit code, established by ANSI, to achieve compatibility between data services. Equivalent to the international **ISO** 7-bit code.

ATM . . . . . Asynchronous Transfer Mode.

AUI . . . . . Attachment Unit Interface. The cable that connects the **DTE** to the **MAU**. Also called the **Drop Cable**.

Backplane (VMEbus) . . . . . A **PCB** with 96- or 160-pin connectors and signal paths that bus the connected pins. Some systems have a single PCB, called the J1 backplane. This provides the signal paths needed for basic operation. Other systems also have a second PCB, called the J2 backplane. This provides the additional 96- or 160-pin connectors and signal paths needed for wider data and address transfers. The J1 and J2 sections may be combined into a single J1/J2 backplane PCB.

BBSY . . . . . Bus Busy on the **VMEbus**.

BCLR . . . . . Bus Clear on the **VMEbus**.

BERR . . . . . Bus ERRor on the **VMEbus**.

Big-endian . Refers to the way in which multi-byte data is stored in memory. Big-endian data is stored with the most significant byte at the lowest address (68XXX style). See also **Little-endian**.

BLT . . . . . BLock Transfer on the **VMEbus**.

Byte . . . . . An 8-bit data structure.

Cache . . . . . A small, fast access memory between the processor and the larger, slower main memory. Used to store the most recently used instructions/data to improve overall memory access time.

CHRP . . . . . Common Hardware Reference Platform.

Chassis . . . . See **enclosure**.

Chassis Ground . . . . . Most applications require the chassis to be connected to earth, normally via a main cable or separate earthing strap.

CL . . . . . Cas Latency is the ratio between column access time (t_{CAC}) and the clock cycle time (t_{CLK}), rounded to the next higher whole number.

CPU . . . . . Central Processing Unit.

CR/CSR . . . . Configuration ROM/Control and Status Register on data and address lines.

CTS . . . . . Clear To Send. A serial signal. See **RTS**.

D64 . . . . . Sending and receiving data 64 bits at a time over D00 to D31 and A01 to A32/LWORD on the **VMEbus**.

D32 . . . . . Sending and receiving data 32 bits at a time over D00 to D31 on the **VMEbus**.

D16 . . . . . Sending and receiving data 16 bits at a time over D00 to D15 on the **VMEbus**.

D08(EO) . . . . Sending and receiving data 8 bits at a time over D00 to D07 or D08 to D15 on the **VMEbus**.

D08(O) . . . . . Sending and receiving data or Status/**ID** 8 bits at a time over D00 to D07 on the **VMEbus**.

Daisy Chain A signal line that propagates a signal from board to board (or chip to chip), starting with the first slot and ending at the last slot. There are 4 **VMEbus** grant daisy chains and one **VMEbus** interrupt acknowledge daisy chain.

DC . . . . . Direct Current.

DCD . . . . . Data Carrier Detect. A serial signal.

DMA . . . . . Direct Memory Access. A direct, rapid link between a peripheral and main memory that avoids the use of the processor to transfer each item of data.

DRAM . . . . . Dynamic **RAM**. Memory that must be refreshed periodically to maintain the storage of information.

DSR . . . . . Data Set Ready. A serial signal.

DTE . . . . . Data Terminal Equipment. The data terminal devices themselves. A category that includes the computer.

DTR . . . . . Data Terminal Ready. A serial signal.

D-type . . . . . A connector that has the approximate shape of a capital letter `D'.

E^{2}PROM (or EEPROM) . . . . . Electrically Erasable **PROM**. PROM whose contents can be erased electrically, so allowing the device to be re-used with new data.

ECC . . . . . Error Correcting Code. The data is protected by Error Correction Coding capable to detecting all single bit and double bit errors, and correcting single bit errors.

EIA-232 . . . . Standard interface approved by Electronic Industries Alliance (EIA) for connecting serial devices. It supports two types of connectors -- a 9-pin D-type connector (DB-9) or a 25-pin D-type connector (DB-25) connector.

EIA-422 . . . . EIA standard for connecting serial devices. The EIA-422 is designed to replace the older EIA-232 because it supports higher data rates and greater immunity to electrical interferences. EIA-422 supports multipoint connections..

EIA-485 . . . . EIA standard for multipoint communications. It supports several types of connectors, including DB-9 and DB-37. RS-485 is similar to RS-422 but can support more nodes per line because it uses lower-impedance drivers and receivers.

EMC . . . . . Electro-Magnetic Compatibility.

Enclosure . . A rigid framework that provides mechanical support for boards inserted into the **backplane**, ensuring that the connectors mate properly and that adjacent boards do not touch each other. It also guides the cooling airflow through the system and ensures that inserted boards do not disengage themselves from the backplane due to vibration or shock.

ESD . . . . . Electrostatic Sensitive Device.

Ethernet . . . Ethernet is a baseband, thick-wire network based on an access method called **CSMA/CD**. It was originally developed by the Xerox Corporation in 1972.

FIFO . . . . . First In First Out. A data queuing mechanism (or the implementation of it) in which the first item stored is the first item processed.

Flash Memory A type of high-capacity **E^2PROM**.

FPU . . . . . Floating Point Unit.

FTP . . . . . File Transfer Protocol. See **TCP/IP**.

FSB . . . . . Front Side Bus. Physical bi-directional data bus that carries all electronic signal information between the central processing unit (CPU) and other devices within the system such as random access memory (RAM), the system BIOS, PCI expansion cards, hard disks, etc.

GND . . . . . The Ground (0V) signal or supply rail.

Handler . . . . See **Interrupt Handler.**

I(x-y) . . . . . The **interrupter** can generate interrupt requests on **VMEbus** lines IRQx* to IRQy*.

IBM . . . . . International Business Machines.

ICPMC . . . . . Kontron 3 slot PMC carrier board.

ID . . . . . Identification.

IDSEL . . . . . Device Number.

IEEE . . . . . Institute of Electrical and Electronic Engineers.

IH(x-y) . . . . . The **interrupt handler** can generate interrupt acknowledge cycles in response to interrupt requests on **VMEbus** lines IRQx* to IRQy*.

Interrupter . An interrupter generates an interrupt request on the **VMEbus** and then provides status/**ID** information when requested by the **interrupt handler**.

Interrupt Handler . . . . . An interrupt handler detects interrupt requests on the **VMEbus**, generated by **interrupter**s. It acknowledges these requests with an IACK* and responds to them by requesting Status/**ID** information.

I/O . . . . . Input/Output.

IPSD . . . . . Kontron up to 256 MB memory mezzanine.

ISA . . . . . Industry Standard Architecture. Very commonly used bus in PC architectures.

ISO . . . . . International Standards Organisation.

JEDEC . . . . . Joint Electronic Devices Engineering Committee.

JTAG . . . . . Joint Test Action Group. A standard for chip-level testing.

KBD . . . . . Keyboard.

L1 Cache . . . First-level **cache**. Integrated inside the processor.

L2 Cache . . . Second-level **cache**. Often implemented outside the processor.

LED . . . . . Light Emitting Diode. A semiconductor diode that radiates light. LEDs that emit in the visible region are used as indicators or warnings.

Little-endian Refers to the way in which multi-byte data is stored in memory. Little-endian data is stored with the least significant byte at the lowest address. See also **Big-endian**.

LSB . . . . . Least Significant Bit.

Master . . . . . A **VMEbus** master initiates bus cycles to transfer data between itself and a **slave** module.

MBLT . . . . . Multiplexed BLock Transfer. A data block transfer that uses address lines as well as data lines.

Mezzanine . The American term for a daughter board.

MSB . . . . . Most Significant Bit.

MTBF . . . . . Mean Time Between Failures.

NFS . . . . . Network File Server.

NMI . . . . . Non-Maskable Interrupt.

NVRAM . . . . Non-volatile **RAM**. Memory that does not lose its information when powered down.

OEM . . . . . Original Equipment Manufacturer.

PC . . . . . Personal Computer.

PCB . . . . . Printed Circuit Board.

PCI . . . . . Peripheral Component Interconnect.

PENTXM2 or PENTXM4 . . . . . Kontron processor card based on the Sossaman dual core processor.

PLCC . . . . . Plastic Leadless Chip Carrier.

PMC . . . . . PCI Mezzanine Card.

POSIX . . . . . Portable Operating System Environment. An **IEEE** standard.

PReP . . . . . PowerPC Reference Platform. An example implementation of a philosophy designed to allow 100% binary compatibility across different platforms, when based on the PowerPC processor.

PRI . . . . . Prioritised. A **VMEbus arbiter** that prioritises the four VMEbus request lines from BR0* (the lowest) to BR3* (the highest) and responds with BG0IN* to BG3IN*. It also informs the VMEbus **master** when there is a higher level request than that being processed, by driving BCLR* low.

RAM . . . . . Random Access Memory. Memory that can be read from or written to at any time.

Requester . . A **VMEbus** requester requests use of the VMEbus when it is required by a **master**.

RI . . . . . Ring Indicator. A serial line signal.

RISC . . . . . Reduced Instruction Set Computer. The basic principle is to have a small set of simple instructions that execute very quickly (i.e. in one cycle). This means that programs are longer in size, and sometimes more complicated, but run faster.

RMW . . . . . Read Modify Write. An indivisible **VMEbus** cycle that is used to both read from and write to a **slave** without permitting any other **master** to access that slave during the cycle. This is most useful in multiprocessing systems where certain memory locations are used to control access to certain resources (e.g. semaphores).

RNE . . . . . Release NEver. A bus release mode that applies to **VMEbus**.

ROC . . . . . Release On Clear. A bus release mode that applies to **VMEbus**.

ROM . . . . . Read Only Memory. Semiconductor memory whose components are not alterable by computer instructions and power off.

ROR . . . . . Release On Request. An access scheme in which the **VMEbus requester** only relinquishes control of the bus when it is required by another requester. This has an advantage over the **RWD** scheme in that if no other **master** uses the bus, the bus request phase of a transfer is avoided.

RRS . . . . . Round Robin Select. Round robin is a **VMEbus** arbitration scheme for resources in which resource **bandwidth** is shared equally between competing requests of different levels. A requester that is granted a resource on one arbitration cycle has the lowest priority on the next arbitration cycle.

RTS . . . . . Ready To Send. A serial signal. See **CTS**.

RTC . . . . . Real Time Clock.

SATA . . . . . Serial Advanced technology Attachment. Serial ATA is a computer bus technology primarily designed for transfer of data to and from a hard disk.

SCSI . . . . . Small Computer Systems Interface. A standard and associated hardware for general purpose communication (usually) between a processor and large capacity storage devices (e.g hard disks).

Slave . . . . . A slave detects **VMEbus** cycles initiated by a **master** and, when these cycles specify its participation, transfers data between itself and the master.

Slot . . . . . A position where a board can be inserted into a **backplane**. If the system has both a J1 and a J2 backplane (or a combination J1/J2 backplane), each slot provides a pair of 96- or 160-pin connectors.

SMI . . . . . System Management Interrupt.

SPECint95 . . A benchmark package, produced in 1995, measuring the integer performance of a processor.

SPECfp95 . . A benchmark package, produced in 1995, measuring the floating point performance of a processor.

Superscalar A superscalar processor is a processor with multiple execution units that *may* operate in parallel.

System Controller . . . . . A board in **slot** 1 of the **VMEbus backplane**. It must have a SYSCLK driver, an **arbiter**, an IACK **daisy chain** driver and a bus timer.

TBD . . . . . To Be Defined.

TCP/IP . . . . . Transport Control Protocol/Internet Protocol. A collection of network protocols that together support host-to-host communication for hosts connected to any of a number of heterogeneous networks.

Network Layer Protocols (ISO Level 3)

IP
Provides internet transaction services for Layer 4 clients.
Generally considered as providing Host-to-Host datagram delivery.

Transport Layer Protocols (ISO Layer 4)

TCP: A connection oriented reliable byte-stream protocol.

UDP: An unacknowledged transaction-oriented protocol parallel to TCP.

Session, Presentation and Application Layer Protocols (ISO Layers 5 to 7)

FTP: Permits exchange of complete files between computers.

Telnet: Provides virtual terminal services for interactive access by terminal servers to hosts.

Telnet . . . . . The ARPA application level protocol. A bi-directional, **byte**-oriented communications protocol. See **TCP/IP**.

Timeout . . . . The elapsing of a period of time within which an action should have happened.

TSOP . . . . . Thin Small Outline Package.

U . . . . . The U is a standard unit of height measurement (e.g. 3U). One U is 4.445 centimetres (1.75 inches).

UAT . . . . . Unaligned Address Transfer. A **VMEbus** data transfer cycle that sends or receives data in an unaligned fashion.

USB . . . . . Universal Serial Bus.

UDP . . . . . User Datagram Protocol. See **TCP/IP**.

VCC . . . . . The five volt supply rail.

VITA . . . . . VMEbu International Trade Association.

VME . . . . . Versa Module Europe. Often used as an abbreviation for **VMEbus**.

VMEbus . . . . An **ANSI/IEEE** standard (1014 - 1987) for a versatile backplane bus based on the Eurocard mechanical standard.

Write Posting This is a pipelining technique that can be used for example in the VME interface chip to increase system performance.

In Master Write Posting, when a local bus **master** writes to the **VMEbus**, instead of requesting and arbitrating for the bus, transferring data to the slave and waiting for the acknowledgement, the VME interface chip acknowledges the local bus master immediately after gaining VMEbus ownership and captures the address and data to write. The local bus master can then continue with its processing and the VME interface chip transfers the data for the host.

Slave Write Posting works in a similar way. Write operations to the VME interface chip as a VME **slave** do not wait for the chip to write the data to the host memory and do not wait for its acknowledge. The VME interface chip acknowledges the VME bus immediately after gaining local bus ownership and captures the address and data to write. Another transfer can then take place on the VMEbus while the VME interface chip writes the data from the previous one.

XMC . . . . . Switched Mezzanine Card: an evolution of the PMC mezzanine card that includes a new connector and the electric signals necessary for switched communications between the mezzanine card and its carrier.

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