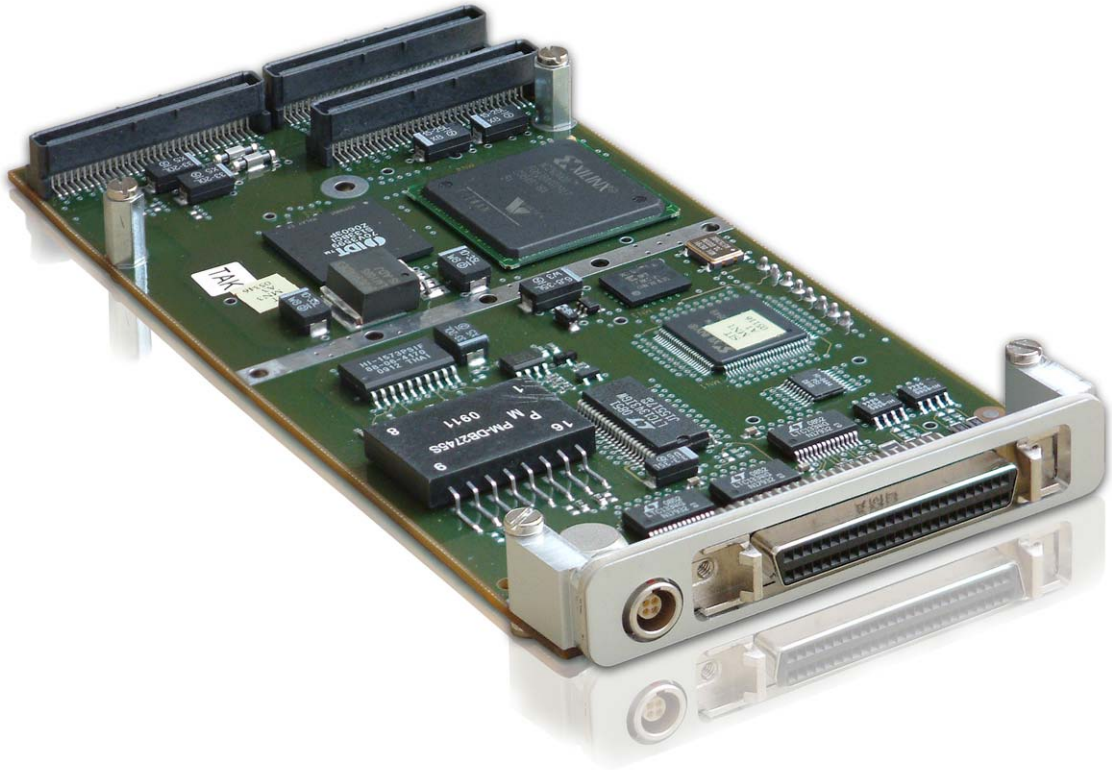
» PMC-6L «



User's Guide

CA.DT.A33-4e - July 2010

Revision History

Publication Title:	PMC-6L User's Guide	
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Rev.	Brief Description of Changes	Date of Issue
4e	New Kontron Corporate Identity	July 2010

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Kontron follows the DEEE/WEEE directive.

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- reduce waste arising from electrical and electronic equipment (EEE)
- make producers of EEE responsible for the environmental impact of their products, especially when they become waste
- encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- improve the environmental performance of all those involved during the lifecycle of EEE

Conventions

This guide uses several types of notice: Note, Caution, ESD.

Note: this notice calls attention to important features or instructions.


Caution: this notice alert you to system damage, loss of data, or risk of personal injury.


ESD: This banner indicates an Electrostatic Sensitive Device.

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix `0x' shows a hexadecimal number, following the `C' programming language convention.

The multipliers `k', `M' and `G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when `K', `M' and `G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

When describing transfer rates, `k' `M' and `G' mean $*10^3$, $*10^6$ and $*10^9$ *not $*2^{10}$ $*2^{20}$ and $*2^{30}$.*

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and CompactPCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Signal names ending with an asterisk (*) or a hash (#) denote active low signals; all other signals are active high.

Signal names follow the PICMG 2.0 R3.0 CompactPCI Specification and the PCI Local Bus 2.3 Specification.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions


Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.


Caution, Electric Shock!
Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Chapter 1 - Introduction

1.1 Manual Overview

This manual describes the PMC-6L board from Kontron. The PMC-6L is the first member of Kontron activities of multifunction Input/Output PCI Mezzanine Card (PMC). This PMC is designed to meet the requirements of compact, real-time systems for the most demanding defense and aerospace application.

- Chapter 1: Board's features.
- Chapter 2: Unpacking, installation and identification instructions.
- Chapter 3: Functional characteristics of the PMC.
- Chapter 4: PMC connectors and associated cables.
- Appendix A: General, physical and environmental specifications, power requirements, EMC regulatory compliance and safety, flammability rating and MTBF data.
- Appendix B: List of abbreviations.

1.2 Conventions

The following symbols and terminology conventions are use in this manual:

This symbol indicates Electrostatic Sensitive Devices (ESD). Appropriate ESD precautions should be taken.

This symbol indicates information that is important for personal safety or board operation.

This symbol indicates general information.

- Addresses and signal names are shown in capital letters.
- Following the PCI convention, signal names ending with a # indicate active low signals, all other signals are active high.
- All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix 0x indicates a hexadecimal number, following the 'C' programming language convention.

1.3 Related Documents

This guide is written to cover a wide range of people; from installation technicians, operators, and system managers, to hardware and software engineers. To better understand how the PMC-6L functions, these individuals should be familiar with the concepts of the following documents.

Document	Ordering Information
PCI Local Bus Specification: Revision 2.2 - 1998	PCI Special Interest Group P.O. Box 14070 Portland, OR 97214 www.pcisig.com
Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC) IEEE Std 1386.1-2001	IEEE Standards Department Order Department 445 Hoes Lane, P.O. Box 1331 Piscataway, NJ 08855-1331 www.ieee.org
Standard Mechanics for a Common Mezzanine Card Family (CMC) - IEEE 1386-2001	
American National Standard for Conduction Cooled PMC - ANSI/VITA 20-2001	VITA P.O. Box 19658 Fountain Hills AZ 85269-1958 www.vita.com
Digital Time Division Command/Response Multiplex Data Bus - MIL-STD 1553B	
Electrical Characteristics for Unbalanced Double-Current Interchange Circuits - ITU-T V.28	ITU Place des Nations CH-1211 Geneva 20 Switzerland www.itu.int
Electrical Characteristics for Unbalanced Double-Current Interchange Circuits Operating at Data Signalling Rates Nominally up to 100 kbit/s - ITU-T V.10	
Electrical Characteristics of Generators and Receivers for Use in Balanced Digital Multipoint Systems - TIA/EIA 485-A	Electronic Industries Alliance Technology Strategy and Standards Department 2500 Wilson Boulevard Arlington, Virginia 22201 USA www.eia.org
Mark 33 Digital Information Tranfer System - ARINC SPECIFICATION 429	

Table 1: Industry Specifications and User Documentation

1.4 PMC-6L Overview

The PMC-6L board is intended to be used with the Kontron Single Board Computer PowerEngine7 host board.

The main component of the board is the FPGA which manages:

- the PCI bus interface,
- the 1553B bus in Bus Controller (BC) and Remote Terminal (RT),
- the ARINC-429 interfaces (4 receive channels and 2 transmit channels),
- the serial lines (up to six full duplex asynchronous lines, or three full duplex synchronous lines),
- the GPIOs (up to 16 General Purpose I/O signals),
- a real-time clock,
- the accesses to the shared memory,
- the interruptions.

Only the physical interfaces are external to the FPGA.

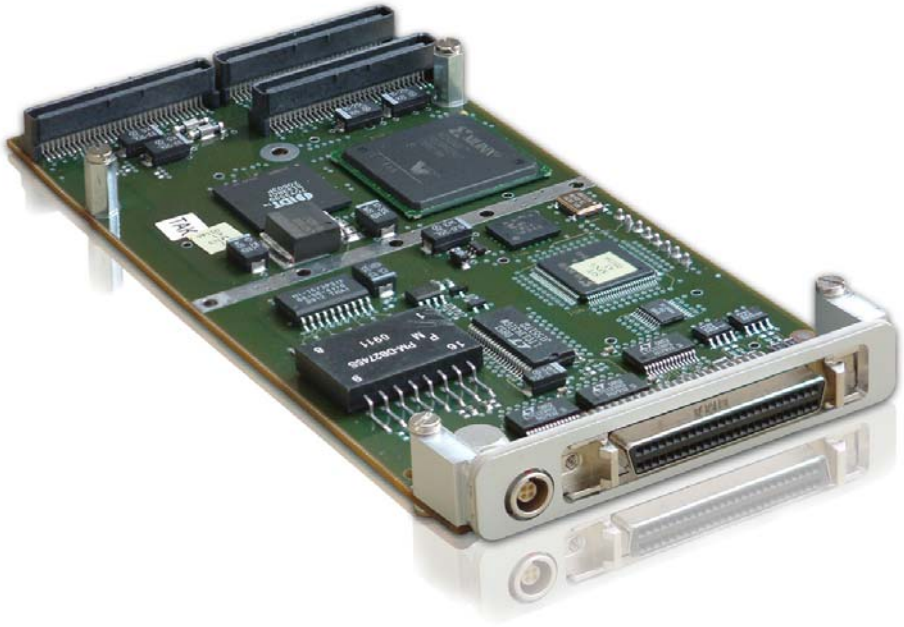

Figure 1: PMC-6L Overview

1.4.1 Features and Functions

- Single PMC form factor
- ARINC-429 Interface
  - Four receive channels (dual speed),
  - Two transmit channels (dual speed),
  - Receive and transmit FIFOs implemented in the shared RAM.
- MIL-STD-1553
  - Single redundant Channel, Bus Controller (BC) or Remote Terminal (RT).
- Serial Lines
  - Up to six serial lines, either EIA-485/422 or EIA-232 interfaces,
  - HDLC Layer 2 protocol capability.
- Up to sixteen General Purpose I/O (GPIO);
  refer to Table 3 "PMC-6L Build Option Description" on page 5.
- Local 512 KB Shared Memory
- PCI Interface
  - Power Supply: 3.3V signaling,
  - PCI bus speed: 33 MHz,
  - PCI bus width: 32 bits.
- Rugged Conduction-Cooled Version available
- Targeted O.S. : VxWorks 6.2

1.4.2 Block Diagram

Figure 2 shows a simplified block diagram of the board.

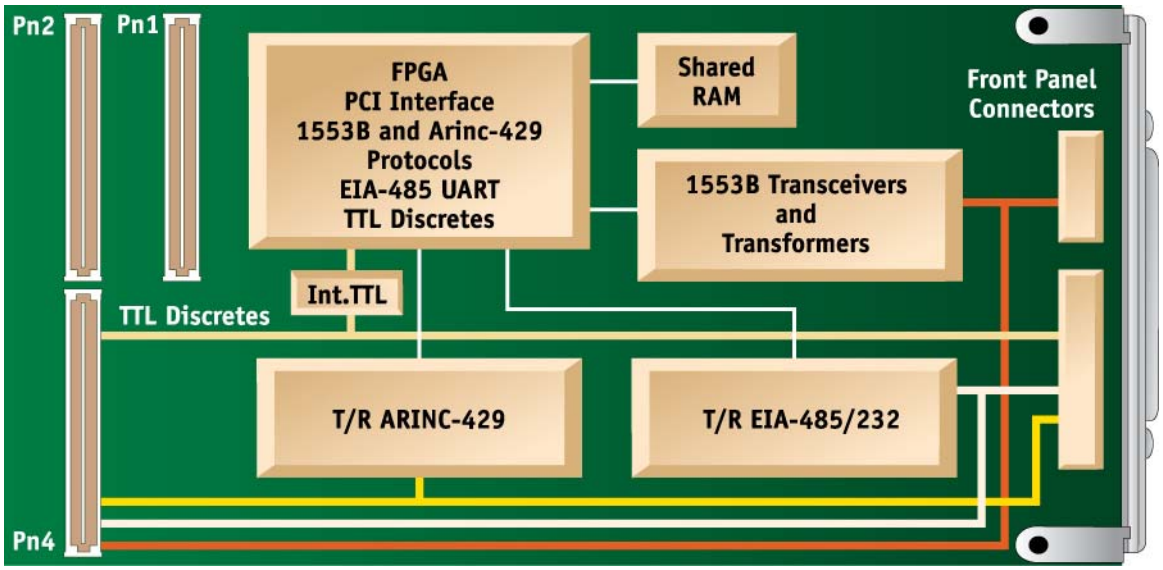

Figure 2: PMC-6L Block Diagram

1.4.3 Order Code

Order Code	Description
PMC-6L-SA	
PMC-6L-SAB000	PMC-6L Air-cooled commercial build, B-Type: Quad UART + 16 GPIO
PMC-6L-SAH000	PMC-6L Air-cooled commercial build, H-Type: Six UART + 8 GPIO
PMC-6L-SAM000	PMC-6L Air-cooled commercial build, M-Type: Full Model + 14 GPIO

Table 2: PMC-6L Order Code

Serial I/O Build Option Environment Class Options available through	B-Type SA/WA Front Panel only	M-Type SA/WA Front Panel only	H-Type SA/WA/RC Front Panel for SA/WA Pn4 for SA/WA/RC
MIL-STD-1553B	Single Redundant Channel, Bus Controller or Remote Terminal		
ARINC-429	4 Receive and 2 Transmit Channels		
Serial Lines	4 UART Simple Lines or 2 HDLC Synchronous Full Duplex Lines	Full Modem Single Port	6 UART Simple Lines or 3 HDLC Synchronous Full Duplex Lines
GPIO Lines	16	14	16 (front + rear)

Table 3: PMC-6L Build Option Description

In **SA/WA** environment classes, for the **B-Type** and **M-Type** serial I/O build options, the options are available only via the **FP1/FP2 Front Panel Connectors**; refer to sections 4.1.2 "FP1 Connector Pin Assignment" and 4.1.3 "FP2 Connector Pin Assignement" on pages 37 and 38.

For the **H-Type** serial I/O build option,

- in **SA/WA** environment classes, the options are available via the **FP1/FP2 Front Panel Connectors**; refer to sections 4.1.2 "FP1 Connector Pin Assignment" and 4.1.3 "FP2 Connector Pin Assignement" on pages 37 and 38.
- in **SA/WA/RC** environment classes, the options are also available via the **Pn4 PMC Connector**; refer to section 4.3.4 "Pn4 PMC Connector Pin Assignment" on page 44.

For the **H-Type** serial I/O build option, **16 GPIO lines** are available:
- **8** via the FP2 Front Panel Connector **or** via the Pn4 PMC connector.
- **8** available only via the Pn4 PMC connector.

Chapter 2 - Preparing Before Using

2.1 Installation

Note Don't throw out the shipping box, it should be used to store or ship the board.

The PMC-6L is shipped in an individual, reusable shipping box closed by an ESD stick-on label.

Closely inspect the board for any signs of shipment-related damages such as loose components or bent pins. If any evidence of damage is discovered, please notify the carrier and Kontron immediately.

The PMC-6L board attaches to a PMC host board. The attaching hardware for the PMC-6L board is included with your order.

Attach the PMC-6L board to the PMC host board according to the following steps.

1. Remove the PMC host board from the chassis.
2. Unscrew the four screws on the bottom of the PMC-6L as described below:

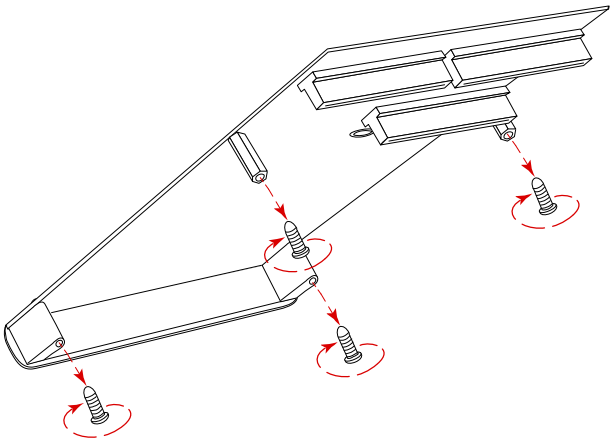

Figure 3: Preparing the PMC-6L

3. Attach the PMC-6L board to the host board by first positioning the PMC-6L front panel bezel with the EMI gasket in the opening on the host board front panel. On a PowerEngine7 host board, the PMC-6L board is fitted to one of the two PCI slot.
   Figure 4 "Installation of a PMC-6L on a PowerEngine7" page 7 gives an example of the PMC-6L fitted to the 64-bit PCI slot, referenced "PMC 1" on the board front panel.
4. Position the PCI connectors so that they engage the corresponding PCI connectors on the host board. Place the host board on a static-free flat surface, and press down on the PMC-6L board to fully engage the PCI connectors.
5. Secure the PMC-6L board to the host board by inserting the screws supplied with the PMC-6L board through the bottom of the PMC host board and into the standoffs and front panel attached to the PMC-6L board.
6. Insert the PMC host board back into the chassis making sure it is plugged into the backplane.
7. The PMC-6L board attachment is now complete.

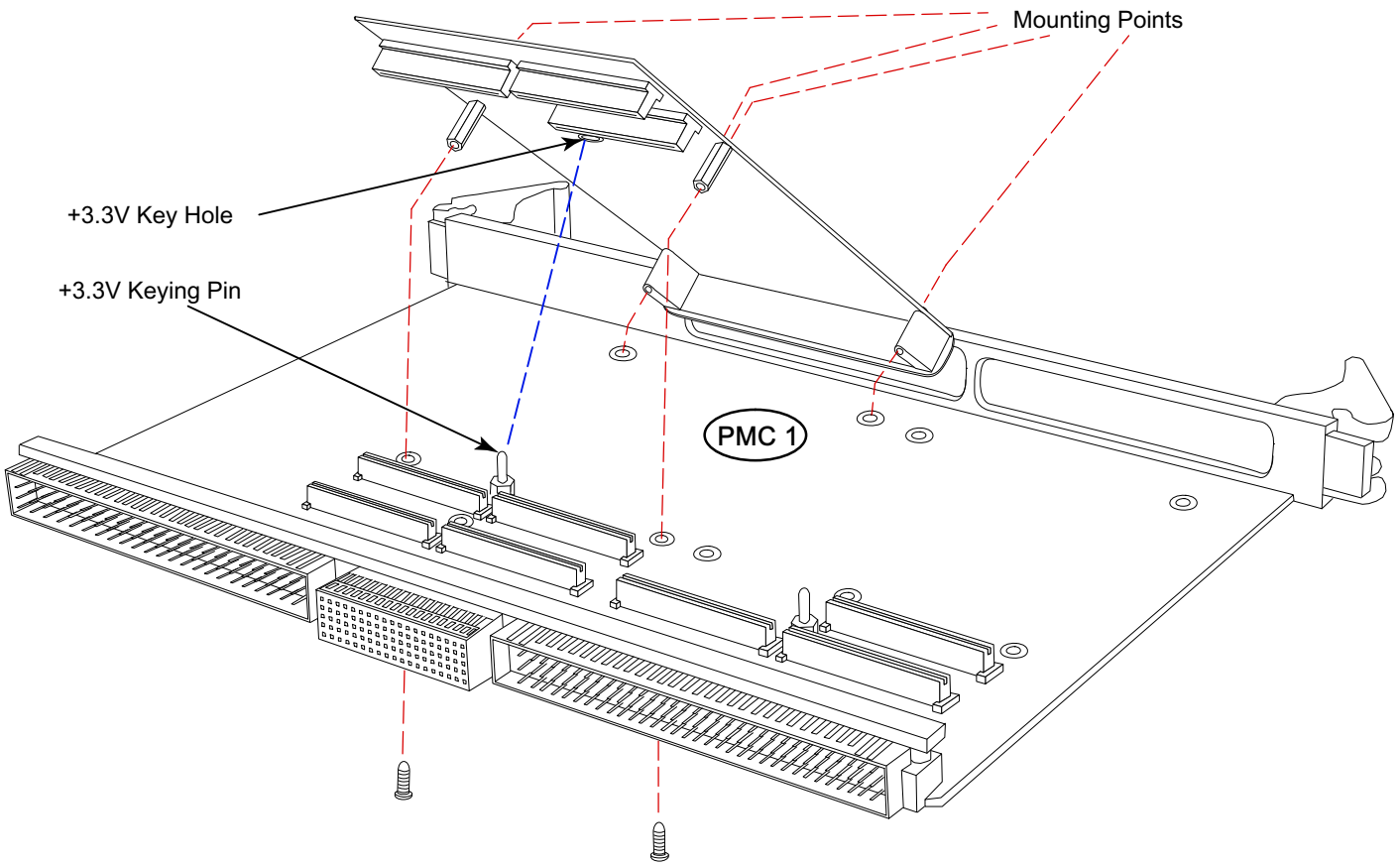

Figure 4: Installation of a PMC-6L on a PowerEngine7 Board

2.2 Board Identification

Kontron PMC-6L boards are identified by labels fitted to the bottom side and to the top side.

Labels fitted to the bottom side of the PMC-6L

- (A) "Chronological serial number" label.
- (B) "Board Identification" label.
- (C) "Variant" and "Engineering Change Level" (E.C. Level) label.

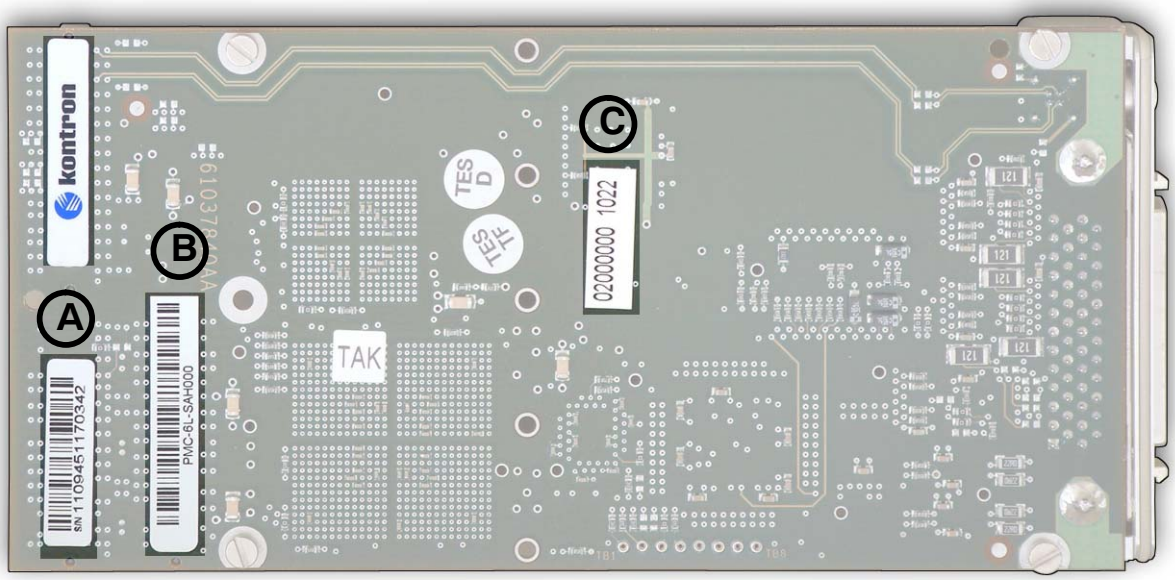

Figure 5: Bottom Side Identification Labels

Labels fitted to the top side of the PMC-6L

D "PLD Identification" label.

E "Flash Identification" label.

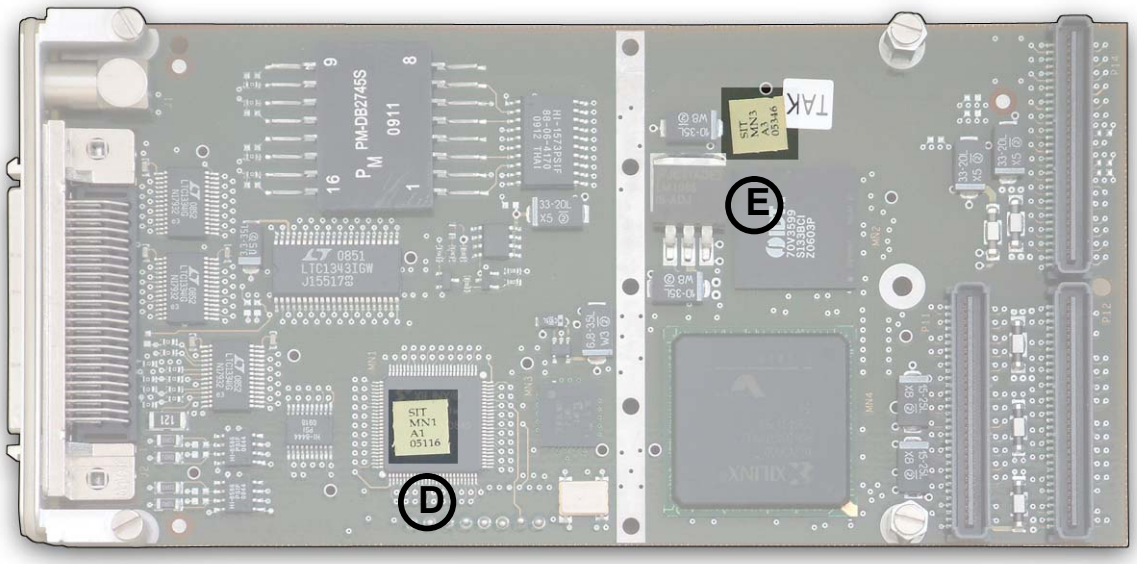

Figure 6: Top Side Identification Labels

Chapter 3 - Functional Description

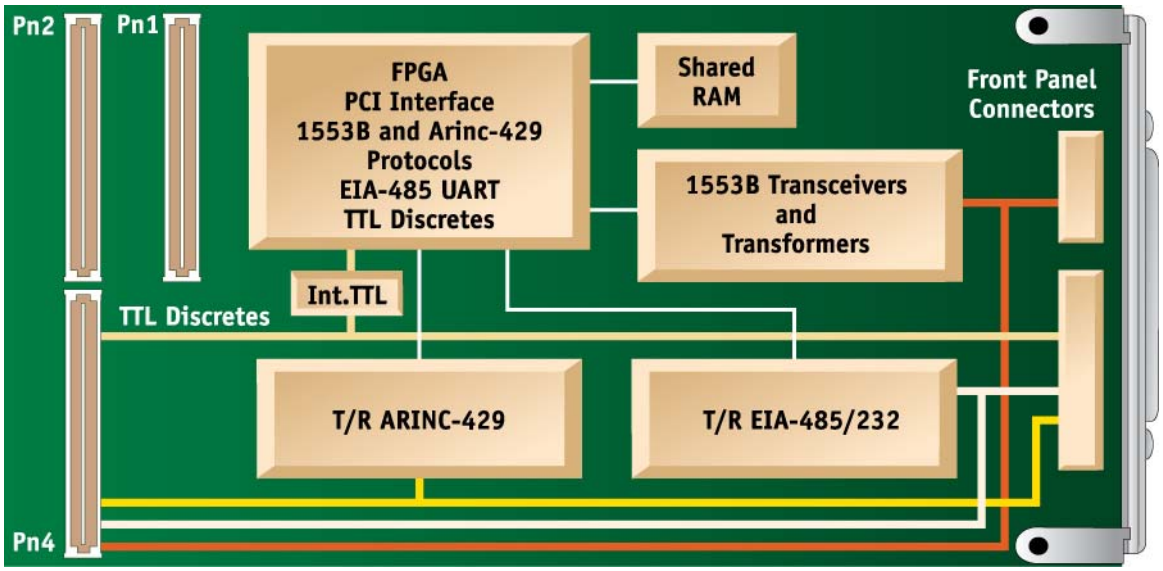

Figure 7: PMC-6L Block Diagram

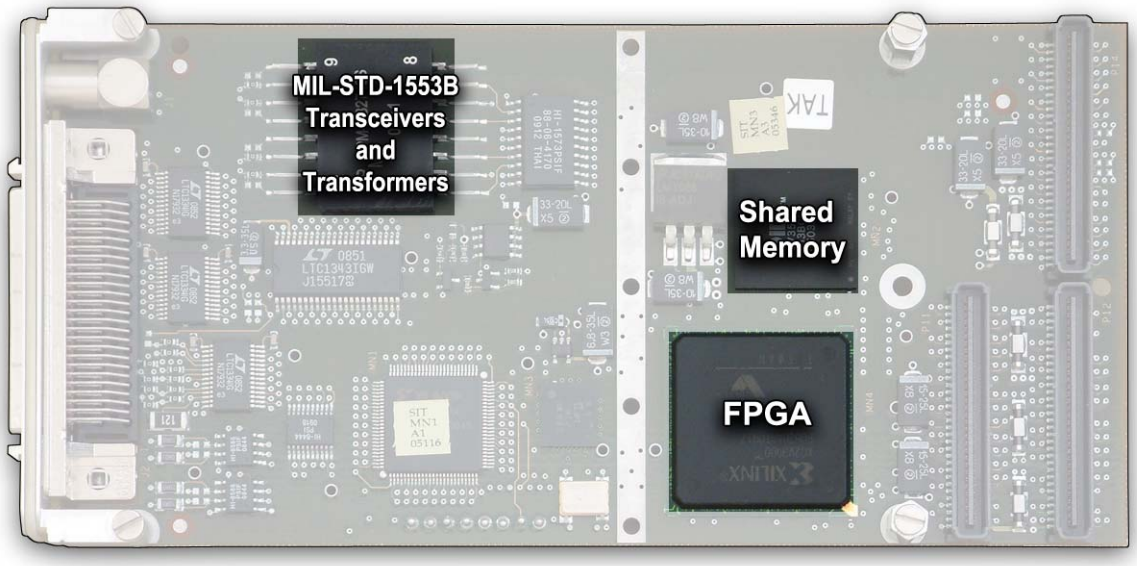

Figure 8: PMC-6L Top Face Layout

3.1 FPGA

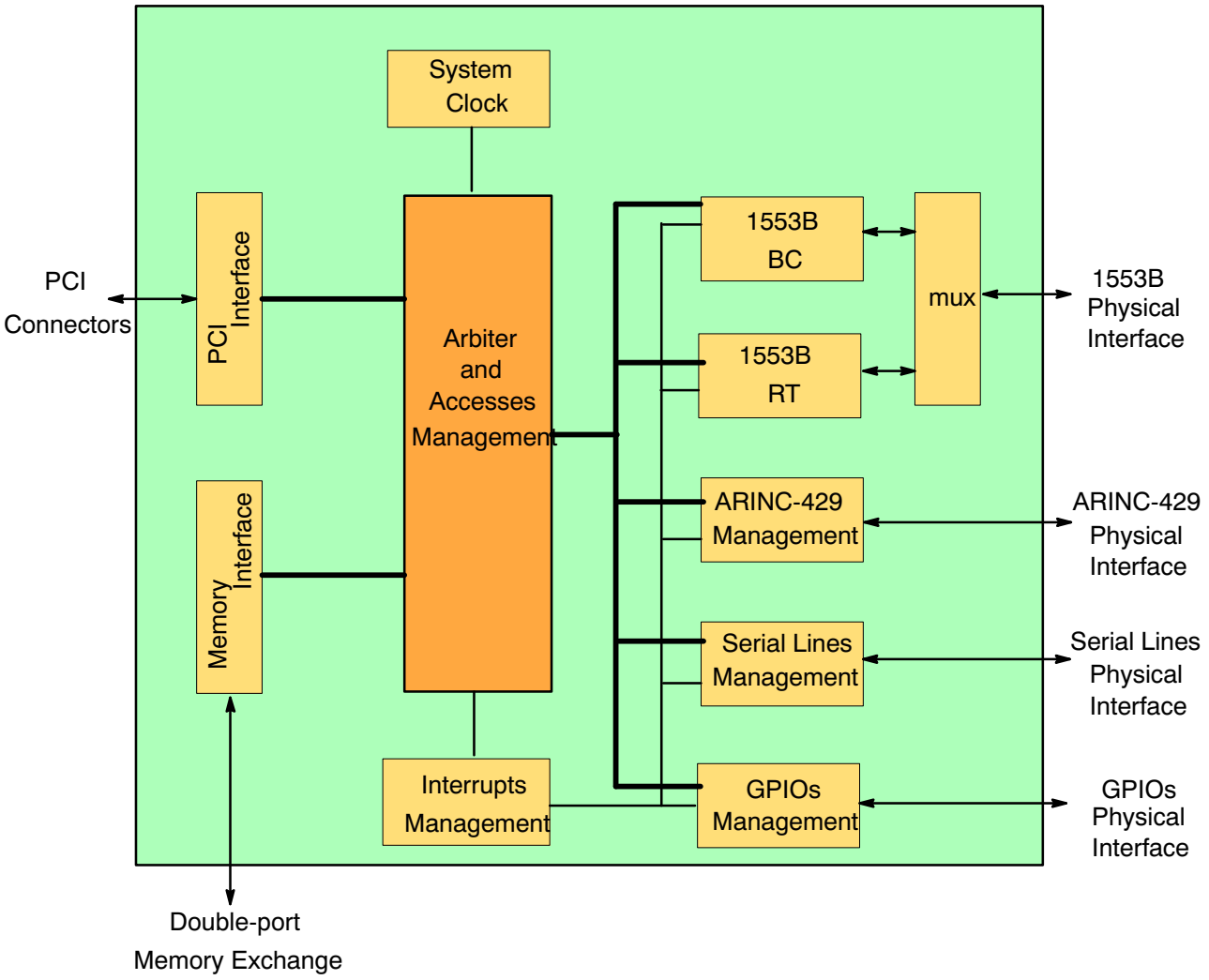

Figure 9: FPGA Block Diagram

3.1.1 PCI Interface

Main characteristics of the PCI interface:

- 32-bit, 33 MHz
- slave interface
- 8, 16 and 32-bit memory accesses
- interrupts managed through one line
- synchronous with the PCI clock

PCI configuration space:

Space Byte Offset	Register Name Bit 31-24	Register Name Bit 23-16	Register Name Bit 15-8	Register Name Bit 7-8
0x00	Vendor ID = 0x0200		Device ID = 0x1269	
0x04	Status		Command	
0x08	Class Code			Revision ID
0x0C	BIST	Header Type	Latency Timer	Cache Line Size
0x10	Base Address Register 0			
0x14	Base Address Register 1			
0x18	Base Address Register 2			
0x1C	Base Address Register 3			
0x20	Base Address Register 4			
0x24	Base Address Register 5			
0x28	CardBus CIS Pointer			
0x2C	Subsystem ID		Subsystem Vendor ID	
0x30	Expansion Rom Base Address Register			
0x34	Reserved			
0x38	Reserved			
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line

Table 4: PCI Configuration Space

- The `Base Address Register 0` (`BAR0`) contains, after programming, the base address of the exchange memory. This memory type is *memory* on the PCI bus.
- The `Base Address Register 1` (`BAR1`) contains, after programming, the base address of the configuration and management registers of the FPGA functionalities. This registers type is *I/O* on the PCI bus.

3.1.2 PCI Memory Space

The 512 KB memory space (BAR0) is organized as follow:

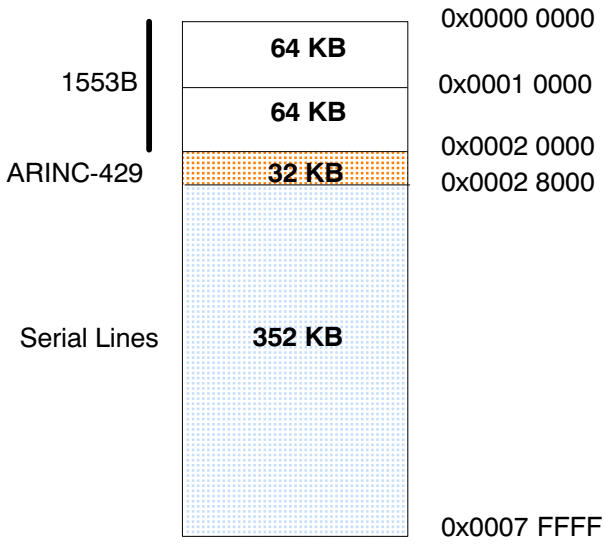

Figure 10: PCI Memory Space Mapping

3.1.3 PCI I/O Space

The I/O space (BAR1) contains 64 KB of registers organized as follow:

Address	Description	Access	
0x00	FPGA Release	16-bit	R
	Reserved		
0x04	PMC Reset (see also 3.1.11)	16-bit	W
	Reserved		
0x10	Watchdog Configuration (see also 3.1.10.2)	16-bit	R/W
0x12	Watchdog GPIO Output (see also 3.1.10.3)	16-bit	R/W
0x14	Watchdog Refresh (see also 3.1.10.1)	16-bit	R/W
	Reserved		
0x20	Interrupt Configuration (sse also 3.1.9.1)	16-bit	R/W
	Reserved		
0x24	Interrupt Identification 1 (see also 3.1.9.2)	16-bit	R/W
0x26	Interrupt Identification 2 (see also 3.1.9.2)	16-bit	R/W
0x28	Interrupt Identification 3 (see also 3.1.9.2)	16-bit	R/W
0x2A	Interrupt Identification 4 (see also 3.1.9.2)	16-bit	R/W
	Reserved		
0x30	Maintanance Time Counter (10 µs) (see also 3.1.8)	32-bit	R/W
	Reserved		
0x40	CONF_1553 (see also 3.1.4.2)	16-bit	R/W
0x42	CSRCOM (1553 BC/RT)	16-bit	W
0x44	CSCONT (1553 BC/RT)	16-bit	W
0x46	CSPP (1553 BC/RT)	16-bit	W
	Reserved		
0x60	ARINC Configuration - Transmit Channel 1 (see also 3.1.5.2)	16-bit	R/W
0x62	ARINC Configuration - Transmit Channel 2 (see also 3.1.5.2)	16-bit	R/W
0x64	ARINC Configuration - Receive Channel 1 (see also 3.1.5.3)	16-bit	R/W
0x66	ARINC Configuration - Receive Channel 2 (see also 3.1.5.3)	16-bit	R/W
0x68	ARINC Configuration - Receive Channel 3 (see also 3.1.5.3)	16-bit	R/W
0x6A	ARINC Configuration - Receive Channel 4 (see also 3.1.5.3)	16-bit	R/W
0x6C	ARINC Status - Transmit Channel 1 (see also 3.1.5.4)	16-bit	R/W
0x6E	ARINC Status - Transmit Channel 2 (see also 3.1.5.4)	16-bit	R/W
0x70	ARINC Status - Receive Channel 1 (see also 3.1.5.5)	16-bit	R
0x72	ARINC Status - Receive Channel 2 (see also 3.1.5.5)	16-bit	R
0x74	ARINC Status - Receive Channel 3 (see also 3.1.5.5)	16-bit	R
0x76	ARINC Status - Receive Channel 4 (see also 3.1.5.5)	16-bit	R
	Reserved		
0x84	Configuration UART 1 (see also 3.1.6.3)	16-bit	R/W
0x86	Configuration UART 2 (see also 3.1.6.3)	16-bit	R/W
0x88	Configuration UART 3 (see also 3.1.6.3)	16-bit	R/W
0x8A	Configuration UART 4 (see also 3.1.6.3)	16-bit	R/W
0x8C	Configuration UART 5 (see also 3.1.6.3)	16-bit	R/W
0x8E	Configuration UART 6 (see also 3.1.6.3)	16-bit	R/W
0x90	Configuration HDLC 1 (see also 3.1.6.8)	16-bit	R/W
0x92	Configuration HDLC 2 (see also 3.1.6.8)	16-bit	R/W
0x94	Configuration HDLC 3 (see also 3.1.6.8)	16-bit	R/W
0x96	Select Line UART 1 (see also 3.1.6.4)	16-bit	R/W
0x98	Select Line UART 2 (see also 3.1.6.4)	16-bit	R/W
0x9A	Select Line UART 3 (see also 3.1.6.4)	16-bit	R/W
0x9C	Select Line UART 4 (see also 3.1.6.4)	16-bit	R/W
0x9E	Select Line UART 5 (see also 3.1.6.4)	16-bit	R/W
0xA0	Select Line UART 6 (see also 3.1.6.4)	16-bit	R/W
0xA2	Select Line HDLC 1 (see also 3.1.6.9)	16-bit	R/W
0xA4	Select Line HDLC 2 (see also 3.1.6.9)	16-bit	R/W

Address	Description	Access	
0xA6	Select Line HDLC 3 (see also 3.1.6.9)	16-bit	R/W
	Reserved		
0xB0	GPIO Configuration Low (see also 3.1.7.1)	16-bit	R/W
0xB2	GPIO Configuration Hi (see also 3.1.7.2)	16-bit	R/W
0xB4	GPIO Status In (see also 3.1.7.3)	16-bit	R/W
0xB6	GPIO Status Out (see also 3.1.7.4)	16-bit	R/W

Table 5: I/O Space Mapping

These registers are used to:

- access the common resources (real time clock, interrupts)
- control the various modules (1553B, ARINC-429 and Serial Lines)
- drive the PMC (software reset, watchdog)
- drive the GPIO

Each register is fully described in related section:

- 1553B Management, refer to section 3.1.4 page 16
- ARINC-429 Management, refer to section 3.1.5 page 17
- Serial Lines Management, refer to section 3.1.6 page 22
- GPIO Management, refer to section 3.1.7 page 33
- Real Time Clock Management, refer to section 3.1.8 page 34
- Interrupt Management, refer to section 3.1.9 page 34
- Watchdog Management, refer to section 3.1.10 page 36
- Reset Management, refer to section 3.1.11 page 36

3.1.4 1553B Management

3.1.4.1 1553B Main Characteristics

» Mode

The FPGA includes a BC (Bus Controller) and a RT (Remote Terminal) modules. Their usage is exclusive. These modules use the same FPGA input/output.

3.1.4.2 CONF_1553 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	enable_rx	enable_tx	enable_rt	enable_bc

> `enable_bc` `bit 0` 1 ⇒ BC mode activated however the value of `enable_rt`

> `enable_rt` `bit 1` 1 ⇒ RT mode activated if `enable_bc` is set to **0**

> `enable_tx` `bit 2` **0** ⇒ 1553 Transmitters disabled
1 ⇒ 1553 Transmitters enabled

> `enable_rx` `bit 3` **0** ⇒ 1553 Receivers disabled
1 ⇒ 1553 Receivers enabled

3.1.5 ARINC-429 Management

3.1.5.1 ARINC-429 Main Characteristics

» Capacity

The FPGA manages up to 2 transmit channels and 4 receive channels.

» Speed

Each of the six ARINC-429 channels works independently at 12.5 kHz (low speed) or 100 kHz (high speed).

On the transmit side, the choice is made by programming.

On the receive side, the automaton synchronizes on the received modulation.

» Dating

The FPGA includes a datation function of the receive messages. The datation is made using the `Time Hour` register.

3.1.5.2 ARINC Configuration - Transmit Channel i Registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	bit_rate	par_enable	chan_enable

> `chan_enable` `bit 0` 1 ⇒ associated ARINC channel enabled
0 ⇒ associated ARINC channel disabled (no transmission)

> `par_enable` `bit 1` 1 ⇒ activate the computing of the parity bit in the ARINC word transmitted
0 ⇒ the parity bit in the ARINC word is set up by software

> `bit_rate` `bit 2` 0 ⇒ 12.5 kHz
1 ⇒ 100 kHz

3.1.5.3 ARINC Configuration - Receive Channel i Registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	par_enable	chan_enable

> `chan_enable` `bit 0` 1 ⇒ associated ARINC channel enabled
0 ⇒ associated ARINC channel disabled (no reception)

> `par_enable` `bit 1` 1 ⇒ activate the checking of the parity bit in the ARINC word received
0 ⇒ no parity bit checking in the ARINC word received

3.1.5.4 ARINC Status - Transmit Channel i Registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	fifo_empty	fifo_full

- `fifo_full` `bit 0` 1 ⇒ FIFO full
- `fifo_empty` `bit 1` 1 ⇒ FIFO empty

3.1.5.5 ARINC Status - Receive Channel i Registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	receive_bit	timeout_err	bit_decode_err	bit_rate	parity_bit

- `parity_bit` `bit 0` value of the parity bit computed by the FPGA
- `bit_rate` `bit 1` 0 ⇒ 100 kHz
  1 ⇒ 12.5 KHz
- `bit_decode_err` `bit 2`
  1 ⇒ overshoot in the number of received bits
- `timeout_err` `bit 3` 1 ⇒ number of bits insufficient to constitue the word
- `receive_bit` `bit 4` 1 ⇒ reception in progress

3.1.5.6 ARINC Mapping

Address	Description		Access
0x00	FIFO status channel Tx1 (flag FIF0 full)		32-bit
0x04	**Transmit Parameter - channel Tx1**		32-bit
0x08	Transmit FIFO channel Tx1	Data word	32-bit
0x0c	Label 0 channel Tx1	Reserved	32-bit
0x10		Label count	32-bit
0x14		Time tag	32-bit
0x1C		Data word	32-bit
...			
0x0FF8	Label 255 channel Tx1	Reserved	32-bit
0x0FFC		Label count	32-bit
0x1000		Time tag	32-bit
0x1004		Data word	32-bit
0x100C	FIFO status channel Tx2 (flag FIF0 full)		32-bit
...	**Transmit Parameter - channel Tx2**		32-bit
...	Transmit FIFO channel Tx2	Data word	32-bit
...	Label 0 channel Tx2	Reserved	32-bit
...		Label count	32-bit
...		Time tag	32-bit
...		Data word	32-bit
...			
...	Label 255 channel Tx2	Reserved	32-bit
...		Label count	32-bit
...		Time tag	32-bit
0x2014		Data word	32-bit
0x2018	**Current pointer receive buffer - channel Rx1**		32-bit
0x201C	Receive Circular Buffer channel Rx1	Block 0 - Time Tag	32-bit
0x2024		Block 0 - Data Word	32-bit
0x202C		**Block 0 - Data Transmission Status**	32-bit
...			
	Receive Circular Buffer channel Rx1	Block 15 - Time Tag	32-bit
		Block 15 - Data Word	32-bit
0x20DA		**Block 15 - Data Transmission Status**	32-bit
0x20DC	Label 0 channel Rx1	**Control / Transmission word (see also 3.1.5.7)**	32-bit
...		Label count	32-bit
...		Time tag	32-bit
...		Data word	32-bit
...			
...	Label 255 channel Rx1	**Control / Transmission word (see also 3.1.5.7)**	32-bit
...		Label count	32-bit
...		Time tag	32-bit
0x30DA		Data word	32-bit
...			
0x5264	**Current pointer receive buffer - channel Rx4**		32-bit
...	Receive Circular Buffer channel Rx4	Block 0 - Time Tag	32-bit
...		Block 0 - Data Word	32-bit
...		**Block 0 - Data Transmission Status**	32-bit
...			
...	Receive Circular Buffer channel Rx4	Block 15 - Time Tag	32-bit
...		Block 15 - Data Word	32-bit
...		**Block 15 - Data Transmission Status**	32-bit

Address	Description		Access
...	Label 0 channel Rx4	Control / Transmission word (see also 3.1.5.7)	32-bit
...		Label count	32-bit
...		Time tag	32-bit
...		Data word	32-bit
...			
...	Label 255 channel Rx4	Control / Transmission word (see also 3.1.5.7)	32-bit
...		Label count	32-bit
...		Time tag	32-bit
0x6326		Data word	32-bit

Transmit Parameter - channel Txi

Hole between two labels, in number of bits.

Current pointer receive buffer - channel Rxi

Current hardware index in the receive circular buffer (block index 0 to 15)

» Data Transmission Status - channel Rxi

31	6	5	4	3	2	1	0
0		data_ready	receive_bit	timeout_err	bit_count_err	bit_rate	parity_err

- `parity_err` bit 0 — 1 ⇒ parity error detected
- `bit_rate` bit 1 — 1 ⇒ 100 kHz; 0 ⇒ 12.5 KHz
- `bit_count_err` bit 2 — 1 ⇒ overshoot in the number of received bits
- `timeout_err` bit 3 — 1 ⇒ number of bits insufficient to make the word
- `receive_bit` bit 4 — 1 ⇒ reception in progress
- `data_ready` bit 5 — 1 ⇒ word ready to be used by the software

3.1.5.7 ARINC Filtering

The FPGA include a function of labels filtering.

The Look-Up-Table allows the labels filtering and the programming of an interruption for each label using the `Control Transmission word`.

» Control / Transmission - channel Rxi

31	19	17	16	15	5	4	3	2	1	0
0		filtering_en	interrupt_en	0		receive_bit	timeout_err	bit_count_err	bit_rate	parity_err

- `parity_err` bit 0 — 1 ⇒ parity error detected
- `bit_rate` bit 1 — 1 ⇒ 100 kHz; 0 ⇒ 12.5 kHz
- `bit_count_err` bit 2 — 1 ⇒ overshoot in the number of received bits
- `timeout_err` bit 3 — 1 ⇒ number of bits insufficient to make the word
- `receive_bit` bit 4 — 1 ⇒ reception in progress
- `data_ready` bit 5 — 1 ⇒ word ready to be used by the software
- `interrupt_en` bit 16 — 1 ⇒ generate an interruption for this label, when inserted in the receive queue
- `filtering_en` bit 17 — 1 ⇒ activate the filtering for this label

3.1.6 Serial Lines Management

3.1.6.1 Serial Lines Main Characteristics

Capacity

The FPGA manages up to 6 transmit lines and 6 receive lines.

The available programmable modes are:

- `Modem Mode`: 3 transmit lines
6 receive lines
V24 functional interface + one asynchronous link TxD/RxD
- `Full-duplex Synchronous Mode`: up to 3 links
- `Full-duplex Asynchronous Mode:` up to 6 links

Full-duplex Synchronous and Full-duplex Asynchronous modes can be mixed.

Electrical Interface

The FPGA provides the command signals needed to configure the electrical interface of the transmitters/receivers of the PMC-6L:

- `V10` (electrical EIA-423)
- `V11` (electrical EIA-485)
- `V28` (electrical EIA-232)

Speed

The speed is programmable with a maximum of:

- 115 kbauds for the asynchronous modes
- 2 Mb/s for the synchronous mode

Protocol

For the asynchronous mode, the data encapsulation is `UART character type`.

For the synchronous mode, transmission are made according to the `HDLC protocol.`

Dating

The FPGA includes a datation function of the receive frames on each active serial links. The datation is made using the `Time Hour` register.

3.1.6.2 Serial Mapping

Address	Description		Access	
0x00	Reserved		8-bit	R/W
0x01	Reserved		8-bit	R/W
0x02	Reserved		8-bit	R/W
0x03	Line Control		8-bit	R/W
0x04	Modem Control		8-bit	R/W
0x05	Line Status		8-bit	R/W
0x06	Modem Status		8-bit	R/W
0x07	Reserved		8-bit	R/W
0x08	Divisor Latch (Hi)		8-bit	R/W
0x09	Divisor Latch (Lo)		8-bit	R/W
0x0A	Reserved		8-bit	R/W
0x0B	Reserved		8-bit	R/W
Reserved				
0x0020	Receive Buffer Descriptor	Rx Buffer Size (see also 3.1.6.6)	16-bit	R/W
0x0022		Rx It Param (see also 3.1.6.6)	16-bit	R/W
0x0024		Rx Data Pointer (see also 3.1.6.6)	32-bit	R/W
Reserved				
0x01A0	Transmit Buffer Descriptor (Tx BD) 0	Tx Status (see also 3.1.6.7)	16-bit	R/W
0x01A2		Tx Data Length (see also 3.1.6.7)	16-bit	R/W
0x01A4		Tx Time Tag (see also 3.1.6.7)	32-bit	R/W
0x01A8		Tx Data Pointer (see also 3.1.6.7)	32-bit	R/W
...				
0x0314	Transmit Buffer Descriptor (Tx BD) 31	Tx Status (see also 3.1.6.7)	16-bit	R/W
0x0316		Tx Data Length (see also 3.1.6.7)	16-bit	R/W
0x0318		Tx Time Tag (see also 3.1.6.7)	32-bit	R/W
0x031C		Tx Data Pointer (see also 3.1.6.7)	32-bit	R/W
0x0320	Asynchronous Serial Line 2 Automaton (idem 1)			
0x0640	Asynchronous Serial Line 3 Automaton (idem 1)			
0x0960	Asynchronous Serial Line 4 Automaton (idem 1)			
0x0C80	Asynchronous Serial Line 5 Automaton (idem 1)			
0x0FA0	Asynchronous Serial Line 6 Automaton (idem 1)			
0x12C0	HDLC Bit Rate (see also 3.1.6.10)		16-bit	R/W
0x12C2	HDLC Mode (see also 3.1.6.11)		16-bit	R/W
0x12C4	HDLC Frame Length		16-bit	R/W
0x12C6	Station Address (see also 3.1.6.11)		16-bit	R/W
Reserved				
0x12D0	Receive Buffer Descriptor (Rx BD) 0	Rx Status (see also 3.1.6.12)	16-bit	R/W
0x12D2		Rx Data Length (see also 3.1.6.12)	16-bit	R/W
0x12D4		Rx Time Tag (see also 3.1.6.12)	32-bit	R/W
0x12D8		Rx Data Pointer (see also 3.1.6.12)	32-bit	R/W
...				
...	Receive Buffer Descriptor (Rx BD) 31	Rx Status (see also 3.1.6.12)	16-bit	R/W
...		Rx Data Length (see also 3.1.6.12)	16-bit	R/W
...		Rx Time Tag (see also 3.1.6.12)	32-bit	R/W
...		Rx Data Pointer (see also 3.1.6.12)	32-bit	R/W
...	Transmit Buffer Descriptor (Tx BD) 0	Tx Status (see also 3.1.6.13)	16-bit	R/W
...		Tx Data Length (see also 3.1.6.13)	16-bit	R/W
...		Tx Time Tag (see also 3.1.6.13)	32-bit	R/W
...		Tx Data Pointer (see also 3.1.6.13)	32-bit	R/W

Address	Description		Access	
...				
...	Transmit Buffer Descriptor (Tx BD) 31	Tx Status (see also 3.1.6.13)	16-bit	R/W
...		Tx Data Length (see also 3.1.6.13)	16-bit	R/W
...		Tx Time Tag (see also 3.1.6.13)	32-bit	R/W
0x15CC		Tx Data Pointer (see also 3.1.6.13)	32-bit	R/W
0x15D0	HDLC 2 Automaton (idem 1)			
0x18E0	HDLC 3 Automaton (idem 1)			
0x1BF0 0x57FFF	Memory (shared between the data buffers of the serial lines used)			

3.1.6.3 UART Configuration Register

Each line in UART mode is configurable via the **Configuration UART *i*** register.

» Configuration UART *i*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
modem	0	0	0	0	0	0	0	0	valid_tx	valid_rx	0	0	interface2	interface1	chan_enable

> `chan_enable` `bit 0` 1 ⇒ Channel (Automaton and lines) Activated (Tx+Rx)
0 ⇒ Channel (Automaton and lines) Desactivated (Tx+Rx) (high impedance)

> `interface2/1` `bit 2/1` 00 ⇒ EIA-232
01 ⇒ EIA-423
10 ⇒ EIA-485
11 ⇒ Reserved

> `valid_rx` `bit 5` 1 ⇒ Data Reception Enabled
0 ⇒ Data Reception Disabled (high impedance)

> `valid_tx` `bit 6` 1 ⇒ Data Transmission Enabled
0 ⇒ Data Transmission Disabled (high impedance)

> `modem` `bit 15` 1 ⇒ Activation of the V24 Modem mode. This bit is significant only for UART 1 automaton. In that configuration, only the UART 2 automaton can be used in addition to the UART 1 automaton.

3.1.6.4 UART Selection Register

The configuration of the transmitter and receiver for the 6 UART channels is achieved using the **Select Line UART *i*** register.

» Default Configuration

UART n°	1	2	3	4	5	6
TxD on transmitter n°	1	2	3	4	5	6
RxD on receiver n°	1	2	3	4	5	6

» Select Line UART *i*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	RxD				TxD			

> `TxD Quartet bit 0-3` 0000 ⇒ Default Configuration
> 0001 ⇒ TxD output of UART *i* channel is directed on transmitter 1
> 0010 ⇒ TxD output of UART *i* channel is directed on transmitter 2
> 0011 ⇒ TxD output of UART *i* channel is directed on transmitter 3
> 0100 ⇒ TxD output of UART *i* channel is directed on transmitter 4
> 0101 ⇒ TxD output of UART *i* channel is directed on transmitter 5
> 0110 ⇒ TxD output of UART *i* channel is directed on transmitter 6
> 0111 ⇒ Default Configuration
> 1000 ⇒ Default Configuration

> `RxD Quartet bit 4-7` 0000 ⇒ Default Configuration
> 0001 ⇒ RxD input of UART *i* channel is directed on receiver 1
> 0010 ⇒ RxD input of UART *i* channel is directed on receiver 2
> 0011 ⇒ RxD input of UART *i* channel is directed on receiver 3
> 0100 ⇒ RxD input of UART *i* channel is directed on receiver 4
> 0101 ⇒ RxD input of UART *i* channel is directed on receiver 5
> 0110 ⇒ RxD input of UART *i* channel is directed on receiver 6
> 0111 ⇒ Default Configuration
> 1000 ⇒ Default Configuration

> Reset default value: **0000**

> The re-assignment of the UART channels can be done only if they are programmed with the same electrical interface.

3.1.6.5 UART Interruptions Management

In UART mode, the interruptions are managed when switching buffers, not at each character reception.

3.1.6.6 UART Reception Management

The `Receive Buffer Descriptor` area allows to access a single data reception buffer.

- `Rx Data Pointer` pointer to a circular buffer used to store the received characters.
- `Rx Buffer Size` size (in bytes) of the circular buffer, multiple of 8
- `Rx It Param`

15		8	7		0
timeout_it			nb_char_it		

  - `nb_char_it` `bit 0-7` an interruption is generated every `nb_char_it` characters.
    0⇒ function desactivated.
  - `timeoutit` `bit 8-15` an interruption is generated every `timeout_it` milli-seconds.
    0⇒ function desactivated.

3.1.6.7 UART Transmit Management

A `Transmit Buffer Descriptor (Tx BD)` table allows to describe each buffer. This table is managed like a circular FIFO.

- `Tx Status`

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	preamble_size				interr	wrap	ready

  - `ready` `bit 0` initalized by the software and updated by the hardware
    0⇒ the buffer associated to the `Tx BD` is not ready to be transmitted.
    1⇒ the transmission of the buffer is in progress. The fields of the `Transmit Buffer Descriptor` and the data buffer must be accessed only by the serial automaton.
  - `wrap` `bit 1` initalized by the software
    1⇒ Last `Tx BD` of the table
  - `interr` `bit 2` initalized by the software
    0⇒ no interrupt
    1⇒ interrupt generated when the buffer has been completely transmitted
  - `preamble_size` `bit 3-6` initalized by the software
    0 ⇒ No preamble transmitted
    N characters '1' (all ones) are sent before sending the data of the buffer, so that the receiver detects the idle characters.
- `Tx Data Length` initalized by the software
  Number of bytes to transmit.
- `Tx Time Tag` updated by the hardware
  Transmit date of the data buffer
- `Tx Data Pointer` initalized by the software
  pointer on the first byte of the data buffer

3.1.6.8 HDLC Configuration Register

Each line in HDLC mode is configurable via the **Configuration HDLC *i*** register.

» Configuration HDLC *i*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	clk_edge	valid_tx	valid_rx	reset	0	interface2	interface1	chan_enable

> `chan_enable` `bit 0` 1 ⇒ Channel activated (Tx+Rx)
0 ⇒ Channel desactivated (Tx+Rx) (high impedance)

> `interface2/1` `bit 2/1` 00 ⇒ EIA-232
01 ⇒ EIA-423
10 ⇒ EIA-485
11 ⇒ Reserved

> `reset` `bit 4` 1 ⇒ re-initialize the serial line automaton (high impedance)

> `valid_rx` `bit 5` 1 ⇒ Data reception enabled
0 ⇒ Data reception disabled (high impedance)

> `valid_tx` `bit 6` 1 ⇒ Data transmission enabled
0 ⇒ Data transmission disabled (high impedance)

> `clk_edge` `bit 7` 1 ⇒ Select the ascending clock edge to sample the data
0 ⇒ Select the descending clock edge to sample the data

3.1.6.9 HDLC Selection Register

The configuration of the transmitter and receiver for the 3 HDLC channels is achieved using the **Select Line HDLC *i*** register.

» Default Configuration

HDLC n°	1	2	3
TxD on transmitter n°	1	3	5
RxD on receiver n°	1	3	5
TxClk on transmitter n°	2	4	6
RxClk on receiver n°	2	4	6

» Select Line HDLC *i*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RxClk				TxClk				RxD				TxD			

> `TxD Quartet bit 0-3` 0000 ⇒ Default Configuration
0001 ⇒ TxD output of HDLC *i* channel is directed on transmitter 1
0010 ⇒ TxD output of HDLC *i* channel is directed on transmitter 2
0011 ⇒ TxD output of HDLC *i* channel is directed on transmitter 3
0100 ⇒ TxD output of HDLC *i* channel is directed on transmitter 4
0101 ⇒ TxD output of HDLC *i* channel is directed on transmitter 5
0110 ⇒ TxD output of HDLC *i* channel is directed on transmitter 6
0111 ⇒ Default Configuration
1000 ⇒ Default Configuration

> `RxD Quartet bit 4-7` 0000 ⇒ Default Configuration
0001 ⇒ RxD input of HDLC *i* channel is directed on receiver 1
0010 ⇒ RxD input of HDLC *i* channel is directed on receiver 2
0011 ⇒ RxD input of HDLC *i* channel is directed on receiver 3
0100 ⇒ RxD input of HDLC *i* channel is directed on receiver 4
0101 ⇒ RxD input of HDLC *i* channel is directed on receiver 5
0110 ⇒ RxD input of HDLC *i* channel is directed on receiver 6
0111 ⇒ Default Configuration
1000 ⇒ Default Configuration

> `TxClk Quartet bit 8-11` 0000 ⇒ Default Configuration
0001 ⇒ TxClk output of HDLC *i* channel is directed on transmitter 1
0010 ⇒ TxClk output of HDLC *i* channel is directed on transmitter 2
0011 ⇒ TxClk output of HDLC *i* channel is directed on transmitter 3
0100 ⇒ TxClk output of HDLC *i* channel is directed on transmitter 4
0101 ⇒ TxClk output of HDLC *i* channel is directed on transmitter 5
0110 ⇒ TxClk output of HDLC *i* channel is directed on transmitter 6
0111 ⇒ Default Configuration
1000 ⇒ Default Configuration

> `RxClk Quartet bit 12-15` 0000 ⇒ Default Configuration
0001 ⇒ RxClk input of HDLC *i* channel is directed on receiver 1
0010 ⇒ RxClk input of HDLC *i* channel is directed on receiver 2
0011 ⇒ RxClk input of HDLC *i* channel is directed on receiver 3
0100 ⇒ RxClk input of HDLC *i* channel is directed on receiver 4
0101 ⇒ RxClk input of HDLC *i* channel is directed on receiver 5
0110 ⇒ RxClk input of HDLC *i* channel is directed on receiver 6
0111 ⇒ Default Configuration
1000 ⇒ Default Configuration

> Reset default value: **0000**

> The re-assignment of the HDLC channels can be done only if they are programmed with the same electrical interface.

3.1.6.10 HDLC Bit Rate

The field `HDLC Bit Rate` is used to program the transmit bit rate using following formula:

```
HDLC Bit Rate = (20000000 / transmit_bit_rate_bps) - 1
```

with `transmit_bit_rate_bps` = transmit bit rate in bits per seconds

3.1.6.11 HDLC Mode

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	number of flags				crc_selection	addr filtering

- `addr_filtering bit 0` initalized by the software
  1 ⇒ Address filtering enabled. If the `Address` field of the entering frames is not equal to the filed `Station address`, the frames are lost.
  0 ⇒ Address filtering disabled.
- `crc_selection bit 1` initalized by the software
  1 ⇒ CRC 32 bits
  0 ⇒ CRC 16 bits
- `number of flags bit 2-5` initalized by the software
  Minimal number of flags between two frames or the beginning of a frame.

3.1.6.12 HDLC Reception Management

The `Receive Buffer Descriptor` (Rx BD i) area allows to access a single data reception buffer.

> `Rx Status`

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	frame_len_viol	byte_error	frame_abort	frame_error	fcs_error	data_ready	interrupt	wrap	empty

- `empty` `bit 0` initialized by the software and updated by the hardware
  0⇒ the buffer contains valid data or the received process has been stopped following a transmission error. The serial automaton will not used this descriptor until the bit `empty` remains to 1
  1⇒ the buffer is empty or the the received process is in progress. The fields of the `Receive Buffer Descriptor` and the data buffer must be accessed only by the serial automaton.
- `wrap` `bit 1` initialized by the software
  1⇒ last Rx BD of the table
- `interrupt` `bit 2` initialized by the software
  0⇒ no interruption
  1⇒ an interruption is generated once the buffer is full
- `data_ready` `bit 3` initialized by the hardware
  1⇒ data buffer available
- `fcs_error` `bit 4` initialized by the hardware
  1⇒ CRC error
- `frame_error` `bit 5` initialized by the hardware
  1⇒ received frame length < 32 bits
- `frame_abort` `bit 6` initialized by the hardware
  1⇒ 8 consecutive bits to 1 in a frame
- `byte_error` `bit 7` initialized by the hardware
  1⇒ received frame with a number of bits not multiple of 8
- `frame_len_viol` `bit 8` initialized by the hardware
  1⇒ received frame is longer than the maximum buffer size

> `Rx Data Length` updated by the hardware
number of bytes written by the serial automaton

> `Rx Time Tag` updated by the hardware
reception date of the data buffer

> `Rx Data Pointer` updated by the software
pointer on the first byte of the data buffer; offset from the beginning of the memory area dedicated to the serial lines

3.1.6.13 HDLC Transmit Management

The `Transmit Buffer Descriptor` (Tx BD i) area allows to access a single data transmit buffer.

- `Tx Status`

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	underrun	interrupt	wrap	ready

  - `ready` `bit 0` initialized by the software and updated by the hardware
    0⇒ the buffer associated to the `Tx BD` is not ready to be transmitted.
    1⇒ the transmission of the buffer is in progress. The fields of the `Transmit Buffer Descriptor` and the data buffer must be accessed only by the serial automaton.
  - `wrap` `bit 1` initialized by the software
    1⇒ last `Tx BD` of the table
  - `interrupt` `bit 2` initialized by the software
    0⇒ no interruption
    1⇒ an interruption is generated once the buffer has been transmitted
  - `underrun` `bit 3` initialized by the hardware
    1⇒ error during the transmission
- `Tx Data Length` updated by the hardware
  number of bytes to be transmitted by the serial automaton
- `Tx Time Tag` updated by the hardware
  transmission date of the data buffer
- `Tx Data Pointer` updated by the software
  pointer on the first byte of the data buffer.

3.1.6.14 Modem Function

The Modem mode uses a `V24 isochrone` transmission mode (UART characters on a synchronous line). This mode uses two UART uatomations;

- one for the signals of the V24 line
- one for the line `Serial/Control (TxD/RxD)`

3.1.7 GPIO

The FPGA manages up to 16 GPIO. Each GPIO is software configurable in Input or Output mode, with transmission of programmable interruptions.

3.1.7.1 GPIO Configuration Low

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO 09 it	GPIO 08 I/O	GPIO 07 it	GPIO 07 I/O	GPIO 06 it	GPIO 06 I/O	GPIO 05 it	GPIO 05 I/O	GPIO 04 it	GPIO 04 I/O	GPIO 03 it	GPIO 03 I/O	GPIO 02 it	GPIO 02 I/O	GPIO 01 it	GPIO 01 I/O

> `GPIO xx I/O` 1 ⇒ Output GPIO
0 ⇒ Input GPIO

> `GPIO xx it` 1 ⇒ An interruption is generated in case of changing state of the GPIO.

3.1.7.2 GPIO Configuration Hi

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO 16 it	GPIO 16 I/O	GPIO 15 it	GPIO 15 I/O	GPIO 14 it	GPIO 14 I/O	GPIO 13 it	GPIO 13 I/O	GPIO 12 it	GPIO 12 I/O	GPIO 11 it	GPIO 11 I/O	GPIO 10 it	GPIO 10 I/O	GPIO 09 it	GPIO 09 I/O

> `GPIO xx I/O` 1 ⇒ Output GPIO
0 ⇒ Input GPIO

> `GPIO xx it` 1 ⇒ An interruption is generated in case of changing state of the GPIO.

3.1.7.3 GPIO Status In

Read only register. If a GPIO is configured as an Ouput GPIO, the associated bit is not applicable.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO 16 state	GPIO 15 state	GPIO 14 state	GPIO 13 state	GPIO 12 state	GPIO 11 state	GPIO 10 state	GPIO 09 state	GPIO 08 state	GPIO 07 state	GPIO 06 state	GPIO 05 state	GPIO 04 state	GPIO 03 state	GPIO 02 state	GPIO 01 state

> `GPIO xx state` `Input GPIO State` 1 ⇒ +5V
0 ⇒ 0V

3.1.7.4 GPIO Status Out

Read Write register. If a GPIO is configured as an Input GPIO, the associated bit is not applicable.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO 16 state	GPIO 15 state	GPIO 14 state	GPIO 13 state	GPIO 12 state	GPIO 11 state	GPIO 10 state	GPIO 09 state	GPIO 08 state	GPIO 07 state	GPIO 06 state	GPIO 05 state	GPIO 04 state	GPIO 03 state	GPIO 02 state	GPIO 01 state

> `GPIO xx state` `Output GPIO State` 1 ⇒ high state
0 ⇒ low state

3.1.8 Real Time Clock Management

The FPGA includes a real time clock made up of a 32-bit counter. This `Time Hour` counter is continuously incremented with a 10 µs quantum.

3.1.9 Interrupts Management

3.1.9.1 Interrupt Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	enable_it

> `enable_it` 1 ⇒ interruptions are sent on the PCI bus

3.1.9.2 Interrupt Identification Registers

The Interrupt Identification registers allow to identify the origin of the interruptions:

- Interrupt Identification 1: 1553B
- Interrupt Identification 1: ARINC-429
- Interrupt Identification 2: UART Serial Lines
- Interrupt Identification 3: HDLC Serial Lines
- Interrupt Identification 4: GPIO

Interrupt Identification 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	it ARINC chan. Rx4	it ARINC chan. Rx3	it ARINC chan. Rx2	it ARINC chan. Rx1	it ARINC chan. Tx2	it ARINC chan. Tx1	it 1553B BC	it 1553B RT

Interrupt Identification 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	it UART Tx chan. 6	it UART Rx chan. 6	it UART Tx chan. 5	it UART Rx chan. 5	it UART Tx chan. 4	it UART Rx chan. 4	it UART Tx chan. 3	it UART Rx chan. 3	it UART Tx chan. 2	it UART Rx chan. 2	it UART Tx chan. 1	it UART Rx chan. 1

Interrupt Identification 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	it HDLC Tx chan. 3	it HDLC Rx chan. 3	it HDLC Tx chan. 2	it HDLC Rx chan. 2	it HDLC Tx chan. 1	it HDLC Rx chan. 1

Interrupt Identification 4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
it GPIO chan. 16	it GPIO chan. 15	it GPIO chan. 14	it GPIO chan. 13	it GPIO chan. 12	it GPIO chan. 11	it GPIO chan. 10	it GPIO chan. 09	it GPIO chan. 08	it GPIO chan. 07	it GPIO chan. 06	it GPIO chan. 05	it GPIO chan. 04	it GPIO chan. 03	it GPIO chan. 02	it GPIO chan. 01

3.1.10 Watchdog

3.1.10.1 Watchdog Overview

The FPGA includes a watchdog timer functionality. Two registers are used to implement this functionality:

- the watchdog refresh register
- the watchdog configuration register, see also section 3.1.10.2

The watchdog, when not re-armed by a software wrtite access in the watchdog refresh register, disables all the transmitters, and sets up in high impedance the transmitters of the serial lines and the GPIO.

The watchdog functionality is disabled after the board power-up or after a reset.

3.1.10.2 Watchdog Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
watchdog_en	watchdog_timeout														

- `watchdog_timeout` `bit 0-14` time limit of the watchdog (in milli-seconds)
- `watchdog_en` `bit 15` 0 ⇒ watchdog functionality disabled
1 ⇒ watchdog functionality enabled

3.1.10.3 Watchdog GPIO Output Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO chan. 16	GPIO chan. 15	GPIO chan. 14	GPIO chan. 13	GPIO chan. 12	GPIO chan. 11	GPIO chan. 10	GPIO chan. 09	GPIO chan. 08	GPIO chan. 07	GPIO chan. 06	GPIO chan. 05	GPIO chan. 04	GPIO chan. 03	GPIO chan. 02	GPIO chan. 01

- `GPIO chan. 01-16` 1 ⇒ GPIO used to give the watchdog status.

- Only one GPIO can be activated (low state) by programming this register (the first non-zero bit starting from bit 0 is taken into account to select the GPIO).
- By default, the GPIO watchdog status is high.
- When the watchdog functionality is disabled, all the GPIO are available.

3.1.11 Reset

A software write access to the Reset register lead the FPGA into its rest state:

- all the output to their default value
- all the registers to their default value
- all the automatons in their rest state

Chapter 4 - Connectors

4.1 Front Panel Connectors

4.1.1 Location

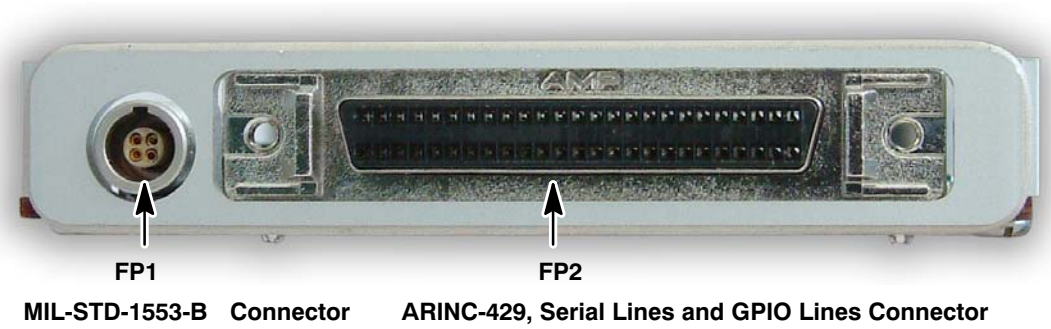

Figure 11: Front Panel Connectors Location

4.1.2 FP1 Connector Pin Assignment

Figure 12: FP1: MIL-STD-1553-B Connector

The Signal Description is available in section 4.4 on page 46.

Pin	Signal Name
1	1553_TXRX_A-
2	1553_TXRX_A+
3	1553_TXRX_B-
4	1553_TXRX_B+

Table 6: FP1 Connector Pin Assignment

4.1.3 FP2 Connector Pin Assignment

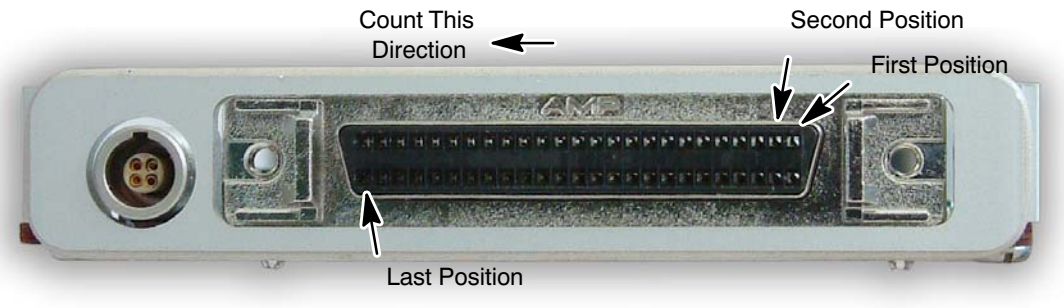

Figure 13: FP2: ARINC-429, Serial Lines and GPIO Lines Connector

The connector pin assigment depends on the Build Option: B-Type, M-Type, H-Type.

- **B-Type Build Option:**
  - ARINC-429 4 Receive and 2 Transmit Channels
  - Serial Lines 4 UART Simple Lines or 2 HDLC Synchronous Full Duplex Lines
  - GPIO Lines 16 Lines
- **M-Type Build Option:**
  - ARINC-429 4 Receive and 2 Transmit Channels
  - Serial Lines 1 Full Modem Line and 1 Single Line
  - GPIO Lines 14 Lines
- **H-Type Build Option:**
  - ARINC-429 4 Receive and 2 Transmit Channels
  - Serial Lines 6 UART Simple Lines or 6 HDLC Synchronous Full Duplex Lines
  - GPIO Lines 8 Lines

The Signal Description is available in section 4.4 on page 46.

Pin	Signal Name		
	B-Type Build Option	M-Type Build Option	H-Type Build Option
29		ARINC429_1_TX+	
27		ARINC429_1_TX-	
28		ARINC429_2_TX+	
26		ARINC429_2_TX-	
5		ARINC429_1_RX+	
6		ARINC429_1_RX-	
7		ARINC429_2_RX+	
8		ARINC429_2_RX-	
1		ARINC429_3_RX+	
2		ARINC429_3_RX-	
3		ARINC429_4_RX+	
4		ARINC429_4_RX-	

Pin	Signal Name		
	B-Type Build Option	M-Type Build Option	H-Type Build Option
24	UART1_TXD- | HDLC1_TXD-	FM_TXD	UART1_TXD- | HDLC1_TXD-
25	UART1_TXD+ | HDLC1_TXD+	-	UART1_TXD+ | HDLC1_TXD+
23	UART2_TXD- | HDLC1_TCK-	FM_RTS	UART2_TXD- | HDLC1_TCK-
48	UART2_TXD+ | HDLC1_TCK+	-	UART2_TXD+ | HDLC1_TCK+
18	UART3_TXD- | HDLC2_TXD-	S1_TXD	UART3_TXD- | HDLC2_TXD-
17	UART3_TXD+ | HDLC2_TXD+	-	UART3_TXD+ | HDLC2_TXD+
15	UART4_TXD- | HDLC2_TCK-	GPIO[11]	UART4_TXD- | HDLC2_TCK-
16	UART4_TXD+ | HDLC2_TCK+	GPIO[12]	UART4_TXD+ | HDLC2_TXD+
9	GPIO[09]	GPIO[09]	UART5_TXD- | HDLC3_TXD-
10	GPIO[10]	GPIO[10]	UART5_TXD+ | HDLC3_TXD+
33	GPIO[13]	GPIO[13]	UART6_TXD- | HDLC3_TCK-
32	GPIO[14]	GPIO[14]	UART6_TXD+ | HDLC3_TCK+
50	UART1_RXD- | HDLC1_RXD-	FM_RXD	UART1_RXD- | HDLC1_RXD-
49	UART1_RXD+ | HDLC1_RXD+	-	UART1_RXD+ | HDLC1_RXD+
21	UART2_RXD- | HDLC1_RCK-	FM_CTS	UART2_RXD- | HDLC1_RCK-
22	UART2_RXD+ | HDLC1_RCK+	-	UART2_RXD+ | HDLC1_RCK+
20	UART3_RXD- | HDLC2_RXD-	S1_RXD	UART3_RXD- | HDLC2_RXD-
19	UART3_RXD+ | HDLC2_RXD+	-	UART3_RXD+ | HDLC2_RXD+
13	UART4_RXD- | HDLC2_RCK-	FM_DSR	UART4_RXD- | HDLC2_RCK-
14	UART4_RXD+ | HDLC2_RCK+	-	UART4_RXD+ | HDLC2_RCK+
11	GPIO[11]	FM_TCK	UART5_RXD- | HDLC3_RXD-
12	GPIO[12]	-	UART5_RXD+ | HDLC3_RXD+
30	GPIO[15]	FM_RCK	UART6_RXD- | HDLC3_RCK-
31	GPIO[16]	-	UART6_RXD+ | HDLC3_RCK+
42	GPIO[01]		
41	GPIO[02]		
40	GPIO[03]		
39	GPIO[04]		
38	GPIO[05]		
37	GPIO[06]		
43	GPIO[07]		
44	GPIO[08]		
34	Ground		
35	Ground		
36	Ground		
45	Ground		
46	Ground		
47	Ground		

Table 7: FP2 Connector Pin Assignment

4.2 Front Panel Cables

Overview

Section available in next release of this document.

Wiring Diagram

Section available in next release of this document.

4.3 Onboard Connectors

4.3.1 Location

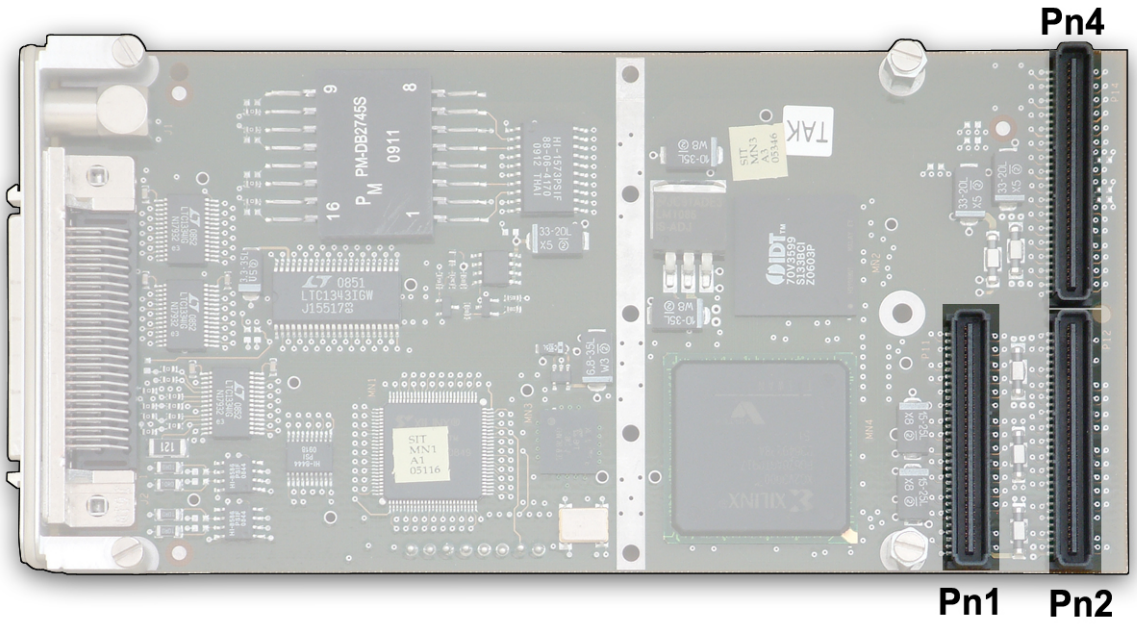

Figure 14: Onboard Connectors Location

4.3.2 Pn1 PMC Connector Pin Assignments

The Pn1 32-bit PCI connector pin assigments are consistent with the standard IEEE Std 1386.1.

Pin	Signal Name	Description	Pin	Signal Name	Description
1	TCK	Test Clock	2	-12 V	-12 volts DC power
3	Ground	Ground	4	INTA#	Interrupt A
5	INTB#	Interrupt B	6	INTC#	Interrupt C
7	BUSMODE1#	Bus Mode 1	8	+5 V	+5 volts DC power
9	INTD#	Interrupt D	10	PCI-RSVD	Reserved for future expansion
11	Ground	Ground	12	3.3Vaux	I/O Voltage
13	CLK	Clock	14	Ground	Ground
15	Ground	Ground	16	GNT#	Grant
17	REQ#	Request	18	+5V	+5 volts DC power
19	N.C.	Not Connected	20	AD[31]	Address/Data Bit 31
21	AD[28]	Address/Data Bit 28	22	AD[27]	Address/Data Bit 27
23	AD[25]	Address/Data Bit 25	24	Ground	Ground
25	Ground	Ground	26	C/BE[3]#	Command/Byte Enables
27	AD[22]	Address/Data Bit 22	28	AD[21]	Address/Data Bit 21
29	AD[19]	Address/Data Bit 19	30	+5 V	+5 volts DC power
31	N.C.	Not Connected	32	AD[17]	Address/Data Bit 17
33	FRAME#	Cycle Frame	34	Ground	Ground
35	Ground	Ground	36	IRDY#	Initiator Ready
37	DEVSEL#	Device Select	38	+5 V	+5 volts DC power
39	Ground	Ground	40	LOCK#	Lock
41	PCI-RSVD	Reserved for future expansion	42	PCI-RSVD	Reserved for future expansion
43	PAR	Parity	44	Ground	Ground
45	N.C.	Not Connected	46	AD[15]	Address/Data Bit 15
47	AD[12]	Address/Data Bit 12	48	AD[11]	Address/Data Bit 11
49	AD[09]	Address/Data Bit 9	50	+5 V	+ 5 volts DC power
51	Ground	Ground	52	C/BE0#	Command/Byte Enable
53	AD[06]	Address/Data Bit 6	54	AD[05]	Address/Data Bit 5
55	AD[04]	Address/Data Bit 4	56	Ground	Ground
57	N.C.	Not Connected	58	AD[03]	Address/Data Bit 3
59	AD[02]	Address/Data Bit 2	60	AD[01]	Address/Data Bit 1
61	AD[00]	Address/Data Bit 0	62	+5 V	+5 volts DC power
63	Ground	Ground	64	REQ64#	Request 64-bit transfer

Table 8: Pn1 PMC Signal Definitions

4.3.3 Pn2 PMC Connector Pin Assignments

The Pn2 32-bit PCI connector pin assigments are consistent with the standard IEEE Std 1386.1.

Pin	Signal Name	Description	Pin	Signal Name	Description
1	+12 V	+12 Volts DC Power	2	TRST#	Test Reset
3	TMS	Test Select	4	TDO	Test Data Output
5	TDI	Test Data Input	6	Ground	Ground
7	Ground	Ground	8	PCI-RSVD	Reserved for future expansion
9	N.C.	Reserved for future expansion	10	PCI-RSVD	Reserved for future expansion
11	BMODE2#	Bus Mode 2	12	+3.3 V	+3.3 Volts DC Power
13	RST#	ResetMode	14	BUSMODE3#	Bus Mode 3
15	+3.3 V	+ 3.3 Volts DC Power	16	BUSMODE4#	Bus Mode 4
17	PME#	Power Management Event	18	Ground	Ground
19	AD[30]	Address/Data Bit 30	20	AD[29]	Address/Data Bit 29
21	Ground	Ground	22	AD[26]	Address/Data Bit 26
23	AD[24]	Address/Data Bit 24	24	+3.3 V	+ 3.3 Volts DC Power
25	IDSEL	Initialization Device Select	26	AD[23]	Address/Data Bit 23
27	+3.3 V	+ 3.3 Volts DC Power	28	AD[20]	Address/Data Bit 20
29	AD[18]	Address/Data Bit 18	30	Ground	Ground
31	AD[16]	Address/Data Bit 16	32	C/BE[2]#	Command/Byte Enable
33	Ground	Ground	34	PMC-RSVD	Reserved for future expansion
35	TRDY#	Target Ready	36	+3.3 V	+ 3.3 Volts DC Power
37	Ground	Ground	38	STOP#	Stop
39	PERR#	Parity Error	40	Ground	Ground
41	+3.3 V	+3.3 Volts DC Power	42	SERR#	System Error
43	C/BE[1]#	Command/Byte Enable	44	Ground	Ground
45	AD[14]	Address/Data Bit 14	46	AD[13]	Address/Data Bit 13
47	M66EN	66 MHz Enable	48	AD[10]	Address/Data Bit 10
49	AD[08]	Address/Data Bit 8	50	+3.3 V	+ 3.3 Volts DC Power
51	AD[07]	Address/Data Bit 7	52	PMC-RSVD	Reserved for future expansion
53	+3.3 V	+3.3 Volts DC Power Supply	54	PMC-RSVD	Reserved for future expansion
55	PMC-RSVD	Reserved for future expansion	56	Ground	Ground
57	PMC-RSVD	Reserved for future expansion	58	PMC-RSVD	Reserved for future expansion
59	Ground	Ground	60	PMC-RSVD	Reserved for future expansion
61	ACK64#	Acknowledge 64-bit transfer	62	+3.3 V	+3.3 Volts DC Power
63	Ground	Ground	64	PMC-RSVD	Reserved for future expansion

Table 9: Pn2 PMC Signal Definitions

4.3.4 Pn4 PMC Connector Pin Assignments

The Pn4 32-bit PCI connector pin assigments depend on the Serial I/O Build Option:

- H-Type Serial I/O Build Option: refer to section 4.3.4.1 on page 45,
- B-Type and M-Type Serial I/O Build Options not available via the Pn4 PMC connector.

The Signal Description is available in section 4.4 on page 46.

4.3.4.1 HDLC H-Type Build Option

- MIL-STD-1553-B Single Redundant Channel, Bus Controller or Remote Terminal
- ARINC-429 4 Receive and 2 Transmit Channels
- Serial Lines 6 UART Simple Lines or 3 HDLC Synchronous Full Duplex Lines
- GPIO Lines 16 Lines

Pin	Signal Name		Pin	Signal Name	
1	Ground		2	GPIO[06]	
3	Ground		4	GPIO[05]	
5	ARINC429_1_TX-		6	GPIO[04]	
7	ARINC429_1_TX+		8	GPIO[03]	
9	ARINC429_2_TX-		10	GPIO[02]	
11	ARINC429_2_TX+		12	GPIO[01]	
13	ARINC429_1_RX+		14	GPIO[08]	
15	ARINC429_1_RX-		16	GPIO[07]	
17	ARINC429_2_RX+		18	Ground	
19	ARINC429_2_RX-		20	Ground	
21	ARINC429_3_RX-		22	UART5_TXD+	HDLC3_TXD+
23	ARINC429_3_RX+		24	UART5_TXD-	HDLC3_TXD-
25	ARINC429_4_RX-		26	UART5_RXD+	HDLC3_RXD+
27	ARINC429_4_RX+		28	UART5_RXD-	HDLC3_RXD-
29	UART6_RXD+	HDLC3_RCK+	30	UART4_RXD-	HDLC2_RCK-
31	UART6_RXD-	HDLC3_RCK-	32	UART4_RXD+	HDLC2_RCK+
33	UART6_TXD+	HDLC3_TCK+	34	UART3_TXD+	HDLC2_TXD+
35	UART6_TXD-	HDLC3_TCK-	36	UART3_TXD-	HDLC2_TXD-
37	UART4_TXD+	HDLC2_TCK+	38	UART1_RXD+	HDLC1_RXD+
39	UART4_TXD-	HDLC2_TCK-	40	UART1_RXD-	HDLC1_RXD-
41	UART3_RXD-	HDLC2_RXD-	42	UART1_TXD+	HDLC1_TXD+
43	UART3_RXD+	HDLC2_RXD+	44	UART1_TXD-	HDLC1_TXD-
45	UART2_RXD+	HDLC1_RCK+	46	UART2_TXD+	HDLC1_TCK+
47	UART2_RXD-	HDLC1_RCK-	48	UART2_TXD-	HDLC1_TCK-
49	Ground		50	GPIO[16]	
51	Ground		52	GPIO[15]	
53	1553_TXRX_B-		54	GPIO[14]	
55	1553_TXRX_B+		56	GPIO[13]	
57	Ground		58	GPIO[12]	
59	Ground		60	GPIO[11]	
61	1553_TXRX_A+		62	GPIO[10]	
63	1553_TXRX_A-		64	GPIO[09]	

Table 10: Pn4 PMC Signal Definitions

4.4 Signal Description

Mnemonic	Description
1553_TXRX_A+/-	1553-B Transmit Receive Channel A +/-
1553_TXRX_B+/-	1553-B Transmit Receive Channel B +/-
ARINC429_*i*_RXCH+/-	ARINC-429 Receive +/-Channel *i*
ARINC429_*i*_TXCH+/-	ARINC-429 Transmit +/- Channel *i*
FM_CTS	Full Modem Serial Line - Clear-To-Send
FM_DSR	Full Modem Serial Line - Data Set Ready
FM_RTS	Full Modem Serial Line - Ready-To-Send
FM_RCK	Full Modem Serial Line - Receive Clock
FM_RXD	Full Modem Serial Line - Receive Data
FM_TCK	Full Modem Serial Line - Transmit Clock
FM_TXD	Full Modem Serial Line - Transmit Data
GPIO	General Purpose Input/Output Signal
Ground	Ground
HDLC*i*_RXD+/-	Synchronous HDLC Receive +/- Line *i*
HDLC*i*_TXD+/-	Synchronous HDLC Transmit +/- Line *i*
HDLC*i*_RCK+/-	Synchronous HDLC Receive Clock +/- Line *i*
HDLC*i*_TCK+/-	Synchronous HDLC Transmit Clock +/- Line *i*
*Si*_RXD	Asynchronous Receive Simplified Line Line *i*
*Si*_TXD	Asynchronous Transmit Simplified Line *i*
UART*i*_RXD+/-	Asynchronous UART Receive Simplified Line +/- Line *i*
UART*i*_TXD+/-	Asynchronous UART Transmit Simplified +/- Line *i*

Table 11: Signal Definitions

Appendix A - Specifications

Appendix A lists the general, physical and environmental specifications. It also covers items such as power requirements, EMC regulatory compliance and safety, and flammability rating.

A.1 General Specifications

Model	PMC-6L PCI Mezzanine Card
PCI Compliance	PCI 3.0, 3.3V signaling
Form Factor	IEEE P1386
PCI Bus Speed	33/66 MHz
PCI-X Bus Speed	66/100/133 MHz
PCI Bus Width	32/64 bits
Signal Standards	LVDS IEEE 1596.3
Certification	Designed to meet FCC Class A, CE, UL 1950

Table 12: General Specifications

A.2 Physical Specifications

Bus Interface	PCI 3.0, 3.3V signaling
Dimension	75 mm x 150 mm x 8.2 mm
Weight	80g
Power Supply	3.3 VDC
Power Consumption	7.5W max.
Form Factor	P1386

Table 13: Physical Specifications

A.3 Environmental Specifications

Depending on its environment class, the PMC-6L operates under the following conditions.

The PMC-6L may be stored or transported without damage within the following limits:

	SA	WA	RA	RC
Temperature Range				
Airflow	1.2 m/s	1.5 m/s	1.8 m/s	NA
Operating	0°C to +55°C	-20°C to +65°C	-40°C to +75°C	-40°C to +85°C
Storage	-45°C to +85°C	-45°C to +85°C	-45°C to +100°C	-45°C to +100°C
Conformal Coating	Optional	Standard	Standard	Standard
Relative Humidity	no condensation 90%	95% 10 cycles 240 hours	95% 10 cycles 240 hours	95% 10 cycles 240 hours
Mechanical				
Vibration Sine	5-200 Hz - 2g Peak	5-200 Hz - 2g Peak	5-2000 Hz - 2.5g Peak	5-2000 Hz - 5g Peak
Vibration	0.01g^2/Hz 10-40 Hz	0.01g^2/Hz 10-40 Hz	0.04g^2/Hz	0.1g^2/Hz
Random	0.0007g^2/Hz 100-200 Hz - 0.00005g^2/Hz 2000 Hz		with a flat response to 1,000 Hz 6 dB/Oct roll-off from 1 KHz-2 KHz	
Shock	10g peak 16 ms Half Sine Pulse		40g peak 20 ms Half Sine Pulse	
Bumps			40g peak 6 ms Half Sine Pulse 3 bumps/sec and 1,000 bumps/direction	
Altitude	-1,000 to 15,000 ft -300 to 4500m	-1,000 to 33,000 ft -300 to 9900m	-1,000 to 33,000 ft -300 to 9900m	-1,000 to 50,000 ft -300 to 15000m

Table 14: Environmental Specifications

A.4 Power Requirements

	PMC-6L Power Drain
+5V +5%, -2.5%	N.A.
+3.3V +5%, -2.5%	~ 5W
-12V +5%, -2.5%	N.A.
-12V +5%, -2.5%	N.A

Table 15: Power Requirements

A.4.1 +5V Power Recommendations

Not used by the PMC-6L.

The +5V voltage (VCC_IN) is insured the the PMC standard in the range [+4.875V - +5.25V]

A.4.2 +3.3V Power Recommendations

The +3.3V voltage (VDD_IN) is insured the the PMC standard in the range [+3.2175V - +3.465V]. It is provided by the Pn2 PMC connector

A.5 EMC Regulatory Compliance and Safety

The PMC-6L is designed for use in systems meeting EMC qualifications EN55082 (Ed. 09/95) and EN55022 (Ed. 22/94) class A.

A.6 Flammability Rating

The boards are manufactured by UL approuved manufacturers and have a flammability rating of 94V-0.

A.7 MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for seven types of environment:

- Ground Benign (GB),
- Air Inhabited Cargo (AIC),
- Ground Fixed (GF),
- Naval Sheltered (NS),
- Air Rotary Wing (ARW),
- Air Uninhabited Fighter (AUF),
- Ground Mobile (GM).

Ground Benign (Hours)		Air Inhabited Cargo (Hours)	Ground Fixed (Hours)		Naval Sheltered (Hours)		Air Rotary Wing (Hours)	Air Uninhabited Fighter (Hours)	Ground Mobile (Hours)
30°C	40°C	40°C	30°C	50°C	30°C	40°C	50°C	40°C	30°C
453 710	374 282	78 430	162 664	132 256	81 933	78 171	29 642	35 565	67 053

Table 16: MTBF Data in Operating Mode

Ground Benign (Hours)		Air Inhabited Cargo (Hours)	Ground Fixed (Hours)		Naval Sheltered (Hours)		Air Rotary Wing (Hours)	Air Uninhabited Fighter (Hours)	Ground Mobile (Hours)
30°C	40°C	40°C	30°C	50°C	30°C	40°C	50°C	40°C	30°C
11 422 834	10 268 323	1 620 268	3 559 591	3 188 151	1 765 676	1 715 364	656 885	731 423	1 490 892

Table 17: MTBF Data in Storage Mode

Appendix B - List of Abbreviations

AC	Alternating Current
ANSI	American National Standards Institute
ASCII	American Standard Code for Information Interchange
BAR	Base Address Register
BC	Bus Controller
BCSR	Board Control and Status Registers
BIST	Built-In Self Test
CR	Control Register
DC	Direct Current
DDR	Double Data Rate
DMA	Direct Memory Access
DMAC	DMA Controller
EPROM	Erasable Programmable Read Only Memory
EEPROM	Electrically Erasable Programmable Read Only Memory
EIA	Electronic Industries Alliance
EOF	End of Frame
EOT	End of Transfer
ESD	Electrostatic Sensitive Device
FIFO	First In, First Out
FPDP	Front Panel Data Port
FPGA	Field Programmable Gate Array
FSTAT	Frame Status
IEEE	Institute of Electrical and Electronic Engineers
IOCM	I/O Configuration Module
ISP	In-System Programming
JTAG	Joint Test Action Group
LE	Logical Element

LED	Light Emitting Diode
LSB	Least Significant Byte
LSW	Least Significant Word
LUT	Look Up Table
LVDS	Low Voltage Differential Signaling
LVTTL	Low Voltage Transistor-Transistor Logic
MFI	Multi-Function Interface
MSW	Most Significant Word
MTBF	Mean Time Between Failures
P4DP	P4 Data Port
PCI	Peripheral Component Interface
PCIBAR	PCI Base Address Register
PIM	PCI Interface Module
PMC	PCI Mezzanine Card
RT	Remote Terminal
R/W	Read/Write
SERDES	Serializer/Deserializer
SOF	Start of Frame
SRAM	Static Random Access Memory
VPD	Vital Product Data

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