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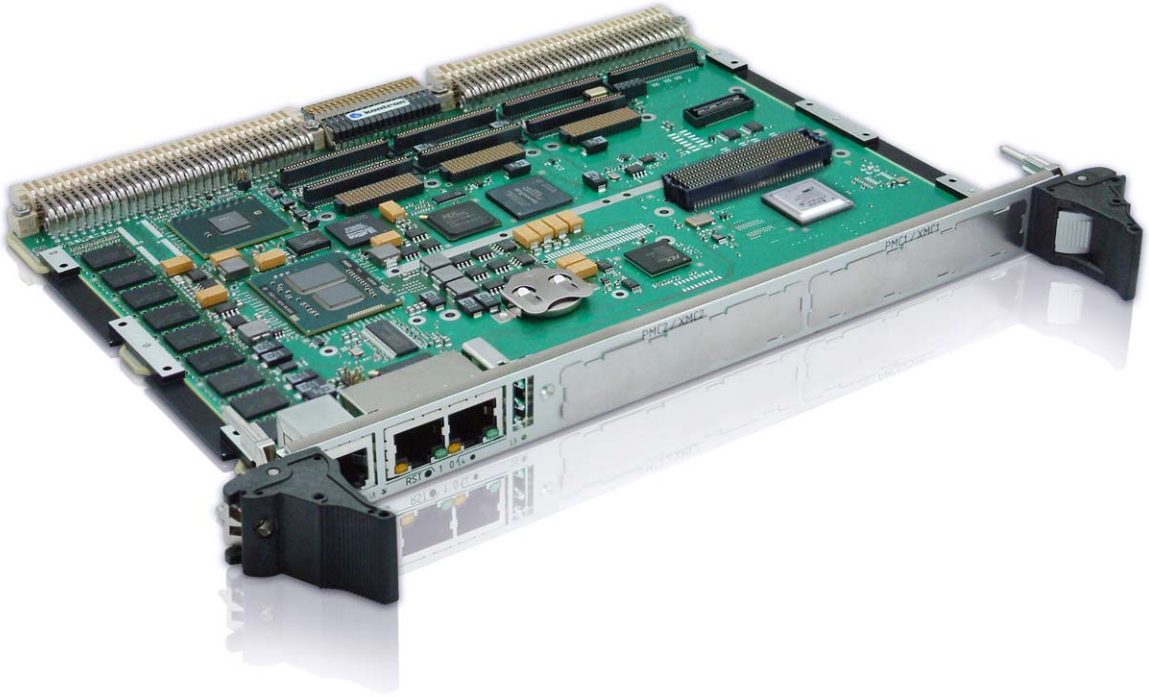

6U VME Single Board Computer
User's Guide

CA.DT.A93-4e - June 2013

Revision History

Publication Title:	VM6050 User's Guide	
Doc. ID:	CA.DT.A93-4e	
Rev.	**Brief Description of Changes**	**Date of Issue**
4e	Main update: - section 3.3 - CPLD Features - new section 3.5 - GPIOs - chapter 5 - Power and Thermal Specifications - section 9.8 - Peripheral Connectivity Other changes are identified by a vertical bar in the margin.	06-2013
3e	New Chapter 8: VM6050-RA Characteristics	10-2012
2e	Add of: - New Order Code available - SA/WA Thermal Curve - RC Frequency Operation - SATA Mezzanine Description - Chapter 6: Graphics Module Description - FMC Routing and IO Block Diagram - Appendix A: Graphics Resolution Update of: - P0 Assignment - VM6050 Power Consumption	07-2012
1e	Update of P0 and P2 Connector Pin Assignments New Chapter 9: VM6050-RC Characteristics	01-2012
0e	Preliminary Version	07-2011

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- improve the environmental performance of all those involved during the lifecycle of EEE

Conventions

This guide uses several types of notice: Note, Caution, ESD.

Note: this notice calls attention to important features or instructions.


Caution: this notice alert you to system damage, loss of data, or risk of personal injury.


ESD: This banner indicates an Electrostatic Sensitive Device.

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix `0x' shows a hexadecimal number, following the `C' programming language convention.

The multipliers `k', `M' and `G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when `K', `M' and `G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

When describing transfer rates, `k' `M' and `G' mean $*10^3$, $*10^6$ and $*10^9$ *not $*2^{10}$ $*2^{20}$ and $*2^{30}$.*

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and CompactPCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Signal names ending with an asterisk (*) or a hash (#) denote active low signals; all other signals are active high.

Signal names follow the PICMG 2.0 R3.0 CompactPCI Specification and the PCI Local Bus 2.3 Specification.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions


Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.


Caution, Electric Shock!
Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Chapter 1 - Introduction

The Kontron VM6050 is a 6U VME Single Board Computer (SBC) for parallel data and signal processing applications in the communications, military, aerospace, medical, industrial, and infotainment markets.

The VM6050 implements Intel's next generation high performance embedded processor with integrated memory controller and Intel® HD graphics - the Intel® Core™ i7 processor - coupled with the highly integrated Intel® Platform Controller Hub (PCH) QM57 with numerous Gigabit Ethernet, SATA, USB 2.0 and PCIe channels.

The VM6050 board comes with EFI BIOS and supports Linux. It is covered by Kontron's long term supply program, which guarantees customers multi-year supply of the product beyond its active life.

The VM6050 provides exceptional I/O capabilities onboard and outstanding flexibility by being a 6U VME board to provide support for PMC, XMC and FMC mezzanine cards.

The VM6050's high performance, 2eSST, VME interface helps customers preserve their investment in legacy VME equipment.

The VM6050 was designed to be Kontron's next generation VME SBC providing substantial price and performance over previous generations of VME computers.

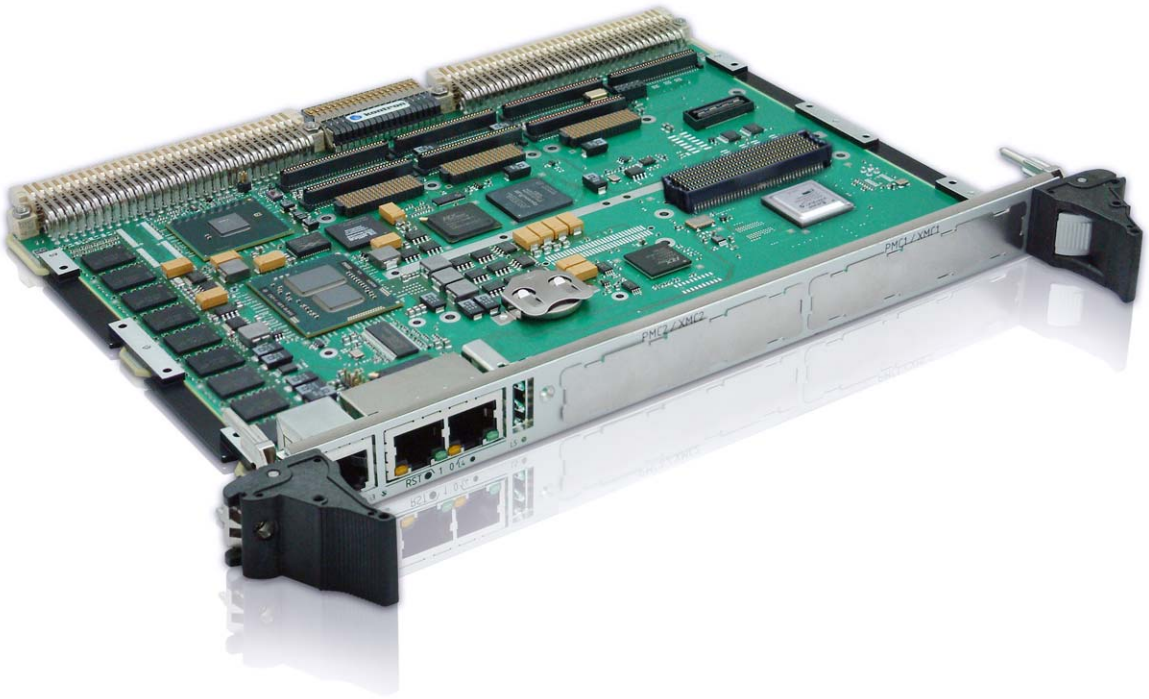


Figure 1: VM6050-SA 6U VME Overview

1.1 Manual Overview

1.1.1 Objective

This guide provides general information, hardware instructions, operating instructions and functional description of the VM6050 board. The onboard programming, onboard firmware and other software (e.g. drivers and BSPs) are described in detail in separate guides (see section 1.x "Related Publications").

This hardware technical documentation reflects the most recent version of the product. The "Hardware release Notes" (see section 1.6 "Related Publications") might help to keep track of potential evolutions.

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

1.1.2 Audience

This guide is written to cover, as far as possible the range of people who will handle or use the VM6050, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, system, cabling, grounding and communications.

1.1.3 Scope

This guide describes all variants of the VM6050 series. It does not cover any PMC/XMC modules which are described in specific guides.

1.1.4 Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- Chapter 1 - Introduction (this chapter)
- Chapter 2 - Installation
- Chapter 3 - Additional Board Features
- Chapter 4 - Physical In/Out
- Chapter 5 - Power and Thermal Specifications
- Chapter 6 - Graphic Module Characteristics
- Chapter 7 - VM6050-RTM Characteristics
- Chapter 8 - VM6050/RA Characteristics
- Chapter 9 - VM6050/RC Characteristics
- Appendix A - Graphics Resolution

1.1.5 Terminology, Definitions and Abbreviations

In this document, the term:

- VM6050 will be associated to the 6U VME board
  - VM6050-SA will be associated to the standard air-cooled commercial version of the board.
  - VM6050-WA will be associated to the air-cooled extended temperature version of the board.
  - VM6050-RA will be associated to the rugged air-cooled version of the board.
  - VM6050-RC will be associated to the rugged conduction-cooled version of the board.
- VM6050-RTM will be associated to the 6U VME Rear Transition Module (RTM).

1.2 Board Overview

1.2.1 Main Features

Intel® Core™ i7 Architecture

The VM6050 single board computer is a VME computing blade for parallel data and signal processing application. Target applications include radar, sonar, imaging systems, airborne fighters, and unmanned aerial vehicle (UAV) radar, as well as rugged multi-display consoles.

The processing node of the VM6050 implements an Intel® Core™ i7 processor coupled with dual channel DDR3 memory. The highly integrated Intel® QM57 Express platform hub provides numerous Gigabit Ethernet, SATA, USB 2.0 and PCIe channels. The 6U-format VM6050 is available in standard air-cooled and conduction-cooled versions.

The frequency of the CPU is 2.0 GHz; however, the processor Intel® Core™ i7 is equipped with the Turbo Boost technology, which allows increasing the frequency up to 2.8 GHz when the total on chip power allows (depending on second core and graphics activity).

Soldered DDR3 Memories with the Support of ECC

The processor accesses two memory-channels (2 x 72-bit) having a total size of 4 or 8 GB. The DDR3 memory technology used operates at 1066 MT/s. An 8 bits ECC memory is implemented to detect and correct errors.

Numerous Storage Interface and Non Volatile Memories

The following storage features are available :

- A USB 2.0 Flash drive slot is available onboard supporting low profile USB 2.0 Flash disk modules up to 16 GB.
- Redundant 32 Mbits NOR flash memories are used to store firmware code.
- Two serial 256 Kbits EEPROMs are dedicated to system and application data storage.
- A 512 Kbits Ferro Magnetic, Non-volatile Random Access Memory allows the backup of critical data when the board is powered off.

All the Flash and non volatile memories onboard have a write protect mechanism taking into account the NVMRO (Non Volatile Memory read Only) signal.

Backplane Switch

Two Gigabit Ethernet links are available on P0 connector. P0 Ethernet routing supports VITA 31.1 backplane networking.

In addition, one 4x PCI Express link is available on P0.

Extensive I/O Connectivity

A SATA drive slot is available onboard supporting SATA HDD up to 120 GB.

The VM6050 is equipped with the ALMA2f VME controller supporting the VME64x and 2eSST (optional) protocols offering up to 320 MB/s peak throughput.

The VM6050 provides up to four 10/100/1000BASE-T(X) Ethernet interfaces, two EIA-232 serial lines, six general purpose I/Os (GPIO), four (+ 2 front I/O) USB 2.0 links, three SATA II interfaces and one 4x PCI-Express link.

Two onboard mezzanine sites support PCI, PCI-Express and FMC cards (VITA 57 FPGA I/O).

FMC Support, VITA 57

The VM6050 is a high-performance 6U VME board able to support the new FPGA Mezzanine Card (FMC) standard defined by VITA 57.

Legacy Compatibility

The VM6050 has been designed to offer a legacy I/O compatibility with the Kontron's PENTXM2 and VM6250 boards to provide an easy path for technology insertion into existing systems.

Software

Kontron is one of the few compact PCI, VME and VPX vendors providing in-house support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software manufacturers, Kontron is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

Finally, Kontron grants his customer owners of a maintenance agreement a hotline software support and regular software updates. A dedicated web site is also available for online updates and release downloads.

The VM6050 is delivered with the UEFI BIOS from AMI.

The VM6050 supports Linux Fedora 14 distribution.

The VM6050 supports VxWorks 6.8 and Windows XP Cube WES 2009.

Please contact Kontron for further information regarding other operating systems and software support.

Harsh Environments

The VM6050 has been designed to use the same PCB for both air and conduction-cooled boards. Build variants span a complete range of temperature, shock and vibration requirements as specified in the VITA 47 standards.

10-year Long Life Cycle

Investing in a new project is always a challenge and risky. Maximizing the lifetime of an application is therefore a critical issue when it comes to saving development investments.

The VM6050 has been designed with long life cycle components. Beyond the use of standard commercially available components, Kontron offers Longevity of Supply services which are designed to make the VM6050 available for then years or longer.

Carrier Board

The VM6050 supports the V2PMC2, a 6U VME PCI-X/PMC carrier card that holds up to two single-width or one double-width PCI-X/PMC modules.

Rear Transition Module

The VM6050 supports the VM6050-RTM, a 6U VME Rear Transition Module compliant to PMC I/O Module Standard VITA 36 - 199x Draft 0.1 July 19, 1999 (mechanical and PIM format).

Extra I/O Module

The VM6050 is able to support a module compliant to PMC standard IEEE P1386.1 with additionnal I/Os such as USB, graphic, GPIO;

1.2.2 Block Diagram

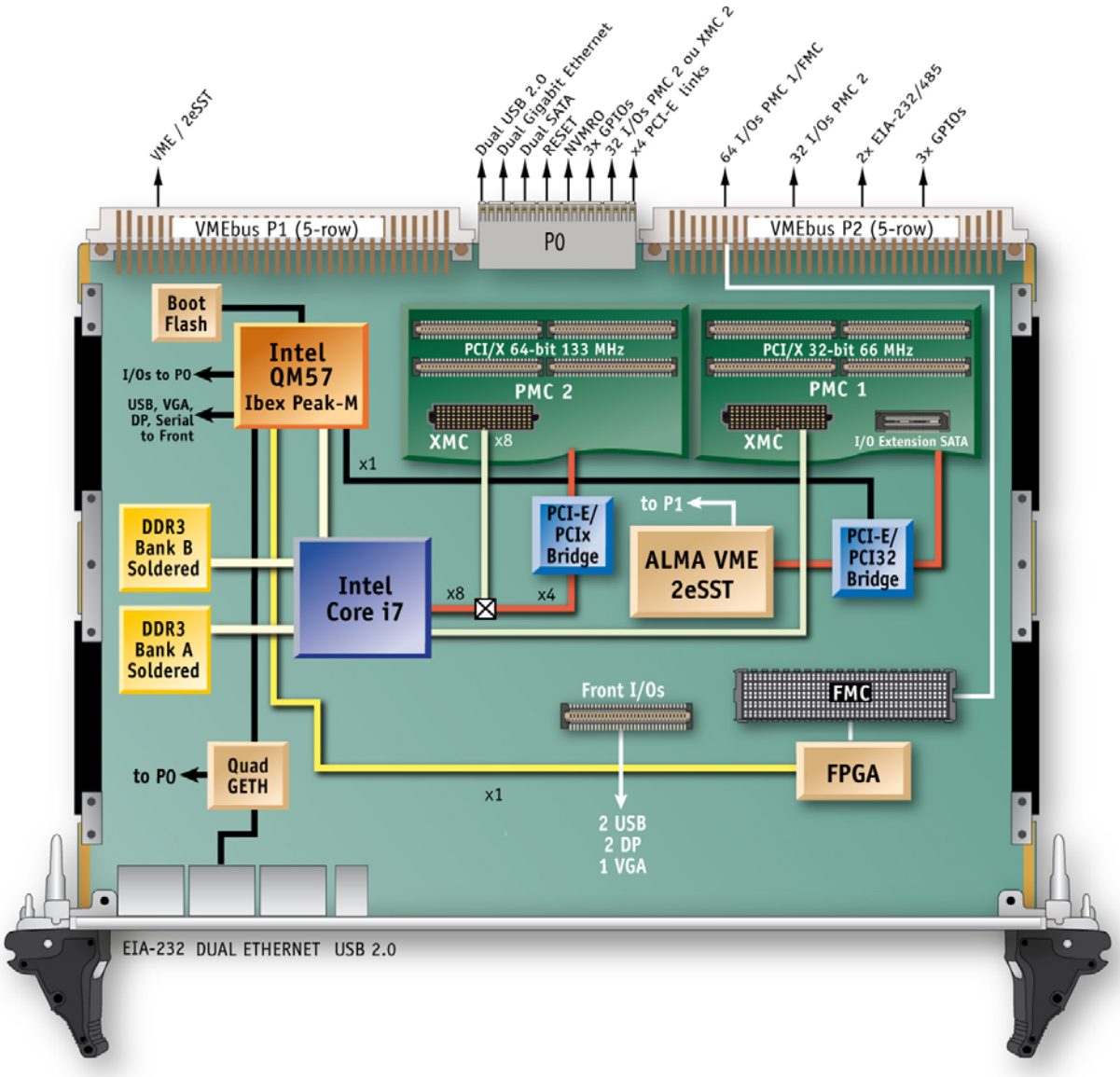


Figure 2: VM6050 Block Diagram

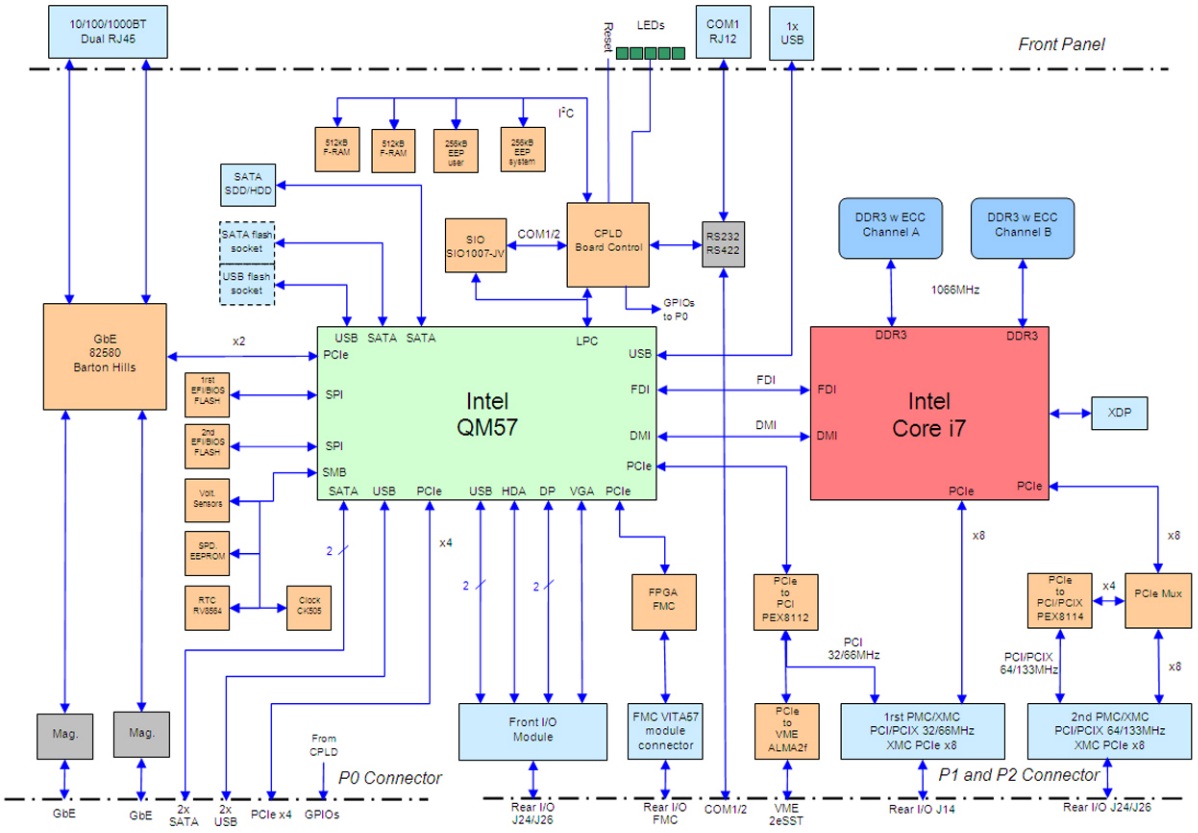


Figure 3: VM6050 Functional Block Diagram

1.2.3 Ordering Information

Manufacturing Options

- CPU Frequency: . . . . . 2 GHz (default)
- DDR3 SDRAM Size: . . . . . 4 GB total onboard
  . . . . . 8 GB total onboard
- Ruggedization Levels: . . . . . Standard Air-Cooled (SA)
  . . . . . Extended Temperature (WA)
  . . . . . Rugged Air-Cooled (RA)
  . . . . . Rugged Conduction-Cooled (RC)

Order Code Available

Order Code		Description
VM6050-SA	VM6050-2SA34-x2110	Core i7 620LE @ 2 GHz, SA class, 4 GB SDRAM, 2 front DP + 1 VGA + PMC/XMC
VM6050-SA	VM6050-2SA34-x0110	Core i7 620LE @ 2 GHz, SA class, 4 GB SDRAM, 2 PMC/XMC

Order Code		Description
VM6050-SA	VM6050-2SA35-x0110	Core i7 620LE @ 2 GHz, SA class, 8 GB SDRAM, 2 PMC/XMC
VM6050-SA	VM6050-2SA34-x0210	Core i7 620LE @ 2 GHz, SA class, 4 GB SDRAM, 2 PMC/XMC, 5V only SBC (12v needed if required by PMC/XMC) without P0
VM6050-SA	VM6050-2SA35-x0210	Core i7 620LE @ 2 GHz, SA class, 8 GB SDRAM, 2 PMC/XMC, 5V only SBC (12v needed if required by PMC/XMC) without P0
VM6050-SA	VM6050-2SA34-x0310	Core i7 620LE @ 2 GHz, SA class, 4 GB SDRAM, 2 PMC/XMC, 5V only SBC with P0
VM6050-SA	VM6050-2SA35-x0310	Core i7 620LE @ 2 GHz, SA class, 8 GB SDRAM, 2 PMC/XMC, 5V only SBC with P0
VM6050-WA	VM6050-2WA34-x0110	Core i7 620LE @ 2 GHz, WA (Extended Air) Class, 4 GB DDR3-SDRAM, 2 PMC/XMC
VM6050-WA	VM6050-2WA35-x0110	Core i7 620LE @ 2 GHz, WA (Extended Air) Class, 8 GB DDR3-SDRAM, 2 PMC/XMC
VM6050-WA	VM6050-2WA34-x0210	Core i7 620LE @ 2 GHz, WA (Extended Air) Class, 4 GB DDR3-SDRAM, 2 PMC/XMC, 5V only, without P0
VM6050-WA	VM6050-2WA35-x0210	Core i7 620LE @ 2 GHz, WA (Extended Air) Class, 8 GB DDR3-SDRAM, 2 PMC/XMC, 5V only, without P0
VM6050-WA	VM6050-2WA34-x0310	Core i7 620LE @ 2 GHz, WA (Extended Air) Class, 4 GB DDR3-SDRAM, 2 PMC/XMC, 5V only, with P0
VM6050-WA	VM6050-2WA35-x0310	Core i7 620LE @ 2 GHz, WA (Extended Air) Class, 8 GB DDR3-SDRAM, 2 PMC/XMC, 5V only, with P0
VM6050/RA	VM6050-2RA34-x0110	Core i7 620LE @ 2 GHz, RA Class, 4 GB SDRAM, 2 PMC/XMC
VM6050/RA	VM6050-2RA34-x0210	Core i7 620LE @ 2 GHz, RA Class, 4 GB SDRAM, 2 PMC/XMC, 5V only (12V needed if required by PMC/XMC
VM6050-RC	VM6050-2RC34-x0110	Core i7 620LE @ 2 GHz, RC Class, 4 GB SDRAM, 2 PMC/XMC
VM6050-RC	VM6050-2RC34-x0210	Core i7 620LE @ 2 GHz, RC Class, 4 GB SDRAM, 2 PMC/XMC, 5V only (12V needed if required by PMC/XMC

x: 0 = no Flash
1 = 8 GB USB Flash min
2 = 8 GB SATA Flash min

Order Code		Description
Associated Product		
RTM	PBV36-P0-VM6-00	6U VME Air-Cooled Rear Transition Module, 2 PIMs, no face-plate to use with PIM-2DP-00
Console Cable	KIT-RJ12DB9	Adaptation Cable RJ-12 <-> DB-9
PMCs Carrier	V2PMC2-SA	6U VME Air-Cooled Dual PMCs Carrier Card
PMCs Carrier	V2PMC2-RC	6U VME Conduction-Cooled Dual PMCs Carrier Card
USB Flash Disk	FDM-USB-xGB-L2-IV	USB Flash Disk Module (contact Kontron for the available capacity)
SATA Flash Disk	FDM-SATA-xGB-10V	SATA Flash Disk Module (contact Kontron for the available capacity)
PIM	PIM-2DP-000	Dual DisplayPort interface PIM module to use with graphic module MOD-GX-RC-00
Kit Disk SATA	KIT-DISK25-SATA	Kit Disk SATA; compatible with SATA disk 2.5-inch
	KIT-DISK18-SATA	Kit Disk SATA; compatible with SATA disk 1.8-inch
EZ-VM6050	EZ-VM6050	Laboratory 6U VME Air-Cooled Development System
FMC Mezzanine	FMC-SER0	EIA-232 serial line interface and GPIO on rear
Graphics Module(*)	MOD-GX-SA-00	Air-cooled graphics module with two DisplayPorts and one VGA Port on front panel
Graphics Module(*)	MOD-GX-RC-00	Conduction cooled graphics module with two DisplayPorts on rear / No VGA

(*) already included in the product when ordering with VGA/eDP option.

Table 1: Order Code

1.2.4 I/O Interfaces

FUNCTION	DESCRIPTION
Ethernet	Intel i82580 low-power quad Gigabit Ethernet Transceiver: - Two 10/100/1000BASE-T(X) ports available on RJ-45 front panel connectors - Two 10/100/1000BASE-T(X) ports available on the rear P0 connector
USB	Four USB 2.0 channels - USB port 0 9-pin USB pin header, horizontal USB flash disk module - USB port 1 One USB port available on the VM6050 front panel - USB ports 2, 3 Two USB ports available on rear P0 connector
Serial ATA (SATA)	- Two SATA II ports are available on rear P0 connector - One SATA II port is available onboard. - One SATA II port is available onboard flash disk module
Serial Ports	Two serial ports EIA-232/485 - COM1 EIA-232/485 (simplified) port on RJ-12 front panel connector or on the rear P2 connector - COM2 EIA-232/485 on the rear P2 connector

FUNCTION	DESCRIPTION
GPIO	Three General Purpose I/O on rear P0 connector and three General Purpose I/O on P2 connector, two extra GPIO are available on P2 on customer request
LED	Five status LEDs on front panel: L1, L2, L3, L4, L5
Reset	One reset button on front panel.
PMC/XMC/FMC	2x PMC/XMC slots and 1x FMC slot PCI 32-bit 66 Mhz available on slot 1, no 5V tolerant PCI-X 64-bit 133 Mhz available on slot 2, no 5V toleant XMC 8*lanes for both slots complant to Gen1 (2.5 GT/s) PCI-e frequency
Graphic	2x DisplayPort interface on P8 connector, HDMI/DVI compatible 1x VGA interface on P8 connector
USB	2x Extra USB on P8 connector
Audio	High definition Audio on P9 connector
Extra GPIOs	6 Extra GPIOs with VITA 57 option on P9 connector

Table 2: I/O Interfaces

FUNCTION	VM6050		VM6050-RTM	
	Front Panel	Onboard	Front Panel	Onboard
Gigabit Ethernet	Y (x2)	-	Y (x2)	-
USB1	-	Y (9-pin)	-	-
USB0	Y	-	-	-
USB2, USB3	-	-	Y (x1)	-
SATA (P0 Manufacturing Option)	-	-	Y (x2)	-
SATA (onboard Manufacturing Option)	-	Y	-	-
SATA Mezzanine	-	Y (9-pin)	-	-
COM1 (EIA-232)	Y	-	-	Y (10-pin)
COM2 (EIA-232)	-	-	-	Y (10-pin)
GPIO	-	-	-	Y (x6)
LED	Y (x5)	-	-	-
Reset Button	Y	-	-	-
PCI-Express	-	-	Y	-
SMB	-	-	-	Y
DisplayPort or HDMI/DVI*	Y (x2)	-	Y (x2)	-
VGA Interface*	Y	-	-	-
USB 4, USB 5	-	Y (x2)	-	-

* Available with MOD-GX board

Table 3: Peripheral Connectivity

Front Interfaces

Not available on RC (Rugged Conduction-Cooled) boards

Figure 4: Front Panel Connectors

Function	Description	See also
Serial Ports	COM: 1x EIA-232/EIA-485 UART interface for CPU on RJ-12 connector.	Section 4.1.1 for Pin Assignment
Gigabit Ethernet	Two 10/100/1000BASE-T(X) ports on RJ45	Section 4.1.2 for Pin Assignment
USB	USB 2.0 interface	Section 4.1.3 for Pin Assignment
Reset	Reset push button	Figure 5
LEDs	5 LEDs reporting the board CPU health status and activity	Section 4.8 for LEDs Description
PMC/XMC	2x PMC/XMC slots	Sections 4.4 & 4.5 for PMC/XMC Description

Table 4: Front I/O Interfaces

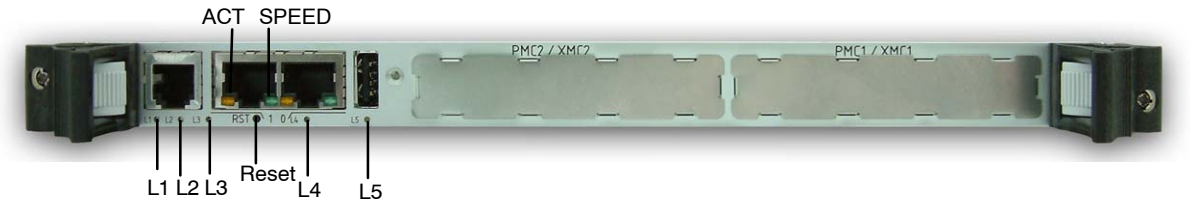


Figure 5: Reset Button and LEDs

1.2.5 Components Layout

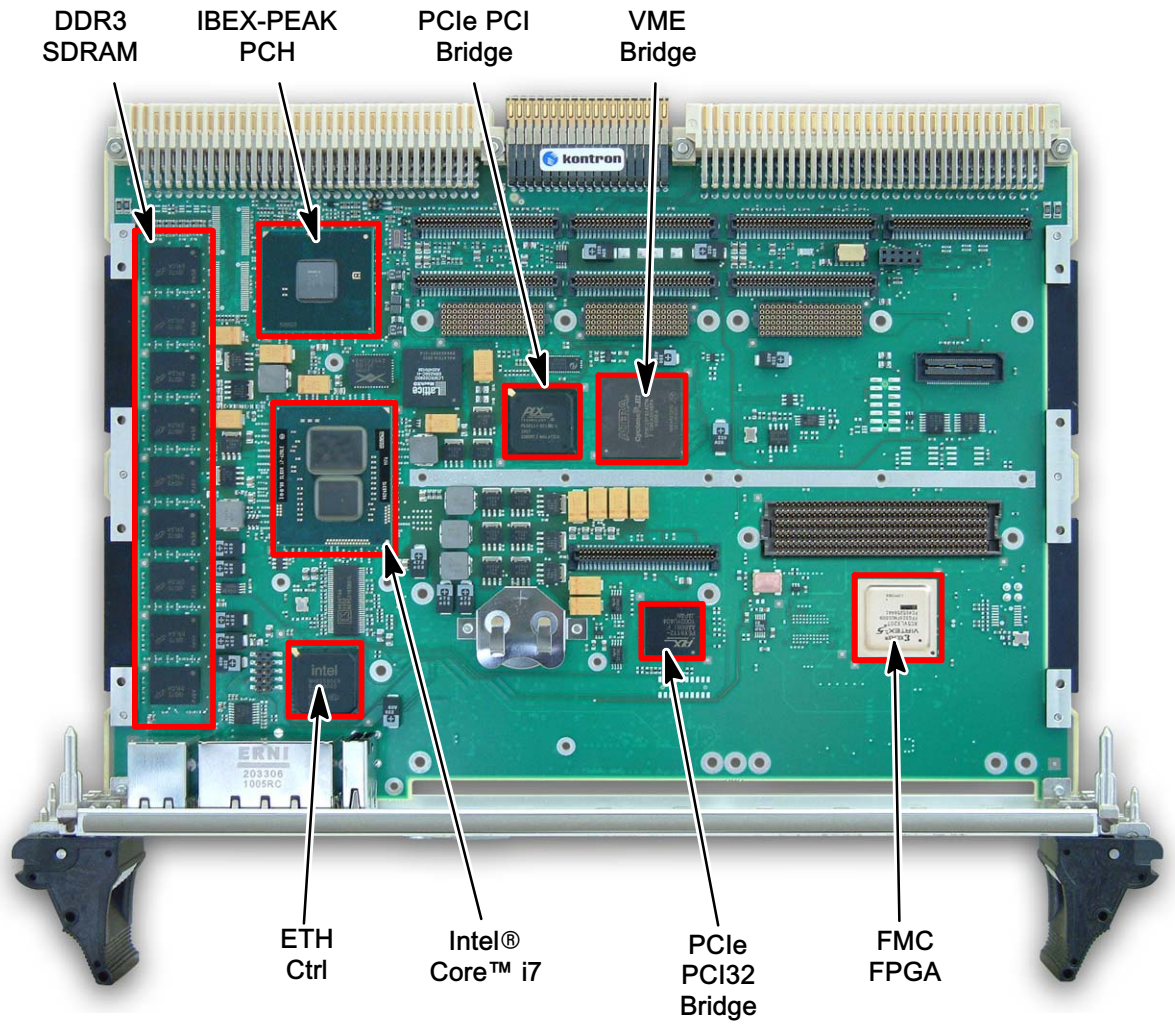


Figure 6: VM6050 Components Layout (Top view)

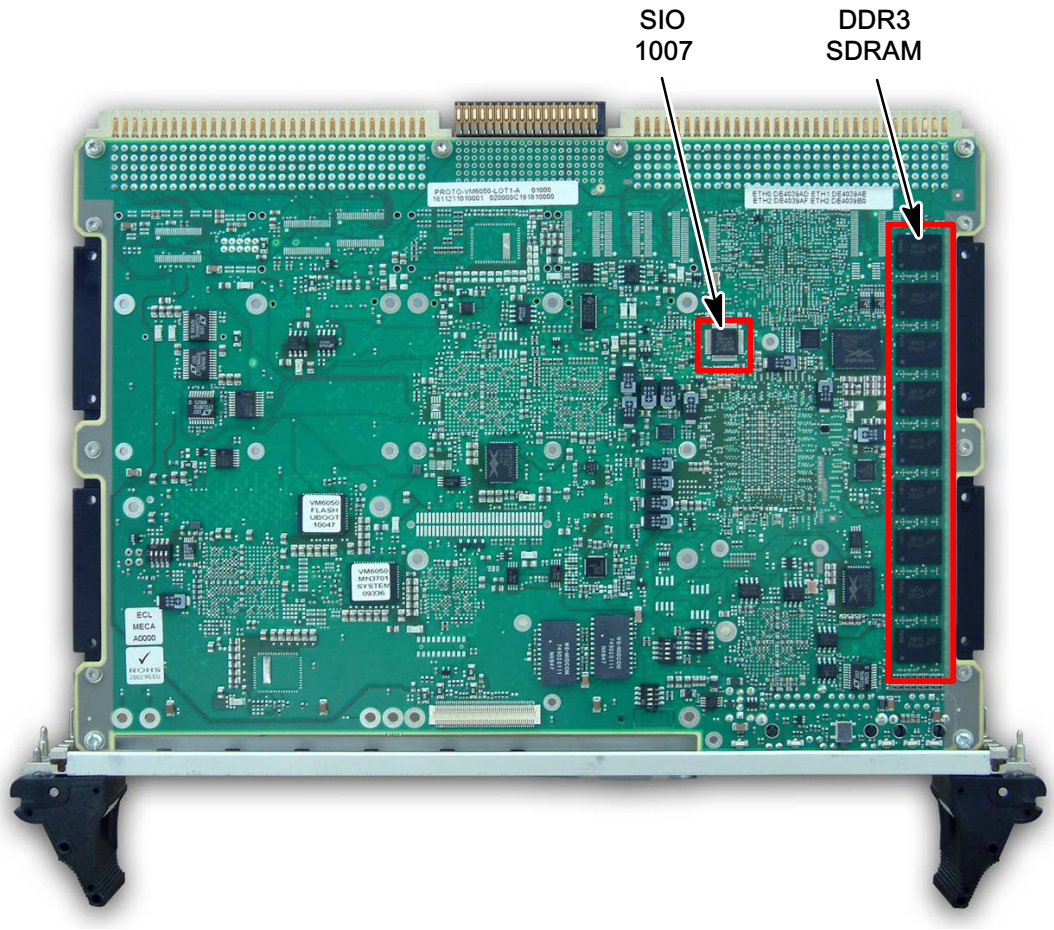


Figure 7: VM6050 Components Layout (Bottom view)

1.2.6 VM6050-WA Specificities

This section sums up the main specificities of the VM6050-WA boards:

» **Environmental Specifications** (see also section 1.3 page 17).

WA **Air-Cooled Extended Temperature**	VITA 47 Conformal Coating	Yes
	Airflow	See Section 5.2.2 page 104 (depending on the processor frequency)
	Temperature VITA 47-Class AC1 VITA 47-Class C1/C2	Cooling Method: Convection Operating: -20°C to +65°C Storage: -45°C to +85°C
	Vibration Sine (Operating) VITA 47-Class V1	2g / 20-500 Hz acceleration / frequency range
	Shock (Operating) VITA 47 - Forced Air Cooled Class	20g / 11ms peak acceleration / shock duration half sine
	Altitude (Operating)	-1,640 to 33,000 ft
	Climatic Humidity	95% non-condensing
	Board Weight	~ 500g

» **Specific tighteners (x2) have been added on the PCB** (see arrows in figure below):

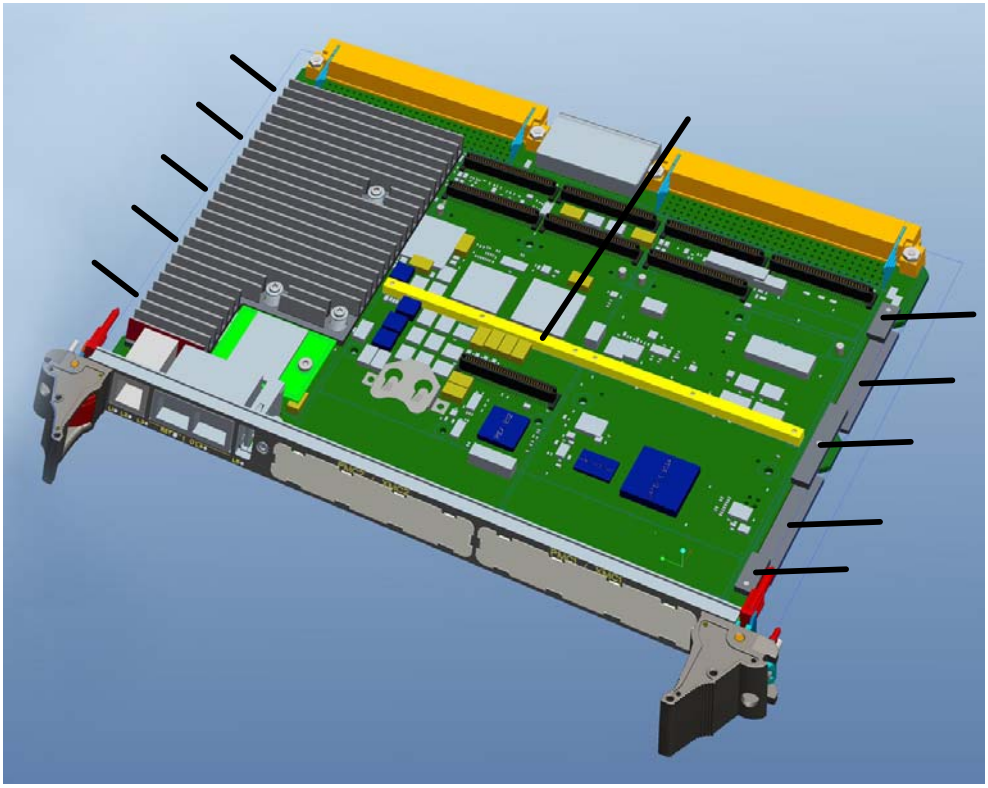


Figure 8: VM6050-WA - Location of the Tighteners

CPU Frequency

The VM6050/WA processor frequency is set to 1.73 Ghz. With this default setting, the VM6050 processing performance is guaranteed across the whole operating temperature range.

Higher Frequency Operation

The processor upper frequency limit can also be set to **2.0 GHz** so as to get increased computing performance. In this case, airflow used to cool the VM6050/WA board should increased to 28 CFM as indicated in Section 5.2 page 103.

This will also keep the dual-core processor outside of its thermal management mode.

To modify the processing frequency, please refer to the section 5.5 “CPU Configuration" of VM6050 AMI-BIOS User Manual (SD.DT.F89).

> **Exceeding the limits will lock the board (without increased airflow)**

Operating the processor at 2.0 GHz and allowing the temperature to reach 65°C is tempting, but the board behaviour cannot be guaranteed. Even if the CPU chip may adapt quickly to the situation with frequency reduction, this shall not be recommanded for other components on the board.

1.2.7 Technical Specification

Form Factor	
Form Factor	6U VME, single slot, 0.8 inch pitch
Processor: Intel® Core™ i7	
Processor	Intel® Core™ i7 -620 LE at 2 GHz 4M cache, 2 execution cores, 4 threads 32-nanometer silicon technology
Cache Structure	32 KB L1, 256 KB L2 per core, 4 MB L3 shared between cores
Memory Controller	Integrated DDR3 memory controller with ECC support, 1067 MT/s on 1066 MHz Two memory channels of 72 bits each
Graphics Core	Integrated Graphics Core
PCI Express Interface	2.5 GT/s gen 1 PCIe 8 lanes PCIe to XMC2 slot or 4 lanes to PCIe/PCI-x Bridge to PMC 8 lanes PCIe to XMC1
DMI Interface	x4 2.5 GT/s point-to-point DMI interface to Platform Controller Hub (PCH).
FDI Interface	Carries display traffic from the integrated graphics controller to the PCH for generation of external display protocols (VGA, DP, ...)
PCH: Ibex Peak-M	
PCI Express Interface	2 lanes PCIe to 1000BASE-T quad Ethernet controller 4 lanes PCIe to VME backplane connector (P0) 1 lane PCIe to PCIe/ PCI bridge to PMC2 and VME bridge 1 lane PCIe to VITA57 FPGA
SPI Interface	Connects to two SPI flash devices (4 MBytes)
LPC	33 MHz LPC, for SuperIO and CPLD connection

SATA	Up to 3 Gb/s integrated Serial ATA host controllers
USB	2 USB 2.0 ports on the P0 rear connectors 2 USB ports on front I/O connector (P8) 1 USB 2.0 port for onboard Flash mezzanine connector 1 front USB 2.0
VGA and DisplayPorts	One VGA port available on front IO connector (P8) Two DisplayPorts or HDMI/DVI available on front IO connector (P8)
Audio Port	High Digital Audio (HDA) port available on front IO connector (P9)
Memory	
System Memory	Up to 8 GB DDR3 SDRAM at 1067 MHz, two memory channels
SPI Flash	Firmware Boot Device
NAND Flash	Up to 16 GB USB Nand Flash storage socket (for USB Nand Flash modules) Up to 32 GB SATA Nand Flash storage Socket
F-RAM	512 Kbit of non volatile ferromagnetic RAM
EEPROM	One serial 256 Kbit EEPROM dedicated to system data One serial 256 Kbit EEPROM dedicated to application data
Onboard Controllers	
Gigabit Ethernet Controller	One i82580 Gigabit MAC/PHY with four 1000BASE-T Ethernet Interface (2 front and 2 rear)
System CPLD	One CPLD Board controller for power sequencing, reset handling, monitoring, failure detection, VME I2C communication. Provides configuration/status registers on LPC interface
SIO	SIO1007 provides two serial lines
VME	ALMA2f VME controller with 2eSST
Onboard Interfaces	
CPU Debug Interface	XDP port for CPU extended debug port connection (only available on a debug connector and need additional test board for XDP access)

Table 5: VM6050 Main Characteristics

1.3 Environmental Specifications

	SA Standard Commercial	WA Extended Temperature	RA Rugged Air-Cooled	RC Rugged Conduction-Cooled
Conformal Coating	Optional	Standard	Standard	Standard
Airflow	2.7 m/s	2.4 m/s	2.8 m/s	NA
Temperature	VITA 47-Class AC1	VITA 47-Class AC2	VITA 47-Class AC3	VITA 47-Class CC4
Cooling Method	Convection	Convection	Convection	Conduction
Operating	0° to +55°C	-20° to +65°C	-40° to +70°C	-40° to +85°C
Storage	-45° to +85°C	-45° to +100°C	-50° to +100°C	-50° to +100°C
Vibration Sine (Operating)	20-500 Hz - 2g	20-500 Hz - 2g	20-2,000 Hz - 3g	20-2,000 Hz - 5g
Random	VITA 47-Class V1	VITA 47-Class V1	VITA 47-Class V2	VITA 47-Class V3
Shock (Operating)	20g/11 ms Half Sine	20g/11 ms Half Sine	20g/11 ms Half Sine	40g/20 ms Half Sine
Altitude (Operating)	-1,500 to 60,000 ft	-1,500 to 60,000 ft	-1,500 to 60,000 ft	-1,500 to 60,000 ft
Relative Humidity	90% without condensation	95% without condensation	95% without condensation	95% without condensation

Table 6: Environmental Specifications

1.4 Mechanical Specifications

Technical Specifications			
	SA Standard Commercial	RA Rugged Air-Cooled	RC Rugged Conduction-Cooled
Board Weight	~450g	~645g	~800g

1.5 MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

VM6050-SAxx-xxxxx and VM6050-WAxx-xxxxx

	GB (Hours)		AIC (Hours)	NS (Hours)		ARW (Hours)
	25°C	40°C	40°C	25°C	40°C	55°C
MTBF (hours)	241 500 h	177 500 h	33 700 h	43 700 h	38 000 h	10 850 h

Table 7: VM6050-SAxx-xxxxx and VM6050-WAxx-xxxxx MTBF Data

VM6050-RAxx-xxxxx

	GB (Hours)			AIC (Hours)		NS (Hours)		ARW (Hours)
	25°C	40°C	55°C	40°C	55°C	25°C	40°C	55°C
MTBF (hours)	292 100 h	295 000 h	-	57 500 h	-	72 400 h	62 600 h	17 100 h

Table 8: VM6050-RAxx-xxxxx MTBF Data

VM6050-RCxx-xxxxx

	GB (Hours)			AIC (Hours)		NS (Hours)		ARW (Hours)
	25°C	40°C	55°C	40°C	55°C	25°C	40°C	55°C
MTBF (hours)	344 800 h	258 400 h	173 400 h	53 500 h	44 300 h	66 600 h	57 100 h	15 400 h

Table 9: VM6050-RCxx-xxxxx MTBF Data

1.6 Related Publications

The following publications contain information relating to this product:

PRODUCT / STANDARD	PUBLICATION
VM6050 Boards	VM6050 Hardware Release Notes CA.DT.A94 VM6050 PBIT User's Guide SD.DT.F88 VM6050 AMI-BIOS User Reference Manual SD.DT.F89 VM6050 Release Notes Fedora14 SD.DT.F82 VM6050 Release Notes VxWorks 6.8 SD.DT.G02
CNET	MIL HDBK 217F, CNET RDF93 and CNET RDF2000 Reliability models
EN	EN55082 and EN55022 Class A Electromagnetic compatibility - Generic immunity standard - Industrial environment - Information technology equipment - Radio disturbances characteristics - Mimits and methods of measuremments
IEEE	IEEE Std 1101.2-1992 IEEE Standard for Machanical Core Specifications for Conduction Cooled Eurocards IEEE P1386-2001 Common Mezzanine Card Family CMC IEEE P1386.1-2001 Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)
Serial ATA	Serial ATA 1.0a Specification
VITA	VITA 1-1994 VME64 Specification VITA 1.1-199x VME64 Extension Draft Specification VITA 35-199x PMC-P4 Pin Out Mapping to VME-P0 and VME64x-P2 Draft Standard VITA 31.1-200x Gigabit Ethernet on VME64x Backplane Draft Standard VITA 20-2000x Conduction Cooled PCI mezzanine Card (CCPMC) VITA 38-2003 System Management on VME VITA 47 Environmental, Design and Construction, Safety, and Quality for Plug-In Units VITA 57 FPGA IO Mezzanine Standard
Underwriters Laboratories	UL94-V0 Standard Physical and environmental Mayers for PCI Mezzanine Cards (PMC)
DisplayPort	DisplayPort V1.1a standard

Table 10: Related Publications

Chapter 2 - Installation

The VM6050 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

2.1 Safety Requirements

The following safety precautions must be observed when installing or operating the VM6050. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Special care shall be taken while handling the board: the heat sink can get very hot during operation. Do not touch the heat sink when installing or removing the board.
In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

This board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:
Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector pins or traces.
- we strongly recommend our customers to work in an environment equipped with anti-static workbenches with professional discharging equipments.

2.2 Board Identification

The VM6050 boards are identified by labels fitted to the bottom side of the board.

Bottom Side

A "Identification" label: Order Code, Serial Number, Variant, E.C. Level

B Ethernet MAC addresses

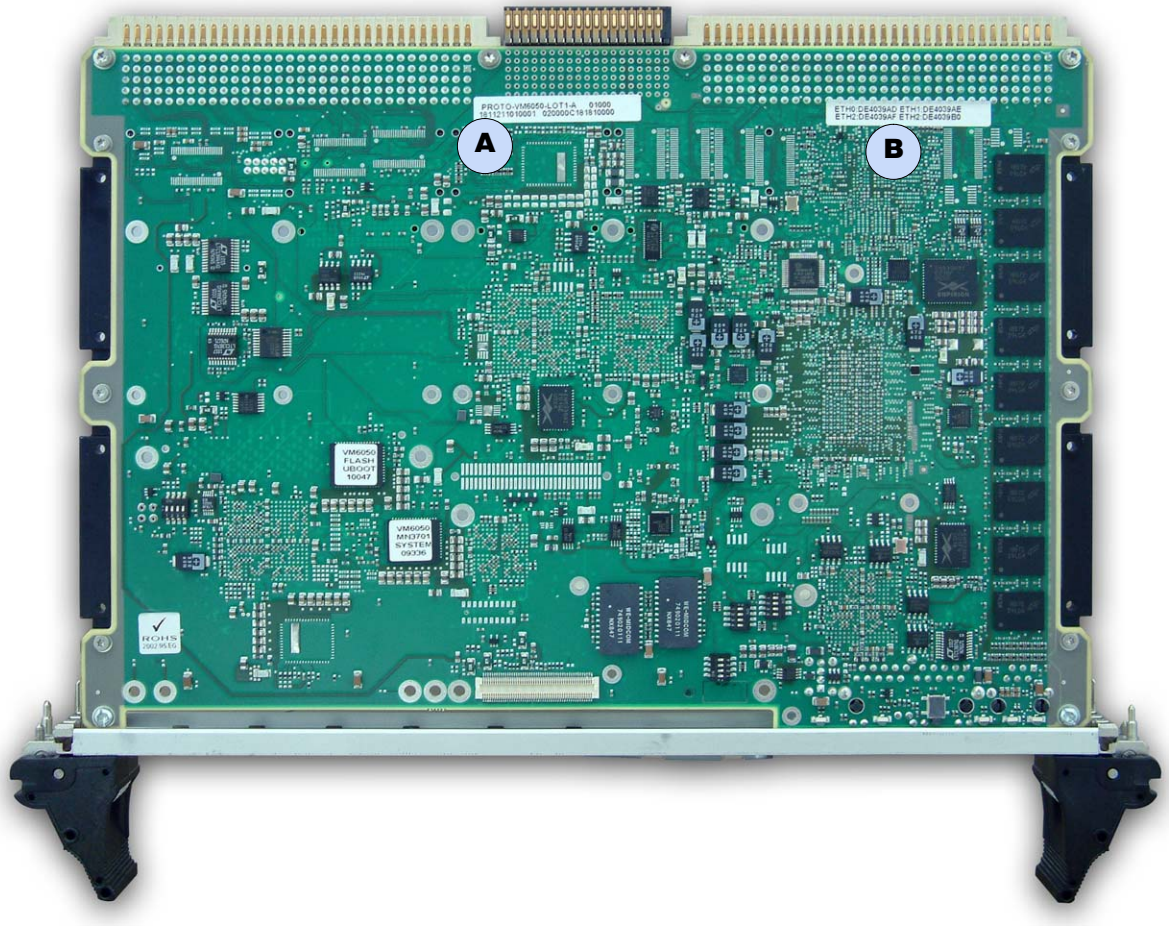


Figure 9: VM6050 Identification (Bottom Side)

See also section “Vital Product Data” in “VM6050 AMI-BIOS User Reference Manual” - SD.DT.F89 to display the VPD information stored in VM6050 EEPROM.

2.3 Package Content

The VM6050 is packaged with several components. The packing contents of the VM6050 Series may vary depending on customer requests.

- CPU Module:
  - Order Code: refer to section 1.2.3 “Order Code Table” :
    - Processor specifications differ depending on Order Code.
    - Heat sink assembled on the board.
    - Battery assembled on the board
  - Serial adaptation cable RJ-12 <-> DB-9 (Order Code: refer to section 1.2.3 “Order Code Table”)
- PMCs Carrier
  - Order Code: V2PMC2-*xx*
- Rear Transition Module:
  - Order Code: refer to section 1.2.3 “Order Code Table”.
- USB Flash Disk Module:
  - Order Code: refer to section 1.2.3 “Order Code Table”.
- CD-ROM - Technical Documentation.
- Graphic Module
  - Order Code: refer to section 1.2.3 “Order Code Table”.
- Graphic PIM
  - Order Code: refer to section 1.2.3 “Order Code Table”.
- FMC Mezzanine Cards
  - Order Code: refer to section 1.2.3 “Order Code Table”.

2.4 Board Configuration

Jumper

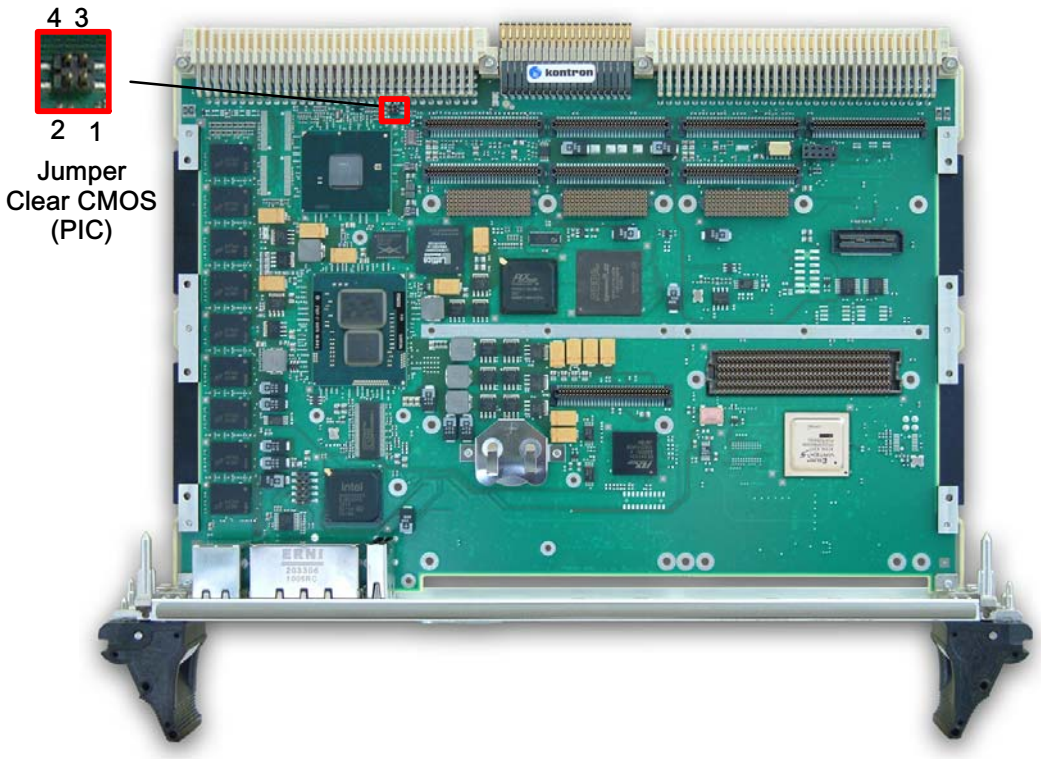
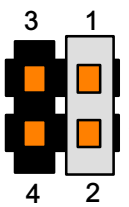


Figure 10: VM6050 Board Configuration (Top view)

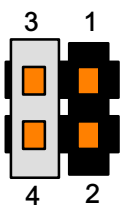
Two jumpers are available on the VM6050 :

- Clear CMOS
- Secondary RTC Reset

Pin	Description
1	GND
2	Clear CMOS
3	GND
4	Secondary RTC Reset



Clear CMOS
Activated



Secondary RTC
Reset Activated

Microswitches

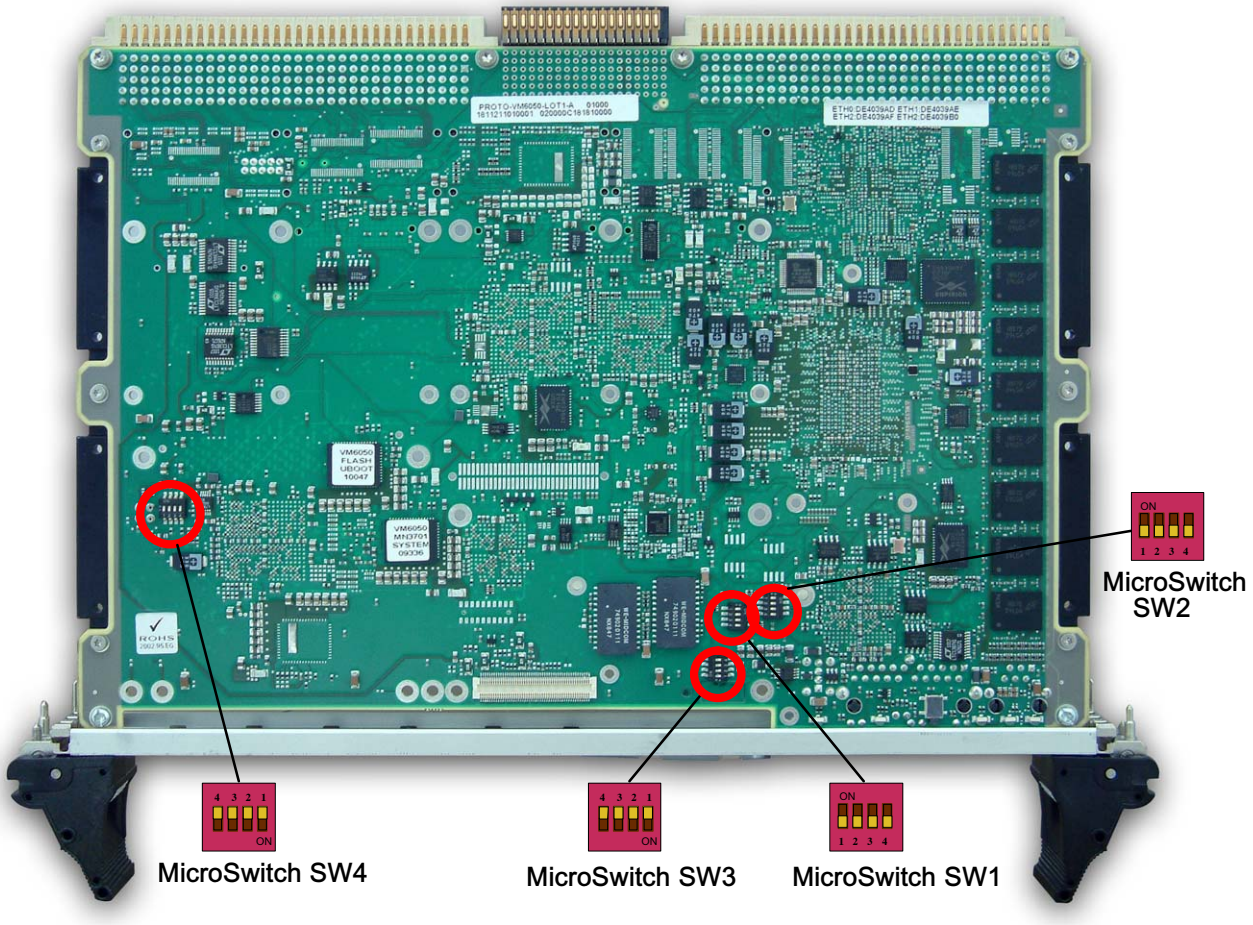


Figure 11: VM6050 Board Configuration (Bottom view)

Four 4-bit microswitches are available on the VM6050: SW1, SW2, SW3 and SW4

2.4.1 Microswitch SW1 Description

Function	Description
1 - Factory Test Mode	**on**: factory test mode is selected **off**: normal operation
2 - VPD (Vital Product Data) EEPROM write protect	**on**: VPD 32Kx8 EEPROM is write protected **off**: VPD 32Kx8 EEPROM is not write protected unless signal NVMRO is active (logic 1)
3 - System (base software parameters) EEPROM write protect	**on**: System 32Kx8 EEPROM is write protected **off**: System 32Kx8 EEPROM is not write protected unless signal NVMRO is active (logic 1)
4 - FRAM (Ferro Magnetic RAM) write protect	**on**: 64Kx8 User FRAM is write protected **off**: 64Kx8 User FRAM is not write protected whatever the level of the NVMRO signal

Table 11: Microswitches SW1

2.4.2 Microswitch SW2 Description

Function	Description
1 - Rescue Boot Flash	**on**: CPU boots the BIOS from its rescue flash. **off**: Normal operation. CPU boots the BIOS from its non rescue flash.
2 - Reserved	
3 - CPU performance limitation	**on**: CPU speed forced to 1.2GHz. **off**: Normal operation.
4 - Reserved	

Table 12: Microswitches SW2

2.4.3 Microswitch SW3 Description

Function	Description
1 - Reserved	
2 - Reserved	
3 - Reserved	
4 - SPD debug mode	**on**: DDR3 SPD debug mode **off**: normal operation

Table 13: Microswitches SW3

2.4.4 Microswitch SW4 Description

Function	Description
1 - VITA 57 FPGA user EEPROM write protect	**on**: VITA 57 FPGA flash is not write protected **off**: VITA 57 FPGA flash is write protected
2 - VITA 57 FPGA rescue EEPROM write protect	**on**: VITA 57 FPGA rescue flash is not write protected **off**: VITA 57 FPGA rescue flash is write protected
3 - JTAG/SPI access selection	**on**: JTAG access mode is selected **off**: SPI access mode is selected
4 - VITA 57 FPGA rescue EEPROM selection	**on**: Rescue image is downloaded in FPGA VITA 57 **off**: Normal operation - Default image is downloaded in FPGA VITA 57

Table 14: Microswitches SW4

2.5 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the VM6050 in a system. Procedures for standard removal operations are found in their respective chapters.

To perform an initial installation of the VM6050 in a system proceed as follows:

1. Ensure that the safety requirements indicated in Section 2.1 are observed.

Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the VM6050 refer to Chapter 5. For the installation of VM6050 specific peripheral devices and Rear I/O devices refer to the appropriate sections in current Chapter.

Care must be taken when applying the procedures below to ensure that neither the VM6050 nor other system boards are physically damaged by the application of these procedures.

3. To install the VM6050 perform the following:
    1. Ensure that no power is applied to the system before proceeding.

When performing the next step, DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

    2. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.
    3. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
    4. Fasten the front panel retaining screws.
    5. Connect all external interfacing cables to the board as required.
    6. Ensure that the board and all required interfacing cables are properly secured.

The VM6050 is now ready for operation. For operation of the VM6050, refer to appropriate VM6050 specific software, application, and system documentation.

2.6 Standard Removal Procedure

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Section 2.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

Care must be taken when applying the procedures below to ensure that neither the VM6050 nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.
5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

7. Dispose of the board as required.

2.7 Installation of Peripheral Devices

The VM6050 is designed to accommodate a variety of peripheral devices whose installation varies considerably. The following chapters provide information regarding installation aspects and not detailed procedures.

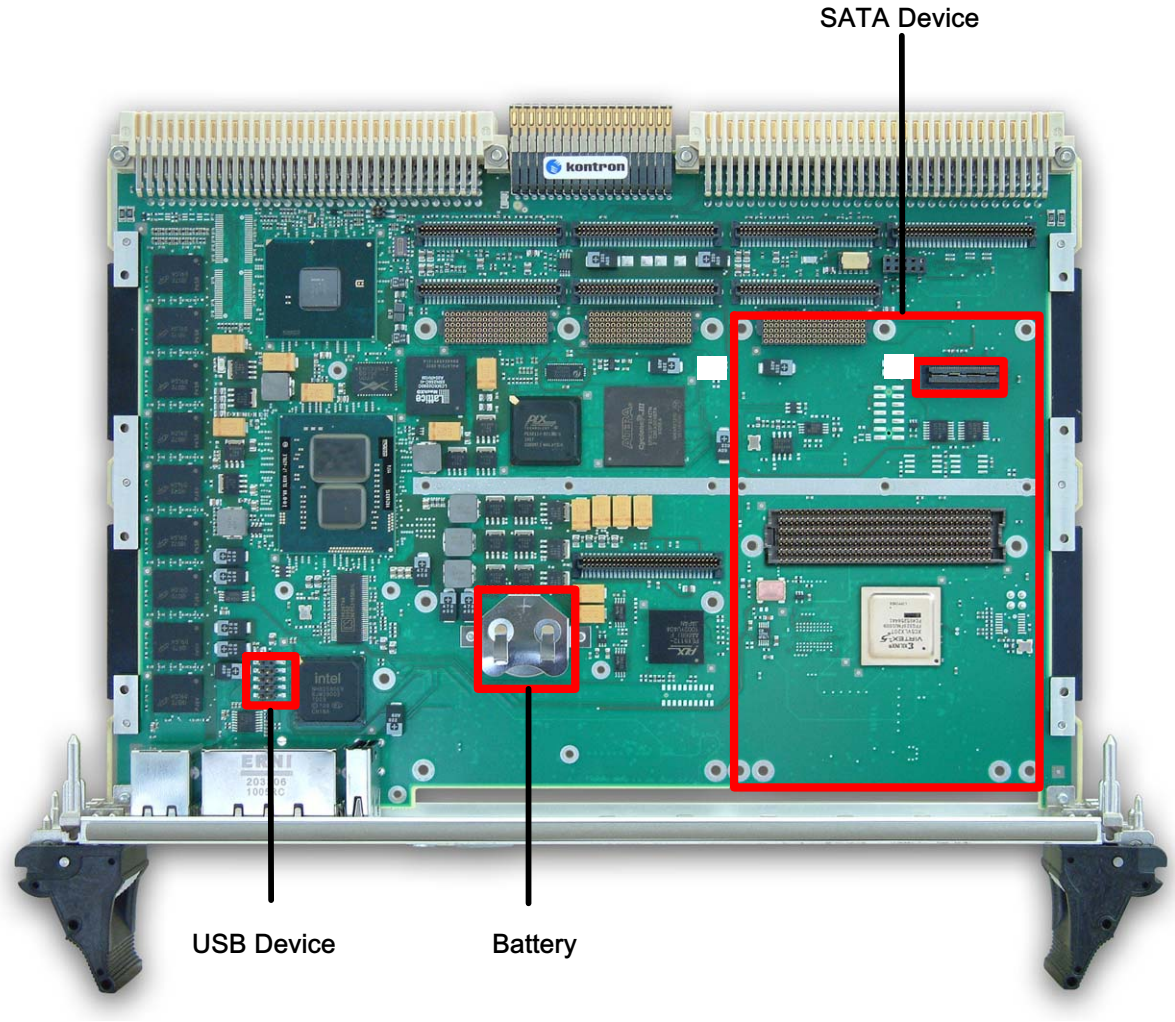


Figure 12: Onboard Devices

2.7.1 USB/SATA Flash Device Installation

The onboard USB device is used to connect an USB Flash Disk.

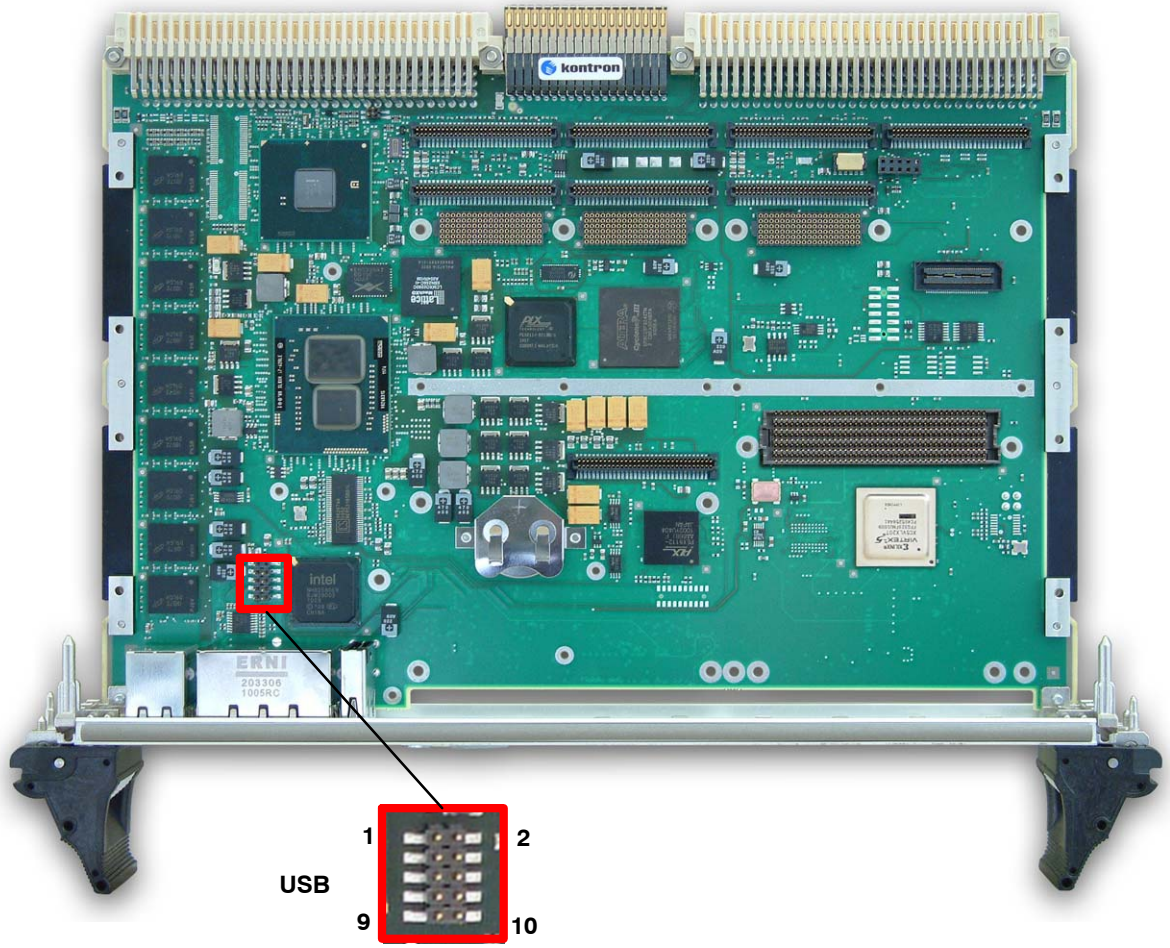


Figure 13: USB/SATA Mezzanine Slots Location

The USB/SATA Flash module is fixed to the board, by using on one side the USB/SATA connector, and on the other side, a standoff screwed to the VM6050 board and to the USB/SATA flash module.

Order Code of the USB/SATA flash disk:

Refer to section 4.2.1 page 65.

> USB/SATA Mezzanine Bulk

- The maximum space reserved for USB flash disk is 36.9 mm x 26.6 mm (LxW)
- The distance between the connector and the screw hole is 27.3 mm~27.9mm
- The maximum allowable connector height is 3.68 mm

> USB Flash Disk Overview

USB flash disk is a standard USB module board compatible with the USB 2.0. It is available in sizes up to 8 GB, commercial or industrial temperature range. USB flash drive feature sustained read speeds of up to 35 MB/s, write speeds up to 15 MB/s.

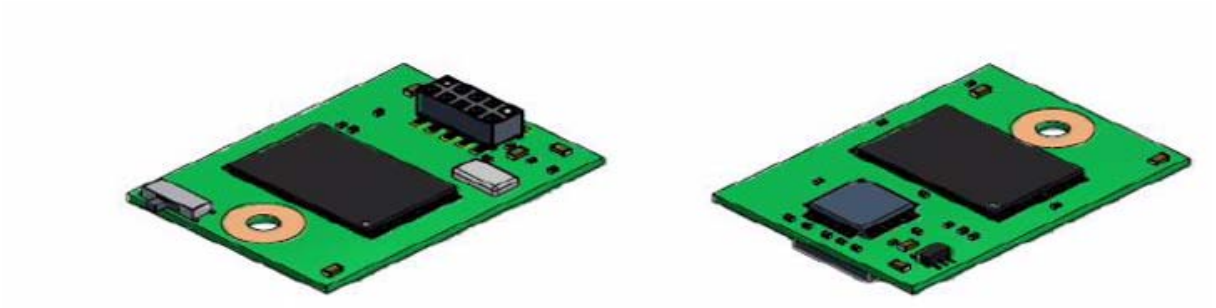
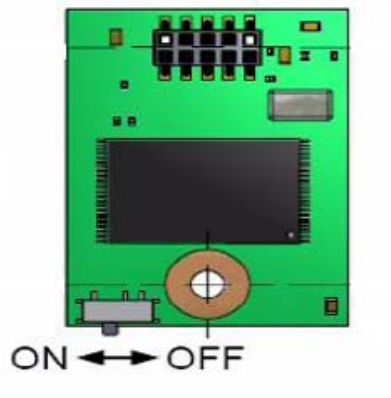


Figure 14: USB Flash Disk Overview

USB flash disk supports write protect feature. Write protect switch is available on module board as shown in the following figure.



> SATA Flash Disk Overview

SATA flash disk is available in sizes up to 64 GB, commercial or industrial temperature range. SATA flash drive feature sustained read speeds of up to 70 MB/s, write speeds up to 20 MB/s.

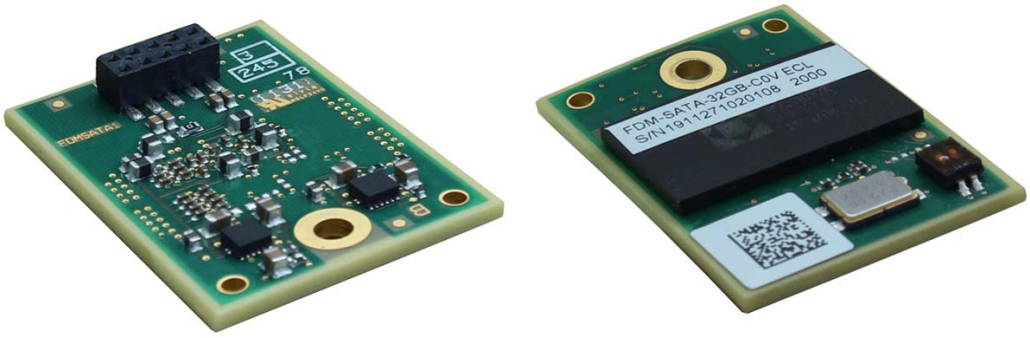


Figure 15: SATA Flash Disk Overview

- Microswitch description for SATA flash disk.

Function	Description
1 - Write Protect	**on**: SATA Flash is write protected **off**: Normal operation
2 - RSVD	

2.7.2 Serial ATA Extension Module

A Serial ATA Extension Module with up to 120 GB SATA HDD may be connected to the VM6050 via the onboard connector PI503.

- This module must be installed only on the VM6050 boards that support the SATA Kit Disk (Order code: KIT-DISK25-SATA)
- Contact Kontron for SATA onboard option on VM6050-RC boards.

If not already done, the SATA extension module must be physically installed on the VM6050 prior to installation of the VM6050 in a system.

Figure 16: SATA Extension Module: front and Bottom Viewes

The SATA extension module (order code: KIT-DISK25-SATA or KIT-DISK18-SATA) is made up of:

- 1 plate fitted with SATA connectors
- 4x screws CZX-M3X5-INOX
- 4x screws CZX-M2.5X5-INOX

Installation process (if not already done):

1. Insert the SATA disk in the SATA connector. Example of SATA disk validated:
   - Manufacturer: Western Digital
   - Part No: SSD-D0015SI-5000
2. Fix the SATA disk to the plate using the four screws CZX-M3X5-INOX. Use medium strengh threadlocker (recommended torque of 0.4 Nm).
3. Plug the kit (plate and disk) on the VM6050 board, SATA connector (P5)
4. Fix the kit to the VM6050 board using the four screws CZX-M2.5X5-INOX. Use medium strengh threadlocker (recommended torque of 0.3 Nm).

2.7.3 Battery Replacement

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Make sure not to remove the battery support, this could damage the heatsink.

To replace the battery, proceed as follows:

- Turn off power.
- Remove PMC/XMC or graphic module if fitted (refer to section 2.8 page 36 or 2.9 page 42.
- Use a thin plastic tool to push the battery outside the safety cache. Push from the right or left top side of the safety cache.
- Remove the battery.
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

Care must be taken to ensure that the battery is correctly replaced.

The battery should be replaced only with an identical or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Reference of the battery used on the VM6050: RAYOVAC BR2032/BN

The design of an electronic circuit powered by a component class battery requires the designer to consider two interacting paths that determine a battery's life: consumption of active electrochemical components and thermal wear-out.

Battery Life

CPU RTC consumption is close to 6 µA at 25°C (PCH specifications). BR2032 battery life on VM6050 at 25°C ambient temperature may reach 195 mAh/6 µA= 32500h= 3.7 years, without stand-by any power.

Figure 17 gives an estimate of years of service at various discharge currents for BR Lithium coin cells at room temperatures.

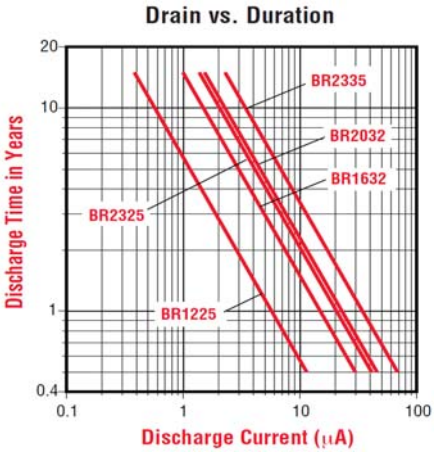


Figure 17: Battery Life

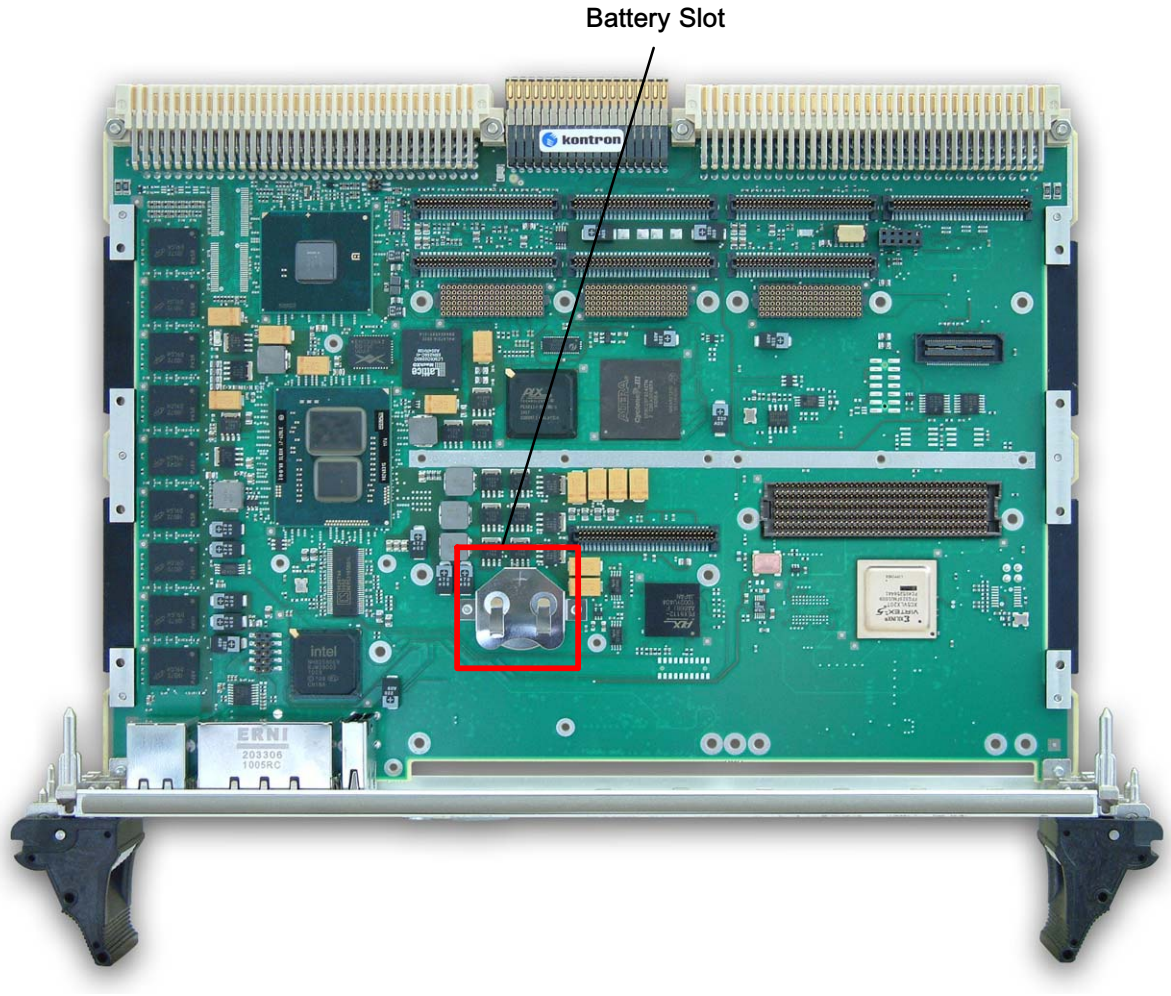


Figure 18: Battery Slot

Battery Use

BR2032 batttery is used to save the date and the hour parameter of internal IBEX PEAK RTC. See also chapter 3.1 page 44. BIOS parameter are saved on system flash EEPROM.

2.8 PMC / XMC / FMC Installation

» PMC Installation

PMC modules are delivered with a full kit of parts for mounting them, and the user guide for the module normally contains instructions on how to fit the module.

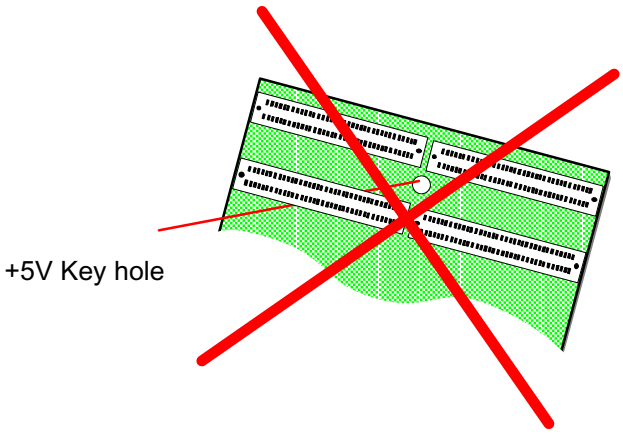
The installation of the PMC on the VM6050 conforms to the IEEE P1386.1 standard.

To install the XMC/PMC module, refer to Figure 19 to Figure 23 and follow the steps below:

To avoid ESD damage, wear an antistatic wrist strap to discharge static electricity while performing any part of the installation that involves touching the VM6050 board or the XMC/PMC.
If you can't wear an antistatic wrist strap, touch one hand to the bare metal surface to provide grounding.

1. Place carefully the VM6050 with the backplane connectors facing you on a static dissipative surface connected to a common ground by a low-resistance connection. Do not slide the board over any surface.
2. Remove the blanking plate from the appropriate XMC/PMC slot of the VM6050.
3. Check that the standoffs are attached to the XMC/PMC.
4. Install the XMC/PMC, component-side down, aligning the PCI connectors with their mating connectors on the VM6050 and the XMC connector if available. Press them together so that the friction from the pins holds them together. Insert the standoff plug mounted on the VM6050 into the keyhole. The module's bezel will fill the slot and provide a connection to the module.

   PMC slot are not VIO 5V tolerant, make sure not to insert a +5V PMC on the board. Failture to observe this restriction may result in damage to the PMC or the VM6050.



5. Screw the XMC/PMC in place using the 4 mounting points, on the bottom side of the VM6050 . You need a Phillips screwdriver for this stage.
6. The XMC/PMC attachment is now complete.
7. Insert the VM6050 into the chassis making sure it is plugged into the backplane.

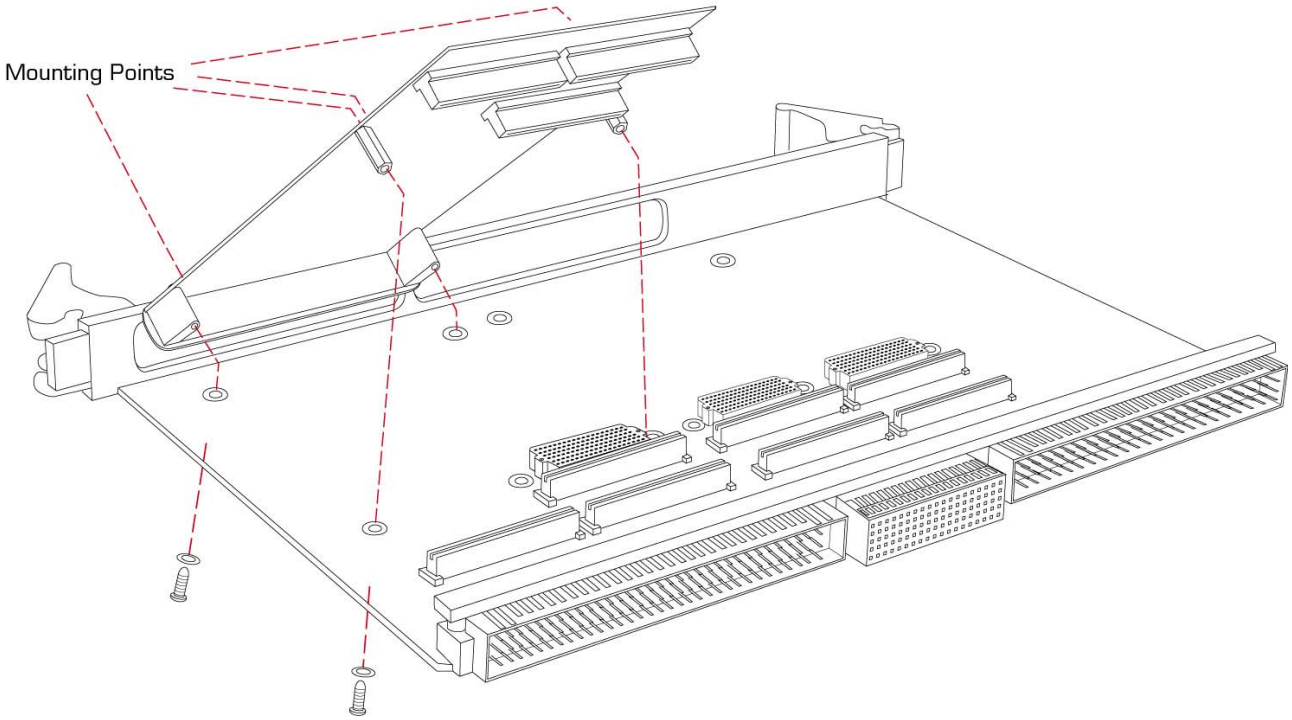


Figure 19: PMC Installation on PMC Site 1

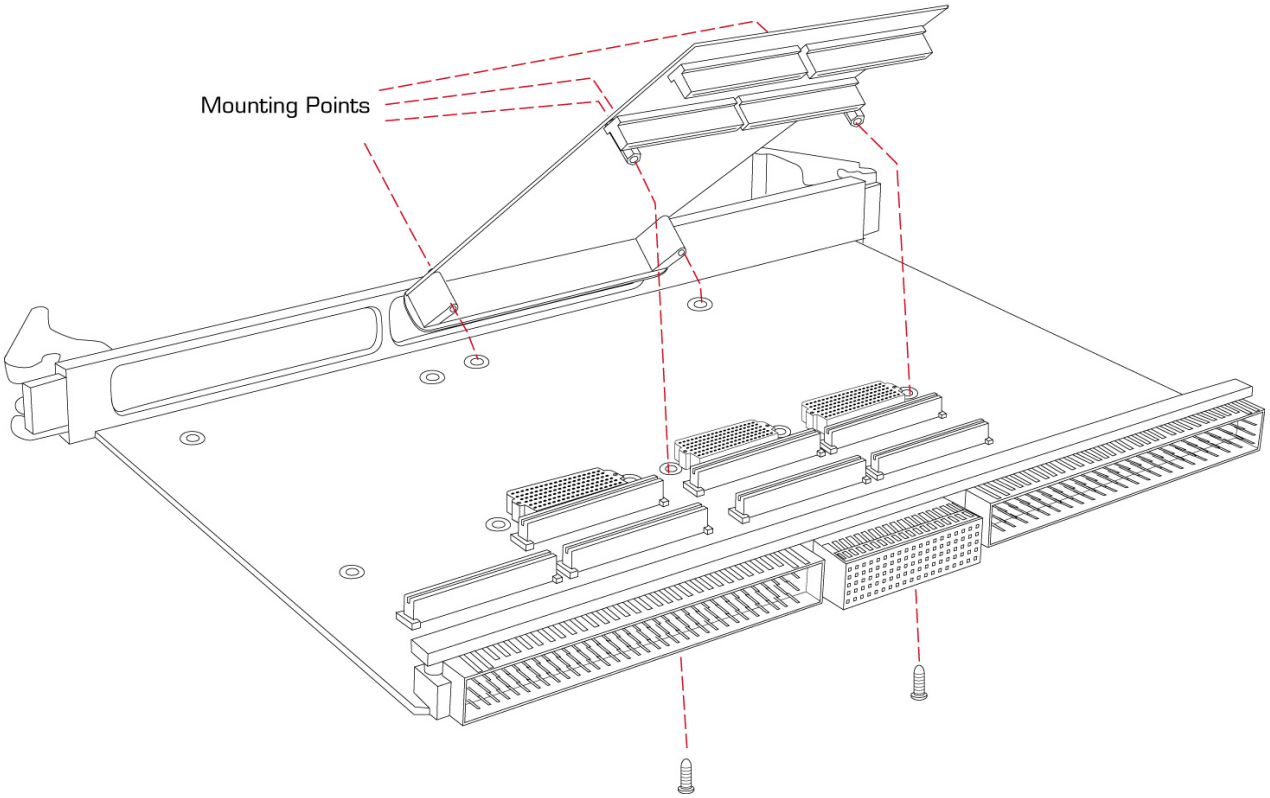


Figure 20: PMC Installation on PMC Site 2

XMC Installation

The XMC board standard is based on the PMC mechanical definition, and occupies the same board area.

The XMC board add one new connector to the connectors already on a PMC. The new connectors support high-speed differential signals for fabric communications.

Figure 21 shows a XMC fitted only with the XMC connector.

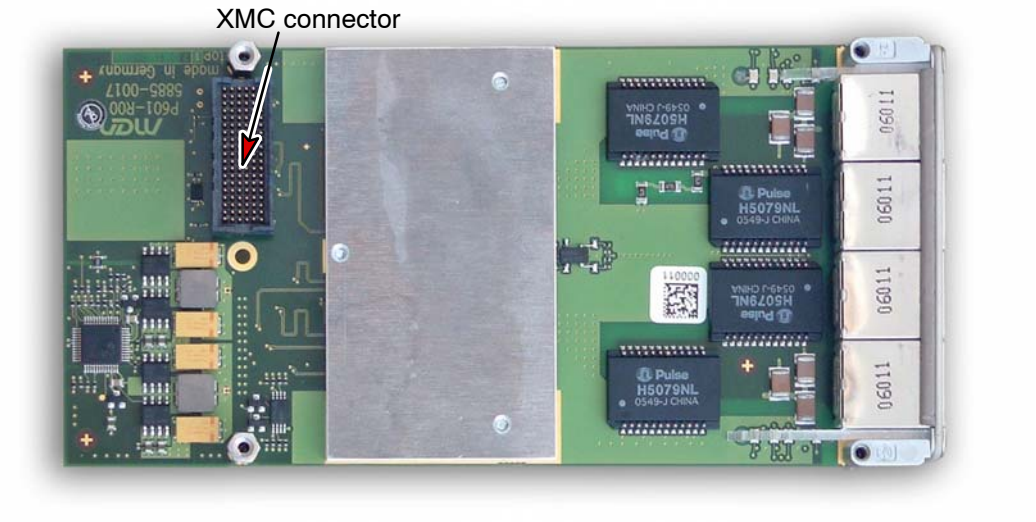


Figure 21: Example of XMC Board

Figure 22 shows a XMC installation on the PMC Site 1.

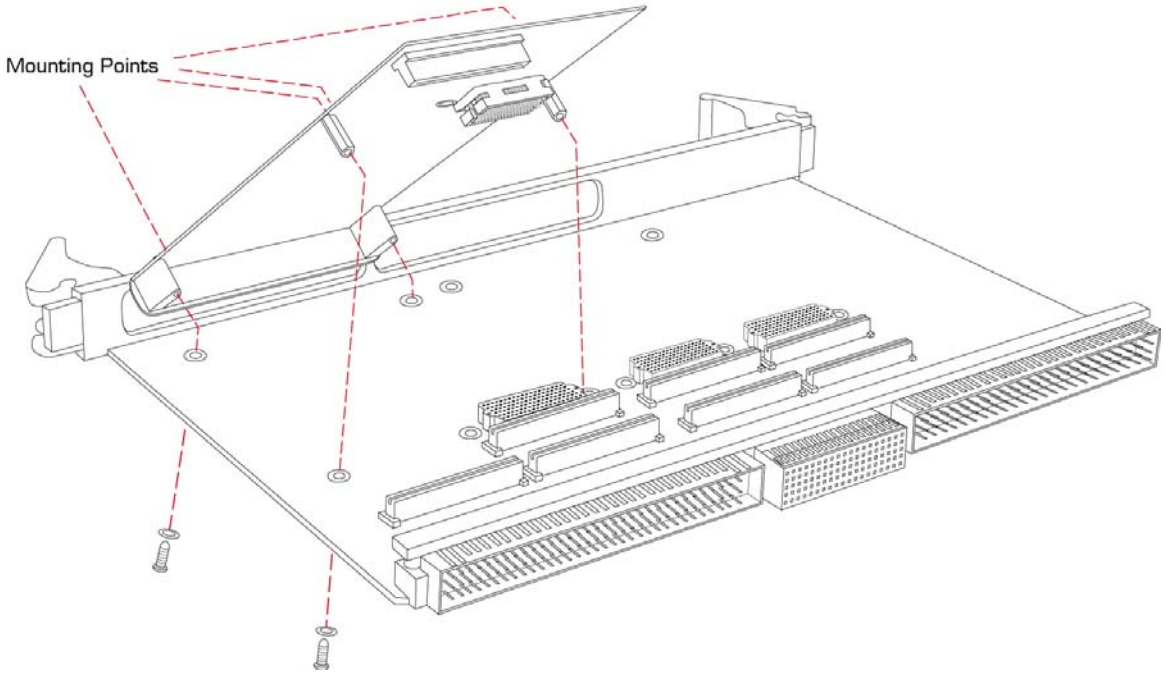


Figure 22: XMC Installation on PMC Site 1

Figure 23 shows a XMC installation on the PMC Site 2.

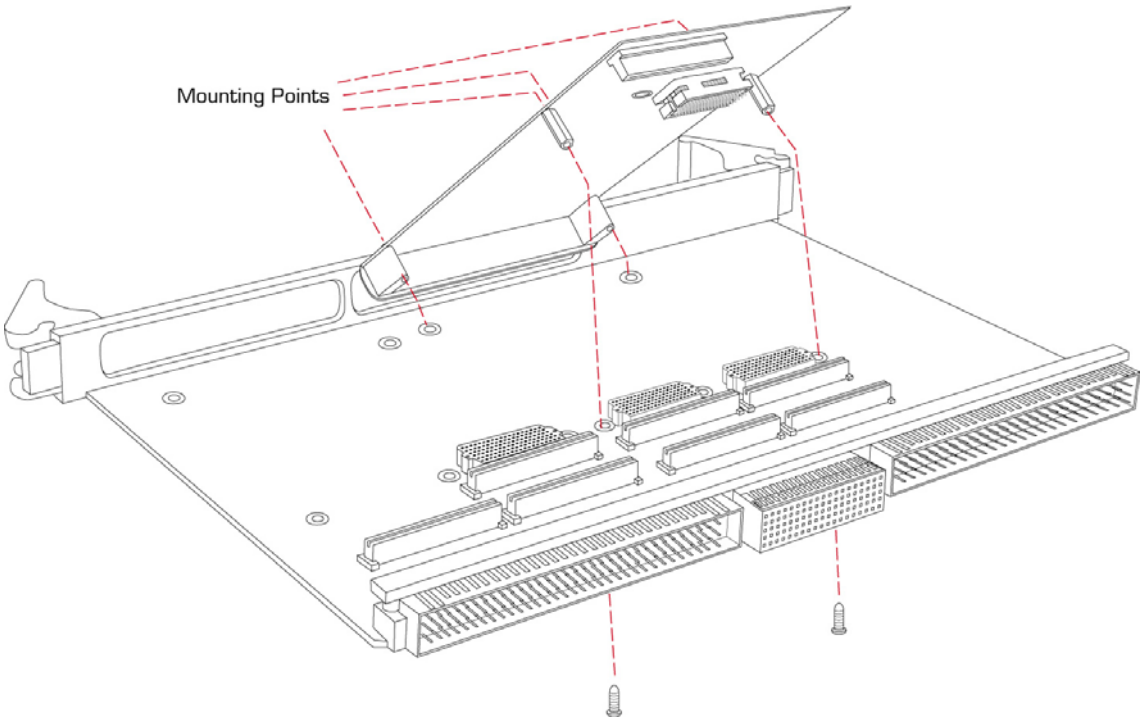
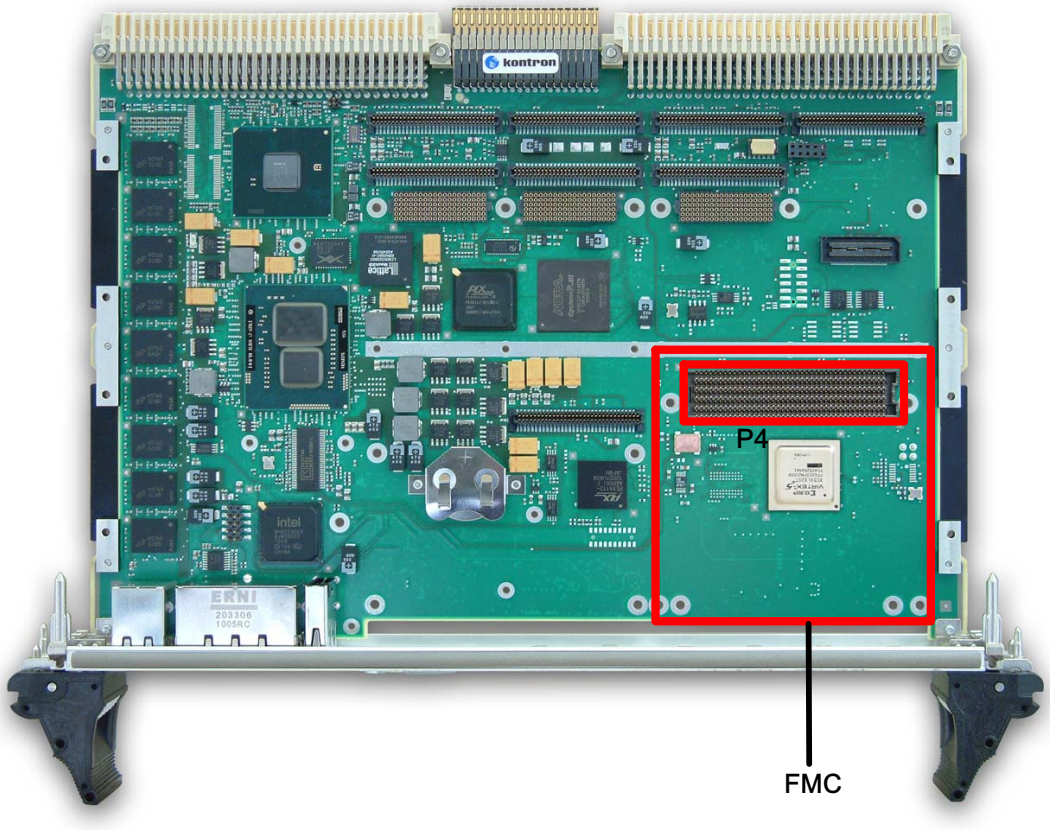


Figure 23: XMC Installation on PMC Site 2

FMC Installation



FPGA Mezzanine Card, or FMC, as defined in VITA 57, provides a specification describing an I/O mezzanine module with connection to an FPGA or other device with reconfigurable I/O capability.

The FMC mezzanine module uses a high-pin count 400 pin high-speed array connector, HPC.

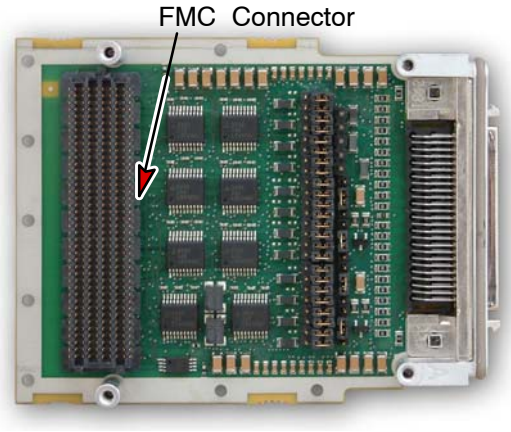


Figure 24: Example of FMC Board

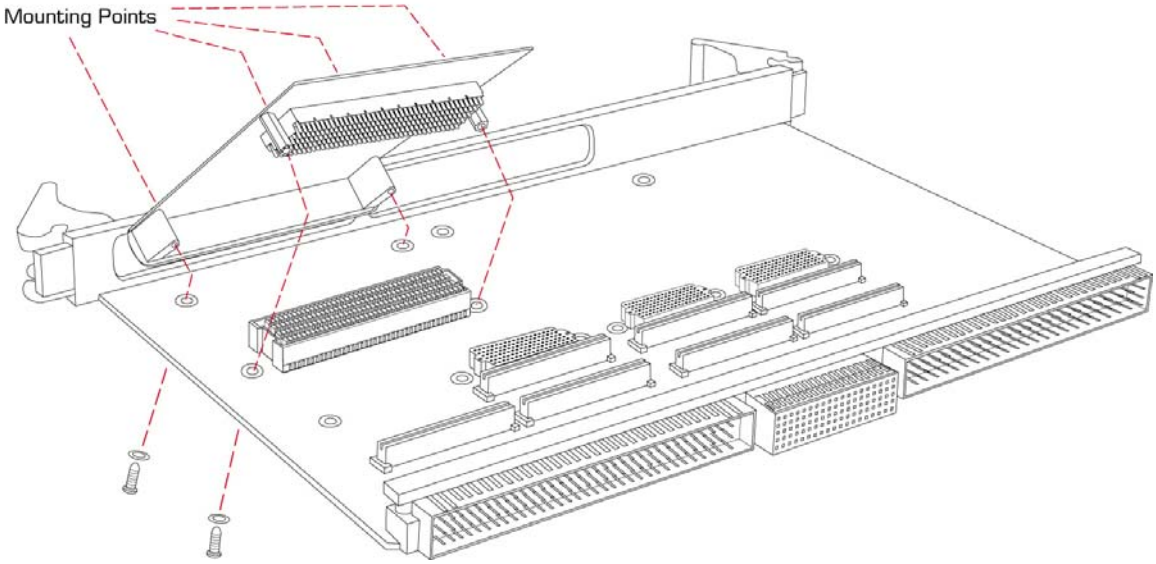


Figure 25: FMC Installation on FMC Site

The installation of the FMC on the VM6050 conforms to the ANSI/VITA 57.1 standard.

To install the FMC module, refer to Figure 25 and follow the steps below:

To avoid ESD damage, wear an antistatic wrist strap to discharge static electricity while performing any part of the installation that involves touching the VM6050 board or the XMC/PMC.
If you can't wear an antistatic wrist strap, touch one hand to the bare metal surface to provide grounding.

1. Place carefully the VM6050 with the backplane connectors facing you on a static dissipative surface connected to a common ground by a low-resistance connection. Do not slide the board over any surface.
2. Remove the blanking plate from the FMC slot of the VM6050.
3. Check that the standoffs are attached to the FMC.
4. Install the FMC, component-side down, aligning the FMC connectors with their mating connectors on the VM6050 and the XMC connector if available. Press them together so that the friction from the pins holds them together. Insert the standoff plug mounted on the VM6050 into the keyhole. The module's bezel will fill the slot and provide a connection to the module.
5. Screw the FMC in place using the 4 mounting points, on the bottom side of the VM6050 . You need a Phillips screwdriver for this stage.
6. The FMC attachment is now complete.
7. Insert the VM6050 into the chassis making sure it is plugged into the backplane.

2.9 Graphic Module Installation

The Graphic Module is based on the PMC mechanical definition and occupies the same board area.

The Graphic Module board adds one new PMC connector. This new connector supports a graphic interface as two DisplayPort interfaces and one VGA interface.

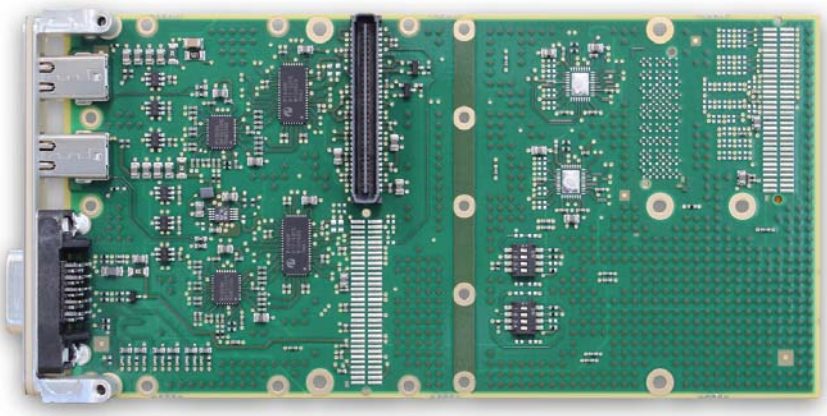


Figure 26: Graphic Module Overview

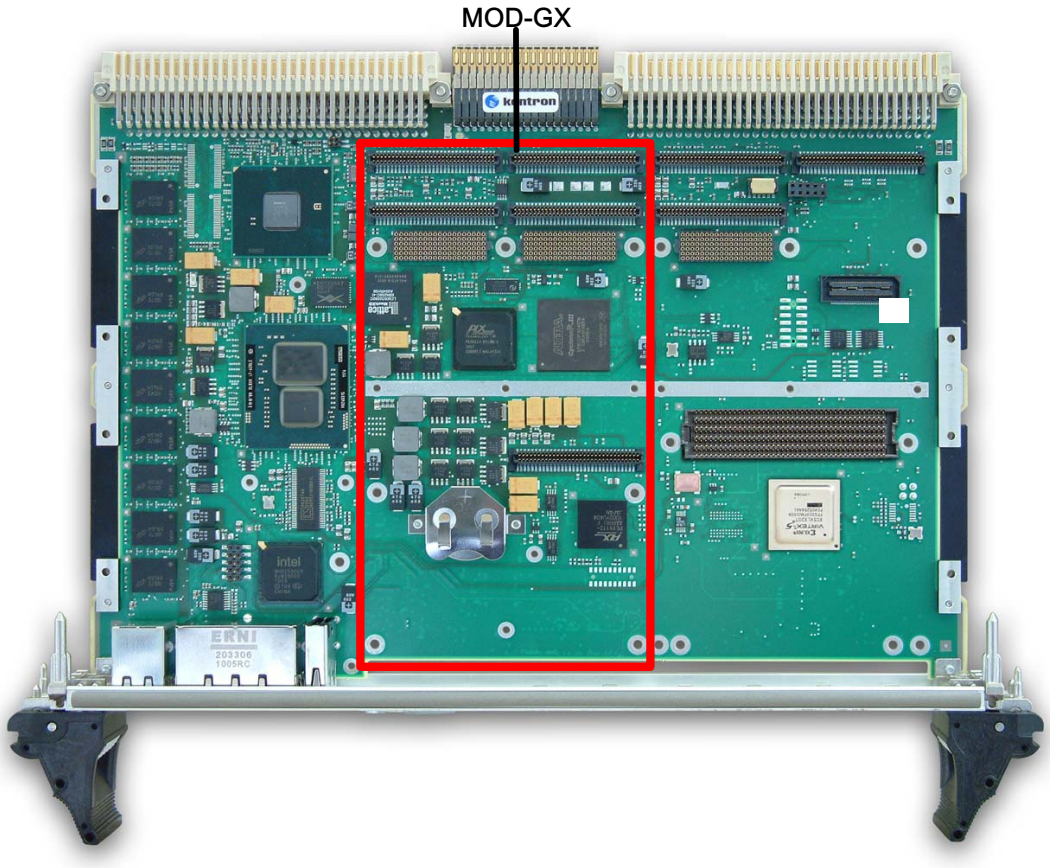


Figure 27: Graphic Module Location

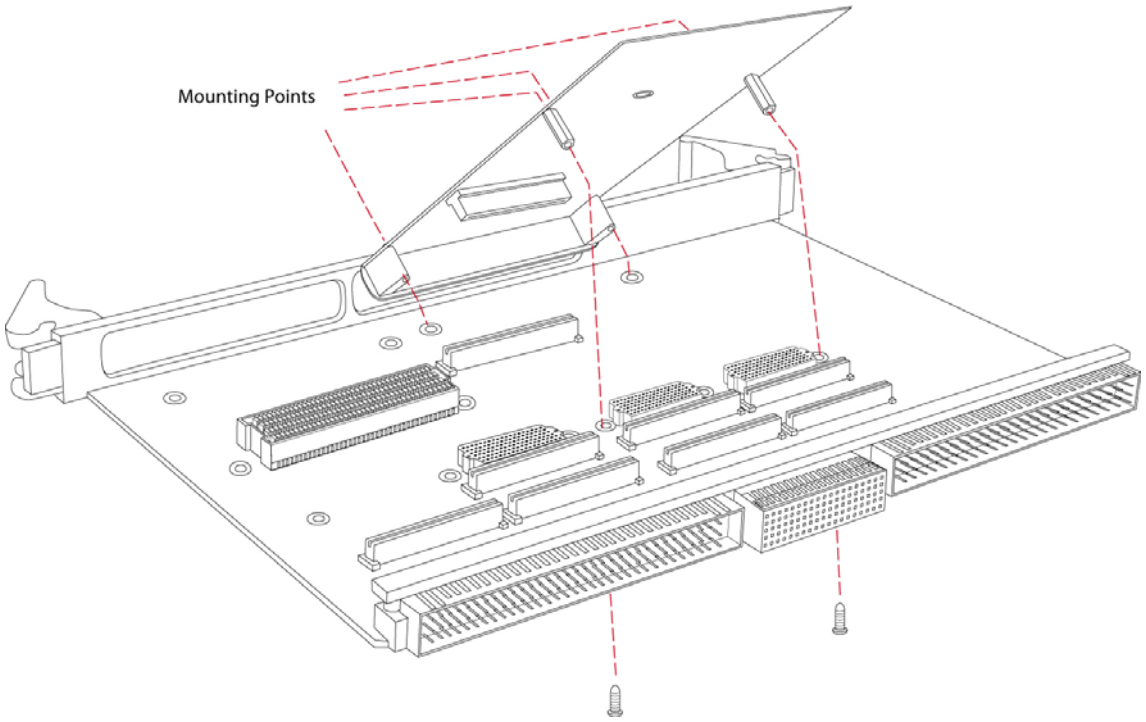


Figure 28: Graphics Module Installation

2.10 Software Installation

The installation of all onboard peripheral drivers is described in detail in the relevant Driver Kit files or Board Support Packages (BSP).

The installation of an operating system is dependent of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.

Chapter 3 - Additional Board Features

3.1 RTC, Watchdog, Timers

3.1.1 Real-Time Clock (RTC)

The following real time clocks are available on the VM6050 board.

- Real-Time Clock (RTC)

  The VM6050 is equipped with an onboard high-precision real-time clock. This real-time clock operates at very low power consumption. The standard equipment of the VM6050 includes a battery. The RTC is powered during the presence of the 5V standby or 5V power or the battery.

- Hardware delay timer for short reliable delay times

  The internal RTC of the IbexPeak PCH is used for the VM6050.

  IbexPeak Time keeping features two banks of static RAM with 128 bytes each. Three interrupts are available.

  The RTC can be powered by an optional battery, with a minimum 3 years lifetime at 25°C.

  The SBC can operate without the use of battery: CMOS memory and RTC will then not be preserved during the absence of power.

- Real Time Clock (RTC) stability:

  PCH offers internal RTC feature. This RTC stability depends on an external 32.768 KHz oscillator. This external oscillator (FC-135 family) has a parabolic coefficient of 0.4 ppm/°C² and +/-20 ppm stability at 25°C. At first rate, only considering external oscillator parameters, PCH RTC stability for ambient temperature is 20ppm at 25°C. 20 ppm stability is equivalent to 10 mn/year, worse case.

3.1.2 Watchdog Timer

The timer is enabled by software. Once enabled it must be restarted at regular intervals. If it is not restarted the timer will expire and cause a Non-Maskable Interrupt (NMI) or reset to the local processor. Failure to trigger the Watchdog Timer in time results in an interrupt or a system reset.

3.1.3 CPLD Watchdog

The PLD includes a hardware Watchdog timer that can be used by the operating software to monitor the normal operation of the system.

The timer is enabled by software. Once enabled it must be restarted at regular intervals. If it is not restarted the timer will expire and cause a Non-Maskable Interrupt (NMI) or reset to the local processor.

The Watchdog module uses a slow clock and it is composed of the following features:

- Watchdog refresh function
- Clear watchdog register when reset occurs
- Watchdog timeout decoder:

The timer timeout is programmable ranging from 1s to 510s by 2s steps in the Watchdog Timer Control register

- Watchdog expiration mode management:

The expiration mode is chosen in the Watchdog Timer Control register.

There are 3 expiration modes:

a. Timer only mode

b. Reset mode

c. Interrupt mode

3.2 I2C Structure

Each CPU subsystem features three I2C busses.

> The first one is attached to the PCH Platform Hub Controller and controls the DDR3 SPD EEPROM, the CK505 clock generator and, for CPU only, the card Voltage monitoring device.

> The remaining i2C busses are handled by the CPLD device according Figure 29 “I2C Diagram”.

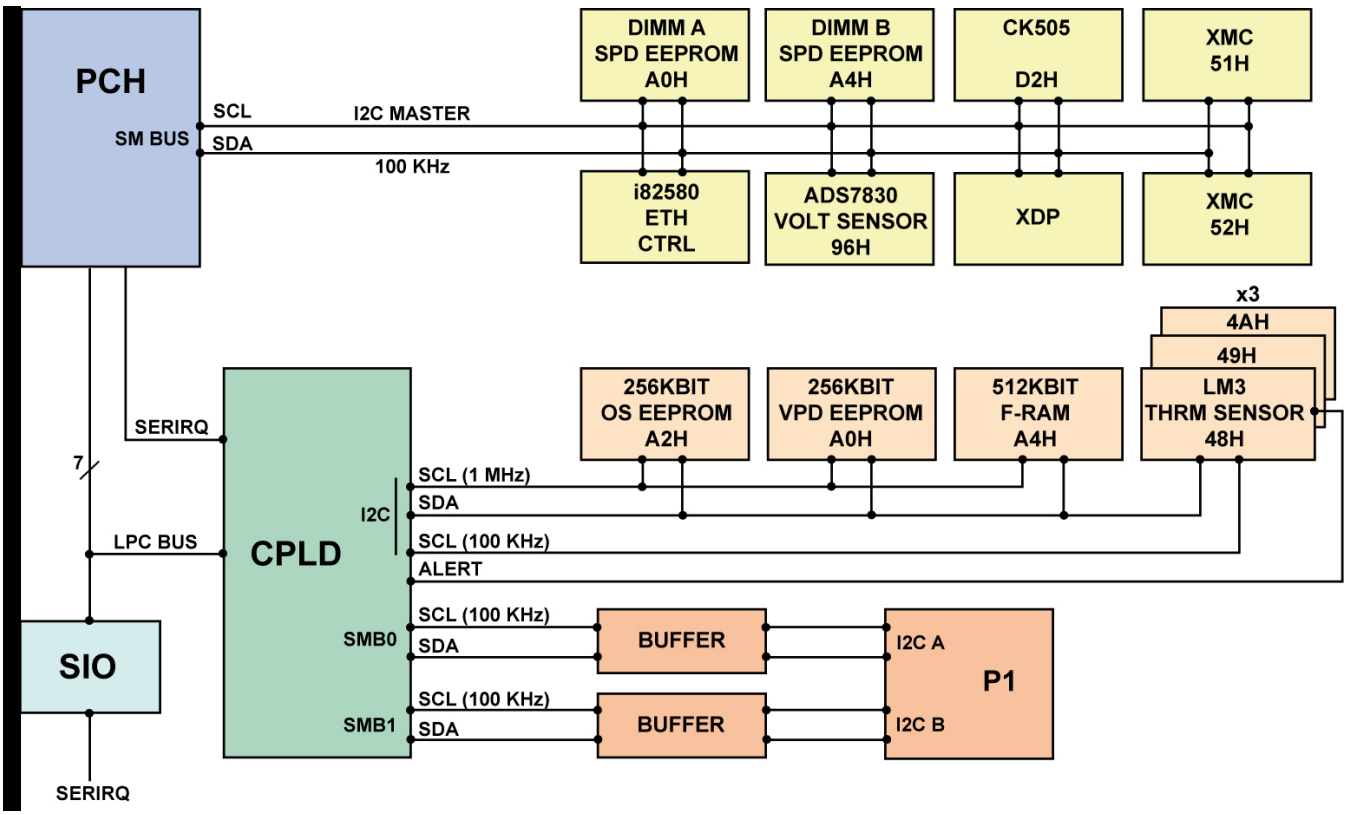


Figure 29: I2C Diagram

3.3 CPLD Features

The CPLD manages following features:

- Power-on/off control
- Reset control
- Local environmental control/monitoring
- LPC interface to processor
- I2C interfaces to I2C bus IPMB (rear P1)
- LEDs control
- Serial lines multiplexer
- Serial VPD and user memories
- User and system GPIOs
- Internal registers that allow system management

VM6050 I2C Interface

The VM6050 implements two SMBus on backplane P1.

- VME SMbus 0/1 master interfaces:

  I2C bus 0/1 master interfaces software tools are described in Fedora Release Note

- VME I2C bus 0 slave interface (IPMB)

  The VM6050 board SMBus 0 slave address depends on VME slot ID (slot geographical address = GA): VME Slot 1 (syscon): slave address is 0x18 (I2C 7bits addressing) VME Slot 2: slave address is 0x19 (I2C 7bits addressing) VME Slot 3: slave address is 0x1A (I2C 7bits addressing) And so on.

  Each board mapped at a unique I2C address implements two registers at register offset 0 (I2C_BOARD_STATUS) and offset 1 (I2C_BOARD_CONTROL). The register offset is sent to the board as a single byte I2C write.

These registers can also be accessed from CPU through LPC bus at I/O address 0x872 (I2C_BOARD_STATUS) and 0x873 (I2C_BOARD_CONTROL)

> I2C bus 0 slave registers definition:

Offset	Name	Access	Register Descritption
0x00	CPLD_ID	R	CPLD identification register
0x01	PCB_ID	R	Board identification register
0x02	FIRM_PWON	RW	Firm Power ON status register
0x03	PWON_STATUS	RW	Power ON status register
0x04	PWR_RST_CONFIG	RW	Power and ceset configuration register
0x05	VPD_BC1	R	VPD board configuration register 1
0x06	VPD_BC2	R	VPD board configuration register 2
0x07	SERIAL_LINES_CTL	RW	Serial Lines Control register
0x08	VM6050_PCI_Mode	RW	PCI2 Mode Configuration register
0x09	MEM_PROTECT	RW	Memory Write Protect register
0x0A	COM TX	RW	Reserved
0x0B	COM RX	RW	Reserved
0x0C	BOARD_CONFIGURATION	RW	Board configuration register
0x0D	PCI_MODE	RW	PCI1 mode and DRAM configuration register
0x0E	DIP_SWITCH_STATE	R	Board DIP switch status register
0x0F	SERIRQ_Control	RO/RW	Serial IRQ control and status register
0x5B	ALERT_STATUS	RW	Alert status register
0x6A	GEO_ADD	R	Geographical Address register
0x70	VME_Control	RW	VME control register
0x72	I2C_BOARD_STATUS	RW	I2C board status register
0x73	I2C_BOARD_CONTROL	RW	I2C board control register

CPLD_ID @ 0x00				
Bit#	Name	Description	Reset	Type
7-6	RSVD	Reserved	N.A	RO
5-0	CPLD_Version	**Version Number**	N.A	RO

PCB_ID @ 0x01				
Bit#	Name	Description	Reset	Type
7-0	Board_ID	**Board Identification** 0x50 = VM6050 (6U Board)	N.A	RO

FIRM_PWON @ 0x02				
Bit#	Name	Description	Reset	Type
7-1	PBIT_FAIL	**ID number of first failing test (updated by PBIT)** 0 No test failed. Any other value indicates ID number of the first failing test	0x00	RW
0	PBIT_RUN	**PBIT run (updated by PBIT)** 0 PBIT has not run 1 PBIT has run	0	RW

Examples:

- **0x00** means Test NOT RUN
- **0x03** means ALL TESTS RUN and TEST 1 FAIL
- **0x61** means ALL TESTS RUN and Test 48 FAIL (48 = 0x30, 0x30 << 1 => 0x60)
- **0x01** means All Test PASSED

PWON_STATUS @ 0x03				
Bit#	Name	Description	Reset	Type
7-4	DPOST	**Debug Power-On Status** Currently unused	0x00	RW
3-1	RSVD	**Reserved**	0	RW
0	POST_RTC	**RTC POST status (updated by BIOS)** 0 POST OK 1 POST FAILED (weak or missing battery)	0	RW

PWR_RST_CONFIG @ 0x04				
Bit#	Name	Description	Reset	Type
7	PWRON_MODE	**Power Mode** 0 Power-on when VME power present 1 Not power-on when VME power present If this bit is 0, the board is automatically powered-on when VME power is applied If this bit is 1 : the board remain in standby mode while not powered-on by reg 0x73 bit 0, and then can be switched on/off by the same bit. Value read from POWER_MODE DIP switch SW2[2]. 0 when switch off; 1 when on. See reg 0x73 bit 0 for power on/off management.	N.A	RO
6	RSVD	**Reserved**	0	RW

PWR_RST_CONFIG @ 0x04				
Bit#	Name	Description	Reset	Type
5	Alarm_Inhib	Fatal alert Inhibition 0 Power off in case of Fatal alert 1 No power off in case of Fatal alert Fatal alerts processed by this bit are : THERM_PROT#, THRMTRIP# , or CATERR#; see register 0x5B for their current status.	1	RW
4-0	RSVD	Reserved	0	RW

VPD_BC1 @ 0x05				
Bit#	Name	Description	Reset	Type
7-0	BC1	BC1 VPD board configuration word loaded from VPD EEPROM This has a copy of the VPD EEPROM at offset @0x0100	N.A	RO

VPD_BC2 @ 0x06				
Bit#	Name	Description	Reset	Type
7-0	BC2	BC2 VPD board configuration word loaded from VPD EEPROM This has a copy of the VPD EEPROM at offset @0x0101	N.A	RO

SERIAL_LINES_CTL @ 0x07				
Bit#	Name	Description	Reset	Type
7	Reserved		0	RW
6	SERIAL2_Full	SERIAL2 Transmit enable 0 Transmit disabled 1 Transmit enabled Transmit should always be enabled in RS232 mode, and only for transmitting in RS485 mode.	1	RW
4-5	SERIAL2_Term	SERIAL2 Termination Type 00 V35 01 V11 (for RXD only, Hi-Z for TXD) 10 Hi-Z (RS232 Mode) 11 V11	10	RW
3	Reserved		0	RW
2	SERIAL1_Full	SERIAL1 Transmit enable 0 Transmit disabled 1 Transmit enabled Transmit should always be enabled in RS232 mode, and only for transmitting in RS485 mode.	1	RW
1-0	SERIAL1_Term	SERIAL1 Termination Type 00 V35 01 V11 (for RXD only, Hi-Z for TXD) 10 Hi-Z (RS232 Mode) 11 V11	10	RW

This register is loaded from value in VPD EEPROM at offset @0x101 (same as register 0x06).

PCI Mode @ 0x08				
Bit#	Name	Description	Reset	Type
7-4	Reserved		0	RW
3	PCI_BUSMODE	PMC BUSMODE1: 0 = PMC1 board is connected 1 = PMC1board is not present	N/A	RO
2	PCI_M66EN	PMC M66EN: 0 = PCI freq forced to 33Mhz 1 = PCI freq not forced to 33Mhz (1= HZ signal) The default value of this register is loaded with EEPROM value (Byte at offset @0x0103 – bit 0)	1	RW
1-0	Reserved		0	RW

MEM_PROTECT @ 0x09				
Bit#	Name	Description	Reset	Type
7	Boot flash CS swap DIP	**Boot flash chip select configuration (from switch)** 0 Boot on normal BIOS (CS0 is the boot device) (switch off) 1 Boot on rescue BIOS (CS1 becomes the boot device) The value of this bit only comes from the switch and is not latched.	N/A	RO
6	Boot flash CS swap Valid#	**Operator Boot flash chip select configuration** IN USER MODE: This bit is hidden and set a 0 IN OPERATOR MODE: This bit is accessible 0 Boot flash CS swap DIP (bi7) has valid value 1 Invert value of boot flash CS swap DIP (bi7)	0	WR hidden
5	Both boot flash	**Operator Boot double flash configuration** IN USER MODE : This bit is hidden and set a 0 IN OPERATOR MODE : This bit is accessible 0 Boot flash 0 only 1 Boot flash 0 and 1	0	WR hidden
4	RSVD	**Reserved**	N/A	WR
3	USER WP	**User level WriteProtect hardware protection** Default value is read from a switch. This bit is forced to 1 when bit 0 = 1. 0 No user level protection (switch off) 1 User level WriteProtect active Protection of OS FRAM at SMB addr 0xA4/A5, Geth switch eeprom, PCIe switch eeprom memories.	N/A	RW
2	SYS WP	**System level WriteProtect hardware protection This bit is forced to 1 when bit 0 = 1** Default value read from a switch 0 No system level protection (switch off) 1 System Level protection active Protection of eeprom at SMB addr 0xA2/A3, and SPI boot flash memories.	N/A	RW
1	VPD WP	**VPD level WriteProtect hardware protection This bit is forced to 1 when bit 0 = 1** Default value read from a switch 0 No VPD level protection (switch off) 1 VPD level protection active Protection of VPD eeprom at SMB addr 0xA0/A1 (3AB_PLD_VPD_WP open drain signal)	N/A	RW
0	NVMRO	**NVMRO** On VM6050, NVMRO is not available	0	RW (1)

BOARD Configuration @ 0x0C				
Bit#	Name	Description	Reset	Type
7	Port D mode	Ibex Port D Display mode 0 Display port mode selected 1 HDMI port mode selected	0	RW
6	Port B mode	Ibex Port B Display mode 0 Display port mode selected 1 HDMI port mode selected	0	RW
5-4	RSVD	Reserved	0	RW
3	RSVD	Reserved	1	RW
2	SERIAL1 Mode	SERIAL1 mode 0 RS232 1 RS422/485	0	RW
1	SERIAL2 Mode	SERIAL2 mode 0 RS232 1 RS422/485	0	RW
0	RSVD	Reserved	0	RW

PCI Mode @ 0x0D				
Bit#	Name	Description	Reset	Type
7	RSVD	Reserved	N/A	RO
6	DRAM_SIZE	DRAM SIZE 0 = 4GB 1 = 8GB	N/A	RO
5-4	RSVD	Reserved	N/A	RO
3	PCI BUSMODE	PMC BUSMODE1 0 = PMCB board is connected 1 = PMCB board is not present	N/A	RO
2	PCI M66EN	PMC M66EN 0 = PCI freq forced to 33Mhz 1 = PCI freq not forced to 33Mhz (1= HZ signal)	1	RW

PCI Mode @ 0x0D				
Bit#	Name	Description	Reset	Type
1	PCIXCAP	PCIXCAP configuration mode 0 = PCI forced to conventional mode 1 = PCI mode depends on PCIXCAP status Note: This bit is not a status bit.	1	RW
0	PCISEL100	PCIX frequency 0 = PCI frequency for 33/66/133 MHz 1 = PCI frequency for 25/50/100 MHz (1= HZ signal)	0	RW

DIP Switch State @ 0x0E				
Bit#	Name	Description	Reset	Type
7	RSVD	Reserved	N/A	RO
7-4	USER_DIP	SW3[3:1] signal status	N/A	RO
3	RSVD	Reserved	0	RO
2	SP2	CPU speed force to 1.2GHZ status SW2[4]	N/A	RO
1	SP1	Reserved . SW2[3]	N/A	RO
0	FACTORY_MODE	FACTORY_MODE: 0: normal operation 1: Factory mode	N/A	RO

SERIQ_Control @ 0x0f				
Bit#	Name	Description	Reset	Type
7	SMB_MSK	SMB_ALERT Mask 1 = interrupt is masked 0 = Interrupt not masked Interrupt from backplane SMB_ALERT_n. The current status of the alert can be read from reg 0x70 (Smb_Alert_Status bit)	1	RW
6	SMB_TEMP_MSK	ALERT Mask 1 = interrupt is masked 0 = Interrupt not masked This bit when set to 1 forces Alert_Int to 0 (interrupt released), however this does not clear the interrupt source that remains active as long as the alert condition is still present, so if this bit is set back to 0 another interrupt is generated. See reg 0x5B bit 3 for current alert status. Alert is from SMBTEMP_ALERTb	1	RW

SERIQ_Control @ 0x0f				
Bit#	Name	Description	Reset	Type
5	TIP_MSK	**TIP_1Second Mask** 1 = interrupt is masked 0 = Interrupt not masked	1	RW
4	GPIOS_INT	**GPIOs Interrupt Status** 1 = GPIO interrupt occurred 0 = No interrupt occurred This interrupt status can be cleared through GPIOs registers	0	RO
3	SMB_INT	**SMB_ALERT Interrupt Status** 1 = SMB_ALERT occurred 0 = No interrupt occurred **Write 0 to clear**	0	RW
2	SMB_TEMP_INT	**ALERT Interrupt Status** 1 = ALERT interrupt pending 0 = No interrupt This bit reflects the state of the interrupt. When the interrupt is unmasked, the interrupt is asserted if the alert source is active. The interrupt is set when the alert source becomes active and automatically released when the alert source becomes inactive. The interrupt is also released as long as the mask bit (bit 6 above) is set to mask the interrupt. See bit 6 above for mask and alert sources See reg 0x5B bit 3 for current alert source state;	0	RO or RW
1	TIP_ INT	**TIP 1s Interrupt Status** 1 = TIP interrupt occurred 0 = No interrupt occurred **Write 0 to clear**	0	RW
0	WDG_INT	**Watchdog Interrupt Status** 1 = Watchdog interrupt occurred 0 = No interrupt occurred This interrupt status can be cleared through register 0x56	0	RO

ALERT_Status @ 0x5B				
Bit#	Name	Description	Reset	Type
7	CATERR	CPU CATERR pending 0 No error 1 CPU CATERR error pending => Power off if bit 5 of register PWR_RST_CONFIG@04 is not set to 1 (3Ux_PLD_CATERR# signal)	N.A	RO
6	THERMTRIP	CPU THERMTRIP pending 0 No error 1 THERMTRIP error pending => Power off if bit 5 of register PWR_RST_CONFIG@04 is not set to 1 (3Ux_PLD_THRMTRIP# signal)	N.A	RO
5	THERM_PROT	CPU THERM_PROT pending 0 No error 1 THERM_PROT	N.A	RO
4	PROCHOT	CPU PROCHOT pending 0 No error 1 PROCHOT error pending	N.A	RO
3	TEMP_ALERT	Board alert 0 No alert 1 Board alert is pending See reg 0xF bit 6 and 2 for interrupt mask and status	N.A	RO
2-1	RSVD	Reserved	N.A	RO
0	DDR throttling	Forces memory throttling to start 0 Memory throttling 1 No memory throttling	1	RW

GEO_ADD @ 0x6A				
Bit#	Name	Description	Reset	Type
7	SYSCON	VME System Controller 0 System Controller 1 Not System Controller	N/A	RO
6	Error	Parity Error 0 Parity is valid 1 Parity is invalid	N/A	RO
5	GAP	Geographical Address Parity	N/A	RO
4-0	GA	Geographical Address	N/A	RO

VME_Control @ 0x70				
Bit#	Name	Description	Reset	Type
7	Reserved	Not used	0	RW
6	Smb_Alert_Status	SMB_ALERT# Status 0 : SMB_ALERT# Signal is low 1 : SMB_ALERT# Signal is high See reg 0x0F for interrupt on this signal	N.A	RO
5-0	Reserved	Not used	0	RW

I2C_BOARD_STATUS @ 0x72 – When bit 3 of Register @73 is set to 0				
Bit#	Name	Description	Reset	Type
7	Power Status	Power Status 0 Power Stand By 1 Power ON	0	RO
6-5	Reset Source	Last Reset Source 0x00 Internal PSUs power-on 0x01 Watchdog expired 0x10 SYSRESET (from VPX or VME) 0x11 Local reset : GPIO2 (maskable reset), reset switch, reset from I2C (reg 0x73), or reset by software asserting	0	RO
4	Reset Status	Reset Status Side A 0 No PWOK or reset asserted 1 PWOK and reset unasserted	0	RO
3-0	Boot Status	Boot Status 0x00: RESET : default hardware value 0x01: BIOS-BOOT : written by BIOS 0x02: BIOS : written by BIOS 0x03: PBIT : written by BIOS 0x04: OS-BOOT : written by BIOS 0x05: OS-RUNNING : to be written by OS at the end of boot 0x06: COMPLETED : to be written by the final application when running 0x07: SHUTDOWN : to be written by OS when issuing a halt/shutdown 0x08: REBOOT : to be written by OS when rebooting 0x09 - 0x0B: Reserved 0x0C - 0x0F: Customer defined These bits are Read Only through I2C Slave Interface and R/W through LPC Interface	0	RW

I2C_BOARD_CONTROL @ 0x73 – when Bit 3 of this register is set to 0				
Bit#	Name	Description	Reset	Type
7-4	Board Id	**Board Identification** 0011 Reserved 0101 VM6050 0110 Reserved 0111 Reserved 1000 Reserved	0	RO
3	Check_Errors	**Error Status Selection** 0 Default meaning for register @ 72 and register @73 1 Select Error Status for register @ 72 and register @73	0	RW
2	RSVD	**Reserved**	0	RW
1	Reset_3UA	**Reset Side A** 0 No Reset 1 Reset Assert	0	RW
0	Power_OnOff	**Power On/Off Control** 0 = Power Off (StandBy) 1 = Power On This bit can always be used to set power on or off, and its default value is set according to POWER_MODE Dip Switch (SW2); 1 if switch is off; 0 if on. NOTE : cannot power on/off the board if reg 0x4 bit 7 is low (power is always on)	N.A	RW

3.4 Serial Lines EIA-422/485 Additional Modes

A total of 2 serial lines are available on VM6050 product.

EIA-232 serial lines mode are available on front panel RJ12 and P2 connectors.

See section 4.1.1 page 59 - “Serial Connector” and section 4.3.3 page 74 - “P2 Connector” for more information on pin assignments.

EIA-232 serial lines mode is the default mode, but EIA-422/485 mode can also be set with the following mode:

Mode	RJ12 fron panel connector	P2 rear connector	RJ12 front pin assignment	P2 rear pin assignment
Default EIA-232	EIA-232: COM1	EIA-232: COM1, COM2	COM1 TXD: pin 3 COM1 RXD: pin 4 COM1 RTS: pin 1 COM1 CTS: pin 6	
EIA-422/485 on COM1	EIA-422/485: COM1	EIA-422/485: COM1 EIA-422/485: COM2	COM1 TXD: pin 3 COM1 RXD: pin 4 COM1 TXD+: pin 1 COM1 RXD+: pin 6	

3.5 GPIOs

There are 8 GPIOs on VM6050 board and they are managed by CPLD. Refer to Fedora 14 release Note chapter 7.10 for further details about

- 3 GPIOs are available on P0 connector, GPIO [1-3]
- 3 GPIOs are available on P2 connector, GPIO [4-6]
- 2 GPIOs are available on P2 connector on customer request, GPIO [7-8], these both GPIOs take PMC1 IO [63-64]’s place

GPIO1-8: LVCMOS33 (0-3V3), Drive strength = 8 mA Slew rate = fast, weak pull-up = 47K.

The pull-up is to prevent GPIOs from floating if left unconnected. This pull-up is not configurable, but can be overriden by an additional stronger pull-down if a pull-down is required instead.

GPIOs are NOT 5V tolerant. Absolute maximum voltage on GPIOs is 3.75V (value not suitable for continuous operation). So any voltage above 3.6V must be reduced using a bridge made of two resistors before being applied to a GPIO.

Chapter 4 - Physical I/O

4.1 Front Panel Connectors

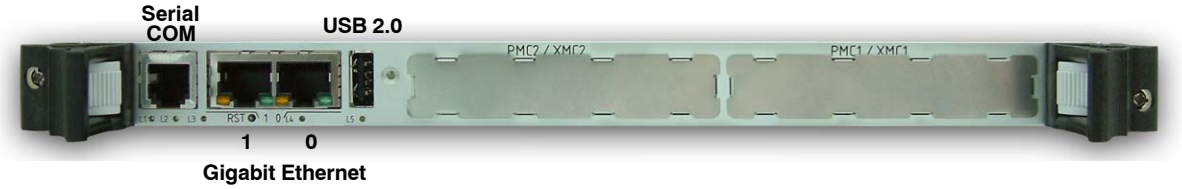


Figure 30: Location of the Front Panel Connectors

4.1.1 Serial Connector - COM

The VM6050 integrates two serial communications ports, COM1 and COM2 in PC parlance. COM1 and COM2 are available on rear via the P2 connector.

COM1 is also available via the front panel connector.

- COM1: EIA-232/485 (simplified RX/TX) port on RJ-12 front panel connector or on the rear P2 connector
- COM2: EIA-232/485 port on the rear P2 connector

Each serial port is configurable via the BIOS setup and CPLD as EIA-232 or EIA-422 or EIA-485. Each port operates in full duplex mode or in half duplex mode. Fast slew rate is the default mode in EIA-485 mode.

The signaling level of EIA-485 is compatible with EIA-422, so full duplex EIA-485 may also be used for point-to-point communications with an EIA-422 serial port. When port is operating in EIA-485 mode software may configure the termination for V.35, V11 or unterminated using CPLD

In EIA-232 mode the port is always unterminated register.

Pin Assignment

PIN	SIGNAL
1	RTS/TXD+
2	Shell
3	TXD/TXD-
4	RXD/RXD-
5	GND
6	CTS/RXD+

Table 15: Serial Connector Pin Assignment

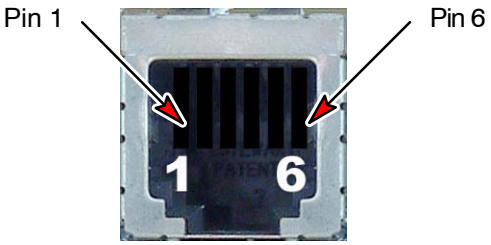


Figure 31: Serial Connector

A serial line should only be used via one connector at the same time, either the Serial front panel connector or the P2 connector.

MNEMONIC	DESCRIPTION
CTS/RXD+	EIA-232 Clear-To-Send / EIA-485 Receive Data
RTS/TXD+	EIA-232 Ready-To-Send / EIA-485 Transmit Data
RXD/RXD-	EIA-232Receive Data / EIA-485 Receive Data
TXD/TXD-	EIA-232 Transmit Data / EIA-485 Transmit Data
GND	Ground
Shell	Chassis Ground

Table 16: Serial Connector Signal Description

Serial Cable Designation

Serial cable is:

- RJ-14 (6 pin, 4 conductor) for a simple EIA-232 without handshake support.
- RJ-12 (6 pin, 6 conductor) for EIA-232 with handshaking.

  A RJ-12 to DB9/DB25 male or DB9/DB25 female adapter is available from multiple sources, such as:
  - Kontron Order Code KIT-RJ12DB9
  - Triangle Cable http://www.trianglecables.com/db9m-rj12.html

Pin Connector DB9	Signal	Pin Connector RJ-12
1	N.C.	1
2	TXD	3
3	RXD	4
4	N.C.	6
5	GND	5

4.1.2 Gigabit Ethernet Connectors

The Ethernet transmission should operate using a CAT5e cable with a maximum length of 50 m.

The Ethernet connectors are available as RJ-45 connectors with tab down. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

Pin Assignment

PIN	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-		I/O	BI_DC+
5	-	-	-		I/O	BI_DC-
6	I	RX-	I	RX-	I/O	BI_DB-
7	-	-	-		I/O	BI_DD+
8	-	-	-		I/O	BI_DD-
Shell	Chassis Ground					

Table 17: Gigabit Ethernet Connectors Pin Assignment

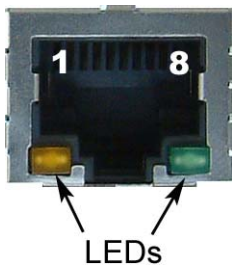


Figure 32: Ethernet Connector

Ethernet LEDs Status

> ACT (green)
This LED monitors network connection and activity. The LED lights up when a valid link (cable connection) has been established. The LED goes temporarily off if network packets are being sent or received through the RJ-45 port. When this LED remains off, a valid link has not been established due to a missing or a faulty cable connection.

STATUS		SPEED LED yellow	ACT LED green
Ethernet Link is not established		OFF	OFF
10 Mbps	Ethernet Link Established	OFF	ON
	Ethernet Link Activity	OFF	BLINK
100 Mbps	Ethernet Link Established	ON	ON
	Ethernet Link Activity	ON	BLINK
1000 Mbps	Ethernet Link Established	BLINK	ON
	Ethernet Link Activity	BLINK	BLINK

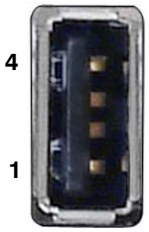
Table 18: Ethernet LEDs Status Definition

4.1.3 USB Connector

Pin Assignment

PIN	SIGNAL	FUNCTION	I/O
1	VCC (+5V Protected)	VCC	--
2	USB_D-	Differential USB-	I/O
3	USB_D+	Differential USB+	I/O
4	GND	GND	--

Table 19: USB Connector Pin Assignment



USB

Figure 33: USB Connector

4.2 Onboard Storage Connectors

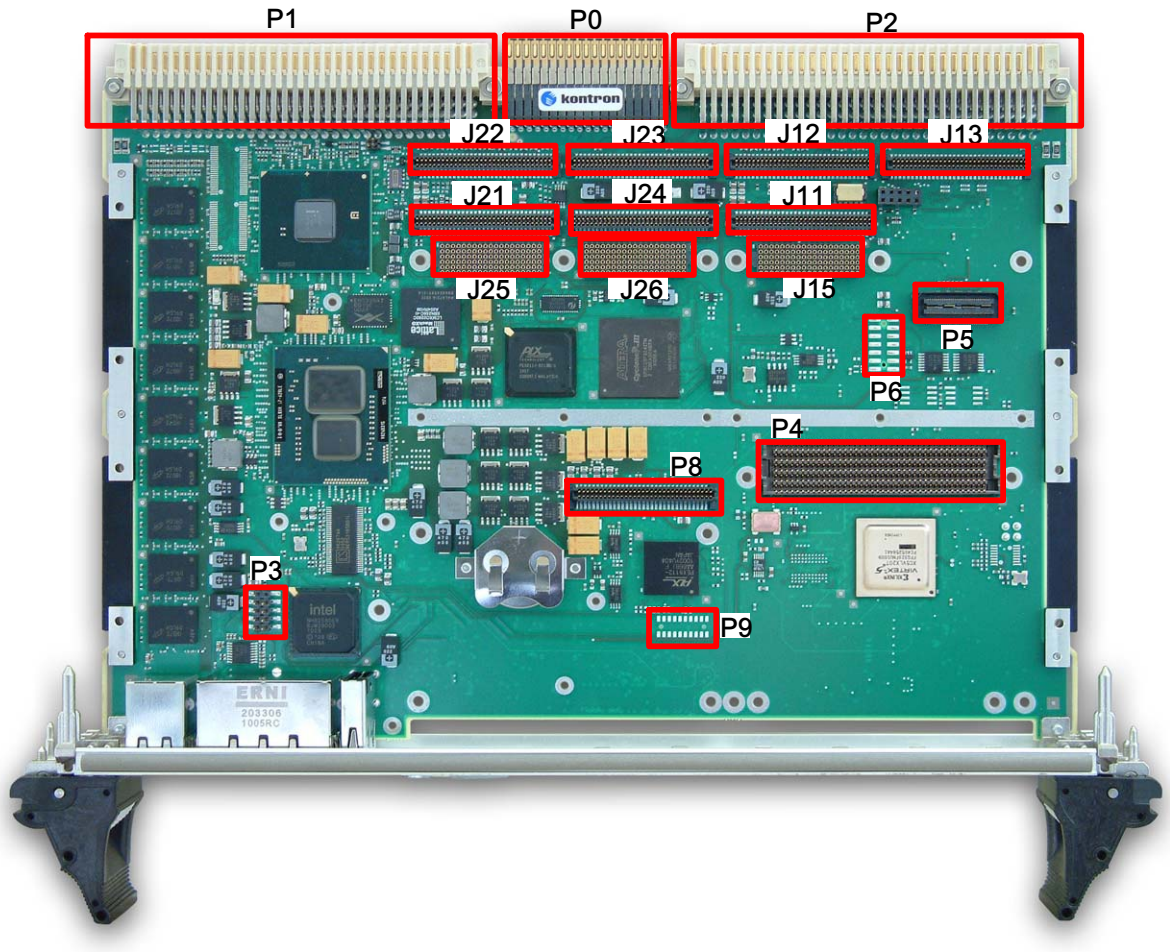


Figure 34: Connector Layout (Top View)

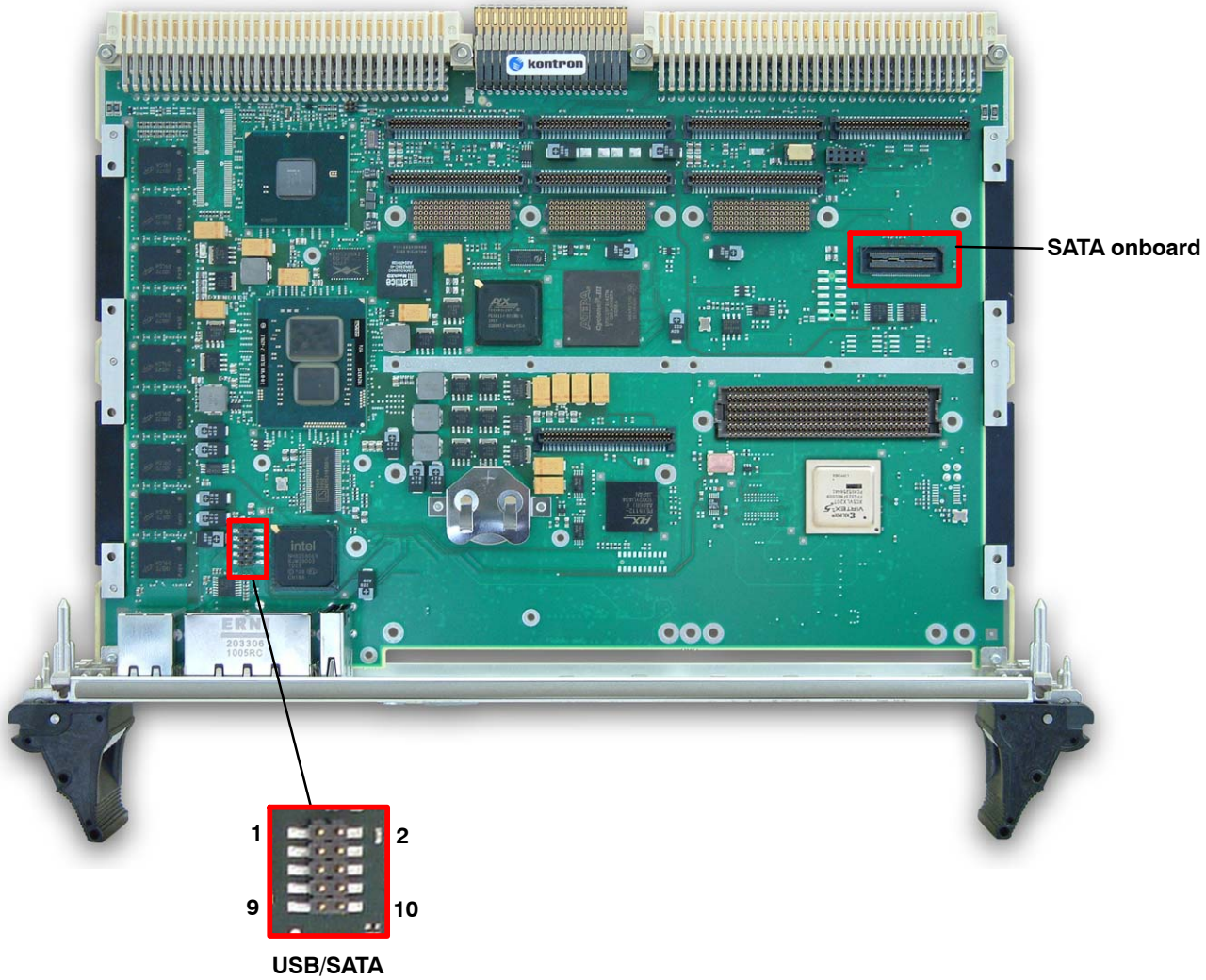


Figure 35: Onboard Storage Connector

4.2.1 Onboard USB/SATA Mezzanine

The onboard USB/SATA slot device (P3 connector) is used to connect an USB flash disk module or a SATA flash disk module. The following figure and table provide pinout information for the onboard USB/SATA connector P3:

PIN	SIGNAL	FUNCTION	I/O
1	USB0_PWR	VCC	--
2	SATA3 RX+	Diff Receive+	I
3	USB0_D-	Differential USB-	I/O
4	SATA RX-	Diff Receive-	I
5	USB0_D+	Differential USB+	I/O
6	GND	GND	--
7	GND	GND	--
8	SATA3 TX+	Diff Transmitt+	O
9	N.C.	Key Pin	--
10	SATA3 TX-	Diff Transmitt-	O

Table 20: USB/SATA onboard P3 Pinout

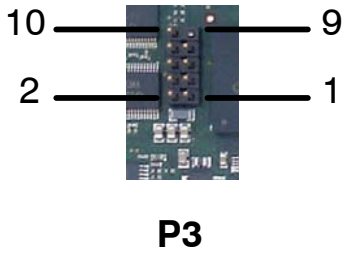


Figure 36: USB/SATA onboard Connector

The USB/SATA Flash module is fixed to the board, by using on one side the P3 connector, and on the other side, a standoff screwed to the VM6050 board and to the USB/SATA Flash module.

Order Code for the USB flash disk:

FDM-USB-*x*GB-2MM-IO: industrial version with conformal coating (*x* GB)

FDM-USB-*x*GB-2MM-IV

Order Code for the SATA flash disk:

FDM-SATA-*x*GB-CO

FDM-SATA-*x*GB-IO

FDM-SATA-*x*GB-COV

FDM-SATA-*x*GB-IOV

- Contact Kontron for available capacity.
- Due to the specific dynamics of the COTS FLASH mezzanine storage market, Kontron VM6050 EC level marking does not change whenever an equivalent FLASH mezzanine model is replaced by a more recent version available on the market. Kontron makes sure the new model will offer same or higher quantity of storage.
- For other aspects such as performance/wear leveling/lifetime, that depend heavily on the mission profile, FLASH users are encouraged to use application specific means to verify that the storage device meets the application needs along its life time or use device unique ID and low level health data information or mechanism (such as SMART) to monitor their installed base. Kontron can also offer specific ‘frozen BOM” services for customers willing to guarantee their installed base homogeneity across deliveries and time.

4.2.2 SATA Interface

The onboard SATA device (P5 connector) is used to connect a SATA HDD. The following table provides pinout information for the onboard SATA connector P5:

PIN	SIGNAL	FUNCTION	I/O
GND1 ... GND4	GND	Ground Signal	--
1	GND	Ground Signal	--
2 .. 6	N.C.	Not Connected	--
7	GND	Ground Signal	--
8 .. 12	N.C.	Not Connected	--
13	GND	Ground Signal	--
14	N.C.	Not Connected	--
15	SATA2 RX-	Differential Receive -	|
16	GND	Ground Signal	--
17	SATA2 RX+	Differential Receive +	|
18	+5V		--
19	GND	Ground Signal	--
20	+5V		--
21	SATA2 TX+	Differential Transmit +	O
22	+5V		--
23	SATA2 TX-	Differential Transmit -	O
24 .. 25	GND	Ground Signal	--
26	+3.3V		--
27	N.C.	Not Connected	--
28	+3.3V		--
29 .. 60	N.C.	Not Connected	--

Table 21: SATA onboard Ethernet Pinout

P5

Figure 37: SATA onboard Connector

4.3 Rear Connectors

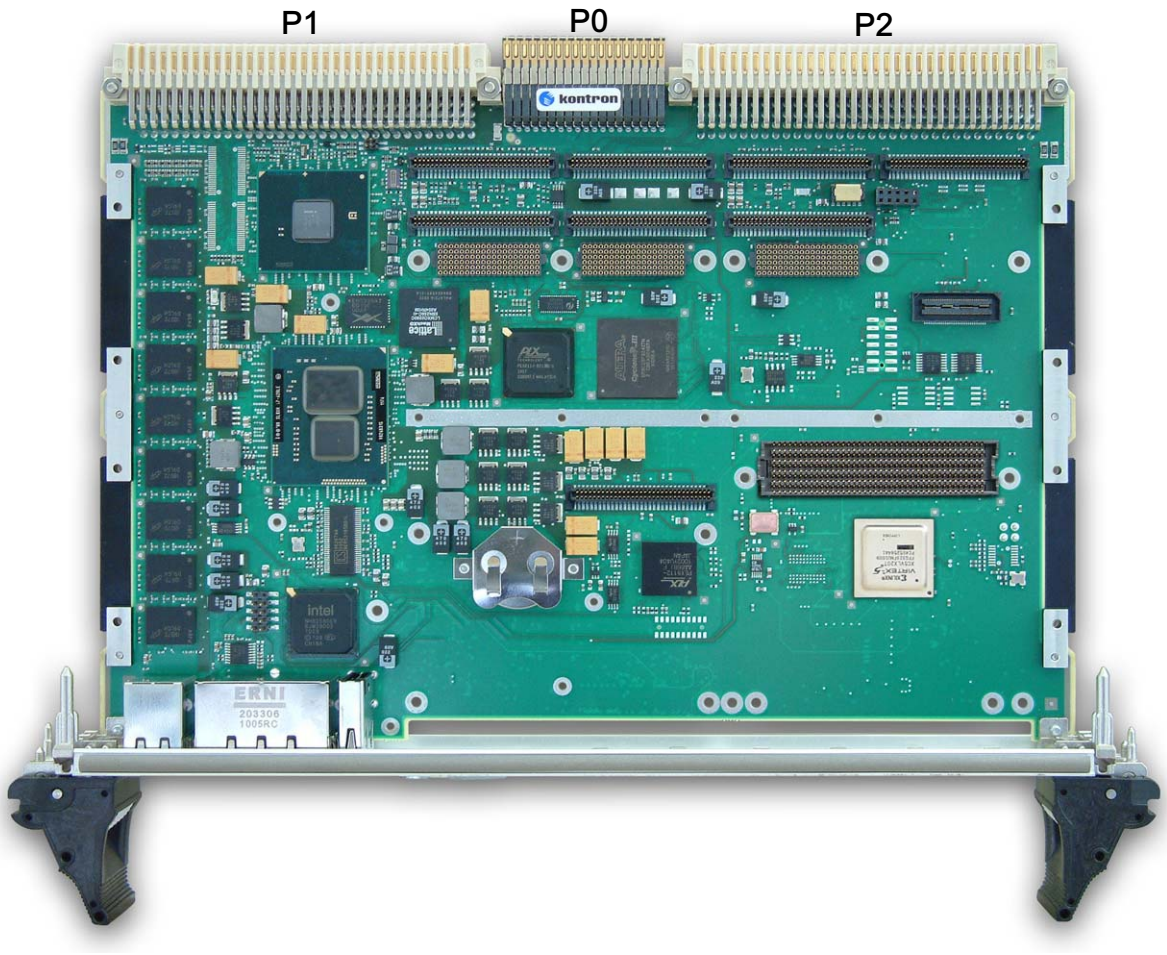


Figure 38: Rear Connectors

4.3.1 P0 Connector

4.3.1.1 P0 Connector Pin Assignment

Pin	P0 connector					
	Row f (2)	Row e	Row d	Row c	Row b	Row a
1 (4)	GND	PMC2 IO 35 or XMC2 IO S5 (1)	PMC2 IO 36 or XMC2 IO S6 (1)	PMC2 IO 37 or XMC2 IO S7 (1)	PMC2 IO 38 or XMC2 IO S8 (1)	PMC2 IO 39 or XMC2 IO S9 (1)
2	GND	ETH2 BI_DC-	ETH2 BI_DC+	GND	ETH2_DA-	ETH2 BI_DA+
3	GND	ETH2 BI_DD-	ETH2 BI_DD+	GND	ETH2_DB-	ETH2 BI_DB+
4	GND	ETH3 BI_DC-	ETH3 BI_DC+	GND	ETH3_DA-	ETH3 BI_DA+
5	GND	ETH3 BI_DD-	ETH3 BI_DD+	GND	ETH3_DB-	ETH3 BI_DB+
6	GND	USB3_PWR	RTC_BAT	NVMRO or (3) PWR-DOWN	USB2_PWR	RESET#
7	GND	USB2_DA-	USB2_DA+	GND	USB3_DA-	USB3_DA+
8	GND	SATA0_RX-	SATA0_RX+	GND	SATA0_TX-	SATA0_TX+
9	GND	SATA1_RX-	SATA1_RX+	GND	SATA1_TX-	SATA1_TX+
10	GND	GPIO3	GPIO2	GPIO1	PMC2 IO 33 or XMC2 IO S2 (1)	PMC2 IO 34 or XMC2 IO S4 (1)
11 (4)	GND	PMC2 IO 50 or XMC2 IO DP 11	PMC2 IO 48 or XMC2 IO DP 11+	PMC2 IO 46 XMC2 IO S1	PMC2 IO 60 or XMC2 IO DP 1-	PMC2 IO 58 or XMC2 IO DP1+
12 (4)	GND	PMC2 IO 54 or XMC2 IO DP 12-	PMC2 IO 52 or XMC2 IO DP 12+	PMC2 IO 45 XMC2 IO S3	PMC2 IO 64 or XMC2 IO DP 2-	PMC2 IO 62 or XMC2 IO DP 2+
13 (4)	GND	PMC2 IO 53 or XMC2 IO DP 13-	PMC2 IO 51 or XMC2 IO DP 13+	PMC2 IO 56 XMC2 IO S11	PMC2 IO 63 or XMC2 IO DP 3-	PMC2 IO 61 or XMC2 IO DP 3+
14 (4)	GND	PMC2 IO 49 or XMC2 IO DP 14-	PMC2 IO 47 or XMC2 IO DP 14+	PMC2 IO 55 XMC2 IO S13	PMC2 IO 59 or XMC2 IO DP 4-	PMC2 IO 57 or XMC2 IO DP 4+
15	GND	PEX_TXL0-	PEX_TXL0+	GND	PEX_RXL0-	PEX_RXL0+
16	GND	PEX_TXL1-	PEX_TXL1+	GND	PEX_RXL1-	PEX_RXL1+
17	GND	PEX_TXL2-	PEX_TXL2+	GND	PEX_RXL2-	PEX_RXL2+
18	GND	PEX_TXL3-	PEX_TXL3+	GND	PEX_RXL3-	PEX_RXL3+
19 (4)	GND	PMC2 IO 40 or XMC2 IO S10 (1)	PMC2 IO 41 or XMC2 IO S12 (1)	PMC2 IO 42 or XMC2 IO S14 (1)	PMC2 IO 43 or XMC2 IO S15 (1)	PMC2 IO 44 or XMC2 IO S16 (1)

(1) In the column 1, 10 and 19, they may be signals or Not Connected (N.C.). The default is the signals listed. The N.C. option is made available by removing three, 0-ohm resistor packs. Please contact Kontron for more information on this topic.

(2) The f row is the metal shielded on the outside P0 connector.

(3) The default is NVMRO signal

(4) The default is PMC signal listed. Please contact Kontron for XMC IO availability

Table 22: P0 Connector Pin Assignment

4.3.1.2 P0 Signal Description

Mnemonic	Legend	Signal Description
ETH*x* BI_DA+/–		Ethernet *x*: First pair of Transmit/Receive data.
ETH*x* BI_DB+/–		Ethernet *x*: Second pair of Transmit/Receive data.
ETH*x* BI_DC+/–		Ethernet *x*: Third pair of Transmit/Receive data.
ETH*x* BI_DD+/–		Ethernet *x*: Fourth pair of Transmit/Receive data.
GND		Ground
GPIO*x*		General Purpose I/O *x*
NVMRO		Non Volatile Memory Read Only signal
PEX RXL*y*+/–		x4 PCI Express (or Serial Rapid IO) Link – Receive+/– Lane *y*
PEX TXL*y*+/–		x4 PCI Express (or Serial Rapid IO) Link – Transmit+/– Lane *y*
PMC2 IO *yy*		PMC Site #2 I/0 signal *yy*
PWRDWN		Power Down board signal
RESET		Board Reset Signal
RTC–BAT		External Battery source for RTC
SATA0 RX+/RX– TX+/TX–		Serial ATA *x* Receive +/–
SATA1 RX+/RX– TX+/TX–		Serial ATA *x* Transmit +/–
USB2 DA+/– USB3 DA+/–		Differential Data Pair of USB Line *x*
USB*x* PWR		USB Line *x*
XMC2 IO *yy*		XMC Site #2 differential and single IO Signal *yy*

Table 23: P0 Signal Description

4.3.2 P1 Connector

4.3.2.1 P1 and P2 Row B (VMEbus) Connector Pin Assignment

Pin	P1					P2
	Row z	Row a	Row b	Row c	Row d	Row b
1	N.C.	D00	BBSY*	D08	+5V	+5V
2	GND	D01	BCLR*	D09	GND	GND
3	N.C.	D02	ACFAIL*	D10	N.C.	RETRY*
4	GND	D03	BG0IN*	D11	N.C.	A24
5	N.C.	D04	BG0OUT*	D12	N.C.	A25
6	GND	D05	BG1IN*	D13	N.C.	A26
7	N.C.	D06	BG1OUT*	D14	N.C.	A27
8	GND	D07	BG2IN*	D15	N.C.	A28
9	N.C.	GND	BG2OUT*	GND	GAP* (1)	A29
10	GND	SYSCLK	BG3IN*	SYSFAIL*	GA0* (1)	A30
11	N.C.	GND	BG3OUT*	BERR*	GA1* (1)	A31
12	GND	DS1*	BR0*	SYSRESET*	+3.3V	GND
13	N.C.	DS0*	BR1*	LWORD*	GA2* (1)	+5V
14	GND	WRITE*	BR2*	AM5	+3.3V	D16
15	N.C.	GND	BR3*	A23	GA3* (1)	D17
16	GND	DTACK*	AM0	A22	+3.3V	D18
17	N.C.	GND	AM1	A21	GA4* (1)	D19
18	GND	AS*	AM2	A20	+3.3V	D20
19	N.C.	GND	AM3	A19	SMB_SCL	D21
20	GND	IACK*	GND	A18	+3.3V	D22
21	N.C.	IACKIN*	IPMB_SCL	A17	SMB_SDA	D23
22	GND	IACKOUT*	IPMB_SDA	A16	+3.3V	GND
23	N.C.	AM4	GND	A15	SMB_ALERT*	D24
24	GND	A07	IRQ7*	A14	+3.3V	D25
25	N.C.	A06	IRQ6*	A13	N.C.	D26
26	GND	A05	IRQ5*	A12	+3.3V	D27
27	N.C.	A04	IRQ4*	A11	N.C.	D28
28	GND	A03	IRQ3*	A10	+3.3V	D29
29	N.C.	A02	IRQ2*	A09	N.C.	D30
30	GND	A01	IRQ1*	A08	+3.3V	D31
31	N.C.	–12V	+5V_STANDB	+12V	GND	GND
32	GND	+5V	+5V	+5V	+5V	+5V

* VME signals active when low.

(1) Geographical address pins, refer to section 4.3.2.2 page 71 for more information.

Table 24: P1 and P2 (Row B) Connector Pin Assignment

Do not exceed the maximum rated input voltages or apply reversed bias to the assembly.
If such conditions occur, *toxic fumes* may be produced due to the destruction of components. Only use the VM6050 in VME IEEE1014x or VME64 backplanes that supply power on both P1 and P2 connectors. Failure to observe this warning may result in damage to the board.

4.3.2.2 Geographical Address Pin Assignment

The 6 geographical address pins (GA0*, GA1*, GA2*, GA3*, GA4* and GAP*) shall be tied to ground or left open (floating) on the backplane P1 connector as defined in the table below.

Slot Number	GAP* Pin	GA4* Pin	GA3* Pin	GA2* Pin	GA1* Pin	GA0* Pin
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
10	GND	Open	GND	Open	GND	Open
11	Open	Open	GND	Open	GND	GND
12	GND	Open	GND	GND	Open	Open
13	Open	Open	GND	GND	Open	GND
14	Open	Open	GND	GND	GND	Open
15	GND	Open	GND	GND	GND	GND
16	Open	GND	Open	Open	Open	Open
17	GND	GND	Open	Open	Open	GND
18	GND	GND	Open	Open	GND	Open
19	Open	GND	Open	Open	GND	GND
20	GND	GND	Open	GND	Open	Open
21	Open	GND	Open	GND	Open	GND

The device that samples the levels of the geographical address pins will read the inverted value of the slot number into which the board is plugged. When the board is powered on without being plugged into a VME/VME64 backplane the slot number will be zero with a parity error (GAP* open).

4.3.2.3 VMEbus Signal Description

The VMEbus signals occupy rows a, b and c of the P1 connector and row b of the P2 connector.

Mnemonic	Signal Description
A01 to A15	**Address Bus (bits 1 to 15)**. Address lines that are used to broadcast a short, standard or extended address.
A16 to A23	**Address Bus (bits 16 to 23)**. Address lines that are used in conjunction with A01-A15 to broadcast a standard or extended address.
A24 to A31	**Address Bus (bits 24 to 31)**. Address lines that are used in conjunction with A01-A23 to broadcast an extended address.
ACFAIL*	**AC Failure**. This signal indicates when the AC input to the power supply is no longer being provided or that the required AC input voltage levels are not being met.
AM0 to AM5	**Address Modifier (bits 0 to 5)**. These signals are used to broadcast information such as the address size, cycle type, master identification or any combination of these.
AS*	**Address Strobe**. This signal indicates when a valid address has been placed on the address bus.
BBSY*	**Bus Busy**. This signal is driven low by the requester associated with the current bus master to indicate that its master is using the bus.
BCLR*	**Bus Clear**. This signal is generated by an arbiter to indicate that there is a higher priority request for the bus than the one being processed. This signal requests the current master to release the bus.
BERR*	**Bus Error**. This signal is generated by a slave or bus timer to tell the master that the data transfer was not completed.
BG0IN* to BG3IN*	**Bus Grant (0 to 3) In**. These signals are generated by the arbiter to tell the board receiving it that if it is requesting the bus on that level, then it has been granted use of the bus. Otherwise the board should pass the signal down the daisy chain. The BGxIN*/BGxOUT* signals form the bus grant daisy chain, i.e. the BGxOUT* of one board forms the BGxIN* of the next board in the daisy chain.
BG0OUT* to BG3OUT*	**Bus Grant (0 to 3) Out**. These signals are generated by requesters to tell the next board in the daisy chain that if it is requesting the bus on that level, then it may use the bus. Otherwise the board should pass the signal down the daisy chain.
BR0* to BR3*	**Bus Request (0 to 3)**. A low level, generated by a requester, on one of these lines, shows that some master needs to use the bus.
D00 to D31	**Data Bus (0 to 31)**. These signals are used to transfer data between masters and slaves, and status/ID information from interrupters to interrupt handlers.
DS0*, DS1*	**Data Strobe 0, 1**. These signals are used with LWORD* and A01 to show how many byte locations are being accessed (1, 2, 3 or 4). Also, during a write cycle, the falling edge of the first data strobe shows that valid data is available on the bus. On a read cycle, the rising edge of the first data strobe shows that data has been accepted from the data bus.
DTACK*	**Data Transfer Acknowledge**. This signal is generated by a slave. The falling edge shows that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle. The rising edge shows that the slave has released the data bus at the end of a read cycle.

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Mnemonic	Signal Description
GA0* to GA4* and GAP*	Geographical address pins (refer to the table in section 4.3.2.2). These pins indicate to the VME board which one of the backplane slot it currently uses (0 to 21).
GND	The DC voltage reference for the system.
IACK*	**Interrupt Acknowledge**. This signal is used by the interrupt handler to acknowledge an interrupt request. It is routed to the IACKIN* pin of slot 1, where it is monitored by the IACK daisy chain driver.
IACKIN*	**Interrupt Acknowledge In**. This signal tells the board receiving it that board can respond to the interrupt acknowledge cycle in process or pass it down the daisy chain. IACKIN*/IACKOUT* form the interrupt acknowledge daisy chain.
IACKOUT*	**Interrupt Acknowledge Out**. This signal is sent by a board to tell the next board in the daisy chain that it can respond to the interrupt acknowledge cycle in progress.
IPMB_SCL	**Intelligent Platform Management Bus** - Clock I2C
IPMB_SDA	**Intelligent Platform Management Bus** - Data I2C
IRQ1* to IRQ7*	**Interrupt Request (1 to 7)**. These signals are driven low by interrupters to request an interrupt on the corresponding level.
LWORD*	**Longword**. This signal is used with DS0*, DS1* and A01 to select which byte location(s) within the 4-byte group are accessed during the data transfer.
N.C.	This pin is not connected.
SMB_ALERT*	**System Management Bus** - Alert
SMB_SCL	**System Management Bus** - Serial clock line from the SMBus master to SMBus slave devices.
SMB_SDA	**System Management Bus** - Bi-directional serial data line between the SMBus master and the SMBus slave device.
SYSCLK	**System Clock**. This signal provides a constant 16 MHz clock signal that is independent of any other bus timing.
SYSFAIL*	**System Fail**. This signal shows that a failure has occurred in the system. It can be generated by any board in the system. It is also asserted after a reset and released when the board reset self-tests are passed successfully.
SYSRESET*	**System Reset**. When this signal is low, it causes the system to be reset.
WRITE*	**Write**. This signal is generated by a master to show whether the data transfer cycle is a read or a write.
+3.3V	+3.3 Volts DC power.
+5V	+5 Volts DC power
+12V	+12 Volts DC power.
-12V	-12 Volts DC power.

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Table 25: VME Signal Description

4.3.3 P2 Connector

4.3.3.1 P2 Connector Pin Assignment

The VMEbus signals occupy rows a, b and c of the P1 connector and row b of the P2 connector. Refer to section 4.3.2.1 page 70 for a detailed description of the row b of the P2 connector.

Pin	Row z	Row a	Row b	Row c	Row d
1	PMC2 IO 02	PMC1 IO 02	+5V	PMC1 IO 01	PMC2 IO 01
2	GND	PMC1 IO 04	GND	PMC1 IO 03	PMC2 IO 03
3	PMC2 IO 05	PMC1 IO 06	RETRY*	PMC1 IO 05	PMC2 IO 04
4	GND	PMC1 IO 08	A24	PMC1 IO 07	PMC2 IO 06
5	PMC2 IO 08	PMC1 IO 10	A25	PMC1 IO 09	PMC2 IO 07
6	GND	PMC1 IO 12	A26	PMC1 IO 11	PMC2 IO 09
7	PMC2 IO 11	PMC1 IO 14	A27	PMC1 IO 13	PMC2 IO10
8	GND	PMC1 IO 16	A28	PMC1 IO 15	PMC2 IO12
9	PMC2 IO 14	PMC1 IO 18	A29	PMC1 IO 17	PMC2 IO 13
10	GND	PMC1 IO 20	A30	PMC1 IO 19	PMC2 IO 15
11	PMC2 IO 17	PMC1 IO 22	A31	PMC1 IO 21	PMC2 IO 16
12	GND	PMC1 IO 24	GND	PMC1 IO 23	PMC2 IO 18
13	PMC2 IO 20	PMC1 IO 26	+5V	PMC1 IO 25	PMC2 IO 19
14	GND	PMC1 IO 28	D16	PMC1 IO 27	PMC2 IO 21
15	PMC2 IO 23	PMC1 IO 30	D17	PMC1 IO 29	PMC2 IO 22
16	GND	PMC1 IO 32	D18	PMC1 IO 31	PMC2 IO 24
17	PMC2 IO 26	PMC1 IO 34	D19	PMC1 IO 33	PMC2 IO 25
18	GND	PMC1 IO 36	D20	PMC1 IO 35	PMC2 IO 27
19	PMC2 IO 29	PMC1 IO 38	D21	PMC1 IO 37	PMC2 IO 28
20	GND	PMC1 IO 40	D22	PMC1 IO 39	PMC2 IO 30
21	PMC2 IO 32	PMC1 IO 42	D23	PMC1 IO 41	PMC2 IO 31
22	GND	PMC1 IO 44	GND	PMC1 IO 43	S0_TX/TX- (1)
23	S1_TX/TX- (1)	PMC1 IO 46	D24	PMC1 IO 45	S0_RX/RX- (1)
24	GND	PMC1 IO 48	D25	PMC1 IO 47	S0-RTS/TX+ (2)
25	S1_RX/RX- (1)	PMC1 IO 50	D26	PMC1 IO 49	S0_CTS/RX+ (2)
26	GND	PMC1 IO 52	D27	PMC1 IO 51	(S0_DTR/DIR) (3)
27	S1_TX+ (1)	PMC1 IO 54	D28	PMC1 IO 53	(S0_DSR)
28	GND	PMC1 IO 56	D29	PMC1 IO 55	(S0_DCD)
29	S1_RX+ (1)	PMC1 IO 58	D30	PMC1 IO 57	GPIO5
30	GND	PMC1 IO 60	D31	PMC1 IO 59	GPIO4
31	GPIO6	PMC1 IO 62	GND	PMC1 IO 61	GND
32	GND	PMC1 IO 64 or GPIO 7 (4)	+5V	PMC1 IO 63 or GPIO 8 (4)	+5V

* Signals active when low.

(1) The serial I/O TX and RX pins act as either single-ended signal for EIA-232 or one side differential pair forEIA-422/485.

(2) In EIA-422/485 modes, CTS and RTS act as the other side of the differental pair for Rx and Tx respectively.

(3) In EIA-485 mode, DTR acts as direction control/indicator

(4) Extra GPIO 7 and 8 are available on P2. The default signal is PMC IO. Please contact Kontron for more information on this topic.

Table 26: P2 Connector Pin Assignment

4.3.3.2 P2 Signal Description

The VME signals (row b) are described in section 4.3.2.3.

Mnemonic	Legend	Signal Description
GND		Ground
GPIO		General Purpose I/O x
PMC *x* IO yy		PMC Site *x* I/O signal *yy*
S*x*_CTS		Channel EIA-232 *x* - Clear-To-Send
S*x*_RTS		Channel EIA-232 *x* - Ready-To-Send
S*x*_RX		Channel EIA-232 *x* - Receive Data
S*x*_TX		Channel EIA-232 *x* - TransmitData
S0_DTR		Channel EIA-232 0 - Data Terminal Ready
S0_DSR		Channel EIA-232 0 - Data Set Ready
S0_DCD		Channel EIA-232 0 - Data Carrier Detect
+5V		+5 Volts DC power

Table 27: P2 Signal Description

4.4 PMC Connectors

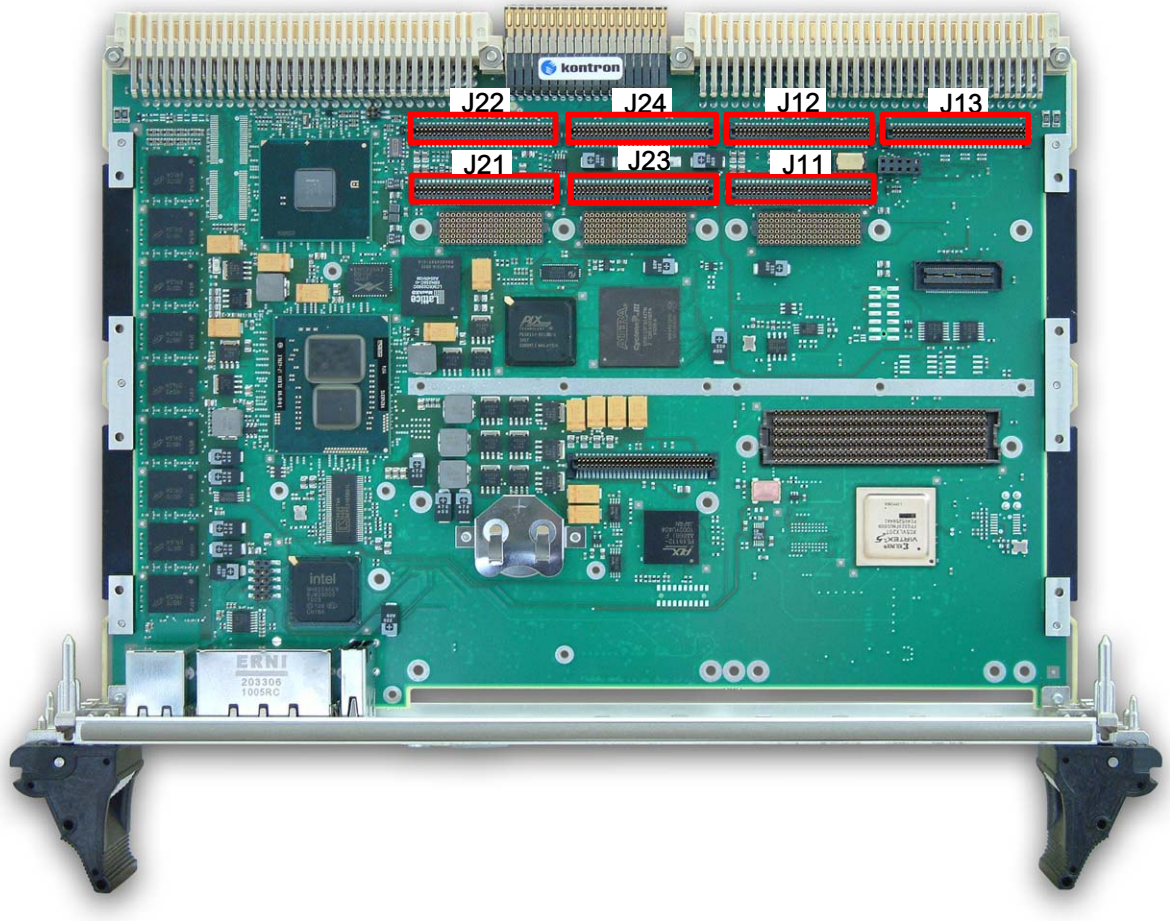


Figure 39: PMC Connectors

4.4.1 PMC J11 and J21 Connector Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	TCK	17	REQ#	33	FRAME#	49	AD[09]
2	-12V	18	+5V	34	GND	50	+5V
3	GND	19	V(I/0) (1)	35	GND	51	GND
4	INTA#	20	AD[31]	36	IRDY#	52	C/BE0#
5	INTB#	21	AD[28]	37	DEVSEL#	53	AD[06]
6	INTC#	22	AD[27]	38	.+5V	54	AD[05]
7	BUSMODE1#	23	AD[25]	39	PCIXCAP	55	AD[04]
8	+5V	24	GND	40	LOCK#	56	GND
9	INTD#	25	GND	41	SDONE#	57	V(I/O) (1)
10	N.C.	26	C/BE3#	42	SBO#	58	AD[03]
11	GND	27	AD[22]	43	PAR	59	AD[02]
12	+3.3V_SUS	28	AD[21]	44	GND	60	AD[01]
13	CLK	29	AD[19]	45	V(I/O) (1)	61	AD[00]
14	GND	30	+5V	46	AD[15]	62	+5V
15	GND	31	V(I/0) (1)	47	AD[12]	63	GND
16	GNT#	32	AD[17]	48	AD[11]	64	REQ64#

(1) V(I/O) is 3.3V only.

PCI signals active when low.

Table 28: PMC J11 and J21 Conne4ctor Pin Assignment

4.4.2 PMC J12 and J22 Connector Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	+12V	17	PME#	33	GND	49	AD[08]
2	TRST	18	GND	34	IDSEL B (1)	50	+3.3V
3	TMS	19	AD[30]	35	TRDY#	51	AD[07]
4	TDO	20	AD[29]	36	+3.3V	52	REQ B# (1)
5	TDI	21	GND	37	GND	53	+3.3V
6	GND	22	AD[26]	38	STOP#	54	GNT B# (1)
7	GND	23	AD[24]	39	PERR#	55	PMC-RSVD
8	N.C.	24	+3.3V	40	GND	56	GND
9	N.C.	25	IDSEL	41	+3.3V	57	PMC-RSVD
10	N.C.	26	AD[23]	42	SERR#	58	EREADY
11	BUSMODE2#	27	+3.3V	43	C/BE1#	59	GND
12	+3.3V	28	AD[20]	44	GND	60	N.C.
13	RST#	29	AD[18]	45	AD[14]	61	ACK64#
14	GND	30	GND	46	AD[13]	62	+3.3V
15	+3.3V	31	AD[16]	47	M66EN	63	GND
16	BUSMODE4#	32	C/BE2#	48	AD[10]	64	N.C.

(1) IDSEL B, REQ B# and GNT B# are provided for use by dual-function PMC modules or processor-PMC modules

PCI signals active when low.

Table 29: PMC J12 and J22 Connector Pin Assignment

4.4.3 PMC J23 Connector Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	N.C.	17	AD[59]	33	GND	49	AD[37]
2	GND	18	AD[58]	34	AD[48]	50	GND
3	GND	19	AD[57]	35	AD[47]	51	GND
4	C/BE7#	20	GND	36	AD[46]	52	AD[36]
5	C/BE6#	21	V(I/O) (1)	37	AD[45]	53	AD[35]
6	C/BE5#	22	AD[56]	38	GND	54	AD[34]
7	C/BE4#	23	AD[55]	39	V(I/O) (1)	55	AD[33]
8	GND	24	AD[54]	40	AD[44]	56	GND
9	V(I/O) (1)	25	AD[53]	41	AD[43]	57	V(I/O)
10	PAR64	26	GND	42	AD[42]	58	AD[32]
11	AD[63]	27	GND	43	AD[41]	59	RSVD
12	AD[62]	28	AD[52]	44	GND	60	RSVD
13	AD[61]	29	AD[51]	45	GND	61	RSVD
14	GND	30	AD[50]	46	AD[40]	62	GND
15	GND	31	AD[49]	47	AD[39]	63	GND
16	AD[60]	32	GND	48	AD[38]	64	N.C.

(1) V(I/O) is 3.3V only

PCI signals active when low.

Table 30: PMC J13 and J23 Connector Pin Assignment

4.4.4 J13 and J24 Connector Pin Assignment

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	PMC IO 01	17	PMC IO 17	33	PMC IO 31	49	PMC IO 49
2	PMC IO 02	18	PMC IO 18	34	PMC IO 34	50	PMC IO 50
3	PMC IO 03	19	PMC IO 19	35	PMC IO 35	51	PMC IO 51
4	PMC IO 04	20	PMC IO 20	36	PMC IO 36	52	PMC IO 52
5	PMC IO 05	21	PMC IO 21	37	PMC IO 37	53	PMC IO 53
6	PMC IO 06	22	PMC IO 22	38	PMC IO 38	54	PMC IO 54
7	PMC IO 07	23	PMC IO 23	39	PMC IO 39	55	PMC IO 55
8	PMC IO 08	24	PMC IO 24	40	PMC IO 40	56	PMC IO 56
9	PMC IO 09	25	PMC IO 25	41	PMC IO 41	57	PMC IO 57
10	PMC IO 10	26	PMC IO 26	42	PMC IO 42	58	PMC IO 58
11	PMC IO 11	27	PMC IO 27	43	PMC IO 43	59	PMC IO 59
12	PMC IO 12	28	PMC IO 28	44	PMC IO 44	60	PMC IO 60
13	PMC IO 13	29	PMC IO 29	45	PMC IO 45	61	PMC IO 61
14	PMC IO 14	30	PMC IO 30	46	PMC IO 46	62	PMC IO 62
15	PMC IO 15	31	PMC IO 31	47	PMC IO 47	63	PMC IO 63
16	PMC IO 16	32	PMC IO 32	48	PMC IO 48	64	PMC IO 64

Table 31: J24 Connector Pin Assignment

4.4.5 PMC Signal Description

Mnemonic	Signal Description
AD[00] to AD[63]	Address/Data bits. Multiplexed address and data bus. AD32 to AD63 are specifics to 64-bit bus extension.
ACK64#	Acknowledge 64-bit Transfer. Driven low by the device to indicate that the target is willing to transfer data using 64 bits.
BUSMODE1#	Bus Mode 1. Driven low by a PMC module to indicate that it supports the current bus mode
BUSMODE2#	Bus Mode 2. Driven low by a PMC module to indicate that it supports the current bus mode
BUSMODE4#	Bus Mode 4. Driven low by a PMC module to indicate that it supports the current bus mode
C/BE0# to C/BE7#	Command/Byte Enables. During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase the signals are byte enables that specify the active bytes on the bus. C/BE4# to C/BE7# are specifics to 64-bit bus extension.
CLK	Clock. Except RST*, the 64-bit PCI bus signals are synchronous to 33 or 66 MHz clock.
DEVSEL#	Device Select. Driven low by a PCI agent to signal that it has decoded its address as the target of the current access.
FRAME#	FRAME. Driven low by the current master to signal the start and duration of an access.
EREADY	EREADY. Output of non-monarch PPMCs that indicates it has completed its onboard initialization and can respond to PCI bus enumeration by the monarch via configuration cycles. Input to the monarch PPMC that indicates all non-monarch PPMCs have completed their onboard initialization and can respond to PCI bus enumeration by the monarch via configuration cycles.
GNT#	Grant. Driven low by the arbiter to grant PCI bus ownership to a PCI agent.
GNT B#	Grant. GNT B# is provided for use by dual-function PMC modules or processor-PMC modules.
IDSEL	Initialization Device Select. Device chip select during configuration cycles.
IDSEL B#	Initialization Device Select. IDSEL B is provided for use by dual-function PMC modules or processor-PMC modules.
INTA# to INTD#	Interrupt lines. Level-sensitive, active-low interrupt requests.
IRDY#	Initiator Ready. Driven low by the initiator to signal its ability to complete the current data phase.
LOCK#	LOCK. Driven low to indicate an atomic operation that may require multiple transactions to complete.
M66EN	66 MHZ Enable. Indicates to a device if the bus segment is operating at 66 or 33 MHz. If it is high then the bus speed is 66 MHz and if it is low then the bus speed is 33 MHz.
N.C.	This pin is not connected.
PAR	Parity. Parity protection bit for AD0 to AD31 and C/BE0# to C/BE3#.
PAR64	Parity Upper DWORD. Parity protection bit for AD32 to AD63 and C/BE4# to C/BE7#.
PERR#	Parity Error. Driven low by a PCI agent to signal a parity error.

Table 1 of 2

Mnemonic	Signal Description
PMC IO 01 to PMC IO 64	64-bit PCI bus PMC 64 signals. Used to transmit I/O signals from PCI 64 PMC connector (J14) to P2 connector.
PMC-RSVD	Reserved. Do not connect this pin.
PME	
REQ#	Request. Driven low by a PCI agent to request ownership of the PCI bus.
REQ B#	Request. REQ B# is provided for use by dual-function PMC modules or processor-PMC modules.
REQ64#	Request 64-bit Transfer. Driven low by the current bus master, indicates that it desires to transfer data using 64 bits.
RST#	Reset. Driven low to reset the PCI bus.
SBO#	Snoop Backoff. Indicates a hit of a modified line asserted.
SDONE#	Snoop Done. Indicates the status of the snoop for the current access.
SERR#	System Error. Driven low by a PCI agent to signal a system error.
STOP#	STOP. Driven low by a PCI target to signal a disconnect or target-abort.
TCK	JTAG Clock.
TDI	JTAG Data In
TDO	JTAG Data Out
TMS	JTAG Mode Select
TRDY#	Target Ready. Driven low by the current target to signal its ability to complete the current data phase.
TRST	JTAG Reset.
V(I/O)	Power supply delivered by the board. On the PCI 64 PMC slots, +3.3 Volts power is supplied. +5 Volts signaling PMCs are not supported. Contact Kontron for more information.
+3.3V	+3.3 Volts DC power
+5V	+5 Volts DC power
+12V	+12 Volts DC power
-12V	-12 Volts DC power
	Table 2 of 2

Table 32: PMC Signal Description

4.5 XMC Connectors

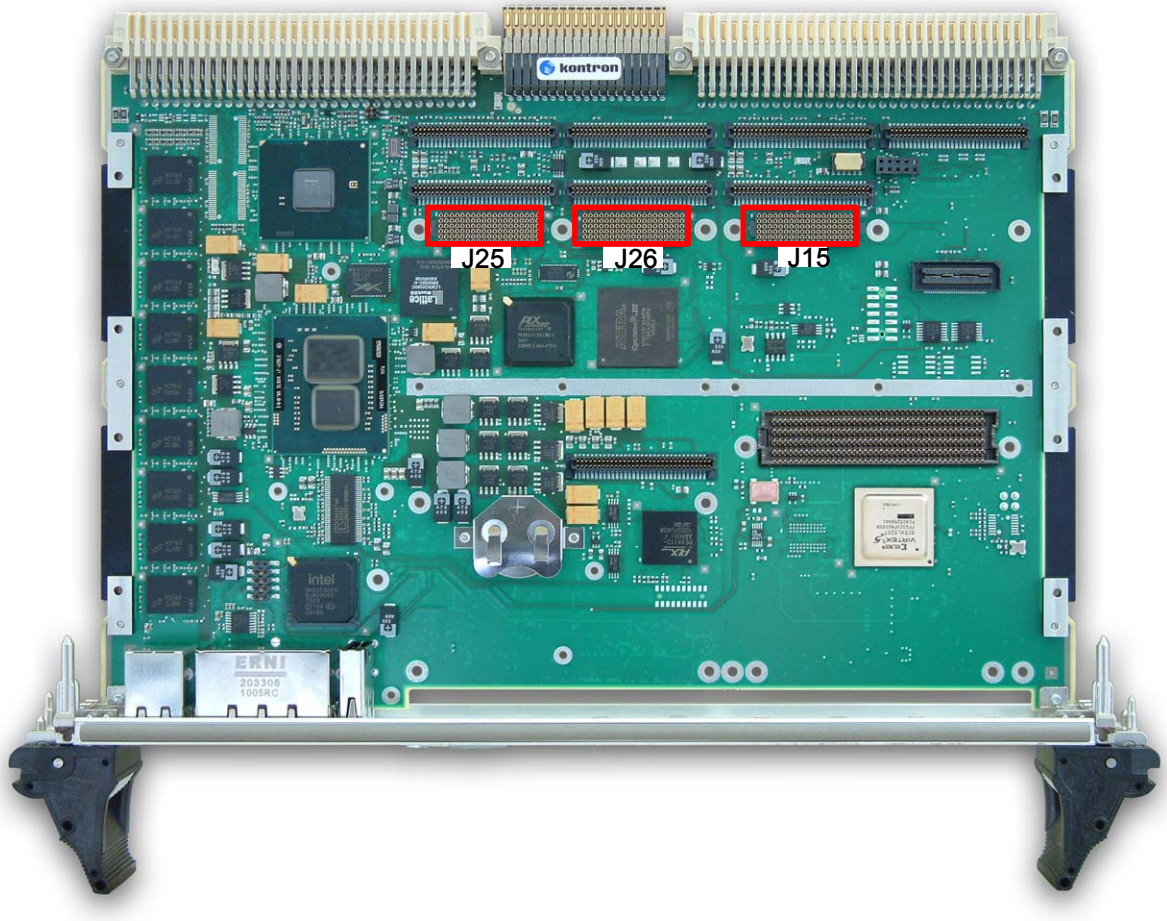


Figure 40: XMC Connectors

4.5.1 XMC J15 and J25 Connector Pin Assignments

Two XMC sites are provided to allow the installation of VITA 42.3, PCI-Express mezzanine cards. The signals assignments are as shown in the following table. The encoding for GA[2:0] should not conflict with other SMbus/IPMI devices.

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR (1)
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR (1)
4	GND	GND	TCK	GND	GND	NC
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR (1)
6	GND	GND	TMS	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR (1)
8	GND	GND	TDI	GND	GND	-12V
9	RFU	RFU	N.C.	RFU	RFU	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	PER0p0	PER0n0	NC	PER0p1	PER0n1	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PER0p2	PER0n2	3.3V AUX	PER0p3	PER0n3	VPWR (1)
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	N.C.	PER0p5	PER0n5	VPWR (1)
16	GND	GND	NVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	N.C.	PER0p7	PER0n7	N.C.
18	GND	GND	N.C.	GND	GND	N.C.
19	REFCLK+0	REFCLK-0	N.C.	N.C.	N.C.	N.C.

(1) VPWR is connected to +5V via a fuse.
The 12V option is available, please contact Kontron for more information on this topic.

Signals active when low.

Table 33: XMC J15 and J25 Connector Pin Assignments

4.5.2 XMC J26 Connector Pin Assignment

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	XMCIO_DP_P<1>	XMCIO_DP_N<1>	XMCIO_S<1>	XMCIO_DP_P<2>	XMCIO_DP_N<2>	XMCIO_S<2>
2	GND	GND	NC	GND	GND	NC
3	XMCIO_DP_P<3>	XMCIO_DP_N<3>	XMCIO_S<3>	XMCIO_DP_P<4>	XMCIO_DP_N<4>	XMCIO_S<4>
4	GND	GND	NC	GND	GND	NC
5	NC	NC	XMCIO_S<5>	NC	NC	XMCIO_S<6>
6	GND	GND	NC	GND	GND	NC
7	NC	NC	XMCIO_S<7>	NC	NC	XMCIO_S<8>
8	GND	GND	NC	GND	GND	NC
9	NC	NC	XMCIO_S<9>	NC	NC	XMCIO_S<10>
10	GND	GND	NC	GND	GND	NC
11	XMCIO_DP_P<11>	XMCIO_DP_N<11>	XMCIO_S<11>	XMCIO_DP_P<12>	XMCIO_DP_N<12>	XMCIO_S<12>
12	GND	GND	NC	GND	GND	NC
13	XMCIO_DP_P<13>	XMCIO_DP_N<13>	XMCIO_S<13>	XMCIO_DP_P<14>	XMCIO_DP_N<14>	XMCIO_S<14>
14	GND	GND	NC	GND	GND	NC
15	NC	NC	XMCIO_S<15>	NC	NC	XMCIO_S<16>
16	GND	GND	NC	GND	GND	NC
17	NC	NC	NC	NC	NC	NC
18	GND	GND	NC	GND	GND	NC
19	NC	NC	NC	NC	NC	NC

Table 34: XMC J26 Connector Pin Assignment

Refer to Table 22 page 68 for the mapping of XMC J26 connector or P0 rear connector.

4.5.3 XMC Signal Decription

Mnemonic	Signal Description
GA[0..2]	I2C channel select. These signals allow a carrier to address a specific XMC slot on an IPMI I2C bus shared by multiple XMCs.
GND	Ground
MPRESENT	Module present. This signal allows the carrier to determine whether an XMC is present.
MRSTI	XMC Reset In. When this signal is asserted low by the carrier, the mezzanine card shall initialize itself into a known state.
MSCL	IPMI I2C serial clock.
MSDA	IPMI I2C serial data.
NVMRO	XMC Write Prohibit. When this signal is asserted high, the XMC shall disable writes to non-volatile memory on the XMC.
N.C.	Not Connected. Do not Used
PET0p/n[0..7]	Link 0 Differential Transmit. These signals are used by the XMC to receive high-speed protocol-specific data TO the carrier over the PCI Express interface.
PER0p/n[0..7]	Link 0 Differential Receive. These signals are used by the XMC to receive high-speed protocol-specific data FROM the carrier over the PCI Express interface.
REFCLK+/-0	Differential reference clock for Link 0 PCI Express interface.
RFU	Reserved for Future Use
TCK	JTAG Clock.
TDI	JTAG Data In
TDO	JTAG Data Out
TMS	JTAG Mode Select
TRST	JTAG Reset.
VPWR	Power pins. These signals carry either 12V or 5V power from the carrier to the XMC. 5V by default
3.3V	
3.3V AUX	
+/-12V	
XMCIO_DP_P/N [1...13]	XMC differential pair. Used to transmitt differential pair IO signals from secondary XMC connector (J26) to P0 connector
XMCIO_S [1...16]	XMC single ended IO. Used to transmitt single ended IO signals from secondary XMC connector (J26) to P0 connector

Table 35: XMC Signal Description

4.6 FMC Connector

4.6.1 FMC Interface - P4 and P6 Connectors

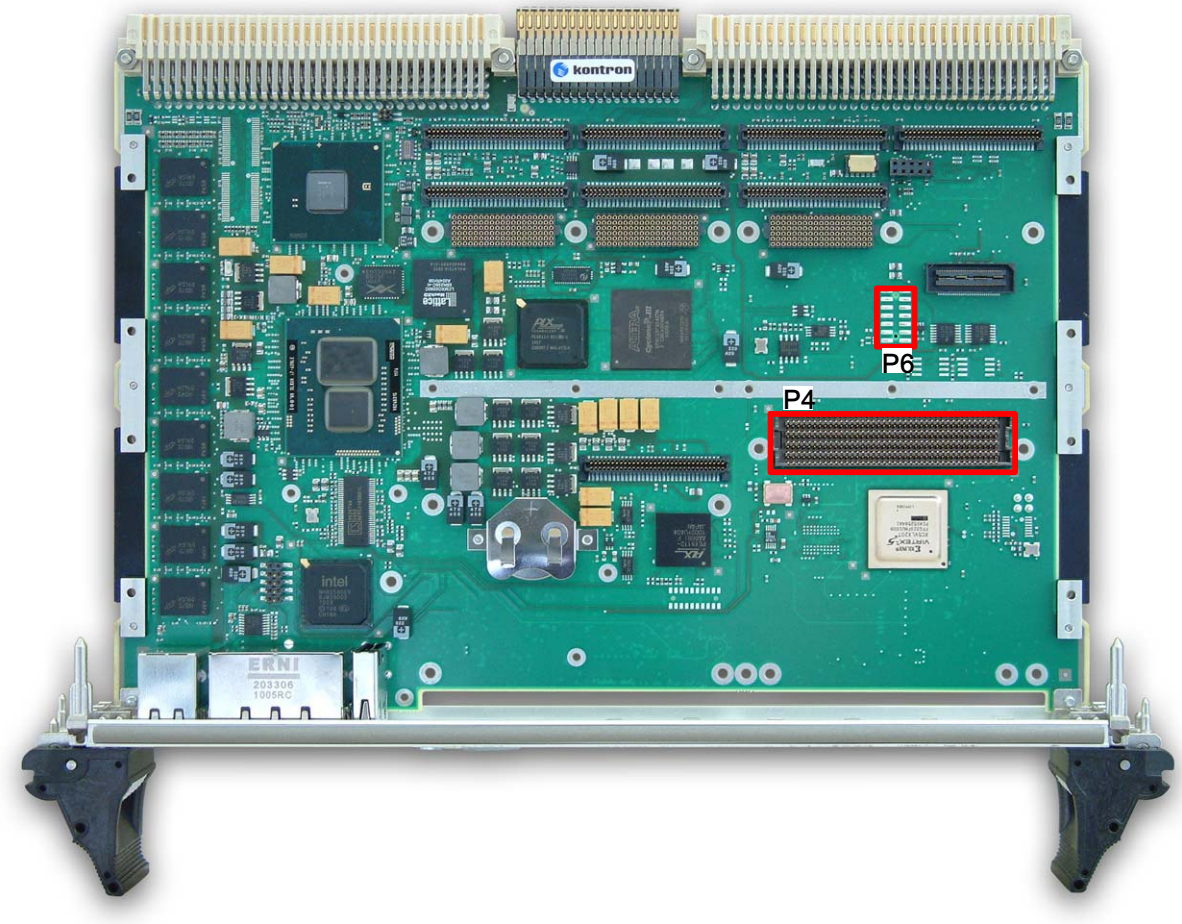


Figure 41: FMC Connectors Layout (Top View)

4.6.2 FMC P4 Connector Pin Assignment

The FMC site is provided to allow the installation of VITA 57.1 FMC mezzanine cards. The signal assignments are shown in the following tables:

	Row H	Row G	Row D	Row C
1	VREF_A_M2C	GND	PG_C2M	GND
2	PRSNT_M2C_L	CLK0_C2M_P	GND	NC
3	GND	CLK0_C2M_N	GND	NC
4	CLK0_M2C_P	GND	NC	GND
5	CLK0_M2C_N	GND	NC	GND
6	GND	LA00_P	GND	NC
7	LA02_P	LA00_N	GND	NC
8	LA02_N	GND	LA01_P	GND
9	GND	LA03_P	LA01_N	GND
10	LA04_P	LA03_N	GND	LA06_P
11	LA04_N	GND	LA05_P	LA06_N
12	GND	LA08_P	LA05_N	GND
13	LA07_P	LA08_N	GND	GND
14	LA07_N	GND	LA09_P	LA10_P
15	GND	LA12_P	LA09_N	LA10_N
16	LA11_P	LA12_N	GND	GND
17	LA11_N	GND	LA13_P	GND
18	GND	LA16_P	LA13_N	LA14_P
19	LA15_P	LA16_N	GND	LA14_N
20	LA15_N	GND	LA17_P	GND
21	GND	LA20_P	LA17_N	GND
22	LA19_P	LA20_N	GND	LA18_P
23	LA19_N	GND	LA23_P	LA18_N
24	GND	LA22_P	LA23_N	GND
25	LA21_P	LA22_N	GND	GND
26	LA21_N	GND	LA26_P	LA27_P
27	GND	LA25_P	LA26_N	LA27_N
28	LA24_P	LA25_N	GND	GND
29	LA24_N	GND	(TCK)	GND
30	GND	LA29_P	(TDI)	SCL
31	LA28_P	LA29_N	(TDO)	SDA
32	LA28_N	GND	3P3VAUX	GND
33	GND	LA31_P	(TMS)	GND
34	LA30_P	LA31_N	(TRST_L)	GA0
35	LA30_N	GND	GA1	12P0V
36	GND	LA33_P	3P3V	GND
37	LA32_P	LA33_N	GND	12P0V
38	LA32_N	GND	3P3V	GND
39	GND	VADJ	GND	3P3V
40	VADJ	GND	3P3V	GND

Table 36: FMC Connector Rows CDGH

	Row K	Row J	Row F	Row E	Row B	Row A
1	NC	GND	PG_M2C	GND	NC	GND
2	GND	CLK1_C2M_P	GND	NC	GND	NC
3	GND	CLK1_C2M_N	GND	NC	GND	NC
4	CLK1_M2C_P	GND	NC	GND	NC	GND
5	CLK1_M2C_N	GND	NC	GND	NC	GND
6	GND	NC	GND	NC	GND	NC
7	NC	NC	NC	NC	GND	NC
8	NC	GND	NC	GND	NC	GND
9	GND	NC	GND	NC	NC	GND
10	NC	NC	NC	NC	GND	NC
11	NC	GND	NC	GND	GND	NC
12	GND	NC	GND	NC	NC	GND
13	NC	NC	NC	NC	NC	GND
14	NC	GND	NC	GND	GND	NC
15	GND	HA14_P	GND	HA16_P	GND	NC
16	HA17_P_CC	HA14_N	HA15_P	HA16_N	NC	GND
17	HA17_N_CC	GND	HA15_N	GND	NC	GND
18	GND	HA18_P	GND	HA20_P	GND	NC
19	HA21_P	HA18_N	HA19_P	HA20_N	GND	NC
20	HA21_N	GND	HA19_N	GND	NC	GND
21	GND	HA22_P	GND	HB03_P	NC	GND
22	HA23_P	HA22_N	HB02_P	HB03_N	GND	NC
23	HA23_N	GND	HB02_N	GND	GND	NC
24	GND	HB01_P	GND	HB05_P	NC	GND
25	HB00_P_CC	HB01_N	HB04_P	HB05_N	NC	GND
26	HB00_N_CC	GND	HB04_N	GND	GND	NC
27	GND	HB07_P	GND	HB09_P	GND	NC
28	HB06_P_CC	HB07_N	HB08_P	HB09_N	NC	GND
29	HB06_N_CC	GND	HB08_N	GND	NC	GND
30	GND	HB11_P	GND	HB13_P	GND	NC
31	HB10_P	HB11_N	HB12_P	HB13_N	GND	NC
32	HB10_N	GND	HB12_N	GND	NC	GND
33	GND	HB15_P	GND	HB19_P	NC	GND
34	HB14_P	HB15_N	HB16_P	HB19_N	GND	NC
35	HB14_N	GND	HB16_N	GND	GND	NC
36	GND	HB18_P	GND	HB21_P	NC	GND
37	HB17_P_CC	HB18_N	HB20_P	HB21_N	NC	GND
38	HB17_N_CC	GND	HB20_N	GND	GND	NC
39	GND	NC	GND	VADJ	GND	NC
40	NC	GND	VADJ	GND	NC	GND

Table 37: FMC Connector Rows ABEFJK

FMC Connector Signal Definition

Mnemonic	Signal Definition
CLK[0,1]_C2M_P, CLK[0,1]_C2M_N	Each differential pair that is assigned for a clock signal, which is driven from the carrier card to the IO Mezzanine Module
CLK[0,1]_M2C_P, CLK[0,1]_M2C_N	Each differential pair that is assigned for a clock signal, which is driven from the IO Mezzanine Module to the carrier card
GA[0..1]	These signals provide geographical addressed of the module and are used for I2C channel select
GND	This is signal ground
HA[00..23]_P HA[00..23]_N	User defined signals on Bank A located on the HPC
HB[00..21]_P HB[00..21]_N	User defined signals on Bank B located on the HPC
LA[00..33]_P LA[00..33]_N	User defined signals on Bank A located on the LPC and HPC
NC	Not Connected
PG_C2M	Power Good Carrier Card. This signal asserts high by the carrier card when power supplies, VADJ, 12P0V, 3P3V, are within tolerance
PG_M2C	Power Good Mezzanine. This signal is routed to an input pin of the FPGA.
PRSNT_M2C_L	Module present signal. This signal allows the carrier to determine whether an IO Mezzanine module is present
SCL, SDA	System Management I2C serial clock and serial data. These signals provide a data line for a two-wire serial management bus
TRST_L, TCK, TMS, TDI, TDO	TAG Reset, Clock, Mode Select, Data In and Data Out signal. The JTAG signals onto the FMC connector of the VX3830 are not activated.
VADJ	These pins carry an adjustable voltage level power from the carrier to the IO Mezzanine module
VREF_A_M2C	This is the reference voltage associated with the signaling standard used by the bank A data pins, LAxx and HAxx. On the VX3830 this signal is routed to the FPGA.
12P0V	These pins carry 12V power from the carrier to the IO Mezzanine module
3P3VAUX	A 3.3V auxiliary power supply.
3P3V	These pins carry 3.3V power from the carrier to the IO Mezzanine module

4.6.3 FMC IO Routing

FPGA to FMC			FMC to P2			
FMC connector pin	FMC signal definition	FPGA pin	FMC connector pin	FMC signal definition	P2 connector pin	P2 signal definition
C10	LA6_P	J17	J15	HA14_P	C1	PMC1 IO 1
C11	LA6_N	K17	J16	HA14_N	C2	PMC1 IO 3
C14	LA10_P	N16	J18	HA18_P	C3	PMC1 IO 5
C15	LA10_N	M16	J19	HA18_N	C4	PMC1 IO 7
C18	LA14_P	R15	J21	HA22_P	C9	PMC1 IO 17
C19	LA14_N	R16	J22	HA22_N	C10	PMC1 IO 19
C22	LA18_P	C15	J24	HB1_P	C13	PMC1 IO 25
C23	LA18_N	B15	J25	HB1_N	C14	PMC1 IO 27
C26	LA27_P	E17	J27	HB7_P	C15	PMC1 IO 29
C27	LA27_N	E16	J28	HB7_N	C16	PMC1 IO 31
D11	LA5_P	H15	J30	HB11_P	C17	PMC1 IO 33
D12	LA5_N	H16	J31	HB11_N	C18	PMC1 IO 35
D14	LA9_P	L18	J33	HB15_P	C19	PMC1 IO 37
D15	LA9_N	L17	J34	HB15_N	C20	PMC1 IO 39
D17	LA13_P	P14	J36	HB18_P	C31	PMC1 IO 61
D18	LA13_N	P15	J37	HB18_N	C32	PMC1 IO 63
D20	LA17_P	F16	K16	HA17_P	C5	PMC1 IO 9
D21	LA17_N	G16	K17	HA17_N	C6	PMC1 IO 11
D23	LA23_P	B14	K19	HA21_P	C7	PMC1 IO 13
D24	LA23_N	A14	K20	HA21_N	C8	PMC1 IO 15
D26	LA26_P	E15	K22	HA23_P	C11	PMC1 IO 21
D27	LA26_N	D15	K23	HA23_N	C12	PMC1 IO 23
D8	LA1_P	M14	K25	HB0_P	C21	PMC1 IO 41
D9	LA1_N	L13	K26	HB0_N	C22	PMC1 IO 43
G10	LA3_N	G18	K28	HB6_P	C23	PMC1 IO 45
G12	LA8_P	L14	K29	HB6_N	C24	PMC1 IO 47
G13	LA8_N	K14	K31	HB10_P	C25	PMC1 IO 49
G15	LA12_P	N13	K32	HB10_N	C26	PMC1 IO 51
G16	LA12_N	M13	K34	HB14_P	C27	PMC1 IO 53
G18	LA16_P	N12	K35	HB14_N	C28	PMC1 IO 55
G19	LA16_N	M11	K37	HB17_P	C29	PMC1 IO 57
G21	LA20_P	A11	K38	HB17_N	C30	PMC1 IO 59
G22	LA20_N	A12	E15	HA16_P	A1	PMC1 IO 2
G24	LA22_P	B13	E16	HA16_N	A2	PMC1 IO 4
G25	LA22_N	A13	E18	HA20_P	A3	PMC1 IO 6
G27	LA25_P	E14	E19	HA20_N	A4	PMC1 IO 8
G28	LA25_N	F14	E21	HB3_P	A9	PMC1 IO 17
G30	LA29_P	D18	E22	HB3_N	A10	PMC1 IO 20
G31	LA29_N	D17	E24	HB5_P	A11	PMC1 IO 22
G33	LA31_P	G14	E25	HB5_N	A12	PMC1 IO 24
G34	LA31_N	G15	E27	HB9_P	A13	PMC1 IO 26
G36	LA33_P	D12	E28	HB9_N	A14	PMC1 IO 28
G37	LA33_N	E12	E30	HB13_P	A15	PMC1 IO 30
G6	LA0_P	N18	E31	HB13_N	A16	PMC1 IO 32

FPGA to FMC			FMC to P2			
FMC connector pin	FMC signal definition	FPGA pin	FMC connector pin	FMC signal definition	P2 connector pin	P2 signal definition
G7	LA0_N	M18	E33	HB19_P	A17	PMC1 IO 34
G9	LA3_P	H17	E34	HB19_N	A18	PMC1 IO 36
H10	LA4_P	H18	E36	HB21_P	A19	PMC1 IO 38
H11	LA4_N	J18	E37	HB21_N	A20	PMC1 IO 40
H13	LA7_P	J15	F16	HA15_P	A5	PMC1 IO 10
H14	LA7_N	K15	F17	HA15_N	A6	PMC1 IO 12
H16	LA11_P	N15	F19	HA19_P	A7	PMC1 IO 14
H17	LA11_N	M15	F20	HA19_N	A8	PMC1 IO 16
H19	LA15_P	P18	F22	HB2_P	A20	PMC1 IO 41
H20	LA15_N	N17	F23	HB2_N	A21	PMC1 IO 44
H22	LA19_P	A18	F25	HB4_P	A23	PMC1 IO 46
H23	LA19_N	A17	F26	HB4_N	A24	PMC1 IO 48
H25	LA21_P	B11	F28	HB8_P	A25	PMC1 IO 50
H26	LA21_N	C11	F29	HB8_N	A26	PMC1 IO 52
H28	LA24_P	D13	F31	HB12_P	A27	PMC1 IO 54
H29	LA24_N	D14	F32	HB12_N	A28	PMC1 IO 56
H31	LA28_P	F18	F34	HB16_P	A31	PMC1 IO 62
H32	LA28_N	F17	F35	HB16_N	A32	PMC1 IO 64
H34	LA30_P	C18	F37	HB20_P	A29	PMC1 IO 58
H35	LA30_N	B18	F38	HB20_N	A30	PMC1 IO 60
H37	LA32_P	B16				
H38	LA32_N	A16				
H7	LA2_P	H13				
H8	LA2_N	J14				
H4	CLK0_M2C_P	T9				
H5	CLK0_M2C_N	U9				
G2	CLK0_C2M_P	T6				
G3	CLK0_C2M_N	R6				
K4	CLK1_M2C_P	P8				
K4	CLK1_M2C_N	P7				
J2	CLK1_C2M_P	T7				
J3	CLK1_C2M_N	R7				

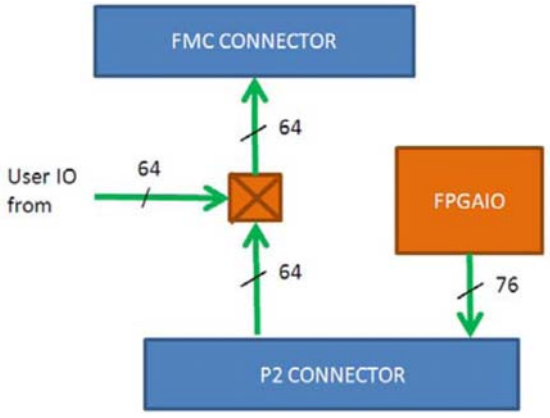


Figure 42: FMC IO Routing

4.6.4 JTAG/SPI Programmation P6 Connector Pin Assignment

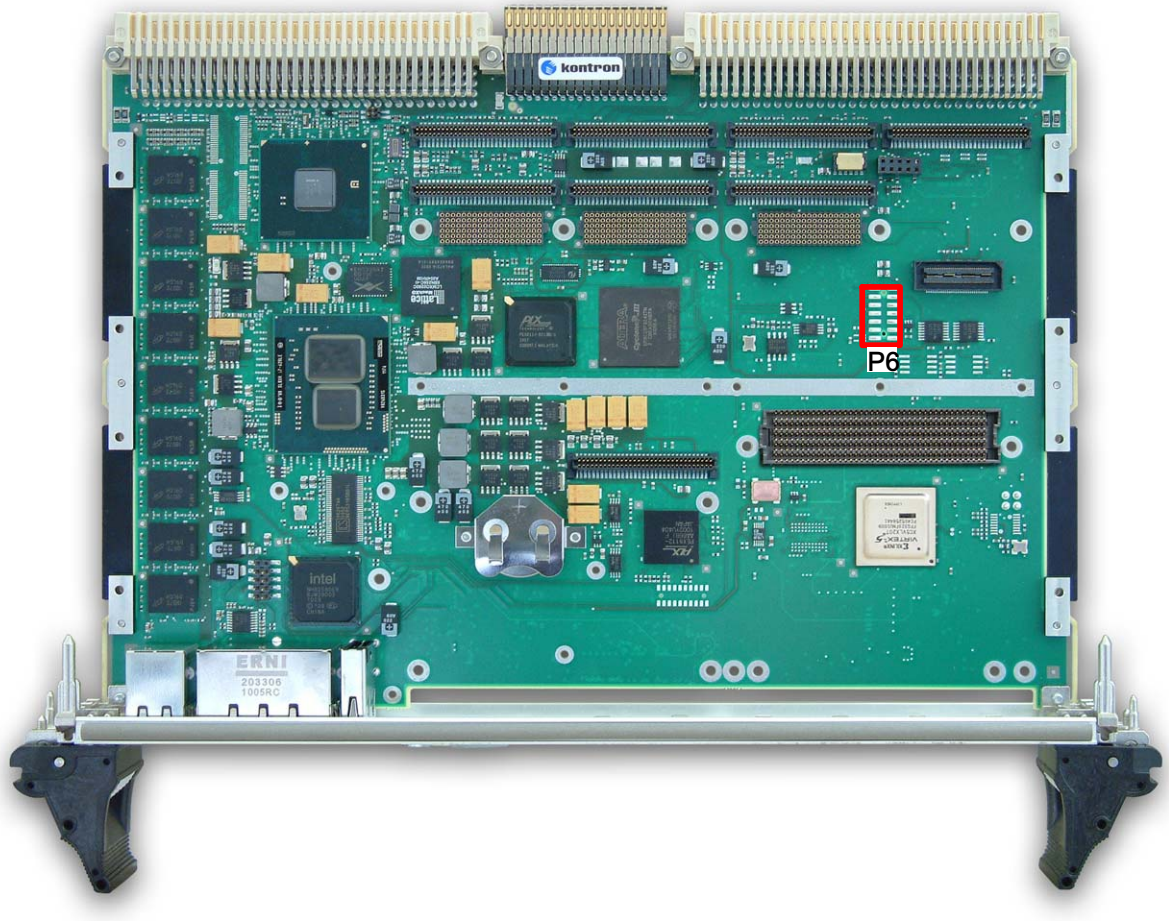


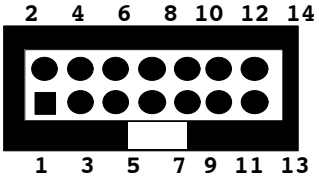
Figure 43: Location of the JTAG/SPI Connector

The JTAG/SPI connector is a 14-pin HE10 connector.

JTAG/SPI Connector Pin Assignment

Pin	Signal	Description
1	N.C.	Not Connected
2	P3V3	+3.3V
3	GND	Ground
4	TMS or $\overline{SS}$	JTAG Test Mode Select Slave Select
5	GND	Ground
6	TCK or SCLK	JTAG Test Clock Serial Clock
7	GND	Ground
8	TDO or MISO	JTAG Test Data Out MASTER IN, SLAVE OUT
9	GND	Ground
10	TDI or MOSI	JTAG Test Data In MASTER OUT, SLAVE IN
11	GND	Ground
12 .. 14	N.C.	Not Connected

Table 38: JTAG/SPI Connector Pin Assigment



JTAG/SPI

Figure 44: Onboard JTAG/SPI Connector

4.7 Front IO Connector

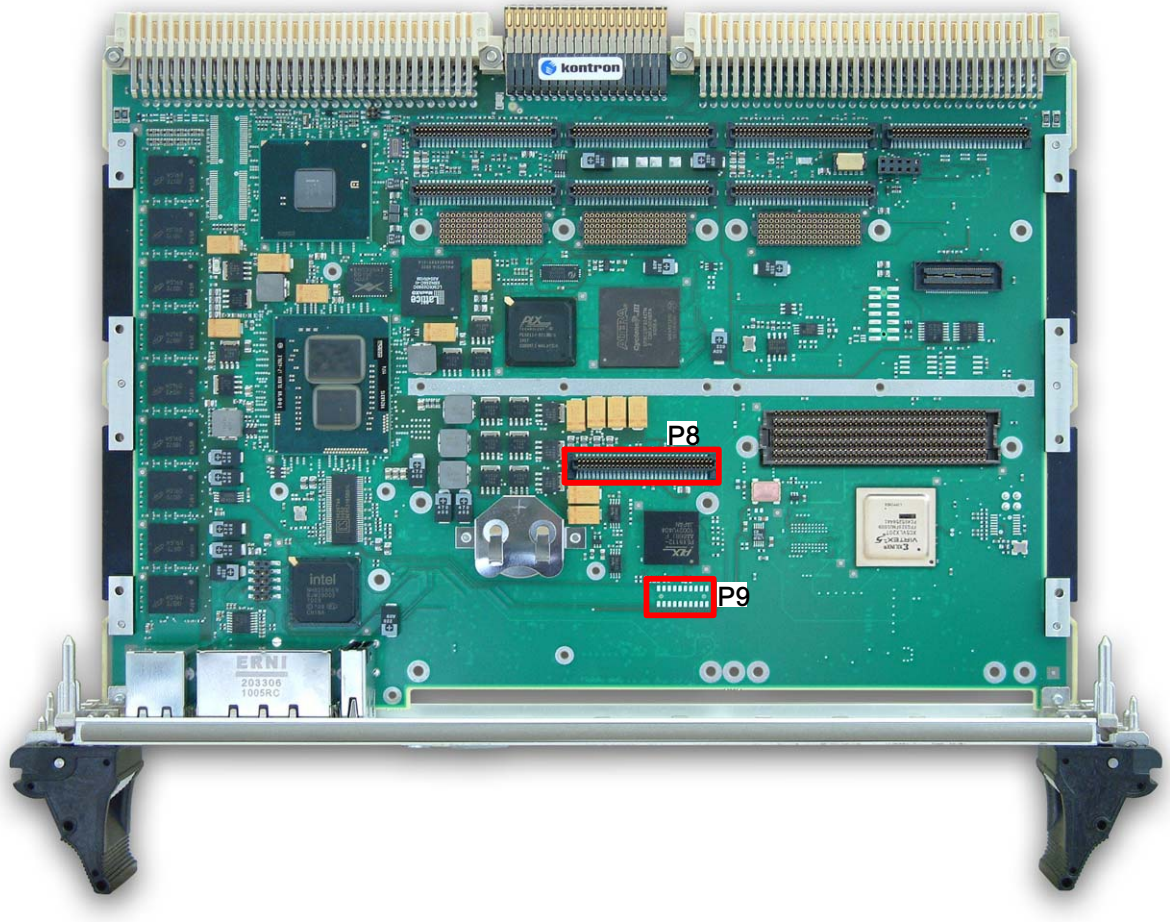


Figure 45: Location of the Front I/O Connector

The front IO connectors P8 and P9 are used to connect module board such as MOD-GX (Graphic Module board). These connectors are optional.

Front IO connectors are essentially provided to allow the installation of graphic module add and to offer graphic interfaces on front panel or on rear P0 connector.

Front IO connectors offer the following extra IO:

- 2 DisplayPort interfaces or HDMI/DVI interface using cable adaptor,
- 1 VGA interface,
- 2 USB ports,
- PCH I2C bus,
- High definition audio interface,
- 6 extra GPIOs.

4.7.1 P8 Pin Assignment

Front IO Pin	Signal	Front IO Pin	Signal
1	DPD_LANE3_P	2	+3.3VDC
3	DPD_LANE3_N	4	GND
5	**+5VDC**	6	DPB_LANE3_P
7	GND	8	DPB_LANE3_N
9	DPD_LANE2_P	10	**+3.3VDC**
11	DPD_LANE2_N	12	GND
13	**GND**	14	DPB_LANE2_P
15	+5VDC	16	DPB_LANE2_N
17	DPD_LANE1_P	18	**GND**
19	DPD_LANE1_N	20	GND
21	**+5VDC**	22	DPB_LANE1_P
23	GND	24	DPB_LANE1_N
25	DPD_LANE0_P	26	**+3.3VDC**
27	DPD_LANE0_N	28	GND
29	**GND**	30	DPB_LANE0_P
31	+5VDC	32	DPB_LANE0_N
33	DPD_AUX_P	34	**GND**
35	DPD_AUX_N	36	GND
37	**+5VDC**	38	DPB_AUX_P
39	DPD_HPD_Q	40	DPB_AUX_N
41	DPB_HPD_Q	42	**+3.3VDC**
43	USB_OC#_4_5	44	USB4P
45	**GND**	46	USB4N
47	USB5P	48	GND
49	USB5N	50	**GND**
51	ISO_CRTCLK	52	ISO_CRTDAT
53	**+5VDC**	54	GND
55	GND	56	CRT_RED
57	CRT_GREEN	58	**+3.3VDC**
59	GND	60	CRT_VSYNC
61	CRT_BLUE	62	GND
63	GND	64	CRT_HSYNC

4.7.2 P9 Pin Assignment

Front IO Pin	Signal	Front IO Pin	Signal
1	PCH_SMB_DAT	2	PCH_SMB_CLK
3	GND	4	GND
5	HDA_SDIN3	6	HDA_RST#
7	HDA_SDIN2	8	HDA_SYNC
9	HDA_SDIN1	10	HDA_BCLK
11	HDA_SDIN0	12	HDA_SDO
13	HDA_R_DOCKEN#	14	HDA_R_DOCKRST#
15	GPIO_P<0>	16	GPIO_P<1>
17	GPIO_N<0>	18	GPIO_N<1>
19	GPIO_P<2>	20	GPIO_N<3>

4.7.3 Front IO Signal Description

Mnemonic	Signal Definition
DPD_LANE_P/N [0...3]	Port D DisplayPort main link lane 0 to 3, support up to 2.7 Gb/s per lane
DPB_LANE_P/N [0...3]	Port B DisplayPort main link lane 0 to 3, support up to 2.7 Gb/s per lane
DPD_AUX_P/N	Port D DisplayPort Auxilliary channel (link device management)
DPB_AUX_P/N	Port B DisplayPort Auxilliary channel (link device management)
DPD_HPD_Q	Port D DisplayPort Hot Plug Detect
DPB_HPD_Q	Port B DisplayPort Hot Plug Detect
USBxP/N	Diffrential Data Pair of USB lines x
USB_OC#_4_5	USB over current interruption of line 4 and line 5
CRT_RED	RED Analog Video Ouptut
CRT_GREEN	GREEN Analog Video Ouptut
CRT_BLUE	BLUE Analog Video Ouptut
CRT_VSYNC	CRT Vertical Synchronisation
CRT_HSYNC	CRT Horizontal Synchronisation
ISO_CRTDAT	Monitor Control Data
ISO_CRTCLK	Monitor Control Clock
GND	Ground
+5VDC	
+3.3VDC	

Mnemonic	Signal Definition
PCH_SMB_DAT	PCH I2C serial data - see section 3.2 page 45
PCH_SMB_CLK	PCH I2C serial clock - see section 3.2 page 45
HDA_SDINx	HDA serial data in from the codec
HDA_RST#	HDA reset master hardware reset to external codec
HDA_SYNC	HDA sync 48 KHz fixed rate sample sync to the codec
HDA_BCLK	HDA bit clock output 24 MHz serial data clock
HDA_SDO	HDA serial data out to the codec
HDA_R_DOCKEN#	HDA dock enable
HDA_R_DOCKRST#	HDA doc reset for the codec
GPIO_N/P<x>	General purpose to signal from VITA 57 FPGA

4.8 LEDs

Status LEDs Default Setting

There are five bicolor LEDs (Red/Green) on the front panel of the VM6050 6U VME board.

Figure 46: LEDs Front panel

CPU LED	COLOR	DESCRIPTION
L1	RED	Permanent error on CPU subsystem (CATERR)
	GREEN	Power-up start
	AMBER	Reset state on CPU subsystem
	BLINKING	CPLD activity (I2C, SMI or COM)
	OFF	No error, no CPLD activity
L2	RED	CPLD watchdog reset timer expired
	GREEN	Normal operation mode
	AMBER	Factory test mode
	BLINKING	SATA activity
	OFF	No error, no SATA activity
L3	RED	Processor Hot (Thermtrip) or CPU frequency limitation to 1.2 GHz
	GREEN	1000BaseT rear LAN link
	AMBER	10/100BaseT(X) rear LAN link
	BLINKING	LAN activity on rear
	OFF	No error, no rear LAN activity/link
L4	RED	PBIT failed
	GREEN	Normal operation mode
	AMBER	ALMA2f VME FPGA downloading
	BLINKING	PCI & VME buses activity
	OFF	No error, no PCI activity
L5	RED	Power failure
	GREEN	Normal operation mode
	AMBER	VITA57 FPGA downloading
	BLINKING	PCI-X activity
	OFF	No error, no PCI-X activity

Table 39: LEDs Description

Chapter 5 - Power and Thermal Specifications

5.1 Power Considerations

5.1.1 System Power

The considerations presented in the ensuing sections must be taken into account by system integrators when specifying the VM6050 system environment.

5.1.1.1 VM6050 Baseboard

The VM6050 board has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the VM6050 should be carefully tested to ensure compliance with these ratings.

Supply Voltage	Maximum Permitted Voltage
+3.3VDC	+3.6V
+5VDC	+6V
+12V/-12VDC (1)	+14V/-14V

(1) if required for mezzanine.

Table 40: Maximum Input Power

The maximum permitted voltage indicated in the table above must not be exceeded. Failure to comply with these figures may result in damage to your board.

The following table specifies the range of the different input power voltages within the board is functional. The VM6050 is not guaranteed to function if the board is not operating within the prescribed limits.

Input Supply Voltage	Absolute Range
+3.3V	3.25V min. to 3.45V max.
+5V	4.875V min to 5.25V max.
+12V (1)	11.64V min. to 12.6V max.
-12V (1)	-12.6V min. to -11.64V max.

(1) if required for mezzanine.

Table 41: DC Operational Input Voltage Ranges

5.1.1.2 5V only option

VM6050 has been designed for operating with 5V only power input. See section 1.2.3 page 7 for ordering information for this product option.

5.1.1.3 Backplane

Backplanes to be used with the VM6050 must be adequately specified. The backplane must provide optimal power distribution for the +3.3V, +5V and +12V power inputs. It is recommended to use only backplanes which have at least two power planes for the +3.3V and +5V voltages.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided. It is recommended to use Positronic or M-type connector backplanes and power supplies where possible.

5.1.1.4 Power Supply Units

Power supplies for the VM6050 must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires.

An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

As the design of the VM6050 has been optimized for minimal power consumption, the power supply unit shall be stable even without minimum load.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for die resistance variations.

» Tolerance

The following table provides information regarding the required characteristics for each board input voltage.

VOLTAGE	NOMINAL VALUE	TOLERANCE	MAX. RIPPLE (P-P)	REMARKS
5V	+5.0 VDC	+5%/-3%	50 mV	Main voltage
3.3V	+3.3 VDC	+5%/-3%	50 mV	Main voltage
+12V	+12 VDC	+5%/-5%	240 mV	Required
-12V	-12 VDC	+5%/-5%	240 mV	Not Required
V I/O (PCI) signalling voltage	+3.3 VDC	+5%/-3%	50 mV	
GND	Ground, not directly connected to potential earth (PE)			

Table 42: Input Voltage Characteristics

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

PMC site 1 and 2 are no 5V tolerant. VIO voltage must be +3.3 VDC

Regulation

The power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it went below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

5.1.2 Power Consumption

The power consumption tables below list the voltage and power specifications for the VM6050 board. The values were measured using an 8-slot passive VME backplane with two power supplies: one for the CPU, and the other for the hard disk.

The processor dissipates the majority of the thermal power.

The power consumption values indicated in the tables below can vary depending on the processor part and the ambient temperature. This can result in deviations of the power consumption values of up to 15%.

	Power Mode	Power Consumption	Current Drawn (1)	Test Condition
VM6050/SA Intel® Core™ i7-620LE @ 2 GHz, 4 GB SDRAM	Idle (2 GHz)	17W	2.75A 5V 1A 3.3V	Idle Linux (interfaces not used)
	Typical (2 GHz)	36W	6.5A 5V 1A 3.3V	Standard configuration (2x 1000B-T, 1x SATA, 2x USB) CPU running complex tests
	Maximum (2 GHz)	42W	7.5A 5V 1.5A 3.3V	All interfaces used (DisplayPort, 4x 1000B-T, 2x SATA, 2x USB, Keyboard, Mouse) CPU running complex tests and TAT 50% (2)

Table 43: VM6050 SA Board Power Consumption

	Power Mode	Power Consumption	Current Drawn (1)	Test Condition
VM6050/SA Intel® Core™ i7-620LE @ 2 GHz, 4 GB SDRAM 5V only mode	Idle (2 GHz)	13W	2.6A 5V	Idle Linux (interfaces not used)
	Maximum processor power (2 GHz)	40W	8A 5V	TAT 100% CPU load

Table 44: VM6050 SA 5V only Mode Power Consumption

VM6050 integrators should carefully review the power ratings before using VM6050 5V only mode in the 3 row VME system. Power dissipation must not exceed 36W including accessories (XMC, PMC, FMC, USB device or SATA onboard disk). Kontron assumes no responsibility for any damage to the VM6050 5V only or other equipment resulting from VM6050 5V only using in a system with 3 row VME. Please contact Kontron for more details.

	Board Load	Power Consumption	Current Drawn (1)	Test Condition
VM6050/SA Intel® Core™ i7-620LE @ 1.20 GHz, 4 GB SDRAM	Maximum processor power (1.2 GHz)	30W	5.2A 5V 1.2A 3.3V	All interfaces used (DisplayPort, 4x 1000BASE-T, 2x SATA, 2x USB, Keyboard, Mouse) CPU running complex tests and TAT 50% (2)

Table 45: VM6050 Power Consumption

	Board Load	Power Consumption	Current Drawn (1)	Test Condition
VM6050/WA Intel® Core™ i7-620LE @ 1.73 GHz, 4 GB SDRAM	Maximum processor power (1.73 GHz)	38W	6.6A 5V 1.5A 3.3V	TAT 100% CPU load

Table 46: VM6050 WA Board Power Consumption

	Board Load	Power Consumption	Current Drawn (1)	Test Condition
VM6050/RA Intel® Core™ i7-620LE @ 1.60 GHz, 4 GB SDRAM	Maximum processor power (1.60 GHz)	36.5W	6.3A 5V 1.5A 3.3V	TAT 100% CPU load

Table 47: VM6050 RA Board Power Consumption

(1) Does not include current eventually supplied to PMC/XMC or external periphals like USB.

(2) This test is power consumption equivalent to thermal analysis tools from Intel with CPU Core workload level at 100%.

Current Draw VM6050-2SA34-00110	5V Rail	3.3V Rail
Maximum Current Draw	8A	1.7A
Peak Current Draw	TBD	TBD

Table 48: VM6050 Maximum Current Draw

5.1.3 Maximum Power Consumption of PMC Module

A maximum power of 7.5W is available on each PMC slot. This is in accordance with the draft standard P1386/Draft 2.4a. The maximum power of 7.5W can be arbitrarily divided on the 3.3V and 5V voltage lines.

PMC site 1 and 2 are no 5V VIO tolerant. PMC VIO voltage must be +3.3 VDC.

The following table indicates the current of a PMC module.

VOLTAGE	CONTINUOUS CURRENT	PEAK CURRENT
3.3V	2.27A	4.5A
5V	1.5A	3.0A
+12V	0.5A	0.5A
-12V	0.4A	0.4A

Table 49: Current of a PMC Module

5.1.4 Maximum Power Consumption of XMC Modules

A maximum power of 7.5W is available on each XMC slot and it can be arbitrarily divided on the 3.3V and 5V (VPWR) voltage lines. XMC modules are based on 3.3V power along with variable power (VPWR) defined as either 5V or 12V in the ANSI/VITA 42.0-200x XMC Switched Mezzanine Card Auxiliary Standard specification. On the VM6050, the VPWR is configured to 5 V.

The following table indicates the current of a XMC module.

VOLTAGE	CONTINUOUS CURRENT	PEAK CURRENT
3.3V	0.75A	3.0A
5V (VPWR)	2.5A	2.5A
+12V (including VPWR option)	0.75A	1.3A
-12V	0.4A	0.4A

Table 50: Current of a XMC Module

XMC integrators should carefully review the power ratings, cooling capacity and airflow requirements in the application prior to installation of an XMC module on the VM6050.

5.2 Thermal Consideration

The following chapter provide system integrators with the necessary information to satisfy thermal and airflow requirements when implementing VM6050 applications (see specific chapter for RC class).

5.2.1 Board Thermal Monitoring

To ensure optimal and long-term reliability of the VM6050, all onboard components must remain within the maximum temperature specifications. The most critical components on the VM6050 are the processor and the memory. Operating the VM6050 above the maximum operating limits will result in permanent damage to the board.

The VM6050 includes several temperature sensors to measure the onboard temperature values:

- Thermal sensors integrated in the processor
- Three on-board temperature sensors

The three onboard temperature sensors (Texas Instrument part LM73) are located on the I^2C bus, and managed by the CPLDs. Refer to Figure 29 “I2C Diagram” page 45.

Key Features of the onboard Temperature Sensors

- Local temperature accuracy: +/- 2°C.
- Operating temperature: -40 °C / +150°C.
- I2C address:

Board sensors	#1	#2	#3
I2C address	48	49	4A

Location of the onboard Temperature Sensors

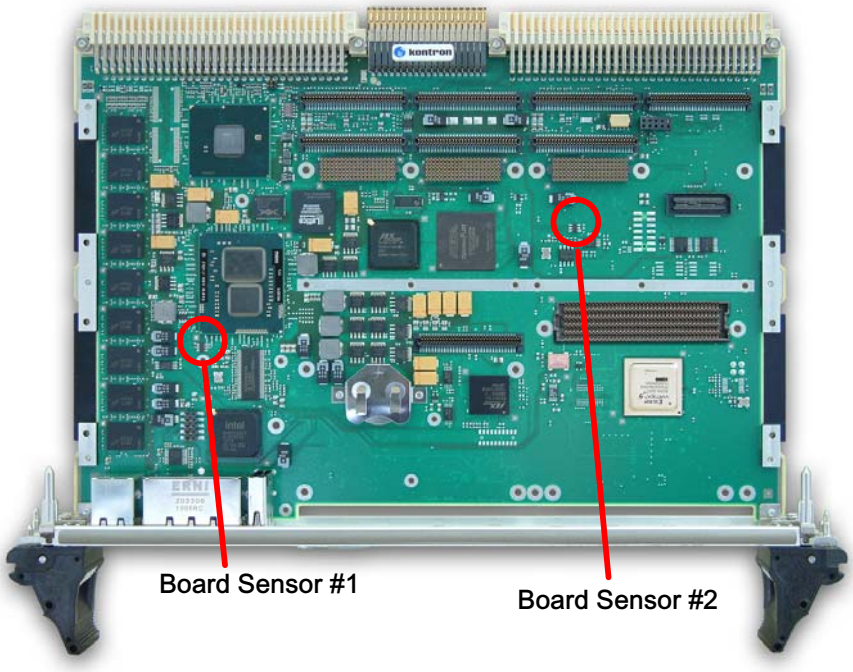


Figure 47: Board Temperature Sensors Location on top side of the Board

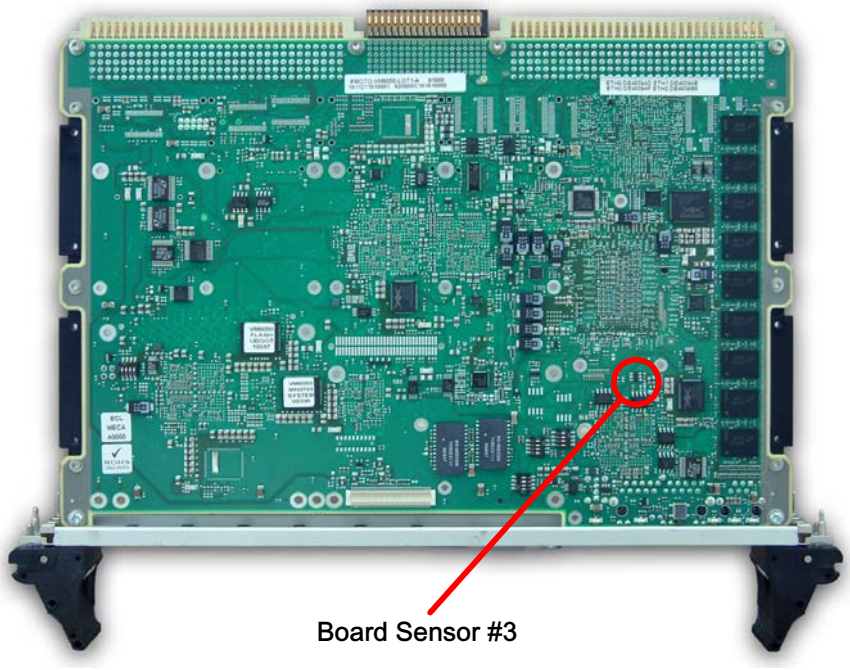


Figure 48: Board Temperature Sensors Location on bottom side of the Board

5.2.2 Processor Thermal Monitoring

To allow optimal operation and long-term reliability of the VM6050, the 2nd generation Intel® Core™ i7 processor must remain within the maximum die temperature specifications. The maximum operating temperature for the processor die is 105°C (100°C for graphix die).

The 2nd generation Intel® Core™ i7 processor uses the Adaptive Thermal Monitor feature to protect the processor from overheating and includes the following on-die temperature sensors:

- One Digital Thermal Sensor (DTS) for monitoring each processor core
- One Digital Thermal Sensor (DTS) for monitoring the graphics core
- One Digital Thermal Sensor (DTS) for monitoring the die temperature
- Catastrophic Cooling Failure Sensor (THERMTRIP#)

These sensors are integrated in the processor and work without any interoperability of the uEFI BIOS or the software application. Thermal Control Circuit allows the processor to maintain a safe operating temperature without the need for special software drivers or interrupt handling routines.

» Digital Thermal Sensor (DTS)

The 2nd generation Intel® Core™ i7 processor includes four on-die Digital Thermal Sensors (DTS), two for the processor cores, one for the graphics core and one for the package die. They can be read via an internal register of the processor. The temperature returned by the Digital Thermal Sensor will always be at or below the maximum operating temperature (105°C). Via the Digital Thermal Sensors, the uEFI BIOS or the application software can measure the processor die temperature.

Adaptive Thermal Monitor

The Adaptive Thermal Monitor feature reduces the processor power consumption and the temperature when the processor silicon exceeds its maximum operating temperature until the processor operates at or below its maximum operating temperature.

The processor core power reduction is achieved by:

- Frequency/sVID Control (by reducing of processor core voltage)
- Clock Modulation (by turning the internal processor core clocks off and on)

Adaptive Thermal Monitor dynamically selects the appropriate method. uEFI BIOS is not required to select a specific method as with previous-generation processors supporting Intel® Thermal Monitor 1 (TM1) and Intel® Thermal Monitor 2 (TM2).

The Adaptive Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

Frequency/sVID Control

Frequency/sVID Control reduces the processor's operating frequency (using the core ratio multiplier) and the input voltage (using serial VID signals). This combination of lower frequency and VID results in a reduction of the processor power consumption.

When the processor temperature reaches the TCC activation point, the event is reported to the bit PROCHOT of the CPLD register Alert Control & Status (0x85B). Refer to chapter 3.3 page 46 for register description.

Running the processor at the lower frequency and voltage will reduce power consumption and should allow the processor to cool off. If the processor temperature does not drop below its maximum operating temperature, a second frequency and voltage transition will take place.

This sequence of temperature checking and Frequency/sVID reduction will continue until either the minimum frequency has been reached or the processor temperature has dropped below its maximum operating temperature. If the processor temperature remains above its maximum operating temperature even after the minimum frequency has been reached, then Clock Modulation at that minimum frequency will be initiated.

When the LED3 on the front panel is lit red after boot-up, it indicates that the processor die temperature is above 105°C.

Clock Modulation

Clock Modulation reduces power consumption by rapidly turning the internal processor core clocks off and on at a duty cycle that should reduce power dissipation (typically a 30-50% duty cycle).

Once the temperature has dropped below the maximum operating temperature, the TCC goes inactive and clock modulation ceases.

When the LED3 on the front panel is lit red after boot-up, it indicates that the processor die temperature is above 105°C.

Catastrophic Cooling Failure Sensor

The Catastrophic Cooling Failure Sensor protects the processor from catastrophic overheating.

The Catastrophic Cooling Failure Sensor threshold is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130°C. Once activated, the event remains latched until the VM6050 undergoes a power-on restart (all power off and then on again).

This function cannot be enabled or disabled in the uEFI BIOS. It is always enabled to ensure that the processor is protected in any event.

5.2.3 Chipset Thermal Monitor Feature

The Intel® QM57 Chipset includes one on-die Thermal Diode Sensor to measure the chipset die temperature. The maximum Intel® QM57 Chipset junction temperature is 108°C.

5.2.4 External Thermal Regulation

To ensure the best possible basis for operational stability and long-term reliability, the VM6050 is equipped with a heat sink (SA and WA classes only). Coupled together with system chassis, which provides variable configurations for forced airflow, controlled active thermal energy dissipation is guaranteed.

The physical size, shape, and construction of the heat sink and ensures the lowest possible thermal resistance. In addition, the VM6050 has been specifically designed to efficiently support forced airflow as found in modern VME systems.

Thermal Characteristic Graphs

The thermal characteristic graphs shown in the following sections illustrate the maximum ambient air temperature as a function of the volumetric airflow rate for the processor frequency indicated.

The diagrams are intended to serve as guidance for reconciling board and system with the required computing power/frequency considering the thermal aspect. Two diagrams are provided, the first for VM6050 SA and WA classes, the second for RA class. There are several curves representing upper level working points based on processor frequency. When operating below the corresponding curve, the CPU runs steadily without any intervention of thermal supervision. When operated above the corresponding curve, various thermal protection mechanisms may take effect resulting in temporarily reduced CPU performance or finally in an emergency stop in order to protect the CPU and the chipset from thermal destruction. In real applications this means that the board can be operated temporarily at a higher ambient temperature or at a reduced flow rate and still provide some margin for temporarily requested peak performance before thermal protection will be activated.

How to read the Diagram

Select a board class, a processor frequency and choose a specific working point. For a given flow rate there is a maximum airflow input temperature (= ambient temperature) provided. Below this operating point, thermal supervision will not be activated. Above this operating point, thermal supervision will become active protecting the CPU from thermal destruction. The minimum airflow rate provided must be higher than the value specified in the diagram.

In addition, some margin must be applied to prevent processor power dispersion and/or tolerance and in case of processor workload higher than typical customer application.

Values indicated in these graphs are issue from Thermal Analysis Tool from Intel with 80% of processor workload. This benchmark is representative of most of customer's applications in term of thermal dissipation.

Volumetric Flow Rate

The volumetric flow rate refers to an airflow through a fixed cross-sectional area (i.e. slot width x depth). The volumetric flow rate is specified in cfm (cubic-feetper- minute).

Airflow

At a given cross-sectional area and a required flow rate, an average, homogeneous airflow speed can be calculated using the following formula:

Airflow = Volumetric Flow Rate / Area

The airflow is specified in m/s (meter-per-second).

Airflow Direction

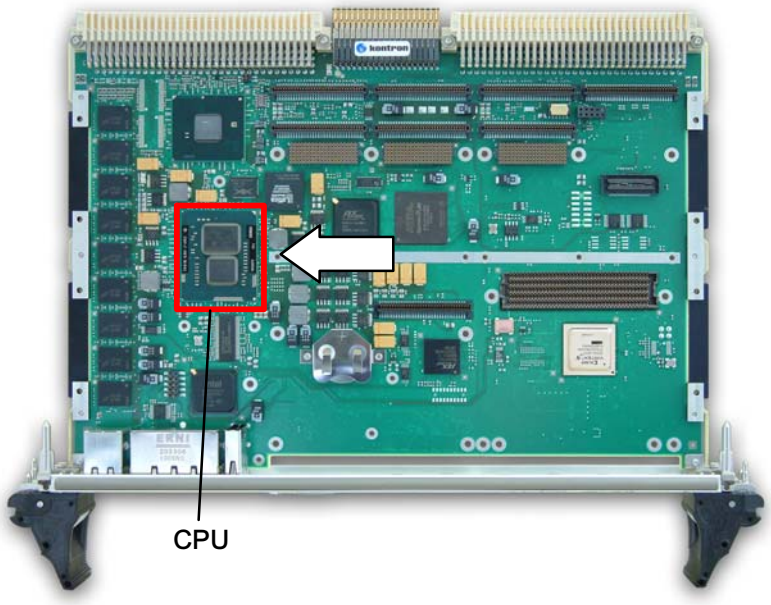


Figure 49: Airflow Direction

5.2.4.1 Operational Limits for the VM6050

The following figures illustrate the operational limits of the VM6050 for typical customer application taking into consideration processor frequency vs. ambient air temperature vs. airflow rate. The measurements were made based on a 4HP slot (0.8 inch height) and using Thermal Analysis Tool from Intel with 80% of processor workload without graphics operation.

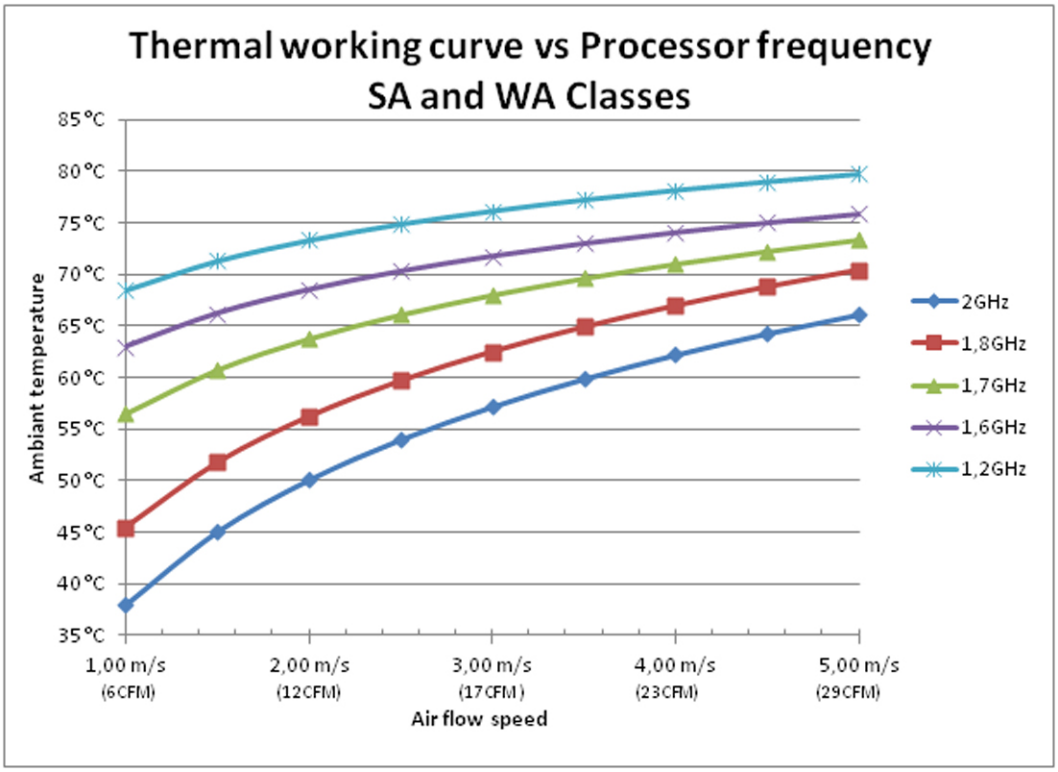


Figure 50: VM6050 SA/WA Thermal Performance

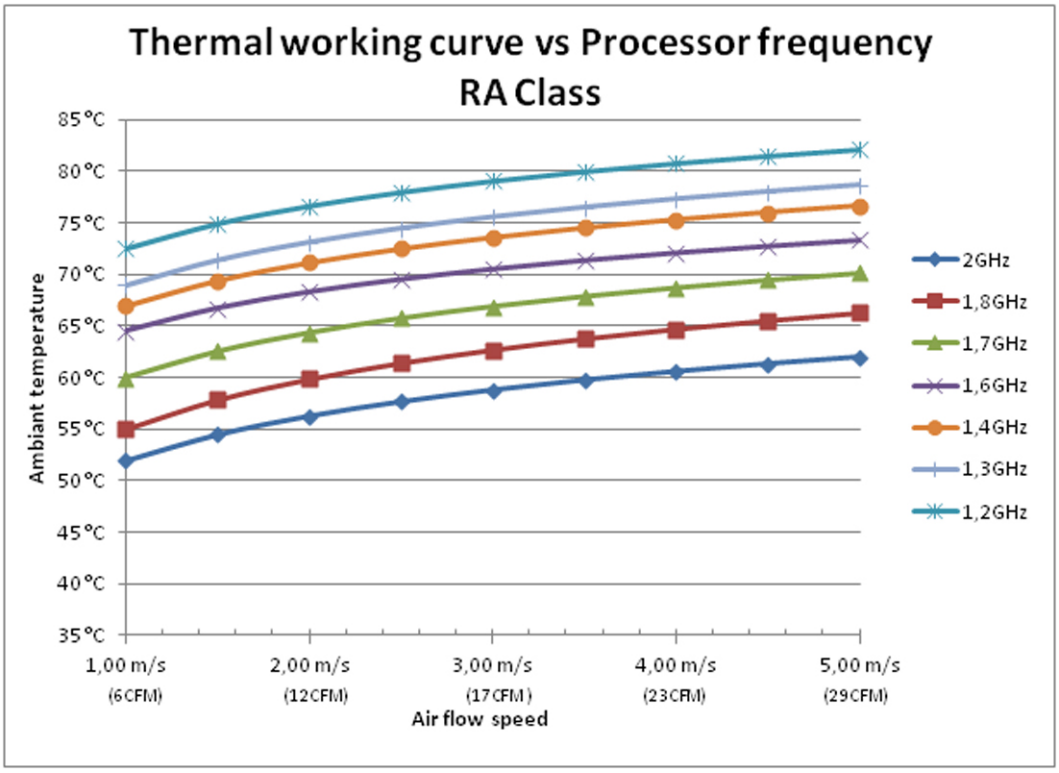


Figure 51: VM6050 RA Thermal Performance

Default frequency

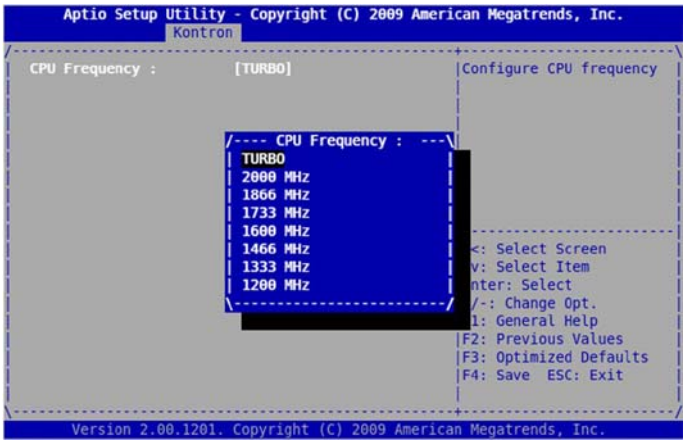
Default frequency on VM6050 board depends on class board to satisfy operating temperature. With this default setting, the VM6050 processing performance is guaranteed across the whole operating temperature range. The VM6050 thermal design is such as the processor, running at this frequency does not enter thermal management mode (frequency throttling) when the processor temperature is maintained within the approved operating range.

Frequency	VM6050 SA	VM6050 WA
2.00 GHz	2.8 m/s (16CFM) (1)	
1.73 GHz		2.5 m/s (14CFM) (1)

(1) Default frequency

Refer to section 8.2 page 145 for VM6050 RA class default frequency.

> The processor frequency is handled by the BIOS through the CPU configuration menu.



Refer to the AMI BIOS for VM6050 - User Reference Manual (SD.DT.F89), section “CPU Configuration”.

Intel® Turbo Boost Technology

Intel® Turbo Boost Technology is one of the many exciting features that Intel has built into latest-generation Intel® microarchitecture. It automatically allows processor cores to run faster than the base operating frequency if it's operating below power, current, and temperature specification limits.

Dynamically increasing performance

Intel Turbo Boost Technology is activated when the Operating System (OS) requests the highest processor performance state (P0). The maximum frequency of Intel Turbo Boost Technology is dependent on the number of active cores. The amount of time the processor spends in the Intel Turbo Boost Technology state depends on the workload and operating environment.

Any of the following can set the upper limit of Intel Turbo Boost Technology on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency will dynamically increase by 133 MHz on short and regular intervals until the upper limit is met or the maximum possible upside for the number of active cores is reached.

Learn more about Intel Turbo Boost Technology: http://www.intel.com/technology/turboboost/

> The Intel Turbo Boost is handled by the BIOS through the CPU configuration menu.

5.2.4.2 Peripherals

When determining the thermal requirements for a given application, peripherals to be used with the VM6050 must also be considered. Devices such as MOD-GX, HDDs, SSDs, PMC modules, XMC modules, and SATA Flash modules which are directly attached to the VM6050 must also be capable of being operated at the temperatures foreseen for the application. It may very well be necessary to revise system requirements to comply with operational environment conditions.

In most cases, this will lead to a reduction in the maximum allowable ambient operating temperature or even require active cooling of the operating environment.

As Kontron assumes no responsibility for any damage to the VM6050 or other equipment resulting from overheating of the CPU, it is highly recommended that system integrators as well as end users confirm that the operational environment of the VM6050 complies with the thermal considerations set forth in this document.

Chapter 6 - Graphic Module Characteristics

6.1 Board Overview

Figure 52: MOD-GX Overview

6.1.1 Main Features

MOD-GX is a module board that is plugged on PMC slot 2 of VM6050 board. It offers three graphics interfaces in front panel of the VM6050, one VGA graphics interface and two mini DisplayPort interfaces.

» Dual-mode DisplayPort

MOD-GX and VM6050 boards are compliant with Dual-mode DisplayPort marked with a DP++ logo:

This mode allows to transmit single-link HDMI and DVI signals through DisplayPort cabling; this requires passive external adapters which convert to the higher signal levels used by DVI/HDMI.

Usually, Dual-mode DisplayPort chipset detects the DVI or HDMI passive adapter and switches to DVI/HDMI mode, this detection is performed by Cable Detect pin of DisplayPort connector (pin 13).

On VM6050 board, the Dual-mode switching is not automatic, Cable Detect pin is not used, the switching is performed by BIOS setting.

On graphic module, the Dual-mode switching is automatic, component of MOD-GX board manage Dual-mode signals using Cable Detect signal.

Note Dual-mode can only transmit single-link DVI/HDMI, as the number of pins in the DisplayPort connector is insufficient for dual-link connections.

» Video resolution

MOD-GX board uses repeater device to improve the signal integrity of Digital video Interface and allows to benefit the better resolution provided by graphic chipset inside Intel Core-i7 (2560 x 1600 @ 60 Hz for DP and 1920 x 1200 @ 60 Hz for HDMI/DVI) .

The maximum resolution available on VGA interface is 2048x1538 (QXGA format).

The maximum recommended resolution for DisplayPort and VGA is 1920 x 1080 @ 60 Hz.

Dual Display

Dual Display is available on the VM6050 board with MOD-GX. Dual display can be realized either by combining VGA interface with one of both DP interface or by combining both DP interfaces.

Main display can be chosen under BIOS setup. The main default display interface is VGA under Operating System at boot (Linux tested) and the main default interface is DisplayPort B under BIOS environment.

Rear Transition Module

Both DisplayPort are routed on the rear of the VM6050 board through the MOD-GX board. DisplayPort signals are redirected to the rear using configuration switches of MOD-GX. RTM and PIM module (PIM-2DP) offer the possibility to have these 2 DisplayPort interfaces on standard DisplayPort connector. Contact Kontron for availability of PIM-2DP module board.

6.1.2 Block Diagram

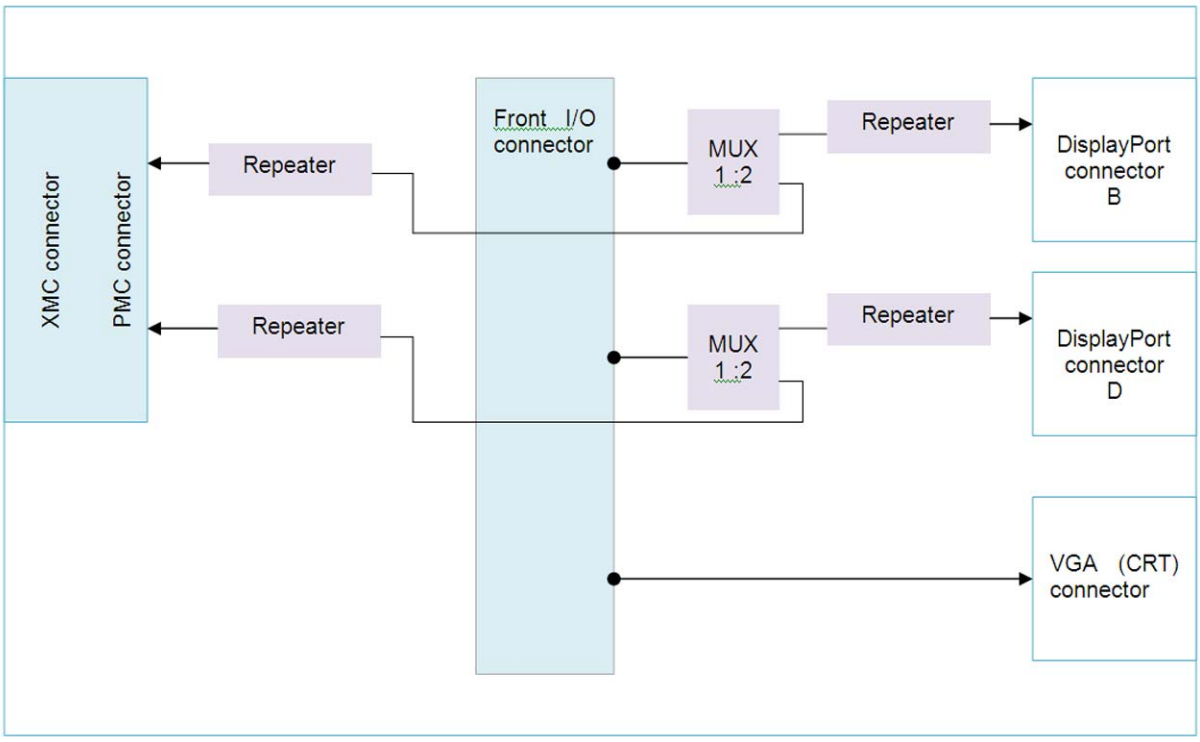


Figure 53: MOD-GX Block Diagram

6.1.3 Ordering Information

ORDER CODE	DESCRIPTION
MOD-GX-SA-00	Air cooled Graphics module with two DisplayPort on front panel
MOD-GX-RC-00	Conduction Cooled Graphics module with two DisplayPort on rear
PIM-2DP-000	Two DisplayPort PIM module

6.2 Installation of Graphic Module

6.2.1 Board identification

The MOD-GX boards are identified by labels fitted on the bottom side of the board.

Ⓐ “Identification” label: Order code, Serial Number, Variant, EC level

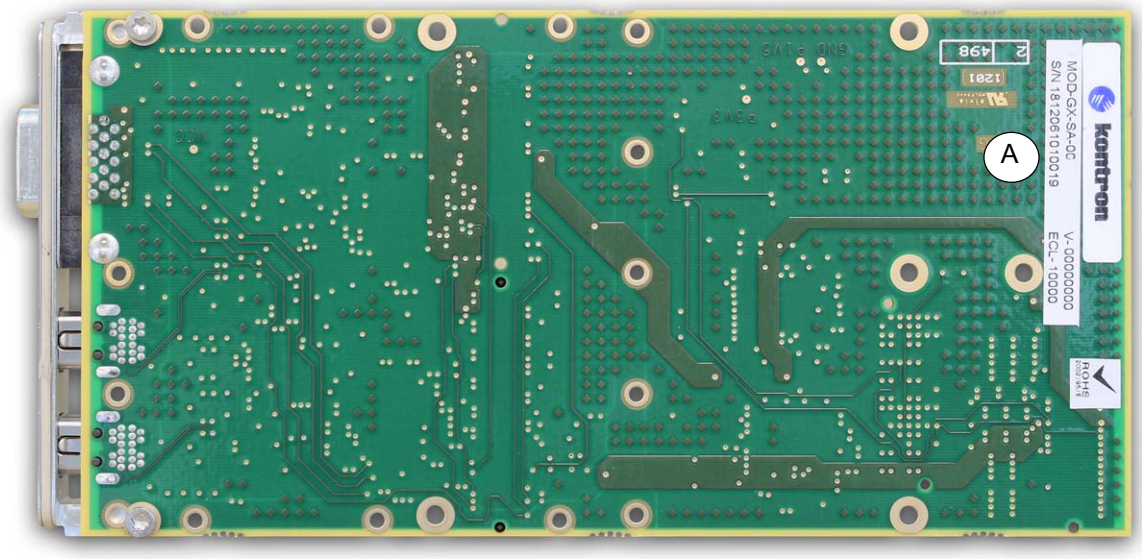


Figure 54: MOD-GX Identification Label Location

6.2.2 Microswitches Description

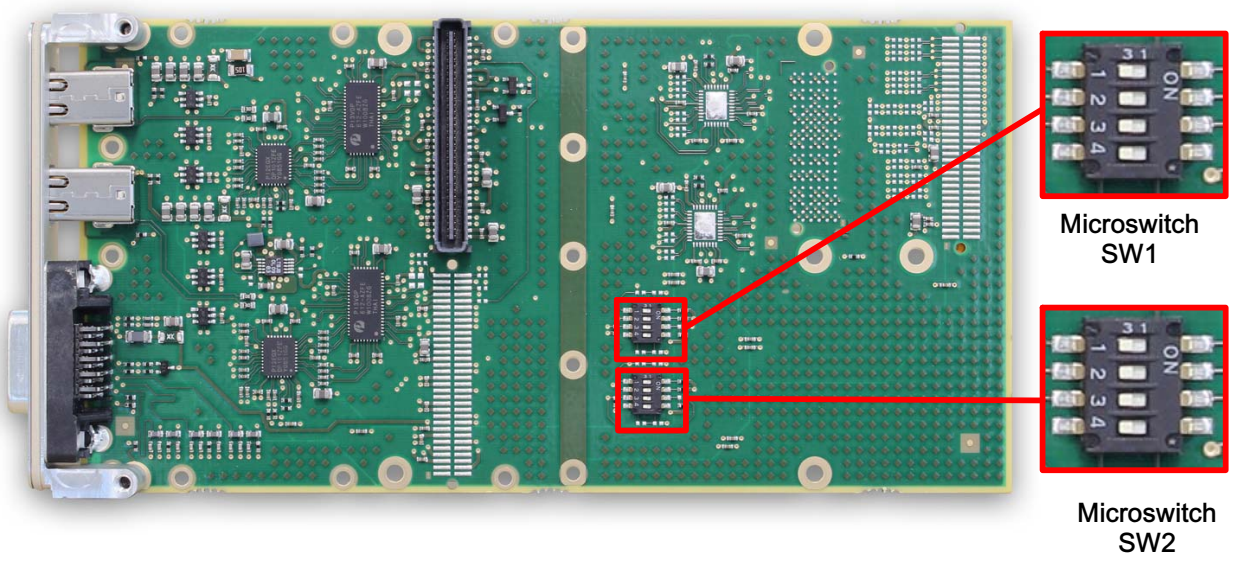


Figure 55: Microswitches Location on MOD-GX

SW1 switch is used for setting DisplayPort interface, port D from VM6050.

Function	Description
1 - Disable cable detect on Front	**on**: Force DisplayPort mode for DP D on front connector, disable cable detection **off**: Enable cable detection for DP D on front connector
2 - Disable cable detect on Rear	**on**: Force DisplayPort mode for DP D on rear connector, disable cable detection **off**: Enable cable detection for DP D on rear connector
3 - Front / Rear DisplayPort selection	**on**: DisplayPort D interface is routed to rear panel **off**: DisplayPort D interface is routed to front panel
4 - Not used	

SW2 switch is used for setting DisplayPort interface, port B from VM6050.

Function	Description
1 - Disable cable detect on Front	**on**: Force DisplayPort mode for DP B on front connector, disable cable detection **off**: Enable cable detection for DP B on front connector
2 - Disable cable detect on Rear	**on**: Force DisplayPort mode for DP B on rear connector, disable cable detection **off**: Enable cable detection for DP B on rear connector
3 - Front / Rear DisplayPort selection	**on**: DisplayPort B interface is routed to rear panel **off**: DisplayPort B interface is routed to front panel
4 - Not used	

6.3 Connectors

6.3.1 Front Panel Connectors

6.3.1.1 VGA Connector

The MOD-GX board integrates one VGA port available only on front panel.

Pin Assignment

Connector used for the analog video signals transmission is the DE-15.

PIN	SIGNAL NAME
1	CRT_RED
2	CRT_GREEN
3	CRT_BLUE
4	N.C.
5	GND
6	N.C.
7	N.C.
8	N.C.
9	+5V
10	GND
11	N.C.
12	CRT_DAT
13	CRT_HSYNC
14	CRT_VSYNC
15	CRT_CLK

(N.C.: Not connected)

Table 51: VGA Connector Pin Assignment on MOD-GX

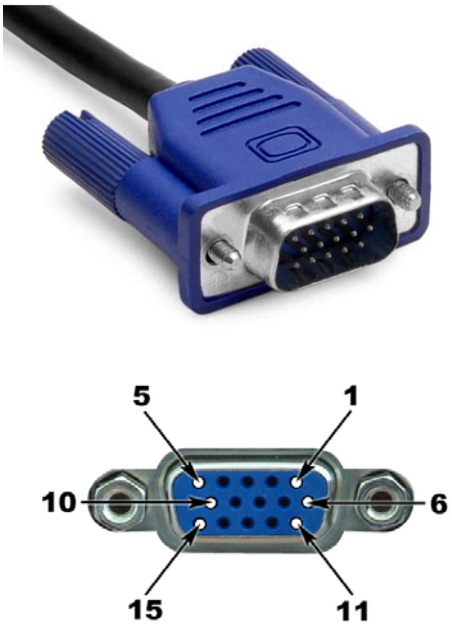


Figure 56: VGA Connector on MOD-GX

MNEMONIC	DESCRIPTION
CRT_RED	Red video signal
CRT_GREEN	Green video signal
CRT_BLUE	Blue Video signal
CRT_HSYNC	Horizontal synchronization video signal
CRT_VSYNC	Vertical synchronization video signal
GND	Ground
+5V	Power supply voltage
CRT_DAT	I2C Data bus
CRT_CLK	I2C clock bus

6.3.1.2 Mini DisplayPort Connectors

The MOD-GX board integrates two mini DisplayPort connectors (mDP) available on front panel and two DisplayPort available on rear using PIM-2DP with RTM module I/O board.
Pin assignment

PIN	SIGNAL NAME	I/O
1	GND	--
2	HPD	I
3	LANE_0P	O
4	CAD	I
5	LANE_ON	O
6	RSVD	--
7	GND	--
8	GND	--
9	LANE_1P	O
10	LANE_3P	O
11	LANE_1N	O
12	LANE_3N	O
13	GND	--
14	GND	--
15	LANE_2P	O
16	AUX_CH_P	I/O
17	LANE_2N	O
18	AUX_CH_N	I/O
19	GND	--
20	+3.3V	--

Table 52: Mini DisplayPort Connector Pin Assignment on MOD-GX

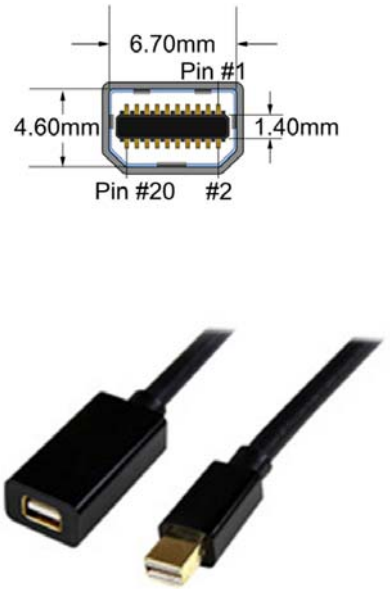
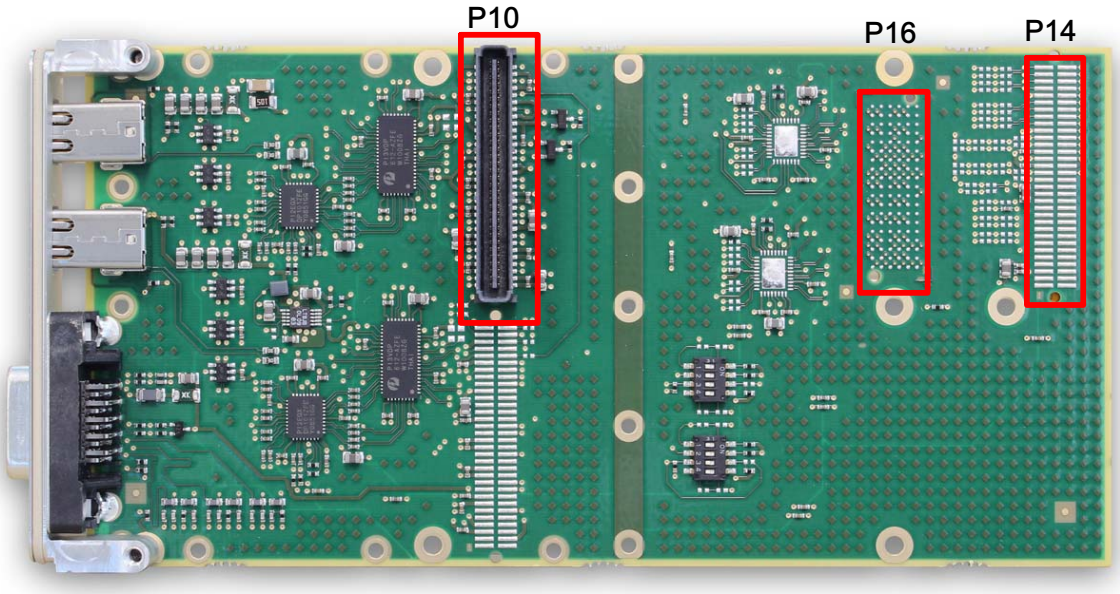


Figure 57: Mini DisplayPort Connector on MOD-GX

MNEMONIC	DESCRIPTION
LANE_xP/N	Display Port main link lane 0 to 3, support up to 2.7 Gb/s per lane
AUX_CH_P/N	Display Port Auxilliary channel (link device management)
HPD	Hot Plug Detect
CAD	Cable Detect
+3.3V	+3.3V power supply output
GND	GROUND

6.3.2 Onboard Connectors



6.3.2.1 Front IO Connector (P10)

This connector is used to interface MOD-GX board to VM6050 board. See also section 4.7 page 93 (Front I/O Connector) of this document.

Front IO pin	Signal	Front IO pin	Signal
1	DPD_LANE3_P	2	+3.3VDC
3	DPD_LANE3_N	4	GND
5	+5VDC	6	DPB_LANE3_P
7	GND	8	DPB_LANE3_N
9	DPD_LANE2_P	10	+3.3VDC
11	DPD_LANE2_N	12	GND
13	GND	14	DPB_LANE2_P
15	+5VDC	16	DPB_LANE2_N
17	DPD_LANE1_P	18	GND
19	DPD_LANE1_N	20	GND
21	+5VDC	22	DPB_LANE1_P
23	GND	24	DPB_LANE1_N
25	DPD_LANE0_P	26	+3.3VDC
27	DPD_LANE0_N	28	GND
29	GND	30	DPB_LANE0_P
31	+5VDC	32	DPB_LANE0_N
33	DPD_AUX_P	34	GND
35	DPD_AUX_N	36	GND
37	+5VDC	38	DPB_AUX_P
39	DPD_HPD_Q	40	DPB_AUX_N
41	DPB_HPD_Q	42	+3.3VDC

Front IO pin	Signal	Front IO pin	Signal
43	USB_OC#_4_5	44	USB4P
45	GND	46	USB4N
47	USB5P	48	GND
49	USB5N	50	GND
51	ISO_CRTCLK	52	ISO_CRTDAT
53	+5VDC	54	GND
55	GND	56	CRT_RED
57	CRT_GREEN	58	+3.3VDC
59	GND	60	CRT_VSYNC
61	CRT_BLUE	62	GND
63	GND	64	CRT_HSYNC

Mnemonic	Signal Definition
DPD_LANE_P/N [0...3]	Port D DisplayPort main link lane 0 to 3, support up to 2.7 Gb/s per lane
DPB_LANE_P/N [0...3]	Port B DisplayPort main link lane 0 to 3, support up to 2.7 Gb/s per lane
DPD_AUX_P/N	Port D DisplayPort Auxilliary channel (link device management)
DPB_AUX_P/N	Port B DisplayPort Auxilliary channel (link device management)
DPD_HPD_Q	Port D DisplayPort Hot Plug Detect
DPB_HPD_Q	Port B DisplayPort Hot Plug Detect
USBxP/N	Diffrential Data Pair of USB lines x
USB_OC#_4_5	USB over current interruption of line 4 and line 5
CRT_RED	RED Analog Video Ouptut
CRT_GREEN	GREEN Analog Video Ouptut
CRT_BLUE	BLUE Analog Video Ouptut
CRT_VSYNC	CRT Vertical Synchronisation
CRT_HSYNC	CRT Horizontal Synchronisation
ISO_CRTDAT	Monitor Control Data
ISO_CRTCLK	Monitor Control Clock
GND	Ground
+5VDC	
+3.3VDC	

6.3.3 XMC/PMC IO Pin Assignment

XMC or PMC IO connector (P16 and P14 connectors) are used to route DisplayPort signal of Port D and Port B to P0 in order to provide on rear of the VM6050 two graphic interfaces.

These connectors are fitted on MOD-GX-RC.

PMC IO Pin Assignment P14

PMC Pin	Signal	PMC Pin	Signal
33	DPB1_HPD	34	DPD1_HPD
35	DPBPWR	36	DPDPWR
37	DPB1_CAD	38	DPDPWR
39	DPBPWR	40	DPD1_AUXn
41	DPD1_AUXp	42	DPD1_CAD
43	DPB1_AUXn/CRT_GREEN*	44	DPB1_AUXp/CRT_RED*
45	GND	46	GND
47	DPB1_LANE3p	48	DPB1_LANE0p
49	DPB1_LANE3n	50	DPB1_LANE0n
51	DPB1_LANE2p	52	DPB1_LANE1p
53	DPB1_LANE2n	54	DPB1_LANE1n
55	GND	56	GND
57	DPD1_LANE3p/CRT_BLUE*	58	DPD1_LANE0p
59	DPD1_LANE3n	60	DPD1_LANE0n
61	DPD1_LANE2p/CRT_HSYNC*	62	DPD1_LANE1p/CRT_VSYNC*
63	DPD1_LANE2n	64	DPD1_LANE1n

PMC [1..32] pins are not connected

(*) VGA signal are available on customer request, default is DisplayPort signal

XMC IO Pin Assignment PJ16

XMC Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	DPD1_LANE0p	DPD1_LANE0n	GND	DPD1_LANE1p	DPD1_LANE1n	DPB1_HPD
2	GND	GND	NC	GND	GND	GND
3	DPD1_LANE2p	DPD1_LANE2n	GND	DPD1_LANE3p	DPD1_LANE3n	DPD1_HPD
4	GND	GND	NC	GND	GND	GND
5	NC	NC	DPBPWR	NC	NC	DPDPWR
6	GND	GND	NC	GND	GND	GND
7	NC	NC	DPB1_CAD	NC	NC	DPDPWR
8	GND	GND	NC	GND	GND	GND
9	NC	NC	DPBPWR	NC	NC	DPD1_AUXn
10	GND	GND	NC	GND	GND	GND
11	DPB1_LANE0p	DPB1_LANE0n	GND	DPB1_LANE1p	DPB1_LANE1n	DPD1_AUXp

XMC Pin	Row A	Row B	Row C	Row D	Row E	Row F
12	GND	GND	NC	GND	GND	GND
13	DPB1_LANE2p	DPB1_LANE2n	GND	DPB1_LANE3p	DPB1_LANE3n	DPD1_CAD
14	GND	GND	NC	GND	GND	GND
15	NC	NC	DPB1_AUXn	NC	NC	DPB1_AUXp
16	GND	GND	NC	GND	GND	GND
17	NC	NC	NC	NC	NC	NC
18	GND	GND	NC	GND	GND	GND
19	NC	NC	NC	NC	NC	NC

DisplayPort Routing to P0 Connector

PMC Pin	XMC Pin	Signal	P0	PMC Pin	XMC Pin	Signal	P0
33	F1	DPB1_HPD	B10	34	F3	DPD1_HPD	A10
35	C5	DPBPWR	E1	36	F5	DPDPWR	D1
37	C7	DPB1_CAD	C1	38	F7	DPDPWR	B1
39	C9	DPBPWR	A1	40	F9	DPD1_AUXn	E19
41	F11	DPD1_AUXp	D19	42	F13	DPD1_CAD	C19
43	C15	DPB1_AUXn	B19	44	F15	DPB1_AUXp	A19
45	C3	GND	C12	46	C1	GND	C11
47	D13	DPB1_LANE3p	D14	48	A11	DPB1_LANE0p	D11
49	E13	DPB1_LANE3n	E14	50	B11	DPB1_LANE0n	E11
51	A13	DPB1_LANE2p	D13	52	D11	DPB1_LANE1p	D12
53	B13	DPB1_LANE2n	E13	54	E11	DPB1_LANE1n	E12
55	C13	GND	C14	56	C11	GND	C13
57	D3	DPD1_LANE3p	A14	58	A1	DPD1_LANE0p	A11
59	E3	DPD1_LANE3n	B14	60	B1	DPD1_LANE0n	B11
61	A3	DPD1_LANE2p	A13	62	D1	DPD1_LANE1p	A12
63	B3	DPD1_LANE2n	B13	64	E1	DPD1_LANE1n	B12

Signal Description

MNEMONIC	SIGNAL DESCRIPTION
DPD1_LANExp/n	Port D Display Port main link lane 0 to 3, support up to 2.7 Gb/s per lane
DPB1_LANExp/n	Port B Display Port main link lane 0 to 3, support up to 2.7 Gb/s per lane
DPD1_AUXp/n	Port D Display Port Auxilliary channel (link device management)
DPB1_AUXp/n	Port B Display Port Auxilliary channel (link device management)
DPD1_HPD	Port D Display Port Hot Plug Detect
DPB1_HPD	Port B Display Port Hot Plug Detect
DPD1_CAD	Port D Cable Detect Signal
DPB1_CAD	Port B Cable Detect Signal
DPDPWR	Port D +3.3VDC power supply. Fuse protection on MOD-GX board.

DPBPWR	Port B +3.3VDC power supply. Fuse protection on MOD-GX board.
GND	Ground

6.4 Environmental Specifications

6.4.1 Environmental Specifications

	SA Standard Commercial	WA Extended Temperature	RC Rugged Conduction-Cooled
Conformal Coating	Optional	Standard	Standard
Temperature	VITA 47-Class AC1	VITA 47-Class AC2	VITA 47-Class CC4
Cooling Method	Convection	Convection	Conduction
Operating	0° to +55°C	-20° to +65°C	-40° to +85°C
Storage	-45° to +85°C	-45° to +85°C	-45° to +100°C
Vibration Sine (Operating)	20-500 Hz - 2g Acceleration / Frequency Range	20-500 Hz - 2g Acceleration / Frequency Range	22-2,000 Hz - 5g Acceleration / Frequency Range
Random	VITA 47-Class V1	VITA 47-Class V1	VITA 47-Class V3
Shock (Operating)	20g/11 ms Peak Accel./ Shock Duration Half Sine	20g/11 ms Peak Accel./ Shock Duration Half Sine	40g/20 ms Peak Accel./ Shock Duration Half Sine
Altitude (Operating)	-1,640 to 15,000 ft	-1,640 to 33,000 ft	-1,640 to 60,000 ft
Relative Humidity	90% non-condensing	95% non-condensing	95% non-condensing

6.4.2 MTBF

	GB			NS		ARW	AIC	
	25°C	40°C	55°C	25°C	40°C	55°C	40°C	55°C
MTBF (hours)	1 610 534h	1 163 805h	-	269 665h	198 571h	35 224h	177 921h	-

Table 53: Graphic Module MTBF Data

6.5 Power Supply

6.5.1 Power supplies

MOD-GX requires +5VDC and +3.3VDC power rail that are provided by VM6050 board and available from Front IO connector.

6.5.2 Electrical Consumption

Following tables indicate current and power consumption and test condition for MOD-GX (5V or 3.3V).

Voltage	5V	3.3V
Result	60 mA	500 mA

Interface	Current Draw
VGA	50 Ma 5V
DP B	200 mA 3.3V
DP D	200 mA 3.3V

Max Power consumption of MOD-GX is 1.6W.

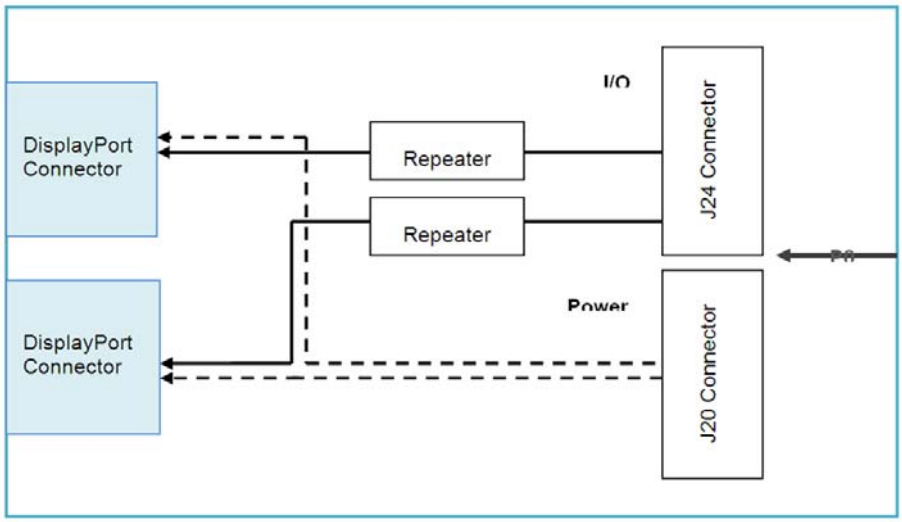
6.6 PIM MODULE Characteristic

6.6.1 Overview

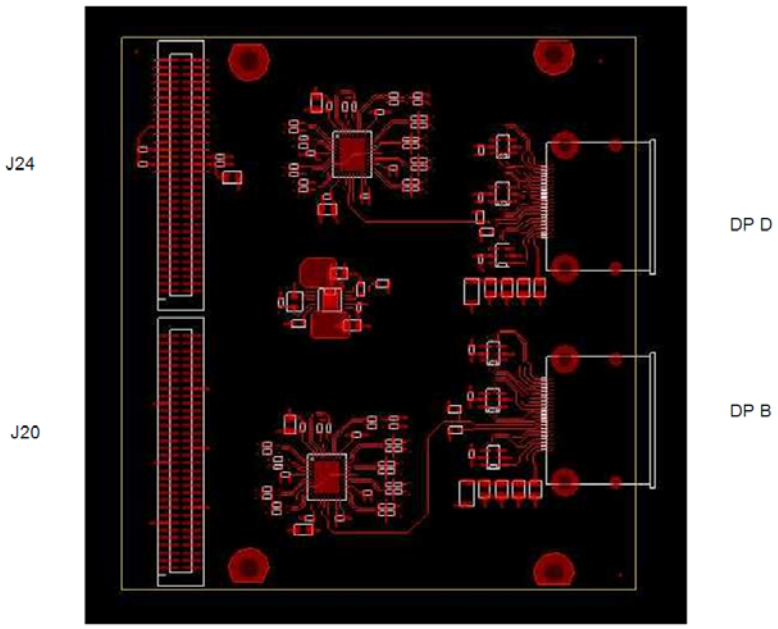
» Main feature

The PIM (Peripheral Interface Module) plugged on Rear Transition Module (RTM) provides 2 DisplayPort signals on the rear panel. Signals come from the graphic module through P0 connector.

» Bloc Diagram



6.6.2 Connector



PIM connector

J24 is a PMC IO connector with 64 pins. The pin assignment is the same that P14.

P0 corresponding assignment is specified.

PMC Pin	XMC Pin	Signal	P0	PMC Pin	XMC Pin	Signal	P0
33	F1	DPB1_HPD	B10	34	F3	DPD1_HPD	A10
35	C5	DPBPWR	E1	36	F5	DPDPWR	D1
37	C7	DPB1_CAD	C1	38	F7	DPDPWR	B1
39	C9	DPBPWR	A1	40	F9	DPD1_AUXn	E19
41	F11	DPD1_AUXp	D19	42	F13	DPD1_CAD	C19
43	C15	DPB1_AUXn	B19	44	F15	DPB1_AUXp	A19
45	C3	GND	C12	46	C1	GND	C11
47	D13	DPB1_LANE3p	D14	48	A11	DPB1_LANE0p	D11
49	E13	DPB1_LANE3n	E14	50	B11	DPB1_LANE0n	E11
51	A13	DPB1_LANE2p	D13	52	D11	DPB1_LANE1p	D12
53	B13	DPB1_LANE2n	E13	54	E11	DPB1_LANE1n	E12
55	C13	GND	C14	56	C11	GND	C13
57	D3	DPD1_LANE3p	A14	58	A1	DPD1_LANE0p	A11
59	E3	DPD1_LANE3n	B14	60	B1	DPD1_LANE0n	B11
61	A3	DPD1_LANE2p	A13	62	D1	DPD1_LANE1p	A12
63	B3	DPD1_LANE2n	B13	64	E1	DPD1_LANE1n	B12

PMC[1..32] pins are not connected.

J20 connector is reserved to power signals (+5V and +3.3V) from RTM.

PMC Pin	Signal	PMC Pin	Signal
1	NC	2	NC
3	NC	4	NC
5	+5V	6	NC
7	NC	8	NC
9	NC	10	+3.3V
11	NC	12	NC
13	GND	14	NC
15	NC	16	NC
17	NC	18	GND
19	NC	20	NC
21	+5V	22	NC
23	NC	24	NC
25	NC	26	+3.3V
27	NC	28	NC
29	GND	30	NC
31	NC	32	NC
33	NC	34	GND
35	NC	36	NC

PMC Pin	Signal	PMC Pin	Signal
37	+5V	38	NC
39	NC	40	NC
41	NC	42	+3.3V
43	NC	44	NC
45	GND	46	NC
47	NC	48	NC
49	NC	50	GND
51	NC	52	NC
53	+5V	54	NC
55	NC	56	NC
57	NC	58	+3.3V
59	NC	60	NC
61	NC	62	NC
63	NC	64	NC

(NC: Not connected)

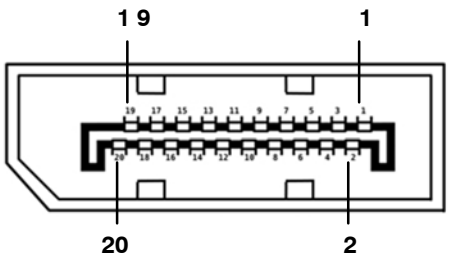
DisplayPort Connector

Two standard DisplayPort connector are available in rear panel of PIM-2DP module board.

Pin Assignment

PIN	SIGNAL	FUNCTION
1	ML_Lane 0 (p)	Lane 0 (positive)
2	GND	Ground
3	ML_Lane 0 (n)	Lane 0 (negative)
4	ML_Lane 1 (p)	Lane 1 (positive)
5	GND	Ground
6	ML_Lane 1 (n)	Lane 1 (negative)
7	ML_Lane 2 (p)	Lane 2 (positive)
8	GND	Ground
9	ML_Lane 2 (n)	Lane 2 (negative)
10	ML_Lane 3 (p)	Lane 3 (positive)
11	GND	Ground
12	ML_Lane 3 (n)	Lane 3 (negative)
13	GND	Ground
14	GND	Ground
15	AUX CH (p)	Auxiliary Channel (positive)
16	GND	Ground
17	AUX CH (n)	Auxiliary Channel (negative)
18	Hot Plug	Hot Plug Detect
19	Return	Return for power
20	DP_PWR	Power for connector

Table 54: DisplayPort Pin Assignment



Display Port

Figure 58: DisplayPort Connector

Chapter 7 - VM6050-RTM Characteristics

The VM6050-RTM (Order Code: PBV36-P0-VM6-00 rear transition module is compliant to PMC I/O Module Standard VITA 36 - 199x Draft 0.1 July 19, 1999 (mechanical and PIM format).

The main functionalities of the VM6050-RTM rear transition module are:

- Two 10/100/1000BASE-T Ethernet interface, **H1** and **H2** connectors on Figure 59
- One USB connector, **H4** on Figure 59
- One SMB connector, **H5** on Figure 59
- Two Serial lines ports available on two HE10 connectors (**H7**, **H8** on Figure 59)
- Three GPIOs signals available through an HE10 connector, **H9** connector on Figure 59
- Two Serial ATA connectors, **H10** and **H11** connector on Figure 59
- One PCI Express connector, **H12** connector on Figure 59
- PMC Site 1[64:1] I/O routed to **J14[32:1]** connector from RP2 connector
- PMC Site 2[64:1] I/O routed to **J24[32:1]** connector from RP2 connector (only on PBV36-P0-VM6-00 Rev. C)

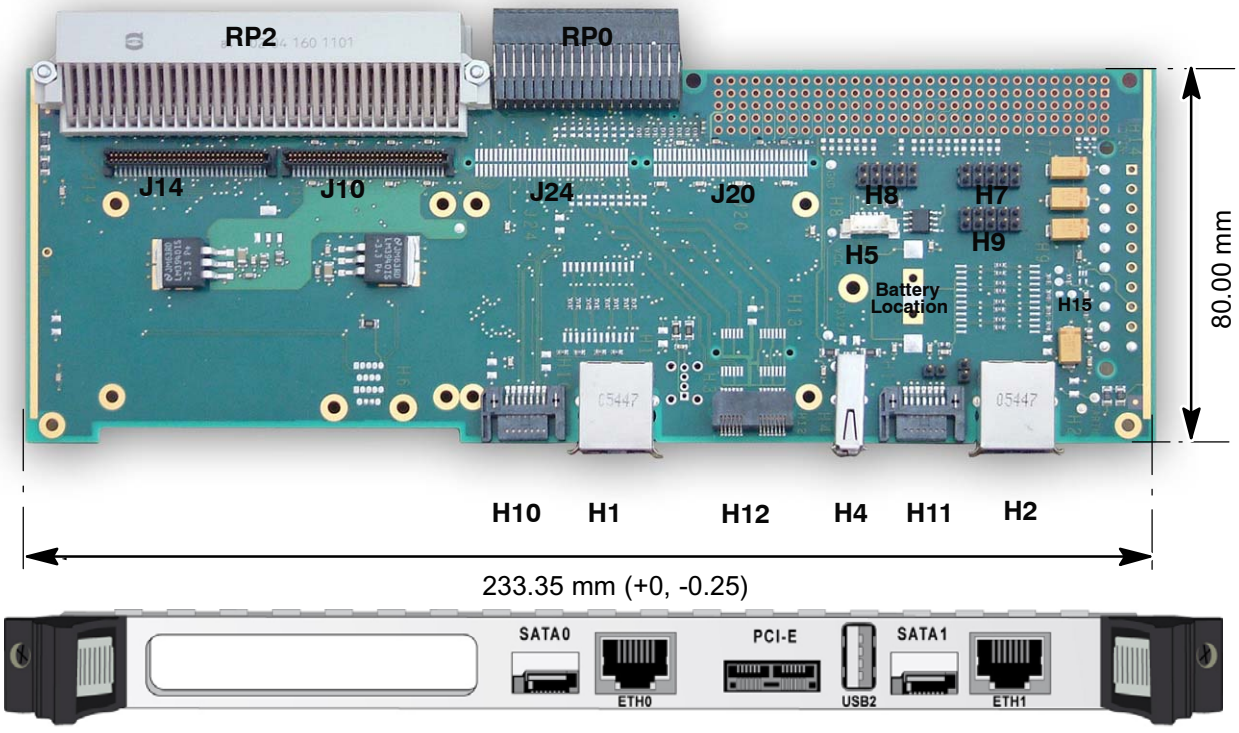


Figure 59: PBV36-P0-VM6-00 Module Overview

7.1 Installation of the Rear Transition Module

The VM6050-RTM module is designed to be used with a VME64 extensions backplane. Each slot in the backplane contains two 160-pin connectors and one connector with 95 user-defined pins. The top connector in each slot is designed J1, the middle connector is J0 and the bottom connector is J2.

The VM6050 rear transition module plugs into the J0, J1 and J2 connectors, on the back side of the VMEbus backplane, in the same slot as the VM6050 board (see Figure 60).

To install the rear transition module:

1. Make sure the system and peripheral equipment power are off.
2. Install the cables into the appropriate connectors on the transition module (see section 7.2 page 130).
3. Line-up the RP0 and RP2 connectors (also named P0 and P2 in this chapter) on the rear transition module with the J0 and J2 connectors on the backplane.
4. Press the outer edge of the transition module until the board is firmly seated in the connector.
5. Connect any additional cables.
6. Turn on system power.

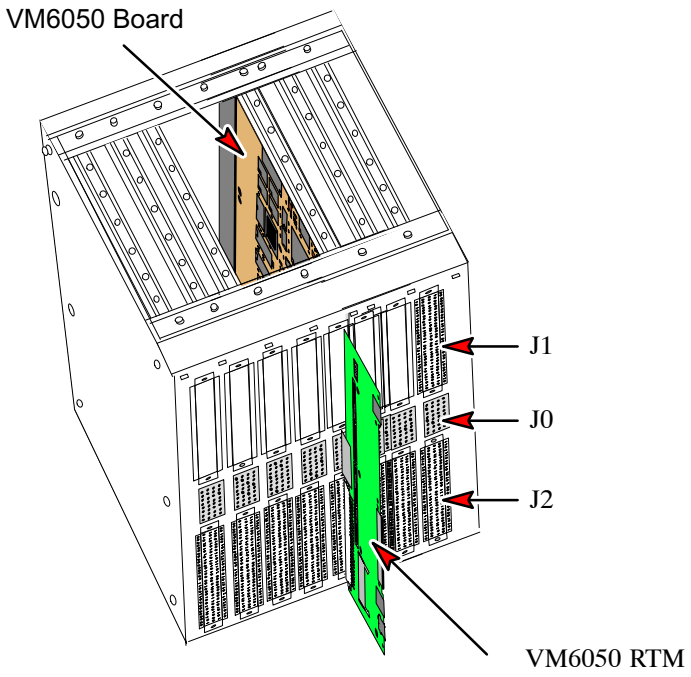


Figure 60: Installing the VM6050-RTM

7.2 Connectors

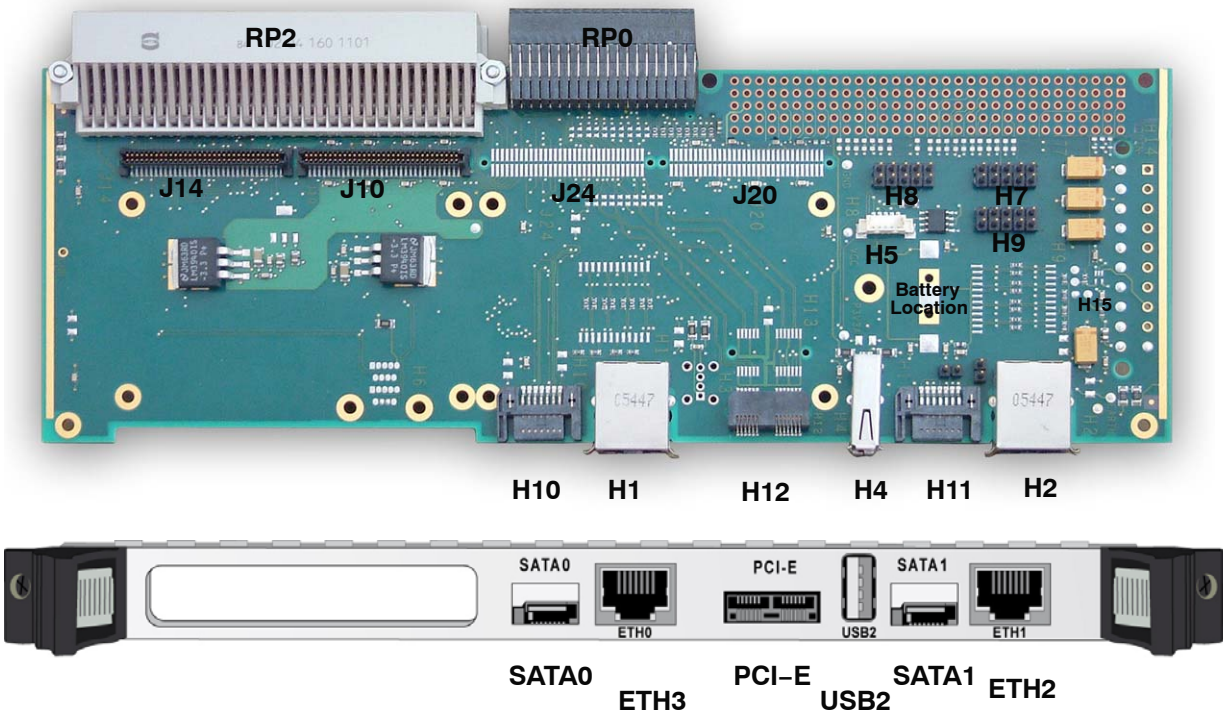


Figure 61: VM6050-RTM Connectors Location

7.2.1 RP0 Connector Pin Assignment

The RP0 connector has the same pin assignment as the P0 connector of the VM6050 board.

Refer to the “VME Bus Interface - P0 Connector" in section 4.3.1 page 68 for a complete information about the pin assignments of the RP0 connector.

7.2.2 RP2 Connector Pin Assignment

The RP2 connector has the same pin assignment as the P2 connector of the VM6050 board.

Refer to the “VME Bus Interface - P2 Connector" in section 4.3.3 page 74 for a complete information about the pin assignments of the RP2 connector.

7.2.3 H1 (ETHERNET 3) & H2 (ETHERNET 2) - Gigabit ETHERNET Connector

Routed from P0 to **H1** and **H2**, RJ-45 connectors (AMP - Part Number 106066-2).

Ethernet port 3 and 2 are respectively available through the **ETH0** and **ETH1** RTM front panel connectors.

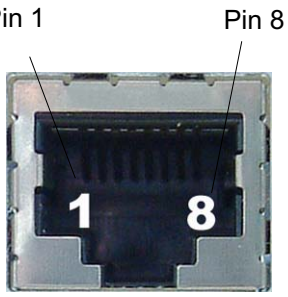
Connector Pin Assignment

Pin	Signal	Pin	Signal
1	BI_DA+	2	BI_DA-
3	BI_DB+	4	BI_DC+ (*)
5	BI_DC- (*)	6	BI_DB-
7	BI_DD+ (*)	8	BI_DD- (*)
9	Chassis Ground		

(*) : In 10BASE-T or 100BASE-T these signals are not used.

Type of Connector

H1 or H2



Signal Description

Mnemonic	Signal Description
BI_DA+/-	In 1000BASE-T: First pair of Transmit/receive data In 10BASE-T/100BASE-T: Pair of Transmit data
BI_DB+/-	In 1000BASE-T: Second pair of Transmit/receive data In 10BASE-T/100BASE-T: Pair of Receive data
BI_DC+/-	In 1000BASE-T: Third pair of Transmit/receive data In 10BASE-T/100BASE-T: Unused.
BI_DD+/-	In 1000BASE-T: Fourth pair of Transmit/receive data In 10BASE-T/100BASE-T: Unused.

7.2.4 H4 (USB1) - USB Connector

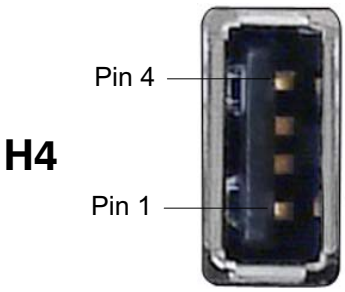
Routed from P0 to **H4**, a vertical USB connector.

Available through the **USB** RTM front panel connectors.

Connector Pin Assignment

Pin	Signal
1	+5 V Fused
2	USB1 DATA-
3	USB1 DATA+
4	GND
CASE	M GND

Type of Connector



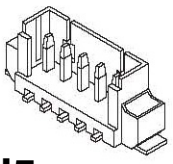
7.2.5 H5 - SMB Connector

Routed from P1 to **H5** (`MOLEX` - Part Number `53398-0590`)

Connector Pin Assignment

Pin	Signal
1	SMB_SCL
2	GND
3	SMB_SDA
4	N.C.
5	SMB_ALERT#

Type of Connector



Signal Description

Mnemonic	Signal Description
GND	Ground
N.C.	Not Connected
SMB_ALERT	System Management Bus - Alert
SMB_SCL	System Management Bus - Serial clock line from the SMBus master to SMBus slave devices.
SMB_SDA	System Management Bus - Bi-directional serial data line between the SMBus master and the SMBus slave device.

7.2.6 H7 (S0/COM1) & H8 (S1/COM2) - SERIAL Connector

Routed from P2 to **H7** and **H8**; individual 10-pin HE10 connectors

A serial line should only be used via one connector at the same time, either the Serial front panel connector or the P2 connector.

H7 Connector Pin Assignment

Pin	Signal	Pin	Signal
1	N.C.	2	S0_RX
3	S0_TX	4	N.C.
5	GND	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	N.C.

H8 Connector Pin Assignment

Pin	Signal	Pin	Signal
1	GPIO4	2	S1_RX
3	S1_TX	4	GPIO6
5	GND	6	GPIO5
7	N.C.	8	N.C.
9	N.C.	10	N.C.

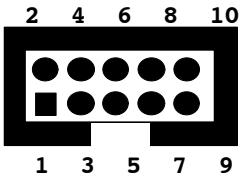
Signal Description

Mnemonic	Signal Description
GND	Ground
N.C.	Not Connected
S*x*_RX	Channel EIA-232 *x* Receive Data
S*x*_TX	Channel EIA-232 *x* Transmit Data
GPIO*x*	GPIO *x* from CPLD

Type of Connector

Right angle HE10 10-pin connector, male, with board lock.

H7 & H8



The H7 and H8 connectors can be connected via a NULL MODEM adapter on a VT100 console.

7.2.7 H9 - GPIOs and MISC Signals

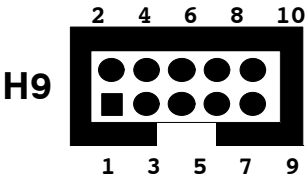
Routed from P0 to **H9**; individual 10 pins HE10 connector.

Connector Pin Assignment

Pin	Signal	Pin	Signal
1	GPIO1	2	N.C.
3	GPIO2	4	N.C.
5	GPIO3	6	N.C.
7	N.C.	8	GND
9	N.C.	10	GND

Type of Connector

Right angle HE10 10-pin connector, male, with board lock.



Signal Meaning

Mnemonic	Signal Description
GPIO*x*	GPIO *x* from cPLD
GND	Ground
N.C.	Not Connected

7.2.8 H10 (SATA0) and H11 (SATA1) - Serial ATA Connector

Routed from P0 to **H10** and **H11**; SATA connector, right angle version with metal latch (`MOLEX` - Part Number `47080-4001`)

Available through the **SATA0** and **SATA1** RTM front panel connectors.

Depending on the SATA manufacturing option of the associated VM6050 board:
- Two SATA devices are available through the SATA0 and SATA1 RTM front panel connectors: SATA on P0 manufacturing option.
- Only one SATA device is available through the SATA0 RTM front panel connectors: SATA onboard manufacturing option.

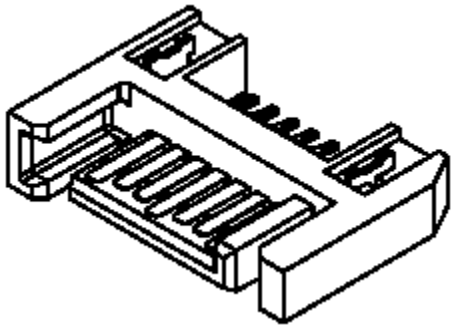
Connector Pin Assignment

Pin	Signal	Pin	Signal
1	GND	2	SATA*x* TX+
3	SATA*x* TX-	4	GND
5	SATA*x* RX-	6	SATA*x* RX+
7	GND		

Signal Description

Mnemonic	Signal Description
GND	Ground
SATA*x* RX+/RX-	Serial ATA *x* Receive +/-
SATA*x* TX+/TX-	Serial ATA *x* Transmit +/-

Type of Connector



7.2.9 H12 - PCI Express Connector

Routed from P0 connector to **H12**, a 26-pin right angle connector (SAMTEC - Order Code MEC8−RA)

Available through the **PCI−E** RTM front panel connectors.

Connector Pin Assignment

Pin	Signal	Pin	Signal
1	GND	2	GND
3	PEX RXL0+	4	PEX TXL0+
5	PEX RXL0-	6	PEX TXL0-
7	GND	8	GND
9	PEX RX1L+	10	PEX TXL1+
11	PEX RXL1-	12	PEX TXL1-
13	GND	14	GND
15	PEX RXL2+	16	PEX TXL2+
17	PEX RXL2-	18	PEX TXL2-
19	GND	20	GND
21	PEX RXL3+	22	PEX TXL3+
23	PEX RXL3-	24	PEX TXL3-
25	GND	26	GND

Type of Connector

Signal Meaning

Mnemonic	Signal Description
PEX RXL[0..3]+/-	x4 PCI Express Link - Differential Receive Lane [0..3]
PEX TXL[0..3]+/-	x4 PCI Express Link - Differential Transmit Lane [0..3]
GND	Ground

Known Limitations

The P0 to P0 connection using CABL-ZPACK-X4-022 cable is recommended when connecting VM6050 and V2PMC2. See “V2PMC2 User's Guide” - section 6.4.1.

7.2.10 PCI 64 PIM Site 1 Connector

J14 Connector Pin Assignment

Pin	Signal	Pin	Signal
1	PMC64 IO 01	2	PMC64 IO 02
...	...	...	...
63	PMC64 IO 63	64	PMC64 IO 64

Signal Description

Mnemonic	Signal Description
PMC64 IO *xx*	I/O 01 through 64 of the motherboard PMC: J14[01 ... 64] for PMC Site 1
N.C.	Not Connected

Known Limitations

- 4.8 mm high components have been placed under PIM site 1. This trangresses the VITA 36 standard which specifies 2.5 mm. Some PIMs may not fit in this site.

J10 Connector Pin Assignment

Pin	Signal	Pin	Signal
1	N.C.	2	N.C.
3	N.C.	4	N.C
5	+5V	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	+3.3V
11	N.C.	12	N.C.
13	GND	14	N.C.
15	N.C.	16	N.C.
17	N.C.	18	GND
19	N.C.	20	N.C.
21	+5V	22	N.C.
23	N.C.	24	N.C.
25	N.C.	26	+3.3V
27	N.C.	28	N.C.
29	GND	30	N.C.
31	N.C.	32	N.C.
33	N.C.	34	GND
35	N.C.	36	N.C
37	+5V	38	N.C.
39	N.C.	40	N.C.
41	N.C.	42	+3.3V
43	N.C.	44	N.C.
45	GND	46	N.C.
47	N.C.	48	N.C.
49	N.C.	50	GND
51	N.C.	52	N.C.
53	+5V	54	N.C.
55	N.C.	56	N.C.
57	N.C.	58	+3.3V
59	N.C.	60	N.C.
61	N.C.	62	N.C.
63	N.C.	64	N.C.

7.2.11 PCI 64 PIM Site 2 Connector

Up to PBV36-P0-VM6-00 Rev. C, the pinout of J20 and J24 connectors is reserved. If available, do not try to use these connectors.

From PBV36-P0-VM6-00 Rev. C, the pinout of the J20 and J24 connectors is available. See sections J24 and J20 Connector Pin Assignment below.

Installation of a PIM on the Site 2 of a PBV36-P0-VM6-00 Rev C. requires specific adjustments:
- removing H10 (SATA0), H1 (ETH0) and H12 (PCI-E) connector on the RTM,
- usage of a RTM specific front panel.

Contact your Kontron representative for more information on this topic.

J24 Connector Pin Assignment

Pin	Signal	Pin	Signal
1	PMC64 IO 01	2	PMC64 IO 02
...	...	...	...
63	PMC64 IO 63	64	PMC64 IO 64

Signal Description

Mnemonic	Signal Description
PMC64 IO *xx*	I/O 01 through 64 of the motherboard PMC: J24[01 ... 64] for PMC Site 2
N.C.	Not Connected

Known Limitations

- The RTM does not include the 3 mm recess at the rear card edge on the area of PIM Site as required by VITA 36 standard. This may require removal or loosening of the rear panel in order to remove and install a PIM at Site 2.

J20 Connector Pin Assignment

Pin	Signal	Pin	Signal
1	N.C.	2	N.C.
3	N.C.	4	N.C
5	+5V	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	+3.3V
11	N.C.	12	N.C.
13	GND	14	N.C.
15	N.C.	16	N.C.
17	N.C.	18	GND
19	N.C.	20	N.C.
21	+5V	22	N.C.
23	N.C.	24	N.C.
25	N.C.	26	+3.3V
27	N.C.	28	N.C.
29	GND	30	N.C.
31	N.C.	32	N.C.
33	N.C.	34	GND
35	N.C.	36	N.C
37	+5V	38	N.C.
39	N.C.	40	N.C.
41	N.C.	42	+3.3V
43	N.C.	44	N.C.
45	GND	46	N.C.
47	N.C.	48	N.C.
49	N.C.	50	GND
51	N.C.	52	N.C.
53	+5V	54	N.C.
55	N.C.	56	N.C.
57	N.C.	58	+3.3V
59	N.C.	60	N.C.
61	N.C.	62	N.C.
63	N.C.	64	N.C.

7.2.12 Reset

The front panel reset toggle switch can be set to the RESET position to generate an hard reset.

7.2.13 Mechanical Ground

One HE10 2-pin connector is placed on the board to allow to hard connect electrical (GND) and mechanical (EARTH) grounds.

While adding a jumper on connector, both ground signals are tighten together.

» H15 Connector Pin Assignment

Pin	Signal	Pin	Signal
1	EARTH	2	GND

» Signal Meaning

Mnemonic	Signal Description
EARTH	Electrical Ground
GND	Mechanical Ground

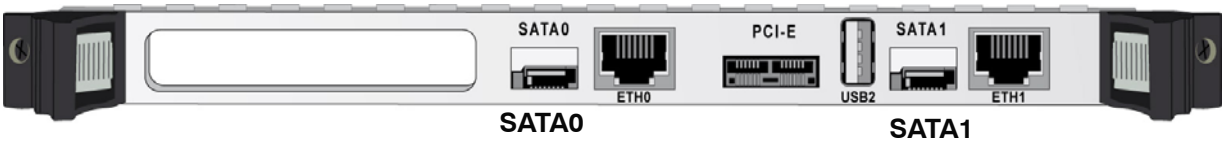
A metalized mechanical hole (3mm diameter) is located on the board to allow to fix an electrical pod in order to bring the mechanical ground from the chassis.

7.2.14 Power Supplies

- Two 800 mAmp voltage regulators are used on the board to provide 3.3V power supply to each PIM site.
- A standard lithium battery to supply CPU board's RTC is also available.

7.3 Cables

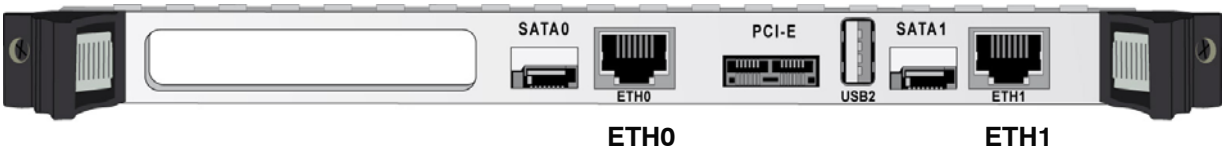
7.3.1 SATA Cable



Serial ATA standard cable

Figure 62: Serial ATA Cable

7.3.2 Ethernet Cable



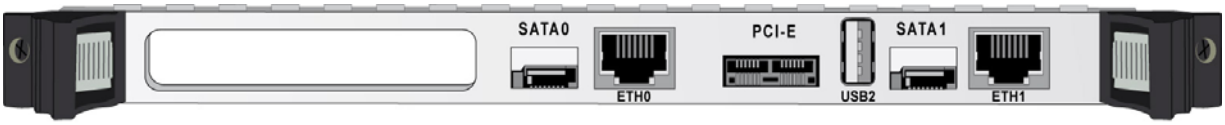
Gigabit Ethernet standard cable:
1000BASE-T requires category 5e, 5+ or 6 copper cable, with a maximal length of 100m for an UTP or FTP cable, and 150m for a STP or FSTP cable.

Figure 63: Gigabit Ethernet Cable

7.3.3 PCI-Express Cable

Please contact your Kontron representative for more information on this topic.

7.3.4 USB 2.0 Cable



USB 2.0

USB 2.0 standard cable

USB series “A" plug and receptacle

Figure 64: USB 2.0 Cable

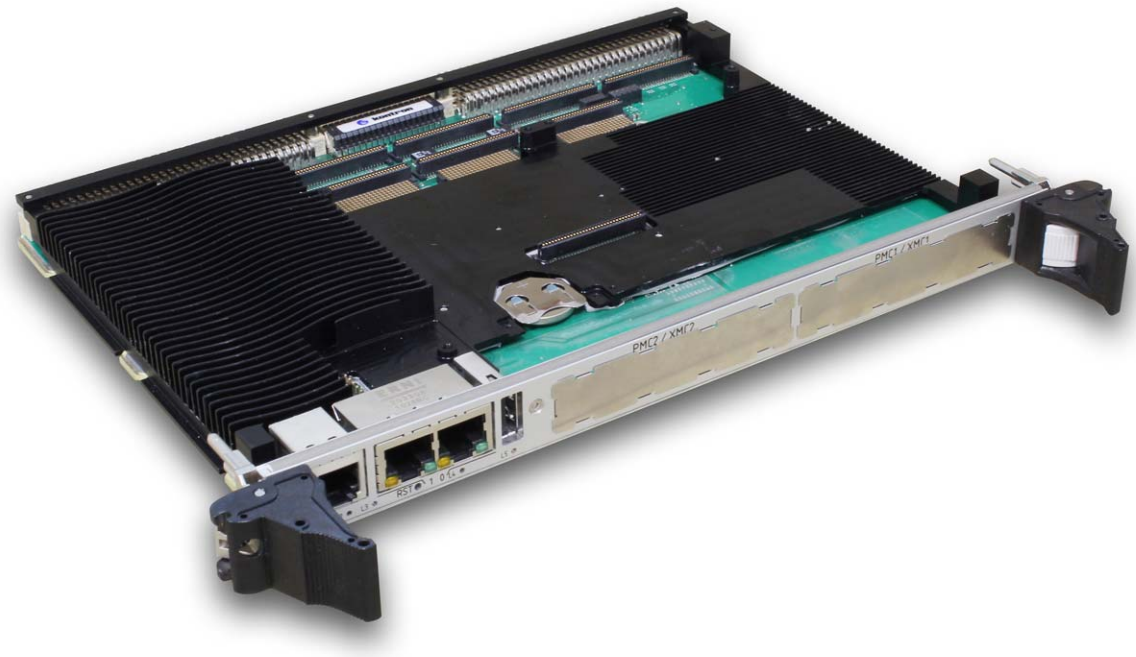
Chapter 8 - VM6050/RA - Characteristics

The VM6050/RA boards uses “The Ruggedizer", a Kontron proven technology to meet the requirements for harsh environments. With an operational temperature range from -40º C up to +70º C (VITA 47 AC3) and its mechanical environmental performances, the VM6050/RA are designed for severe environmental applications with high levels of shock and vibration, small space envelope and restricted cooling such as required in military, marine, avionics, sheltered and industrial applications.

Order Code

Order Code		Description
VM6050/RA	VM6050-2RA34-x0110	Core i7 620LE @ 2 GHz, RA Class, 4 GB SDRAM, 2 PMC/XMC
VM6050/RA	VM6050-2RA34-x0210	Core i7 620LE @ 2 GHz, RA Class, 4 GB SDRAM, 2 PMC/XMC, 5V only (12V needed if required by PMC/XMC

X: 0 = no Flash
1 = 8 GB USB Flash
2 = 8 GB SATA Flash



non−contractual photography

Figure 65: VM6050/RA - Overview

8.1 VM6050/RA Specificities

The VM6050/RA boards have the same features as the VM6050/SA boards, except for the following items which are fully described in associated sections below:

FUNCTION	SEE ALSO
Battery Installation	Section 8.4 page 146
Board Identification	Section 8.5 page 147
Environmental Specifications	Section 8.6 page 148
Mechanical Specifications	Section 8.7 page 149
MTBF	Section 8.8 page 150
Peripheral Connectivity	Section 8.9 page 151
PMC/XMC Installation	Section 9.9 page 163
USB Device Installation	Section 8.10 page 152

Table 55: VM6050/RA Specificities

8.2 Frequency Operation

» Standard Frequency Operation

The VM6050 processor frequency is set to 1.6 GHz. With this default setting, the VM6050 processing performance is guaranteed across the whole operating temperature range. The VM6050 thermal design is such as the processor, running at this frequency does not enter thermal management mode (frequency throttling) when the processor temperature is maintained within the approved operating range.

8.3 CPU Thermal Monitoring

» CPU Temperature

For a given minimum required air-flow, the curves (section 5.2.4.1 page 107) show the maximum **authorized** operating temperature, not to exceed the maximum specified junction temperature of the processor.

T_{JMAX} CPU cores: 105°C

T_{JMAX} GFX cores: 100°C

The T_{JMAX} temperature is the temperature not to exceed, to avoid entering the throttling mode.

	VM6050/RA
1.6 GHz	2.8 m/s (16 CFM)
1.4 GHz	1.7 m/s (10 CFM)
1.3 GHz	1.2 m/s (7 CFM)

These values are determinated using thermal analysis tool from Intel set to 80% of CPU charge. This setting is representative of most of customer's applications.

8.4 Battery Installation

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer (Rayovac BR2032_BN).

Compared with the VM6050/SA boards, an additional cover is added on the battery in order to satisfy the shock and vibration constraints.

To replace the battery, proceed as follows:

- Turn off power and remove the board from the rack.
- Unscrew the two flat head screws (FX-M2x3) that maintain the cover in position, and remove the cover.
- Use a thin plastic tool to push the battery outside the safety cache. Push from the right or left top side of the safety cache.
- Remove the battery.
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!
- Make sure the insulator under the cover is in good condition, otherwise contact your Kontron representative.
- Put back the cover and screw back the two flat head screws (FX-M2x3) applying a torque of 0.138 Nm (1.221 Lb-In).
- Secure the two screws with a drop of Loctite 222.

Note Care must be taken to ensure that the battery is correctly replaced.
The battery should be replaced only with an identical or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

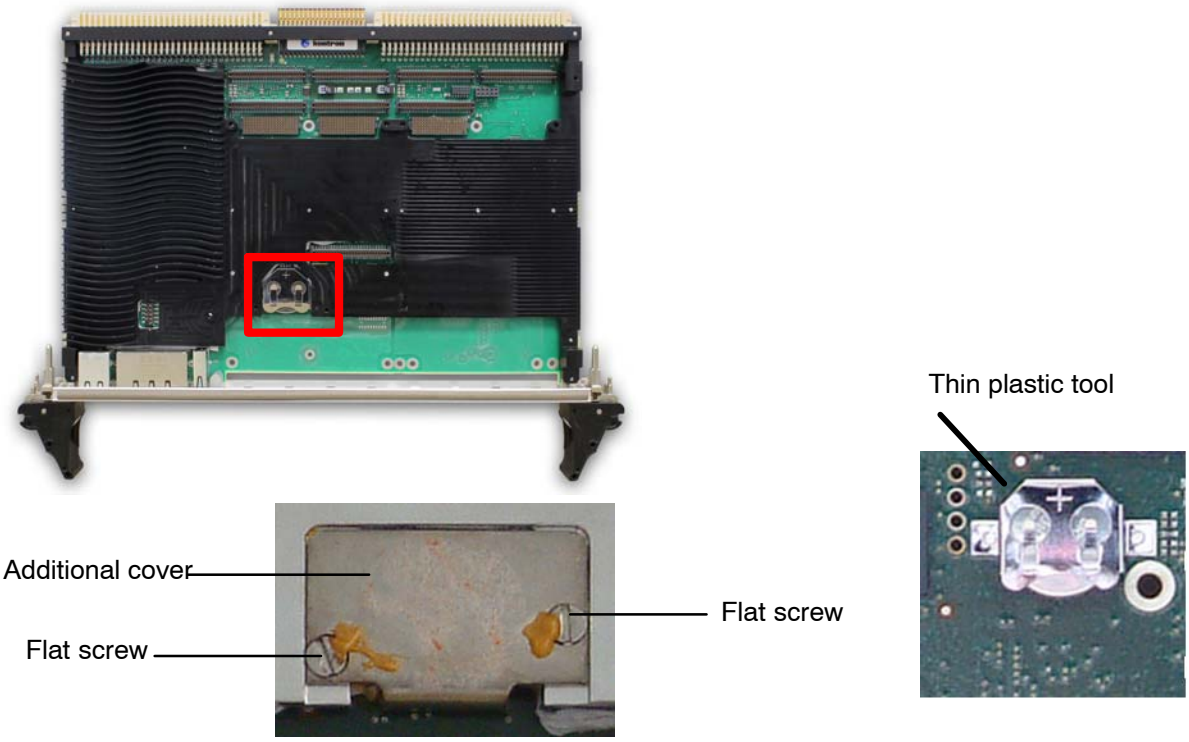


Figure 66: Battery Installation on VM6050/RA

8.5 Board Identification

The VM6050/RA boards are identified by labels fitted to the bottom side. These labels are at the same location and have the same meaning (except the “Board Identification" label) as the VM6050/SA boards labels (refer to the section 2.2 page 21 for more information).

> The “Board Identification" label prefix of a VM6050/RA board is VM6050_xRA.

In addition, on VM6050/RA boards, the ruggedizer is identified by:

> the “Ruggedizer Identification” (printed on the ruggedizer).

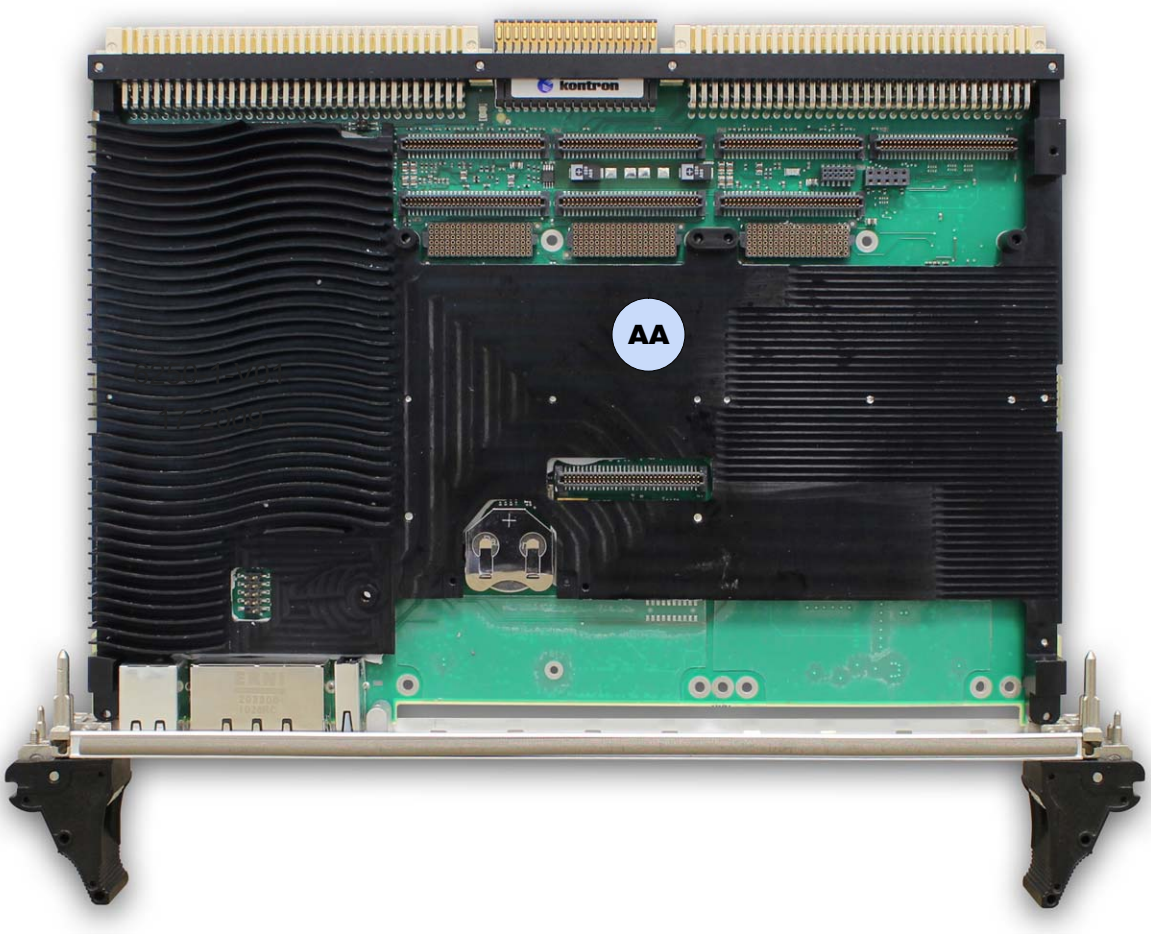


Figure 67: VM6050/RA Identification

8.6 Environmental Specifications

VM6050/RA ENVIRONMENTAL SPECIFICATIONS	
	RA - Rugged Air-Cooled
Conformal Coating	Standard
Airflow	N.A.
Temperature	VITA 47-Class AC3
Cooling Method	Convection
Operating	-40°C to +70°C
Storage	-50°C to +100°C, except battery that must be stored in -40°C / +85°C
Vibration Sine (Operating)	3g / 20-2,000 Hz acceleration / frequency range
Random	VITA 47-Class V2
Shock (Operating)	20g / 11 ms peak accel. / shock duration half sine
Altitude (Operating)	-1,500 to 60,000 ft
Relative Humidity	95% non-condensing

Table 56: VM6050/RA Environmental Specifications

8.7 Mechanical Specifications

The VM6050/RA boards are build on a multi-layer double Eurocard and conforms to the dimensions specified in the ANSI/VITA VME64 1-1994. The dimensions shown below are in millimeters, with inches (in parentheses) for general guidance only.

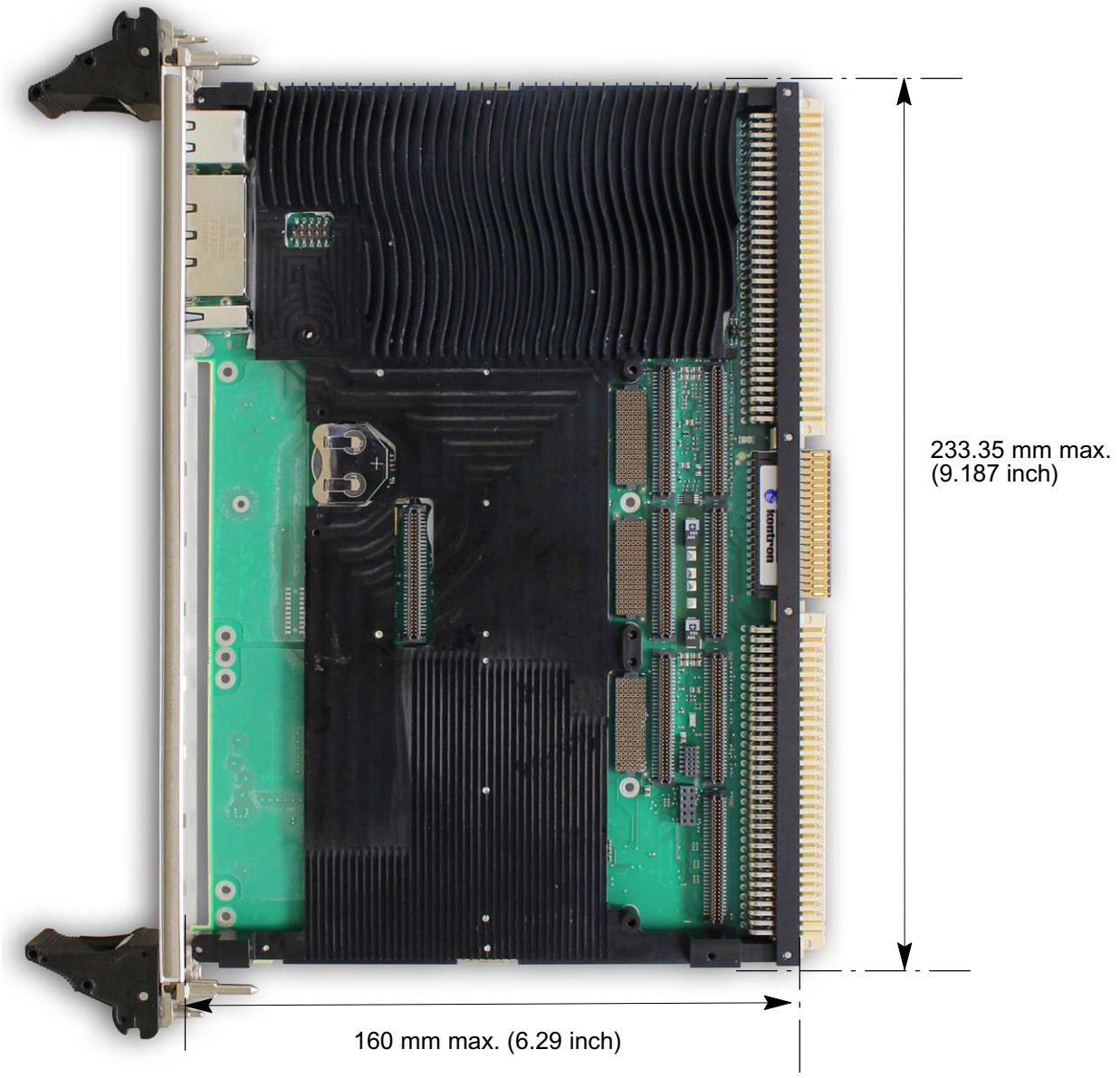


Figure 68: VME Dimensions

- **Length:** 233.35 mm max.
- **Depth:** 160 mm max.
- **Height:** 1 VME slot compatible
- **Weight:** ~645 g (approximatively)

8.8 MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

	GB (Hours)			AIC (Hours)		NS (Hours)		ARW (Hours)
	25°C	40°C	55°C	40°C	55°C	25°C	40°C	55°C
MTBF (hours)	292 100 h	295 000 h	-	57 500 h	-	72 400 h	62 600 h	17 100 h

Table 57: VM6050/RA MTBF Data

8.9 Peripheral Connectivity

The VM6050/RA board features the same connectors as the VM6050/SA except that:

> the P4, P5, P6 and P9 onboard connectors are not fitted on the VM6050/RA board.

For detailed information about the connectors located on the VM6050, refer to section 4.2 page 63 “Onboard Connectors”.

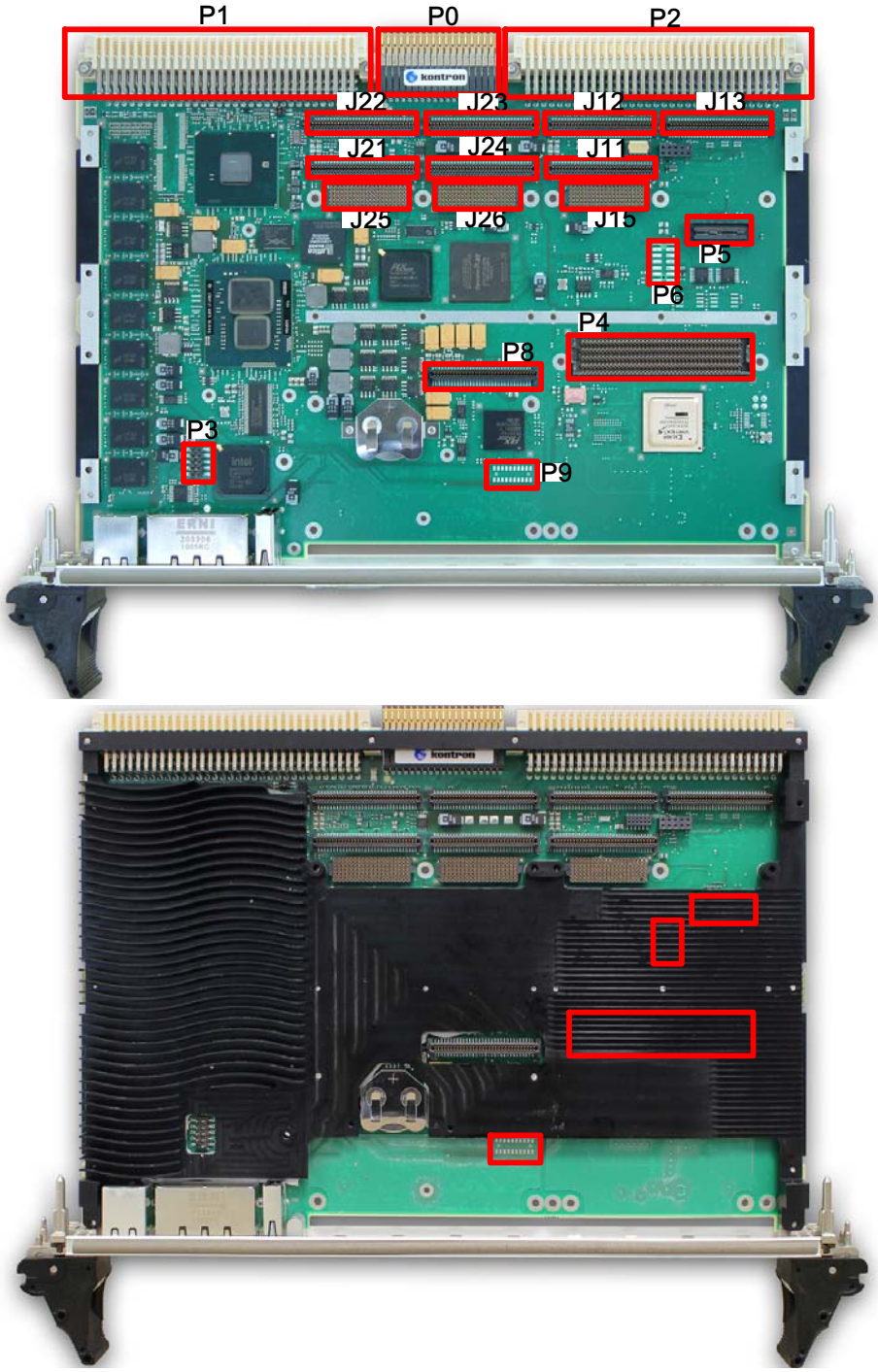
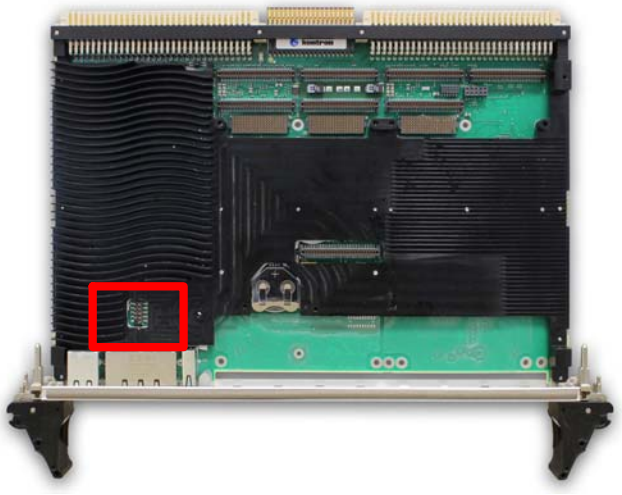


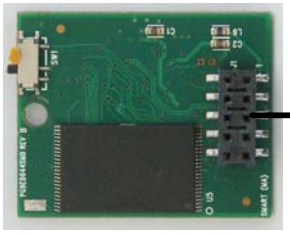
Figure 69: VM6050/RA Peripheral Connectivity

8.10 USB/SATA Device Installation

The fastenings kit is delivered with the board, it includes:

- 1x screws CZX-M2.5X5 P3 side

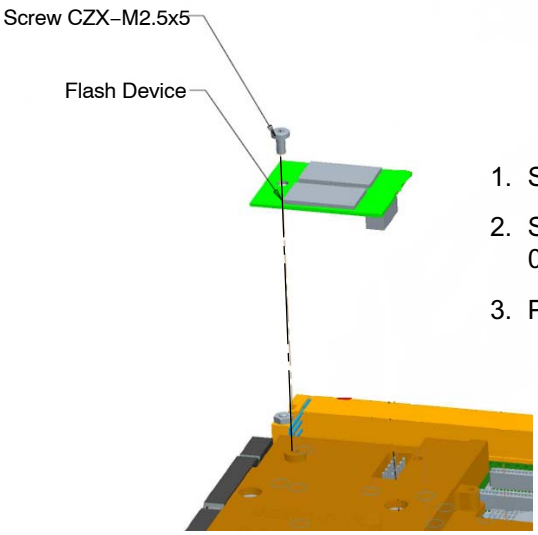




Flash Device

P3

Figure 70: USB Device Location on VM6050/RA



1. Set up the flash device using the P3 connector.
2. Screw the screw CZX-M2.5x5 using a torque of 0.279 N.m. (2.469 Lb-In).
3. Put a drop of Loctite 222 on the screw head.

Figure 71: USB Device Installation on VM6050/RA

Chapter 9 - VM6050/RC - Characteristics

The VM6050/RC boards uses “The Ruggedizer", a Kontron proven technology to meet the requirements for harsh environments. With an operational temperature range from -40º C up to +85º C (VITA 47 CC4) and its mechanical environmental performances, the VM6050/RC are designed for severe environmental applications with high levels of shock and vibration, small space envelope and restricted cooling such as required in military, marine, avionics, sheltered and industrial applications.

Order Code

Order Code		Description
VM6050-RC	VM6050-2RC34-X0110	Rugged Conduction-cooled 6U VME SBC, 2.0 GHz Intel® Core™ i7, 4 GB SDRAM, 2 PMC/XMC
VM6050-RC	VM6050-2RC34-X0210	Rugged Conduction-cooled 6U VME SBC, 2 GHz Intel® Core™ i7, 4 GB SDRAM, 2 PMC/XMC, 5V only (12V needed if required by PMC/XMC

X: 0 = no Flash
1 = 8 GB USB Flash

non−contractual photography

Figure 72: VM6050/RC - Overview

9.1 VM6050/RC Specificities

The VM6050/RC boards have the same features as the VM6050/SA boards, except for the following items which are fully described in associated sections below:

FUNCTION	SEE ALSO
Battery Installation	Section 9.3 page 157
Board Identification	Section 9.4 page 158
Environmental Specifications	Section 9.5 page 159
Mechanical Specifications	Section 9.6 page 160
MTBF	Section 9.7 page 161
Peripheral Connectivity	Section 9.8 page 162
PMC/XMC Installation	Section 9.9 page 163
USB Device Installation	Section 9.10 page 165

Table 58: VM6050/RC Specificities

9.2 Frequency Operation

Standard Frequency Operation

The VM6050 processor frequency is set to 1.2 GHz. With this default setting, the VM6050 processing performance is guaranteed across the whole operating temperature range. The VM6050 thermal design is such as the processor, running at 1.2 GHz does not enter thermal management mode (frequency throttling) when the wedgelock temperature is maintained within the approved operating range.

The standard operating range for a **VM6050/RC is -40° to +85°C.** The card edge temperature check point is measured as follows: the middle point in the wedgelock channel on the ruggedizer. The wedgelock channel is the channel between the edge of the ruggedizer and the cold wall of the rack. Refer to arrows numbers **1** and **2** in following pictures.

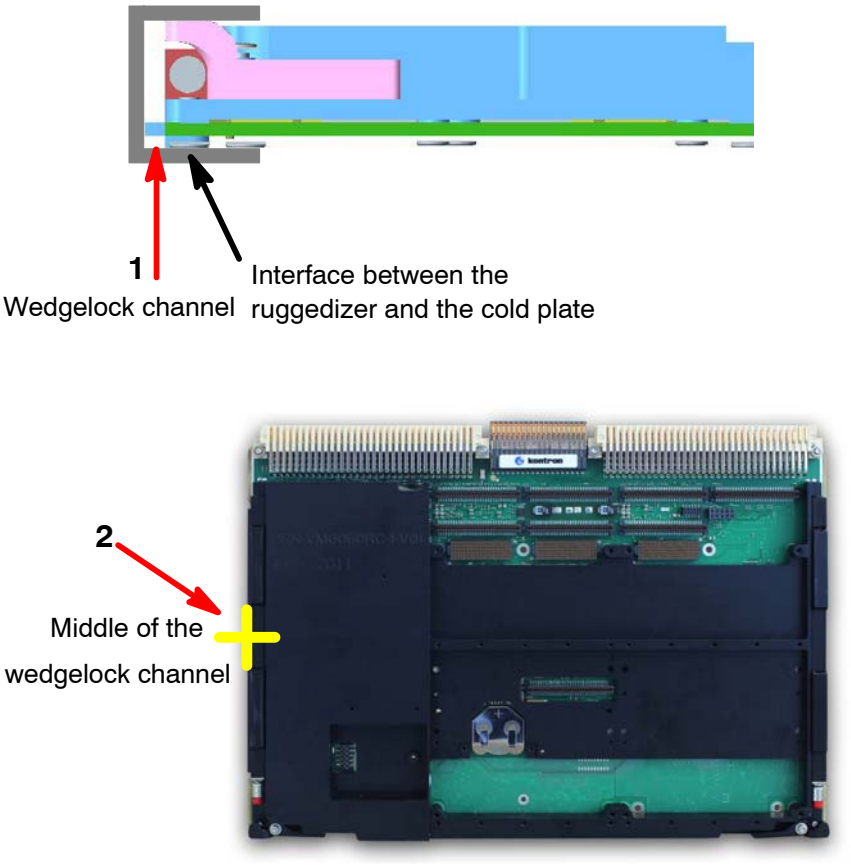


Figure 73: Measuring the Temperature

According to ANSI/VITA 47 standard, the plug-in unit edge surface temperature is measured on the plug-in unit.

Higher Frequency Operation

The processor upper frequency limit can also be set to **2.0 GHz** so as to get increased computing performance. In this case, the highest operating temperature on the wedgelock should limited to **70° C**.

This will also keep the dual-core processor outside of its thermal management mode.

To modify the processing frequency, please refer to the section 5.5 “CPU Configuration" of VM6050 AMI-BIOS User Manual (SD.DT.F89).

> **Exceeding the limits will lock the board**

Operating the processor at 2.0 GHz and allowing the wedgelock temperature to reach 85°C is tempting, but the board behaviour cannot be guaranteed. Even if the CPU chip may adapt quickly to the situation with frequency reduction, this shall not be recommanded.

9.3 Battery Installation

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer (Rayovac BR2032_BN).

Compared with the VM6050/SA boards, an additional cover is added on the battery in order to satisfy the shock and vibration constraints.

To replace the battery, proceed as follows:

- Turn off power and remove the board from the rack.
- Unscrew the two flat head screws (FX-M2x3) that maintain the cover in position, and remove the cover.
- Use a thin plastic tool to push the battery outside the safety cache. Push from the right or left top side of the safety cache.
- Remove the battery.
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!
- Make sure the insulator under the cover is in good condition, otherwise contact your Kontron representative.
- Put back the cover and screw back the two flat head screws (FX-M2x3) applying a torque of 0.138 Nm (1.221 Lb-In).
- Secure the two screws with a drop of Loctite 222.

Note Care must be taken to ensure that the battery is correctly replaced.
The battery should be replaced only with an identical or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

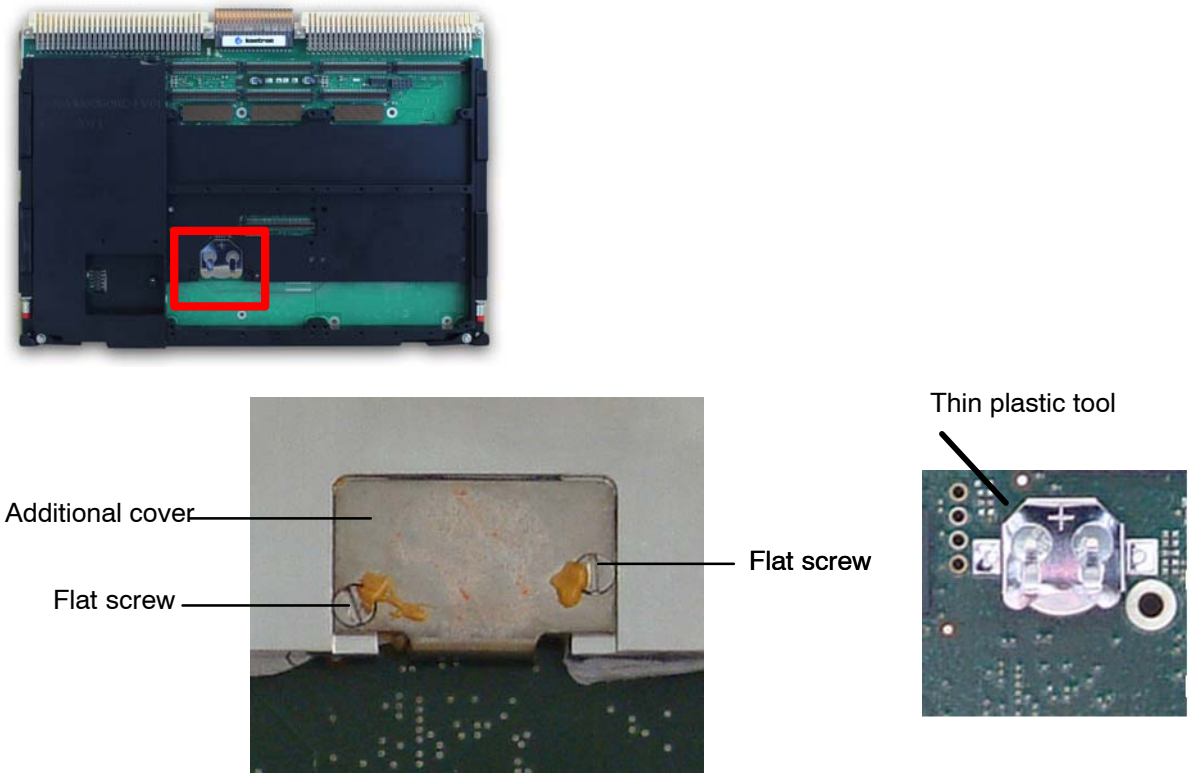


Figure 74: Battery Installation on VM6050/RC

9.4 Board Identification

The VM6050/RC boards are identified by labels fitted to the bottom side. These labels are at the same location and have the same meaning (except the “Board Identification" label) as the VM6050/SA boards labels (refer to the section 2.2 page 21 for more information).

> The “Board Identification" label prefix of a VM6050/RC board is **VM6050_xRC.**

In addition, on VM6050/RC boards, the ruggedizer is identified by:

> the “Ruggedizer Identification” (printed on the ruggedizer).

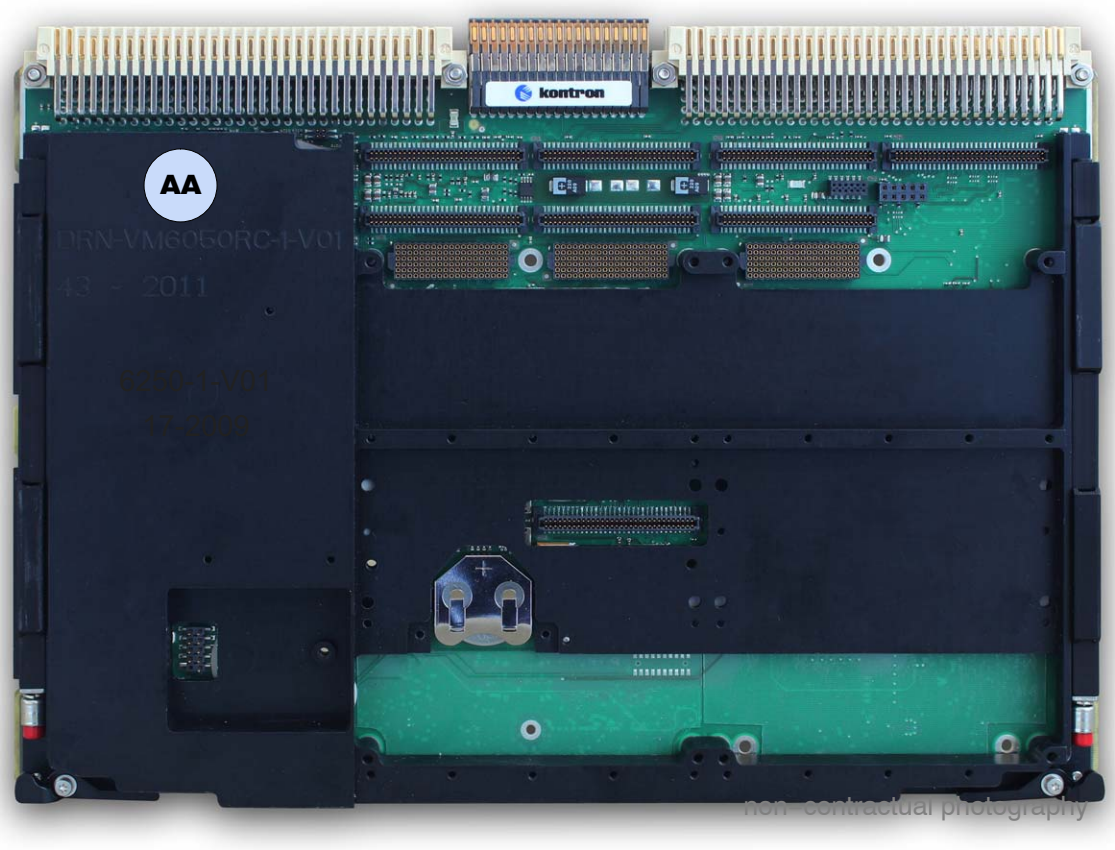


Figure 75: VM6050/RC Identification

9.5 Environmental Specifications

VM6050/RC ENVIRONMENTAL SPECIFICATIONS	
	RC - Rugged Conduction-Cooled
Conformal Coating	Standard
Airflow	N.A.
Temperature	VITA 47-Class CC4
Cooling Method	Conduction
Operating	-40°C to +85°C at 1.2 Ghz CC4 -40°C to +70°C at 2.0 Ghz CC3
Storage	-50°C to +100°C, except battery that must be stored in -40°C / +85°C
Vibration Sine (Operating)	5g / 22-2,000 Hz acceleration / frequency range
Random	VITA 47-Class V3
Shock (Operating)	40g / 20 ms peak accel. / shock duration half sine
Altitude (Operating)	-1,500 to 60,000 ft
Relative Humidity	95% non-condensing

Table 59: VM6050/RC Environmental Specifications

9.6 Mechanical Specifications

The VM6050/RC boards are build on a multi-layer double Eurocard and conforms to the dimensions specified in the ANSI/VITA VME64 1-1994. The dimensions shown below are in millimeters, with inches (in parentheses) for general guidance only.

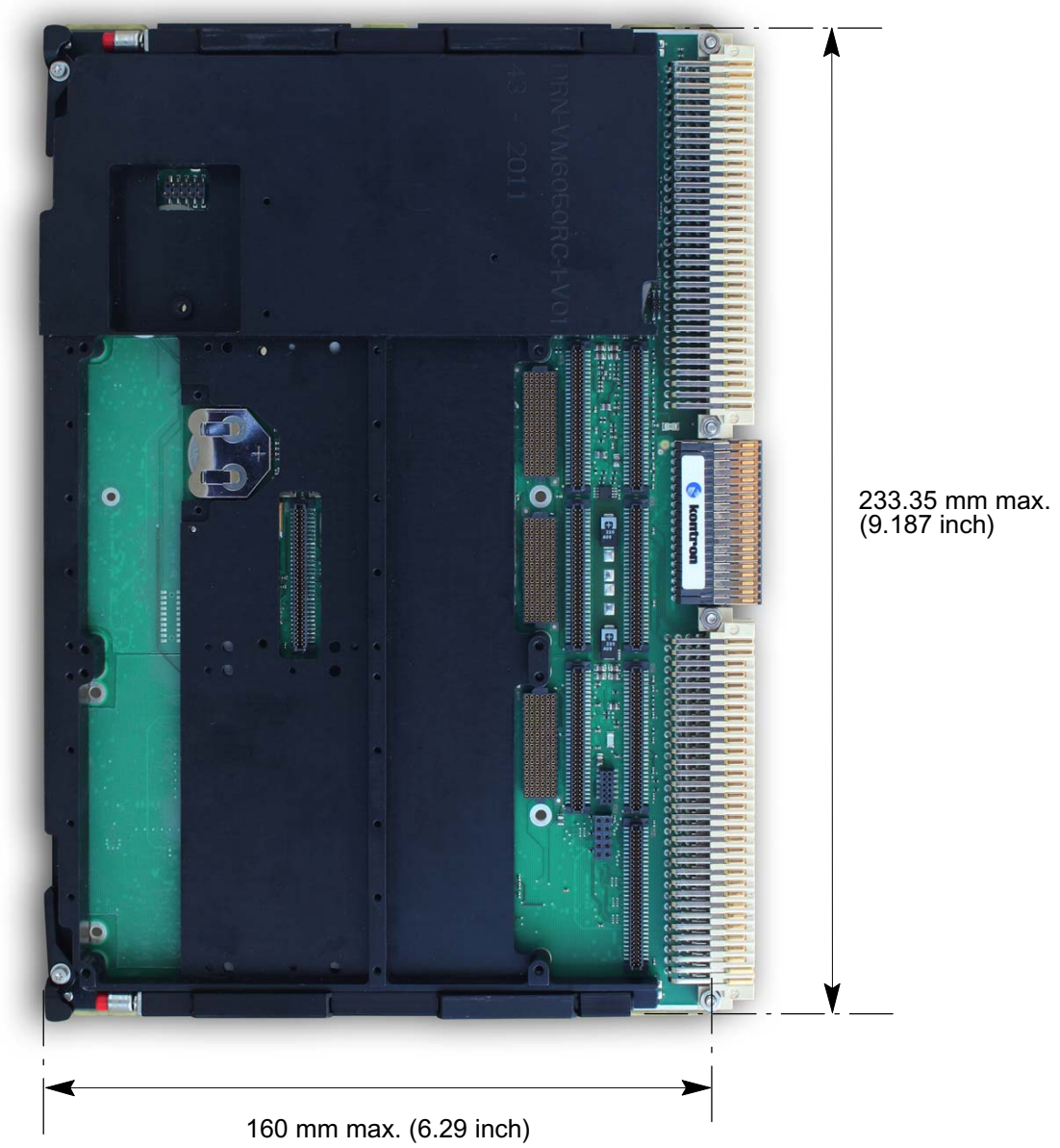


Figure 76: VME Dimensions

- **Length:** 233.35 mm max.
- **Depth:** 160 mm max.
- **Height:** 1 VME slot compatible
- **Weight:** ~800 g (approximatively)

9.7 MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

	GB (Hours)			AIC (Hours)		NS (Hours)		ARW (Hours)
	25°C	40°C	55°C	40°C	55°C	25°C	40°C	55°C
MTBF (hours)	344 800 h	258 400 h	173 400 h	53 500 h	44 300 h	66 600 h	57 100 h	15 400 h

Table 60: VM6050/RC MTBF Data

9.8 Peripheral Connectivity

The VM6050/RC board features the same connectors as the VM6050/SA except that:

- the front panel connectors are absent (serial lines COM1/COM2 are always routed to P2 on the rugged conduction-cooled board), ETH0 and ETH1 are no more available, only ETH2 and ETH3 are usable through rear P0 connector.
- the P4, P5, P6 and P9 onboard connectors are not fitted on the VM6050/RC board.

For detailed information about the connectors located on the VM6050, refer to section 4.2 page 63 “Onboard Connectors”.

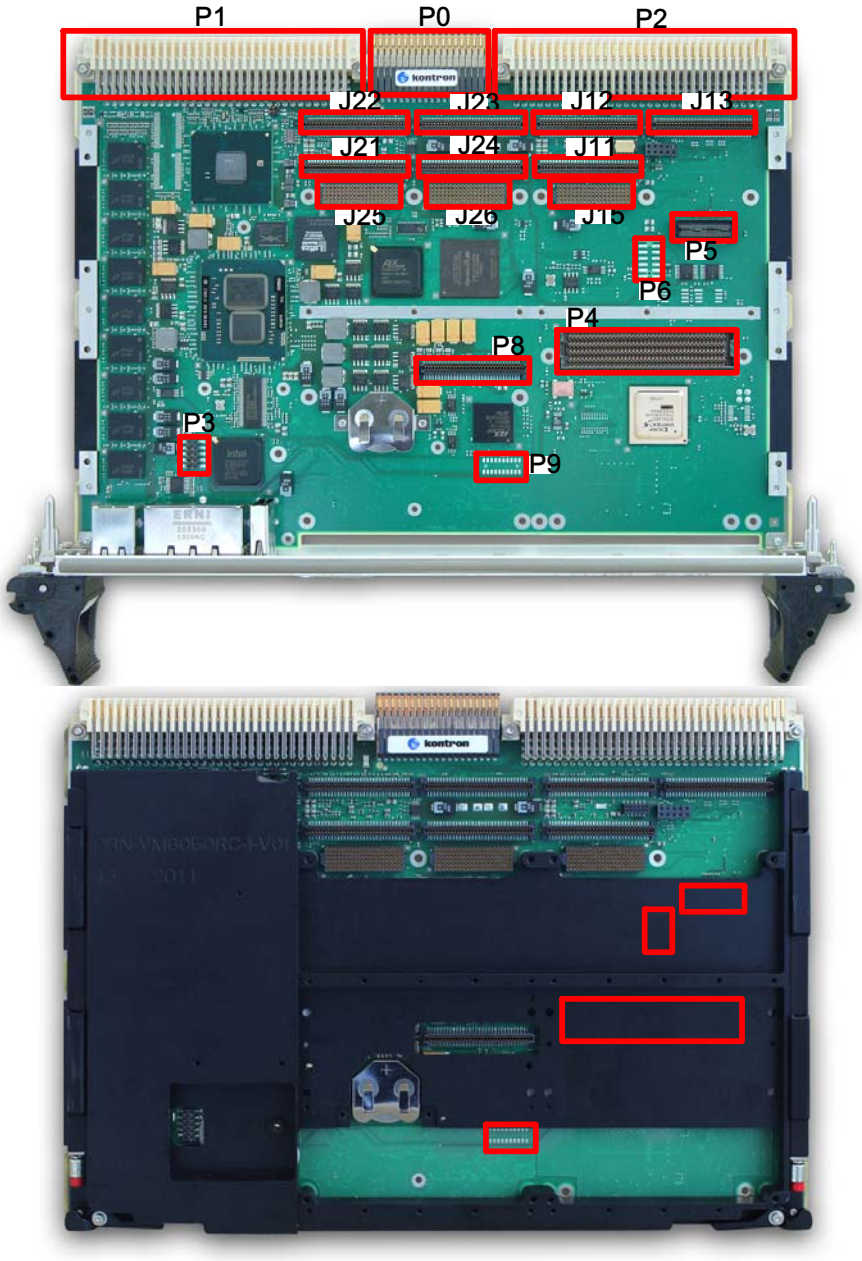


Figure 77: VM6050/RC Peripheral Connectivity

9.9 PMC/XMC Installation

Standard Anchorage Points

Install the XMC/PMC (for example XMC-ETH2-RC) to the VM6050/RC according to the following steps.

1. Check that the standoffs are attached to the XMC/PMC. Align the standoffs and the holes at the front, the middle and the rear of the PMC with the matching holes on the VM6050/RC board.
2. Lower the XMC/PMC component side down, fitting the mezzanine board connectors into their mating connectors on the VM6050/RC. Press them together so that the friction from the pins holds the mezzanine board in place.
3. Screw the XMC/PMC in place using mounting screws (5+2 at the front of the board, 5 in the middle of the board and 2 at the rear of the board). Tighten with a torque of 0.383 N.m. (3.389 Lb-In). Figure 78 shows the location of the standard anchorage points on an VM6050/RC board.

The PMC Installation Fastenings Kit is delivered with the VM6050/RC board. For each PMC location, it includes:

- 4x VIS-CZX-M2.5X6-INOX For the PMC assembly on the board red marks below
- 10x VIS-CZX-M2X6-INOX For PMC assembly on the board blue marks below

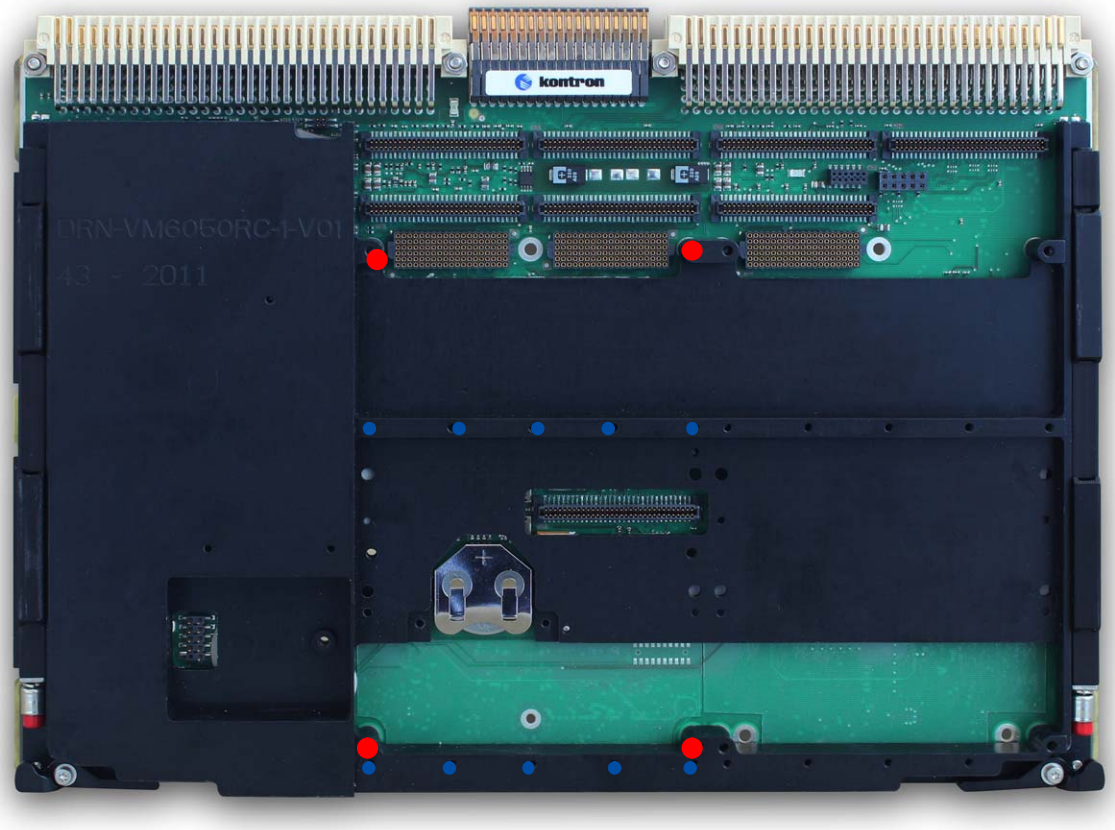


Figure 78: Standard **Anchorage Points on VM6050/RC Board**

Fastenings Kit

An optional secondary thermal interface ribs should be used to get the specified module thermal performance.

Order Code: **KIT-RIBPMC1V01-1**

2x RIB-PMC-1-V01	Two additional ribs		
4x VIS-CZX-M2X5-INOX	For the ribs assembly on the board		**black** marks below
10x VIS-CZX-M2.5X6-INOX	For the PMC assembly on the ribs	(6x)	
	For the PMC assembly on the board	(4x)	red marks below
10x VIS-CZX-M2X6-INOX	For PMC assembly on the board		blue marks below

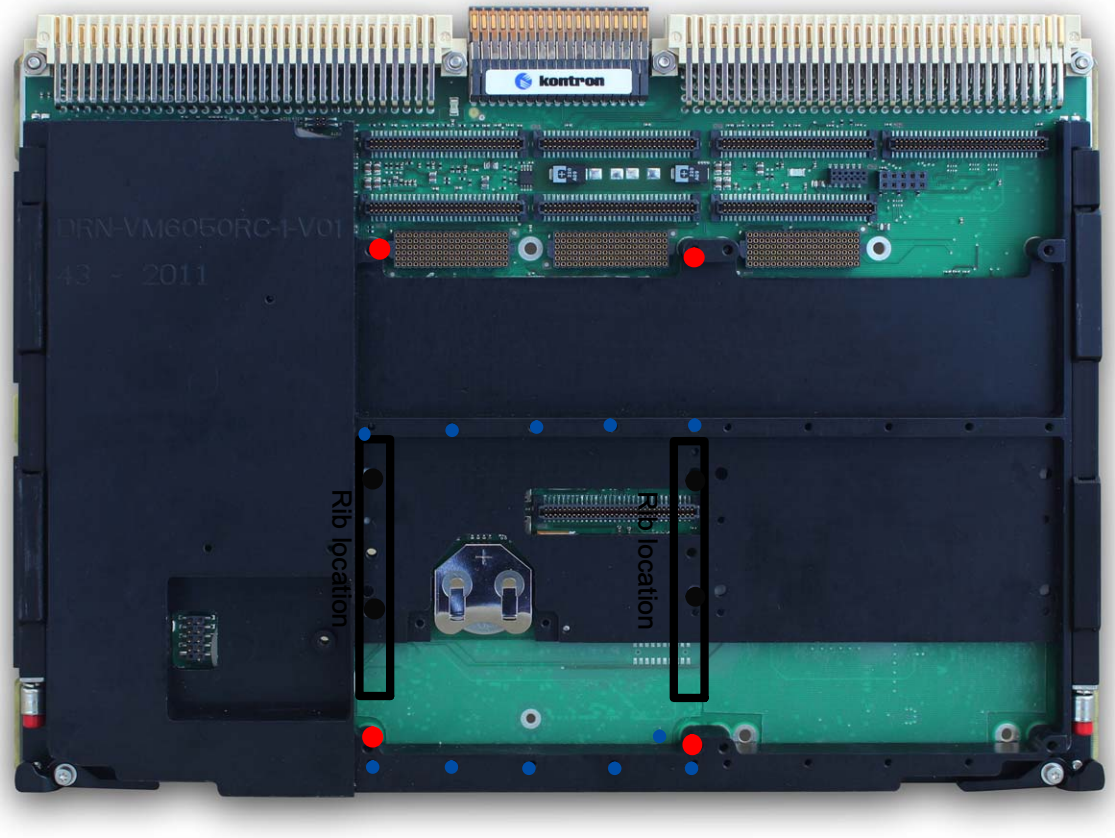


Figure 79: Usage of Fastenings Kit Ribs on VM6050/RC Board

9.10 USB/SATA Device Installation

The fastenings kit is delivered with the board, it includes:

- 1x screws CZX-M2.5X5 P3 side

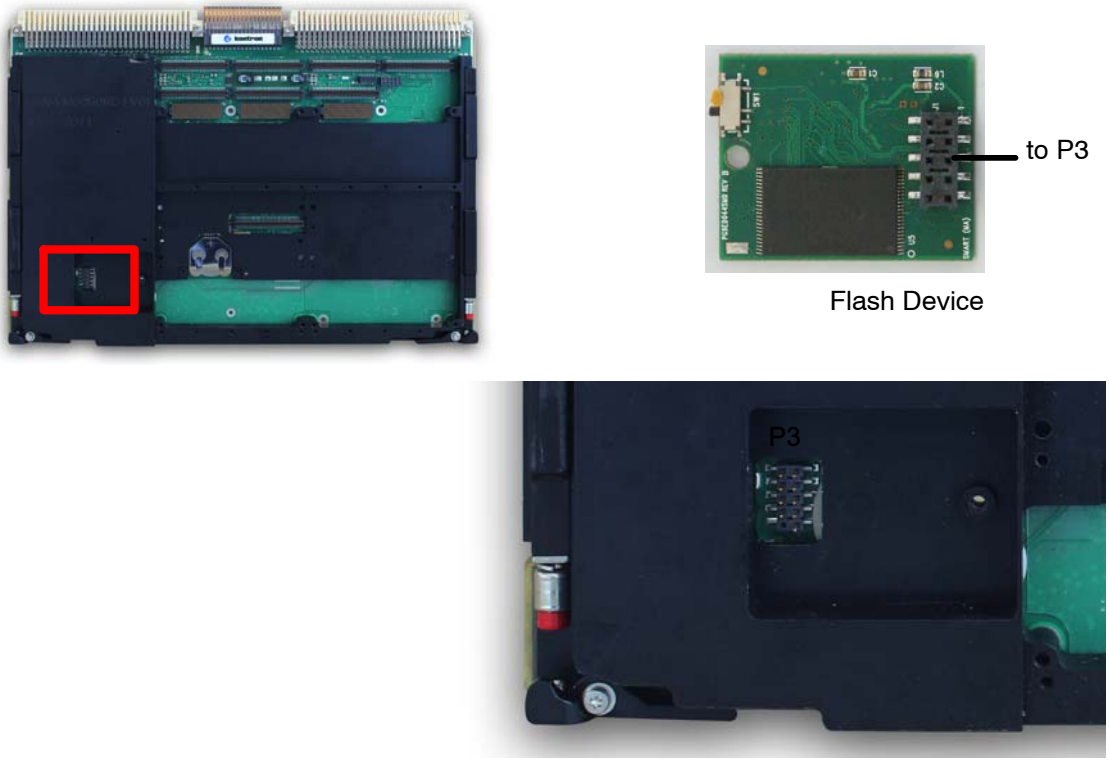
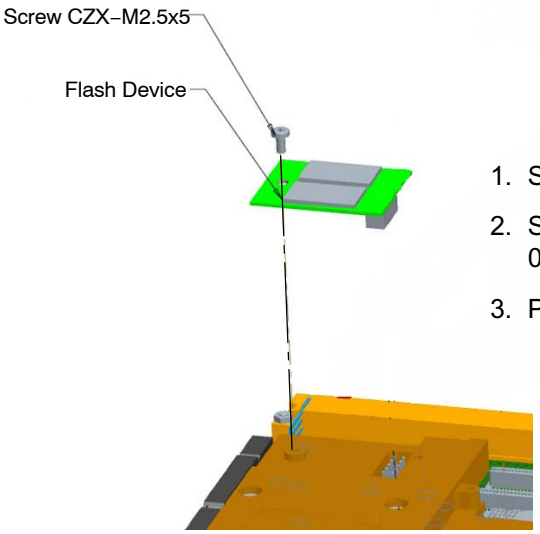


Figure 80: USB Device Location on VM6050/RC



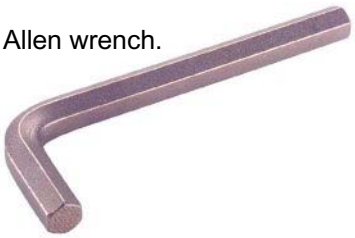
1. Set up the flash device using the P3 connector.
2. Screw the screw CZX-M2.5x5 using a torque of 0.279 N.m. (2.469 Lb-In).
3. Put a drop of Loctite 222 on the screw head.

Figure 81: USB Device Installation on VM6050/RC

9.11 Inserting and Removing the Board

Inserting the Board

1. Insert the board into the backplane of the rack.
2. Screw both hexagonal socket drive 3/32 across flats with a 3/32 Allen wrench.



Conduct the installation using a torque spanner with a the recommended torque of 0.682 N.m. (6.03 Lb-In).

Removing the Board

1. Unscrew both hexagonal socket drive 3/32 across flats with a 3/32 Allen wrench.
2. Remove the board from the backplane of the rack.

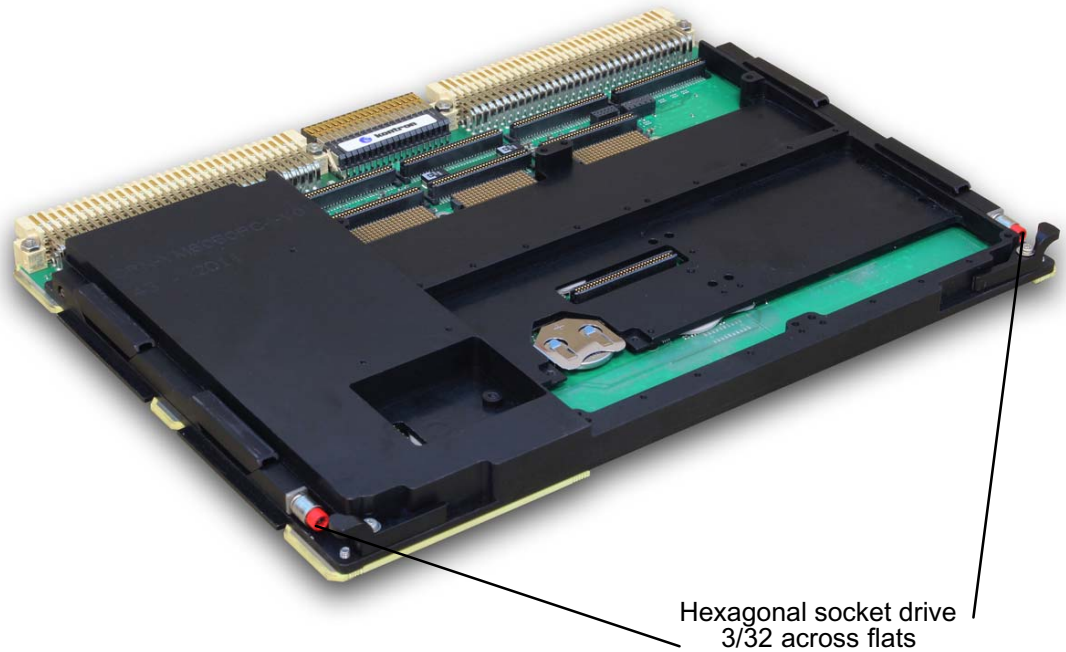


Figure 82: VM6050/RC - Inserting the Board

Do not touch the ruggedizer while removing the board from a rack because it can get very hot. Do not place the board on any surface or in any form of storage container until the board and its heatsink have cooled down to room temperature.

Depending on the chassis type (horizontal slots or vertical slots), make sure to insert the board correctly, as shown below:

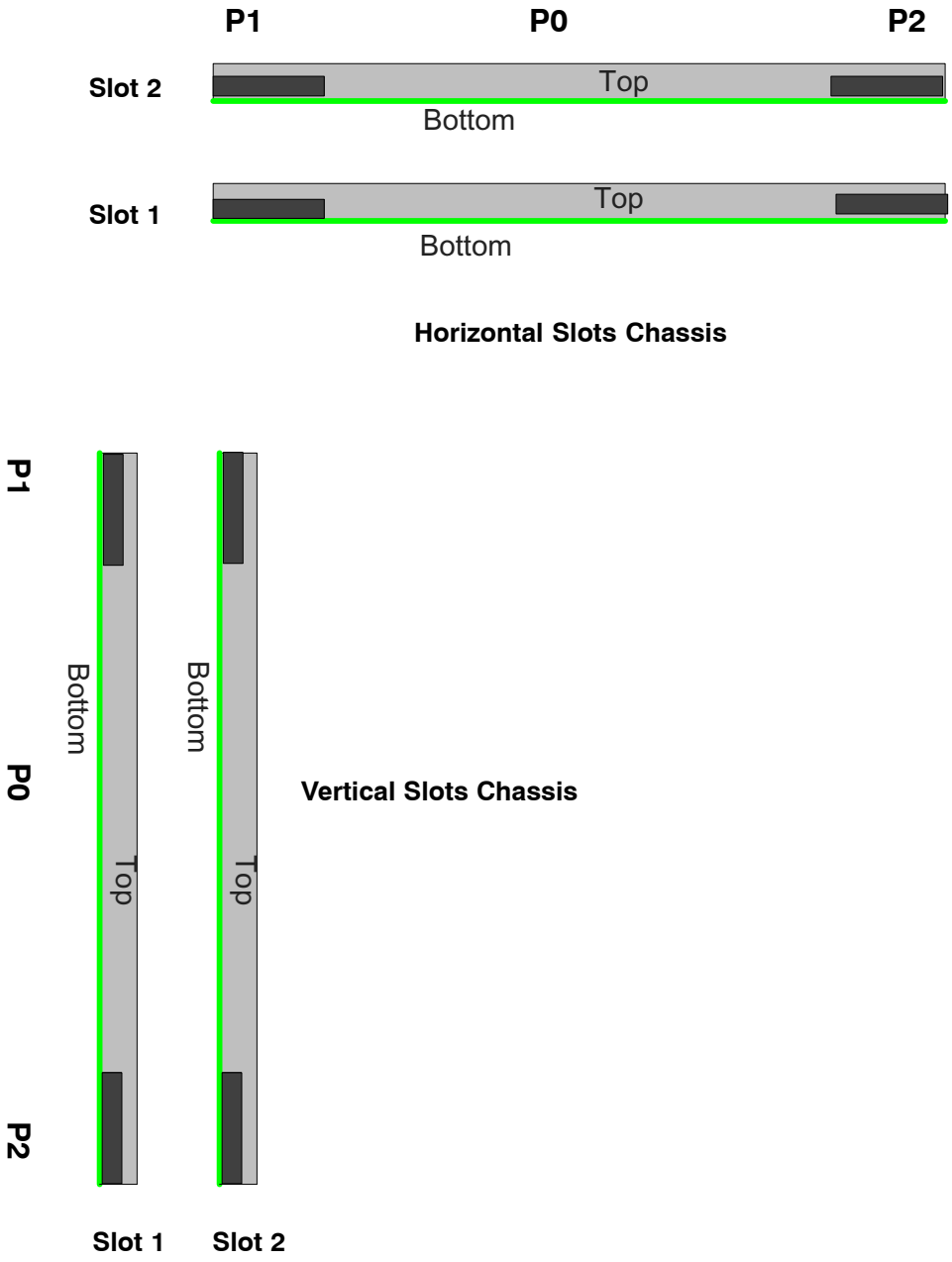


Figure 83: VM6050/RC - Slots Orientation

Appendix A - Graphics Resolution

Resolution	Supported (tested)	Video Display standard	Large Display Standard
2048 x 1536	No	QXGA	WQXGA
1920 x 1200	Yes	-	-
1920 x 1080	Yes	-	-
1680 x 1050	Yes	-	-
1600 x 1200	Yes	UXGA	WUXGA
1600 x 900	Yes	-	-
1440 x 900	Yes	-	-
1400 x 1050	Yes	SXGA+	WSXGA+
1366 x 768	Yes	-	-
1360 x 768	Yes	-	-
1280 x 1024	Yes	SXGA	WSXGA
1280 x 960	Yes	-	-
1280 x 800	Yes	-	-
1280 x 720	Yes	-	-
1280 x 600	Yes	-	-
1250 x 960	Yes	-	-
1152 x 864	Yes	XGA+	WXGA+
1024 x 768	Yes	XGA	WXGA
832 x 624	Yes		-
800 x 600	Yes	SVGA	-
720 x 400	Yes	-	-
640 x 480	Yes	VGA	WVGA
320 x 240	No	QVGA	-

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