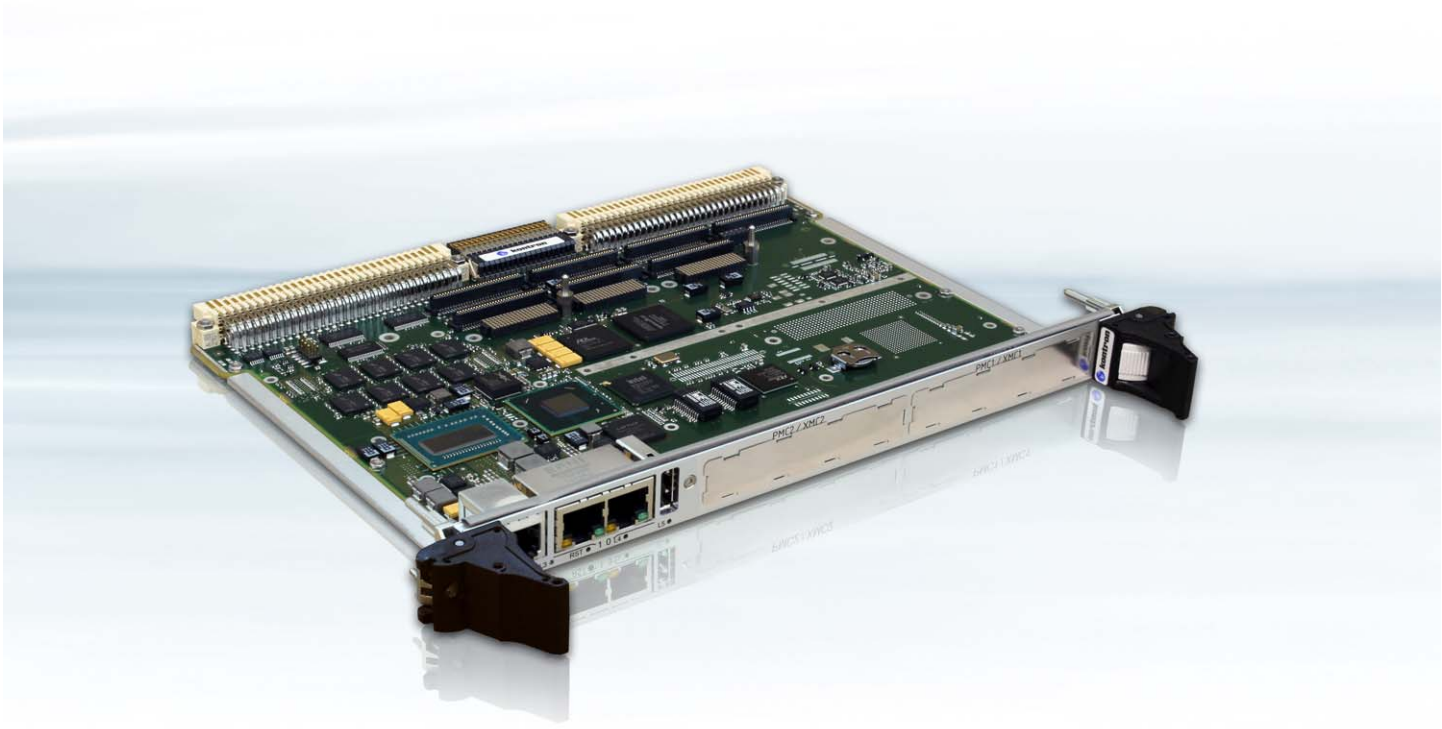
USER'S GUIDE



VM6052 / VM6054
6U VME Single Board Computer

CA.DT.B19-4e - May 2018

POSSIBILITIES START HERE kontron

VM6052/VM6054 User's Guide

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0e	Initial Issue	03-2015

Customer Support

Please contact our support team at support.KFR@kontron.com

Customer Service

As a trusted technology innovator and global solutions provider, Kontron extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly-experienced support enables Kontron to provide exceptional peace of mind to build and maintain successful products.

For more details on Kontron's service offerings such as: enhanced repair services, extended warranty, Kontron training academy, and more visit http://www.kontron.com/support-and-services/services.

Customer Comments

If you have any difficulties using this manual, discover an error, or just want to provide some feedback, contact Kontron support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised manual on our website.

SYMBOLS

The following symbols may be used in this manual:

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
NOTICE	NOTICE indicates a property damage message.
	**Electric Shock!** This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	**ESD Sensitive Device!** This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	**HOT Surface!** Do NOT touch! Allow to cool before servicing.
	**Laser!** This symbol inform of the risk of exposure to laser beam from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user manual. This symbol also indicates detail information about the specific product configuration.
	This symbol indicates important information which must be read carefully.
	This symbol precedes helpful hints and tips for daily use.

FOR YOUR SAFETY

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Caution, Electric Shock!
Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.
Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instructions

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

GENERAL INSTRUCTIONS ON USAGE

In order to maintain Kontron's product warranty and CE compliance, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty and the CE compliance.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version, that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

ENVIRONMENTAL PROTECTION STATEMENT

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Environmental protection is a high priority with Kontron.
Kontron follows the DEEE/WEEE directive.
You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when they become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE

Improve the environmental performance of all those involved during the lifecycle of EEE

TERMS AND CONDITIONS

Kontron warrants products in accordance with defined regional warranty periods. For more information about warranty compliance and conformity, and the warranty period in your region, visit http://www.kontron.com/terms-and-conditions

Kontron sells products worldwide and declares regional General Terms & Conditions of Sale, and Purchase Order Terms & Conditions. Visit http://www.kontron.com/terms-and-conditions

For contact information, refer to the corporate offices contact information on the last page of this user guide or visit our website CONTACT US.

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1 / Introduction

The Kontron VM605x is a 6U VME Single Board Computer (SBC) for parallel data and signal processing applications in the communications, military, aerospace, medical, industrial, and infotainment markets.

The VM605x implements Intel's next generation high performance embedded processor with integrated memory controller and Intel® HD graphics 4000 - the Intel Core™ i7 3rd Generation processor - coupled with the highly integrated Intel® Platform Controller Hub (PCH) QM77 with numerous Gigabit Ethernet, SATA, USB and PCIe channels.

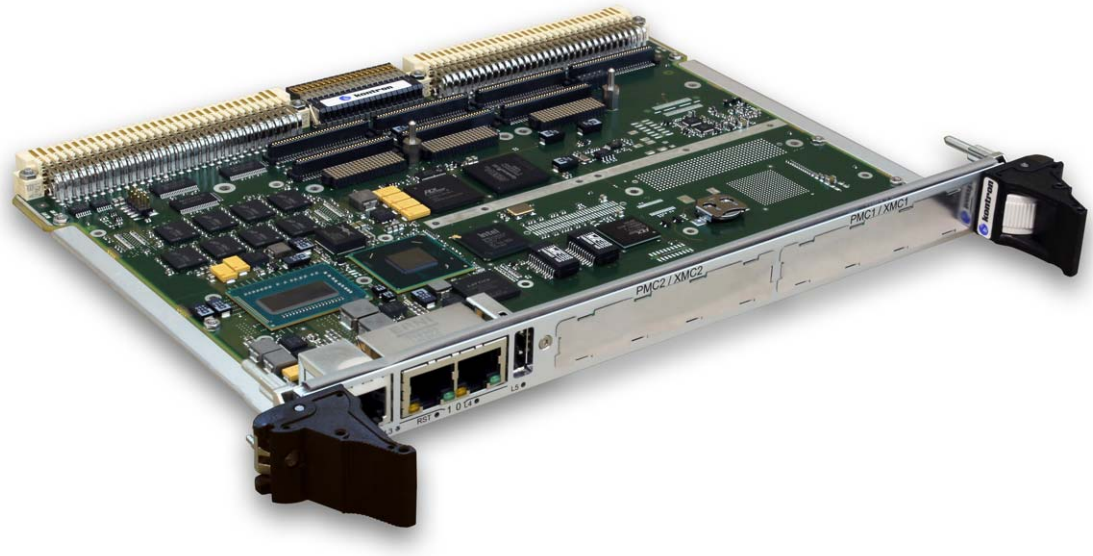
The VM605x board comes with UEFI BIOS and supports Linux. It is covered by Kontron's long term supply program, which guarantees customers multi-year supply of the product beyond its active life.

The VM605x provides exceptional I/O capabilities onboard and outstanding flexibility by being a 6U VME board to provide support for PMC and XMC mezzanine cards.

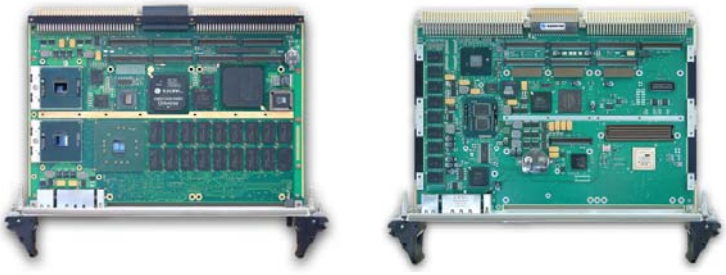
The VM605x's high performance, 2eSST, VME interface helps customers preserve their investment in legacy VME equipment.

The VM605x was designed to be Kontron's next generation VME SBC providing substantial price and performance improvement over previous generations of VME computers.

Figure 1: VM605x-SA/WA Overview



VM605x are designed to be I/O compatible with the 2 previous generation of x86 6U VME SBC from Kontron. See section 1.2 - Board Overview for more information on this.



1.1 Manual Overview

1.1.1 Objective

This guide provides general information, hardware instructions, operating instructions and functional description of the VM605x board. The onboard programming, onboard firmware and other software (e.g. drivers and BSPs) are described in detail in separate guides (see section 1.x "Related Publications").

This hardware technical documentation reflects the most recent version of the product. The "Hardware release Notes" (see section 1.6 "Related Publications") keeps track of the successive product evolutions.

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

1.1.2 Audience

This guide is written to cover, as far as possible the range of people who will handle or use the VM605x, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, system, cabling, grounding and communications.

1.1.3 Scope

This guide describes all variants of the VM605x series. It does not cover any PMC/XMC modules which are described in specific guides.

1.1.4 Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- 1 - Introduction (this chapter)
- 2 - Installation
- 3 - Additional Board Features
- 4 - Physical I/O
- 5 - Power and Thermal Specifications
- 6 - Graphics Module Characteristics
- 7 - Graphics and Audio Module Characteristics
- 8 - VM605x-RC - Characteristics
- 9 - VM605x-RTM Characteristics

1.1.5 Terminology, Definitions and Abbreviations

In this document, the term:

- **VM605x** will be associated to the 6U VME board including VM6052 dual core and VM6054 quad core modules.
  - VM605x-SA will be associated to the standard air-cooled commercial version of the board.
  - VM605x-WA will be associated to the extended air-cooled temperature version of the board.
  - VM605x-RA will be associated to the rugged air-cooled version of the board
  - VM605x-RC will be associated to the rugged conduction-cooled version of the board
- **VM605x-RTM** will be associated to the 6U VME Rear Transition Module (RTM).
- **MOD-GX** will be associated to the Graphic Module
- **MOD-GXA** will be associated to the Graphic and Audio Module

1.2 Board Overview

1.2.1 Main Features

Intel® Core™ i7 3rd Generation Architecture

The VM605x single board computer is a VME computing blade for parallel data and signal processing application. Target applications include radar, sonar, imaging systems, airborne fighters, and unmanned aerial vehicle (UAV) radar, as well as rugged multi-display consoles.

The processing node of the VM605x implements an Intel Core™ i7 3rd Generation processor with Hyperthreading and Turbo boost technology coupled with a dual channel DDR3 memory. The VM6054 board implements a quad core Standard Voltage i7-3612QE, TDP 35W and the VM6052 board implements a dual core Utra Low Voltage i7-3517UE, TDP 25W. The highly integrated Intel® QM77 platform hub provides numerous Ethernet, SATA, USB and PCIe channels. The 6U-format VM605x is available in standard air-cooled version, extended air-cooled version, rugged air-cooled version and rugged conduction cooled version.

The processor frequency is 2.1 GHz for the quad core version at 35W and 2.2 GHz for the dual core version at 25W. The dual core version can also be configured by the user to operate at 1.7 GHz/17W or 0.8 GHz/14W.

Moreover, the Intel Core™ i7 3rd Generation processor is equipped with the Turbo Boost technology, which allows increasing the frequency up to 3.1 GHz for quad core and 2.8 GHz for dual core (2.8 GHz on quad core model with all cores running and 2.6 GHz on dual core model with all cores running) when the total on chip power allows it (depending on other cores, graphics activity and previous overall activities).

Soldered DDR3 Memories with the Support of ECC

The processor accesses two memory-channels (2 x 72-bit) having a total size of 8 or 16 GB. The DDR3 memory technology used operates at 1,333 or 1,600 Mbits/s depending on the VM605x model. An 8-bit ECC memory is implemented to detect and correct errors.

Numerous Storage Interface and Non Volatile Memories

The following storage features are available :

- An onboard or mezzanine SATA NAND Flash with 32 GB capacity (Multiple Levels Cell) or 8 GB capacity (Single Level Cell extended temperature).
- Redundant 64 Mbits NOR flash memories are used to store firmware code.
- Two serial 256 Kbits EEPROMs are dedicated to system and application data storage.
- A 1 Mbits ferroelectric, non-volatile random access memory allows the backup of critical data when the board is powered off. This 1 Mbits ferroelectric RAM is a user memory device.

All the Flash and non volatile memories onboard have a write protect mechanism taking into account the NVMRO (Non Volatile Memory read Only) signal.

Backplane Switch

Two Gigabit Ethernet links are available on P0 connector. P0 Ethernet routing supports VITA 31.1 backplane networking.

In addition, one 4x PCI Express link is available on P0.

Extensive I/O Connectivity

A SATA drive slot is available onboard supporting SATA HDD or SATA SSD.

The VM605x is equipped with the ALMA2f VME controller supporting the VME64x and 2eSST protocols offering up to 320 MB/s peak throughput.

The VM605x provides up to four 10/100/1000BASE-T(X) Ethernet interfaces, two EIA-232 serial lines, up to 8 general purpose I/Os (GPIO), four USB 2.0 links, four SATA interfaces, one 4x PCI-Express link and one optional DisplayPort interface.

Two onboard mezzanine sites support PCI and PCI-Express cards.

Legacy Compatibility

The VM605x has been designed to offer a legacy I/O compatibility with the Kontron's PENTXM2/ PENTXM4, VM6050 and VM6250 boards to provide an easy path for technology insertion into existing systems.

Software

Kontron is one of the few compact PCI, VME and VPX vendors providing in-house support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software manufacturers, Kontron is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

Finally, Kontron grants his customer owners of a maintenance agreement a hotline software support and regular software updates. A dedicated web site is also available for online updates and release downloads.

The VM605x is delivered with the UEFI BIOS from AMI.

The VM605x supports Linux Fedora distribution.

Please contact Kontron for further information regarding other operating systems and software support.

Harsh Environments

The VM605x has been designed to use the same PCB for both air and conduction-cooled boards. Build variants span a complete range of temperature, shock and vibration requirements as specified in section 1.3 page 16.

10-year Long Life Cycle

Investing in a new project is always a challenge and risky. Maximizing the lifetime of an application is therefore a critical issue when it comes to saving development investments.

The VM605x has been designed with long life cycle components. Beyond the use of standard commercially available components, Kontron offers longevity of supply services which are designed to make the VM605x available for ten years or longer.

Carrier Board

The VM605x supports the V2PMC2, a 6U VME PCI-X/PMC carrier card that holds up to two single-width or one double-width PCI-X/PMC modules.

Rear Transition Module

The VM605x supports the VM605x-RTM, a 6U VME Rear Transition Module compliant to PMC I/O Module Standard VITA 36 - 199x Draft 0.1 July 19, 1999 (mechanical and PIM format).

Extra I/O Module

The VM605x is able to support a module compliant to PMC standard IEEE P1386.1 with additionnal I/Os such as graphic. This approach has been used to design mezzanine cards implementing, depending on card, VGA and DP support or audio and HDMI on the front and back of VM605x. See chapter 6 page 88 (Graphics Module Characteristics) and chapter 7 page 100 (Graphics and Audio Module Characteristics) for details on these boards which fit the middle PMC/XMC slot of the SBC .

1.2.2 Block Diagram

Figure 2: VM605x Block Diagram

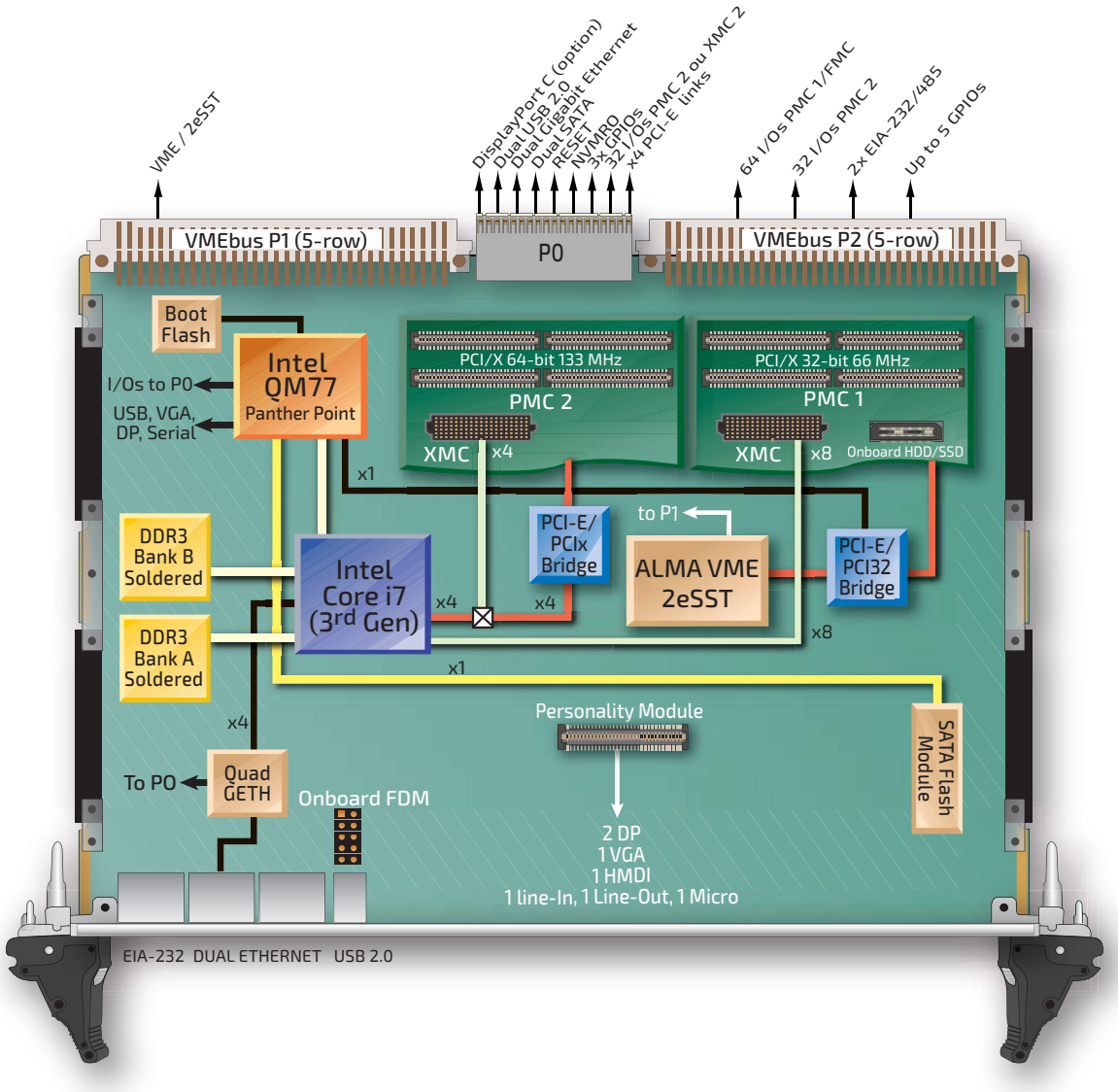
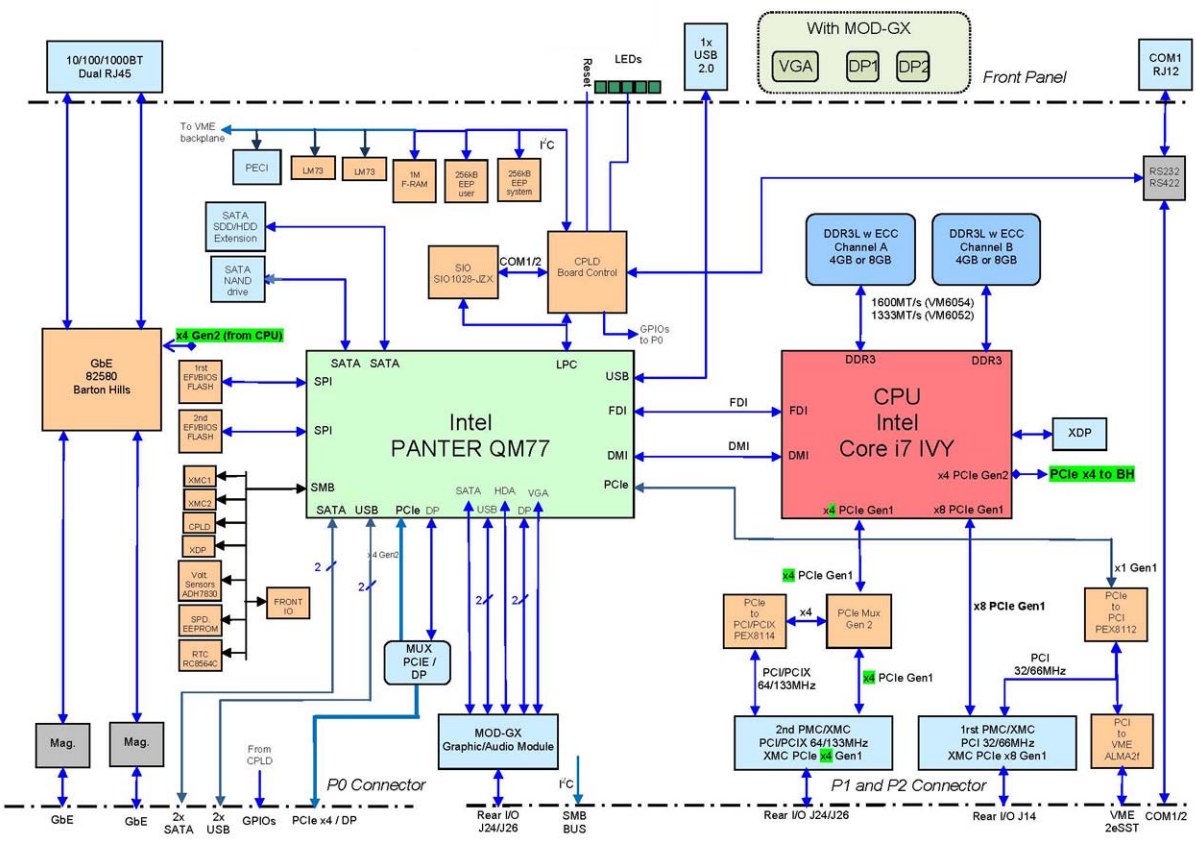


Figure 3: VM605x Functional Block Diagram



1.2.3 Ordering Information

Manufacturing Options

- CPU Frequency:
  2.1 GHz (VM6054)
  2.2 GHz (VM6052)
- DDR3 SDRAM Size:
  8 GB total onboard
  16 GB total onboard
- Ruggedization Levels:
  Standard Air-Cooled (SA)
  Extended Temperature (WA)
  Rugged Air-Cooled (RA)
  Rugged Conduction-Cooled (RC)
- SATA Flash Size:
  Absent
  16 GB SLC industrial grade
  32 GB SLC industrial grade
  32 GB MLC commercial grade
- Trusted Platform Module:
  On demand
- Battery:
  Present
  Absent (including support)
- Serial line/ GPIOs:
  Full COM2 / 3 GPIOs (PENTXM2 legacy compatibility)
  Simplified COM2/ 6 GPIOs (VM6050 legacy compatibility)
  Simplified COM2/ 8 GPIOs (VM6050 legacy compatibility)
- SATA Extension Module
  Absent (default, no P5 connector)
  On-board disk carrier (KIT-DISK25-SATA)
- Power-on Built-In-Test
  Absent
  PBIT object run time

Table 1: VM605x Order Codes

ORDER CODE		DESCRIPTION
VM6052	VM6052-SA28-x0110000	6U single slot 4 HP (0,8") VME SBC 2.2 GHz Intel® dual-core Core i7 3517UE processor, 8 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, 3 GPIOSs on P0, Air-Cooled (0°C to +55°C)
VM6052	VM6052-SA28-x0210000	6U single slot 4 HP (0,8") VME SBC 2.2 GHz Intel® dual-core Core i7 3517UE processor, 8 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, 3 GPIOSs on P0, Air-Cooled (0°C to +55°C), 5V only SBC without P0 (12V needed for soldered flash and PMC/XMC is required)
VM6052	VM6052-SA28-x0310000	6U single slot 4 HP (0,8") VME SBC 2.2 GHz Intel® dual-core Core i7 3517UE processor, 8 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, 3 GPIOSs on P0, Air-Cooled (0°C to +55°C), 5V only SBC with P0 (12V needed for soldered flash and PMC/XMC is required)
VM6052	VM6052-SA28-x0160000	6U single slot 4 HP (0,8") VME SBC 2.2 GHz Intel® dual-core Core i7 3517UE processor, 8 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, 3 GPIOs on P2 + 3 GPIOSs on P0, Air-Cooled (0°C to +55°C)
VM6052	VM6052-SA28-x0111000	6U single slot 4 HP (0,8") VME SBC 2.2 GHz Intel® dual-core Core i7 3517UE processor, 8 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, 3 GPIOSs on P0, no battery, Air-Cooled (0°C to +55°C)
VM6052	VM6052-SA28-x011000P	6U single slot 4 HP (0,8") VME SBC 2.2 GHz Intel® dual-core Core i7 3517UE processor, 8 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, 3 GPIOSs on P0, PBIT object run time, Air-Cooled (0°C to +55°C)
VM6052	VM6052-SA2F-x0110000	6U single slot 4 HP (0,8") VME SBC 2.2 GHz Intel® dual-core Core i7 3517UE processor, 16 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, Air-Cooled (0°C to +55°C)

ORDER CODE		DESCRIPTION
VM6052	VM6052-WA28-x0110000	6U single slot 4 HP (0,8") VME SBC 2.2 GHz Intel® dual-core Core i7 3517UE processor, 8 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, 3 GPIOSs on P0, Extended Air-Cooled (-20°C to +65°C)
VM6052	VM6052-RC28-x0110000	6U single slot 4 HP (0,8") VME SBC 2.2 GHz Intel® dual-core Core i7 3517UE processor, 8 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, 3 GPIOSs on P0, Conduction Cooled (-40°C to +85°C)
VM6054	VM6054-SA48-x0110000	6U single slot 4 HP (0,8") VME SBC 2.1 GHz Intel® quad-core Core i7 3612QE processor, 8 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, 3 GPIOSs on P0, Air-Cooled (0°C to +55°C)
VM6054	VM6054-SA48-x0210000	6U single slot 4 HP (0,8") VME SBC 2.1 GHz Intel® quad-core Core i7 3612QE processor, 8 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, 3 GPIOSs on P0, Air-Cooled (0°C to +55°C), 5V only SBC without P0 (12V needed for soldered flash and PMC/XMC is required)
VM6054	VM6054-SA48-x0310000	6U single slot 4 HP (0,8") VME SBC 2.1 GHz Intel® quad-core Core i7 3612QE processor, 8 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, 3 GPIOSs on P0, Air-Cooled (0°C to +55°C), 5V only SBC with P0 (12V needed for soldered flash and PMC/XMC is required)
VM6054	VM6054-SA48-x0160000	6U single slot 4 HP (0,8") VME SBC 2.1 GHz Intel® quad-core Core i7 3612QE processor, 8 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, 3 GPIOs on P2 + 3 GPIOSs on P0, Air-Cooled (0°C to +55°C)
VM6054	VM6054-SA48-x0111000	6U single slot 4 HP (0,8") VME SBC 2.1 GHz Intel® quad-core Core i7 3612QE processor, 8 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, 3 GPIOSs on P0, no battery, Air-Cooled (0°C to +55°C)
VM6054	VM6052- SA48-x011000P	6U single slot 4 HP (0,8") VME SBC 2.1 GHz Intel® quad-core Core i7 3612QE processor, 8 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, 3 GPIOSs on P0, PBIT object run time, Air-Cooled (0°C to +55°C)
VM6054	VM6054-SA4F-x0110000	6U single slot 4 HP (0,8") VME SBC 2.1 GHz Intel® quad-core Core i7 3612QE processor, 16 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, Air-Cooled (0°C to +55°C)
VM6054	VM6054-WA48-x0110000	6U single slot 4 HP (0,8") VME SBC 2.1 GHz Intel® quad-core Core i7 3612QE processor, 8 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, 3 GPIOSs on P0, Extended Air-Cooled (-20°C to +65°C)
VM6054	VM6054-RC48-x0110000	6U single slot 4 HP (0,8") VME SBC 2.1 GHz Intel® quad-core Core i7 3612QE processor, 8 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, 3 GPIOSs on P0, Conduction Cooled (-40°C to +70°C)

x: 0 = no soldered flash
2 = 16 GB soldered flash (industrial grade)
3 = 32 GB soldered flash (commercial grade)
4 = 32 GB soldered flash (industrial grade)

Table 2: Associated Product Order Codes

ASSOCIATED PRODUCT		
ORDER CODE		DESCRIPTION
RTM	PBV36-P0-VM6-00	6U VME Air-Cooled Rear Transition Module, 2 PIMs, no face-plate to use with PIM-2DP-00
Console Cable	KIT-RJ12DB9	Adaptation Cable RJ-12 <-> DB-9
PMCs Carrier	V2PMC2-SA	6U VME Air-Cooled Dual PMCs Carrier Card
PMCs Carrier	V2PMC2-RC	6U VME Conduction-Cooled Dual PMCs Carrier Card
USB Flash Disk	FDM-USB-xGB-2MM-IV	USB Flash Disk Module (contact Kontron for the available capacity)
SATA Flash Disk	FDM-SATA-xGB-I0V	SATA Flash Disk Module (contact Kontron for the available capacity)

ORDER CODE		DESCRIPTION
Kit Disk SATA(1)	KIT-DISK25-SATA	Kit Disk SATA; compatible with SATA disk 2.5-inch
EZ-VM605x	EZ-VM605x	Laboratory 6U VME Air-Cooled Development System
Graphics Module	MOD-GX-SA-00	Air-cooled graphics module with two DisplayPorts and one VGA Port on front panel
Graphics Module	MOD-GX-RC-00	Conduction cooled graphics module with two DisplayPorts on rear / No VGA
Audio and graphics module	MOD-GXA-SA-00	Air-cooled audio and graphics module with two HDMI interface and analogic audio interface on front panel

(1) Kit disk are only available on VM605x SA or WA version.

1.2.4 I/O Interfaces

Table 3: I/O Interfaces

FUNCTION	DESCRIPTION
Ethernet	Intel i82580 low-power quad Gigabit Ethernet Transceiver: - Two 10/100/1000BASE-T(X) ports available on RJ-45 front panel connectors - Two 10/100/1000BASE-T(X) ports available on the rear P0 connector
USB	Four USB 2.0 channels - USB0 — One USB port available on the VM605x front panel - USB2 — USB port available on rear P0 connector - USB3 — USB port available on rear P0 connector - FDM-USB — 9-pin USB pin header, horizontal USB flash disk module
Serial ATA (SATA)	- Two SATA II ports are available on rear P0 connector - One SATA port is available onboard. - One SATA port is available onboard flash disk module
Serial Ports	Two serial ports EIA-232/485 - COM1 — EIA-232/485 (simplified) port on RJ-12 front panel connector or on the rear P2 connector - COM2 — EIA-232/485 on the rear P2 connector
GPIO	Three General Purpose I/Os on rear P0 connector. Extra GPIOs are available on P2 on customer request
LED	Five status LEDs on front panel: L1, L2, L3, L4, L5
Reset	One reset button on front panel.
PMC/XMC	2x PMC/XMC slots PCI 32-bit 66 Mhz available on slot 1, no 5V tolerant PCI-X 64-bit 133 Mhz available on slot 2, no 5V toleant XMC 8*lanes for slot 1, XMC 4x lanes for slot 2 compliant to Gen1 (2.5 GT/s) PCI-e frequency
Graphic	2x DisplayPort interface on P8 connector, HDMI/DVI compatible 1x VGA interface on P8 connector
Audio	High definition Audio on P9 connector

Table 4: Peripheral Connectivity

FUNCTION	VM605x		VM605x-RTM	
	FRONT PANEL	ONBOARD	FRONT PANEL	ONBOARD
Gigabit Ethernet	Y (x2)	-	Y (x2)	-
USB0	Y	-	-	-
USB2, USB3	-	-	Y (x1)	-
USB-FDM	-	Y (9-pin)	-	-
SATA (P0 Manufacturing Option)	-	-	Y (x2)	-
SATA (onboard Manufacturing Option)	-	Y	-	-
SATA Mezzanine	-	Y (9-pin)	-	-
COM1 (EIA-232)	Y	-	-	Y (10-pin)
COM2 (EIA-232)	-	-	-	Y (10-pin)
GPIO	-	-	-	Y (upt to 8)
LED	Y (x5)	-	-	-
Reset Button	Y	-	-	-
PCI-Express	-	-	Y	-
SMB	-	-	-	Y
DP* or HDMI/DVI** (port B & D)	Y (x2)	-	Y (x2)	-
DP or HDMI/DVI (port C)	-	-	Y***	-
VGA Interface*	Y	-	-	-
Analogic Audio**	Y	-	Y***	-

* Available with MOD-GX board

** Available with MOD-GXA board

*** Contact Kontron for availability

1.2.5 Front Interfaces

Not available on RC (Rugged Conduction-Cooled) boards

Figure 4: Front Panel Connectors

Table 5: Front I/O Interfaces

FUNCTION	DESCRIPTION	SEE ALSO
Serial Ports	COM: 1x EIA-232/EIA-485 UART interface for CPU on RJ-12 connector.	Section 4.1.1 for Pin Assignment
Gigabit Ethernet	Two 10/100/1000BASE-T(X) ports on RJ45	Section 4.1.2 for Pin Assignment
USB	USB 2.0 interface	Section 4.1.3 for Pin Assignment
Reset	Reset push button	Figure 5
LEDs	5 LEDs reporting the board CPU health status and activity	Section 4.7 for LEDs Description
PMC/XMC	2x PMC/XMC slots	Sections 4.4 & 4.5 for PMC/XMC Description

Figure 5: Reset Button and LEDs

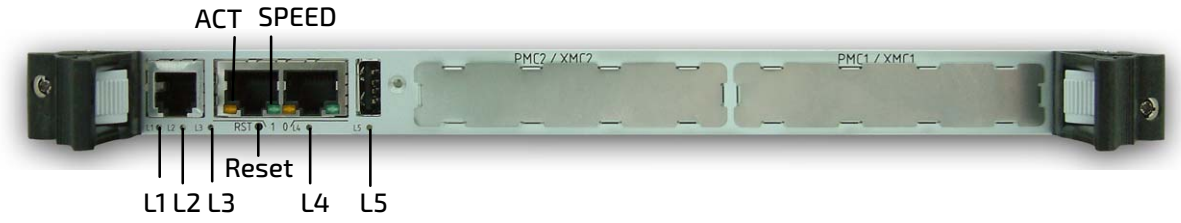


Figure 6: MOD-GX Front Panel

Figure 7: MOD-GXA Front Panel

1.2.6 Components Layout

Figure 8: VM605x Components Layout (Top view)

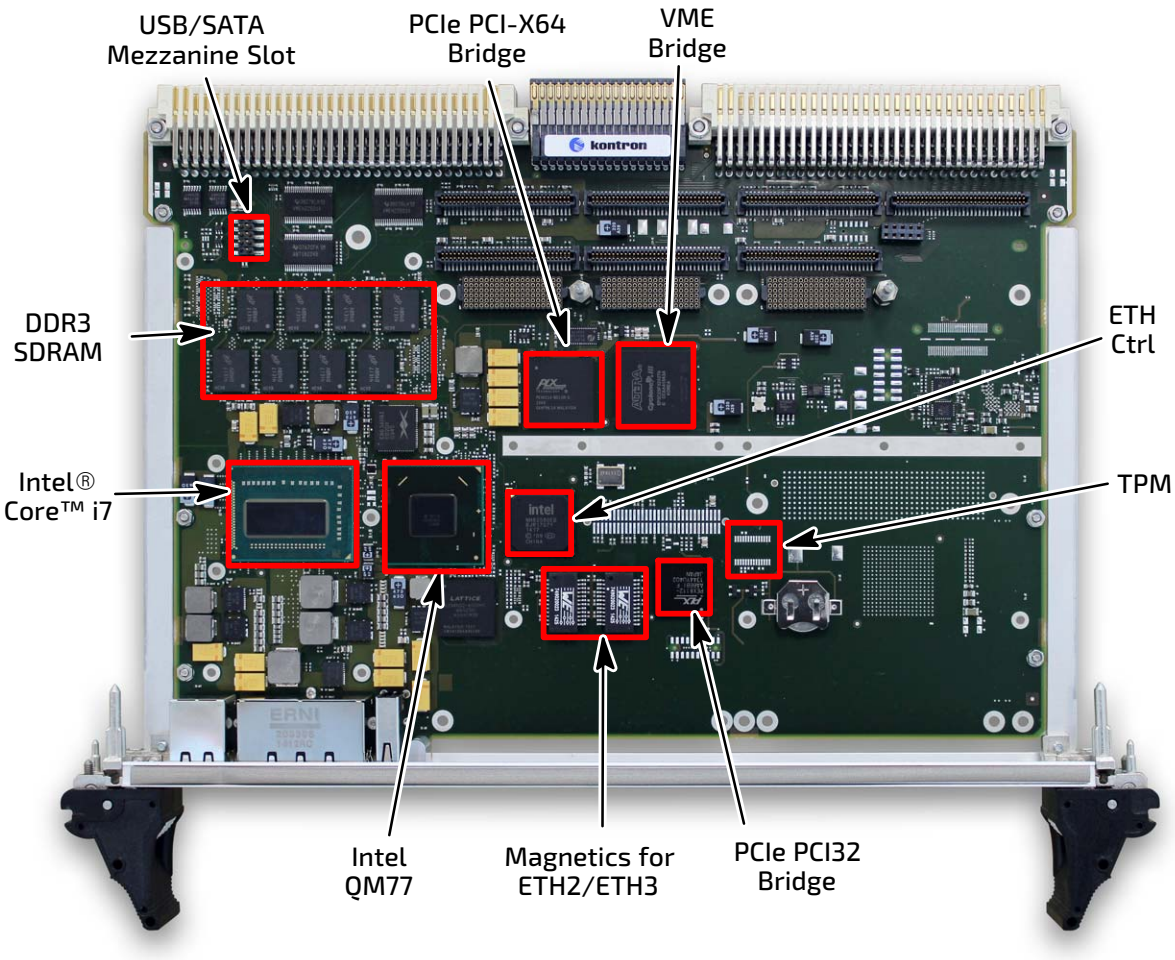
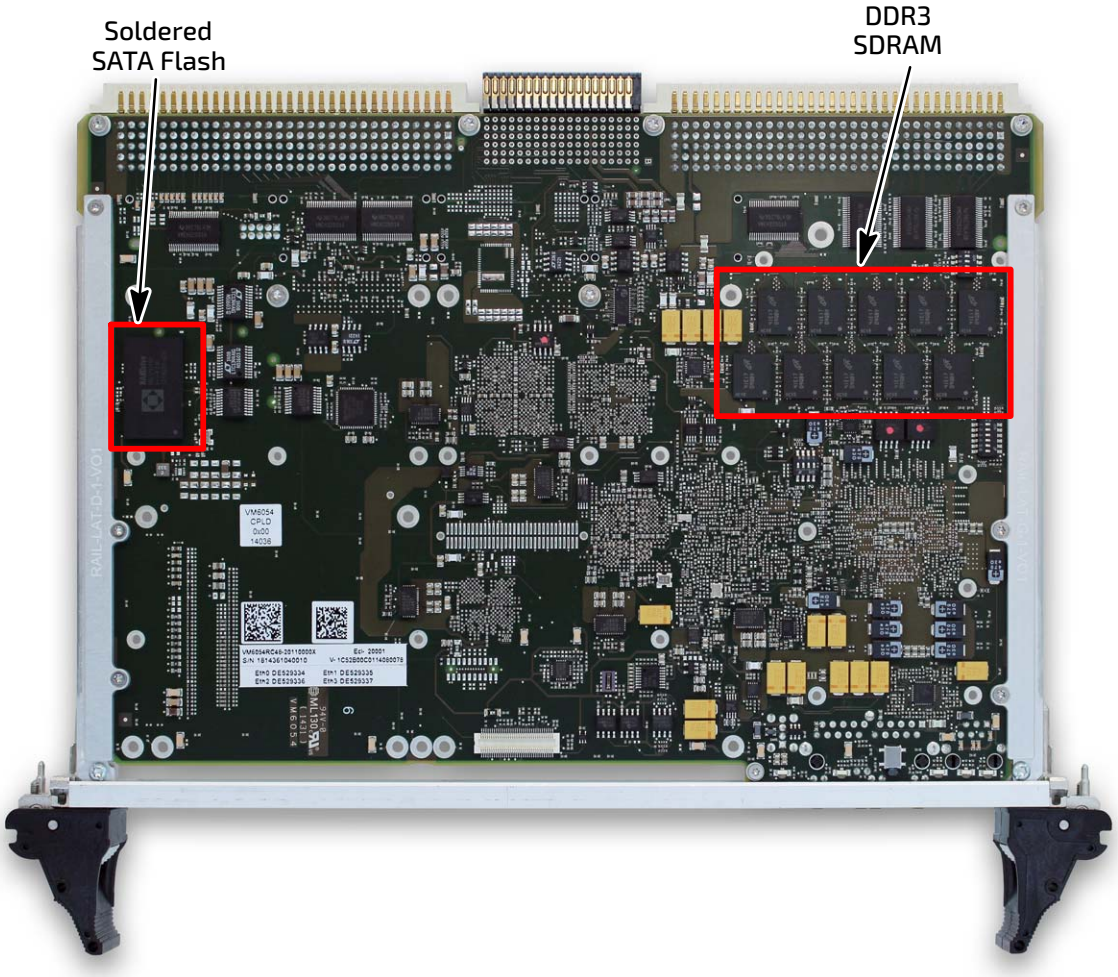


Figure 9: VM605x Components Layout (Bottom view)



1.2.7 Technical Specification

Table 6: VM605x Main Characteristics

Form Factor	
Form Factor	6U VME, single slot, 0.8 inch pitch
Processor: Intel® Core™ i7	
Processor	Intel® Core™ i7 3rd Gen - 3612QE (quad core 2.1 GHz) or 3517UE (dual core 2.2 GHz) Quad Core: 6M cache, 4 execution cores, 8 threads Dual Core: 4M cache, 2 execution cores, 4 threads. CPU power dissipation: Quad core, TDP 35W Dual core, user configurable TDP 25W/2.2 GHz, 17W/1.7 GHz, 14W/0.8 GHz 22-nanometer silicon technology.
Memory Controller	Integrated DDR3 memory controller with ECC support, 1333 or 1600 Mbits/s depending on models. Two memory channels of 72 bits each.
Graphics Core	Integrated Graphics Core, Intel® HD graphics 4000
PCI Express Interface	4 lanes 5 GT/s gen 2(*) PCIe to 1000BASE-T quad Ethernet controller 4 lanes 2.5 GT/s gen 1 PCIe to XMC2 slot or to PCIe/PCI-x Bridge to PMC 8 lanes 2.5 GT/s gen 1 PCIe to XMC1

(*) PCI Express interface of quad Ethernet controller is reduce to 2 lanes 2.5 GT/s gen 1 for all classes operating below 0°C, SA class is not concerned.
Refer to Hardware Release Note for further details.

DMI Interface	x4 5 GT/s point-to-point DMI interface to Platform Controller Hub (PCH).
FDI Interface	Carries display traffic from the integrated graphics controller to the PCH for generation of external display protocols
AVX Instructions	Supported by the two processors 3612QE and 3517UE
PCH: Panther point-M	
PCI Express Interface	4 lanes PCIe to VME backplane connector (P0) 1 lane PCIe to PCIe/ PCI bridge to PMC1 and VME bridge
SPI Interface	Connects to two SPI flash devices (8 Mbytes each)
LPC	33 MHz LPC, for SuperIO and CPLD link
SATA	Up to 6 Gb/s integrated Serial ATA host controllers 2 SATA ports on P0 1 SATA port for onboard SATA FLASH 1 SATA port on FDM-SATA mezzanine connector 1 SATA pont on HDD-carrier
USB	2 USB 2.0 ports on the P0 rear connectors 1 USB 2.0 port for onboard Flash mezzanine connector 1 front USB 2.0
DisplayPorts	Two DisplayPorts or HDMI/DVI available on personality module connector (P8) One DisplayPort or HDMI/DVI available on P0 connector (Option)
VGA	One VGA port available on personality module connector (P8)
Audio Port	High Digital Audio (HDA) port available on personality module connector (P9)
Memory	
System Memory	Up to 16 GB DDR3 SDRAM at 1600 Mb/s, two memory channels
SPI Flash	Firmware Boot Device, 2x 8 Mbytes
NAND Flash	Option Up to 32 GB SATA Nand Flash storage
F-RAM	F-RAM 1 Mbit of non volatile ferroelectric RAM
EEPROM	One serial 256 Kbit EEPROM dedicated to system data One serial 256 Kbit EEPROM dedicated to application data
Onboard Controllers	
Gigabit Ethernet Controller	One i82580 Gigabit MAC/PHY with four 1000BASE-T Ethernet Interface (2 front and 2 rear)
System CPLD	One CPLD Board controller for power sequencing, reset handling, monitoring, failure detection, VME I2C communication. Provides configuration/status registers on LPC interface
SIO	SIO1028 provides two serial lines
VME	ALMA2f VME controller with 2eSST
Onboard Interfaces	
CPU Debug Interface	XDP port for CPU extended debug port connection (only available on a debug connector and need additional test board for XDP access)

1.3 Environmental Specifications

Table 7: Environmental Specifications

	SA STANDARD COMMERCIAL			WA EXTENDED TEMPERATURE			RC RUGGED CONDUCTION-COOLED
Conformal Coating	Optional			Standard			Standard
Cooling Method	Convection			Convection			Conduction
Operating Temperature	0° to +55°C			-20° to +65°C			-40° to +85°C
Storage Temperature	-40° to +85°C			-45° to +100°C			-50° to +100°C
Vibration Sine (Operating)	20-500 Hz - 2g Acceleration / Frequency Range			20-500 Hz - 2g Acceleration / Frequency Range			22-2,000 Hz - 5g Acceleration / Frequency Range
Random	f (Hz)	10	40	100	200	2000	5Hz to 100Hz +3dB/octave 100Hz to 1000Hz 0.1g²/Hz 1000Hz to 2000Hz - 6dB/octave
	PSD (g2/Hz)	0.01	0.01	0.0007	0.0007	0.00005	
Shock (Operating)	20g/11 ms Peak Accel./ Shock Duration Half Sine			20g/11 ms Peak Accel./ Shock Duration Half Sine			40g/20 ms Peak Accel./ Shock Duration Half Sine
Altitude (Operating)	-1,500 to 60,000 ft			-1,500 to 60,000 ft			-1,500 to 60,000 ft
Relative Humidity	90% non-condensing			95% non-condensing			95% non-condensing

1.4 Mechanical Specifications

Table 8: Board Weight

BOARD WEIGHT	SA/WA STANDARD COMMERCIAL	RC RUGGED CONDUCTION-COOLED
VM6052	~480g	~800g
VM6054	~650g	~800g

1.5 MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

Table 9: VM6052-SAxx-xxxxx and VM6052-WAxx-xxxxx MTBF Data

	GB		AIC	NS		ARW
	25°C	40°C	40°C	25°C	40°C	55°C
MTBF (hours)	243 700	177 300	39 650	32 850	25 350	7240

Table 10: VM6054-SAxx-xxxxx and VM6054-WAxx-xxxxx MTBF Data

	GB		AIC	NS		ARW
	25°C	40°C	40°C	25°C	40°C	55°C
MTBF (hours)	218 700	167 200	22 200	40 800	31 400	5 300

Table 11: PBV36-P0-VM6-00 (RTM) MTBF Data

	GB		AIC	NS		ARW
	25°C	40°C	40°C	25°C	40°C	55°C
MTBF (hours)	1 515 750	1 085 000	199 700	277 050	195 850	30 300

Table 12: Carrier Disk SATA MTBF Data

	GB		AIC	NS		ARW
	25°C	40°C	40°C	25°C	40°C	55°C
MTBF (hours)	10 032 000	7 840 000	1 477 700	1 905 500	1 466 800	265 000

1.6 Related Publications

The following publications contain information relating to this product:

Table 13: Related Publications

PRODUCT/STANDARD	PUBLICATION	
VM605x Boards	VM605x Hardware Release Notes VM605x PBIT User's Guide VM605x AMI-BIOS User Reference Manual VM605x Release Notes Fedora16	CA.DT.B17 SD.DT.G35 SD.DT.G34 SD.DT.G11
CNET	MIL HDBK 217F, CNET RDF93 and CNET RDF2000 Reliability models	
EN	EN55022 Class A: EN61000-6-2: EN61000-3-2: EN61000-3-3: EN60950-1:	Information technology equipment - Radio disturbances characteristics - Limits and methods of measurements Electromagnetic compatibility (EMC) - Part 6-2: Generic standards – Immunity for industrial environments Electromagnetic compatibility (EMC) - Part 3-2 : limits - Limits for harmonic current emissions Electromagnetic compatibility (EMC) - Part 3-3: Limits - Limitation of voltage changes, voltage fluctuations and flicker in public low-voltage supply systems, for equipment with rated current ≤ 16 A per phase and not subject to conditional connection Information technology equipment - Safety - Part 1: General requirements
IEEE	IEEE Std 1101.2-1992 IEEE P1386-2001 IEEE P1386.1-2001	IEEE Standard for Machanical Core Specifications for Conduction Cooled Eurocards Common Mezzanine Card Family CMC Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)
Serial ATA	Serial ATA 3.0 specification, revision 3.0	
VITA	VITA 1-1994 VITA 1.1-199x VITA 35-199x VITA 31.1-200x VITA 20-2000x VITA 38-2003 VITA 47	VME64 Specification VME64 Extension Draft Specification PMC-P4 Pin Out Mapping to VME-P0 and VME64x-P2 Draft Standard Gigabit Ethernet on VME64x Backplane Draft Standard Conduction Cooled PCI mezzanine Card (CCPMC) System Management on VME Environmental, Design and Construction, Safety, and Quality for Plug-In Units
Underwriters Laboratories	UL94-V0	Standard Physical and environmental Mayers for PCI Mezzanine Cards (PMC)
DisplayPort	DisplayPort V1.1a standard	

2 / Installation

The VM605x has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

2.1 Safety Requirements

The following safety precautions must be observed when installing or operating the VM605x. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Special care shall be taken while handling the board: the heat sink can get very hot during operation. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

This board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector pins or traces.
- we strongly recommend our customers to work in an environment equipped with anti-static workbenches with professional discharging equipments.

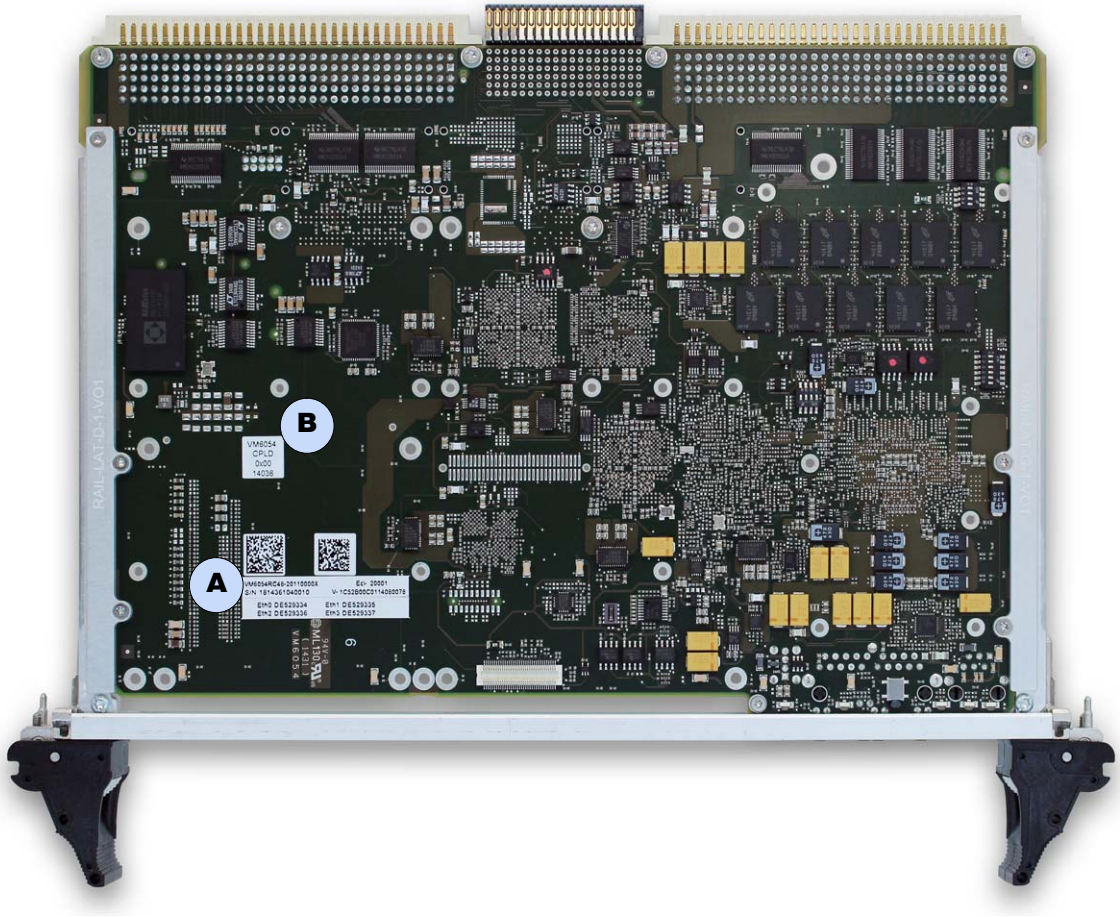
2.2 Board Identification

The VM605x boards are identified by labels fitted to the bottom side of the board.

Figure 10: VM605x Identification (Bottom Side)

A "Identification" label: Order Code, Serial Number, Variant, E.C. Level, Ethernet MAC addresses

B CPLD Label



The E.C. Level format is “xxxxxLy” where:

- The five digits “xxxxx” indicate the board E.C. Level (PCB revision included)
- “Ly” indicates the mechanical E.C. Level:
  - Letter “L” varies with the environment class (“A” for SA, “B” for WA, “C” for RA and “D” for RC)
  - Digit “y” gives the mechanical E.C. Level

See also section “Vital Product Data” in “VM605x AMI-BIOS User Reference Manual” - SD.DT.G34 to display the VPD information stored in VM605x EEPROM.

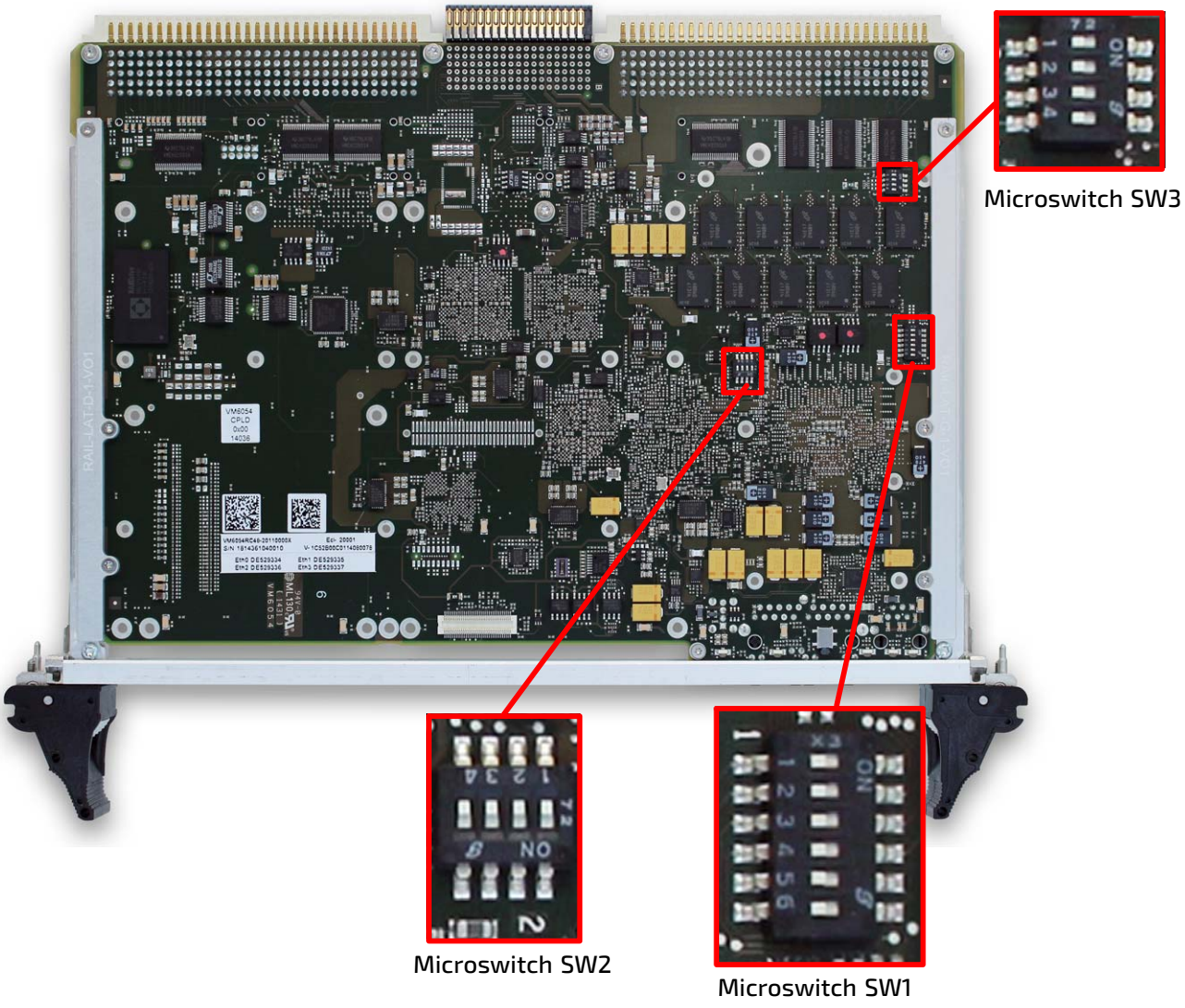
2.3 Package Content

The VM605x is packaged with several components. The packing contents of the VM605x Series may vary depending on customer requests.

- **CPU Module:**
  - Order Code: refer to section 1.2.3 “Order Code Table” :
    - Processor specifications differ depending on Order Code.
    - Heat sink assembled on the board.
    - Battery assembled on the board
  - Serial adaptation cable RJ-12 <-> DB-9 (Order Code: refer to section 1.2.3 “Order Code Table”)
- **PMCs Carrier**
  - Order Code: V2PMC2-*xx*
- **Rear Transition Module:**
  - Order Code: refer to section 1.2.3 “Order Code Table”.
- **USB Flash Disk Module:**
  - Order Code: refer to section 1.2.3 “Order Code Table”.
- **CD-ROM - Technical Documentation.**
- **Graphic Module**
  - Order Code: refer to section 1.2.3 “Order Code Table”.
- **Graphic PIM**
  - Order Code: refer to section 1.2.3 “Order Code Table”.
- **SATA Flash Disk Module**
  - Order Code: refer to section 1.2.3 “Order Code Table”.
- **SATA Disk Carrier**
  - Order Code: refer to section 1.2.3 “Order Code Table”.

2.4 Board Configuration

Figure 11: VM605x Microswitches (Bottom view)



2.4.1 Microswitches Description

Table 14: SW1 Microswitch

PORT	FUNCTION	DESCRIPTION
1	Factory Test Mode	on: Factory test mode is selected off: Normal operation
2	VPD (Vital Product Data) EEPROMs write protect	on: VPD 32Kx8 EEPROM(1), i82580 configuration EEPROMs(2), SPD EEPROM and XMC (NVMRO on XMC connector) are write protected. off: VPD 32Kx8 EEPROM, i82580 configuration EEPROMs, SPD EEPROM and XMC (NVMRO on XMC connector) are not write protected unless signal NVMRO is active (logic 1).
3	System EEPROM write protect	on: System 32Kx8 EEPROM and both SPI BIOS boot flash are write protected(2). off: System 32Kx8 EEPROM and both SPI BIOS boot flash are not write protected unless signal NVMRO is active (logic 1)
4	FRAM (Ferroelectric RAM) write protect	on: 128Kx8 User FRAM is write protected off: 128Kx8 User FRAM is not write protected unless signal NVMRO is active (logic 1).
5	Optional on board SATA NAND Flash SSD write protect	on: Optional onboard SATA NAND Flash SSD is write protected. off: Optional onboard SATA NAND Flash SSD is not write protected unless signal NVMRO is active (logic 1).
6	Debug mode for onboard power supplies and SPD	on: Debug mode active off: Normal operation

(1) The VPD EEPROM also stores the PBIT detailed results and non-volatile CPLD setup. If this EEPROM is write-protected, these data will not be updated.

(2) BIOS setup modifications will not be saved if SW1.3 is ON.

All protections are enabled when NVMRO is active, regardless the state of the switches.

Table 15: SW2 Microswitch

PORT	FUNCTION	DESCRIPTION
1	Rescue Boot Flash	on: CPU boots the BIOS from its rescue flash. off: Normal operation. CPU boots the BIOS from its non rescue flash.
2	BIOS Failsafe Boot	on: BIOS failsafe boot. off: Normal operation.
3:4	Configurable TDP	[off:off]:Set ULV CPU on VM6052 up operation at 25W / 2.2 GHz. No impact on SV CPU on VM6054. [off:on]: Set ULV CPU on VM6052 nominal operation at 17W / 1.7GHz. No impact on SV CPU on VM6054. [on:off]: Set ULV CPU on VM6052 down operation at 14W / 0.8GHz. No impact on SV CPU on VM6054. [on:on]: CPU forced in Low Frequency Mode LFM: 0.8 GHz for ULV CPU on VM6052, 30W/1.2 GHz for SV quad core CPU instead of 35W/2.1 GHz on VM6054.

Table 16: SW3 Microswitch

PORT	FUNCTION	DESCRIPTION
1:4	User	The state of each switch (ports 1 to 4) can be read from I/O port @0x80E (cPLD register 0xE), bits 3,4,5,6. on: 1 off: 0

2.5 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the VM605x in a system. Procedures for standard removal operations are found in their respective chapters.

To perform an initial installation of the VM605x in a system proceed as follows:

1. Ensure that the safety requirements indicated in Section 2.1 are observed.

CAUTION: Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the VM605x refer to Chapter 5. For the installation of VM605x specific peripheral devices and Rear I/O devices refer to the appropriate sections in current Chapter.

CAUTION: Care must be taken when applying the procedures below to ensure that neither the VM605x nor other system boards are physically damaged by the application of these procedures.

3. To install the VM605x perform the following:

3.1. Ensure that no power is applied to the system before proceeding.

CAUTION: When performing the next step, DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

3.2. Ensure that P0 connector is not damaged. Check that tongue on the bottom of P0 connector is not missing or bent. Check that female pins of P0 connector of VM605x are intact. Ensure also that the pins of J0 of the backplane are not bent.

3.3. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.

3.4. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.

3.5. Fasten the front panel retaining screws.

3.6. Connect all external interfacing cables to the board as required.

3.7. Ensure that the board and all required interfacing cables are properly secured.

The VM605x is now ready for operation. For operation of the VM605x, refer to appropriate VM605x specific software, application, and system documentation.

2.6 Standard Removal Procedure

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Section 2.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

CAUTION: Care must be taken when applying the procedures below to ensure that neither the VM605x nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.
5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.

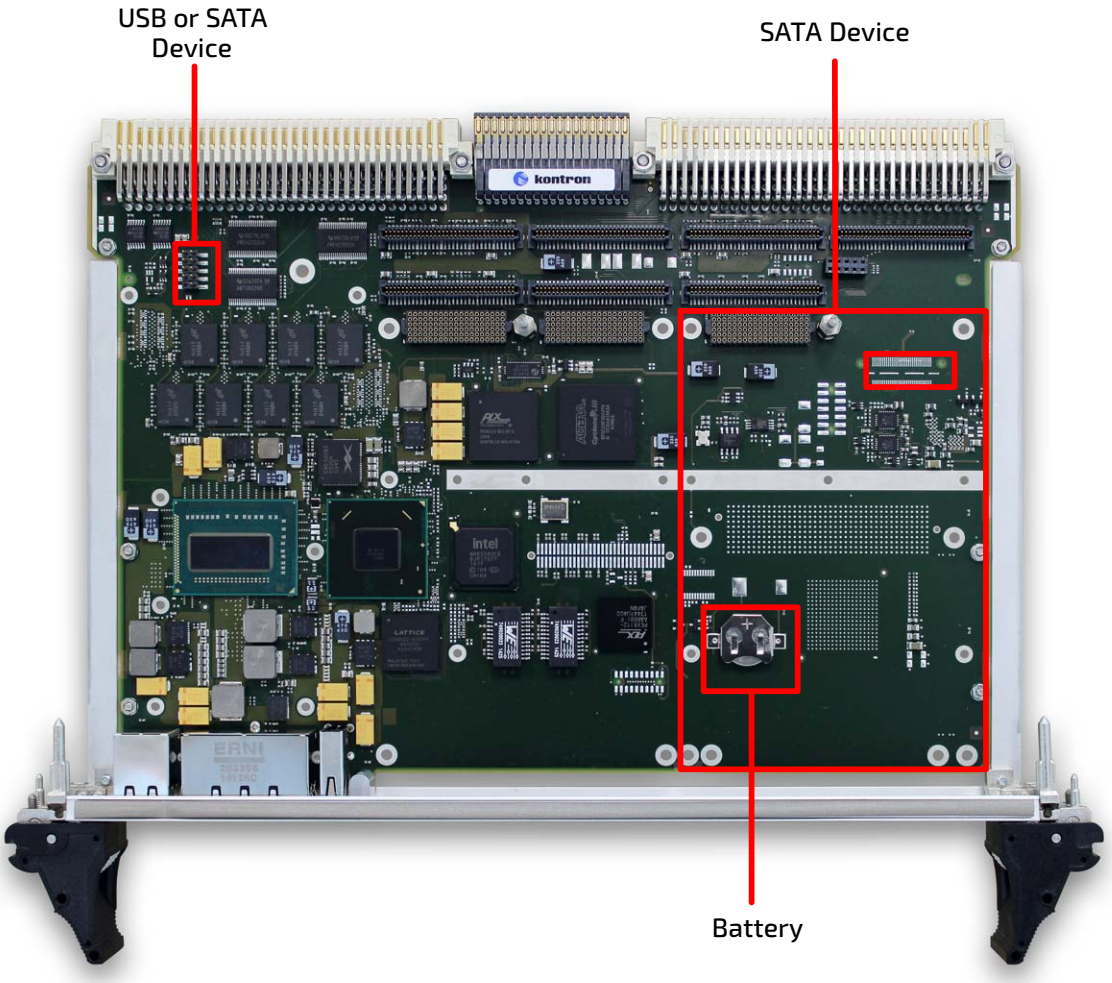
Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

7. Dispose of the board as required.

2.7 Installation of Peripheral Devices

The VM605x is designed to accommodate a variety of peripheral devices whose installation varies considerably. The following chapters provide information regarding installation aspects and not detailed procedures.

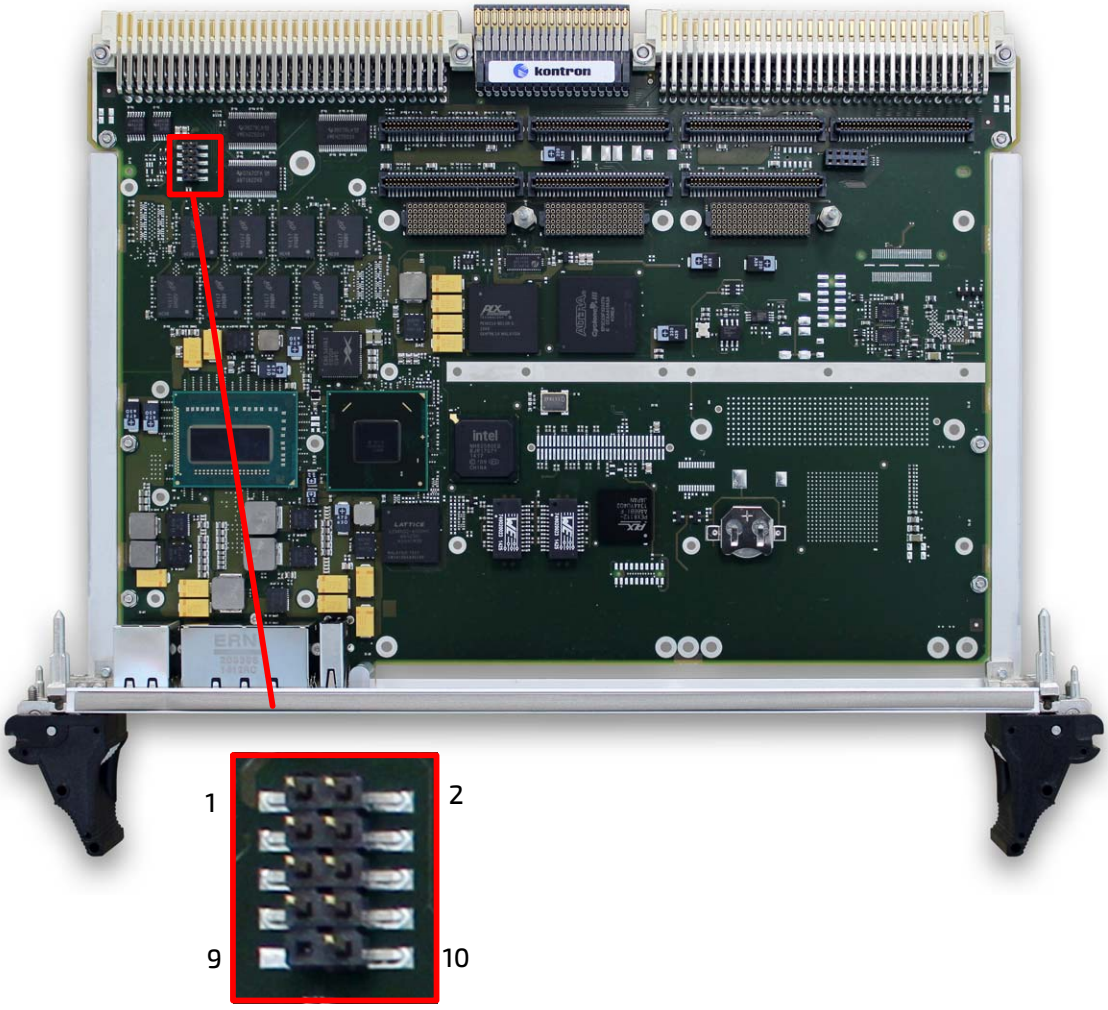
Figure 12: Onboard Devices



2.7.1 USB/SATA Flash Device Installation

The onboard USB/SATA device is used to connect an USB/SATA Flash Disk.

Figure 13: USB/SATA Mezzanine Slots Location



The USB/SATA Flash module is fixed to the board, by using on one side the USB/SATA connector, and on the other side, a standoff screwed to the VM605x board and to the USB/SATA flash module.

Order Code of the USB/SATA flash disk:

Refer to section 4.2.1 page 51.

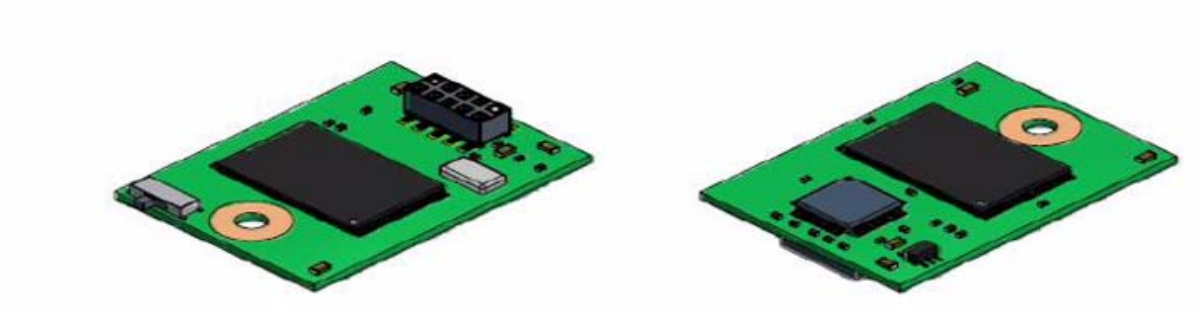
USB/SATA Mezzanine Bulk

- The maximum space reserved for USB flash disk is 36.9 mm x 26.6 mm (LxW)
- The distance between the connector and the screw hole is 27.3 mm~27.9mm
- The maximum allowable connector height is 3.68 mm

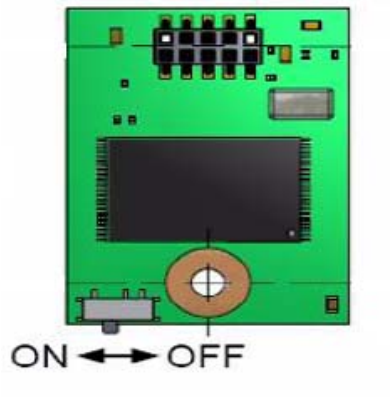
USB Flash Disk Overview

USB flash disk is a standard USB module board compatible with the USB 2.0. It is available in sizes up to 8 GB, commercial or industrial temperature range. USB flash drive feature sustained read speeds of up to 35 MB/s, write speeds up to 15 MB/s.

Figure 14: USB Flash Disk Overview



USB flash disk supports write protect feature. Write protect switch is available on module board as shown in the following figure.

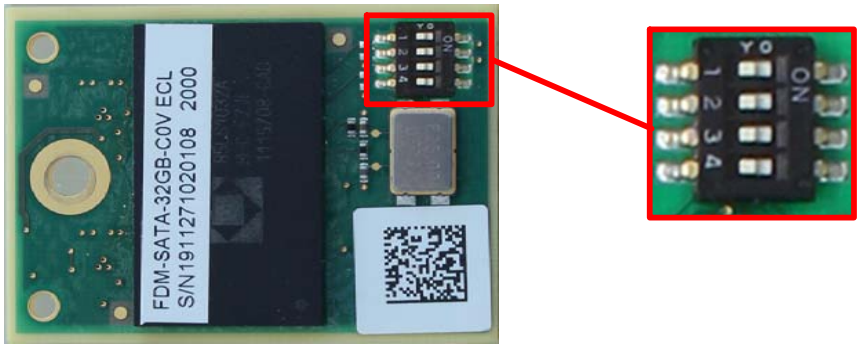


SATA Flash Disk Overview

SATA flash disk is available in sizes up to 32 GB, commercial or industrial temperature range. SATA flash drive feature sustained read speeds of up to 70 MB/s, write speeds up to 20 MB/s.

Figure 15: SATA Flash Disk Overview

- Microswitch description for SATA flash disk.



FUNCTION	DESCRIPTION
1 - Reserved	Shall be off
2 - Write Protect	on: write protect off: no write protect (default)
3 - Power down notification (not available on all models)	on: Enable early power down notification off: No early powerdown notification (default)
4 - Power down notification (not available on all models)	Shall be set identically to switch 3.

In addition, switch 2 and 3/4 shall not be all on. The same pin is used on the NAND Flash device for both functions, write protect and early power down notification. The function of this pin can be selected by software and is kept as a non-volatile setting by the NAND Flash device (only need to do it once). The hardware default (prior any selection by software) is write protect.

The early power down notification increases the robustness against loss of data when the power is removed during write operations to the NAND Flash.

2.7.2 Serial ATA Extension Module

A Serial ATA Extension Module SATA HDD or SSD may be connected to the VM605x via the onboard connector P5.

- This module must be installed only on the VM605x boards that support the SATA Kit Disk (Order code: KIT-DISK25-SATA)
- Contact Kontron for SATA onboard option.
  P5 connector is not fitted by default.

If not already done, the SATA extension module must be physically installed on the VM605x prior to installation of the VM605x in a system.

Figure 16: SATA Extension Module: front and Bottom Viewes

The SATA extension module (order code: KIT-DISK25-SATA) is made up of:

- 1 plate fitted with SATA connectors
- 4x screws CZX-M3X5-INOX
- 4x screws CZX-M2.5X5-INOX

Installation process (if not already done):

1. Replace blank front panel PMC on slot 1 by soft front panel
2. Remove key pin of PMC slot 1
3. Insert the SATA disk in the SATA connector. Example of SATA disk validated:
   - Manufacturer: Western Digital
   - Part No: SSD-D0015SI-5000
4. Fix the SATA disk to the plate using the four screws CZX-M3X5-INOX. Use medium strengh threadlocker (recommended torque of 0.4 Nm).
5. Plug the kit (plate and disk) on the VM605x board, SATA connector (P5)
6. Fix the kit to the VM605x board using the four screws CZX-M2.5X5-INOX. Use medium strengh threadlocker (recommended torque of 0.3 Nm).

2.7.3 Battery Replacement

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. The battery is used to run a time of day clock during the absence of power. Operation without the battery is possible but the date and time will not be retained in the absence of power. Alternatively, the VME RTC_BAT signal on P0 can provide a 3.3V voltage from the backplane to retain the date and time.

Make sure not to remove the battery support, this could damage the heatsink.

To replace the battery, proceed as follows:

- Turn off power.
- Use a thin plastic tool to push the battery outside the safety cache. Push from the right or left top side of the safety cache.
- Remove the battery.
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

⚠CAUTION Danger of explosion when replacing with wrong type of battery. Replace only with the same or equivalent type recommended by the manufacturer. The lithium battery type must be UL recognized.

Do not dispose of lithium batteries in general trash collection. Dispose of the battery according to the local regulations dealing with the disposal of these special materials, (e.g. to the collecting points for dispose of batteries).

Reference of the battery used on the VM605x SA and WA classes only: RENATA CR1220MFR. Refer to section 8.3 for RC class boards
The design of an electronic circuit powered by a component class battery requires the designer to consider two interacting paths that determine a battery's life: consumption of active electrochemical components and thermal wear-out.

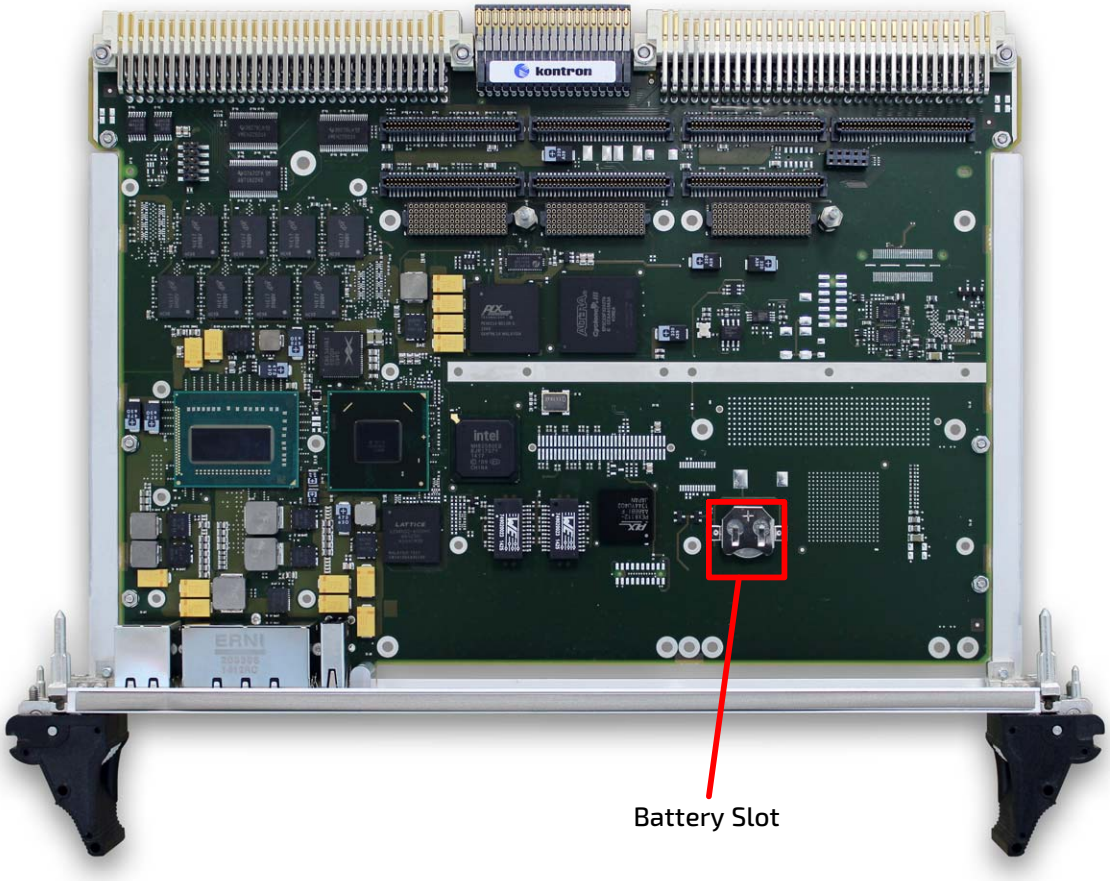
Battery Life

The RTC circuit power consumption is specified at 500 nA, giving an expected duration of higher than 9 years in the absence of external power. In case of storage temperature or operating temperature is higher than 55°C or lower than 0°C, the battery life is reduced to 6 years in worst case.

Battery Use

BR1225 batttery is used to save the date and the hour parameter of external RTC. See also chapter 3.1 “RTC, Watchdog, Timers” page 38. BIOS parameter are saved on system flash EEPROM.

Figure 17: Battery Slot



2.8 PMC Installation

PMC modules are delivered with a full kit of parts for mounting them, and the user guide for the module normally contains instructions on how to fit the module.

The installation of the PMC on the VM605x conforms to the IEEE P1386.1 standard.

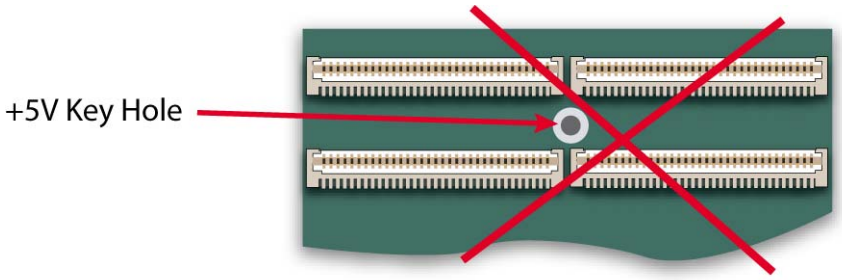
To install the XMC/PMC module, refer to Figure 18 to Figure 22 and follow the steps below:

To avoid ESD damage, wear an antistatic wrist strap to discharge static electricity while performing any part of the installation that involves touching the VM605x board or the XMC/PMC.

If you can't wear an antistatic wrist strap, touch one hand to the bare metal surface to provide grounding.

1. Place carefully the VM605x with the backplane connectors facing you on a static dissipative surface connected to a common ground by a low-resistance connection. Do not slide the board over any surface.
2. Remove the blanking plate from the appropriate XMC/PMC slot of the VM605x.
3. Check that the standoffs are attached to the XMC/PMC.
4. Install the XMC/PMC, component-side down, aligning the PCI connectors with their mating connectors on the VM605x and the XMC connector if available. Press them together so that the friction from the pins holds them together. Insert the standoff plug mounted on the VM605x into the keyhole. The module's bezel will fill the slot and provide a connection to the module.

CAUTION: PMC slot are not VIO 5V tolerant, make sure not to insert a +5V PMC on the board. Failture to observe this restriction may result in damage to the PMC or the VM605x.



5. Screw the XMC/PMC in place using the 4 mounting points, on the bottom side of the VM605x . You need a Phillips screwdriver for this stage.
6. The XMC/PMC attachment is now complete.
7. Insert the VM605x into the chassis making sure it is plugged into the backplane.

Figure 18: PMC Installation on PMC Site 1

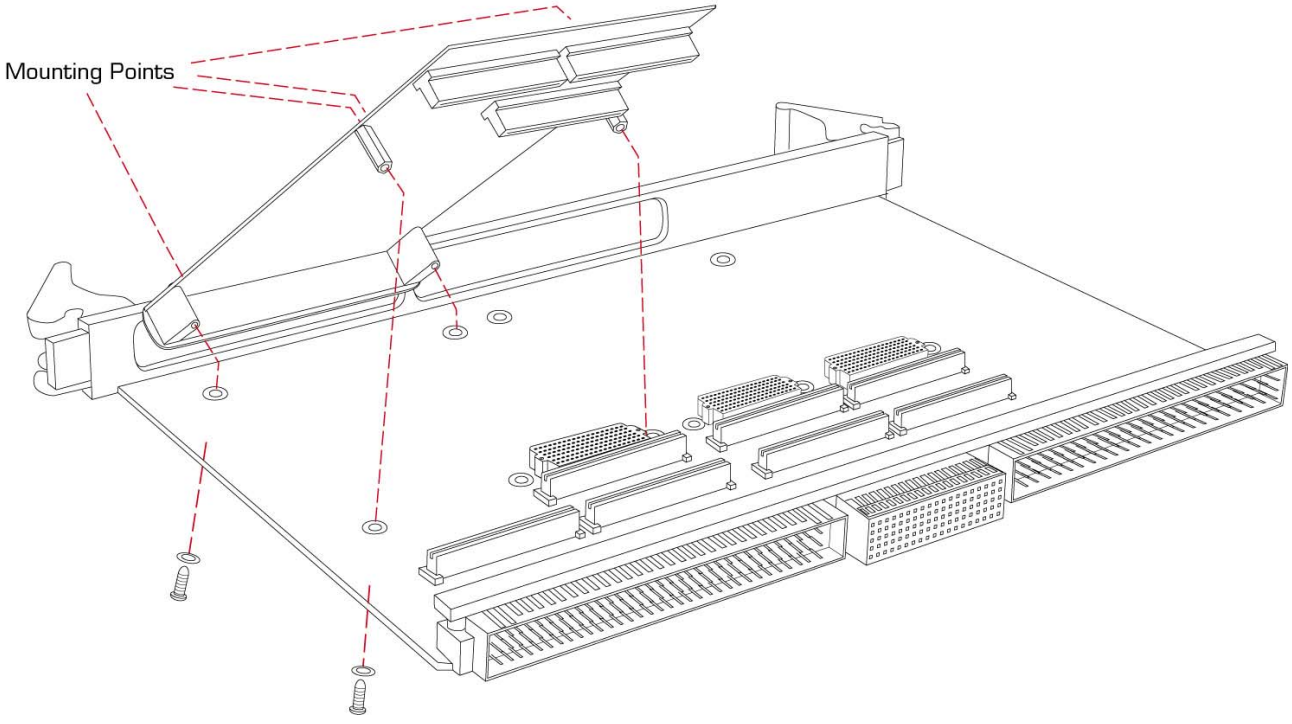
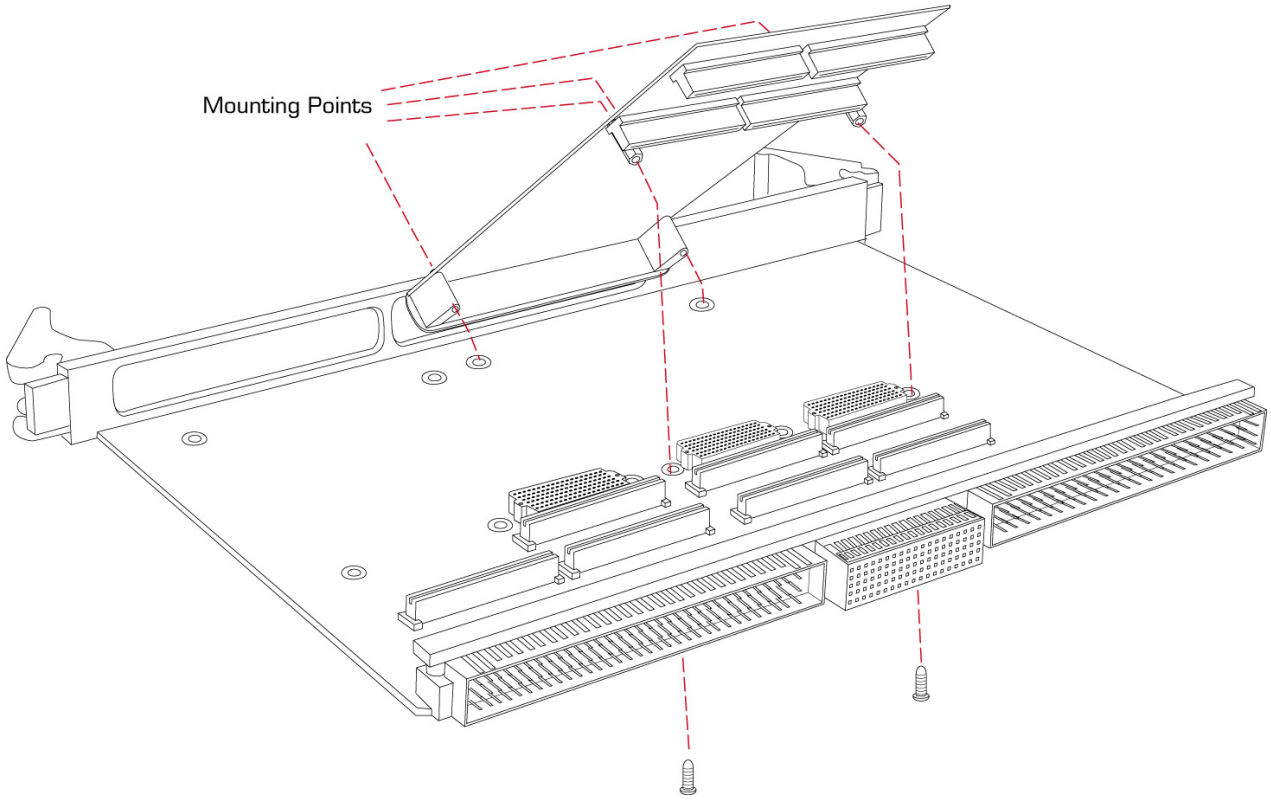


Figure 19: PMC Installation on PMC Site 2



2.9 XMC Installation

The XMC board standard is based on the PMC mechanical definition, and occupies the same board area.

The XMC board add one new connector to the connectors already on a PMC. The new connectors support high-speed differential signals for fabric communications.

Figure 20 shows a XMC fitted only with the XMC connector.

Figure 20: Example of XMC Board

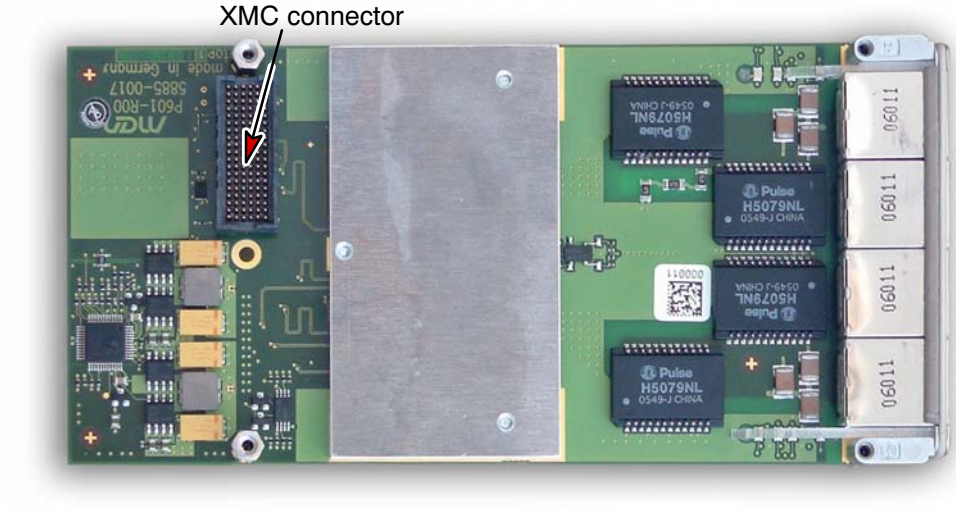


Figure 21 shows an XMC installation on the PMC Site 1.

Figure 21: XMC Installation on PMC Site 1

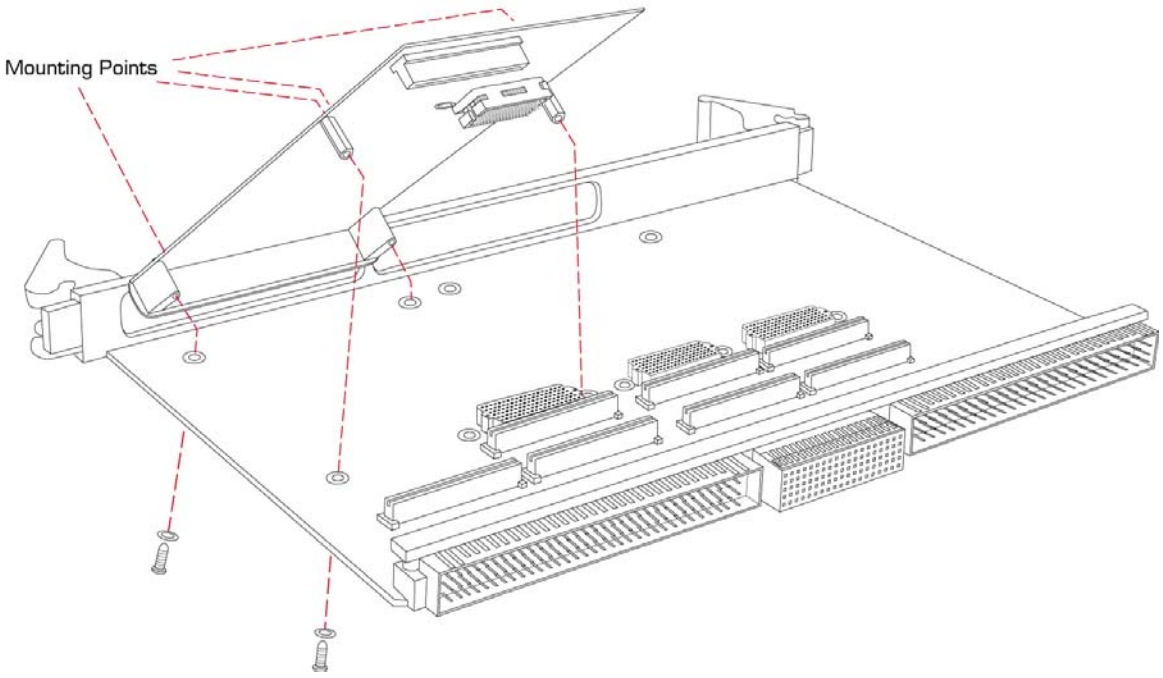
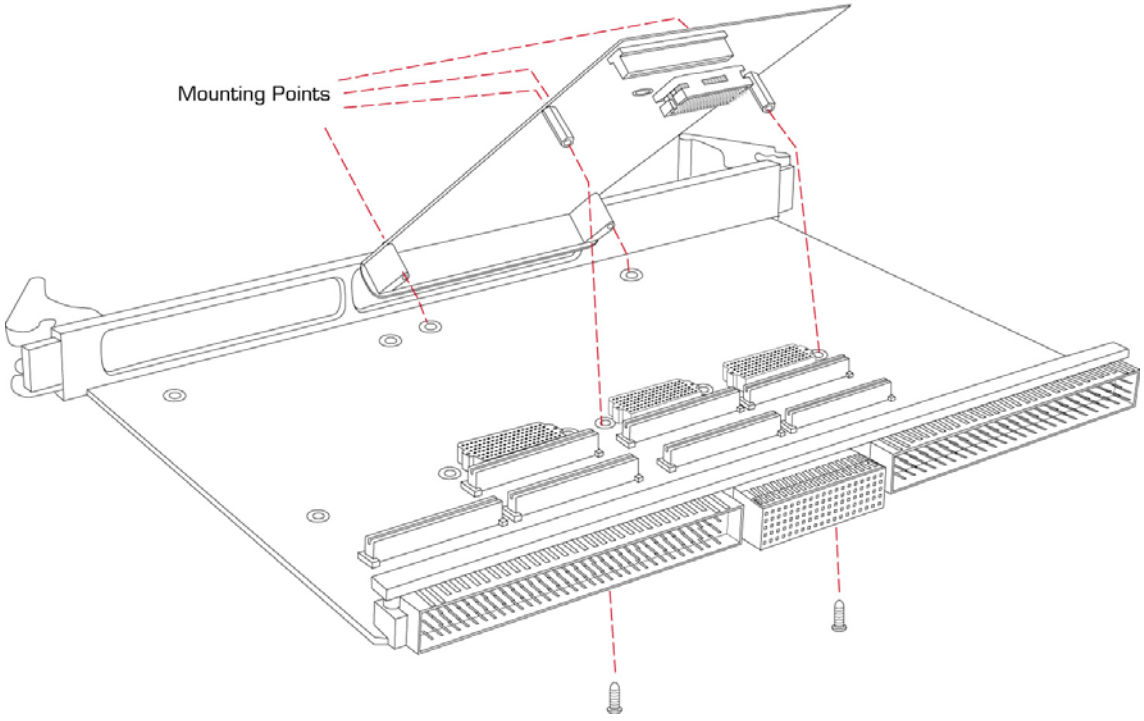


Figure 22 shows an XMC installation on the PMC Site 2.

Figure 22: XMC Installation on PMC Site 2



2.10 Graphic Module Installation

The Graphic Module is based on the PMC mechanical definition and occupies the same board area.

The Graphic Module board adds one new PMC connector. This new connector supports a graphic interface as two DisplayPort interfaces and one VGA interface.

Figure 23: Graphic Module Overview

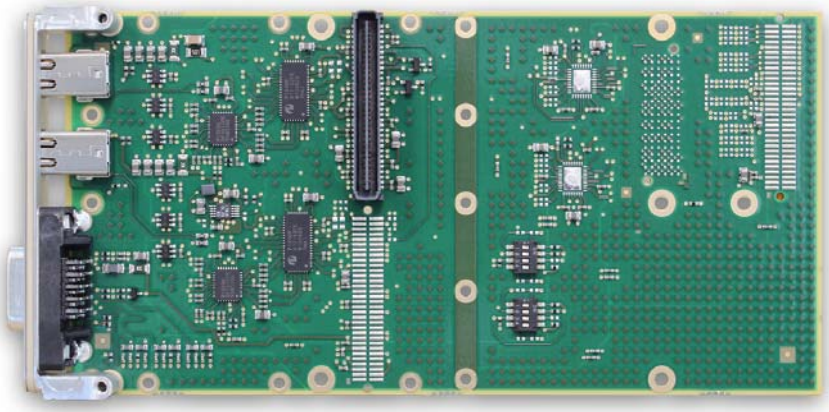


Figure 24: Graphic Module Location

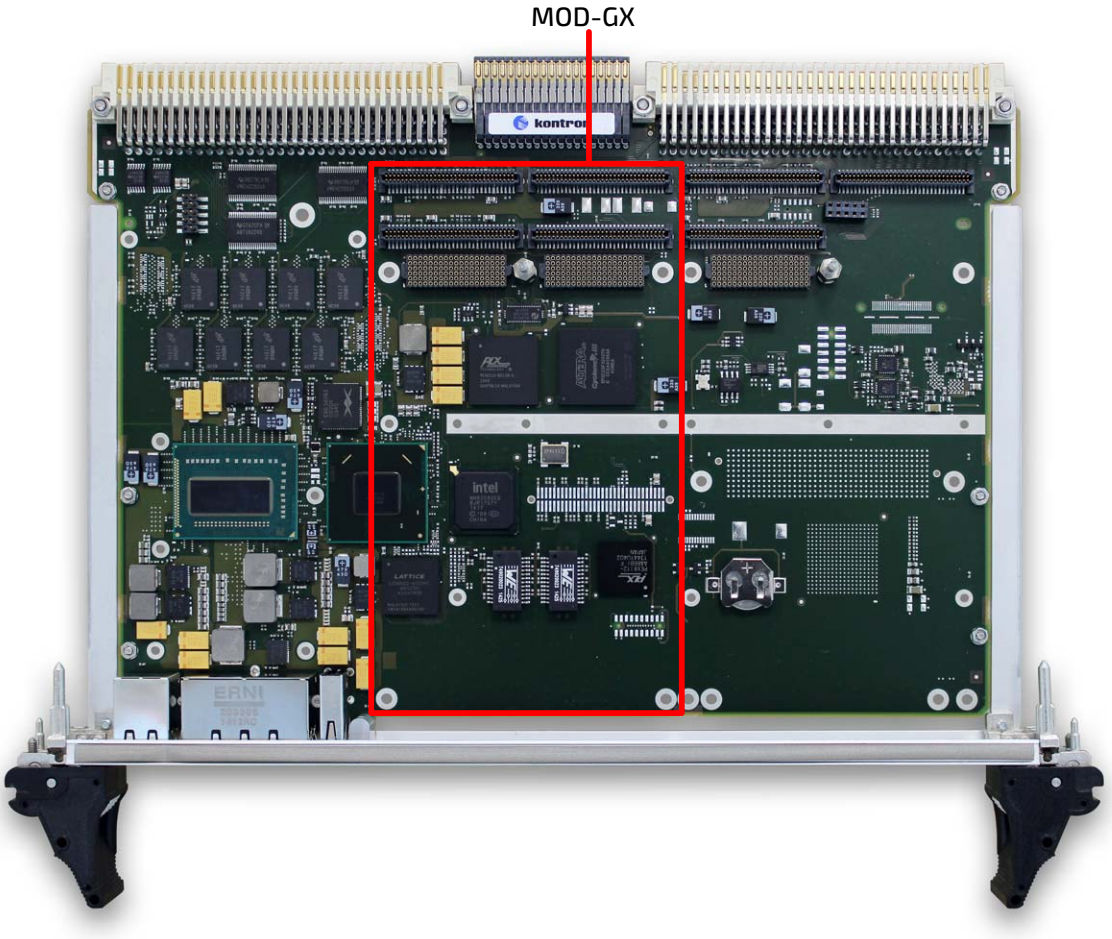
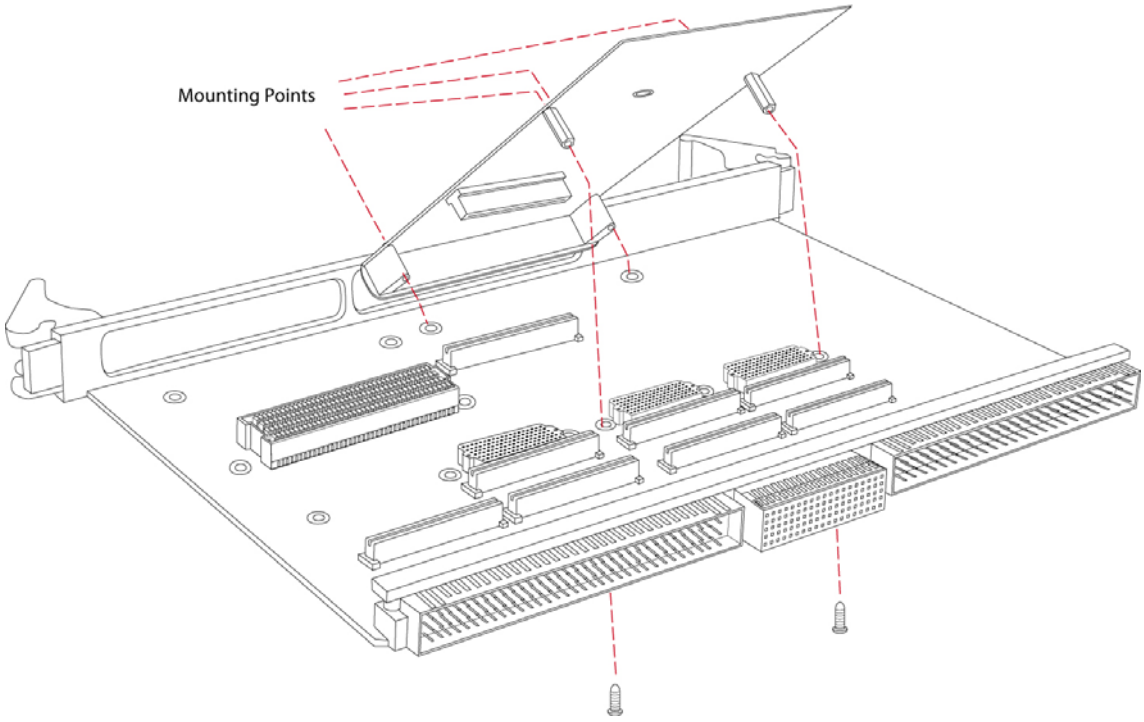


Figure 25: Graphics Module Installation



2.11 Software Installation

The installation of all onboard peripheral drivers is described in detail in the relevant Driver Kit files or Board Support Packages (BSP).

The installation of an operating system is dependent of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.

3 / Additional Board Features

3.1 RTC, Watchdog, Timers

3.1.1 Real-Time Clock (RTC)

Two Real Time Clocks (RTC) are available on the VM605x: one is embedded in the PCH while the other is a standalone, high-precision, low-power component located on the PCH SMBus (RV8564 by Micro Crystal). The latter is more precise and is powered when the board is off.

Standby power supplied to the RV8564 RTC

When the VM605x is powered off, the RTC is powered either by the onboard battery or through the 3.3V_AUX rail or the VBAT rail on the VME backplane.

To ensure data retention in the RV8564 RTC, VBAT must be set in the range [2.5V - 5.5V]. The maximum current drawn over the -40°C/+85°C temperature range is 500nA (VBAT= 3V, no I2C activity) or 550 nA (VBAT=5V, no I2C activity).

The RTC present in the Panther Point PCH chipset is never powered by the battery.

Internal PCH RTC

The PCH RTC module provides a date and time keeping device with two banks of static RAM with 128 bytes each. The BIOS programs the RTC interrupt on Legacy IRQ8 that is never shared with other interrupts. It is clocked by an external 32.768 KHz oscillator with a parabolic coefficient of 0.4 ppm/°C² and a stability of +/-20 ppm at 25°C. A 20 ppm stability is equivalent to a 10 mn/year drift.

Standalone low-power RTC RV8564

The RV8564C2/B RTC by Micro Crystal features an internal oscillator, date and time keeping module with programmable alarm, timer and interrupt functions. It has an ultra low-power consumption in time keeping mode: 250 nA, typical and 500 nA, maximum. Its stability is 20 ppm at 25°C. It is connected to the PCH SMBus

RTC management by BIOS and OS

At each startup, the BIOS retrieves the date and time information from the high-precision RV8564 RTC and copies it into the PCH RTC. This is necessary since the PCH RTC is not saved.

Any update of date and time in the BIOS settings will be done both in PCH RTC and RV8564 RTC.

Regarding the RTC management by the OS, the OS should use the high-precision RV8564 RTC driver. Failing to do so, the updates will be done only in PCH RTC and will not be saved.

If no power is applied on the RV8564 RTC, the BIOS displays the BIOS build date and time instead of the current date and time.

Century flag

For compatibility reasons, the BIOS implements the century flag for the high-precision RTC as follows:

- Century Flag C = 0 for 1900-1999 years
- Century Flag C = 1 for 2000-2099 years.

The user should check that the OS driver implements the same convention.

3.1.2 PCH Watchdog Timer

The timer is enabled by software. Once enabled it must be restarted at regular intervals. If it is not restarted the timer will expire and cause a Non-Maskable Interrupt (NMI) or reset to the local processor. Failure to trigger the Watchdog Timer in time results in an interrupt or a system reset.

3.1.3 CPLD Watchdog

In addition to the standard watchdog timer included inside the PCH, the cPLD includes a hardware watchdog timer that can be used by the operating software to monitor the normal operation of the system.

It is enabled by software, and once enabled must be restarted at regular intervals.

If not, its expiration sets off an interrupt (IRQ) to the local processor, a board reset, or a board power-cycle.

The watchdog has the following features:

- Timeout programmable from 1 to 511 periods, by steps of 2 periods
- Periods of 1s or 1mS
- Lock bit: when set, can only refresh (restart) the watchdog, but not change its settings
- 4 modes: timer, reset, interrupt, or power-cycle
- Restart counter: can manage the remaining number of resets or power-cycles done by the watchdog before giving-up.

3.2 I2C Structure

The VM605x board features four I2C busses.

- The first one is attached to the PCH Platform Hub Controller.
- The remaining i2C busses are handled by the CPLD device. The Figure 26 "I2C Diagram" shows the component attached to the different I2C buses.

I2c addresses shown below are 8-bit values with read/write bit. Shift one bit right to get 7-bit addresses.

Figure 26: I2C Diagram

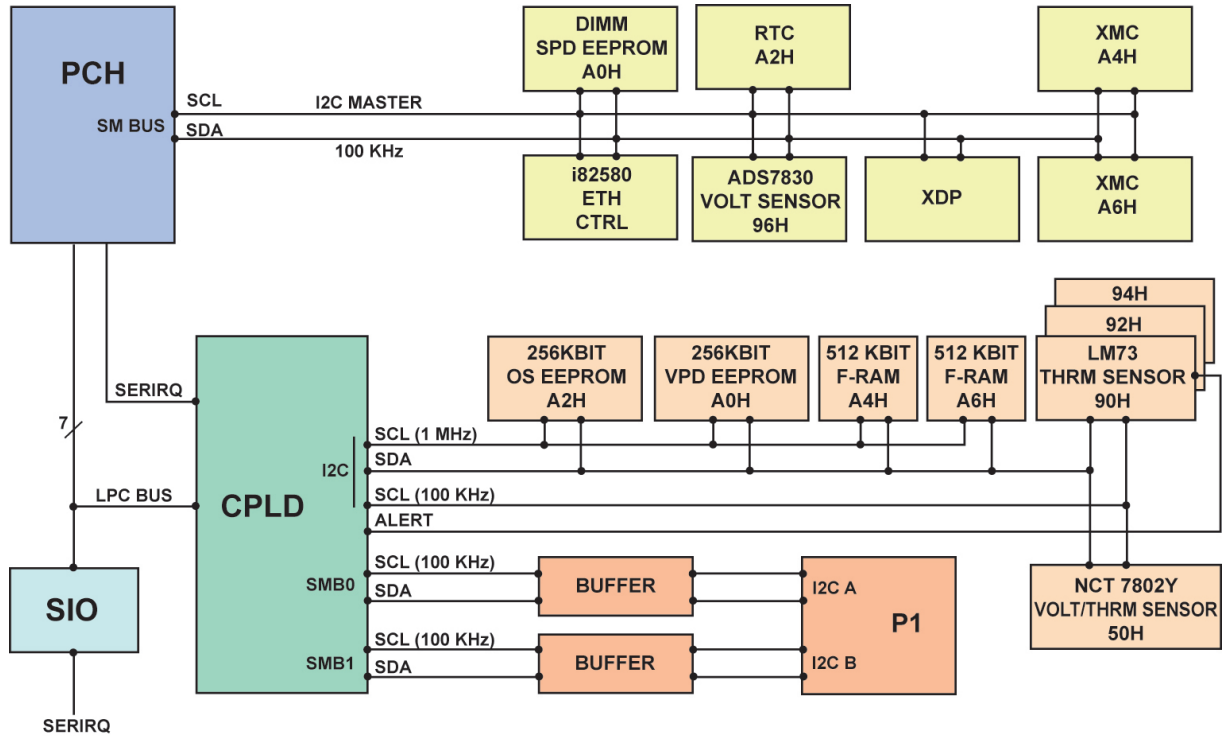


Table 17: I2C devices connected to the PLD

I2C PLD DEVICE	7-BIT I2C ADDRESS	I2C ADDRESS BYTE
NCT7802Y	0x28	0x50 / 0x51
LM73 on TOP	0x4A	0x94 / 0x95
LM73 on Top (close to CPU)	0x48	0x90 / 0x91
LM73 on BOTTOM	0x49	0x92 / 0x93
VPD EEPROM	0x50	0xA0/0xA1
SYS EEPROM	0x51	0xA2/0xA3
FRAM 128Kx8	0x52/0x53	0xA4/0xA5 / 0xA6/0xA7

CAUTION: The FRAM memory of 128Kx8 is seen as two devices of 64Kx8 on the I2C bus.

3.3 CPLD Features

The CPLD manages following features:

- Power-on/off control
- Reset control
- Local environmental control/monitoring
- LPC interface to processor
- I2C interfaces to local I2C bus, and backplane I2C busses (rear P1)
- LEDs control
- Serial lines multiplexer
- Serial VPD and user memories
- User and system GPIOs
- Internal registers that allow system management

3.3.1 VM605x I2C Interface

The VM605x implements two SMBus on backplane P1.

- **VME SMbus 0/1 master interfaces:**

  I2C bus 1 master interface is only available if the board is VME system controller.
  I2C bus 0/1 master interfaces software tools are described in Fedora Release Note.

- **VME I2C bus 0 slave interface**

  The VM605x board SMBus 0 slave address depends on VME slot ID (slot geographical address = GA):

  - VME Slot 1: slave address is 0x18 (I2C 7bits addressing)
  - VME Slot 2: slave address is 0x19 (I2C 7bits addressing)
  - VME Slot 3: slave address is 0x1A (I2C 7bits addressing) And so on.

Each board mapped at a unique I2C address implements 7 registers. The register to access is selected by sending a 1 byte "register offset" from 0x0 to 0x6, following the I2C address byte.

These registers can also be accessed from CPU through LPC bus at I/O address 0x872 to 0x878 (cPLD registers 0x72 to 0x78).

Only registers accessible from the I2C are describe in this documentation.

3.3.2 cPLD registers definition:

3.3.2.1 Overview

These registers can be accessed from CPU through LPC bus at I/O address 0x800+offset.

Registers 0x72 to 0x78 can also be accessed from I2C bus 0 (register offset 0 to 6) by an external I2C master.

OFFSET	NAME	ACCESS	REGISTER DESCRITPTION
0x72	I2C_BOARD_STATUS	RW	VME Registers facilities
0x73	I2C_BOARD_CONTROL	RW	VME Registers facilities
0x74	I2C_ERROR_STATUS	RW	VME Registers facilities
0x75	I2C_PORT80	RW	VME Registers facilities
0x76	I2C_FAILCODE	RW	VME Registers facilities
0x77	I2C_SCRATCHPAD	RW	VME Registers facilities
0x78	I2C_MISC	RW	VME Registers facilities

3.3.2.2 Detailed Description

- VME backplane I2C bus registers

I2C_BOARD_STATUS @ 0x72 Can also be accessed from I2C0 slave interface with register offset 0				
Bit#	Name	Description	Reset	Type
7	PowerStatus	**Power Status** 0: :Power Stand By 1: :Power ON	0	RO
6-5	Reset Source	**Last Reset Source** 0x00 Internal PSUs power-on 0x01 Watchdog expired 0x10 SYSRESET (from VME) 0x11 Local reset: reset switch, reset from I2C (reg 0x73), or reset by software asserting PLD_PLTRST_n	0	RO
4	Reset Status	**Reset Status Side A** 0 No PWOK or reset asserted 1 PWOK and reset unasserted	0	RO
3-0	Boot Status	**Boot Status** 0x00:RESET: default hardware value 0x01: BIOS-BOOT: written by BIOS 0x02:BIOS: written by BIOS 0x03:PBIT: written by BIOS 0x04:OS-BOOT: written by BIOS 0x05:OS-RUNNING: to be written by OS at the end of boot 0x06:COMPLETED: to be written by the final application when running 0x07:SHUTDOWN: to be written by OS when issuing a halt/shut-down 0x08:REBOOT: to be written by OS when rebooting 0x09 - 0x0B: Reserved 0x0C - 0x0F: Customer defined These bits are Read Only through I2C Slave Interface and R/W through LPC Interface The boot status is also reset at each board reset.	0	RW

I2C_BOARD_CONTROL @ 0x73 Can also be accessed from I2C0 slave interface with register offset 1				
Bit#	Name	Description	Reset	Type
7-4	Board Id	Board Identification 0100 VM6052/VM6054	0	RO
3	Check Errors	**Error Status Selection** 0 Default meaning for register @ 72 and register @73 1 Select Error Status for register @ 72 and register @73 **This bit must be left at 0**	0	RW
2	Reserved	Reserved	0	RW
1	Reset	**Reset** 0: No reset 1: Reset asserted	0	RW
0	Power_OnOff	**Power On/Off Control** 0: Power Off (StandBy) 1: Power On This bit can always be used to power on or off, and its default value is loaded when standby is applied from inverted VPD EEPROM offset 0x100 bit 1, if FACTORY mode is not enabled **WARNING** Setting this bit to 0 asserts VME SYSRESET (the board does not fully support standby because of Alma2f and its VME buffers)	*	RW

I2C_ERROR_STATUS @ 0x74 Can also be accessed from I2C0 slave interface with register offset 2				
Bit#	Name	Description	Reset	Type
7	Alert	Alert 0: no alert 1: alert pending Alert is from PLD_PECI_ALERT_n, PLD_PCH_TEMP_ALERT_n or PLD_SMBTEMP_ALERT_n See reg 0x5B for current state on theses signals. See reg 0xF bit 2 and bit 6 for interrupts,	0	RO
6	POST_Error	POST Error 0: no error 1: error This bit is set when PBIT has been run with errors (according to reg 0x2)	0	RO
5	POST_RTC	POST RTC 0: POST OK 1: POST FAILED (weak or missing battery) This bit is a copy of reg 0x3 bit 0 (POST_RTC), that is set when RTC battery islow	0	RO

I2C_ERROR_STATUS @ 0x74 Can also be accessed from I2C0 slave interface with register offset 2				
Bit#	Name	Description	Reset	Type
4-0	Error Status	Error status 0x02 ERR_3V3_PWRGD (THRM_3V3PG_PROT_n) 0x03 ERR_1V0A_PWRGD 0x04 ERR_PCH_PWRGD 0x05 ERR_1V8_PWRGD 0x06 ERR_DDR3_PWRGD 0x07 ERR_VCCIO_PWRGD 0x08 ERR_VCCSA_PWRGD 0x09 ERR_1V5_PWRGD 0x0A ERR_VCORE_PWRGD 0x0B ERR_VGFX_PWRGD 0x0C ERR_PECI_CRIT 0x0D ERR_THRM_3V3PG_PROT 0x0E ERR_THRMTRIP 0x0F ERR_CATERR 0x10 ERR_VME_UV_PWRGD 0x11 ERR_VME_OV_PWRGD 0x12 ERR_1V0_PWRGD 0x13 ERR_3V0_PWRGD 0x14 ERR_2V5_PWRGD 0x15 ERR_VINT_ALMA_PWRGD 0x16 ERR_P3V3SSD_PWRGD When a power error or unmasked fatal alert occurs, this register is updated, all internal PSUs are switched off and the error status is also reported on the front panel LEDs.	0	RO

I2C_PORT80 @ 0x75 Can also be accessed from I2C0 slave interface with register offset 3				
Bit#	Name	Description	Reset	Type
7-0	Port_80	Port 80 value The value of this register is automatically updated at each write access to port 0x80 (write snooping). It is cleared at each reset.	0	RW (LPC) RO (I2C)

I2C_FAILCODE @ 0x76 Can also be accessed from I2C0 slave interface with register offset 4				
Bit#	Name	Description	Reset	Type
7-0	Reserved	Reserved for future use	0	RW (LPC) RO (I2C)

I2C_SCRATCHPAD @ 0x77 Can also be accessed from I2C0 slave interface with register offset 5				
Bit#	Name	Description	Reset	Type
7-0	Scratchpad	**Scratchpad register** The purpose of this register is not defined	0	RW

I2C_MISC @ 0x78 Can also be accessed from I2C0 slave interface with register offset 6				
Bit#	Name	Description	Reset	Type
7	Force_rescue_BIOS	**Force rescue BIOS** 0=not forced (default) 1=forced Changing this bit will take effect at next board reset (LPC reset). See reg 0x9 bit 7 for current BIOS selected.	0	RW
6	Force_EFI_Shell	**Force stop at EFI shell** 0=not forced (default) 1=forced	0	RW
5-3	Power_CUR	**Current power profile** This field is updated by the board (BIOS/OS) according to its current power profile (power/TDP budget) 000: power profile unsupported other value: see below	000	RW (LPC) RO (I2C)
2-0	Power_REQ	**Requested power profile** This filed is expected to be set by a shelf-manager (such as CMB) or another board, and used by the board (BIOS/OS) to set its power profile. 000: uncontrolled : the board uses its onboard switches and/or BIOS settings to set a power profile 001:low TDP 010:normal TDP 011:high TDP	000	RW

3.4 Serial Lines EIA-422/485 Additional Modes

A total of 2 serial lines are available on VM605x product.

EIA-232 serial lines mode are available on front panel RJ12 and P2 connectors.

See section 4.1.1 page 47 - “Serial Connector” and section 4.3.3 page 60 - “P2 Connector” for more information on pin assignments.

EIA-232 serial lines mode is the default mode, but EIA-422/485 mode can also be set with the following mode:

MODE	RJ12 FRON PANEL CONNECTOR	P2 REAR CONNECTOR	RJ12 FRONT PIN ASSIGNMENT	P2 REAR PIN ASSIGNMENT
Default EIA-232	EIA-232: COM1	EIA-232: COM1, COM2	COM1 TXD: pin 3 COM1 RXD: pin 4 COM1 RTS: pin 1 COM1 CTS: pin 6	
EIA-422/485 on COM1	EIA-422/485: COM1	EIA-422/485: COM1 EIA-422/485: COM2	COM1 TXD: pin 3 COM1 RXD: pin 4 COM1 TXD+: pin 1 COM1 RXD+: pin 6	

3.5 GPIOs

There are up to 8 GPIOs on VM605x board and they are managed by CPLD. Refer to Fedora 16 Release Notes, section 7.7 for further details about.

- 3 GPIOs are available on P0 connector, GPIO [1-3]
- 3 GPIOs are available on P2 connector, GPIO [4-6] (option)
- 2 GPIOs are available on P2 connector on customer request, GPIO [7-8], these both GPIOs take PMC1 IO [63-64]'s place
- LVCMOS33 (0 - 3V3)
- Drive strength is 4 mA; can sink or source up to 4 mA simultaneously on all GPIOs.
- Clamping diode, but NOT 5V tolerant. So any voltage above 3.3V must be scaled by a voltage divider or limiter before being applied to a GPIO. Maximum voltage is 3.6V. Absolute maximum voltage is 3.75V (value not suitable for continuous operation).
- Weak pull-up (to 3V3SB board's internal standby power): 47K.
  This pull-up is to prevent GPIOs from floating if left unconnected. It is not configurable, but can be overridden by an additional stronger pull-down if a pull-down is required instead.
- Hysteresis: 250 mV

GPIOs are NOT 5V tolerant. Absolute maximum voltage on GPIOs is 3.75V (value not suitable for continuous operation). So any voltage above 3.6V must be reduced using a bridge made of two resistors before being applied to a GPIO.

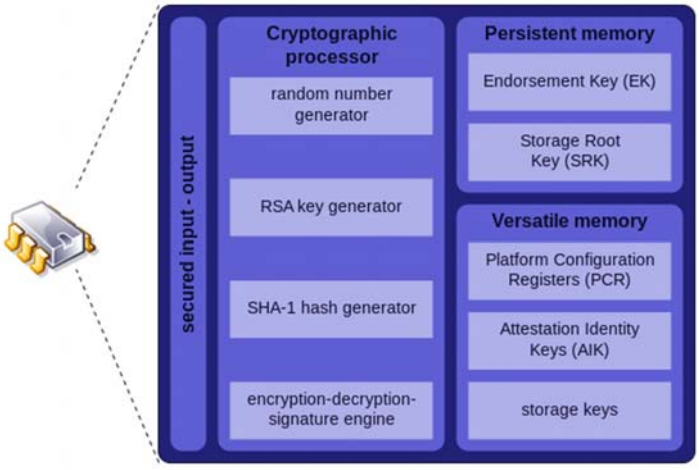
3.6 Trusted Platform Module

The VM605x can offer in option a security hardware device normalized by the Trusted Computing Group (TCG) called TPM (Trusted Platform Module). This device communicates with the CPU through a low speed interface (LPC), with a standardized API. It is active from reset and the very first bloc of instructions participates to the internal hash value calculated on each sequence of code executed during the boot.

The TPM doesn't block or restrict execution by itself (unlike secure boot) but it might be used in addition to. TPM can be viewed as:

- A device to calculate a hash value on a set of submitted data, using an algorithm designed to make it very hard to modify the input data and still produce the same hash value. For TPM1.2, the algorithms is SHA-1
- A way to store and use private keys without having to manipulate private keys outside in software & memory,
- A device to deliver local and remote attestations (based on the calculated hash value) that hardware and software running on the machine, from the reset to the end of boot, are not modified compared to a reference.

Figure 27: Trusted Platform Module



3.7 SATA NAND Flash Write Protect Mode vs Power Down Mode

The GLS85 module by Greenliant may be set through BIOS settings to either Write Protect Mode or Power Down Mode. This mode is memorised in the module and will not be changed by power-off or reset. The default mode is Write Protect.

Write Protect Mode

In this mode, the WP#/PD# pin of the GLS85 module is used as a WP# pin (active low). This pin is driven by cPLD and reflects the state of switch SW1.5.

Power Down Mode

In this mode (also called Early Power Down Mode), the WP#/PD# pin of the GLS85 module is used as a PD# pin (active low). In the event of a power failure, the cPLD will activate this signal and onboard capacitors will ensure a minimum delay of 5 ms to allow the module to perform an orderly power down (resume internal operations).

In Power Down Mode, the switch SW1.5 must be in OFF position.Setting this switch in ON position will automatically power down the module. In Power Down Mode, the Write Protect feature is not available

4 / Physical I/O

4.1 Front Panel Connectors

Figure 28: Location of the Front Panel Connectors

4.1.1 Serial Connector - COM

The VM605x integrates two serial communications ports, COM1 and COM2 in PC parlance. COM1 and COM2 are available on rear via the P2 connector.

COM1 is also available via the front panel connector.

- COM1: EIA-232/485 (simplified RX/TX) port on RJ-12 front panel connector or on the rear P2 connector
- COM2: EIA-232/485 port on the rear P2 connector

Each serial port is configurable via the BIOS setup and CPLD as EIA-232 or EIA-422 or EIA-485. Each port operates in full duplex mode or in half duplex mode. Fast slew rate is the default mode in EIA-485 mode.

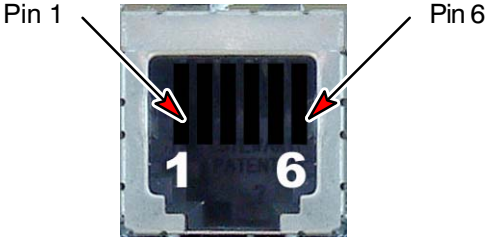
The signaling level of EIA-485 is compatible with EIA-422, so full duplex EIA-485 may also be used for point-to-point communications with an EIA-422 serial port. When port is operating in EIA-485 mode software may configure the termination for V.35, V11 or unterminated using CPLD

In EIA-232 mode the port is always unterminated register.

Table 18: Serial Connector Pin Assignment

PIN	SIGNAL
1	RTS/TXD+
2	Shell
3	TXD/TXD-
4	RXD/RXD-
5	GND
6	CTS/RXD+

Figure 29: Serial Connector



A serial line should only be used via one connector at the same time, either the Serial front panel connector or the P2 connector.

Table 19: Serial Connector Signal Description

MNEMONIC	DESCRIPTION
CTS/RXD+	EIA-232 Clear-To-Send / EIA-485 Receive Data
RTS/TXD+	EIA-232 Ready-To-Send / EIA-485 Transmit Data
RXD/RXD-	EIA-232Receive Data / EIA-485 Receive Data
TXD/TXD-	EIA-232 Transmit Data / EIA-485 Transmit Data
GND	Ground
Shell	Chassis Ground

Serial Cable Designation

Serial cable is:

- RJ-14 (6 pin, 4 conductor) for a simple EIA-232 without handshake support.
- RJ-12 (6 pin, 6 conductor) for EIA-232 with handshaking.

  A RJ-12 to DB9/DB25 male or DB9/DB25 female adapter is available from multiple sources, such as:

  - Kontron Order Code KIT-RJ12DB9
  - Triangle Cable http://www.trianglecables.com/db9m-rj12.html

PIN CONNECTOR DB9	SIGNAL	PIN CONNECTOR RJ-12
1	N.C.	1
2	TXD	3
3	RXD	4
4	N.C.	6
5	GND	5

Rj-12 Cable

DB9 Female Adpater

4.1.2 Gigabit Ethernet Connectors

The Ethernet transmission should operate using a CAT5e cable with a maximum length of 50 m.

The Ethernet connectors are available as RJ-45 connectors with tab down. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

Table 20: Gigabit Ethernet Connectors Pin Assignment

PIN	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-		I/O	BI_DC+
5	-	-	-		I/O	BI_DC-
6	I	RX-	I	RX-	I/O	BI_DB-
7	-	-	-		I/O	BI_DD+
8	-	-	-		I/O	BI_DD-
Shell	Chassis Ground					

Figure 30: Ethernet Connector

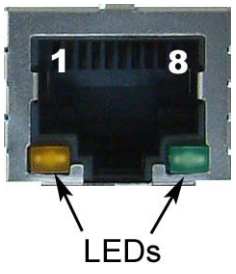


Table 21: Ethernet LEDs Status Definition

STATUS		SPEED LED YELLOW	ACT LED GREEN
Ethernet Link is not established		OFF	OFF
10 Mbps	Ethernet Link Established	OFF	ON
	Ethernet Link Activity	OFF	BLINK
100 Mbps	Ethernet Link Established	OFF	ON
	Ethernet Link Activity	OFF	BLINK
1000 Mbps	Ethernet Link Established	ON	ON
	Ethernet Link Activity	ON	BLINK

- **ACT (green)**

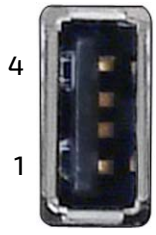
  This LED monitors network connection and activity. The LED lights up when a valid link (cable connection) has been established. The LED goes temporarily off if network packets are being sent or received through the RJ-45 port. When this LED remains off, a valid link has not been established due to a missing or a faulty cable connection.

4.1.3 USB Connector

Table 22: USB Connector Pin Assignment

PIN	SIGNAL	FUNCTION	I/O
1	VCC (+5V Protected)	VCC	--
2	USB_D-	Differential USB-	I/O
3	USB_D+	Differential USB+	I/O
4	GND	GND	--

Figure 31: USB Connector



USB

4.2 Onboard Storage Connectors

Figure 32: Connector Layout (Top View)

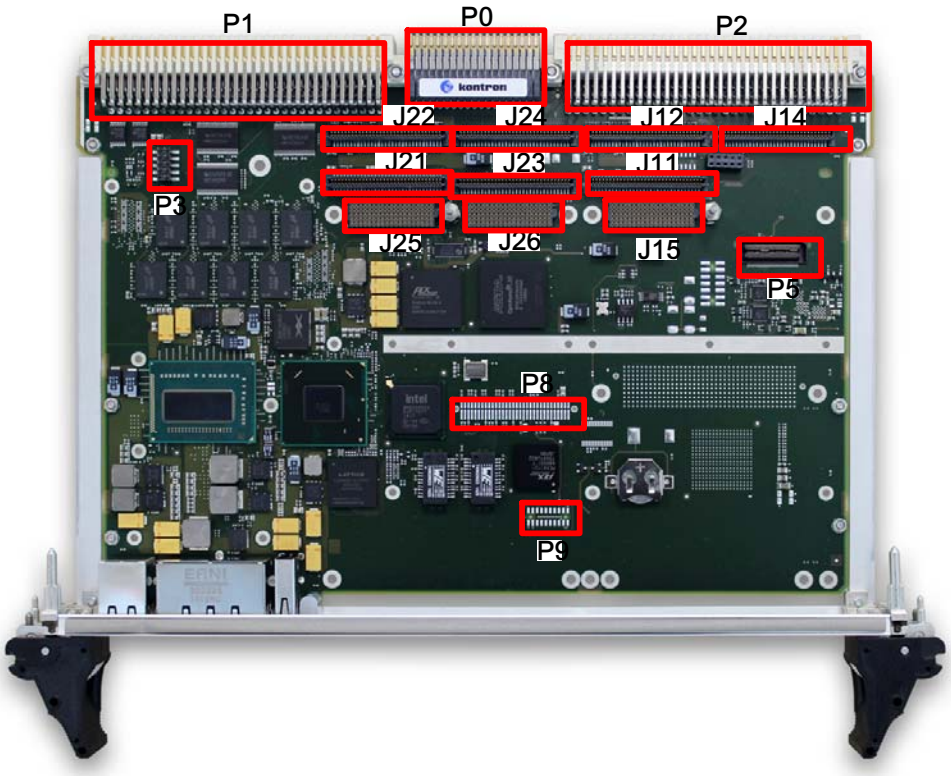
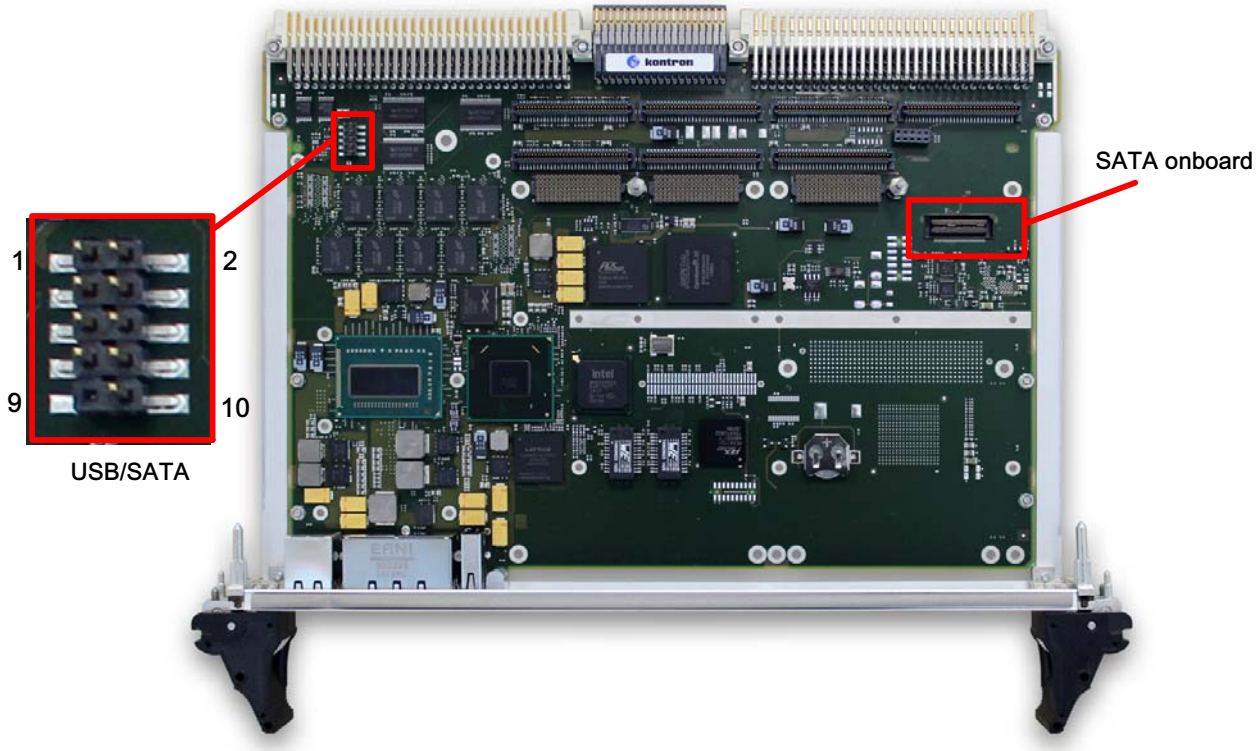


Figure 33: Onboard Storage Connector



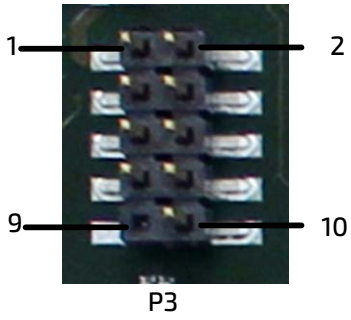
4.2.1 Onboard USB/SATA Mezzanine

The onboard USB/SATA slot device (P3 connector) is used to connect an USB flash disk module or a SATA flash disk module. The following figure and table provide pinout information for the onboard USB/SATA connector P3:

Table 23: USB/SATA onboard P3 Pinout

PIN	SIGNAL	FUNCTION	I/O
1	USB_PWR	VCC	--
2	SATA RX+	Diff Receive+	I
3	USB_D-	Differential USB-	I/O
4	SATA RX-	Diff Receive-	I
5	USB_D+	Differential USB+	I/O
6	GND	GND	--
7	GND	GND	--
8	SATA TX+	Diff Transmitt+	O
9	N.C.	Key Pin	--
10	SATA TX-	Diff Transmitt-	O

Figure 34: USB/SATA onboard Connector



The USB/SATA Flash module is fixed to the board, by using on one side the P3 connector, and on the other side, a standoff screwed to the VM605x board and to the USB/SATA Flash module.

Order Code for the USB flash disk:

FDM-USB-*x*GB-2MM-IO

FDM-USB-*x*GB-2MM-IV: industrial version with conformal coating (*x* GB)

Order Code for the SATA flash disk:

FDM-SATA-*x*GB-CO

FDM-SATA-*x*GB-IO

FDM-SATA-*x*GB-COV

FDM-SATA-*x*GB-IOV

- Contact Kontron for available capacity.
- Due to the specific dynamics of the COTS FLASH mezzanine storage market, Kontron VM605x EC level marking does not change whenever an equivalent FLASH mezzanine model is replaced by a more recent version available on the market. Kontron makes sure the new model will offer same or higher quantity of storage.
- For other aspects such as performance/wear leveling/lifetime, that depend heavily on the mission profile, FLASH users are encouraged to use application specific means to verify that the storage device meets the application needs along its life time or use device unique ID and low level health data information or mechanism (such as SMART) to monitor their installed base. Kontron can also offer specific 'frozen BOM" services for customers willing to guarantee their installed base homogeneity across deliveries and time.

4.2.2 SATA Interface

The onboard SATA device (P5 connector) is used to connect a SATA HDD. The following table provides pinout information for the onboard SATA connector P5:

Table 24: SATA onboard P5 Pinout

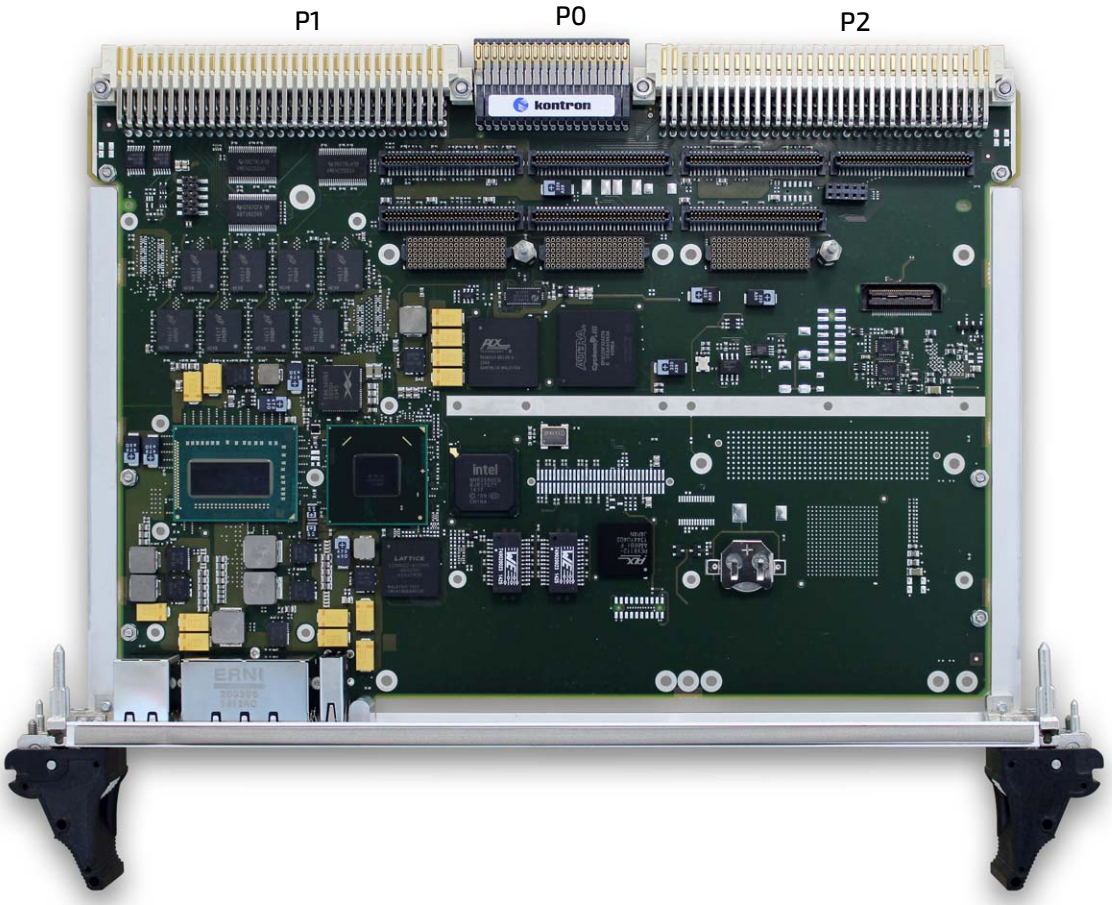
PIN	SIGNAL	FUNCTION	I/O
GND1 ... GND4	GND	Ground Signal	--
1	GND	Ground Signal	--
2 .. 6	N.C.	Not Connected	--
7	GND	Ground Signal	--
8 .. 12	N.C.	Not Connected	--
13	GND	Ground Signal	--
14	N.C.	Not Connected	--
15	SATA2 RX-	Differential Receive -	|
16	GND	Ground Signal	--
17	SATA2 RX+	Differential Receive +	|
18	+5V		--
19	GND	Ground Signal	--
20	+5V		--
21	SATA2 TX+	Differential Transmit +	O
22	+5V		--
23	SATA2 TX-	Differential Transmit -	O
24 .. 25	GND	Ground Signal	--
26	+3.3V		--
27	N.C.	Not Connected	--
28	+3.3V		--
29 .. 60	N.C.	Not Connected	--

Figure 35: SATA onboard Connector

P5

4.3 Rear Connectors

Figure 36: Rear Connectors



4.3.1 P0 Connector

4.3.1.1 P0 Connector Pin Assignment

Table 25: P0 Connector Pin Assignment

PIN #	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F(2)
1(4)	PMC2 IO 39 or XMC2 IO S9(1) [DPBPWR(5)]	PMC2 IO 38 or XMC2 IO S8(1) [DPDPWR(5)]	PMC2 IO 37 or XMC IO S7(1) [DPB_CAD(5)]	PMC2 IO 36 or XMC2 IO S6(1) [DPDPWR(5)]	PMC2 IO 35 or XMC2 IO S5(1) [DPBPWR(5)]	GND
2	ETH2_DA+	ETH2_DA–	GND	ETH2_DC+	ETH2_DC–	GND
3	ETH2_DB+	ETH2_DB–	GND	ETH2_DD+	ETH2_DD–	GND
4	ETH3_DA+	ETH3_DA–	GND	ETH3_DC+	ETH3_DC–	GND
5	ETH3_DB+	ETH3_DB–	GND	ETH3_DD+	ETH3_DD–	GND
6	RESET*	USB3_PWR	NVMRO(3) or PWR-DOWN	RTC_BAT	USB2_PWR	GND
7	USB3_DA+	USB3_DA-	GND	USB2_DA+	USB2_DA-	GND
8	SATA0_TX+	SATA0_TX-	GND	SATA0_RX+	SATA0_RX–	GND
9	SATA1_TX+	SATA1_TX-	GND	SATA1_RX+	SATA1_RX–	GND
10(4)	PMC2 IO 34 or XMC2 IO S4(1) [DPD_HPD_Q(5)]	PMCA IO 33 or XMC2 IO S2(1) [DPB_HPD_Q(5)]	GPIO1 (1) or GND	GPIO2 (1) or PCIe_CLK+	GPIO3 (1) or PCIe_CLK-	GND
11(4)	PMC2 IO 58 or XMC2 IO DP1+ [DPD_LANE0_P(5)]	PMC2 IO 60 or XMC2 IO DP1- [DPD_LANE0_N(5)]	PMC2 IO 46 or XMC2 IO S1 or GND(6)	PMC2 IO 48 or XMC2 IO DP11+ [DPB_LANE0_P(5)]	PMC2 IO 50 or XMC2 IO DP11- [DPB_LANE0_N(5)]	GND
12(4)	PMC2 IO 62 or XMC2 IO DP2+ [DPD_LANE1_P(5)]	PMC2 IO 64 or XMC2 IO DP2- [DPD_LANE1_N(5)]	PMC2 IO 45 or XMC2 IO S3 or GND(6)	PMC2 IO 52 or XMC2 IO DP12+ [DPB_LANE1_P(5)]	PMC2 IO 54 or XMC2 IO DP12- [DPB_LANE1_N(5)]	GND
13(4)	PMC2 IO 61 or XMC2 IO DP3+ [DPD_LANE2_P(5)]	PMC2 IO 63 or XMC2 IO DP3- [DPD_LANE2_N(5)]	PMC2 IO 56 or XMC IO S11 or GND(6)	PMC2 IO 51 or XMC2 IO DP13+ [DPB_LANE2_P(5)]	PMC2 IO 53 or XMC2 IO DP13- [DPB_LANE2_N(5)]	GND
14(4)	PMC2 IO 57 or XMC2 IO DP4+ [DPD_LANE3_P(5)]	PMC2 IO 59 or XMC2 IO DP4- [DPD_LANE3_N(5)]	PMC2 IO 55 or XMC2 IO S13 or GND(6)	PMC2 IO 47 or XMC2 IO DP14+ [DPB_LANE3_P(5)]	PMC2 IO 49 or XMC2 IO DP14- [DPB_LANE3_N(5)]	GND
15	PEX_RXL0+	PEX_RXL0-	GND	PEX_TXL0+	PEX_TXL0-	GND
16	PEX_RXL1+ or GND(7)	PEX_RXL1- or DPC_HPD_Q(7)	GND	PEX_TXL1+ or DPC_AUX_P(7)	PEX_TXL1- or DPC_AUX_N(7)	GND
17	PEX_RXL2+ or DPC_LANE0_P(7)	PEX_RXL2- or DPC_LANE0_N(7)	GND	PEX_TXL2+ or DPC_LANE1_P(7)	PEX_TXL2- or DPC_LANE1_N(7)	GND
18	PEX_RXL3+ or DPC_LANE2_P(7)	PEX_RXL3- or DPC_LANE2_N(7)	GND	PEX_TXL3+ or DPC_LANE3_P(7)	PEX_TXL3- or DPC_LANE3_N(7)	GND
19(4)	PMC2 IO 44 or XMC2 IO S16 [DPB_AUX_P(5)]	PMC2 IO 43 or XMC2 IO S15 [DPB_AUX_N(5)]	PMC2 IO 42 or XMC2 IO S14 [DPD_CAD(5)]	PMC2 IO 41 or XMC2 IO S12 [DPD_AUX_P(5)]	PMC2 IO 40 or XMC2 IO S10 [DPD_AUX_N(5)]	GND

(1) In the column 1, 10 and 19, they may be signals or Not Connected (N.C.). The default is the signals listed. The N.C. option is made available by removing three, 0-ohm resistor packs. Please contact Kontron for more information on this topic.
(2) The F row is the metal shielded on the outside P0 connector.
(3) The default is NVMRO signal. This signal has a pull down of 2K7 Ohms on the board. This signal is active high.
(4) The default is PMC signal listed. Please contact Kontron for XMC IO availability.
(5) Display Port on P0 routing if MOD-GX-RC-00 equipped.
(6) It is possible to have this pin connected to GND. Please contact Kontron to have this pin connected to GND.
(7) Option Display Port on P0 routing

NVMRO on P0 is 3V3 signaling, this signal is not 5V tolerant.

4.3.1.2 P0 Signal Description

Table 26: P0 Signal Description

MNEMONIC	LEGEND	SIGNAL DESCRIPTION
DPy_HPD_Q		Port y DisplayPort Hot Plug Detect
DPy_LANEx_P/N		Port y DisplayPort main link lane x
DPy_AUX_P/N		Port y DisplayPort Auxilliary channel (link device management)
ETH*x* BI_DA+/-		Ethernet *x*: First pair of Transmit/Receive data.
ETH*x* BI_DB+/-		Ethernet *x*: Second pair of Transmit/Receive data.
ETH*x* BI_DC+/-		Ethernet *x*: Third pair of Transmit/Receive data.
ETH*x* BI_DD+/-		Ethernet *x*: Fourth pair of Transmit/Receive data.
GND		Ground
GPIO*x*		General Purpose I/O *x*
NVMRO		Non Volatile Memory Read Only signal
PCIe_CLK+/-		Optional PCIe clock reference for 4x PCIe on P0
PEX RXL*y*+/-		x4 PCI Express (or Serial Rapid IO) Link - Receive+/- Lane *y*
PEX TXL*y*+/-		x4 PCI Express (or Serial Rapid IO) Link - Transmit+/- Lane *y*
PMC2 IO *yy*		PMC Site #2 I/0 signal *yy*
PWR-DOWN		Power Down board signal
RESET		Board Reset Signal
RTC-BAT		External Battery source for RTC
SATA0 RX+/RX- TX+/TX-		Serial ATA *x* Receive +/-
SATA1 RX+/RX- TX+/TX-		Serial ATA *x* Transmit +/-
USB2 DA+/- USB3 DA+/-		Differential Data Pair of USB Line *x*
USB*x* PWR		USB Line *x*
XMC2 IO *yy*		XMC Site #2 differential and single IO Signal *yy*

4.3.2 P1 Connector

4.3.2.1 P1 and P2 Row B (VMEbus) Connector Pin Assignment

Table 27: P1 and P2 (Row B) Connector Pin Assignment

PIN	P1					P2
	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW B
1	N.C.	D00	BBSY*	D08	+5V	+5V
2	GND	D01	BCLR*	D09	GND	GND
3	N.C.	D02	ACFAIL*	D10	N.C.	RETRY*
4	GND	D03	BG0IN*	D11	N.C.	A24
5	N.C.	D04	BG0OUT*	D12	N.C.	A25
6	GND	D05	BG1IN*	D13	N.C.	A26
7	N.C.	D06	BG1OUT*	D14	N.C.	A27
8	GND	D07	BG2IN*	D15	N.C.	A28
9	N.C.	GND	BG2OUT*	GND	GAP* (1)	A29
10	GND	SYSCLK	BG3IN*	SYSFAIL*	GA0* (1)	A30
11	N.C.	GND	BG3OUT*	BERR*	GA1* (1)	A31
12	GND	DS1*	BR0*	SYSRESET*	+3.3V	GND
13	N.C.	DS0*	BR1*	LWORD*	GA2* (1)	+5V
14	GND	WRITE*	BR2*	AM5	+3.3V	D16
15	N.C.	GND	BR3*	A23	GA3* (1)	D17
16	GND	DTACK*	AM0	A22	+3.3V	D18
17	N.C.	GND	AM1	A21	GA4* (1)	D19
18	GND	AS*	AM2	A20	+3.3V	D20
19	N.C.	GND	AM3	A19	SMB_SCL	D21
20	GND	IACK*	GND	A18	+3.3V	D22
21	N.C.	IACKIN*	IPMB_SCL	A17	SMB_SDA	D23
22	GND	IACKOUT*	IPMB_SDA	A16	+3.3V	GND
23	N.C.	AM4	GND	A15	SMB_ALERT*	D24
24	GND	A07	IRQ7*	A14	+3.3V	D25
25	N.C.	A06	IRQ6*	A13	N.C.	D26
26	GND	A05	IRQ5*	A12	+3.3V	D27
27	N.C.	A04	IRQ4*	A11	N.C.	D28
28	GND	A03	IRQ3*	A10	+3.3V	D29
29	N.C.	A02	IRQ2*	A09	N.C.	D30
30	GND	A01	IRQ1*	A08	+3.3V	D31
31	N.C.	-12V	+5V_STANDBY	+12V	GND	GND
32	GND	+5V	+5V	+5V	+5V	+5V

* VME signals active when low.
(1) Geographical address pins, refer to section 4.3.2.2 page 57 for more information.

⚠CAUTION

Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. Only use the VM605x in VME IEEE1014x or VME64 backplanes that supply power on both P1 and P2 connectors. Failure to observe this warning may result in damage to the board.

4.3.2.2 Geographical Address Pin Assignment

The 6 geographical address pins (GA0*, GA1*, GA2*, GA3*, GA4* and GAP*) shall be tied to ground or left open (floating) on the backplane P1 connector as defined in the table below.

SLOT NUMBER	GAP* PIN	GA4* PIN	GA3* PIN	GA2* PIN	GA1* PIN	GA0* PIN
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
10	GND	Open	GND	Open	GND	Open
11	Open	Open	GND	Open	GND	GND
12	GND	Open	GND	GND	Open	Open
13	Open	Open	GND	GND	Open	GND
14	Open	Open	GND	GND	GND	Open
15	GND	Open	GND	GND	GND	GND
16	Open	GND	Open	Open	Open	Open
17	GND	GND	Open	Open	Open	GND
18	GND	GND	Open	Open	GND	Open
19	Open	GND	Open	Open	GND	GND
20	GND	GND	Open	GND	Open	Open
21	Open	GND	Open	GND	Open	GND

The device that samples the levels of the geographical address pins will read the inverted value of the slot number into which the board is plugged. When the board is powered on without being plugged into a VME/VME64 backplane the slot number will be zero with a parity error (GAP* open).

4.3.2.3 VMEbus Signal Description

The VMEbus signals occupy rows a, b and c of the P1 connector and row b of the P2 connector.

Table 28: VME Signal Description

MNEMONIC	SIGNAL DESCRIPTION
A01 to A15	Address Bus (bits 1 to 15). Address lines that are used to broadcast a short, standard or extended address.
A16 to A23	Address Bus (bits 16 to 23). Address lines that are used in conjunction with A01-A15 to broadcast a standard or extended address.
A24 to A31	Address Bus (bits 24 to 31). Address lines that are used in conjunction with A01-A23 to broadcast an extended address.
ACFAIL*	AC Failure. This signal indicates when the AC input to the power supply is no longer being provided or that the required AC input voltage levels are not being met.
AM0 to AM5	Address Modifier (bits 0 to 5). These signals are used to broadcast information such as the address size, cycle type, master identification or any combination of these.
AS*	Address Strobe. This signal indicates when a valid address has been placed on the address bus.
BBSY*	Bus Busy. This signal is driven low by the requester associated with the current bus master to indicate that its master is using the bus.
BCLR*	Bus Clear. This signal is generated by an arbiter to indicate that there is a higher priority request for the bus than the one being processed. This signal requests the current master to release the bus.
BERR*	Bus Error. This signal is generated by a slave or bus timer to tell the master that the data transfer was not completed.
BG0IN* to BG3IN*	Bus Grant (0 to 3) In. These signals are generated by the arbiter to tell the board receiving it that if it is requesting the bus on that level, then it has been granted use of the bus. Otherwise the board should pass the signal down the daisy chain. The BGxIN*/BGxOUT* signals form the bus grant daisy chain, i.e. the BGxOUT* of one board forms the BGxIN* of the next board in the daisy chain.
BG0OUT* to BG3OUT*	Bus Grant (0 to 3) Out. These signals are generated by requesters to tell the next board in the daisy chain that if it is requesting the bus on that level, then it may use the bus. Otherwise the board should pass the signal down the daisy chain.
BR0* to BR3*	Bus Request (0 to 3). A low level, generated by a requester, on one of these lines, shows that some master needs to use the bus.
D00 to D31	Data Bus (0 to 31). These signals are used to transfer data between masters and slaves, and status/ID information from interrupters to interrupt handlers.
DS0*, DS1*	Data Strobe 0, 1. These signals are used with LWORD* and A01 to show how many byte locations are being accessed (1, 2, 3 or 4). Also, during a write cycle, the falling edge of the first data strobe shows that valid data is available on the bus. On a read cycle, the rising edge of the first data strobe shows that data has been accepted from the data bus.
DTACK*	Data Transfer Acknowledge. This signal is generated by a slave. The falling edge shows that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle. The rising edge shows that the slave has released the data bus at the end of a read cycle.
GA0* to GA4* and GAP*	Geographical address pins (refer to the table in section 4.3.2.2). These pins indicate to the VME board which one of the backplane slot it currently uses (0 to 21).
GND	The DC voltage reference for the system.

Page 1 of 2

MNEMONIC	SIGNAL DESCRIPTION
IACK*	Interrupt Acknowledge. This signal is used by the interrupt handler to acknowledge an interrupt request. It is routed to the IACKIN* pin of slot 1, where it is monitored by the IACK daisy chain driver.
IACKIN*	Interrupt Acknowledge In. This signal tells the board receiving it that board can respond to the interrupt acknowledge cycle in process or pass it down the daisy chain. IACKIN*/IACKOUT* form the interrupt acknowledge daisy chain.
IACKOUT*	Interrupt Acknowledge Out. This signal is sent by a board to tell the next board in the daisy chain that it can respond to the interrupt acknowledge cycle in progress.
IPMB_SCL	Intelligent Platform Management Bus - Clock I2C
IPMB_SDA	Intelligent Platform Management Bus - Data I2C
IRQ1* to IRQ7*	Interrupt Request (1 to 7). These signals are driven low by interrupters to request an interrupt on the corresponding level.
LWORD*	Longword. This signal is used with DS0*, DS1* and A01 to select which byte location(s) within the 4-byte group are accessed during the data transfer.
N.C.	This pin is not connected.
SMB_ALERT*	System Management Bus - Alert
SMB_SCL	System Management Bus - Serial clock line from the SMBus master to SMBus slave devices.
SMB_SDA	System Management Bus - Bi-directional serial data line between the SMBus master and the SMBus slave device.
SYSCLK	System Clock. This signal provides a constant 16 MHz clock signal that is independent of any other bus timing.
SYSFAIL*	System Fail. This signal shows that a failure has occurred in the system. It can be generated by any board in the system. It is also asserted after a reset and released when the board reset self-tests are passed successfully.
SYSRESET*	System Reset. When this signal is low, it causes the system to be reset.
WRITE*	Write. This signal is generated by a master to show whether the data transfer cycle is a read or a write.
+3.3V	+3.3 Volts DC power.
+5V	+5 Volts DC power
+12V	+12 Volts DC power.
-12V	-12 Volts DC power.

4.3.3 P2 Connector

4.3.3.1 P2 Connector Pin Assignment

The VMEbus signals occupy rows a, b and c of the P1 connector and row b of the P2 connector. Refer to section 4.3.2.1 page 56 for a detailed description of the row b of the P2 connector.

Table 29: P2 Connector Pin Assignment

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D
1	PMC2 IO 02 or HDA_SDO(6)	PMC1 IO 02	+5V	PMC1 IO 01	PMC2 IO 01 or HDA_BCLK(6)
2	GND	PMC1 IO 04	GND	PMC1 IO 03	PMC2 IO 03 or GND(6)
3	PMC2 IO 05 or HDA_SDIN0(6)	PMC1 IO 06	RETRY*	PMC1 IO 05	PMC2 IO 04 or HDA_SYNC(6)
4	GND	PMC1 IO 08	V_A<24>	PMC1 IO 07	PMC2 IO 06 or GND(6)
5	PMC2 IO 08 or HDA_SDIN1(6)	PMC1 IO 10	V_A<25>	PMC1 IO 09	PMC2 IO 07 or HDA_RST#(6)
6	GND	PMC1 IO 12	V_A<26>	PMC1 IO 11	PMC2 IO 09 or HDA_DOCKEN#(6)
7	PMC2 IO 11 or HDA_SDIN3(6)	PMC1 IO 14	V_A<27>	PMC1 IO 13	PMC2 IO10 or HDA_SDIN2(6)
8	GND	PMC1 IO 16	V_A<28>	PMC1 IO 15	PMC2 IO12 or HDA_DOCKRST#(6)
9	PMC2 IO 14	PMC1 IO 18	V_A<29>	PMC1 IO 17	PMC2 IO 13
10	GND	PMC1 IO 20	V_A<30>	PMC1 IO 19	PMC2 IO 15
11	PMC2 IO 17	PMC1 IO 22	V_A<31>	PMC1 IO 21	PMC2 IO 16
12	GND	PMC1 IO 24	GND	PMC1 IO 23	PMC2 IO 18
13	PMC2 IO 20	PMC1 IO 26	+5V	PMC1 IO 25	PMC2 IO 19
14	GND	PMC1 IO 28	V_D<16>	PMC1 IO 27	PMC2 IO 21
15	PMC2 IO 23	PMC1 IO 30	V_D<17>	PMC1 IO 29	PMC2 IO 22
16	GND	PMC1 IO 32	V_D<18>	PMC1 IO 31	PMC2 IO 24
17	PMC2 IO 26	PMC1 IO 34	V_D<19>	PMC1 IO 33	PMC2 IO 25
18	GND	PMC1 IO 36	V_D<20>	PMC1 IO 35	PMC2 IO 27
19	PMC2 IO 29	PMC1 IO 38	V_D<21>	PMC1 IO 37	PMC2 IO 28
20	GND	PMC1 IO 40	V_D<22>	PMC1 IO 39	PMC2 IO 30
21	PMC2 IO 32	PMC1 IO 42	V_D<23>	PMC1 IO 41	PMC2 IO 31
22	GND	PMC1 IO 44	GND	PMC1 IO 43	S1_TX or S1_TX- (1)
23	S2_TX or S2_TX- (1)	PMC1 IO 46	V_D<24>	PMC1 IO 45	S1_RX or S1_RX- (1)
24	GND	PMC1 IO 48	V_D<25>	PMC1 IO 47	S1_RTS or S1_TX+ (2)
25	S2_RX or S2_RX-	PMC1 IO 50	V_D<26>	PMC1 IO 49	S1_CTSor S1_RX+ (2)
26	GND	PMC1 IO 52	V_D<27>	PMC1 IO 51	S1_DTRor DIR (3)
27	S2_TX+ (1)	PMC1 IO 54	V_D<28>	PMC1 IO 53	S1_DSR
28	GND	PMC1 IO 56	V_D<29>	PMC1 IO 55	S1_DCD
29	S2_RX+ (1)	PMC1 IO 58	V_D<30>	PMC1 IO 57	S2_DSR or GPIO5 (5)
30	GND	PMC1 IO 60	V_D<31>	PMC1 IO 59	S2 DCD or GPIO4 (5)

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D
31	S2_DTR or GPIO6 (5)	PMC1 IO 62	GND	PMC1 IO 61	GND
32	GND	PMC1 IO 64 or GPIO7 (4)	+5V	PMC1 IO 63 or GPIO8 (4)	+5V

* Signals active when low.

(1) The serial I/O TX and RX pins act as either single-ended signal for EIA-232 or one side differential pair forEIA-422/485.

(2) In EIA-422/485 modes, CTS and RTS act as the other side of the differental pair for Rx and Tx respectively.

(3) In EIA-485 mode, DTR acts as direction control/indicator.

(4) Extra GPIO 7 and 8 are available on P2. The default signal is PMC IO. Please contact Kontron for more information on this topic.

(5) Extra GPIO 4, 5 and 6 are available on P2. The default signal is serial line. Please contact Kontron for more information on this topic.

(6) HDA Audio routing on P2. The default signal is PMC IO. Please contact Kontron for more information on this topic.

4.3.3.2 P2 Signal Description

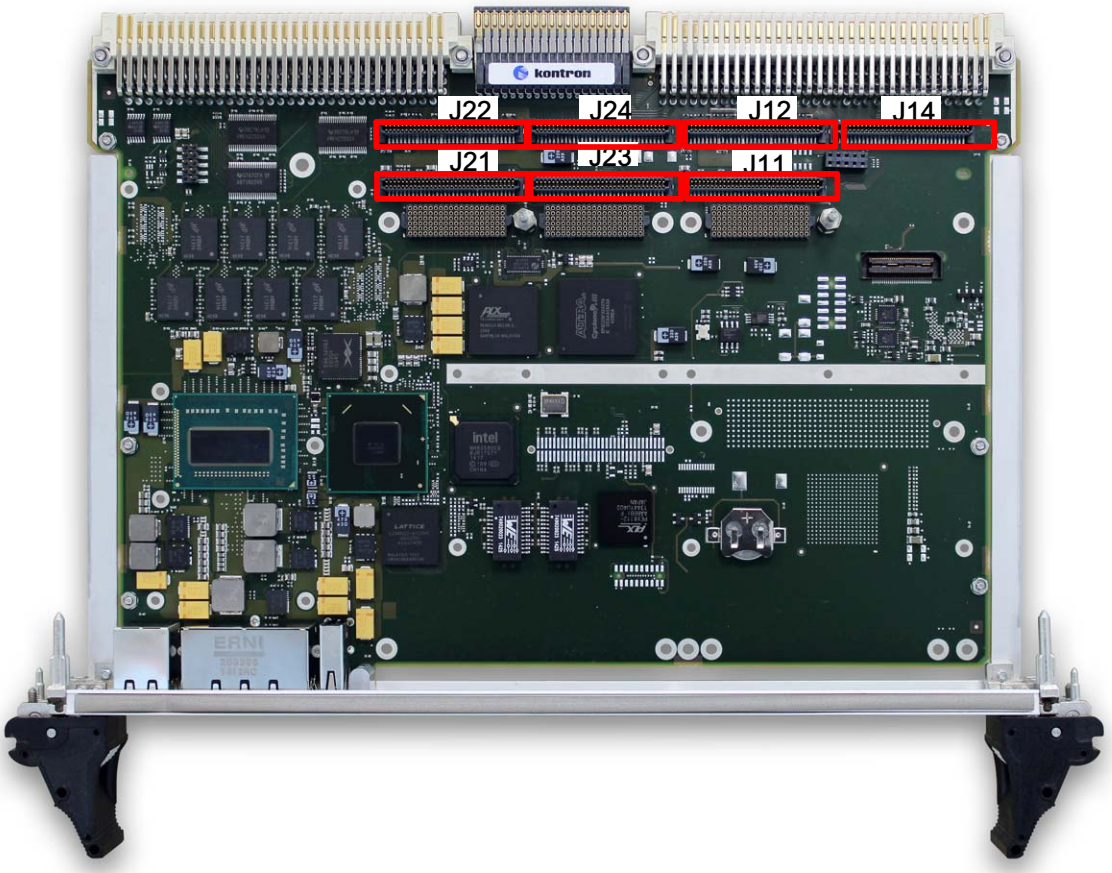
The VME signals (row b) are described in section 4.3.2.3.

Table 30: P2 Signal Description

MNEMONIC	LEGEND	SIGNAL DESCRIPTION
GND		Ground
GPIO		General Purpose I/O x
HDA_BCLK		Intel High Definition Audio Bit Clock Output: 24.000 MHz serial data clock generated by the Intel High Definition Audio controller (the PCH).
HDA_DOCKEN#		Intel High Definition Audio Dock Enable
HDA_DOCKRST		Intel High Definition Audio Dock Reset: This signal is a dedicated HDA_RST# signal for the codec(s) in the docking station.
HDA_RST#		Intel® High Definition Audio Reset: Master hardware reset to external codec(s).
HDA_SDINx		Intel High Definition Audio Serial Data In x : Serial TDM data inputs from the codecs.
HDA_SDO		Intel High Definition Audio Serial Data Out : Serial TDM data output to the codec(s).
HDA_SYNC		Intel High Definition Audio Sync: 48 kHz fixed rate sample sync to the codec(s).
PMC *x* IO yy		PMC Site *x* I/O signal *yy*
Sx_CTS		Channel EIA-232 *x* - Clear-To-Send
Sx_DCD		Channel EIA-232 x - Data Carrier Detect
Sx_DSR		Channel EIA-232 x - Data Set Ready
Sx_DTR		Channel EIA-232 x - Data Terminal Ready
Sx_RTS		Channel EIA-232 *x* - Ready-To-Send
Sx_RX		Channel EIA-232 *x* - Receive Data
Sx_TX		Channel EIA-232 *x* - TransmitData
S0_DTR		Channel EIA-232 0 - Data Terminal Ready
S0_DSR		Channel EIA-232 0 - Data Set Ready
S0_DCD		Channel EIA-232 0 - Data Carrier Detect
+5V		+5 Volts DC power

4.4 PMC Connectors

Figure 37: PMC Connectors



4.4.1 PMC J11 and J21 Connector Pin Assignments

Table 31: PMC J11 and J21 Conne4ctor Pin Assignment

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	TCK	17	REQ#	33	FRAME#	49	AD[09]
2	-12V	18	+5V	34	GND	50	+5V
3	GND	19	V(I/O) (1)	35	GND	51	GND
4	INTA#	20	AD[31]	36	IRDY#	52	C/BE0#
5	INTB#	21	AD[28]	37	DEVSEL#	53	AD[06]
6	INTC#	22	AD[27]	38	.+5V	54	AD[05]
7	BUSMODE1#	23	AD[25]	39	PCIXCAP	55	AD[04]
8	+5V	24	GND	40	LOCK#	56	GND
9	INTD#	25	GND	41	SDONE#	57	V(I/O) (1)
10	N.C.	26	C/BE3#	42	SBO#	58	AD[03]
11	GND	27	AD[22]	43	PAR	59	AD[02]
12	+3.3V_SUS	28	AD[21]	44	GND	60	AD[01]
13	CLK	29	AD[19]	45	V(I/O) (1)	61	AD[00]
14	GND	30	+5V	46	AD[15]	62	+5V
15	GND	31	V(I/O) (1)	47	AD[12]	63	GND
16	GNT#	32	AD[17]	48	AD[11]	64	REQ64#

(1) V(I/O) is 3.3V only.

PCI signals active when low.

4.4.2 PMC J12 and J22 Connector Pin Assignments

Table 32: PMC J12 and J22 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	+12V	17	PME#	33	GND	49	AD[08]
2	TRST	18	GND	34	IDSEL B (1)	50	+3.3V
3	TMS	19	AD[30]	35	TRDY#	51	AD[07]
4	TDO	20	AD[29]	36	+3.3V	52	REQ B# (1)
5	TDI	21	GND	37	GND	53	+3.3V
6	GND	22	AD[26]	38	STOP#	54	GNT B# (1)
7	GND	23	AD[24]	39	PERR#	55	PMC-RSVD
8	N.C.	24	+3.3V	40	GND	56	GND
9	N.C.	25	IDSEL	41	+3.3V	57	PMC-RSVD
10	N.C.	26	AD[23]	42	SERR#	58	EREADY
11	BUSMODE2#	27	+3.3V	43	C/BE1#	59	GND
12	+3.3V	28	AD[20]	44	GND	60	N.C.
13	RST#	29	AD[18]	45	AD[14]	61	ACK64#
14	GND	30	GND	46	AD[13]	62	+3.3V
15	+3.3V	31	AD[16]	47	M66EN	63	GND
16	BUSMODE4#	32	C/BE2#	48	AD[10]	64	N.C.

(1) IDSEL B, REQ B# and GNT B# are provided for use by dual-function PMC modules or processor-PMC modules

PCI signals active when low.

4.4.3 PMC J23 Connector Pin Assignments

Table 33: PMC J13 and J23 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	N.C.	17	AD[59]	33	GND	49	AD[37]
2	GND	18	AD[58]	34	AD[48]	50	GND
3	GND	19	AD[57]	35	AD[47]	51	GND
4	C/BE7#	20	GND	36	AD[46]	52	AD[36]
5	C/BE6#	21	V(I/O) (1)	37	AD[45]	53	AD[35]
6	C/BE5#	22	AD[56]	38	GND	54	AD[34]
7	C/BE4#	23	AD[55]	39	V(I/O) (1)	55	AD[33]
8	GND	24	AD[54]	40	AD[44]	56	GND
9	V(I/O) (1)	25	AD[53]	41	AD[43]	57	V(I/O)
10	PAR64	26	GND	42	AD[42]	58	AD[32]
11	AD[63]	27	GND	43	AD[41]	59	RSVD
12	AD[62]	28	AD[52]	44	GND	60	RSVD
13	AD[61]	29	AD[51]	45	GND	61	RSVD
14	GND	30	AD[50]	46	AD[40]	62	GND
15	GND	31	AD[49]	47	AD[39]	63	GND
16	AD[60]	32	GND	48	AD[38]	64	N.C.

(1) V(I/O) is 3.3V only

PCI signals active when low.

4.4.4 J14 and J24 Connector Pin Assignment

Table 34: J24 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	PMC IO 01	17	PMC IO 17	33	PMC IO 31	49	PMC IO 49
2	PMC IO 02	18	PMC IO 18	34	PMC IO 34	50	PMC IO 50
3	PMC IO 03	19	PMC IO 19	35	PMC IO 35	51	PMC IO 51
4	PMC IO 04	20	PMC IO 20	36	PMC IO 36	52	PMC IO 52
5	PMC IO 05	21	PMC IO 21	37	PMC IO 37	53	PMC IO 53
6	PMC IO 06	22	PMC IO 22	38	PMC IO 38	54	PMC IO 54
7	PMC IO 07	23	PMC IO 23	39	PMC IO 39	55	PMC IO 55
8	PMC IO 08	24	PMC IO 24	40	PMC IO 40	56	PMC IO 56
9	PMC IO 09	25	PMC IO 25	41	PMC IO 41	57	PMC IO 57
10	PMC IO 10	26	PMC IO 26	42	PMC IO 42	58	PMC IO 58
11	PMC IO 11	27	PMC IO 27	43	PMC IO 43	59	PMC IO 59
12	PMC IO 12	28	PMC IO 28	44	PMC IO 44	60	PMC IO 60
13	PMC IO 13	29	PMC IO 29	45	PMC IO 45	61	PMC IO 61
14	PMC IO 14	30	PMC IO 30	46	PMC IO 46	62	PMC IO 62
15	PMC IO 15	31	PMC IO 31	47	PMC IO 47	63	PMC IO 63
16	PMC IO 16	32	PMC IO 32	48	PMC IO 48	64	PMC IO 64

4.4.5 PMC Signal Description

Table 35: PMC Signal Description

MNEMONIC	SIGNAL DESCRIPTION
AD[00] to AD[63]	Address/Data bits. Multiplexed address and data bus. AD32 to AD63 are specifics to 64-bit bus extension.
ACK64#	Acknowledge 64-bit Transfer. Driven low by the device to indicate that the target is willing to transfer data using 64 bits.
BUSMODE1#	Bus Mode 1. Driven low by a PMC module to indicate that it supports the current bus mode
BUSMODE2#	Bus Mode 2. Driven low by a PMC module to indicate that it supports the current bus mode
BUSMODE4#	Bus Mode 4. Driven low by a PMC module to indicate that it supports the current bus mode
C/BE0# to C/BE7#	Command/Byte Enables. During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase the signals are byte enables that specify the active bytes on the bus. C/BE4# to C/BE7# are specifics to 64-bit bus extension.
CLK	Clock. Except RST*, the 64-bit PCI bus signals are synchronous to 33 or 66 MHz clock.
DEVSEL#	Device Select. Driven low by a PCI agent to signal that it has decoded its address as the target of the current access.
FRAME#	FRAME. Driven low by the current master to signal the start and duration of an access.
EREADY	EREADY. Output of non-monarch PPMCs that indicates it has completed its onboard initialization and can respond to PCI bus enumeration by the monarch via configuration cycles. Input to the monarch PPMC that indicates all non-monarch PPMCs have completed their onboard initialization and can respond to PCI bus enumeration by the monarch via configuration cycles.
GNT#	Grant. Driven low by the arbiter to grant PCI bus ownership to a PCI agent.
GNT B#	Grant. GNT B# is provided for use by dual-function PMC modules or processor-PMC modules.
IDSEL	Initialization Device Select. Device chip select during configuration cycles.
IDSEL B#	Initialization Device Select. IDSEL B is provided for use by dual-function PMC modules or processor-PMC modules.
INTA# to INTD#	Interrupt lines. Level-sensitive, active-low interrupt requests.
IRDY#	Initiator Ready. Driven low by the initiator to signal its ability to complete the current data phase.
LOCK#	LOCK. Driven low to indicate an atomic operation that may require multiple transactions to complete.
M66EN	66 MHZ Enable. Indicates to a device if the bus segment is operating at 66 or 33 MHz. If it is high then the bus speed is 66 MHz and if it is low then the bus speed is 33 MHz.
N.C.	This pin is not connected.
PAR	Parity. Parity protection bit for AD0 to AD31 and C/BE0# to C/BE3#.
PAR64	Parity Upper DWORD. Parity protection bit for AD32 to AD63 and C/BE4# to C/BE7#.
PERR#	Parity Error. Driven low by a PCI agent to signal a parity error.
PMC IO 01 to PMC IO 64	64-bit PCI bus PMC 64 signals. Used to transmit I/O signals from PCI 64 PMC connector (J14) to P2 connector.
PMC-RSVD	Reserved. Do not connect this pin.

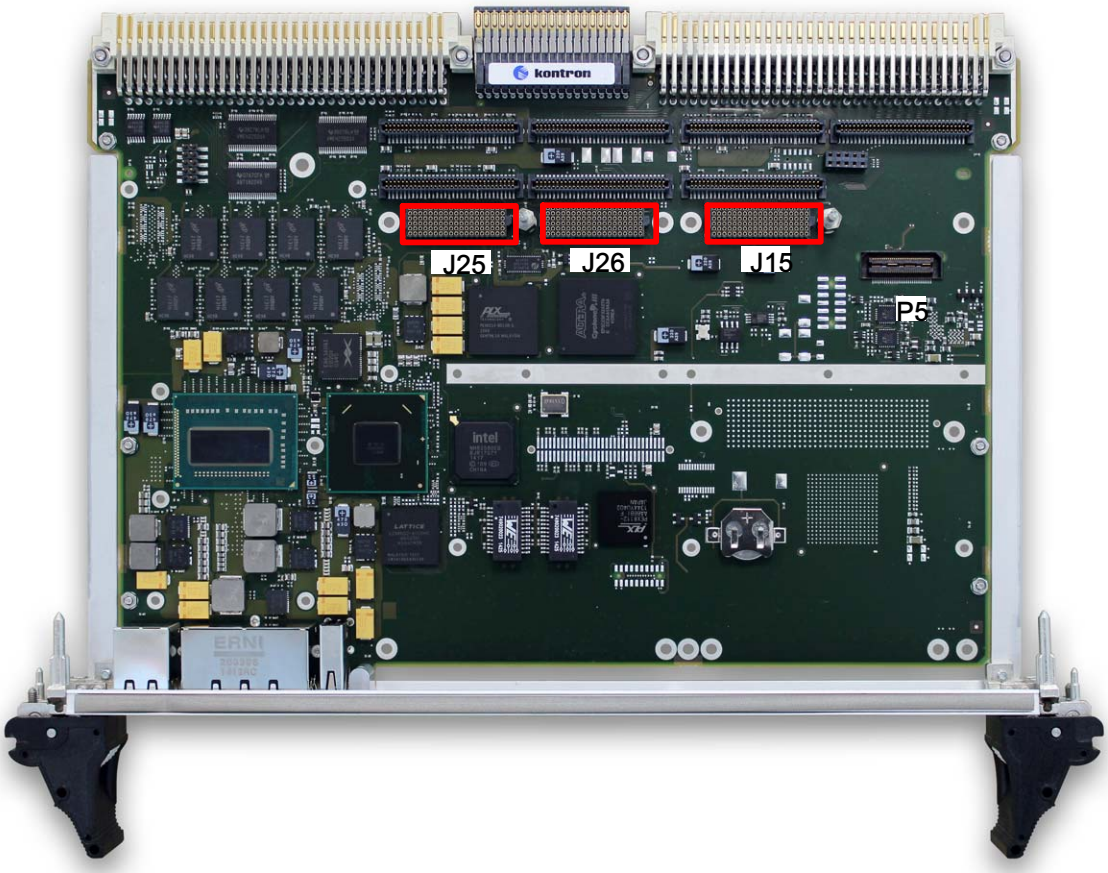
Table 1 of 2

MNEMONIC	SIGNAL DESCRIPTION
PME	
REQ#	Request. Driven low by a PCI agent to request ownership of the PCI bus.
REQ B#	Request. REQ B# is provided for use by dual-function PMC modules or processor-PMC modules.
REQ64#	Request 64-bit Transfer. Driven low by the current bus master, indicates that it desires to transfer data using 64 bits.
RST#	Reset. Driven low to reset the PCI bus.
SBO#	Snoop Backoff. Indicates a hit of a modified line asserted.
SDONE#	Snoop Done. Indicates the status of the snoop for the current access.
SERR#	System Error. Driven low by a PCI agent to signal a system error.
STOP#	STOP. Driven low by a PCI target to signal a disconnect or target-abort.
TCK	JTAG Clock.
TDI	JTAG Data In
TDO	JTAG Data Out
TMS	JTAG Mode Select
TRDY#	Target Ready. Driven low by the current target to signal its ability to complete the current data phase.
TRST	JTAG Reset.
V(I/O)	Power supply delivered by the board. On the PCI 64 PMC slots, +3.3 Volts power is supplied. +5 Volts signaling PMCs are not supported. Contact Kontron for more information.
+3.3V	+3.3 Volts DC power
+5V	+5 Volts DC power
+12V	+12 Volts DC power
-12V	-12 Volts DC power

Table 2 of 2

4.5 XMC Connectors

Figure 38: XMC Connectors



4.5.1 XMC J15 and J25 Connector Pin Assignments

Two XMC sites are provided to allow the installation of VITA 42.3, PCI-Express mezzanine cards. The signals assignments are as shown in the following table. The encoding for GA[2:0] should not conflict with other SMbus/IPMI devices.

Table 36: XMC J15 and J25 Connector Pin Assignments

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR (1)
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR (1)
4	GND	GND	TCK	GND	GND	NC
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR (1)
6	GND	GND	TMS	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR (1)
8	GND	GND	TDI	GND	GND	-12V
9	RFU	RFU	N.C.	RFU	RFU	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	PER0p0	PER0n0	NC	PER0p1	PER0n1	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PER0p2	PER0n2	3.3V AUX	PER0p3	PER0n3	VPWR (1)
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	N.C.	PER0p5	PER0n5	VPWR (1)
16	GND	GND	NVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	N.C.	PER0p7	PER0n7	N.C.
18	GND	GND	N.C.	GND	GND	N.C.
19	REFCLK+0	REFCLK-0	N.C.	N.C.	N.C.	N.C.

(1) VPWR is connected to +5V via a fuse.
The 12V option is available, please contact Kontron for more information on this topic.

Signals active when low.

4.5.2 XMC J26 Connector Pin Assignment

Table 37: XMC J26 Connector Pin Assignment

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	XMCIO_DP_P<1>	XMCIO_DP_N<1>	XMCIO_S<1>	XMCIO_DP_P<2>	XMCIO_DP_N<2>	XMCIO_S<2>
2	GND	GND	NC	GND	GND	NC
3	XMCIO_DP_P<3>	XMCIO_DP_N<3>	XMCIO_S<3>	XMCIO_DP_P<4>	XMCIO_DP_N<4>	XMCIO_S<4>
4	GND	GND	NC	GND	GND	NC
5	NC	NC	XMCIO_S<5>	NC	NC	XMCIO_S<6>
6	GND	GND	NC	GND	GND	NC
7	NC	NC	XMCIO_S<7>	NC	NC	XMCIO_S<8>
8	GND	GND	NC	GND	GND	NC
9	NC	NC	XMCIO_S<9>	NC	NC	XMCIO_S<10>
10	GND	GND	NC	GND	GND	NC

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
11	XMCIO_DP_P<11>	XMCIO_DP_N<11>	XMCIO_S<11>	XMCIO_DP_P<12>	XMCIO_DP_N<12>	XMCIO_S<12>
12	GND	GND	NC	GND	GND	NC
13	XMCIO_DP_P<13>	XMCIO_DP_N<13>	XMCIO_S<13>	XMCIO_DP_P<14>	XMCIO_DP_N<14>	XMCIO_S<14>
14	GND	GND	NC	GND	GND	NC
15	NC	NC	XMCIO_S<15>	NC	NC	XMCIO_S<16>
16	GND	GND	NC	GND	GND	NC
17	NC	NC	NC	NC	NC	NC
18	GND	GND	NC	GND	GND	NC
19	NC	NC	NC	NC	NC	NC

Refer to Table 25 page 54 for the mapping of XMC J26 connector or P0 rear connector.

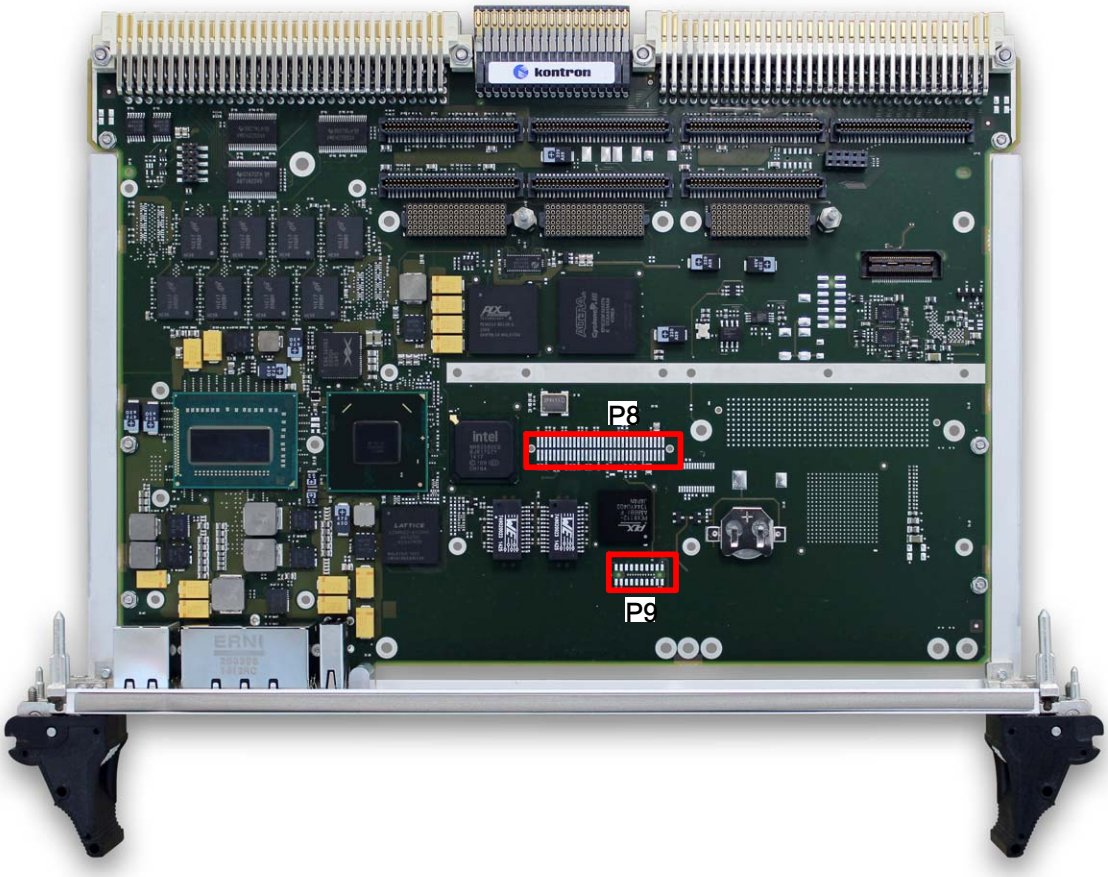
4.5.3 XMC Signal Decription

Table 38: XMC Signal Description

MNEMONIC	SIGNAL DESCRIPTION
GA[0..2]	I2C channel select. These signals allow a carrier to address a specific XMC slot on an IPMI I2C bus shared by multiple XMCs.
GND	Ground
MPRESENT	Module present. This signal allows the carrier to determine whether an XMC is present.
MRSTI	XMC Reset In. When this signal is asserted low by the carrier, the mezzanine card shall initialize itself into a known state.
MSCL	IPMI I2C serial clock.
MSDA	IPMI I2C serial data.
NVMRO	XMC Write Prohibit. When this signal is asserted high, the XMC shall disable writes to non-volatile memory on the XMC.
N.C.	Not Connected. Do not Used
PET0p/n[0..7]	Link 0 Differential Transmit. These signals are used by the XMC to receive high-speed protocol-specific data TO the carrier over the PCI Express interface.
PER0p/n[0..7]	Link 0 Differential Receive. These signals are used by the XMC to receive high-speed protocol-specific data FROM the carrier over the PCI Express interface.
REFCLK+/-0	Differential reference clock for Link 0 PCI Express interface.
RFU	Reserved for Future Use
TCK	JTAG Clock.
TDI	JTAG Data In
TDO	JTAG Data Out
TMS	JTAG Mode Select
TRST	JTAG Reset.
VPWR	Power pins. These signals carry either 12V or 5V power from the carrier to the XMC. 5V by default
3.3V	
3.3V AUX	
+/-12V	
XMCIO_DP_P/N [1...13]	XMC differential pair. Used to transmitt differential pair IO signals from secondary XMC connector (J26) to P0 connector
XMCIO_S [1...16]	XMC single ended IO. Used to transmitt single ended IO signals from secondary XMC connector (J26) to P0 connector

4.6 Personality Module Connectors

Figure 39: Location of the Personality Module Connectors



The personality module connectors P8 and P9 are used to connect module board such as MOD-GX (Graphic Module board) or MOD-GXA (Graphic and Audio Module board). These connectors are optional.

The personality module connectors are essentially provided to allow the installation of graphic module add and to offer graphic interfaces on front panel or on rear P0 connector.

The personality module connectors offer the following extra IO:

- 2 DisplayPort interfaces or HDMI/DVI interface,
- 1 VGA interface,
- PCH I2C bus,
- High definition audio interface.

4.6.1 P8 Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	DPD_LANE3_P	2	+3.3V
3	DPD_LANE3_N	4	GND
5	+5V	6	DPB_LANE3_P
7	GND	8	DPB_LANE3_N
9	DPD_LANE2_P	10	+3.3V
11	DPD_LANE2_N	12	GND
13	GND	14	DPB_LANE2_P
15	+5V	16	DPB_LANE2_N
17	DPD_LANE1_P	18	GND
19	DPD_LANE1_N	20	GND
21	+5V	22	DPB_LANE1_P
23	GND	24	DPB_LANE1_N
25	DPD_LANE0_P	26	+3.3V
27	DPD_LANE0_N	28	GND
29	GND	30	DPB_LANE0_P
31	+5V	32	DPB_LANE0_N
33	DPD_AUX_P	34	GND
35	DPD_AUX_N	36	GND
37	+5V	38	DPB_AUX_P
39	DPD_HPD_Q	40	DPB_AUX_N
41	DPB_HPD_Q	42	+3.3V
43	PLD_MODGX_MPRES#	44	DPB_CTRL_CLK
45	GND	46	DPB_CTRL_DATA
47	DPD_CTRL_CLK	48	GND
49	DPD_CTRL_DATA	50	GND
51	ISO_CRTCLK	52	ISO_CRTDAT
53	+5V	54	GND
55	GND	56	CRT_RED
57	CRT_GREEN	58	+3.3V
59	GND	60	CRT_VSYNC
61	CRT_BLUE	62	GND
63	GND	64	CRT_HSYNC

4.6.2 P9 Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	PCH_SMB_CLK	2	PCH_SMB_DAT
3	GND	4	GND
5	HDA_RST#	6	HDA_SDIN3
7	HDA_SYNC	8	HDA_SDIN2
9	HDA_BCLK	10	HDA_SDIN1
11	HDA_SDO	12	HDA_SDIN0
13	HDA_R_DOCKRST#	14	HDA_R_DOCKEN#
15	HDA_SPKR	16	MODGA_MPRES#
17	NC	18	NC
19	NC	20	NC

4.6.3 Personality Module Signal Description

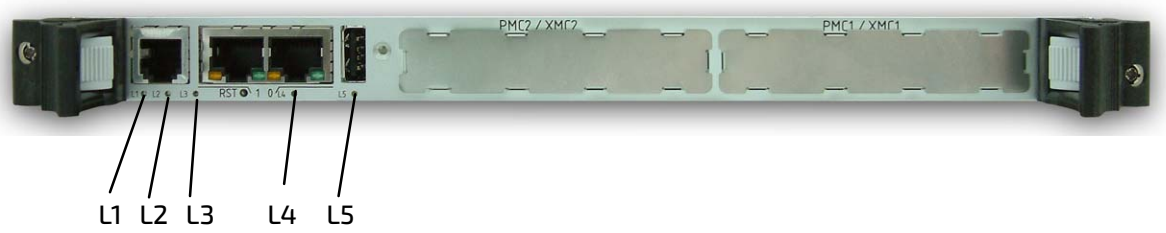
MNEMONIC	SIGNAL DEFINITION
CRT_RED	RED Analog Video Ouptut
CRT_GREEN	GREEN Analog Video Ouptut
CRT_BLUE	BLUE Analog Video Ouptut
CRT_VSYNC	CRT Vertical Synchronisation
CRT_HSYNC	CRT Horizontal Synchronisation
DPD_LANE_P/N [0...3]	Port D DisplayPort main link lane 0 to 3, support up to 2.7 Gb/s per lane
DPB_LANE_P/N [0...3]	Port B DisplayPort main link lane 0 to 3, support up to 2.7 Gb/s per lane
DPD_AUX_P/N	Port D DisplayPort Auxilliary channel (link device management)
DPB_AUX_P/N	Port B DisplayPort Auxilliary channel (link device management)
DPD_HPD_Q	Port D DisplayPort Hot Plug Detect
DPB_HPD_Q	Port B DisplayPort Hot Plug Detect
DPy_CTRL_CLK	Port y HDMI/DVI DDC clock signal
DPy_CTRL_DATA	Port y HDMI/DVI DDC data signal
ISO_CRTDAT	Monitor Control Data
ISO_CRTCLK	Monitor Control Clock
GND	Ground
+5VDC	
+3.3VDC	
PCH_SMB_DAT	PCH I2C serial data - see section 3.2 page 39
PCH_SMB_CLK	PCH I2C serial clock - see section 3.2 page 39
PLD_MODGX_MPRES#	MOD-GX presence indication
HDA_SDINx	HDA serial data in from the codec
HDA_RST#	HDA reset master hardware reset to external codec
HDA_SYNC	HDA sync 48 KHz fixed rate sample sync to the codec
HDA_BCLK	HDA bit clock output 24 MHz serial data clock
HDA_SDO	HDA serial data out to the codec
HDA_R_DOCKEN#	HDA dock enable
HDA_R_DOCKRST#	HDA doc reset for the codec
MOD-GXA_MPRES#	MOD-GXA board presence indication

4.7 LEDs

Status LEDs Normal Operation

There are five bicolor LEDs (Red/Green) on the front panel of the VM605x 6U VME board.

Figure 40: LEDs Front panel



By default (normal mode), the state of L3, L4 and L5 is according to the table below. But these LEDs can also be switched to user mode with the color and blinkling mode controlled by software.

When L1 is red (permanent error), the meaning of the other LEDs no more comply to the states listed in the table below, but report an error code as listed in the table at next paragraph.

Table 39: LEDs Description

CPU LED	COLOR	DESCRIPTION
L1	RED	Permanent error on CPU subsystem (CATERR, THERMTRIP, THERMPROT, Power failure, Power-on, Timeout)
	GREEN	Power-up start
	AMBER	Reset state on CPU subsystem
	BLINKING	CPLD activity (LPC access to CPLD, or backplane I2C activity). Blinking orange if reset; otherwise green.
	OFF	No error, no reset, no CPLD activity
L2	RED	CPLD watchdog reset timer expired
	GREEN	Normal operation mode
	AMBER	Factory test mode
	BLINKING	SATA activity
L3	RED	Processor Hot (PROCHOT) or CPU frequency limitation to 1.2 GHz
	GREEN	1000BaseT rear LAN link
	AMBER	10/100BaseT(X) rear LAN link
	BLINKING	LAN activity on rear
L4	RED	PBIT failed
	GREEN	PCI activity
	AMBER	ALMA2f VME FPGA downloading
	OFF	No error, no PCI activity
L5	RED	Power failure
	GREEN	PCI-X activity
	OFF	No error, no PCI-X activity

Status LEDs for permanent error

	L1	L2	L3	L4	L5	
ERR_PECI_CRIT	R	-	-	R	R	Critical level reported by NCT7802Y
ERR_THRMTRIP	R	-	R	R	R	CPU Thermal trip
ERR_CATERR	R	R	R	R	R	CPU Catastrophic error
ERR_VME_UV_PWRGD	R	-	-	-	O	Over voltage on backplane
ERR_VME_OV_PWRGD	R	R	-	-	O	Under voltage on backplane
ERR_INTERNAL_PSU	R	x	x	x	x	Board's internal PSU error

R : red
O : amber (orange)
- : off
x : any other combination of LEDs not already listed above

5 / Power and Thermal Specifications

5.1 Power Considerations

5.1.1 System Power

The considerations presented in the ensuing sections must be taken into account by system integrators when specifying the VM605x system environment.

5.1.1.1 VM605x Baseboard

The VM605x board has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the VM605x should be carefully tested to ensure compliance with these ratings.

Table 40: Maximum Input Power

SUPPLY VOLTAGE	MAXIMUM PERMIT VOLTAGE
+3.3VDC	+3.6V
+5VDC	+6V
+12V/-12VDC (1)	+14V/-14V

(1) if required for mezzanine.

+12V is mandatory for the board equipped with onboard SATA FLASH otherwise +12V is necessary if required by PMC or XMC board
-12V is necessary if required by PMC or XMC board

CAUTION: The maximum permitted voltage indicated in the table above must not be exceeded. Failure to comply with these figures may result in damage to your board.

The following table specifies the range of the different input power voltages within the board is functional. The VM605x is not guaranteed to function if the board is not operating within the prescribed limits.

Table 41: DC Operational Input Voltage Ranges

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE
+3.3V	3.25V min. to 3.45V max.
+5V	4.875V min to 5.25V max.
+12V (1)	11.64V min. to 12.6V max.
-12V (1)	-12.6V min. to -11.64V max.

(1) if required for mezzanine.

5.1.1.2 Backplane

Backplanes to be used with the VM605x must be adequately specified. The backplane must provide optimal power distribution for the +3.3V, +5V and +12V power inputs. It is recommended to use only backplanes which have at least two power planes for the +3.3V and +5V voltages.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided. It is recommended to use Positronic or M-type connector backplanes and power supplies where possible.

5.1.1.3 Power Supply Units

Power supplies for the VM605x must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires.

An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

As the design of the VM605x has been optimized for minimal power consumption, the power supply unit shall be stable even without minimum load.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for die resistance variations.

Tolerance

The following table provides information regarding the required characteristics for each board input voltage.

Table 42: Input Voltage Characteristics

VOLTAGE	NOMINAL VALUE	TOLERANCE	MAX. RIPPLE (P-P)	REMARKS
5V	+5.0 VDC	+5%/-3%	50 mV	Main voltage
3.3V	+3.3 VDC	+5%/-3%	50 mV	Main voltage
+12V	+12 VDC	+5%/-5%	240 mV	Required
-12V	-12 VDC	+5%/-5%	240 mV	Not Required
V I/O (PCI) signalling voltage	+3.3 VDC	+5%/-3%	50 mV	
GND	Ground, not directly connected to potential earth (PE)			

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

PMC site 1 and 2 are no 5V tolerant. VIO voltage must be +3.3 VDC

Regulation

The power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it went below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

5.1.2 Power Consumption

The power consumption tables below list the voltage and power specifications for the VM605x board. The values were measured using an 8-slot passive VME backplane with two power supplies: one for the CPU, and the other for the hard disk.

The processor dissipates the majority of the thermal power.

The power consumption of board can vary depending on the processor part and the ambient temperature, a deviation up to -20% with regard to the table below has been noted on VM6052 board.

Following board power consumption values take into account maximum processor TDP values.

Table 43: VM6052 Thermal Power: board power based on current measurements

	POWER MODE	CPU POWER MEASURED	MAX TOTAL POWER CONSUMPTION	CURRENT DRAWN	TEST CONDITION
VM6052 Intel® Core™ i7-3517UE	Turbo On	31.3W	50W	9.3 A / 5.0VDC 1.0 A / 3.3VDC	Linux FC16, TAT 100%, furmark GpuTest, 100°C processor junction temperature, USB keyboard/mouse, Front VGA interface with MOD-GX, 4x Gigabit Ethernet links, 8GB Dual bank DDR3-1333 memory configuration, no SSD flash on-board.
	Turbo off TDP UP @2.2 GHz	25W	42W	7.7 A / 5.0VDC 1.0 A / 3.3VDC	
	Turbo off TDP Nominal @1.7 GHz	17W	33W	5.9 A / 5.0VDC 1.0 A / 3.3VDC	
	Turbo off TDP Down @0.8 GHz	14W	30W	5.3 A / 5.0VDC 1.0 A / 3.3VDC	
	Linux idle Linux "on demande" mode Processor frequency 0.8 GHz, C1-State enable	4W	16W	2.5 A / 5.0VDC 1.0 A / 3.3VDC	Linux FC16, 55°C ambient temperature, 15CFM, USB keyboard/mouse, Front VGA interface with MOD-GX, 4x Gigabit Ethernet links, 8GB Dual bank DDR3-1333 memory configuration, no SSD flash on-board.
	BIOS under EFI shell prompt Processor frequency 0.8 GHz, C1-State enable	5W	17W	2.7 A / 5.0VDC 1.0 A / 3.3VDC	USB keyboard/mouse, Front VGA interface with MOD-GX, 4x Gigabit Ethernet links, 8GB Dual bank DDR3-1333 memory configuration, no SSD flash on-board. +/-1W tolerance on processor power measurement depending on Turbo/TDP mode configured.
Additional SSD flash on board			+1.2W	0.1A / 12VDC	
Additional PMC/XMC daughter card consumption			+15W	1.2mA/ 12VDC	
VM6052 Intel® CoreTM i7-3517UE 5V only	Turbo On	31.3W	50W	10 A / 5.0VDC	Linux FC16, TAT 100%, furmark GpuTest, 100°C processor junction temperature, USB keyboard/mouse, Front VGA interface with MOD-GX, 4x Gigabit Ethernet links, 8GB Dual bank DDR3-1333 memory configuration, no SSD flash on-board.
	Turbo off TDP UP @ 2.2 GHz	25W	42W	8.4 A / 5.0VDC	
	Turbo off TDP Nominal @ 1.7 GHz	17W	33W	6.6 A / 5.0VDC	
	Turbo off TDP Down @ 0.8 GHz	14W	30W	6.0 A / 5.0VDC	

Table 44: VM6054 Thermal Power: board power based on current measurements

	POWER MODE	MAX CPU POWER	MAX TOTAL POWER CONSUMP-TION	CURRENT DRAWN	TEST CONDITION
VM6054 Intel® CoreTM i7-3612QE	Turbo On	43.8W	62W	11.8 A / 5.0VDC 1.0 A / 3.3VDC	
	Turbo off @2.1GHz	35W	52W	9.8 A / 5.0VDC 1.0 A / 3.3VDC	Linux FC16, TAT 100%, furmark GpuTest, 100°C processor junction temperature, USB keyboard/mouse, Front VGA interface with MOD-GX, 4x Gigabit Ethernet links, 8GB Dual bank DDR3-1600 memory configuration, no SSD flash on-board.
	Turbo off @1.9 GHz	32W	49W	9.2 A / 5.0VDC 1.0 A / 3.3VDC	
	Turbo off @1.7 GHz	32W	49W	9.2 A / 5.0VDC 1.0 A / 3.3VDC	
	Turbo off @1.5 GHz	30W	46W	8.6 A / 5.0VDC 1.0 A / 3.3VDC	
	Turbo off @1.2 GHz	28W	43W	8.0 A / 5.0VDC 1.0 A / 3.3VDC	
	Linux idle Linux "on demand" mode Turbo off @2.1GHz, C1-State enable	8.5W	20W	3.4 A / 5.0VDC 1.0 A / 3.3VDC	Linux FC16, 55°C ambiant temperature, 15CFM, USB keyboard/mouse, Front VGA interface with MOD-GX, 4x Gigabit Ethernet links, 8GB Dual bank DDR3-1600 memory configuration, no SSD flash on-board.
	BIOS under EFI shell prompt Turbo off @2.1GHz, C1-State enable	8.5W	21W	TBD A / 5.0VDC 1.0 A / 3.3VDC	USB keyboard/mouse, Front VGA interface with MOD-GX, 4x Gigabit Ethernet links, 8GB Dual bank DDR3-1600 memory configuration, no SSD flash on-board. +/-1W tolerance on processor power measurement depending on Turbo/TDP mode configured.
Additional SSD flash on-board			+1.2W	0.1 A / 12VDC	
Additional PMC/XMC daughter card consumption			+15W	1.2 mA / 12VDC	

Table 45: Rail Current Draw

BOARD	5V RAIL CURRENT DRAW		3.3V RAIL CURRENT DRAW		12V RAIL CURRENT DRAW	
	MAXIMUM	PEAK	MAXIMUM	PEAK	MAXIMUM	PEAK
VM6052	11.5A	43A	1A	7.6A	0.14A	4A
VM6054	16.5A	43A	1A	7.6A	0.14A	4A

Maximum and peak current draw are intended as with enabled Turbo mode and without mezzanine card or USB device plugged on board.

Configurable TDP

In order to dynamically adjust the processor's behavior and package TDP to a desired system performance and power envelope, Intel has introduced Configurable TDP (cTDP) technology. This technology is available on VM6052 board only and allows operation in situations where extra cooling is available or situations where a cooler and quieter mode of operation is desired. With cTDP, the processor is now capable of altering the TDP power with an alternate ensured frequency. Configurable TDP can be enabled using firmware.

The cTDP consists of three modes :

- Nominal: This is the processor's rated frequency and TDP.
- TDP-Up: When extra cooling is available, this mode specifies a higher TDP and higher ensured frequency versus the nominal mode. Recommended mode.
- TDP-Down: When a cooler or quieter mode of operation is desired, this mode specifies a lower TDP and lower ensured frequency versus the nominal mode.

In each mode, the Intel Turbo Boost Technology power and frequency ranges are reprogrammed and the operating system is given a new effective HFM operating point. The cTDP mode does not change the maximum Turbo frequency. On VM6052 board turbo mode is disabled.

Configurable TDP is limited to a ULV processor i7-3517UE used on VM6052 board. TDP-Up mode is recommended for VM6052 in SA class and Nominal mode is recommended for VM6052 in WA class

5.1.3 Maximum Power Consumption of PMC Module

A maximum power of 7.5W is available on each PMC slot. This is in accordance with the draft standard P1386/Draft 2.4a. The maximum power of 7.5W can be arbitrarily divided on the 3.3V and 5V voltage lines.

PMC site 1 and 2 are no 5V VIO tolerant. PMC VIO voltage must be +3.3 VDC.

The following table indicates the current of a PMC module.

Table 46: Current of a PMC Module

VOLTAGE	STANDARD LIMIT CURRENT	DESIGN LIMIT CURRENT
3.3V	2.27A	4.6A
5V	1.5A	3A
+12V	0.5A	2A
-12V	0.4A	1A

Standard limit current is the limit current defined by P1386 standard. PMC should be able to dissipate at maximum 7.5W per voltage rail (3.3V and 5V).

Design limit current is the limit current defined by the board design, the current that not be exceed to avoid board damage.

5.1.4 Maximum Power Consumption of XMC Modules

A maximum power of 7.5W is available on each XMC slot and it can be arbitrarily divided on the 3.3V and 5V (VPWR) voltage lines. XMC modules are based on 3.3V power along with variable power (VPWR) defined as either 5V or 12V in the ANSI/VITA 42.0-200x XMC Switched Mezzanine Card Auxiliary Standard specification. On the VM605x, the VPWR is configured to 5 V.

The following table indicates the current of a XMC module.

Table 47: Current of a XMC Module

VOLTAGE	STANDARD LIMIT CURRENT	DESIGN LIMIT CURRENT
3.3V	0.75A	4.6A
5V (VPWR)	2.5A	3A
+12V (including VPWR option)	0.75A	2A
-12V	0.4A	1A

XMC integrators should carefully review the power ratings, cooling capacity and airflow requirements in the application prior to installation of an XMC module on the VM605x.

5.2 Thermal Consideration

The following chapter provide system integrators with the necessary information to satisfy thermal and airflow requirements when implementing VM605x applications.

5.2.1 Board Thermal Monitoring

To ensure optimal and long-term reliability of the VM605x, all onboard components must remain within the maximum temperature specifications. The most critical components on the VM605x are the processor and the memory. Operating the VM605x above the maximum operating limits will result in permanent damage to the board.

The VM605x includes several temperature sensors to measure the onboard temperature values:

- Thermal sensors integrated in the processor
- Four onboard temperature sensors

The four onboard temperature sensors (Texas Instrument LM73 and Nuvoton NCT7802Y) are located on the I^2C bus, and managed by the CPLDs (SMBus master interface). Refer to Figure 26 “I2C Diagram” page 39.

NCT7802Y Key specifications:

NCT7802Y is a Nuvoton Hardware Monitor IC, which can monitor power supply voltages and temperatures.

NCT7802Y designs on VM605x boards monitors processor core, memory, VME 12V and VME 5V voltages.

NCT7802Y supports one on-die temperature sensor and can also get the Intel® CPU temperature directly via Intel® PECI3.0 interface. NCT7802Y supports 3 alarm outputs: ALERT#, T_CRIT#, RESET# signals to activate system protection, connected to cPLD for event reporting.

As LM73 temperature sensors, NCT7802Y temperature and voltages monitoring comes with Linux "sensors" command.

- Voltage monitoring accuracy +-10mV
- Temperature Sensor Accuracy
  - On-chip Temperature Sensor Accuracy (25~70°C) +- 2°C typ.
  - On-chip Temperature Sensor Resolution 1 °C
- Operating Temperature Range -40°C ~ 85°C

Key Features of the onboard Temperature Sensors

- Local temperature accuracy: +/- 2°C.
- Operating temperature: -40 °C / +150°C.
- I2C address:

BOARD SENSORS	#1	#2	#3	#4
I2C address	90	92	94	50

Location of the onboard Temperature Sensors

Figure 41: Board Temperature Sensors Location on top side of the Board

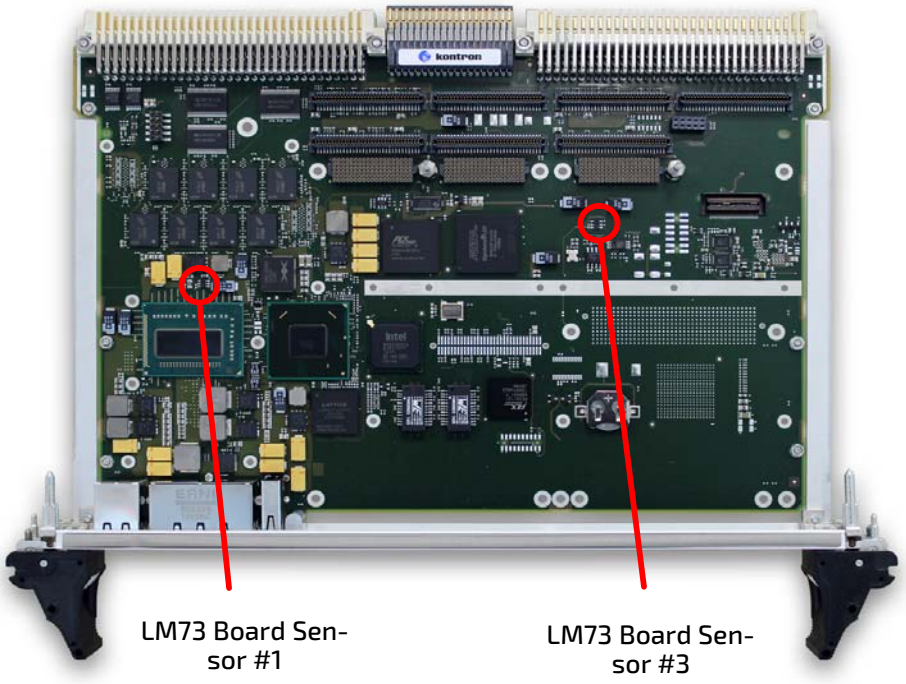
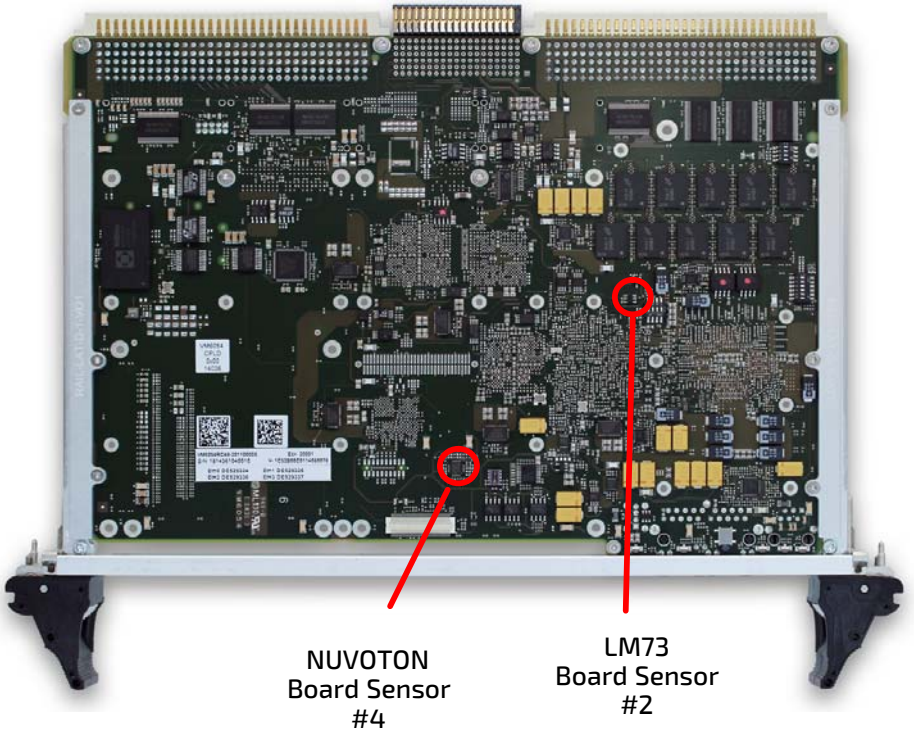


Figure 42: Board Temperature Sensors Location on bottom side of the Board



5.2.2 Processor Thermal Monitoring

To allow optimal operation and long-term reliability of the VM605x, the 3rd generation Intel® Core™ i7 Ivy Bridge processor must remain within the maximum die temperature specifications. The maximum operating temperature for the processor dies (TJMAX) is 105°C (including graphic and core). The TJMAX temperature is the temperature not to exceed, to avoid entering the throttling mode.

The 3rd generation Intel® Core ™ i7 processor uses the Adaptive Thermal Monitor feature to protect the processor from overheating and includes the following on-die temperature sensors:

- One Digital Thermal Sensor (DTS) for monitoring each processor core
- One Digital Thermal Sensor (DTS) for monitoring the graphics core
- One Digital Thermal Sensor (DTS) for monitoring the die temperature
- Catastrophic Cooling Failure Sensor (THERMTRIP#)

These sensors are integrated in the processor and work without any interoperability of the uEFI BIOS or the software application. Thermal Control Circuit allows the processor to maintain a safe operating temperature without the need for special software drivers or interrupt handling routines.

Digital Thermal Sensor (DTS)

The 3rd generation Intel® Core™ i7 processor includes four on-die Digital Thermal Sensors (DTS), one per processor cores, one for the graphics core and one for the package die. They can be read via an internal register of the processor. The temperature returned by the Digital Thermal Sensor will always be at or below the maximum operating temperature (105°C). Via the Digital Thermal Sensors, the uEFI BIOS or the application software can measure the processor die temperature.

Adaptive Thermal Monitor

The Adaptive Thermal Monitor feature reduces the processor power consumption and the temperature when the processor silicon exceeds its maximum operating temperature until the processor operates at or below its maximum operating temperature.

The processor core power reduction is achieved by:

- Frequency/sVID Control (by reducing of processor core voltage)
- Clock Modulation (by turning the internal processor core clocks off and on)

Adaptive Thermal Monitor dynamically selects the appropriate method. uEFI BIOS is not required to select a specific method as with previous-generation processors supporting Intel® Thermal Monitor 1 (TM1) and Intel® Thermal Monitor 2 (TM2).

The Adaptive Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

Frequency/sVID Control

Frequency/sVID Control reduces the processor's operating frequency (using the core ratio multiplier) and the input voltage (using serial VID signals). This combination of lower frequency and VID results in a reduction of the processor power consumption.

When the processor temperature reaches the TCC activation point, the event is reported to the bit PROCHOT of the CPLD register Alert Control & Status (0x85B). Refer to chapter 3.3 page 40 for register description.

Running the processor at the lower frequency and voltage will reduce power consumption and should allow the processor to cool off. If the processor temperature does not drop below its maximum operating temperature, a second frequency and voltage transition will take place.

This sequence of temperature checking and Frequency/sVID reduction will continue until either the minimum frequency has been reached or the processor temperature has dropped below its maximum operating temperature. If the processor temperature remains above its maximum operating temperature even after the minimum frequency has been reached, then Clock Modulation at that minimum frequency will be initiated.

When the LED3 on the front panel is lit red after boot-up, it indicates that the processor die temperature is above 105°C.

Clock Modulation

Clock Modulation reduces power consumption by rapidly turning the internal processor core clocks off and on at a duty cycle that should reduce power dissipation (typically a 30-50% duty cycle).

Once the temperature has dropped below the maximum operating temperature, the TCC goes inactive and clock modulation ceases.

When the LED3 on the front panel is lit red after boot-up, it indicates that the processor die temperature is above 105°C.

Catastrophic Cooling Failure Sensor

The Catastrophic Cooling Failure Sensor protects the processor from catastrophic overheating.

The Catastrophic Cooling Failure Sensor threshold is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds approximately 130°C. Once activated, the event remains latched until the VM605x undergoes a power-on restart (all power off and then on again).

This function cannot be enabled or disabled in the uEFI BIOS. It is always enabled to ensure that the processor is protected in any event.

5.2.3 Chipset Thermal Monitor Feature

The Intel® QM77 Chipset includes one on-die Thermal Diode Sensor to measure the chipset die temperature.
The maximum Intel® QM77 Chipset junction temperature is 108°C.

The PCH data sheet specifies: "The range is approximatively 40°C to 130°C. Temperature below 40°C will be truncated to 40°C".

5.2.4 External Thermal Regulation

To ensure the best possible basis for operational stability and long-term reliability, the VM605x is equipped with a heat sink (SA and WA classes only). Coupled together with system chassis, which provides variable configurations for forced airflow, controlled active thermal energy dissipation is guaranteed.

The physical size, shape, and construction of the heat sink ensures the lowest possible thermal resistance.
In addition, the VM6052/VM6054 has been specifically designed to efficiently support forced airflow as found in modern VME systems.

Thermal Characteristics Graphs

The thermal characteristic graphs shown in the following sections illustrate the maximum ambient air temperature as a function of the volumetric airflow rate for the processor frequency indicated.

The diagrams are intended to serve as guidance for reconciling board and system with the required computing power/ frequency considering the thermal aspect.

Two diagrams are provided, the first for VM6052 SA and WA classes, the second for VM6054 SA and WA classes. There are several curves representing upper level working points based on processor frequency (or configurable TDP for VM6052 board). When operating below the corresponding curve, the CPU runs steadily without any intervention of thermal supervision. When operated above the corresponding curve, various thermal protection mechanisms may take effect resulting in temporarily reduced CPU performance or finally in an emergency stop in order to protect the CPU and the chipset from thermal destruction. In real applications this means that the board can be operated temporarily at a higher ambient temperature or at a reduced flow rate and still provide some margin for temporarily requested peak performance before thermal protection will be activated.

How to read the Diagram

Select a board and its class, a processor frequency (or a cTDP) and choose a specific working point. For a given flow rate there is a maximum airflow input temperature (= ambient temperature) provided. Below this operating point, thermal supervision will not be activated. Above this operating point, thermal supervision will become active protecting the CPU from thermal destruction. The minimum airflow rate provided must be higher than the value specified in the diagram.

Values indicated in these graphs are issued from Thermal Analysis Tool from Intel with 100% of processor workload combined with GPU benchmark. These benchmarks exceed most of customer's applications in term of thermal dissipation.

Volumetric Flow Rate

The volumetric flow rate refers to an airflow through a fixed cross-sectional area (i.e. slot width x depth). The volumetric flow rate is specified in cfm (cubic-feetper- minute).

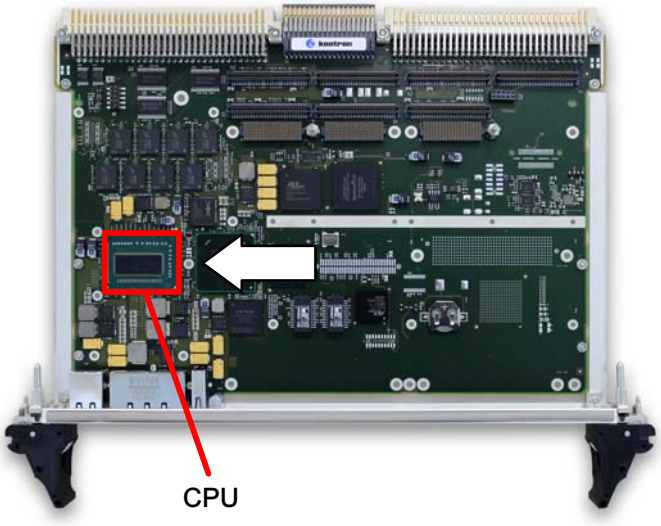
Airflow

At a given cross-sectional area and a required flow rate, an average, homogeneous airflow speed can be calculated using the following formula:

Airflow = Volumetric Flow Rate / Area

The airflow is specified in m/s (meter-per-second).

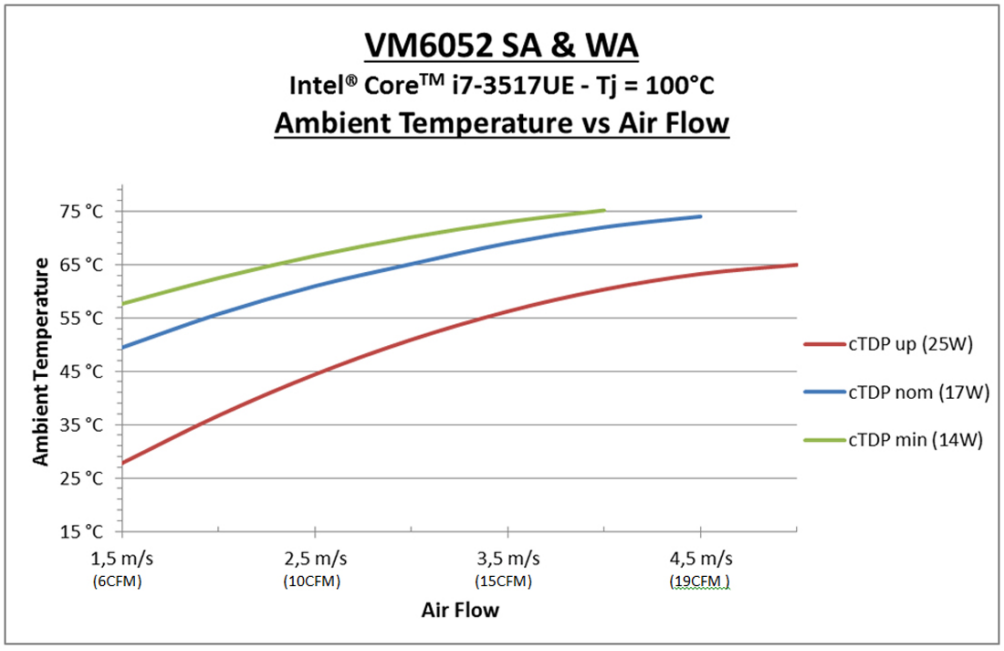
Figure 43: Airflow Direction

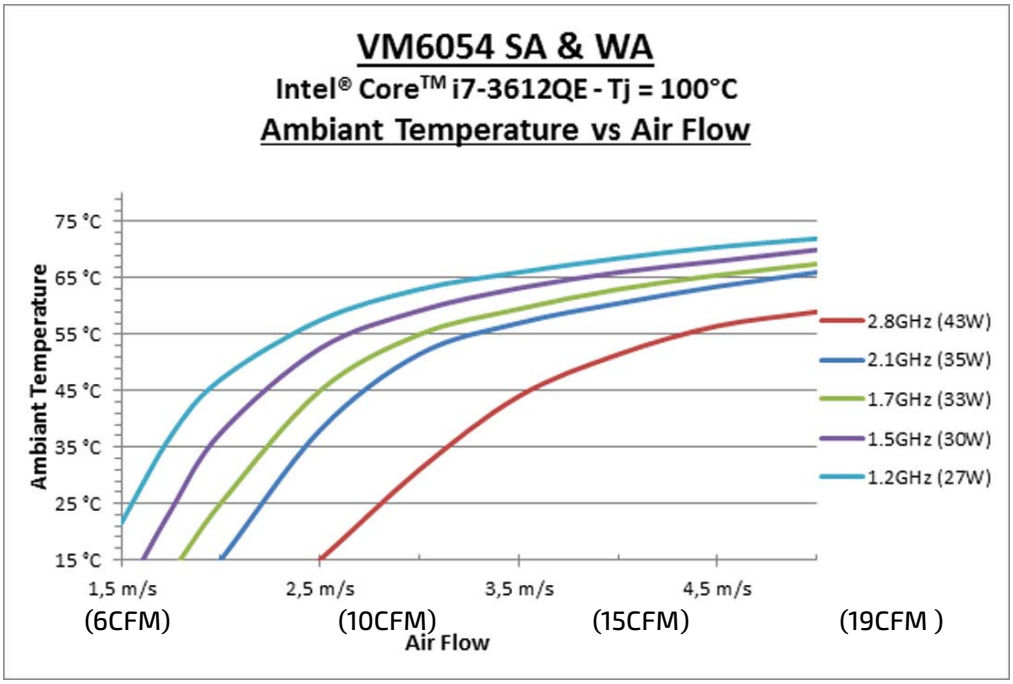


5.2.4.1 Operational Limits for the VM605x

The following figures illustrate the operational limits of the VM6052/VM6054 taking into consideration processor frequency (or configurable TDP) vs. ambient air temperature vs. airflow rate. The measurements were made based on a 4HP slot (0.8 inch height) and using Thermal Analysis Tool from Intel with 100% of processor workload combined with graphics benchmark.

Figure 44: VM6052 SA/WA Ambient Temperature vs Airflow





The above figure indicates the minimum air flow required for VM605x cooling. Be careful, these values are intended as without MOD-GX board presence and without PMC/XMC board presence and without carrier HDD onboard presence.

Default Frequency

Default frequency (or configurable TDP) on VM605x boards depends on class board to satisfy operating temperature. With this default setting, the VM605x processing performance is guaranteed across the whole operating temperature range. The VM605x thermal design is such as the processor, running at this frequency (or cTDP) does not enter thermal management mode (frequency throttling) when the processor temperature is maintained within the approved operating range.

CLASS	BOARD	CPU TDP	FREQUENCY	TJMAX ALL CORES	TAMB	MIN AIRFLOW	CALCULATED INPUT AIR SPEED FOR 0.8" INPUT SECTION
SA Class	VM6052 SA Corei7-3517UE	25W	2.2 GHz (1)	< 105°C	55°C	15 CFM	3.5 m/s
		17W	1.7 GHz	< 105°C	55°C	8 CFM	2.0 m/s
		14W	0.8 GHz	< 105°C	55°C	6 CFM	1.5 m/s
WA Class	VM6052 WA Corei7-3517UE	25W	2.2 GHz	< 105°C	65°C	21 CFM	5.0 m/s
		17W	1.7 GHz (1)	< 105°C	65°C	12.5 CFM	3.0 m/s
		14W	0.8GHz	< 105°C	65°C	10.5 CFM	2.5 m/s
SA Class	VM6054 SA Corei7-3612QE	35W	2.1 GHz (1)	< 105°C	55°C	13.3 CFM	3.3 m/s
		33W	1.7 GHz	< 105°C	55°C	12.1 CFM	3.0 m/s
		30W	1.5 GHz	< 105°C	55°C	10.4 CFM	2.6 m/s
		27W	1.2 GHz	< 105°C	55°C	8.7 CFM	2.3 m/s
WA Class	VM6054 WA Corei7-3612QE	35W	2.1 GHz	< 105°C	65°C	20.0 CFM	4.8 m/s
		30W	1.7 GHz	< 105°C	65°C	18.3 CFM	4.4 m/s
		30W	1.5 GHz	< 105°C	65°C	16.2 CFM	3.9 m/s
		27W	1.2 GHz(1)	< 105°C	65°C	13.7 CFM	3.3 m/s

(1) Default frequency

The processor frequency (or cTDP) is handled by the BIOS through the CPU configuration menu. Refer to the AMI BIOS for VM605x - User Reference Manual (SD.DT.G34). section 4.5 and section 5.1 for VM6054 board.

Intel® Turbo Boost Technology

Intel® Turbo Boost Technology is one of the many exciting features that Intel has built into latest-generation Intel® microarchitecture. It automatically allows processor cores to run faster than the base operating frequency if it's operating below power, current, and temperature specification limits.

On VM605x boards this technology is not recommended regarding to power dissipation rising and then turbo mode is disabled by default.

Dynamically increasing performance

Intel Turbo Boost Technology is activated when the Operating System (OS) requests the highest processor performance state (P0).

The maximum frequency of Intel Turbo Boost Technology is dependent on the number of active cores. The amount of time the processor spends in the Intel Turbo Boost Technology state depends on the workload and operating environment.

Any of the following can set the upper limit of Intel Turbo Boost Technology on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency will dynamically increase by 133 Mhz on short and regular intervals until the upper limit is met or the maximum possible upside for the number of active cores is reached.

Learn more about Intel Turbo Boost Technology: http://www.intel.com/technology/turboboost/

The Intel Turbo Boost is handled by the BIOS through the CPU configuration menu.

5.2.4.2 Peripherals

When determining the thermal requirements for a given application, peripherals to be used with the VM605x must also be considered. Devices such as MOD-GX, HDDs, SSDs, PMC modules, XMC modules, and SATA Flash modules which are directly attached to the VM605x must also be capable of being operated at the temperatures foreseen for the application. It may very well be necessary to revise system requirements to comply with operational environment conditions.

In most cases, this will lead to a reduction in the maximum allowable ambient operating temperature or even require active cooling of the operating environment.

CAUTION: As Kontron assumes no responsibility for any damage to the VM605x or other equipment resulting from overheating of the CPU, it is highly recommended that system integrators as well as end users confirm that the operational environment of the VM605x complies with the thermal considerations set forth in this document.

6 / Graphics Module Characteristics

6.1 Board Overview

Figure 45: MOD-GX Overview

6.1.1 Main Features

MOD-GX is a module board that is plugged on the personality module P8 of the VM605x board (refer to section 4.6 - Personality Module Connectors page 70). It offers three graphics interfaces in front panel of the VM605x, one VGA graphics interface and two mini DisplayPort interfaces.

Dual-mode DisplayPort

MOD-GX and VM605x boards are compliant with Dual-mode DisplayPort marked with a DP++ logo:

This mode allows to transmit single-link HDMI and DVI signals through DisplayPort cabling; this requires passive external adapters which convert to the higher signal levels used by DVI/HDMI.

Usually, Dual-mode DisplayPort chipset detects the DVI or HDMI passive adapter and switches to DVI/HDMI mode, this detection is performed by Cable Detect pin of DisplayPort connector (pin 13).

On VM6052 and VM6054 boards, the Dual-mode switching is not automatic, Cable Detect pin is not used, the switching is performed by hardware setting. Please contact Kontron to have this setting.

On graphic module, the Dual-mode switching is automatic, component of MOD-GX board manage Dual-mode signals using Cable Detect signal.

Dual-mode can only transmit single-link DVI/HDMI, as the number of pins in the DisplayPort connector is insufficient for dual-link connections.

Video resolution

MOD-GX board uses repeater device to improve the signal integrity of Digital video Interface and allows to benefit the better resolution provided by graphic chipset inside Intel Core-i7 (2560 x 1600 @ 60 Hz for DP and 1920 x 1200 @ 60 Hz for HDMI/DVI) .

The maximum resolution available on VGA interface is 2048x1538 (QXGA format).

The maximum recommended resolution for DisplayPort and VGA is 1920 x 1080 @ 60 Hz.

Dual Display

Dual Display is available on the VM605x board with MOD-GX. Dual display can be realized either by combining VGA interface with one of both DP interface or by combining both DP interfaces.

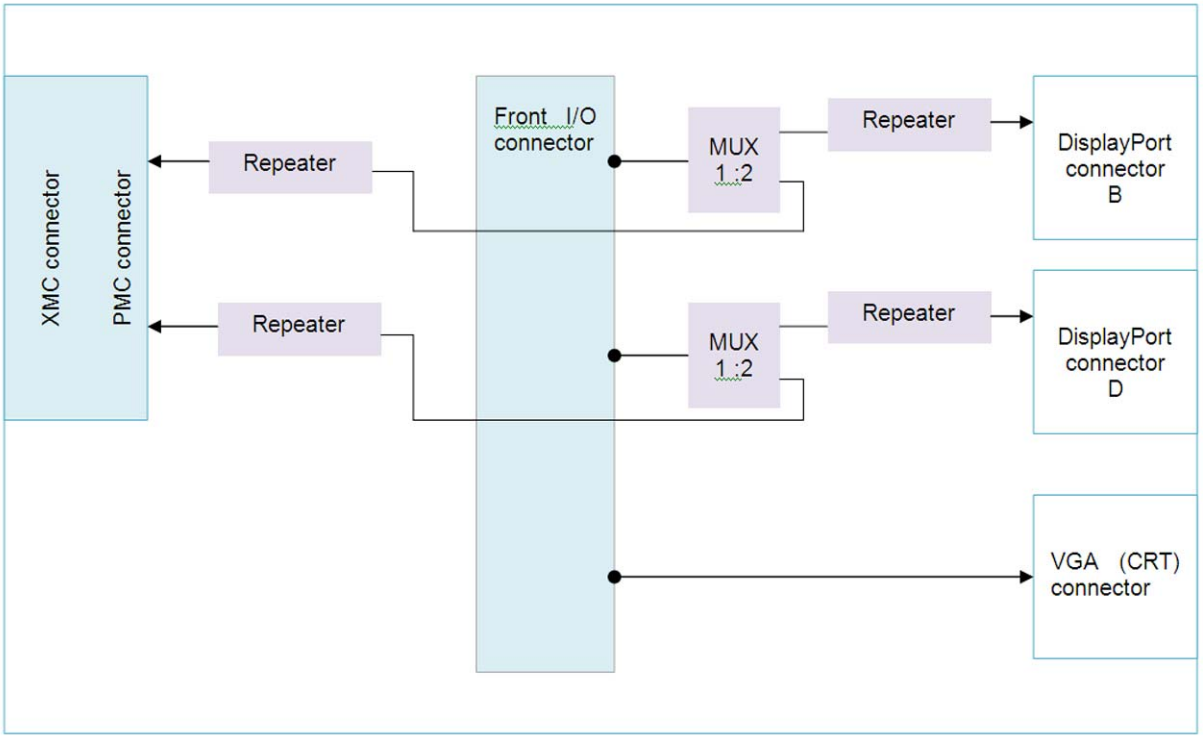
Main display can be chosen under BIOS setup. The main default display interface is VGA under Operating System at boot (Linux tested) and the main default interface is DisplayPort B under BIOS environment.

Rear Transition Module

Both DisplayPort are routed on the rear of the VM605x board through the MOD-GX board. DisplayPort signals are redirected to the rear using configuration switches of MOD-GX. RTM and PIM module (PIM-2DP) offer the possibility to have these 2 DisplayPort interfaces on standard DisplayPort connector. Contact Kontron for availability of PIM-2DP module board.

6.1.2 Block Diagram

Figure 46: MOD-GX Block Diagram



6.1.3 Ordering Information

ORDER CODE	DESCRIPTION
MOD-GX-SA-00	Air cooled Graphics module with two DisplayPort on front panel
MOD-GX-RC-00	Conduction Cooled Graphics module with two DisplayPort on rear

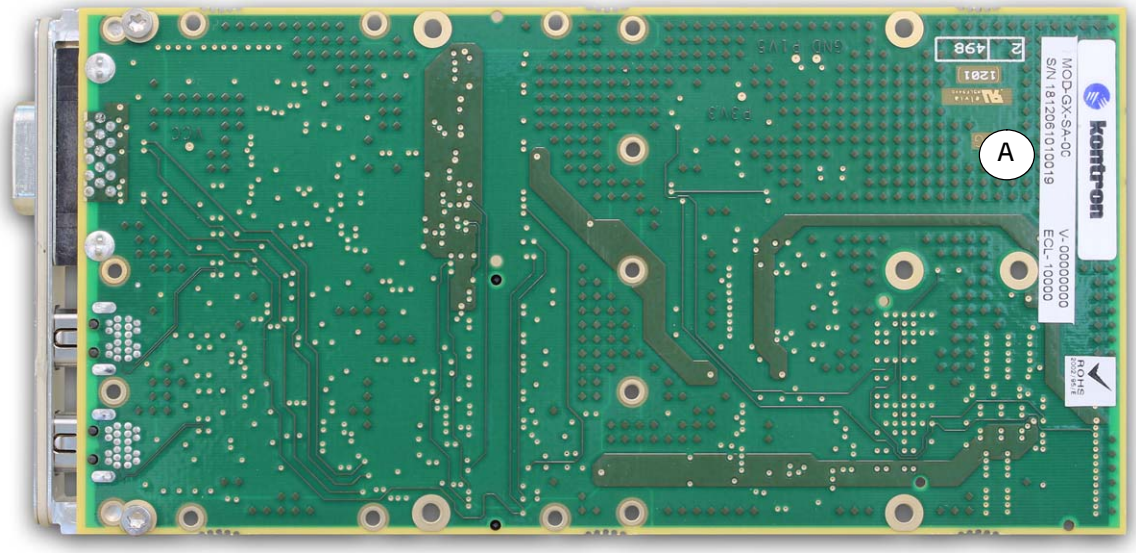
6.2 Installation of Graphic Module

6.2.1 Board identification

The MOD-GX boards are identified by labels fitted on the bottom side of the board.

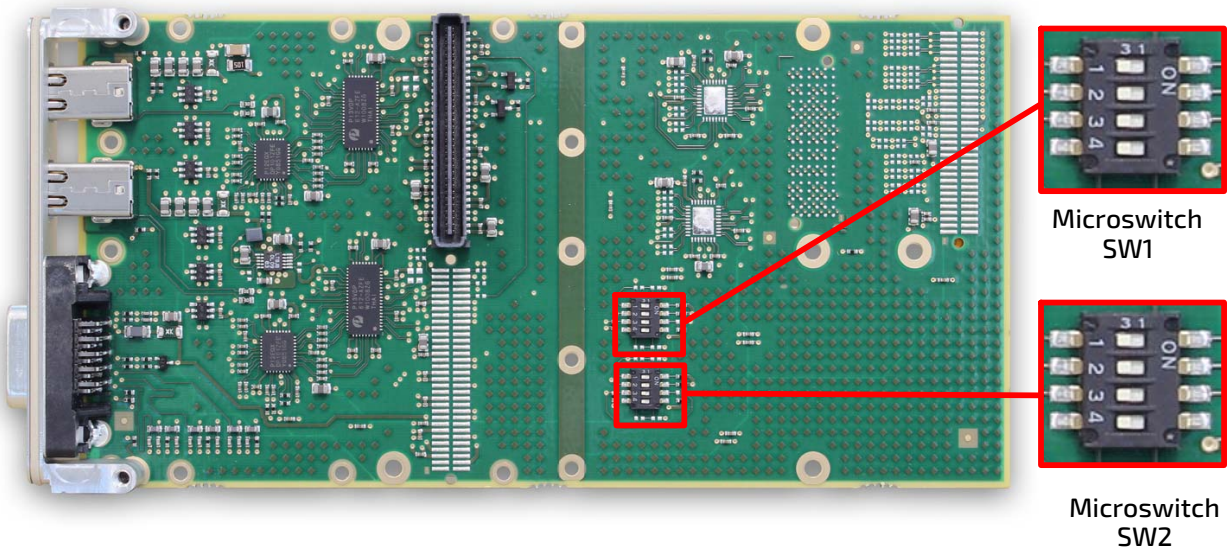
Figure 47: MOD-GX Identification Label Location

(A) "Identification" label: Order code, Serial Number, Variant, EC level



6.2.2 Microswitches Description

Figure 48: Microswitches Location on MOD-GX



SW1 switch is used for setting DisplayPort interface, port D from VM605x.

FUNCTION	DESCRIPTION
1 - Disable cable detect on Front	on: Force DisplayPort mode for DP D on front connector, disable cable detection off: Enable cable detection for DP D on front connector
2 - Disable cable detect on Rear	on: Force DisplayPort mode for DP D on rear connector, disable cable detection off: Enable cable detection for DP D on rear connector
3 - Front / Rear DisplayPort selection	on: DisplayPort D interface is routed to rear panel off: DisplayPort D interface is routed to front panel
4 - Not used	

SW2 switch is used for setting DisplayPort interface, port B from VM605x.

FUNCTION	DESCRIPTION
1 - Disable cable detect on Front	on: Force DisplayPort mode for DP B on front connector, disable cable detection off: Enable cable detection for DP B on front connector
2 - Disable cable detect on Rear	on: Force DisplayPort mode for DP B on rear connector, disable cable detection off: Enable cable detection for DP B on rear connector
3 - Front / Rear DisplayPort selection	on: DisplayPort B interface is routed to rear panel off: DisplayPort B interface is routed to front panel
4 - Not used	

6.3 Connectors

6.3.1 Front Panel Connectors

6.3.1.1 VGA Connector

The MOD-GX board integrates one VGA port available only on front panel.

- Pin Assignment

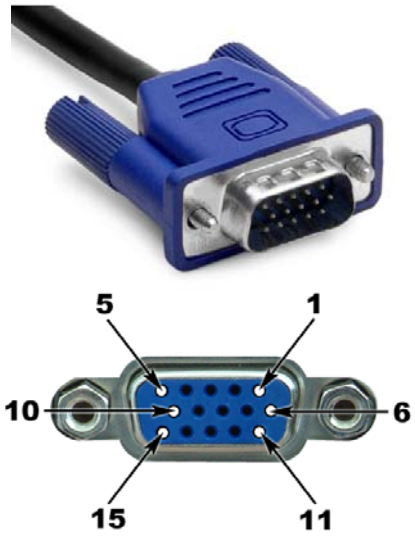
Connector used for the analog video signals transmission is the DE-15.

Table 48: VGA Connector Pin Assignment on MOD-GX

PIN	SIGNAL NAME
1	CRT_RED
2	CRT_GREEN
3	CRT_BLUE
4	N.C.
5	GND
6	N.C.
7	N.C.
8	N.C.
9	+5V
10	GND
11	N.C.
12	CRT_DAT
13	CRT_HSYNC
14	CRT_VSYNC
15	CRT_CLK

(N.C.: Not connected)

Figure 49: VGA Connector on MOD-GX



MNEMONIC	DESCRIPTION
CRT_RED	Red video signal
CRT_GREEN	Green video signal
CRT_BLUE	Blue Video signal
CRT_HSYNC	Horizontal synchronization video signal
CRT_VSYNC	Vertical synchronization video signal
GND	Ground
+5V	Power supply voltage
CRT_DAT	I2C Data bus
CRT_CLK	I2C clock bus

6.3.1.2 Mini DisplayPort Connectors

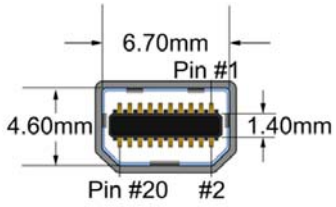
The MOD-GX board integrates two mini DisplayPort connectors (mDP) available on front panel and two DisplayPort available on rear.

Pin assignment

Table 49: Mini DisplayPort Connector Pin Assignment on MOD-GX

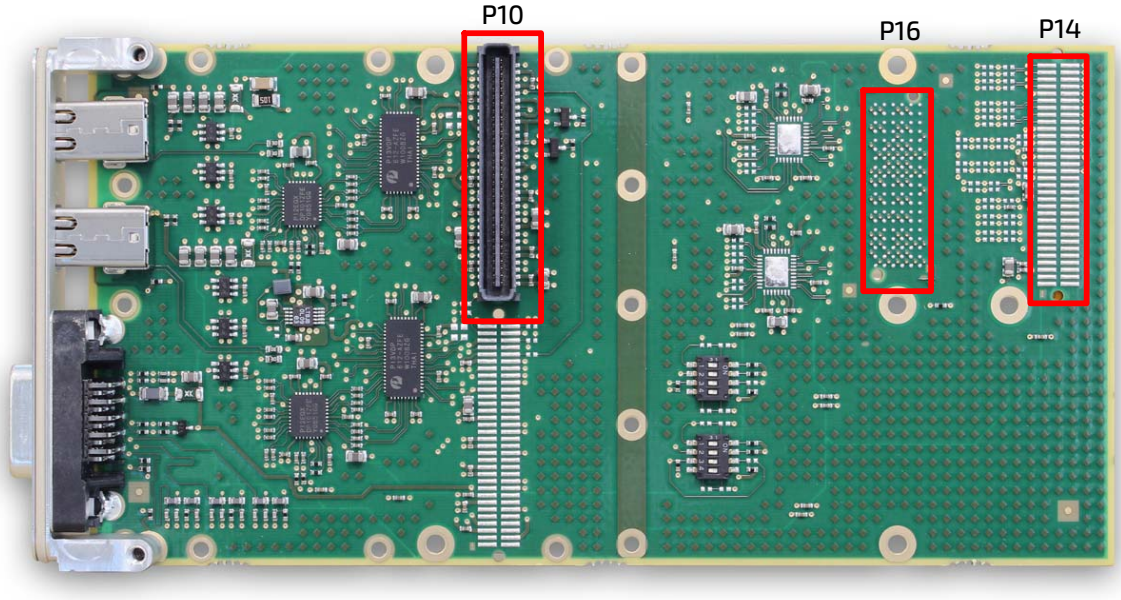
PIN	SIGNAL NAME	I/O
1	GND	--
2	HPD	I
3	LANE_0P	O
4	CAD	I
5	LANE_ON	O
6	RSVD	--
7	GND	--
8	GND	--
9	LANE_1P	O
10	LANE_3P	O
11	LANE_1N	O
12	LANE_3N	O
13	GND	--
14	GND	--
15	LANE_2P	O
16	AUX_CH_P	I/O
17	LANE_2N	O
18	AUX_CH_N	I/O
19	GND	--
20	+3.3V	--

Figure 50: Mini DisplayPort Connector on MOD-GX



MNEMONIC	DESCRIPTION
LANE_xP/N	Display Port main link lane 0 to 3, support up to 2.7 Gb/s per lane
AUX_CH_P/N	Display Port Auxilliary channel (link device management)
HPD	Hot Plug Detect
CAD	Cable Detect
+3.3V	+3.3V power supply output
GND	GROUND

6.3.2 Onboard Connectors



6.3.3 Front IO Connector (P10)

This connector is used to interface MOD-GX board to VM605x board. See also section 4.6 page 70 (Front I/O Connector) of this document.

Table 50: Front IO Connector Pin Assignment

FRONT IO PIN	SIGNAL		FRONT IO PIN	SIGNAL
1	DPD_LANE3_P		2	+3.3VDC
3	DPD_LANE3_N		4	GND
5	+5VDC		6	DPB_LANE3_P
7	GND		8	DPB_LANE3_N
9	DPD_LANE2_P		10	+3.3VDC
11	DPD_LANE2_N		12	GND
13	GND		14	DPB_LANE2_P
15	+5VDC		16	DPB_LANE2_N
17	DPD_LANE1_P		18	GND
19	DPD_LANE1_N		20	GND
21	+5VDC		22	DPB_LANE1_P
23	GND		24	DPB_LANE1_N
25	DPD_LANE0_P		26	+3.3VDC
27	DPD_LANE0_N		28	GND
29	GND		30	DPB_LANE0_P
31	+5VDC		32	DPB_LANE0_N
33	DPD_AUX_P		34	GND
35	DPD_AUX_N		36	GND
37	+5VDC		38	DPB_AUX_P
39	DPD_HPD_Q		40	DPB_AUX_N
41	DPB_HPD_Q		42	+3.3VDC
43	NC		44	NC
45	GND		46	NC

FRONT IO PIN	SIGNAL		FRONT IO PIN	SIGNAL
47	NC		48	GND
49	NC		50	GND
51	ISO_CRTCLK		52	ISO_CRTDAT
53	+5VDC		54	GND
55	GND		56	CRT_RED
57	CRT_GREEN		58	+3.3VDC
59	GND		60	CRT_VSYNC
61	CRT_BLUE		62	GND
63	GND		64	CRT_HSYNC

Table 51: Front IO Connector Signal Definition

MNEMONIC	SIGNAL DEFINITION
DPD_LANE_P/N [0...3]	Port D DisplayPort main link lane 0 to 3, support up to 2.7 Gb/s per lane
DPB_LANE_P/N [0...3]	Port B DisplayPort main link lane 0 to 3, support up to 2.7 Gb/s per lane
DPD_AUX_P/N	Port D DisplayPort Auxilliary channel (link device management)
DPB_AUX_P/N	Port B DisplayPort Auxilliary channel (link device management)
DPD_HPD_Q	Port D DisplayPort Hot Plug Detect
DPB_HPD_Q	Port B DisplayPort Hot Plug Detect
CRT_RED	RED Analog Video Ouptut
CRT_GREEN	GREEN Analog Video Ouptut
CRT_BLUE	BLUE Analog Video Ouptut
CRT_VSYNC	CRT Vertical Synchronisation
CRT_HSYNC	CRT Horizontal Synchronisation
ISO_CRTDAT	Monitor Control Data
ISO_CRTCLK	Monitor Control Clock
GND	Ground
+5VDC	
+3.3VDC	

6.3.4 XMC/PMC IO Pin Assignment

XMC or PMC IO connector (P16 and P14 connectors) are used to route DisplayPort signal of Port D and Port B to P0 in order to provide on rear of the VM605x two graphic interfaces.

These connectors are fitted on MOD-GX-RC.

Table 52: PMI IO Connector Pin Assignement P14

PMC PIN	SIGNAL		PMC PIN	SIGNAL
33	DPB1_HPD		34	DPD1_HPD
35	DPBPWR		36	DPDPWR
37	DPB1_CAD		38	DPDPWR
39	DPBPWR		40	DPD1_AUXn
41	DPD1_AUXp		42	DPD1_CAD
43	DPB1_AUXn/CRT_GREEN*		44	DPB1_AUXp/CRT_RED*
45	GND		46	GND
47	DPB1_LANE3p		48	DPB1_LANE0p
49	DPB1_LANE3n		50	DPB1_LANE0n
51	DPB1_LANE2p		52	DPB1_LANE1p
53	DPB1_LANE2n		54	DPB1_LANE1n
55	GND		56	GND
57	DPD1_LANE3p/CRT_BLUE*		58	DPD1_LANE0p
59	DPD1_LANE3n		60	DPD1_LANE0n
61	DPD1_LANE2p/CRT_HSYNC*		62	DPD1_LANE1p/CRT_VSYNC*
63	DPD1_LANE2n		64	DPD1_LANE1n

PMC [1..32] pins are not connected

(*) VGA signal are available on customer request, default is DisplayPort signal

Table 53: XMC IO Pin Assignement P16

XMC PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	DPD1_LANE0p	DPD1_LANE0n	GND	DPD1_LANE1p	DPD1_LANE1n	DPB1_HPD
2	GND	GND	NC	GND	GND	GND
3	DPD1_LANE2p	DPD1_LANE2n	GND	DPD1_LANE3p	DPD1_LANE3n	DPD1_HPD
4	GND	GND	NC	GND	GND	GND
5	NC	NC	DPBPWR	NC	NC	DPDPWR
6	GND	GND	NC	GND	GND	GND
7	NC	NC	DPB1_CAD	NC	NC	DPDPWR
8	GND	GND	NC	GND	GND	GND
9	NC	NC	DPBPWR	NC	NC	DPD1_AUXn
10	GND	GND	NC	GND	GND	GND
11	DPB1_LANE0p	DPB1_LANE0n	GND	DPB1_LANE1p	DPB1_LANE1n	DPD1_AUXp
12	GND	GND	NC	GND	GND	GND
13	DPB1_LANE2p	DPB1_LANE2n	GND	DPB1_LANE3p	DPB1_LANE3n	DPD1_CAD
14	GND	GND	NC	GND	GND	GND
15	NC	NC	DPB1_AUXn	NC	NC	DPB1_AUXp
16	GND	GND	NC	GND	GND	GND
17	NC	NC	NC	NC	NC	NC
18	GND	GND	NC	GND	GND	GND
19	NC	NC	NC	NC	NC	NC

Table 54: DisplayPort Routing to P0 Connector

PMC PIN	XMC PIN	SIGNAL	P0		PMC PIN	XMC PIN	SIGNAL	P0
33	F1	DPB1_HPD	B10		34	F3	DPD1_HPD	A10
35	C5	DPBPWR	E1		36	F5	DPDPWR	D1
37	C7	DPB1_CAD	C1		38	F7	DPDPWR	B1
39	C9	DPBPWR	A1		40	F9	DPD1_AUXn	E19
41	F11	DPD1_AUXp	D19		42	F13	DPD1_CAD	C19
43	C15	DPB1_AUXn	B19		44	F15	DPB1_AUXp	A19
45	C3	GND	C12		46	C1	GND	C11
47	D13	DPB1_LANE3p	D14		48	A11	DPB1_LANE0p	D11
49	E13	DPB1_LANE3n	E14		50	B11	DPB1_LANE0n	E11
51	A13	DPB1_LANE2p	D13		52	D11	DPB1_LANE1p	D12
53	B13	DPB1_LANE2n	E13		54	E11	DPB1_LANE1n	E12
55	C13	GND	C14		56	C11	GND	C13
57	D3	DPD1_LANE3p	A14		58	A1	DPD1_LANE0p	A11
59	E3	DPD1_LANE3n	B14		60	B1	DPD1_LANE0n	B11
61	A3	DPD1_LANE2p	A13		62	D1	DPD1_LANE1p	A12
63	B3	DPD1_LANE2n	B13		64	E1	DPD1_LANE1n	B12

Table 55: DisplayPort Signal Description

MNEMONIC	SIGNAL DESCRIPTION
DPD1_LANExp/n	Port D Display Port main link lane 0 to 3, support up to 2.7 Gb/s per lane
DPB1_LANExp/n	Port B Display Port main link lane 0 to 3, support up to 2.7 Gb/s per lane
DPD1_AUXp/n	Port D Display Port Auxilliary channel (link device management)
DPB1_AUXp/n	Port B Display Port Auxilliary channel (link device management)
DPD1_HPD	Port D Display Port Hot Plug Detect
DPB1_HPD	Port B Display Port Hot Plug Detect
DPD1_CAD	Port D Cable Detect Signal
DPB1_CAD	Port B Cable Detect Signal
DPDPWR	Port D +3.3VDC power supply. Fuse protection on MOD-GX board.
DPBPWR	Port B +3.3VDC power supply. Fuse protection on MOD-GX board.
GND	Ground

6.4 Environmental Specifications

Table 56: MOD-GX Environmental Specifications

	SA STANDARD COMMERCIAL			WA EXTENDED TEMPERATURE			RC RUGGED CONDUCTION-COOLED
Conformal Coating	Optional			Standard			Standard
Cooling Method	Convection			Convection			Conduction
Operating Temperature	0° to +55°C			-20° to +65°C			-40° to +85°C
Storage Temperature	-40° to +85°C			-45° to +100°C			-50° to +100°C
Vibration Sine (Operating)	20-500 Hz - 2g Acceleration / Frequency Range			20-500 Hz - 2g Acceleration / Frequency Range			22-2,000 Hz - 5g Acceleration / Frequency Range
Random	f (Hz)	10	40	100	200	2000	5Hz to 100Hz +3dB/octave 100Hz to 1000Hz 0.1g²/Hz 1000Hz to 2000Hz - 6dB/octave
	PSD (g2/Hz)	0.01	0.01	0.0007	0.0007	0.00005	
Shock (Operating)	20g/11 ms Peak Accel./ Shock Duration Half Sine			20g/11 ms Peak Accel./ Shock Duration Half Sine			40g/20 ms Peak Accel./ Shock Duration Half Sine
Altitude (Operating)	-1,500 to 60,000 ft			-1,500 to 60,000 ft			-1,500 to 60,000 ft
Relative Humidity	90% non-condensing			95% non-condensing			95% non-condensing

6.5 MTBF

Table 57: Graphic Module MTBF Data

	GB			NS		ARW	AIC	
	25°C	40°C	55°C	25°C	40°C	55°C	40°C	55°C
MTBF (hours)	1 610 534h	1 163 805h	-	269 665h	198 571h	35 224h	177 921h	-

6.6 Power Supply

6.6.1 Power Supplies

MOD-GX requires +5VDC and +3.3VDC power rail that are provided by VM605x board and available from Front IO connector.

6.6.2 Electrical Consumption

Following tables indicate current and power consumption and test condition for MOD-GX (5V or 3.3V).

VOLTAGE	5V	3.3V
RESULT	60 mA	500 mA

INTERFACE	CURRENT DRAW
VGA	50 Ma 5V
DP B	200 mA 3.3V
DP D	200 mA 3.3V

Max Power consumption of MOD-GX is 1.6W.

7 / Graphics and Audio Module Characteristics

7.1 Board Overview

Figure 51: MOD-GXA Overview

7.1.1 Main Features

MOD-GXA is a module board that is plugged on the personality module P8 and P9 connectors of the VM605x board (refer to section 4.6 - Personality Module Connectors page 70). It offers two micro HDMI interfaces and three audio jacks 3.5 mm interfaces in front panel of the VM605x, a line-in, line-out and a micro interfaces.

MOD-GXA board adapts DisplayPort signals coming from P8 connector of the VM605x board to HDMI signals using level shifter. It also converts High Definition Audio (HDA) signals coming from P9 connector to output/input analogue audio signals.

Video Resolution

MOD-GXA board uses repeater device to improve the signal integrity of Digital video Interface and allows to benefit the better resolution provided by graphic chipset inside Intel Core-i7 (1920 x 1200 @ 60 Hz for HDMI/DVI).

Dual Display

As MOD-GX, Dual Display is available on the VM605x board with MOD-GXA. Dual display can be realized by combining both HDMI interfaces.

Main display can be chosen under BIOS setup. The main default display interface is HDMI B under Operating System at boot (Linux tested) and under BIOS environment.

Audio

MOD-GXA implements a high performance multi-channel audio CODEC WOLFSON WM6680 offering full compatibility with Intel High Definition Audio (HDA) available on VM605x board.

MOD-GXA supports a stereo analogue line output and offers a high quality output audio (192 KHz/24 bits) with a ground-referenced stereo headphone amplifier. Line-out port (green) is dedicated to headset or speaker.

LINE-OUT FEATURES	
DAC sampling frequency	8 KHz – 192 KHz
SNR	108 dB
THD	-96 dB
Maximum output power	40 mW
Output impedance	16 Ω to 47 kΩ

Serial output capacitors are missing on line-out port. The using of headset is not recommended on this output, prefer speaker

MOD-GXA also has two high performance stereo input, an analogue line input and an analogue microphone input. MOD-GXA contains a stereo microphone interface with integrated pre-amp. Line-in port (blue) is dedicated to audio source. Microphone port (pink) is used to connect a analogue microphone.

FEATURES	LINE-IN	MICROPHONE
DAC sampling frequency	8 KHz – 96 KHz	8 KHz – 96 KHz
SNR	105 dB	105 dB
THD	-95 dB	-95 dB
V_{INRMS} (max)	1.6V	1.1 V
Output impedance	9 kΩ to 42 kΩ	10 kΩ to 120 kΩ

VPD EEPROM

MOD-GXA features an EEPROM 2 Kbits to store VPD (Vital Product Data). It is connected on PCH SMBus at address @0xA4 (7-bit I2C address @0x52). VPDs of MOD-GXA including ordering code, engineering change level, board serial number) are available under BIOS by using EFI shell command.

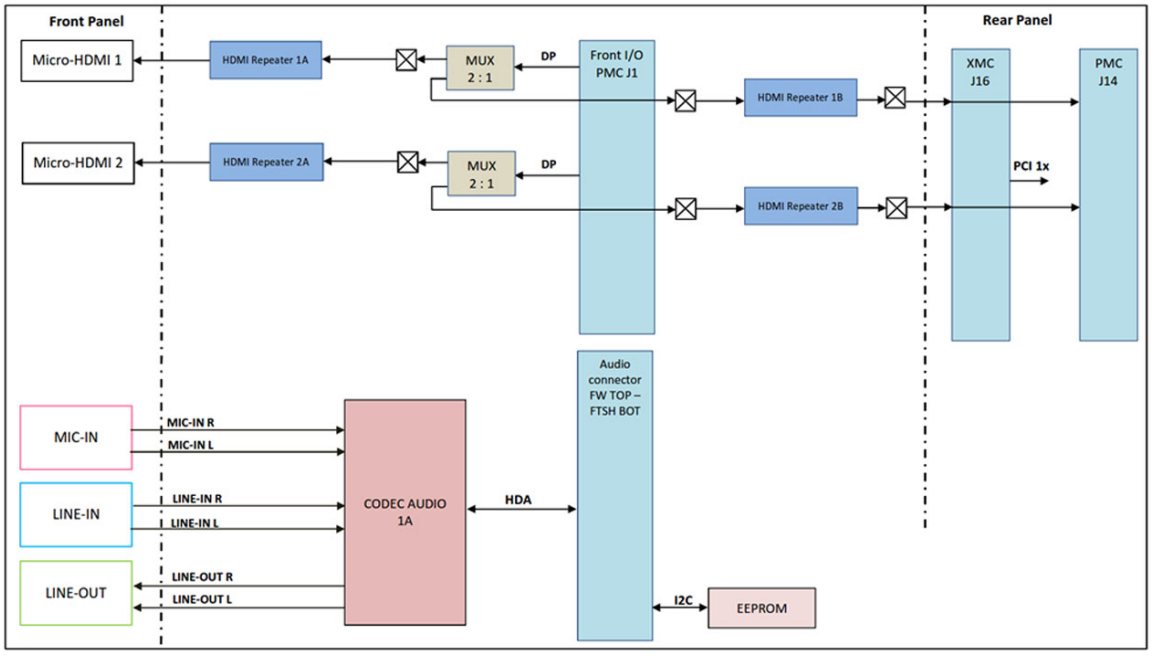
See section "Vital Product Data" in "VM605x AMI-BIOS User Reference Manual" – SD.DT.G34 to display the VPD information stored in MOD-GXA.

Rear Transition Module

Both HDMI are routed on the rear of the VM605x board through the MOD-GXA board. HDMI signals are redirected to the rear using the configuration switches of MOD-GXA.

7.1.2 Block Diagram

Figure 52: MOD-GXA Block Diagram



7.1.3 Ordering Information

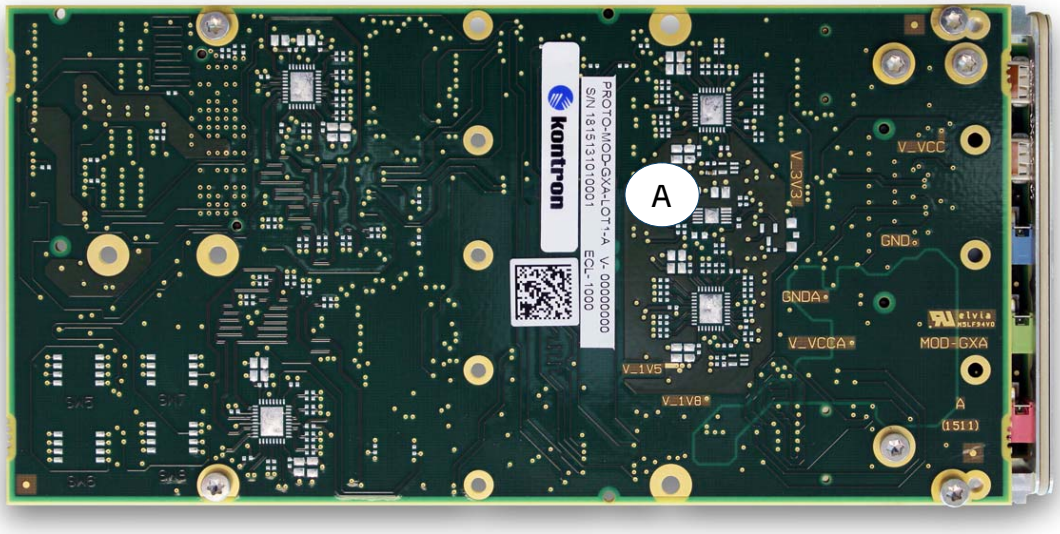
PRODUCT	ORDER CODE	DESCRIPTION
MOD-GXA	MOD-GXA-SA-00	Air cooled Graphics and Audio module with two HDMI and three audio 3.5 jack connector on front panel
MOD-GXA	MOD-GXA-RC-00	Conduction cooled Graphics and Audio module with two HDMI on rear

7.2 Installation of Graphic and Audio Module

7.2.1 Board identification

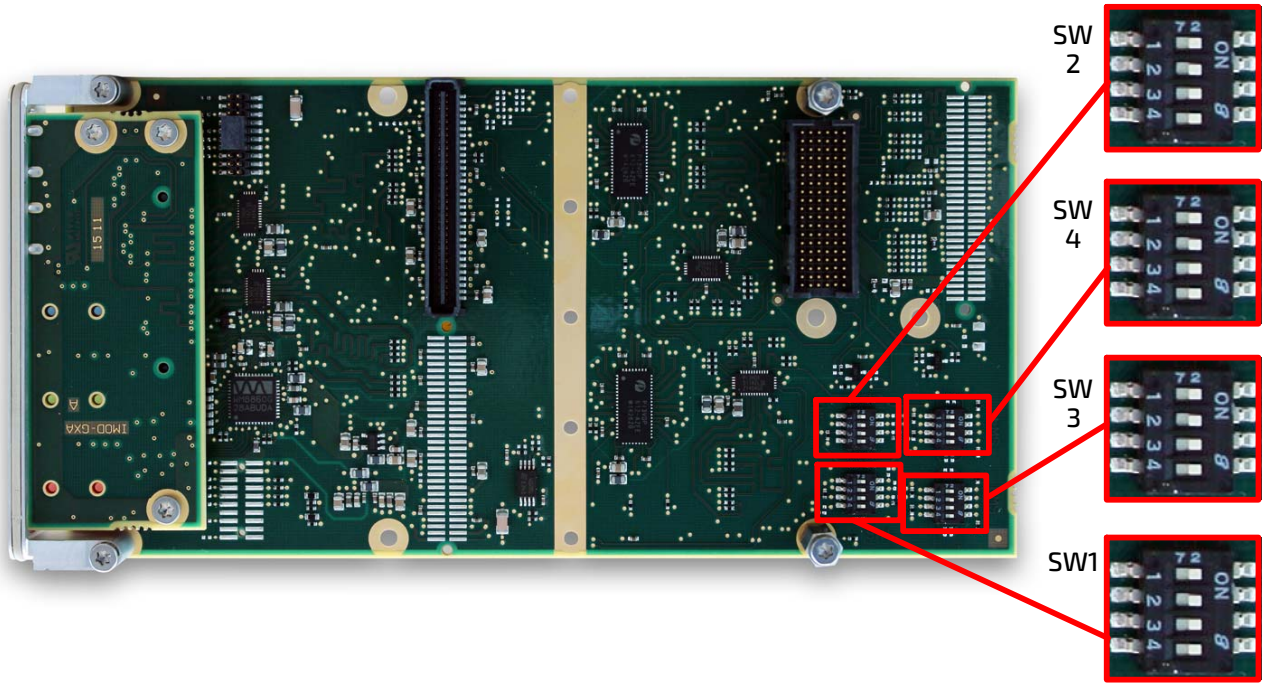
The MOD-GXA boards are identified by labels fitted on the bottom side of the board.

A "Identification" label: Order Code, Serial Number, Variant E.C. Level



7.2.2 Microswitches Description

Figure 53: Microswitches Location



- SW1 switch is used for setting HDMI interface, port D from VM605x.

PORT	FUNCTION	DESCRIPTION
1	Not Used	off: (default)
2	Not Used	off: (default)
3	Front or rear Video selection	on: Redirect Video interface to rear off: Redirect Video interface to front panel (default)
4	EEPROM SPD Write protection	on: Write Protect Enabled (default) off: Write Protected

- SW2 switch is used for setting HDMI interface, port B from VM605x.

PORT	FUNCTION	DESCRIPTION
1	Not Used	off: (default)
2	Not Used	off: (default)
3	Front or rear Video selection	on: Redirect Video interface to rear off: Redirect Video interface to front panel (default)
4	Not used	off: (default)

- SW3 switch is used for setting HDMI interface, port D from VM605x.
- SW4 switch is used for setting HDMI interface, port B from VM605x.

PORT	FUNCTION	DESCRIPTION
1	Operation mode	on: POWER DOWN Mode off: NORMAL operation mode (default)
2 and 3	TMDS output pre-emphasis Setting	SW3.2 and SW3.3 Off : 2.5dB Source termination (default) SW3.2 Off and SW3.3 On : 0dB Source termination SW3.2 On and SW3.3 Off : 2.5dB Open Drain SW3.2 On and SW3.3 On : 0dB Open Drain
4	TMDS input equalization	on: 9 dB (default) off: 3dB

7.3 Connectors

7.3.1 Front Panel Connectors

7.3.1.1 HDMI Connectors

The MOD-GXA board integrates two micro HDMI connectors available on front panel.

Table 58: HDMI Connectors Pin Assignement

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	HPD	2	NC
3	TMDS_DATA_2-	4	GND
5	TMDS_DATA_2+	6	TMDS_DATA_1+
7	GND	8	TMDS_DATA_1-
9	TMDS_DATA_0+	10	GND
11	TMDS_DATA_0-	12	TMDS_DATA_CLOCK+
13	GND	14	TMDS_DATA_CLOCK-
15	CEC	16	DDC/CEC GND
17	SCL	18	SDA
19	HDMI_PWR		

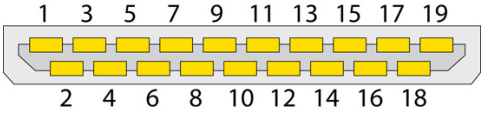


Table 59: HDMI Connectors Signal Description

MNEMONIC	DESCRIPTION
TMDS_DATA_x+/-	HDMI main channel 0 to 2
TMDS_DATA_CLOCK+/-	HDMI clock channel
HPD	Hot Plug detect
CEC	Consumer Electronics Control
SCL	Serial clock for DDC (Display Data Channel)
SDA	Serial data line for DDC (Display Data Channel)
HDMI_PWR	+5V power supply
GND	Ground
DDC/CEC GND	DDC/CEC Ground

7.3.1.2 Audio Connectors

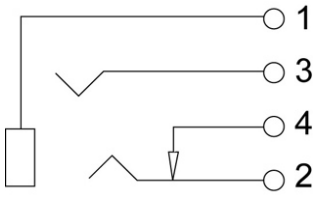
The MOD-GXA board integrates three audio 3.5mm jack connectors. There are available on front panel in Green, Blue and Pink color regarding kind of input/output analogue audio.

Table 60: Audio Connectors Pin Assignement

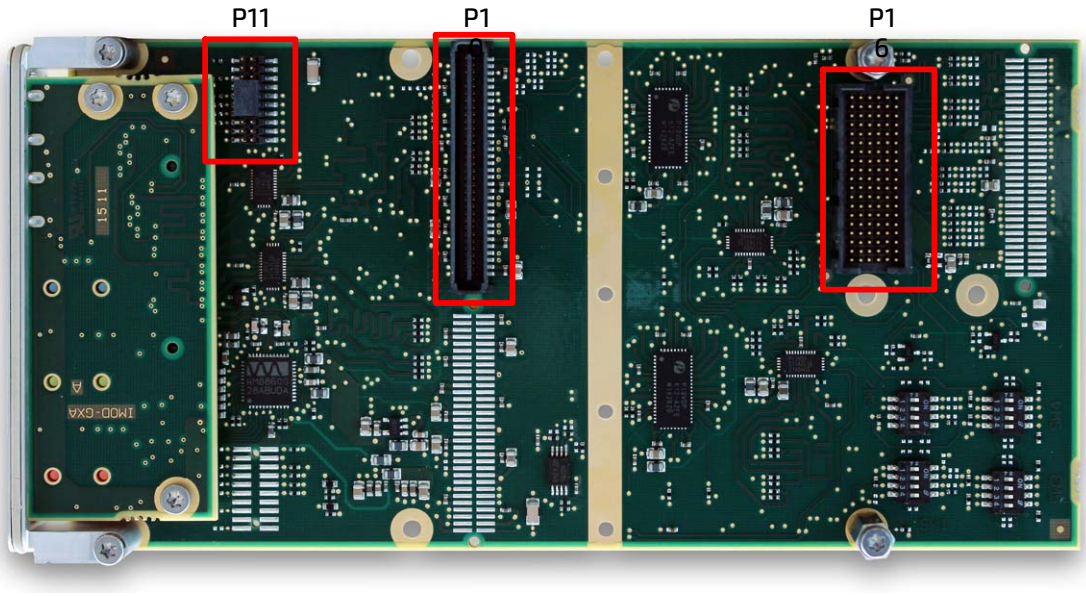
PIN	LINE-OUT SIGNAL NAME	LINE-IN SIGNAL NAME	MICROPHONE SIGNAL NAME
1	GNDA	GNDA	GNDA
2	CON_HEADPHONE_L	CON_LINE_IN_L	CON_MIC_L
3	CON_HEADPHONE_R	CON_LINE_IN_R	CON_MIC_R
4	CON_HEADPHONE_L	CON_LINE_IN_L	CON_MIC_L

Table 61: Audio Connectors Signal Description

MNEMONIC	DESCRIPTION
CON_HEADPHONE_L	Left analogue speaker output
CON_HEADPHONE_R	Right analogue speaker output
CON_LINE_IN_L	Left analogue line input
CON_LINE_IN_R	Right analogue line input
CON_MIC_L	Left analogue microphone input
CON_MIC_R	Right analogue microphone input
GNDA	Analogue Ground

MODEL NO	SJ-3524-SMT
Schematic	
PIN	
1	Sleeve
2	Tip
3	Ring
4	Tip Switch

7.3.2 On-board Connectors



7.3.2.1 Front IO Connector (P10)

This connector is used to interface video signal of VM605x carrier board to MOD-GXA board. See also section 4.6 page 70 (Front I/O Connector) of this document.

Table 62: Front IO Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	DPD_LANE3_P	2	+3.3V
3	DPD_LANE3_N	4	GND
5	+5V	6	DPB_LANE3_P
7	GND	8	DPB_LANE3_N
9	DPD_LANE2_P	10	+3.3V
11	DPD_LANE2_N	12	GND
13	GND	14	DPB_LANE2_P
15	+5V	16	DPB_LANE2_N
17	DPD_LANE1_P	18	GND
19	DPD_LANE1_N	20	GND
21	+5V	22	DPB_LANE1_P
23	GND	24	DPB_LANE1_N
25	DPD_LANE0_P	26	+3.3V
27	DPD_LANE0_N	28	GND
29	GND	30	DPB_LANE0_P
31	+5V	32	DPB_LANE0_N
33	DPD_AUX_P	34	GND
35	DPD_AUX_N	36	GND
37	+5V	38	DPB_AUX_P
39	DPD_HPD_Q	40	DPB_AUX_N

PIN	SIGNAL	PIN	SIGNAL
41	DPB_HPD_Q	42	+3.3V
43	MODGX_MPRES#	44	HDMI_B_DDC_CLK
45	GND	46	HDMI-B-DDC_DATA
47	HDMI_D_DDC_CLK	48	GND
49	HDMI_D_DDC_DATA	50	GND
51	ISO_CRTCLK	52	ISO_CRTDAT
53	+5V	54	GND
55	GND	56	CRT_RED
57	CRT_GREEN	58	+3.3V
59	GND	60	CRT_VSYNC
61	CRT_BLUE	62	GND
63	GND	64	CRT_HSYNC

Table 63: Front IO Connector Signal Definition

MNEMONIC	SIGNAL DEFINITION
DPD_LANE_P/N [0...3]	Port D DisplayPort main link lane 0 to 3, support up to 2.7 Gb/s per lane
DPB_LANE_P/N [0...3]	Port B DisplayPort main link lane 0 to 3, support up to 2.7 Gb/s per lane
DPD_AUX_P/N	Port D DisplayPort Auxilliary channel (link device management)
DPB_AUX_P/N	Port B DisplayPort Auxilliary channel (link device management)
DPD_HPD_Q	Port D DisplayPort Hot Plug Detect
DPB_HPD_Q	Port B DisplayPort Hot Plug Detect
CRT_RED	RED Analog Video Ouptut
CRT_GREEN	GREEN Analog Video Ouptut
CRT_BLUE	BLUE Analog Video Ouptut
CRT_VSYNC	CRT Vertical Synchronisation
CRT_HSYNC	CRT Horizontal Synchronisation
ISO_CRTDAT	Monitor Control Data
ISO_CRTCLK	Monitor Control Clock
GND	Ground
+5VDC	
+3.3VDC	
HDMI_D_DDC_CLK	Port D HDMI DDC Serial clock clock (Display Data Channel)
HDMI_D_DDC_DATA	Port D HDMI DDC Serial data line (Display Data Channel)
HDMI_B_DDC_CLK	Port B HDMI DDC Serial clock clock (Display Data Channel)
HDMI_B_DDC_DATA	Port B HDMI DDC Serial data line (Display Data Channel)
MODGX_MPRES#	MOD-GXA board presence indication

7.3.2.2 Audio Connector (P11)

This connector is used to interface HDA signals and PCH SMBus of VM605x carrier board to MOD-GXA board. See also section 4.6 page 79 (Front I/O Connector) of this document.

Table 64: Audio Connector Pin Assignement

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	PCH_SMB_CLK	2	PCH_SMB_DAT
3	GND	4	GND
5	HDA_RST#	6	HDA_SDIN3
7	HDA_SYNC	8	HDA_SDIN2
9	HDA_BLCK	10	HDA_SDIN1
11	HDA_SDO	12	HDA_SDIN0
13	NC	14	NC
15	NC	16	MODGA_MPRES#
17	NC	18	NC
19	NC	20	Reserved

Table 65: Audio Connector Signal Description

MNEMONIC	DESCRIPTION
PCH_SMB_CLK	PCH I2C serial clock - see section 3.2 page 39
PCH_SMB_DAT	PCH I2C serial data - see section 3.2 page 39
HDA_SDINx	HDA serial data in from the codec
HDA_RST#	HDA reset master hardware reset to external codec
HDA_SYNC	HDA sync 48 KHz fixed rate sample sync to the codec
HDA_BLCK	HDA bit clock output 24 MHz serial data clock
HDA_SDO	HDA serial data out to the codec
MODGA_MPRES#	MOD-GXA board audio signal presence

7.3.2.3 XMC IO Pin Connector (P16)

XMC IO connector is used to route HDMI signal of Port D and Port B to P0 in order to provide on rear of the VM605x two HDMI graphic interfaces.

Table 66: XMC IO Pin Assignment

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	HDMI_D_0+	HDMI_D_0-	GND	HDMI_D_1+	HDMI_D_1-	HPD_B
2	GND	GND	NC	GND	GND	NC
3	HDMI_D_2+	HDMI_D_2-	GND	HDMI_D_3+	HDMI_D_3-	HPD_D
4	GND	GND	NC	GND	GND	NC
5	NC	NC	PWR_B	NC	NC	PWR_D
6	GND	GND	NC	GND	GND	NC
7	NC	NC	NC	NC	NC	PWR_D
8	GND	GND	NC	GND	GND	NC
9	NC	NC	PWR_B	NC	NC	HDMI_D_DDC-
10	GND	GND	NC	GND	GND	NC
11	HDMI_B_0+	HDMI_B_0-	GND	HDMI_B_1+	HDMI_B_1-	HDMI_D_DDC+
12	GND	GND	NC	GND	GND	NC
13	HDMI_B_2+	HDMI_B_2-	GND	HDMI_B_3+	HDMI_B_3-	NC
14	GND	GND	NC	GND	GND	NC

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
15	NC	NC	HDMI_B_DDC-	NC	NC	HDMI_B_DDC+
16	GND	GND	NC	GND	GND	NC
17	NC	NC	NC	NC	NC	NC
18	GND	GND	NC	GND	GND	NC
19	NC	NC	NC	NC	NC	NC

Table 67: XMC IO Signal Definition

MNEMONIC	DESCRIPTION
HDMI_D_x+/-	TMDS main channel 0 to 2 of HDMI port D
HDMI_D_3+/-	TMDS clock of HDMI port D
HDMI_D_DDC+	Serial clock for DDC (Display Data Channel) of HDMI port D
HDMI_D_DDC-	Serial data line for DDC (Display Data Channel) of HDMI port D
HPD_D	Hot plug detect for HDMI port D
HDMI_B_x+/-	TMDS main channel 0 to 2 of HDMI port B
HDMI_B_3+/-	TMDS clock of HDMI port B
HDMI_B_DDC+	Serial clock for DDC (Display Data Channel) of HDMI port B
HDMI_B_DDC-	Serial data line for DDC (Display Data Channel) of HDMI port B
HPD_B	Hot plug detect for HDMI port B
PWR_D	5VDC power supply for HDMI port D
PWR_B	5VDC power supply for HDMI port B
GND	Ground

Table 68: HDMI Routing to P0 Connector

XMC PIN	SIGNAL	P0		XMC PIN	SIGNAL	P0
F1	HPD_B	B10		F3	HPD_D	A10
C5	PWR_B	E1		F5	PWR_D	D1
C7	NC	C1		F7	PWR_D	B1
C9	PWR_B	A1		F9	HDMI_D_DDC-	E19
F11	HDMI_D_DDC+	D19		F13	NC	C19
C15	HDMI_B_DDC-	B19		F15	HDMI_B_DDC+	A19
C3	GND	C12		C1	GND	C11
D13	HDMI_B_3+	D14		A11	HDMI_B_0+	D11
E13	HDMI_B_3-	E14		B11	HDMI_B_0-	E11
A13	HDMI_B_2+	D13		D11	HDMI_B_1+	D12
B13	HDMI_B_2-	E13		E11	HDMI_B_1-	E12
C13	GND	C14		C11	GND	C13
D3	HDMI_D_3+	A14		A1	HDMI_D_0+	A11
E3	HDMI_D_3-	B14		B1	HDMI_D_0-	B11
A3	HDMI_D_2+	A13		D1	HDMI_D_1+	A12
B3	HDMI_D_2-	B13		E1	HDMI_D_1-	B12

7.4 Environmental Specifications

Table 69: MOD-GXA Environmental Specifications

	SA STANDARD COMMERCIAL			WA EXTENDED TEMPERATURE			RC RUGGED CONDUCTION-COOLED
Conformal Coating	Optional			Standard			Standard
Cooling Method	Convection			Convection			Conduction
Operating Temperature	0° to +55°C			-20° to +65°C			-40° to +85°C
Storage Temperature	-40°C to +85°C			-45° to +100°C			-50° to +100°C
Vibration Sine (Operating)	20-500 Hz - 2g Acceleration / Frequency Range			20-500 Hz - 2g Acceleration / Frequency Range			22-2,000 Hz - 5g Acceleration / Frequency Range
Random	f (Hz)	10	40	100	200	2000	5Hz to 100Hz +3dB/octave 100Hz to 1000Hz 0.1g²/Hz 1000Hz to 2000Hz -6dB/octave
	PSD (g2/Hz)	0.01	0.01	0.0007	0.0007	0.00005	
Shock (Operating)	20g/11 ms Peak Accel./ Shock Duration Half Sine			20g/11 ms Peak Accel./ Shock Duration Half Sine			40g/20 ms Peak Accel./ Shock Duration Half Sine
Altitude (Operating)	-1,500 to 60,000 ft			-1,500 to 60,000 ft			-1,500 to 60,000 ft
Relative Humidity	90% non-condensing			95% non-condensing			95% non-condensing

7.5 MTBF

Table 70: MOD-GXA MTBF Data

	GB			NS		ARW	AIC	
	25°C	40°C	55°C	25°C	40°C	55°C	40°C	55°C
MTBF (hours)	1 139 100h	890 000h	673 300h	230 300h	178 050h	33 500h	157 250h	157 250

7.6 Power Supply

7.6.1 Power Supplies

MOD-GXA requires +5VDC and +3.3VDC power rail that are provided by VM605x board and available from Front IO connector.

7.6.2 Electrical Consumption

Following tables indicate current and power consumption and test condition for MOD-GXA (5V or 3.3V).

VOLTAGE	5V	3.3V
RESULT	200 mA	400 mA

INTERFACE	CURRENT DRAW
HDMIB	50 mA 5V
HDMID	50 mA 5V

8 / VM605x-RC - Characteristics

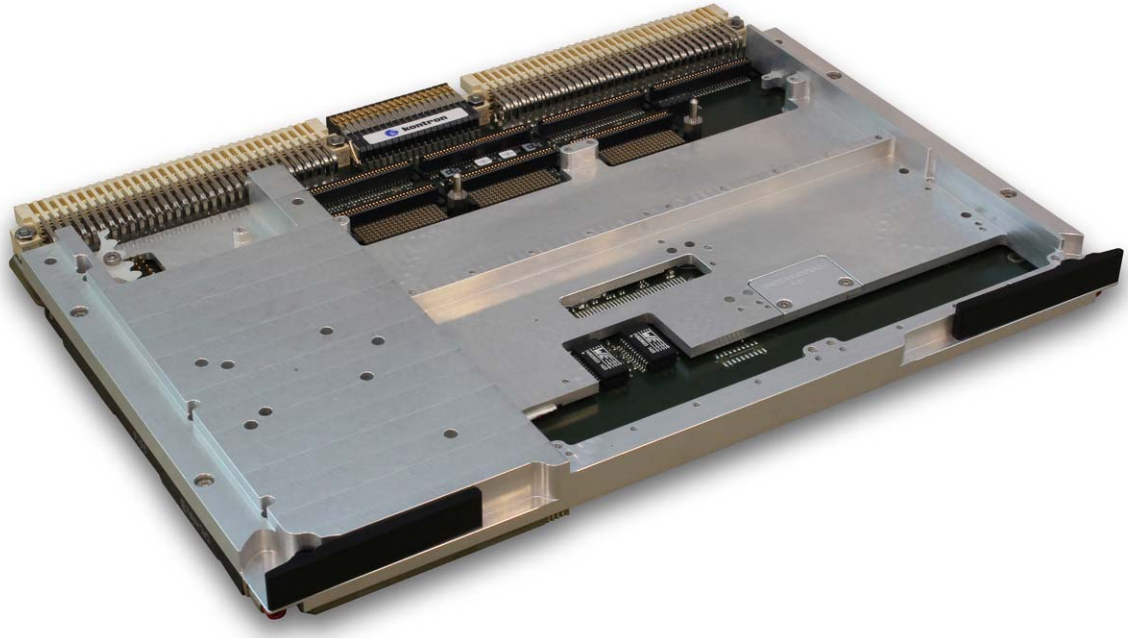
The VM605x-RC boards use "The Ruggedizer", a Kontron proven technology to meet the requirements for harsh environments. With an operational temperature range from -40° C up to +85° C for VM6052-RC and an operational temperature range from -40° C up to +70° C for VM6054-RC and its mechanical environmental performances, the VM605x-RC are designed for severe environmental applications with high levels of shock and vibration, small space envelope and restricted cooling such as required in military, marine, avionics, sheltered and industrial applications.

Table 71: VM605x-RC Order Code

PRODUCT	ORDER CODE	DESCRIPTION
VM6054-RC	VM6054-RC48-x0110000	6U single slot 4 HP (0,8") VME SBC 2.1 GHz Intel® quad-core Core i7 3612QE processor, 8 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, 3 GPIOSs on P0, Conduction Cooled (-40°C to +70°C)
VM6052-RC	VM6052-RC28-x0110000	6U single slot 4 HP (0,8") VME SBC 2.2 GHz Intel® dual-core Core i7 3517UE processor, 8 GB dual bank DDR3-SDRAM with ECC, two PMC/XMC slots, 3 GPIOSs on P0, Conduction Cooled (-40°C to +85°C)

X: 0 = no Flash
1 = 8 GB USB Flash

Figure 54: VM605x-RC - Overview



8.1 VM605x-RC Specificities

The VM605x-RC boards have the same features as the VM605x-SA boards, except for the following items which are fully described in associated sections below:

Table 72: VM605x-RC Specificities

FUNCTION	SEE ALSO
Battery Installation	Section 8.3 page 115
Board Identification	Section 8.4 page 118
Environmental Specifications	Section 8.5 page 118
Mechanical Specifications	Section 8.6 page 119
MTBF	Section 8.7 page 120
Peripheral Connectivity	Section 8.8 page 121
PMC/XMC Installation	Section 8.9 page 122
USB Device Installation	Section 8.10 page 124

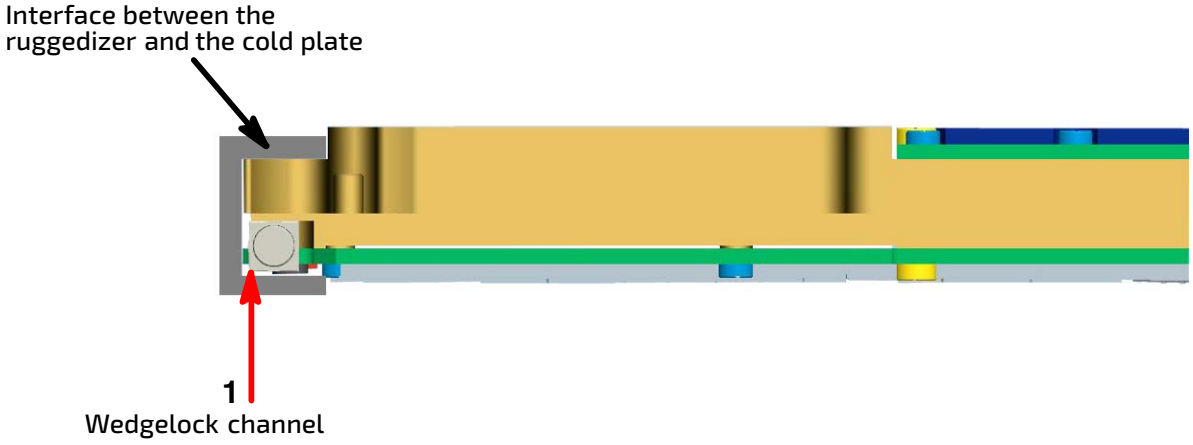
8.2 Frequency Operation

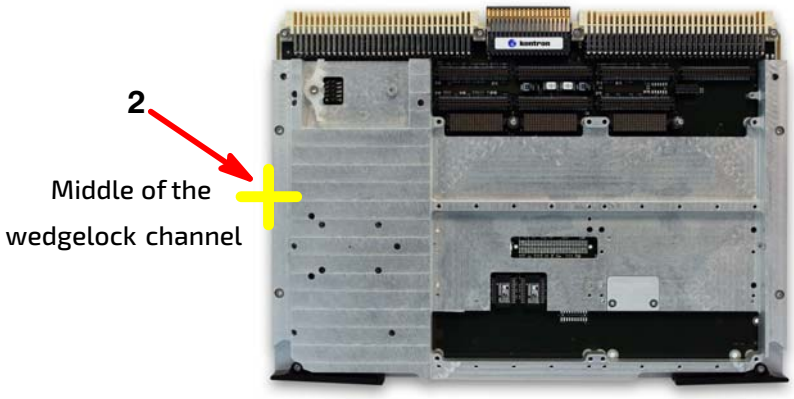
Standard Frequency Operation

The VM6052 processor frequency is set to 1.7 GHz (nominal TDP) and the VM6054 processor frequency is set to 2.2 GHz. With these default settings, the VM605x processing performance is guaranteed across the whole operating temperature range. The VM605x thermal design is such as the processor, running at these default frequencies does not enter thermal management mode (frequency throttling) when the wedgelock temperature is maintained within the approved operating range.

CAUTION: The standard operating range is -40° to +85°C for a VM6052-RC and -40° to +70°C for a VM6054-RC. The card edge temperature check point is measured as follows: the middle point in the wedgelock channel on the ruggedizer. The wedgelock channel is the channel between the edge of the ruggedizer and the cold wall of the rack. Refer to arrows numbers 1 and 2 in following pictures.

Figure 55: Measuring the Temperature





According to ANSI/VITA 47 standard, the plug-in unit edge surface temperature is measured on the plug-in unit.

BOARD	TEMPERATURE OPERATING RANGE	PROCESSOR FREQUENCY	MAX CPU LOAD	MAX CPU LOAD
VM6052	-40°C / +85°C	1.7GHz	80%	Default settings
	-40°C / +70°C	2.2GHz	100%	
VM6054	-40°C / +70°C	2.1GHz	100%	Default settings
	-40°C / +85°C	1.2GHz	< 50%	Not recommended settings

Higher Frequency Operation

The processor upper frequency limit of VM6052-RC can also be set to 2.2 GHz so as to get increased computing performance. In this case, the highest operating temperature on the wedgelock should limited to 70° C.

This will also keep the dual-core processor outside of its thermal management mode.

To modify the VM6052 processing frequency, please refer to the section 4.5 “CPU PPM Configuration" of VM6052/VM6054 AMI-BIOS User Manual (SD.DT.G34).

- **Exceeding the limits will lock the board**

  Operating the processor at 1.2 GHz of VM6054 and allowing the wedgelock temperature to reach 85°C is tempting, but the board behaviour cannot be guaranteed. Even if the CPU chip may adapt quickly to the situation with frequency reduction, this shall not be recommended.

8.3 Battery Installation

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer (Rayovac BR1225X-RA).

Compared with the VM605x/SA boards, an additional cover is added on the battery in order to satisfy the shock and vibration constraints.

To replace the battery, proceed as follows:

- Turn off power and remove the board from the rack.
- Unscrew the two flat head screws (FX-M2x3) that maintain the cover in position, and remove the cover.
- Use a thin plastic tool to push the battery outside the safety cache. Push from the right or left top side of the safety cache.
- Remove the battery.
- Place the new battery in the socket.

- Make sure that you insert the battery the right way round. The plus pole must be on the top!
- Make sure the insulator under the cover is in good condition, otherwise contact your Kontron representative.
- Put back the cover and screw back the two flat head screws (FX-M2x3) applying a torque of 0.138 Nm (1.221 Lb-In).
- Secure the two screws with a drop of Loctite 222.

⚠CAUTION

Danger of explosion when replacing with wrong type of battery. Replace only with the same or equivalent type recommended by the manufacturer. The lithium battery type must be UL recognized.

Do not dispose of lithium batteries in general trash collection. Dispose of the battery according to the local regulations dealing with the disposal of these special materials, (e.g. to the collecting points for dispose of batteries).

Reference of the battery used on the VM605x: RAYOVAC BR1225X-RA
The design of an electronic circuit powered by a component class battery requires the designer to consider two interacting paths that determine a battery's life: consumption of active electrochemical components and thermal wear-out.

Battery Life

Figure 56 gives an estimate of years of service at various discharge currents for BR Lithium coin cells at room temperatures. The RTC circuit power consumption is specified at 500 nA, giving an expected duration of more than 10 years in the absence of external power. In case of storage temperature or operating temperature is higher than 55°C or lower than 0°C, the battery life is reduced to 7 years in worst case.

Figure 56: Battery Life

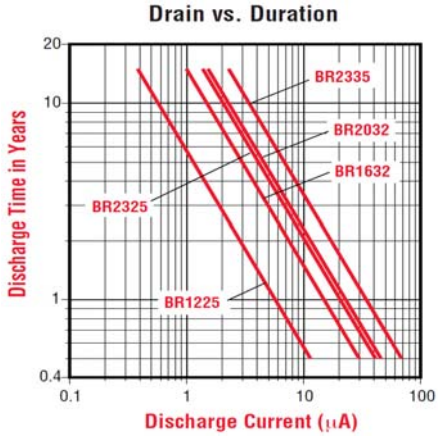
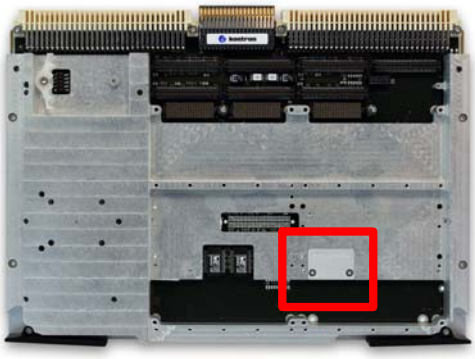
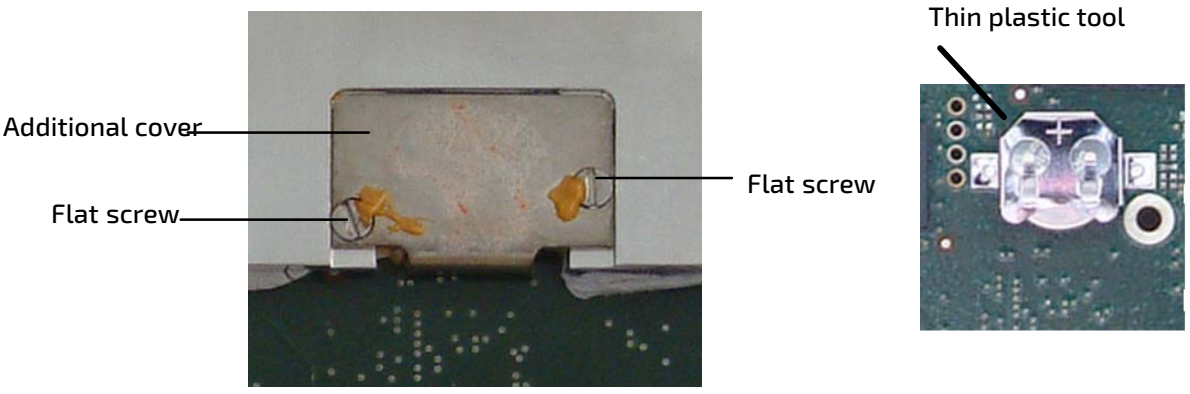


Figure 57: Battery Installation on VM605x-RC





8.4 Board Identification

The VM605x-RC boards are identified by labels fitted to the bottom side. These labels are at the same location and have the same meaning (except the "Board Identification" label) as the VM605x/SA boards labels (refer to the section 2.2 page 20 for more information).

8.5 Environmental Specifications

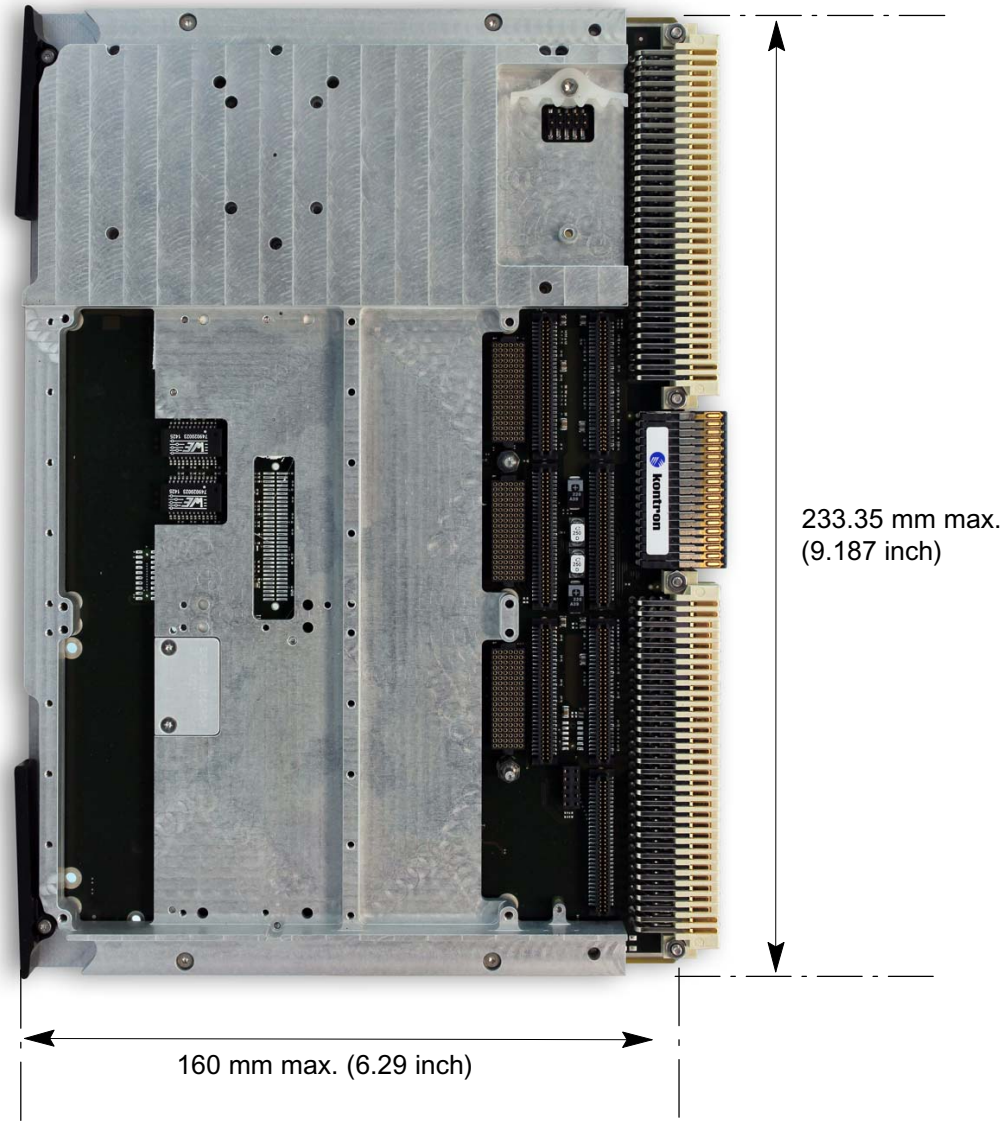
Table 73: VM605x-RC Environmental Specifications

	VM6052-RC RUGGED CONDUCTION-COOLED	VM6054-RC RUGGED CONDUCTION-COOLED
Conformal Coating	Standard	Standard
Cooling Method	Conduction	Conduction
Operating Temperature	-40°C to +85°C at 1.7 Ghz -40°C to +70°C at 2.2 Ghz	-40°C to +85°C at 1.2 Ghz (not recommended) -40°C to +70°C at 2.2 Ghz
Storage Temperature	-50° to +100°C	-50° to +100°C
Vibration Sine (Operating)	20-2,000 Hz - 5g Acceleration / Frequency Range	20-2,000 Hz - 5g Acceleration / Frequency Range
Random	5Hz to 100Hz +3dB/octave 100Hz to 1000Hz 0.1g^2/Hz 1000Hz to 2000Hz - 6dB/octave	5Hz to 100Hz +3dB/octave 100Hz to 1000Hz 0.1g^2/Hz 1000Hz to 2000Hz - 6dB/octave
Shock (Operating)	40g/20 ms Peak Accel./Shock Duration Half Sine	40g/20 ms Peak Accel./Shock Duration Half Sine
Altitude (Operating)	-1,500 to 60,000 ft	-1,500 to 60,000 ft
Relative Humidity	95% non-condensing	95% non-condensing

8.6 Mechanical Specifications

The VM605x-RC boards are build on a multi-layer double Eurocard and conforms to the dimensions specified in the ANSI/VITA VME64 1-1994. The dimensions shown below are in millimeters, with inches (in parentheses) for general guidance only.

Figure 58: VME Dimensions



- **Length:** 233.35 mm max.
- **Depth:** 160 mm max.
- **Height:** 1 VME slot compatible
- **Weight:** ~800 g (approximatively)

8.7 MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

Table 74: VM6052-RC MTBF Data

	GB		AIC	NS		ARW
	25°C	40°C	40°C	25°C	40°C	55°C
MTBF (hours)	403 200h	71 500h	40 450h	70 600h	55 800h	9 470h

Table 75: VM6054-RC MTBF Data

	GB		AIC	NS		ARW
	25°C	40°C	40°C	25°C	40°C	55°C
MTBF (hours)	396 500h	312 550h	39 850h	69 400h	54 950h	9 360h

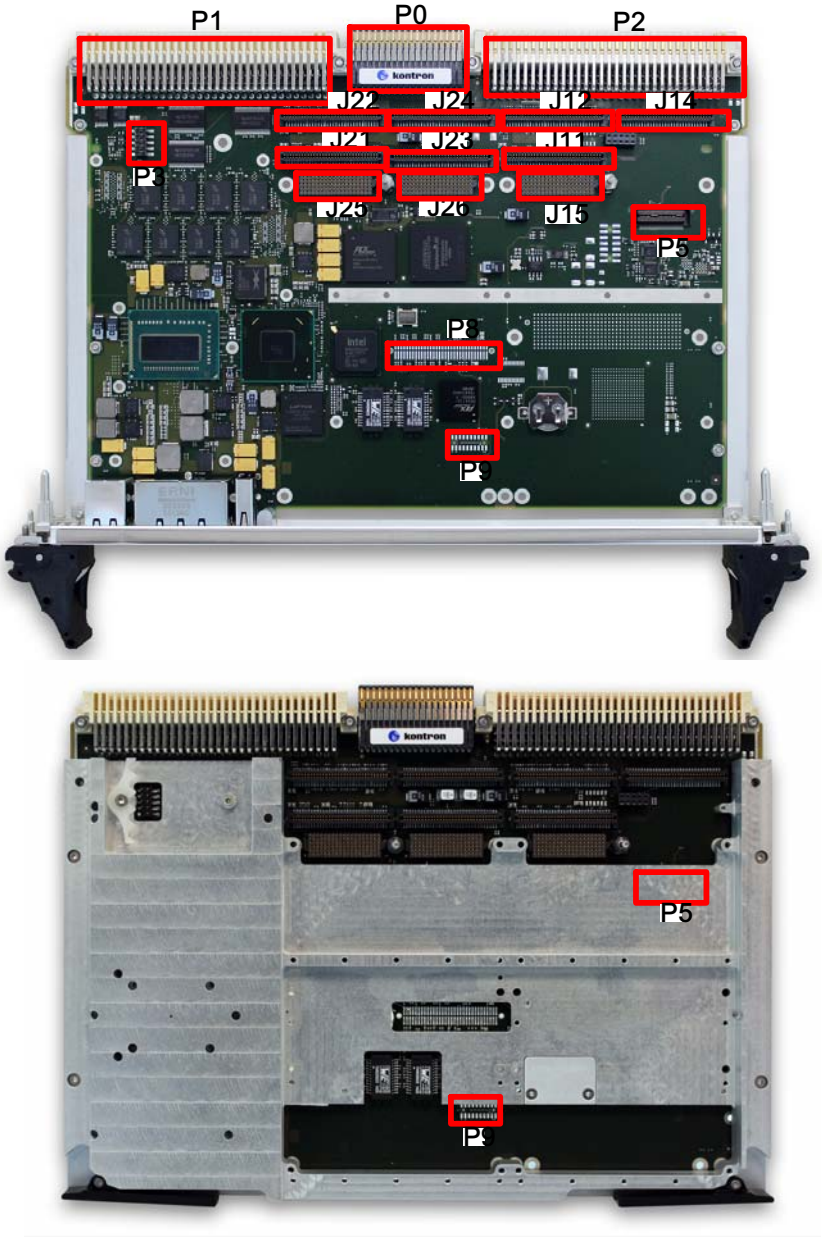
8.8 Peripheral Connectivity

The VM605x-RC board features the same connectors as the VM605x/SA except that:

- the front panel connectors are absent (serial lines COM1/COM2 are always routed to P2 on the rugged conduction-cooled board), ETH0 and ETH1 are no more available, only ETH2 and ETH3 are usable through rear P0 connector.
- the P5 and P9 onboard connectors are not fitted on the VM605x/RC board.

For detailed information about the connectors located on the VM605x, refer to section 4.2 page 50 "Onboard Connectors".

Figure 59: VM605x-RC Peripheral Connectivity



8.9 PMC/XMC Installation

Standard Anchorage Points

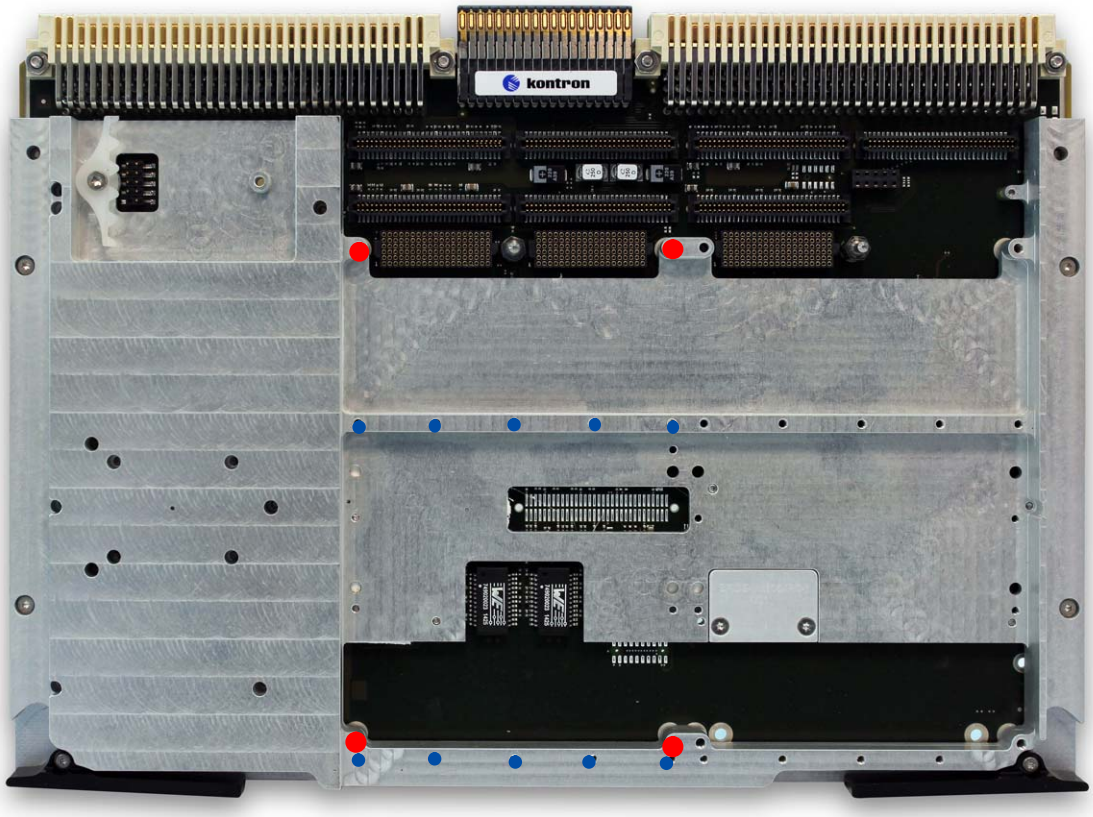
Install the XMC/PMC (for example XMC-ETH2-RC) to the VM605x-RC according to the following steps.

1. Check that the standoffs are attached to the XMC/PMC. Align the standoffs and the holes at the front, the middle and the rear of the PMC with the matching holes on the VM605x-RC board.
2. Lower the XMC/PMC component side down, fitting the mezzanine board connectors into their mating connectors on the VM605x-RC. Press them together so that the friction from the pins holds the mezzanine board in place.
3. Screw the XMC/PMC in place using mounting screws (5+2 at the front of the board, 5 in the middle of the board and 2 at the rear of the board). Tighten with a torque of 0.383 N.m. (3.389 Lb-In). Figure 60 shows the location of the standard anchorage points on an VM605x-RC board.

The PMC Installation Fastenings Kit is delivered with the VM605x-RC board. For each PMC location, it includes:

- 4x VIS-CZX-M2.5X6-INOX For the PMC assembly on the board red marks below
- 10x VIS-CZX-M2X6-INOX For PMC assembly on the board blue marks below

Figure 60: Standard Anchorage Points on VM605x-RC Board



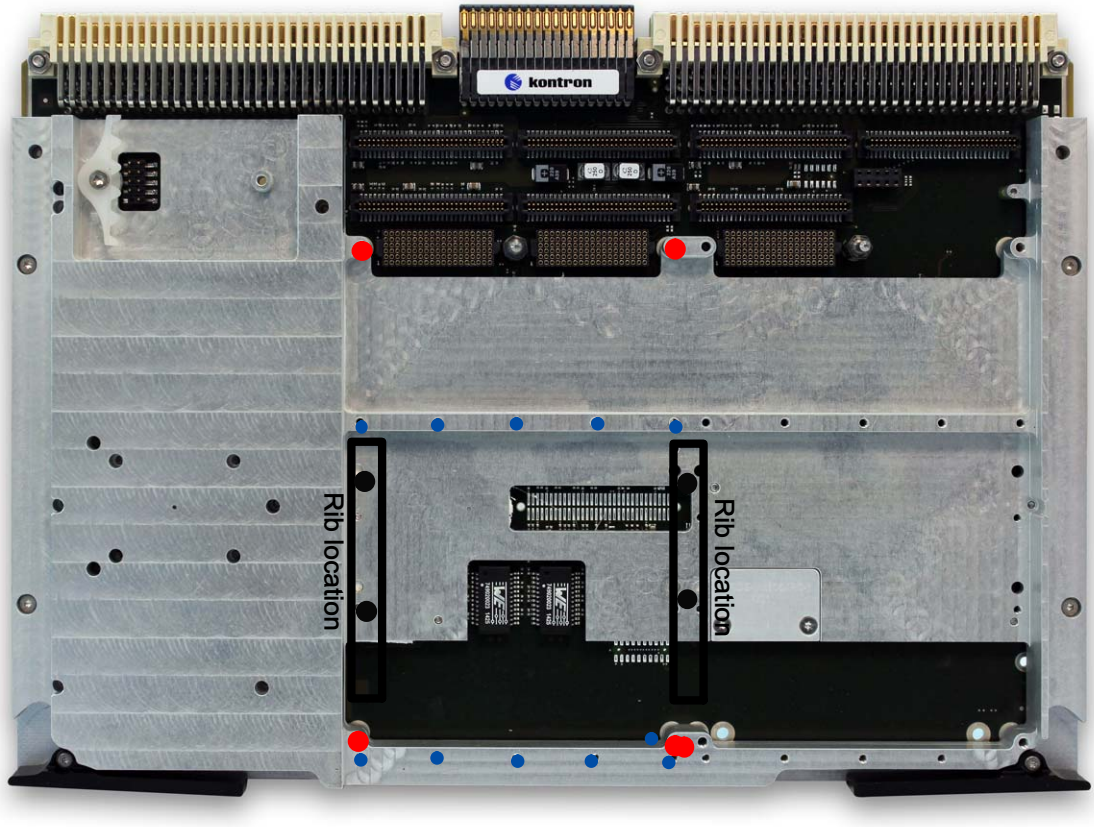
Fastenings Kit

An optional secondary thermal interface ribs should be used to get the specified module thermal performance.

Order Code: KIT-RIBPMC1V01-1

2x RIB-PMC-1-V01	Two additional ribs	
4x VIS-CZX-M2X5-INOX	For the ribs assembly on the board	black marks below
10x VIS-CZX-M2.5X6-INOX	For the PMC assembly on the ribs (6x) For the PMC assembly on the board (4x)	red marks below
10x VIS-CZX-M2X6-INOX	For PMC assembly on the board	blue marks below

Figure 61: Usage of Fastenings Kit Ribs on VM605x-RC Board



8.10 USB/SATA Device Installation

The fastenings kit is delivered with the board, it includes:

- 1x screws CZX-M2.5X5 P3 side

Figure 62: USB Device Location on VM605x-RC

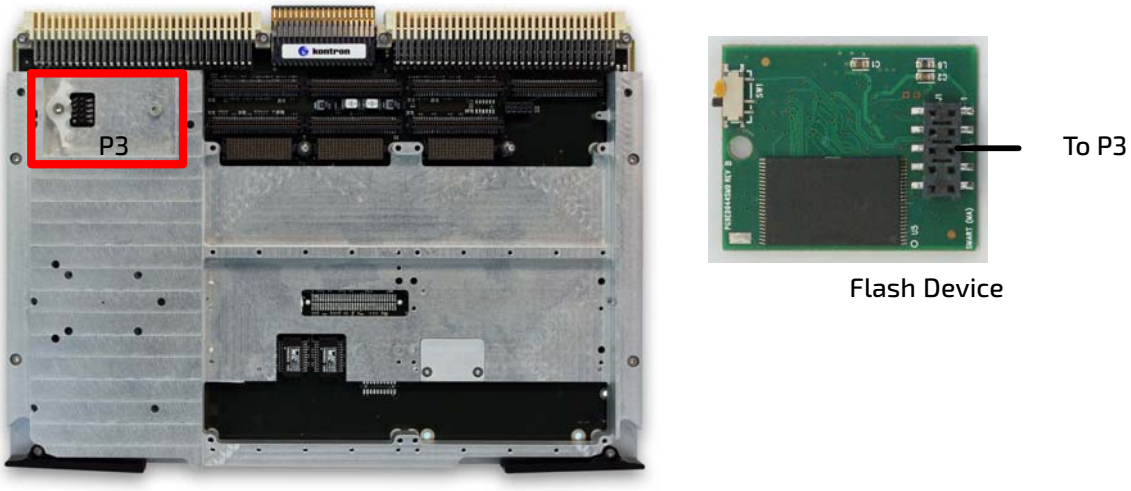
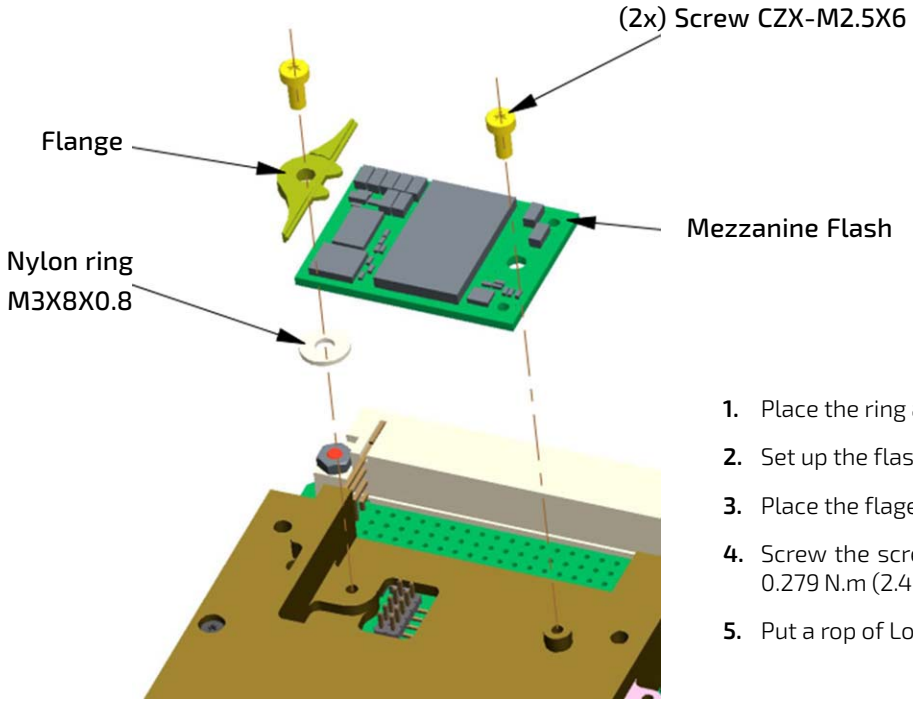


Figure 63: USB Device Installation on VM605x-RC



1. Place the ring as indicated on the left picture
2. Set up the flash device using P3 connector
3. Place the flage
4. Screw the screws CZX-M2.5X5 using a troque of 0.279 N.m (2.469 Lb-In)
5. Put a rop of Loctite 222 on the screws head.

8.11 Inserting and Removing the Board

Inserting the Board

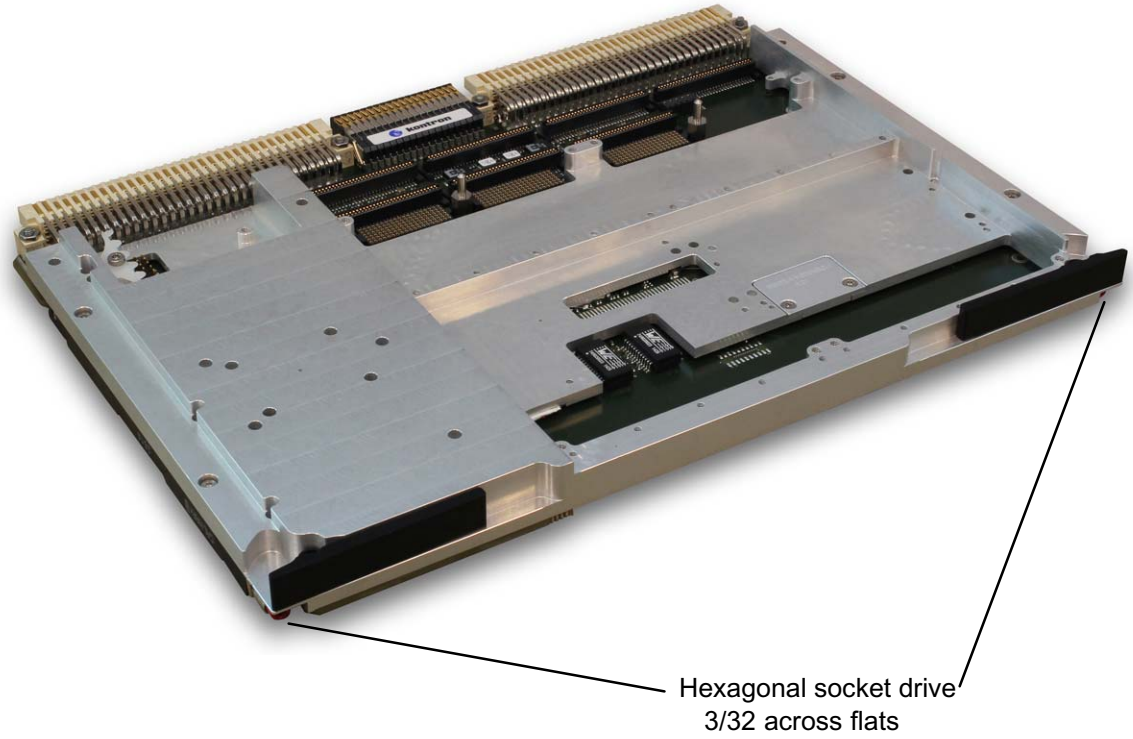
1. Insert the board into the backplane of the rack.
2. Screw both hexagonal socket drive 3/32 across flats with a 3/32 Allen wrench.

Conduct the installation using a torque spanner with a recommended torque of 0.9N.m (7.96 Lb-In)

Removing the Board

1. Unscrew both hexagonal socket drive 3/32 across flats with a 3/32 Allen wrench.
2. Remove the board from the backplane of the rack.

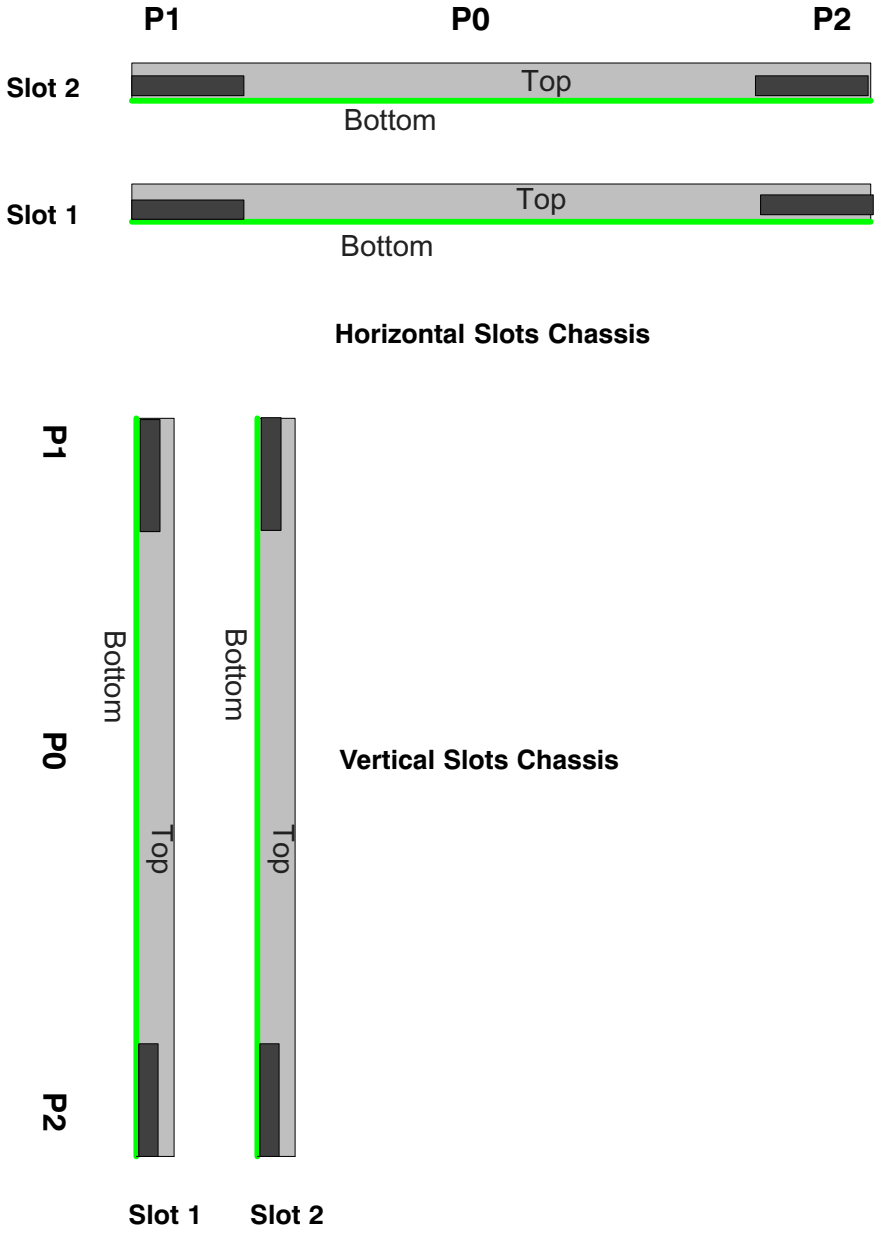
Figure 64: VM605x-RC - Inserting the Board



Do not touch the ruggedizer while removing the board from a rack because it can get very hot.
Do not place the board on any surface or in any form of storage container until the board and its heatsink have cooled down to room temperature.

Depending on the chassis type (horizontal slots or vertical slots), make sure to insert the board correctly, as shown below:

Figure 65: VM605x-RC - Slots Orientation



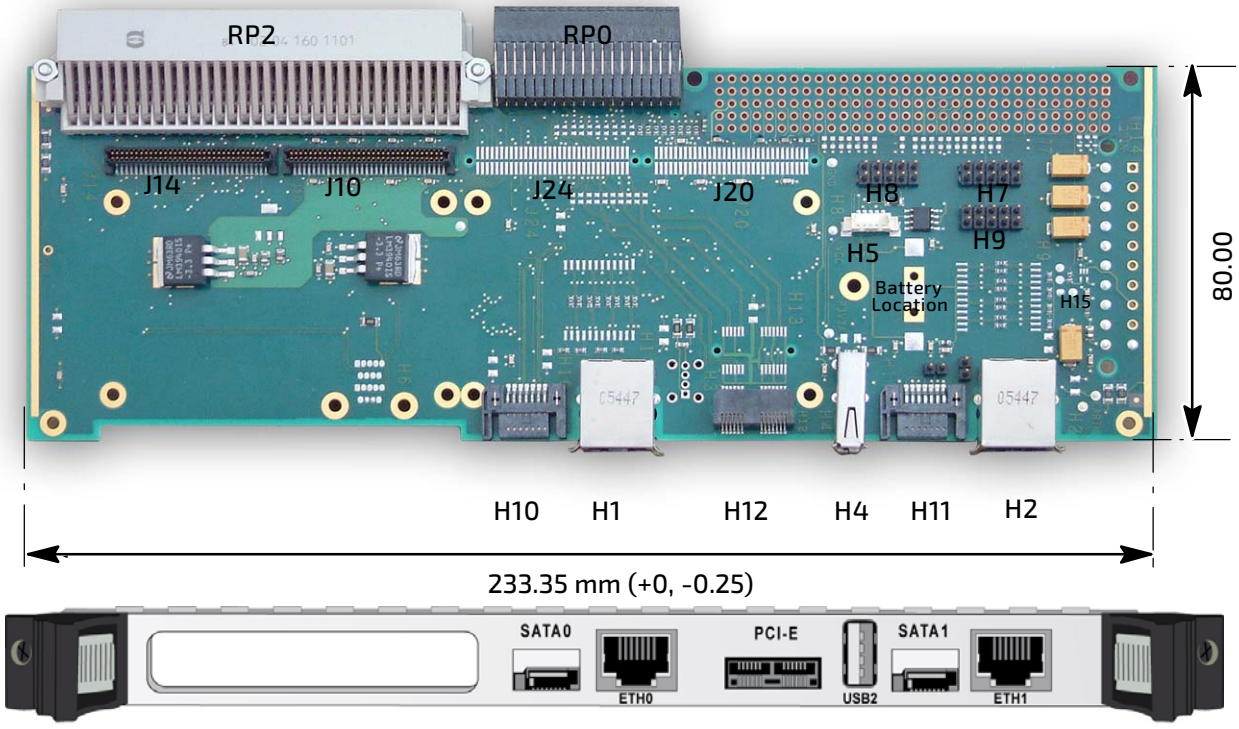
9 / VM605x-RTM Characteristics

The VM605x-RTM (Order Code: PBV36-P0-VM6-00 rear transition module is compliant to PMC I/O Module Standard VITA 36 - 199x Draft 0.1 July 19, 1999 (mechanical and PIM format).

The main functionalities of the VM605x-RTM rear transition module are:

- Two 10/100/1000BASE-T Ethernet interface, **H1** and **H2** connectors on Figure 66
- One USB connector, **H4** on Figure 66
- One SMB connector, **H5** on Figure 66
- Two Serial lines ports available on two HE10 connectors (**H7**, **H8** on Figure 66)
- Three GPIOs signals available through an HE10 connector, **H9** connector on Figure 66
- Two Serial ATA connectors, **H10** and **H11** connector on Figure 66
- One PCI Express connector, **H12** connector on Figure 66
- PMC Site 1[64:1] I/O routed to **J14[32:1]** connector from RP2 connector
- PMC Site 2[64:1] I/O routed to **J24[32:1]** connector from RP2 connector (only on PBV36-P0-VM6-00 Rev. C)

Figure 66: PBV36-P0-VM6-00 Module Overview



9.1 Installation of the Rear Transition Module

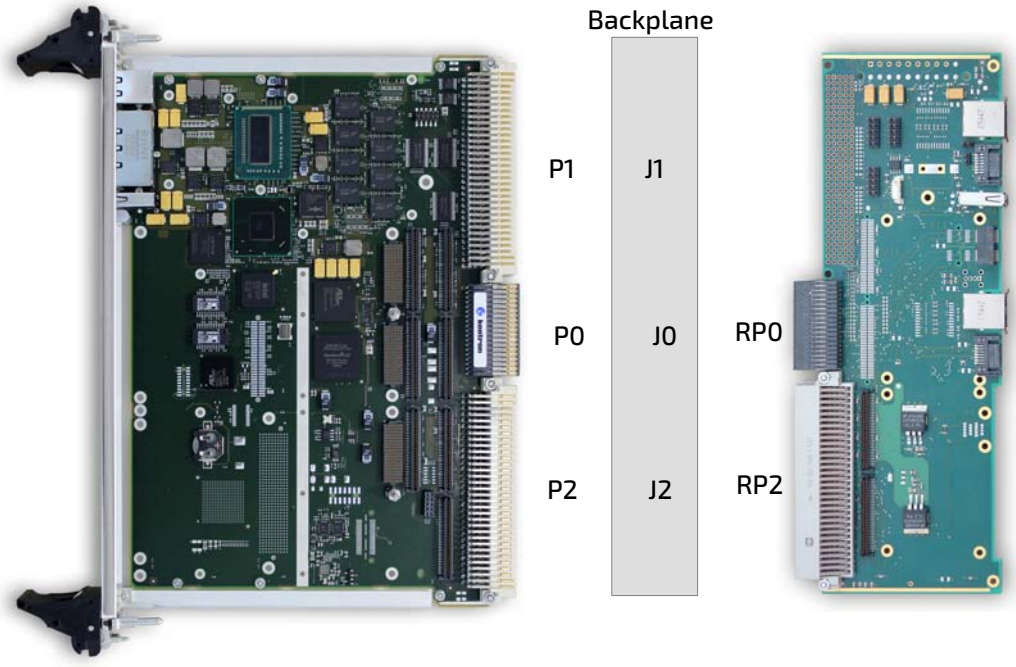
The VM605x-RTM module is designed to be used with a VME64 extensions backplane. Each slot in the backplane contains two 160-pin connectors and one connector with 95 user-defined pins. The top connector in each slot is designed J1, the middle connector is J0 and the bottom connector is J2.

The VM605x rear transition module plugs into the J0, J1 and J2 connectors, on the back side of the VMEbus backplane, in the same slot as the VM605x board (see Figure 67).

To install the rear transition module:

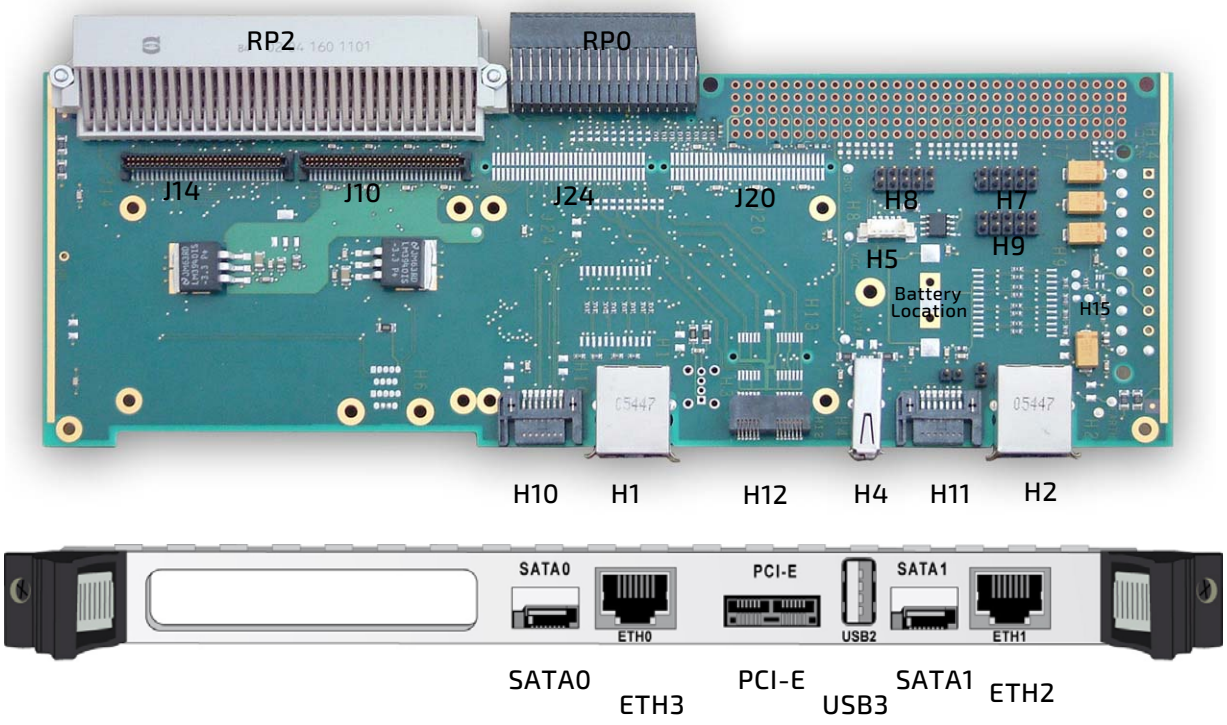
1. Make sure the system and peripheral equipment power are off.
2. Install the cables into the appropriate connectors on the transition module (see section 9.2 page 129).
3. Line-up the RP0 and RP2 connectors (also named P0 and P2 in this chapter) on the rear transition module with the J0 and J2 connectors on the backplane.
4. Press the outer edge of the transition module until the board is firmly seated in the connector.
5. Connect any additional cables.
6. Turn on system power.

Figure 67: Installing the VM605x-RTM



9.2 Connectors

Figure 68: VM605x-RTM Connectors Location



9.2.1 RP0 Connector Pin Assignment

The RP0 connector has the same pin assignment as the P0 connector of the VM605x board.

Refer to the "VME Bus Interface - P0 Connector" in section 4.3.1 page 54 for a complete information about the pin assignments of the RP0 connector.

9.2.2 RP2 Connector Pin Assignment

The RP2 connector has the same pin assignment as the P2 connector of the VM605x board.

Refer to the "VME Bus Interface - P2 Connector" in section 4.3.3 page 60 for a complete information about the pin assignments of the RP2 connector.

9.2.3 H1 (ETHERNET 3) & H2 (ETHERNET 2) - Gigabit ETHERNET Connector

Routed from P0 to **H1** and **H2**, RJ-45 connectors (AMP - Part Number 106066-2).

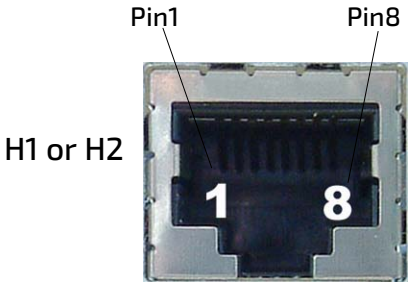
Ethernet port 3 and 2 are respectively available through the **ETH0** and **ETH1** RTM front panel connectors.

Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	BI_DA+	2	BI_DA-
3	BI_DB+	4	BI_DC+ (*)
5	BI_DC- (*)	6	BI_DB-
7	BI_DD+ (*)	8	BI_DD- (*)
9	Chassis Ground		

(*) : In 10BASE-T or 100BASE-T these signals are not used.

Type of Connector



Signal Description

MNEMONIC	SIGNAL DESCRIPTION
BI_DA+/-	In 1000BASE-T: First pair of Transmit/receive data In 10BASE-T/100BASE-T: Pair of Transmit data
BI_DB+/-	In 1000BASE-T: Second pair of Transmit/receive data In 10BASE-T/100BASE-T: Pair of Receive data
BI_DC+/-	In 1000BASE-T: Third pair of Transmit/receive data In 10BASE-T/100BASE-T: Unused.
BI_DD+/-	In 1000BASE-T: Fourth pair of Transmit/receive data In 10BASE-T/100BASE-T: Unused.

9.2.4 H4 (USB3) - USB Connector

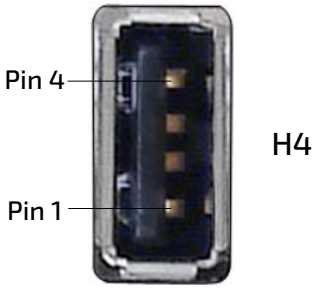
Routed from P0 to **H4**, a vertical USB connector.

Available through the **USB** RTM front panel connectors.

Connector Pin Assignment

PIN	SIGNAL
1	+5 V Fused
2	USB3 DATA-
3	USB3 DATA+
4	GND
CASE	M GND

Type of Connector



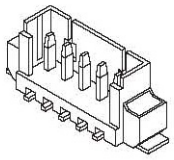
9.2.5 H5 - SMB Connector

Routed from P1 to **H5** (MOLEX - Part Number 53398-0590)

Connector Pin Assignment

PIN	SIGNAL
1	SMB_SCL
2	GND
3	SMB_SDA
4	N.C.
5	SMB_ALERT#

Type of Connector



H5

Signal Description

MNEMONIC	SIGNAL DESCRIPTION
GND	Ground
N.C.	Not Connected
SMB_ALERT	System Management Bus - Alert
SMB_SCL	System Management Bus - Serial clock line from the SMBus master to SMBus slave devices.
SMB_SDA	System Management Bus - Bi-directional serial data line between the SMBus master and the SMBus slave device.

9.2.6 H7 (S0/COM1) & H8 (S1/COM2) - SERIAL Connector

Routed from P2 to **H7** and **H8**; individual 10-pin HE10 connectors

A serial line should only be used via one connector at the same time, either the Serial front panel connector or the P2 connector.

H7 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	S0_DCD	2	S0_RX
3	S0_TX	4	S0_DTR
5	GND	6	S0_DSR
7	S0_RTS	8	S0_CTS
9	N.C.	10	N.C.

H8 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	S1_DCD or GPIO4	2	S1_RX
3	S1_TX	4	S1_DTR or GPIO6
5	GND	6	S1_DSR or GPIO5
7	S1_RTS	8	S1_CTS
9	N.C.	10	N.C.

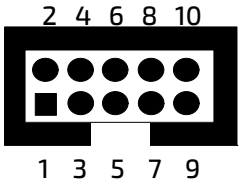
GPIO on connector H8 are an option of the VM605x board.

Signal Description

MNEMONIC	SIGNAL DESCRIPTION
CTS	Channel EIA-232 x Clear to Send
DCD	Channel EIA-232 x Data Carrier Detect
DSR	Channel EIA-232 x Data Set Ready
DTR	Channel EIA-232 x Data Terminal Ready
GND	Ground
GPIO*x*	GPIO *x* from CPLD
N.C.	Not Connected
RTS	Channel EIA-232 x Request to Send
S*x*_RX	Channel EIA-232 *x* Receive Data
S*x*_TX	Channel EIA-232 *x* Transmit Data

Type of Connector

Right angle HE10 10-pin connector, male, with board lock.



H7 & H8

The H7 and H8 connectors can be connected via a NULL MODEM adapter on a VT100 console.

9.2.7 H9 - GPIOs and MISC Signals

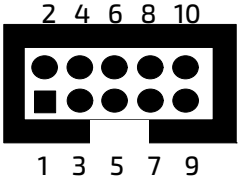
Routed from P0 to **H9**; individual 10 pins HE10 connector.

Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	GPIO1	2	N.C.
3	GPIO2	4	N.C.
5	GPIO3	6	N.C.
7	N.C.	8	GND
9	N.C.	10	GND

Type of Connector

Right angle HE10 10-pin connector, male, with board lock.



H9

Signal Meaning

MNEMONIC	SIGNAL DESCRIPTION
GPIO*x*	GPIO *x* from cPLD
GND	Ground
N.C.	Not Connected

9.2.8 H10 (SATA0) and H11 (SATA1) - Serial ATA Connector

Routed from P0 to **H10** and **H11**; SATA connector, right angle version with metal latch (`MOLEX` - Part Number `47080-4001`)

Available through the **SATA0** and **SATA1** RTM front panel connectors.

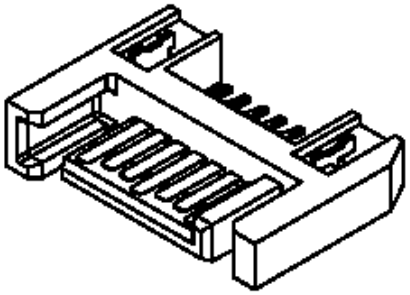
Depending on the SATA manufacturing option of the associated VM605x board:

- Two SATA devices are available through the SATA0 and SATA1 RTM front panel connectors: SATA on P0 manufacturing option.
- Only one SATA device is available through the SATA0 RTM front panel connectors: SATA onboard manufacturing option.

Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	SATA*x* TX+
3	SATA*x* TX-	4	GND
5	SATA*x* RX-	6	SATA*x* RX+
7	GND		

Type of Connector



Signal Description

MNEMONIC	SIGNAL DESCRIPTION
GND	Ground
SATA*x* RX+/RX-	Serial ATA *x* Receive +/-
SATA*x* TX+/TX-	Serial ATA *x* Transmit +/-

9.2.9 H12 - PCI Express Connector

Routed from P0 connector to **H12**, a 26-pin right angle connector (`SAMTEC` - Order Code `MEC8-RA`)

Available through the **PCI-E** RTM front panel connectors.

Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	GND
3	PEX RXL0+	4	PEX TXL0+
5	PEX RXL0-	6	PEX TXL0-
7	GND	8	GND
9	PEX RX1L+	10	PEX TXL1+
11	PEX RXL1-	12	PEX TXL1-
13	GND	14	GND
15	PEX RXL2+	16	PEX TXL2+
17	PEX RXL2-	18	PEX TXL2-
19	GND	20	GND
21	PEX RXL3+	22	PEX TXL3+
23	PEX RXL3-	24	PEX TXL3-
25	GND	26	GND

Type of Connector

Signal Meaning

MNEMONIC	SIGNAL DESCRIPTION
PEX RXL[0..3]+/-	x4 PCI Express Link - Differential Receive Lane [0..3]
PEX TXL[0..3]+/-	x4 PCI Express Link - Differential Transmit Lane [0..3]
GND	Ground

Known Limitations

The P0 to P0 connection using CABL-ZPACK-X4-022 cable is recommended when connecting VM605x and V2PMC2. See "V2PMC2 User's Guide" - section 6.4.1.

9.2.10 PCI 64 PIM Site 1 Connector

J14 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	PMC64 IO 01	2	PMC64 IO 02
…		…	
61	PMC64 IO 61	62	PMC64 IO 62
63	PMC64 IO 63 or GPIO7 (*)	64	PMC64 IO 64 or GPIO8 (*)

(*) depending on VM605x build option.

Signal Description

MNEMONIC	SIGNAL DESCRIPTION
PMC64 IO *xx*	I/O 01 through 64 of the motherboard PMC: J14[01 ... 64] for PMC Site 1
GPIOx	GPIOx from CPLD
N.C.	Not Connected

Known Limitations

- 4.8 mm high components have been placed under PIM site 1. This trangresses the VITA 36 standard which specifies 2.5 mm. Some PIMs may not fit in this site.

J10 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	N.C.	2	N.C.
3	N.C.	4	N.C
5	+5V	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	+3.3V
11	N.C.	12	N.C.
13	GND	14	N.C.
15	N.C.	16	N.C.
17	N.C.	18	GND
19	N.C.	20	N.C.
21	+5V	22	N.C.
23	N.C.	24	N.C.
25	N.C.	26	+3.3V
27	N.C.	28	N.C.
29	GND	30	N.C.
31	N.C.	32	N.C.
33	N.C.	34	GND
35	N.C.	36	N.C
37	+5V	38	N.C.
39	N.C.	40	N.C.
41	N.C.	42	+3.3V
43	N.C.	44	N.C.
45	GND	46	N.C.
47	N.C.	48	N.C.
49	N.C.	50	GND
51	N.C.	52	N.C.
53	+5V	54	N.C.
55	N.C.	56	N.C.
57	N.C.	58	+3.3V
59	N.C.	60	N.C.
61	N.C.	62	N.C.
63	N.C.	64	N.C.

9.2.11 PCI 64 PIM Site 2 Connector

Up to PBV36-P0-VM6-00 Rev. C, the pinout of J20 and J24 connectors is reserved. If available, do not try to use these connectors.

From PBV36-P0-VM6-00 Rev. C, the pinout of the J20 and J24 connectors is available. See sections J24 and J20 Connector Pin Assignment below.

Installation of a PIM on the Site 2 of a PBV36-P0-VM6-00 Rev C. requires specific adjustments:

- removing H10 (SATA0), H1 (ETH0) and H12 (PCI-E) connector on the RTM,
- usage of a RTM specific front panel.

Contact your Kontron representative for more information on this topic.

J24 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	PMC64 IO 01	2	PMC64 IO 02
...	...	...	...
63	PMC64 IO 63	64	PMC64 IO 64

Signal Description

MNEMONIC	SIGNAL DESCRIPTION
PMC64 IO *xx*	I/O 01 through 64 of the motherboard PMC: J24[01 ... 64] for PMC Site 2
N.C.	Not Connected

Known Limitations

- The RTM does not include the 3 mm recess at the rear card edge on the area of PIM Site as required by VITA 36 standard. This may require removal or loosening of the rear panel in order to remove and install a PIM at Site 2.

J20 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	N.C.	2	N.C.
3	N.C.	4	N.C
5	+5V	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	+3.3V
11	N.C.	12	N.C.
13	GND	14	N.C.
15	N.C.	16	N.C.
17	N.C.	18	GND
19	N.C.	20	N.C.
21	+5V	22	N.C.
23	N.C.	24	N.C.
25	N.C.	26	+3.3V
27	N.C.	28	N.C.
29	GND	30	N.C.
31	N.C.	32	N.C.
33	N.C.	34	GND
35	N.C.	36	N.C
37	+5V	38	N.C.
39	N.C.	40	N.C.
41	N.C.	42	+3.3V
43	N.C.	44	N.C.
45	GND	46	N.C.
47	N.C.	48	N.C.
49	N.C.	50	GND
51	N.C.	52	N.C.
53	+5V	54	N.C.
55	N.C.	56	N.C.
57	N.C.	58	+3.3V
59	N.C.	60	N.C.
61	N.C.	62	N.C.
63	N.C.	64	N.C.

9.2.12 Reset

The front panel reset toggle switch can be set to the RESET position to generate an hard reset.

9.2.13 Mechanical Ground

One HE10 2-pin connector is placed on the board to allow to hard connect electrical (GND) and mechanical (EARTH) grounds.

While adding a jumper on connector, both ground signals are tighten together.

H15 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	EARTH	2	GND

Signal Meaning

MNEMONIC	SIGNAL DESCRIPTION
EARTH	Electrical Ground
GND	Mechanical Ground

A metalized mechanical hole (3mm diameter) is located on the board to allow to fix an electrical pod in order to bring the mechanical ground from the chassis.

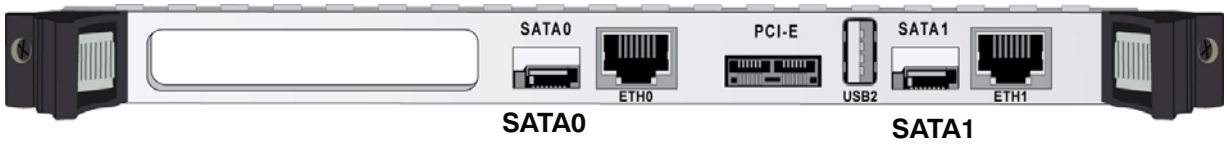
9.2.14 Power Supplies

- Two 800 mAmp voltage regulators are used on the board to provide 3.3V power supply to each PIM site.
- A standard lithium battery to supply CPU board's RTC is also available.

9.3 Cables

9.3.1 SATA Cable

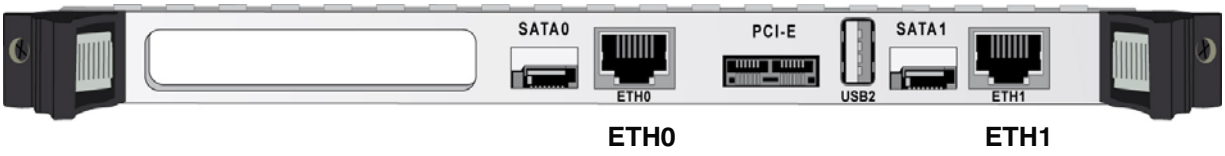
Figure 69: Serial ATA Cable



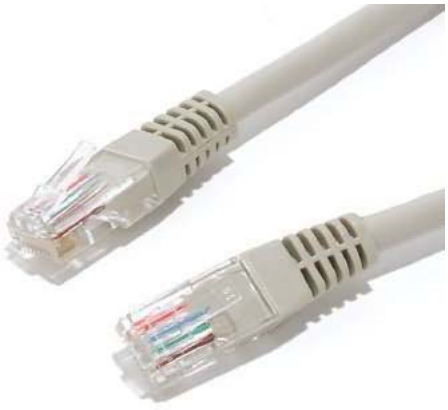
Serial ATA standard cable

9.3.2 Ethernet Cable

Figure 70: Gigabit Ethernet Cable



Gigabit Ethernet standard cable:
1000BASE-T requires category 5e, 5+ or 6 copper cable, with a maximal length of 100m for an UTP or FTP cable, and 150m for a STP or FSTP cable.

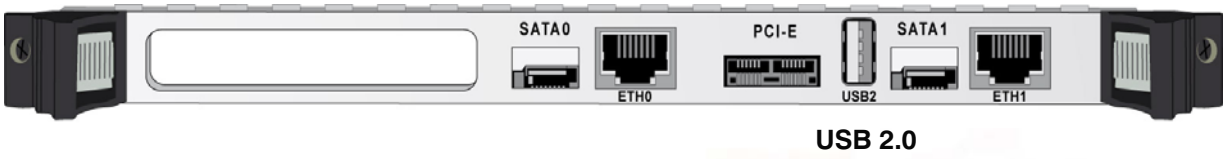


9.3.3 PCI-Express Cable

Please contact your Kontron representative for more information on this topic.

9.3.4 USB 2.0 Cable

Figure 71: USB 2.0 Cable



USB 2.0 standard cable

USB series "A" plug and receptacle

About Kontron - An S&T Company

Kontron is a global leader in IoT/Embedded Computing Technology (ECT). As a part of technology group S&T, Kontron offers a combined portfolio of secure hardware, middleware and services for Internet of Things (IoT) and Industry 4.0 applications. With its standard products and tailor-made solutions based on highly reliable state-of-the-art embedded technologies, Kontron provides secure and innovative applications for a variety of industries. As a result, customers benefit from accelerated time-to-market, reduced total cost of ownership, product longevity and the best fully integrated applications overall.

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