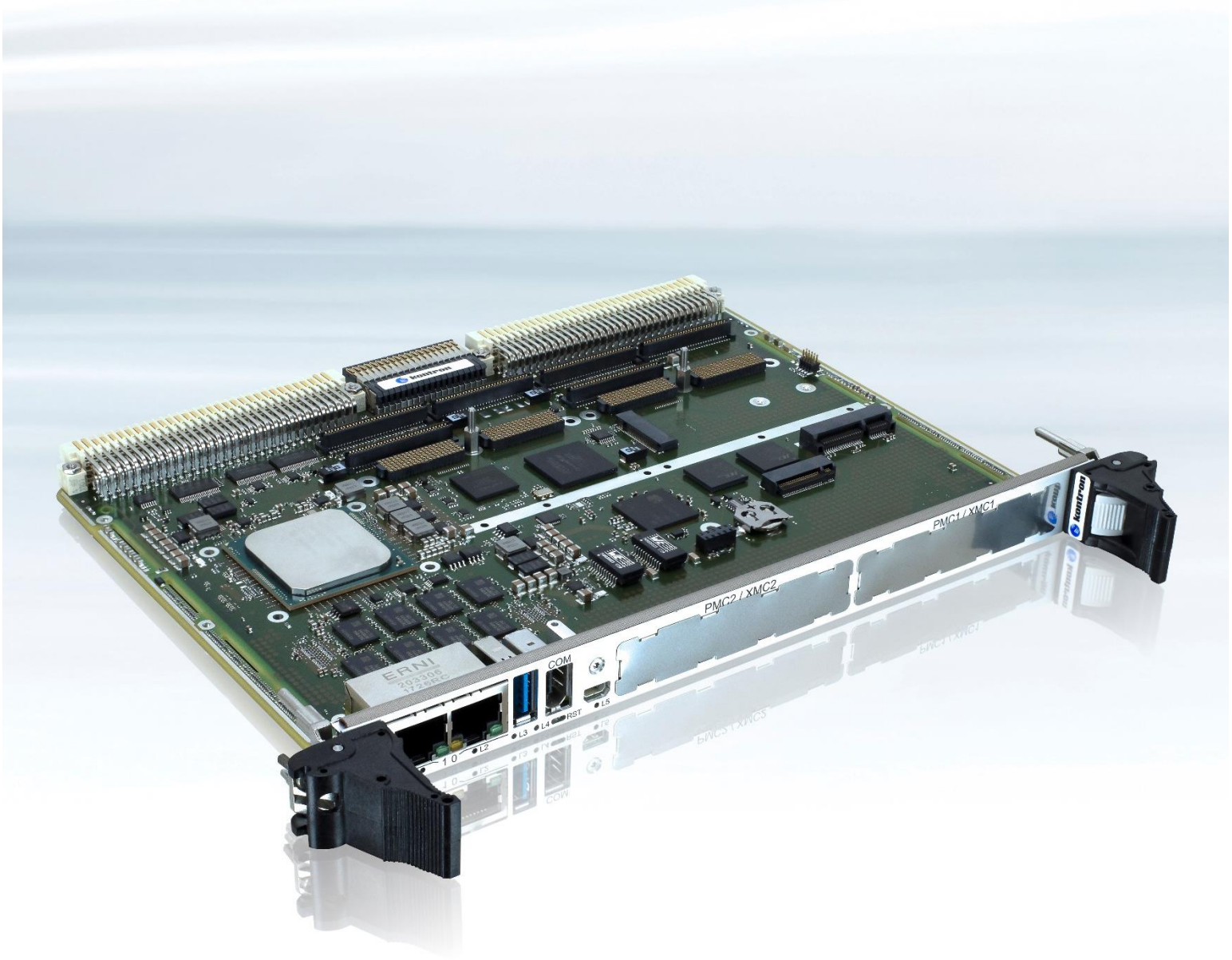
USER GUIDE



VM606x

6U VME Single Board Computer

D206640 - 1.1 - June 2020

VM606x - User Guide

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Kontron S&T AG

Lise-Meitner-Str. 3-5
86156 Augsburg
Germany
www.kontron.com

Revision History

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Revision	Brief Description of Changes	Date of Issue
1.0	Preliminary release	09-2018
1.1	- Chap. 1.2: Table 1 (Related Publications) updated. - Chap. 2.1: Added comment on PBV36-P0-VM6-00 tooling; added RA & RC temperature grades. - Chap. 2.3.1: Table 2 (VM606x Order Codes) updated. - Chap. 2.3.1: Table 3 (Associated Products Order Codes) updated. - Chap. 2.3.2: Table 4 (Coding of the Manufacturing Options) updated. - Chap. 2.3.3 added (P0 part number change) - Chap. 2.4.2 : Table 6 (Rear IOs Distribution) updated. - Chap. 2.6 : Table 7 (VM606x Main Characteristics) updated. - Chap. 2.7 : Table 8 (Environmental Specifications) updated. - Chap. 2.8: Table 9 (Board Weight) updated. - Chap. 2.9: Table 10 (VM606x MTBF Data) - Chap. 3.3 : Package contents updated. - Chap. 3.7.1 : M.2 modules assembly updated. - Chap. 3.7.2 : MiniPCIe/mSATA card assembly updated. - Chap. 3.7.3: Battery replacement updated (Rayovac PN added). - Chap. 4.2: I2C Busses 7- and 8- bit addresses mentionned. - Chap. 4.4.2: Table 16 (I2C_BOARD_CONTROL @0x73) bit0 ID fixed. - Chap. 5.1.1: Added Table 31 (Serial Cable Description) - Chap. 5.3.2: Table 50 (P0 pin assignement) updated with note (2). - Chap. 5.4: Table 57 (LEDs meaning) updated. - Chap. 5.4: Table 58 (Error codes displayed by LEDs) updated. - Chap. 6.1: Table 61 (VME Input Power Rails Monitoring) updated. - Chap. 7.2: PTU tool availability addressed. - Chap. 7.3: Table 65 (VM606x Maximum Current) updated. Table 66 (VM606x Power Consumption) updated. XMC supply from 12V power rail added. Table 67 (PMC and XMC Mezzanines Maximum Power Consumption) updated. - Chap. 7.4.1: Reference to Intel® documentation for thermal management. - Chap. 7.4.2: 7- & 8- bit I2C addresses of LM73 & NCT7802 sensors added in text and figures 34 & 35. - Chap. 7.4.2: Temperature thresholds of NCT7802 & LM73 sensors updated. - Chap. 7.5.2: Table 69 (Recommended Thermal Operating Points for Air-Cooled VM606x) and text updated. Figures 37 & 38 (Power Dissipation vs Air Flow) added. - Chap. 8 (Conduction-Cooled VM606x-RC) added	06-2020

Customer Support

Please contact our support team at support.KFR@kontron.com

Customer Service

As a trusted technology innovator and global solutions provider, Kontron extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly-experienced support enables Kontron to provide exceptional peace of mind to build and maintain successful products.

For more details on Kontron's service offerings such as: enhanced repair services, extended warranty, Kontron training academy, and more visit http://www.kontron.com/support-and-services/services.

Customer Comments

If you have any difficulties using this user guide, discover an error, or just want to provide some feedback, contact Kontron support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user guide on our website.

Symbols

The following symbols may be used in this user guide

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
NOTICE	NOTICE indicates a property damage message.
	**Electric Shock!** This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	**ESD Sensitive Device!** This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	**HOT Surface!** Do NOT touch! Allow to cool before servicing.
	**Laser!** This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol indicates important information which must be read carefully.
	This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!

Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

General Instructions on Usage

In order to maintain Kontron's product warranty and CE compliance, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty and CE compliance.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Environmental protection is a high priority with Kontron.
Kontron follows the WEEE directive
You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Terms and Conditions

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Kontron sells products worldwide and declares regional General Terms & Conditions of Sale, and Purchase Order Terms & Conditions. Visit http://www.kontron.com/terms-and-conditions.

For contact information, refer to the corporate offices contact information on the last page of this user guide or visit our website CONTACT US.

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1/ Introduction

1.1. Manual Overview

1.1.1. Objective

This guide provides general information, hardware instructions, operating instructions and functional description of the VM606x board. The onboard programming, onboard firmware and other software (e.g. drivers and BSPs) are described in detail in separate guides (refer to section 1.2"Related Publications").

This hardware technical documentation reflects the most recent version of the product. The "Hardware Release Notes" (refer to section 1.6 "Related Publications") keeps track of the successive product evolutions.

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

1.1.2. Audience

This guide is written to cover, as far as possible the range of people who will handle or use the VM606x, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, system, cabling, grounding and communications.

1.1.3. Scope

This guide describes all variants of the VM606x series. It does not cover any PMC/XMC modules which are described in specific guides.

1.1.4. Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with a brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- Chapter 1 - Introduction (this chapter)
- Chapter 2 - Board Overview
- Chapter 3 - Installation
- Chapter 4 - Additional Board Features
- Chapter 5 - Physical IOs
- Chapter 6 - Electrical Specifications
- Chapter 7 - Power and Thermal Management

1.1.5. Terminology, Definitions and Abbreviations

> VM606x family

This User Guide describes the VM606x family. The "x" suffix codes the number of cores inside the Xeon: VM6062 is a dual-core SBC, VM6064 a quad-core SBC etc.

- Environment classes terminology:
  - VM606x-SA will be associated to the standard air-cooled commercial version of the board.
  - VM606x-WA will be associated to the extended temperature version of the board.
  - VM606x-RA will be associated to the rugged air-cooled version of the board.
  - VM606x-RC will be associated to the rugged conduction-cooled version of the board.
- Terms and acronyms

Term or Acronym	Definition
1 GbE	Abbreviation for 1-Gbit Ethernet interface (1000BASE-T).
AVX2 (Intel®)	Intel® Advanced Vector Extensions 2.0. A set of advanced instructions including 256-bit integer instructions, floating-point fused multiply add (FMA) instructions and gather operations meant to improve performance in math and digital signal processing, vector calculations and general purpose high performance computing.
Core	A processing unit including instruction cache, data cache, and often L2 cache.
COTS	Commercial Off The Shelf.
CPLD	Complex Programmable Logic Device
FRAM	Ferroelectric Random Access Memory
LPC	Low Pin Count bus interface.
MTBF	Mean Time Between Failure.
MiniPCIe card	Synonym of MiniPCI Express card.
OD	Open Drain Output
Option	A feature which requires a specific order code.
PCB	Printed Circuit Board.
PCH	Platform Controller Hub. In Xeon® D architecture, the PCH is integrated in the SoC.
Processor	According to Intel® terminology, the processor - synonymous with SoC - includes the 64-bit cores, uncore, IOs, Integrated PCH Logic, Integrated 10GbE, and package.
PCIe	Synonym of PCI Express.
Provision	A feature not yet available.
PTU (Intel®)	Intel® Performance Test Utility.
SBC	Single Board Computer (the term defaults to VM606x).
SKU	Stock Keeping Unit: A catalog's product and service identification code.

Term or Acronym	Definition
SMBus	System Management Bus.
SoC (Intel®)	System on chip. According to Intel® terminology, the SoC - synonymous with processor - includes the 64-bit cores, uncore, IOs, Integrated PCH Logic, Integrated 10GbE, and package. In this document, SoCA and SoCB terms are used to identify SoC on side A or B of the VM606x.
SWaP, SWaP-C	Seize, Weight and Power - Cost: an acronym to summarize the capabilities of an embedded system in Military or Aerospace.
TDP	Thermal Design Power: the target power level of the processor. It represents the maximum sustained power expected from realistic applications. It is an input to the thermal design of the board.
TPM	Trusted Platform Module: An international standard for a secure cryptoprocessor based on a dedicated hardware device and integrating cryptographic keys. Promoted by consortium TCG (Trusted Computing Group).
Turbo Boost Technology (Intel®)	A feature that opportunistically enables the processor to run a faster frequency. This results in increased performance of both single and multi-threaded applications.
Uncore	In Xeon® D architecture, a unit of the SoC which includes the Ring, the Caching Agent Cbo, the Last Level Cache (LLC), the Home Agent (HA), the Integrated Memory Controller (IMC), the Integrated IO Module (IIO), the Power Control Unit (PCU).

1.2. Related Publications

The following publications contain information relating to this product.

Table 1: Related Publications

TOPIC	PUBLICATION
Standards	
ANSI/VITA 1.0	VME64 - ANSI/VITA 1-1994 (S2011)
ANSI/VITA 1.1	VME64x Extensions - ANSI/VITA 1.1-1997 (S2011)
ANSI/VITA 1.5	2eSST - ANSI/VITA 1.5-2003 (S2014)
ANSI/VITA 1.7	Increased Current Level for 96 Pin & 160 Pin DIN/IEC Connector Standard - ANSI/VITA 1.7-2003 (S2014)
ANSI/VITA 35	PMC-P4 Pin Out Mapping To VME P0 and VME64x P2 - ANSI/VITA 35-2000 (S2011)
ANSI/VITA 42.0	XMC Switched Mezzanine Card Auxiliary Standard - ANSI/VITA 42.0-2016
ANSI/VITA 42.3	XMC PCI Express Protocol Layer Standard - ANSI/ VITA 42.3-2014
ANSI/VITA 47	Environments, Design and Construction, Safety, and Quality for Plug-In Units Standard ANSI/VITA 47-2007
ANSI/VITA 61.0	XMC 2.0 - ANSI/VITA 61.0-2014

TOPIC	PUBLICATION
IEC62380	Reliability data handbook – Universal model for reliability prediction of electronics components, PCBs and equipment - IEC IEC62380-2004
IEEE 1386	IEEE Standard for a Common Mezzanine Card (CMC) Family - IEEE Std 1386-2001
IEEE 802.3	- Clause 40 and other clauses related to 1000BASE-T: IEEE 802.3 Physical Layer specification for a 1000 Mb/s CSMA/CD LAN using four pairs of Category 5 balanced copper cabling.
MIL-HDBK-217	Military Handbook - Reliability Prediction of Electronic Equipment - Department Of Defense MIL-HDBK-217-1991
MIL-STD-810-G	Environmental Engineering Considerations and Laboratory Tests - Department Of Defense MIL-STD-810-G w/ Change 1 - 2014
PCI Express M.2	PCI Express M.2 Specification - PCI SIG-2013
Serial ATA	Serial ATA Revision 3.2 - SATA IO-2013
Trusted Platform Module	TPM Main Specification Level 2 Version 1.2, Revision 116
USB3	Universal Serial Bus Specification 3.0 - 1.0 2008
Hardware	
ALMA2f User Manual	ALMA2f - PCI32-66 MHz / VME 2eSST FPGA Bridge User Manual - CI.DT.A00-1e - October 2009
ALMA2f Release Notes	ALMA2f - FPGA Bridge Release Notes - CI.DT.A01-0e - March 2013
VM606x	VM606x Hardware Release Notes : D209560
Firmware	
VM606x	AMI-BIOS User Manual: D216708
Operating System	
SD.DT.G53	Kontron VME/VPX Fedora 28 Remix - Release Notes for VX6060, VX3030, VM6050, VX3035, VX3040, VX6080, VM6052, VM6054, VM606x, VX305x, VX609x, VX6064, VX6058, VM606x, VX305x-40G Boards: D215295

2/ Board Overview

The VM606x is a high-performance, SWaP-C optimized, 6U VME computing blade well-suited for intensive data and signal processing in harsh environment.

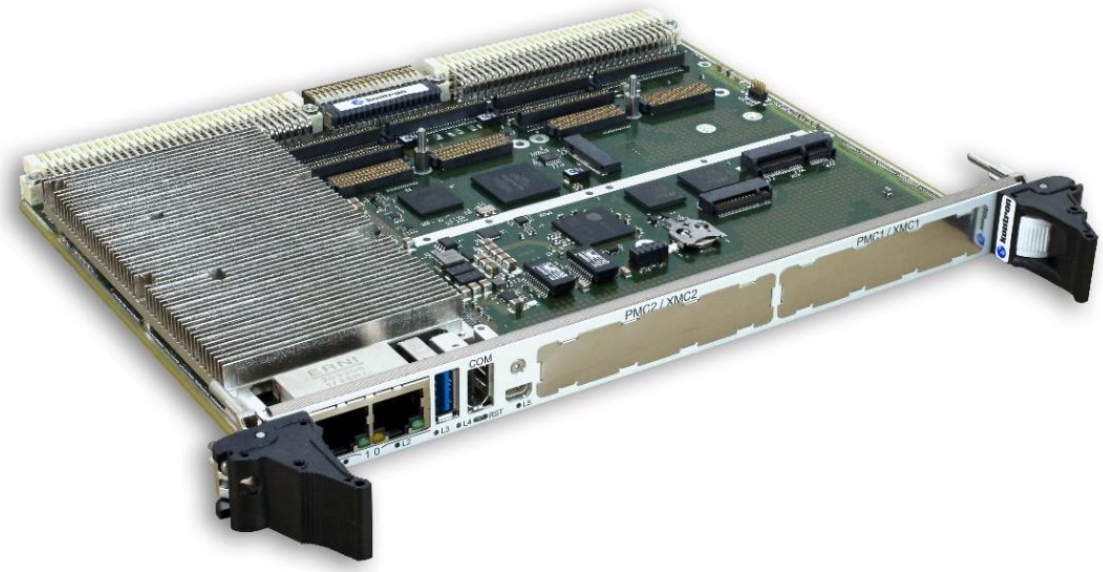
The board features a System-on-Chip from the Intel® Xeon® Processor D-1500 Product Family which includes multiple 14-nm, 64-bit cores. It supports up to 32 GBytes of DDR4 memory, a high performance 2eSST VME interface, a high bandwidth PCI Express 2.0 link, a 2-D SM750 graphic controller, two Gigabit Ethernet controllers, two XMC/PMC sites, and a M.2 socket for SSD M.2 modules. In addition, several IOs ports are available on front panel and rear backplane as well: SATA, USB3.0, USB2.0, serials and GPIOs.

For further flexibility, one of the XMC/PMC may be replaced on demand by a MiniPCIe card socket and a second M.2 socket.

The VM606x is available in three configurations: standard air-cooled (SA), ruggedized air-cooled (RA) and ruggedized conduction-cooled (RC). The latter is described in dedicated section "Conduction-Cooled VM606x-RC".

The VM606x comes with EFI BIOS. It is covered by Kontron's long term supply program, which guarantees customers multi-year supply of the product beyond its active life.

Figure 1: VM606x-SA Overview



VM606x IOs are compatible with VM605x, the previous generation of Core™ i7 6U VME SBC by Kontron.

2.1. Main Features

A Multiple Applications Computing Node

The VM606x single board computer - successor to the VM605x - is a VME computing blade for parallel data and signal processing applications.

Intel® Xeon® D Processor D-1500 Product Family

The processors of the Intel® Xeon® D-1500 Product Family are 64-bit, multi-core SoC built on 14-nanometer process technology. They implement:

- Two, four or more cores running at a frequency ranging from 1.5 to 2.2 GHz. This frequency can be either decreased in order to make appropriate power/performance trade-offs or opportunistically increased via "Turbo Boost" to enhance performance. Each core includes two levels of cache: Instruction and Data Cache (ICU and DCU, corresponding to a L1 cache) and Mid-Level Cache (MLC, corresponding to a L2 cache). The cores support Intel® Hyper-Threading Technology (two threads per core).
- A unit called "uncore module" which implements the "Ring", a bi-directional topology to interconnect core and uncore modules, the "Caching Agent" (Cbo), the Last Level Cache (LLC, corresponding to a L3 cache), the "Home Agent" (HA) which handles the DRAM requests, the Integrated Memory Controller (IMC), the "Integrated IO Module" (IIO) which is the PCI Express interface and the "Power Control Unit" (PCU).
- An integrated PCH with several PCI Express gen3 and gen2 interfaces, SATA III ports, USB3.0 and USB2.0 ports, a SMBus, a LPC interface, two UARTs.

Soldered DDR4 Memory with ECC

The two banks of DDR4 memory include ECC and are soldered directly on the PCB. Total capacity is 8, 16 or 32 GB.

Additional onboard Features

In addition to the functions supported by the System on Chip and listed above, the board features:

- Two Intel® i210IT controllers supporting two 1000BASE-T ports routed either to front or rear.
- One 2-D graphic Silicon Motion SM750 controller supporting a HDMI interface routed either to front or rear. It includes a 16MB embedded DDR memory (32-bit mode). The maximum graphics resolution is 1280x1024.
- One RTC and a watchdog/timer.
- A CPLD for the handling of I2C interfaces (VME, onboard sensors), resets, internal power-supplies, monitoring.

VME Interface, Rear and Front IOs

Like its predecessors, the VM606x is based on the ALMA2f VME bridge and keeps all of its VME performance (2eSST bandwidth). On front, two 1GbE ports and a COM1/COM2 serial port are available while the USB port has been upgraded to USB 3.0 and a HDMI port has been added. On rear, the same IOs may be found but the number of GPIOs has been increased from 8 to 14.

High Versatility with add-on Modules and Mezzanines

The VM606x offers several expansion slots:

- One or two PMC/XMC sites.
- One or two M.2 sockets to host SSD M.2 modules.
- An optional MiniPCIe or mSATA socket.

Numerous Storage Interfaces and Non Volatile Memories

- The M.2 socket can host SATA SSD modules with various form factors and capacities: 2242-D4-M or 2260-D4-M on socket S1 and 2242-D5-M on socket S3.
- Redundant 64-Mbit SPI NOR Flash memories are used to store firmware code.
- Two serial 256-Kbit I2C EEPROMs are dedicated to VPD and data storage.
- One 1-Mbit, non-volatile, FRAM allows the backup of critical data when the board is powered off. This FRAM is a user memory device.
- Lastly, several SPI Flash and EEPROMs store the set-up information for the local controllers: ALMA2f VME bridge, i210 1000BASE-T Ethernet controllers, SM750 graphic controller, DDR4 SPD.

All onboard Flash devices and non-volatile memories feature a write protect mechanism implementing the VME NVMRO signal. Refer to section 4.8 for detailed information.

Security Features

Approtect Secure Element

A secure element by Wibu can be accessed through a USB 2.0 interface and protects the application integrity and confidentiality. All or part of the application execution code is encrypted on the storage device and will only be decrypted in memory in presence of the keys stored inside the secure element. At run time, the integrity of the application in memory is also permanently checked.

TPM Secure Element

The Trusted Platform Module (version 1.2, revision 116 - component SLB9660XQ1.2 FW 4.43 by Infineon) is a secure element to protect the system. It is used for trusted boot and for TLS ethernet connections (https, ...): Any single bit change in the boot, as compared to a reference value, is detected and reported in a local or remote cryptographic attestation. For the TLS connections, the secure element is used to store internally the private key and execute internally the authentication operation.

For more information on security in Kontron products, refer to SEC-Line datasheet.

10-Year Life Cycle

The VM606x has been designed with long life cycle components. Beyond the use of standard commercially available components, Kontron offers longevity through supply services which are designed to make the VM606x available for ten years or longer.

Legacy Compatibility

The VM606x has been designed to offer a legacy IO compatibility with the Kontron's PENTXM2/PENTXM4, VM6050, VM6250, VM6052/VM6054 boards to provide an easy path for technology insertion into existing systems.

Rear transition module (tooling)

The PBV36-P0-VM6-00 rear transition module is compliant to PMC IO Module Standard VITA 36 - 199x Draft 0.1 July 19, 1999 (mechanical and PIM format) and features: Two 10/100/1000BASE-T Ethernet ports, one USB connector, one SMBus connector, two serial lines on two HE10 connectors, three GPIOs signals through a HE10 connector, two SATA connectors, one PCIe connector, PMC IOs connectors.

Although it has been designed according to the relevant I/O standards, the PBV36-P0-VM6-00 is meant as a tool and therefore was not qualified for product deployment. If you need to deploy with such accessories, please contact Kontron.

Carrier Board

The VM606x supports the V2PMC2, a 6U VME PCI-X/PMC carrier card that holds up to two single-width or one double width PCI-X/PMC modules.

Form Factor and Temperature Grade

The VM606x form factor is VME 6U, 4HP (233.35 x 160 x 20.32 mm).

The VM606x is available in standard air-cooled 0 to 55°C (SA), ruggedized air-cooled -40 to 70°C (RA) or conduction-cooled -40 to 70°C/85°C (RC3/RC4) versions.

Software

Kontron is one of the few compactPCI, VME and VPX vendors providing in-house support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software editors, Kontron is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

The VM606x is delivered with the UEFI BIOS from AMI.

For information regarding operating systems and software support, please contact Kontron.

2.2. Block Diagram

Figure 2: VM606x Simplified Block Diagram

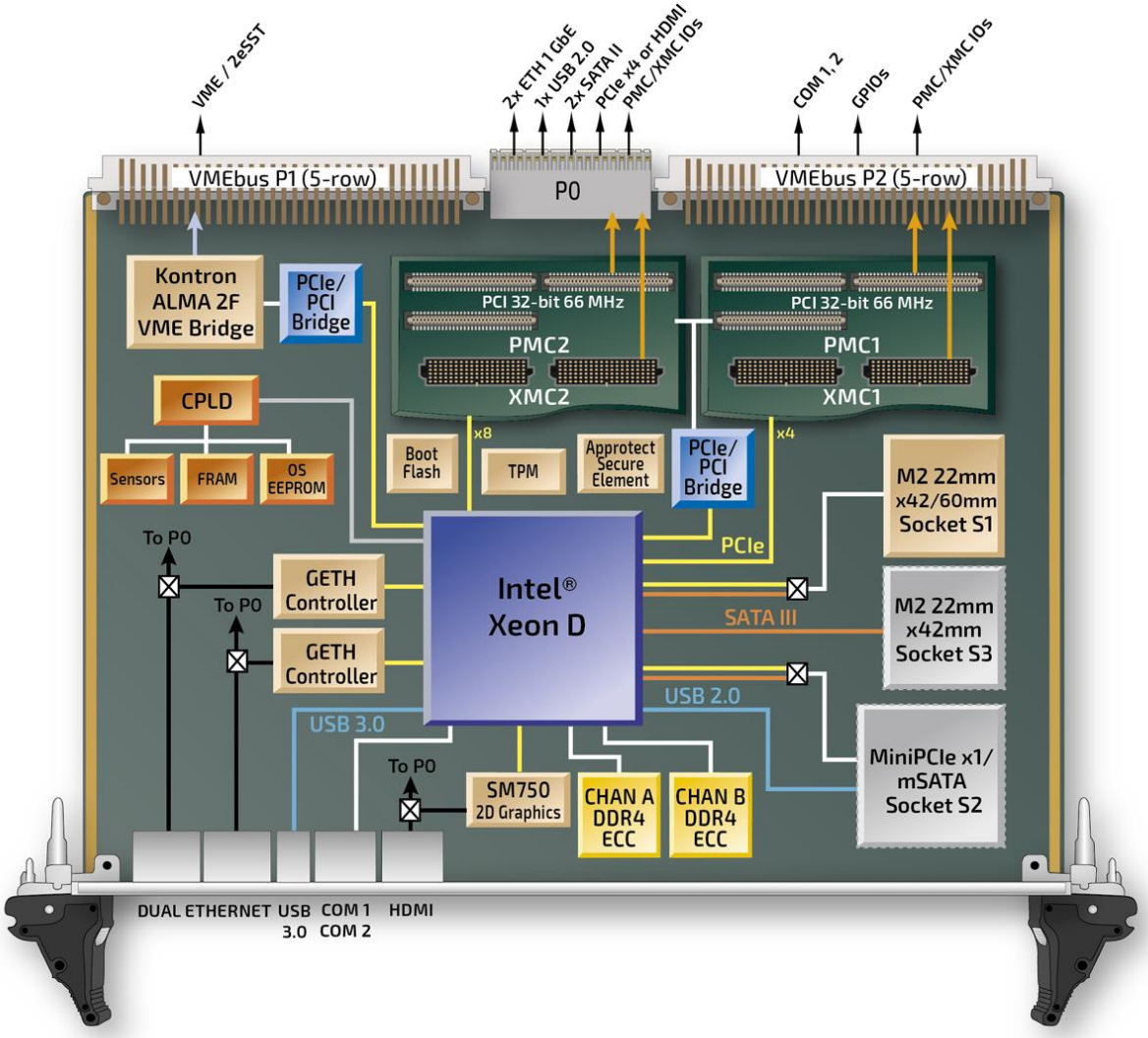
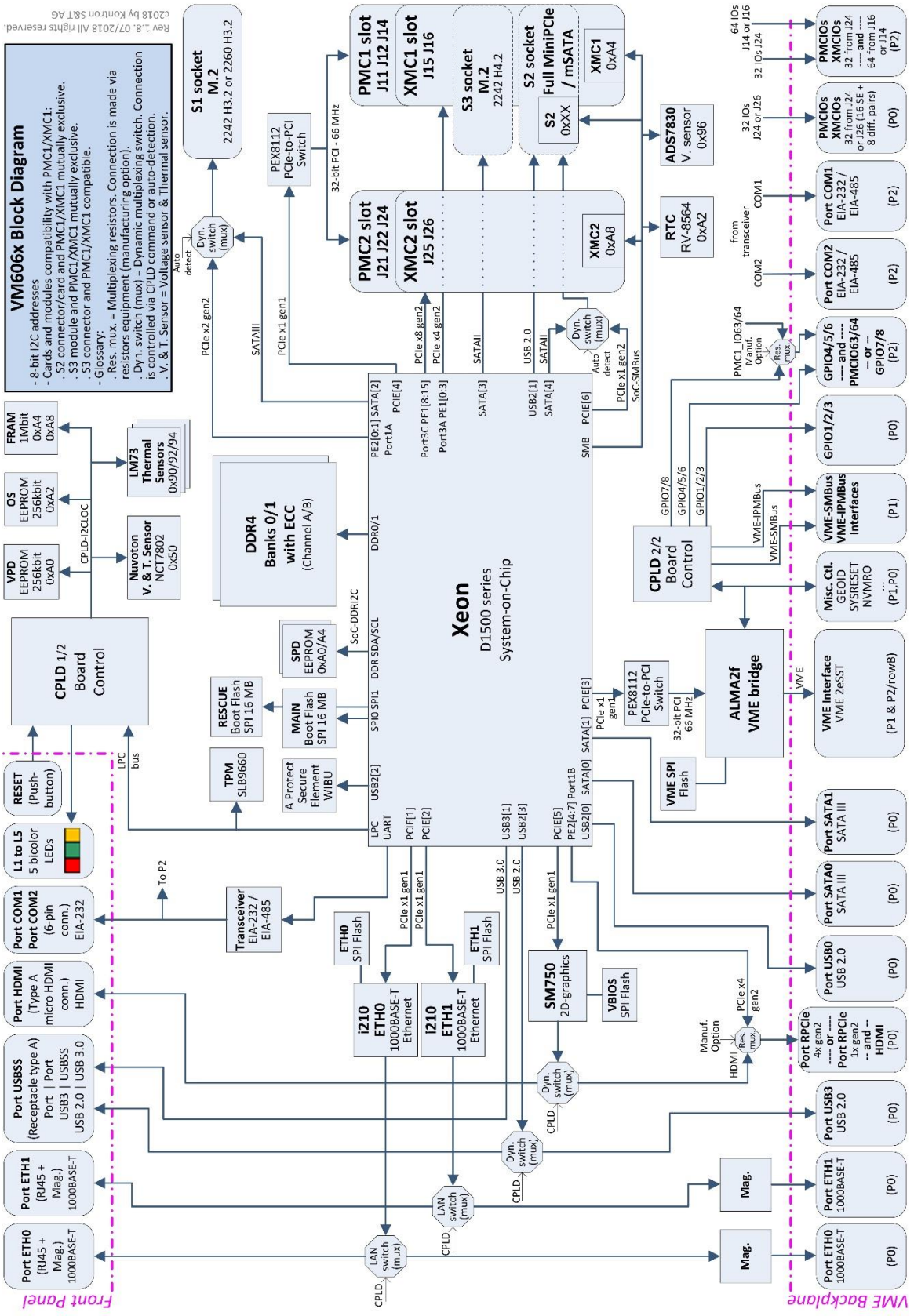


Figure 3: VM606x Detailed Block Diagram



2.3. Ordering Information

2.3.1. Order Codes

Examples of VM606x order codes are listed in Table 2. For actual availability, please contact Kontron.
For conduction-cooled order codes, refer to Chapter 8 Conduction-Cooled VM606x-RC.

Table 2: VM606x Order Codes

Order Code	Description
VM6062-SA28-00200100	6U VME Single Board Computer 2-core Intel® processor D-1508, 2.2 GHz, TDP 25W, 3 MB cache 8GB dual-bank DDR4 Secure element : TPM Two PMC/XMC sites, two M.2 socket (PMC1/XMC1 and M.2 module in S3 mutually exclusive) Standard P0: 1000BASE-T ETH0 & ETH1 ports, USB 2.0 USB3 & USB0 ports, rear HDMI port, GPIOs, PMC/XMCIOx, utility signals. (1) 6 GPIOs, COM1 & COM2, PMC1 IOs 64ac Battery equipped Standard Air-Cooled "SA" (0°C to +55°C) No conformal coating
VM6062-SA28-00000100	Same as VM6062-SA28-00000100 but with higher-speed P0 option Higher-speed P0: 1000BASE-T ETH0 & ETH1 ports, USB 2.0 USB3 & USB0 ports, rear HDMI port, GPIOs, PMC/XMCIOx, utility signals. PCI Express x4 gen2 port RPCIE and SATA II ports SATA0 & SATA1. This version is non-standard and may not be available.
VM6062-RA2G-10200100	6U VME Single Board Computer 2-core Intel® processor D-1508, 2.2 GHz, TDP 25W, 3 MB cache 32GB dual-bank DDR4 Secure element : TPM One PMC/XMC site, one mPCIe/mSATA socket, two M.2 sockets Standard P0: 1000BASE-T ETH0 & ETH1 ports, USB 2.0 USB3 & USB0 ports, rear HDMI port, GPIOs, PMC/XMCIOx, utility signals. (1) 6 GPIOs, COM1 & COM2, PMC1 IOs 64ac Battery equipped Rugged Air-Cooled "RA" (-40°C to +70°C) Conformal coating
VM6064-SA4G-00300100	6U VME Single Board Computer 4-core Intel® processor D-1527, 2.2 GHz, TDP 35W, 6 MB cache 32GB dual-bank DDR4 Secure element : TPM Two PMC/XMC sites, two M.2 socket (PMC1/XMC1 and M.2 module in S3 mutually exclusive) Standard P0: 1000BASE-T ETH0 & ETH1 ports, USB 2.0 USB3 & USB0 ports, rear HDMI port, GPIOs, PMC/XMCIOx, utility signals. (1) 6 GPIOs, COM1 & COM2, PMC1 IOs 64ac Battery equipped Standard Air-Cooled "SA" (0°C to +55°C) No conformal coating

(1) For rear SATA and PCIe interfaces with standard P0, please refer to section 2.3.3 P0 Part Number Change and its Impact on Rear SATA and PCIe Interfaces.

Table 3: Associated Products Order Codes

Order Code	Description
PBV36-P0-VM6-00	6U VME Air-Cooled Rear Transition Module, 2 PIMs, no face-plate to use with PIM-2DP-00
1064-4995	Adaptation Cable for Serial Lines: IEEE 1394 <-> DB-9
V2PMC2-SA	6U VME Air-Cooled Dual PMCs Carrier Card

2.3.2. Coding of the Manufacturing Options

The table 4 shows how the manufacturing options are coded in the order code.

This table is for information only. Please contact Kontron for available order codes.

Table 4: Coding of the Manufacturing Options

				VM606	2	-	SA	2	8	-	0	0	0	0	0	0	0	0
Processor	Intel® Server Class D15xx 2-core 4-thread processor		2															
	Intel® Server Class D15xx 4-core 8-thread processor		4	ASK														
Environment	Air-Cooled 'SA' (0°C to 55°C)		SA															
Class	Air-Cooled 'WA' (-20°C to +65°C) with conformal coating		WA															
	Rugged Air-Cooled 'RA' (-40°C to +70°C) with conformal coating		RA															
	Rugged Conduction-Cooled 'RC3/RC4' (-40°C to +70°C/85°C) with conformal coating		RC															
Processor ID	Intel® D-1508, 2c, 3MB cache, 2.2GHz, TDP 25W		2															
	Intel® D-1519, 4c, 6MB cache, eTEMP, 1.5GHz, TDP 25W		3															
	Intel® D-1527, 4c, 6MB cache, 2.2GHz, TDP 35W		4															
SDRAM	8 GB soldered SDRAM with ECC		8															
	16 GB soldered SDRAM with ECC		F	ASK														
	32 GB soldered SDRAM with ECC		G	ASK														
Expansion slot	Two PMC/XMC sites, up to two M.2 sockets		0															
	One PMC/XMC site, mPCIe/mSATA, Dual M.2 sockets (on demand)		1															
Power Supply	+3.3V/+5V		0															
	+5V Only		5	ASK														
Rear IOs P0	PCI-Express x4	& Higher-Speed P0	0	ASK														
	HDMI and PCI-Express x1	& Higher-Speed P0	1	ASK														
	PCI-Express x4	& Standard P0 (1)	2															
	HDMI and PCI-Express x1	& Standard P0 (1)	3															
	No P0		N															
Rear IOs P2	6 GPIOs, COM1 & COM2, PMC1 IOs 64ac		0															
	8 GPIOs, COM1 & COM2, PMC1 IOs 62ac		1	ASK														
	14 GPIOs, COM 1, PMC1 IOs 62ac (on demand)		2	ASK														
Battery	Battery,		0															
	No battery		1	ASK														
Secure Element	Dual SE : TPM + Wibu Code Meter		0	ASK														
	Single SE: TPM		1															
	No SE		3	ASK														
Coating	-		0															
	Conformal Coating option on 'SA' build		V															
Power on Built In Test	no PBIT		0															
	PBIT object run time		P															

(1) For rear SATA and PCIe interfaces with standard P0, please refer to section 2.3.3 P0 Part Number Change and its Impact on Rear SATA and PCIe Interfaces.

2.3.3. P0 Part Number Change and its Impact on Rear SATA and PCIe Interfaces

The P0 connector part 3M UHM-S095B3-5AP1-KR which was used in the VM606x original design has been discontinued in 2019.

Unfortunately none of the replacement solutions on the market can achieve the 7 Gbps data rate offered by the UHM series. The replacement part selected by Kontron is Harting 17250951102 with a 2.5 Gbps data rate.

As a consequence, the performance, or even the availability, of the rear fast links (SATA and PCIe) is impacted:

- The original VM606x order codes supporting the UHM series part – now referred to as "higher-speed P0" – keep their performance but may be subject to restrictions depending on available stock. Please contract Kontron for further information.
- New VM606x order codes implementing the Harting 17250951102 part – referred to as "standard P0" in this document – can technically support lower data rates such as 1.5 Gbps SATA I or 2.5 Gbps PCIe gen1. But the availability of these links now depends on the ability of the application software to enforce the link data rate and not simply rely on the link auto-negociation. If your application requires the use of SATA or PCIe on P0, please contact Kontron and provide the mission profile details (features, required speed, temperature range etc.).

2.3.4. Expansion Cards Equipment Options

The VM606x has been designed to offer the maximum flexibility for the equipment of the expansion cards. Nevertheless, space is not unlimited and some restrictions apply.

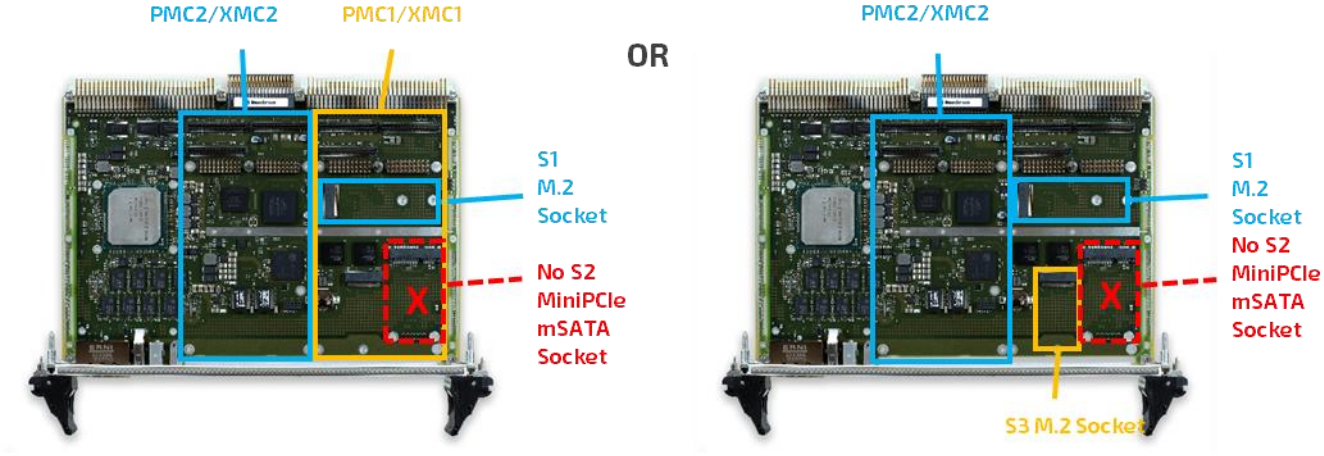
- "Expansion Slots" option = 0: Two PMC/XMC sites, two M.2 sockets.

The PMC2/XMC2 mezzanine and the S1 M.2 module may always be installed (in blue in Figure 4).

The PMC1/XMC1 mezzanine and the S3 M.2 module cannot be installed at the same time because they would conflict in the PMC/XMC keep-out IO area (in orange in Figure 4).

The MiniPCIe/mSATA card cannot be installed because socket connector is not present (in dotted red in Figure 4).

Figure 4: Expansion Slots Option 0



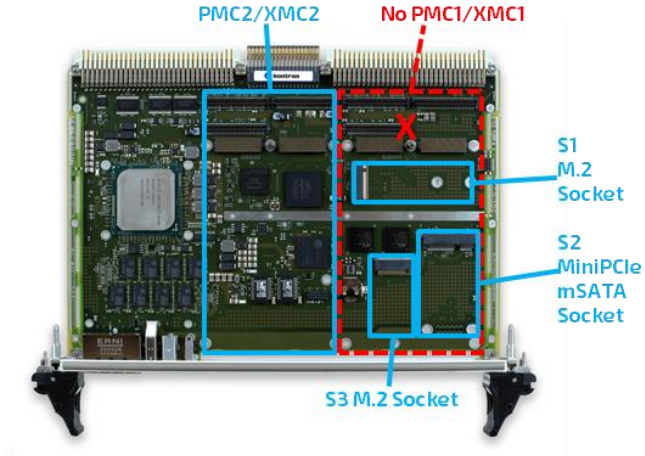
- "Expansion Slots" option = 1: One PMC/XMC site (VITA 42 XMC), two M.2 sockets, one MiniPCIe/mSATA socket

The PMC2/XMC2 mezzanine, the S1 & S3 M.2 modules, the MiniPCIe/mSATA card may always be installed (in blue in Figure 5).

The PMC1/XMC1 mezzanine cannot be installed (in dotted red in Figure 5).

The S2 socket for MiniCPIe or mSATA cards is an "on demand" option. Please contact Kontron.

Figure 5: Expansion Slots Option 1



2.4. IO Interfaces

2.4.1. Front Interfaces

Front IOs are available in SA, WA and RA classes.

Figure 6: Front Panel Connectors and LEDs

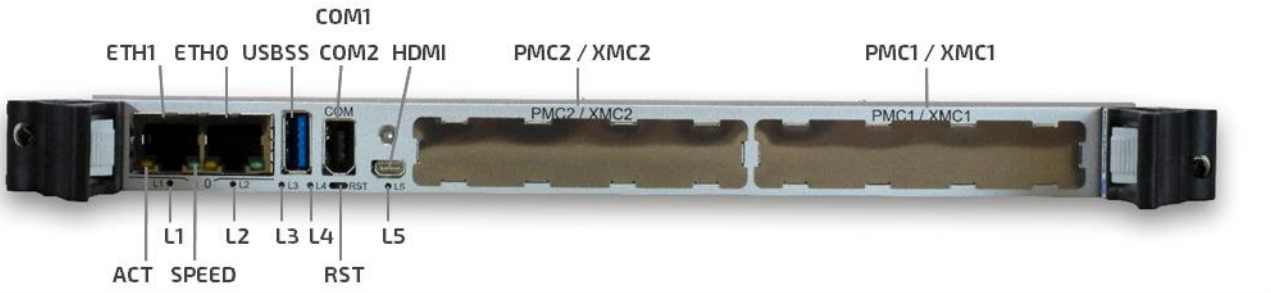


Table 5: Front IO Interfaces

Port ID	Function	Description	Full Description
COM1, COM2	Serial Ports	Two EIA-232 ports	Section 5.1.1
ETH0, ETH1	Gigabit Ethernet	Two 1000BASE-T ports on a dual RJ-45 connector	Section 5.1.2
USBSS	USB 3.0	USB 3.0 port	Section 5.1.3
HDMI	HDMI graphics	HDMI interface (without audio)	Section 5.1.4
PMC1/XMC1, PMC2/XMC2	PMC/XMC	Two PMC/XMC sites	Section 5.2.1 Section 5.2.2
RST	Reset	Reset push button.	Section 4.7
L1 to L5	LEDs	Five LEDs reporting the board health status and activity	Section 5.4
ACT, SPEED	Ethernet LEDs	Activity and Speed LEDs attached to ETH0 and ETH1	

2.4.2. Rear Interfaces

Figure 7: Rear Connectors

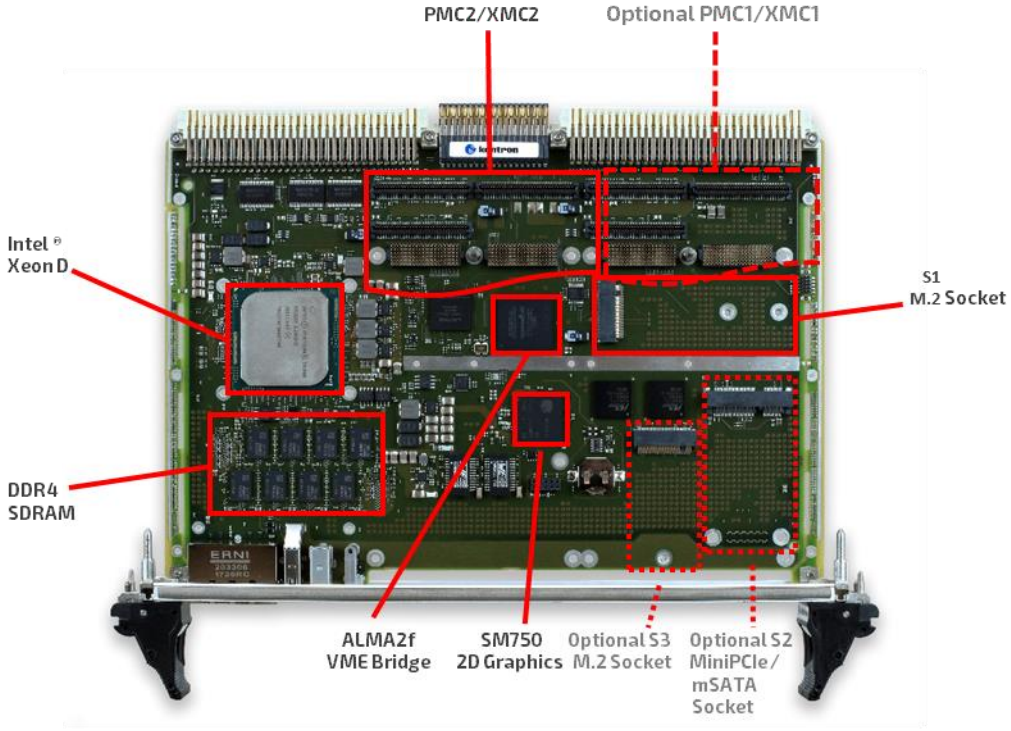
Table 6: Rear IOs Distribution

	VME	PCI Express	Graphics	SATA	USB	Ethernet	Serial	GPIOs	I2C	PMC IOs XMC IOs	Misc
P1	VME (on rows A, B, C)								SMBus & VME-IPMBus		
P0		RPCIE (4x or 1x) (1)	Option: RHDMI (HDMI, no audio)	SATA0 & SATA1 (1)	USB0 & P0_USB3 (USB 2.0)	ETH0 & ETH1 (1000BASE- T)		GPIO[1:3]		PMC2 IOs XMC2 IOs	GA[0:5]# (Geographic al Addresses)
P2	VME (on row B)						COM1 & COM2 (EIA-232 or EIA422/485)	GPIO[4:6] - - - Option: GPIO[7:14]		PMC1 IOs (P4V2-64ac) PMC2 IOs (P4V2-32dz) or XMC1 IOs	RESET#, NVMRO, V_BAT_EXT

(1) For rear SATA and PCIe interfaces with standard P0, please refer to section 2.3.3 P0 Part Number Change and its Impact on Rear SATA and PCIe Interfaces.

2.5. Components Layout

Figure 8: VM606x Components Layout (Top view)



2.6. Technical Specification

Table 7: VM606x Main Characteristics

Device or Function	Description
Onboard Functions	
Processor	Server Class Intel® Xeon® Processor D-1500 family. Typically D1508 System on Chip, 2-core/4-thread, 3 MB, 2.2GHz, 25W TDP. Note: other part numbers available, please contact Kontron.
System DDR4 memory	DDR4 dual channel memory with ECC, up to 2400 MT/s over 144 bits. Capacity of 8, 16 or 32 GB depending on manufacturing option.
RTC, Watchdog, Timer	- RTC: RV-8564-C2 device powered by onboard battery or backplane VBAT. Connected to SoC-SMBus. - Watchdog and Timer (integrated in CPLD): timeout ranging from 2 µs to 510s, IRQ, Reset, dual-stage.
FRAM, boot and rescue Flash Devices, VPD and OS EEPROM	- FRAM: 1-Mbit serial I2C device. Connected to CPLD-I2CLOC bus. - Boot and rescue Flash Devices: 16-MByte devices. Connected to SoC SPI0 and SPI1 interfaces. - VPD and OS EEPROM: 256kbit devices. Connected to CPLD-I2CLOC bus.
System CPLD	The CPLD handles the I2C interfaces, power-on/off controls and board resets, internal power-supplies sequencing and their monitoring, alerts, LEDs, GPIOs, onboard multiplexors controls (Ethernet, Graphics, USB), serial lines configuration. Configuration/status registers can be accessed from SoC LPC interface.
TPM	TPM device, version 1.2, revision 116. Component SLB9660XQ1.2 FW by Infineon. Connected to SoC LPC interface.
Monitoring	Voltage monitoring is achieved through the Nuvoton NCT7802 and the ADS7830 sensors. Temperature monitoring is achieved through the Nuvoton NCT7802 sensor, the Xeon sensors and three LM73 thermal sensors.
Approtect Secure Element	Secure Element by Wibu to protect application integrity and confidentiality. Connection: from SoC USB interface USB[2].
Add-on Modules and Mezzanines	
M.2 socket S1	- Form factor: 2242-D4-M H3.2 or 2260-D4-M H3.2. - Interface: Connected to SoC SATA III capable port SATA[2] or PCIe x2 gen2 port Port1A PE2[0:1] with autodetect connection.
M.2 socket S3	- Form factor: One M.2 socket 2242-D5-M H4.2. - Interface: Connected to SoC SATA III capable port SATA[3]. - Limitation: when equipped, the M.2 module on S3 protrudes into the PMC1/XMC1 keep-out IO area. The S3 socket connector is always equipped and does not conflict with XMC1/PMC1 envelope, but the user may not be able to equip both XMC1/PMC1 and the M.2 module.
Optional MiniPCIe socket S2	One MiniPCIe socket for a full size F1 or F2 minicard or a mSATA card. Connected to SoC interfaces USB 2.0 port USB2[1], PCIe x1 gen2 port PCIE[6] or SATA port SATA[4] with autodetect connection. Exclusive with PMC1/XMC1 slot. This manufacturing option is on demand. Please contact Kontron.
PMC site PMC1	32-bit, 66 MHz PMC, 3.3V VIO. Connected to SoC PCIe port x1 gen2 PCIE[4] through PEX8211 PCIe/PCI bridge. PMC1 and PMC2 share the same PCI bus. PMC1 mezzanine: 10 mm stack form factor. PMC1 IOs: P4V2-64ac from J14 to P2 as per VITA 35.
PMC site PMC2	32-bit, 66 MHz PMC, 3.3V VIO. Connected to SoC PCIe port x1 gen2 PCIE[4] through PEX8211

	PCIe/PCI bridge. PMC1 and PMC2 share the same PCI bus. PMC2 mezzanine: 10 mm stack form factor. PMC2 IOs: "P4V2-32dz" from J24 to P2. 32 IOs routed to P0.
XMC site XMC1	VITA 42 XMC slot. Connected to SoC PCIe x4 gen2 interface Port3A PE1[0:3] Stack 10 mm achieved by motherboard connectors. XMC mezzanine: 10 mm stack form factor. XMC IOs: 20 differential pairs routed to P2 rows A & C, 24 single ended IOs routed to P2 rows A & C. For PCIe gen3 VITA 61 solutions, please contact Kontron. Manufacturing option.
XMC site XMC2	VITA 42 XMC slot. Connected to SoC PCI Express x8 gen2 interface Port3C PE1[8:15] Stack 10 mm achieved by motherboard connectors. XMC mezzanine: 10 mm stack form factor. XMC IOs: 8 differential pairs and 16 single ended IOs routed to P0, For PCIe gen3 VITA 61 solutions, please contact Kontron.
Front panel	
10/100/1000BASE-T ports ETH0 & ETH1	Two Intel® i210IT controllers. 10/100/1000BASE-T protocol with Auto-Negotiation. Auto-wire switching for crossed cables (Auto-MDI/X). Connection: From SoC PCI Express PCIE[1] & PCIE[2] to i210 and then to LAN switch and front RJ45 connector. The LAN switch is controlled by BIOS through CPLD.
USB 3.0 port USBSS	USB 3.0 port. Connection: from SoC USB interface USB3[1] to front panel.
Serial ports COM1 COM2	Two full duplex EIA-232 simplified interfaces (TXD, RXD, GND), 115.200baud max. Connection: From SoC UARTs to transceivers and front pannel.
HDMI port	HDMI interface without audio. Connection: from SoC PCI Express gen2 interface PCIE[5] to SM750 graphics controller and then to front microHDMI connector through graphics multiplexor.
LEDs	Five bicolor LEDs (Red/Green/Orange) reporting the board health status and activity. Handled by CPLD.
Reset	Reset push button. Handled by CPLD.
VME Backplane, Rear IOs and Interfaces	
VME interface	VME64x as per VITA 1.1 with 2eSST as per VITA 1.5 (320 MB/s peak throughput). VME interface based on ALMA2f VME controller. Connection: From SoC PCIe 1x gen1 PCIE[3] to ALMA2f through PCIe/PCI bridge PEX8112.
PCI Express port RPCIE	PCI Express link : x4 configuration. May be reduced to x1 link (manufacturing option). Speed: PCI Express gen1 with standard P0 option, PCI Express gen2 with higher-speed P0 option. Refer to 2.3.3 P0 Part Number Change and its Impact on Rear SATA and PCIe Interfaces. Connection: From SoC PCI Express interface Port1B PE2[4:7] to P0.
Optional rear HDMI port RHDMI	HDMI interface without audio on P0. Connection: from SoC PCI Express gen2 interface PCIE[5] to SM750 graphics controller and then to front microHDMI connector through graphics multiplexor. Manufacturing option.
Rear SATA ports SATA0 SATA1	SATA links: SATA I 1.5 Gbps with standard P0 option, SATA II 3Gbps with higher-speed P0 option. Refer to 2.3.3 P0 Part Number Change and its Impact on Rear SATA and PCIe Interfaces. Connection: From SoC SATA interfaces SATA[0], SATA[1] to P0.

1000BASE-T port ETH0 & ETH1.	Two Intel® i210IT controllers. 10/100/1000BASE-T protocol with Auto-Negotiation. Auto-wire switching for crossed cables (Auto-MDI/X). Connection: From SoC PCI Express PCIE[1] or PCIE[2] to i210 controller, LAN switch, magnetics and P0. The LAN switch is controlled by BIOS through CPLD.
USB 2.0 ports USB0 & USB3.	Two USB 2.0 ports. Connection: From SoC USB 2.0 interface USB2[0] to P0. From SoC USB 2.0 interface USB2[3] to dynamic switch to P0. The dynamic switch is controlled by BIOS through CPLD.
GPIOs	GPIO1 to GPIO3: Routed from CPLD to P0. GPIO4 to GPIO6: Routed from CPLD to P2. GPIO7, GPIO8: Routed from CPLD to P2 through resistors multiplexor P2MUX1. Six additional GPIOs available on demand. Please contact Kontron.
Serial COM1 & COM2	Either EIA-232 or EIA-485 protocol. Simplified serial line: TXD, RXD, GND; no hardware flow control. Protocol selection made by BIOS through CPLD and transceiver. In EIA-485, termination selection made by BIOS through CPLD and transceiver. Connection: from SoC UARTs to transceivers and P2.
XMC & PMC IO	On P2: 32 PMC IOs from PMC2 J24 always available. Additional 64 PMC IOs from PMC1 J14 or 64 XMC IOs from XMC1 J16 (20 differential pairs and 24 single ended IOs). On P0: Either 32 PMC IOs from PMC2 J24 or 32 XMC IOs from XMC2 J26 (8 differential pairs and 16 single ended IOs).
Supervisory functions	On P0: NVMRO, RESET#, V_BAT. On P1: Master-only VME-SMBus and Master/Slave VME-IPMBus interfaces for system management. On P1: geographical addresses GA[0:5]#.
Power Supplies	On P1: +5.0V, +3.3V, +12V, -12V, GND. On P2: +5.0V, GND. Onboard battery (manufacturing option).
Software	
UEFI	UEFI BIOS from AMI.
PBIT	Kontron PBIT test suite. Available only when selected in order code (VM606x-SAxx-xxxxxxxP).
OS support	Please contact Kontron.
Form Factor	
Height	VME 6U or double height (233.35 mm) as per VITA 1.
Width	Single slot (20.32 mm, 0.8 inch) as per VITA 1.
Front Panel	EMC front panel as per VITA 1.1 / IEEE 1101.10.
Extractors	Compliant to VITA 1.1 / IEEE 1101.10.

2.7. Environmental Specifications

Table 8: Environmental Specifications

	SA - STANDARD COMMERCIAL	WA - EXTENDED TEMPERATURE	RA - RUGGED AIR-COOLED
Conformal coating	Optional	Standard	Standard
Air flow (1)	Recommended: 8 CFM @33 W (2)	Recommended: 13 CFM @33 W (2)	Recommended: 15 CFM @33 W (2)
Cooling method	Convection	Convection	Convection
Operating	0°C to +55°C	-20°C to +65°C	-40°C to +70°C
Storage (3)	-40°C to +85°C	-45°C to +100°C	-50°C to +100°C
Vibration Sine (Operating)	5 to 20 Hz : Displacement 1.25 mm 20 Hz to 500 Hz: 2 g Sweep rate : 1 octave / minute		5 to 19 Hz : Displacement 1.25 mm 19 Hz to 2000 Hz: 3 g Sweep rate : 1 octave / minute
Random (Operating)	**5 Hz to 100 Hz:** PSD = 0.04g^2/Hz		**5 Hz to 100 Hz:** +3dB/octave **100 Hz to 1000 Hz:** 0.04 g^2/Hz **1000 Hz to 2000 Hz:** -6dB/octave
Shock (Operating)	20 g, 11 ms, half-sine	20 g, 11 ms, half-sine	20 g, 11 ms, half-sine
Altitude (Operating)	-1 500 ft to 60 000 ft	-1 500 ft to 60 000 ft	-1 500 ft to 60 000 ft
Relative Humidity	90% without condensation (95% with coating option)	95% without condensation	95% without condensation

(1) Thermal characterization performed in laminar flow bench according to Kontron procedure. Air flow direction is from right to left.
(2) No PMC/XMC. The power dissipation at which the air flow is specified is the overall board power dissipation. Specified without XMC. For thermal management see section 7/ Power and Thermal Management.
(3) The battery temperature range is -30°C to +70°C in SA and WA classes and -40°C to +85°C in RA class.

2.8. Board Weight

Table 9: Board Weight

	SA - STANDARD COMMERCIAL (1)	WA - EXTENDED TEMPERATURE (1)	RA - RUGGED AIR-COOLED (1)
Weight	705g +/- 10g	705g +/- 10g	705g +/- 10g

(1) No mezzanine or add-on card.

2.9. Reliability and MTBF

The reliability predictions in Table 10 are based on standard MIL-HDBK-217F Notice 2 and were calculated for the following environments:

- Ground Benign (GB)
- Naval Sheltered (NS)
- Air Rotary Wing (ARW)
- Air Inhabited Cargo (AIC)

Other standard-based reliability predictions on demand.

Table 10: VM606x MTBF Data

MTBF	MIL-HDBK-217F Notice 2					
	GB (hours)		NS (hours)		ARW (hours)	AIC (hours)
	25°C	40°C	25°C	40°C	55°C	40°C
VM6062-SA28-00000000	329 970 h	239 694 h	54 524 h	38 607 h	5 165 h	25 318 h

3/ Installation

The VM606x has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

3.1. Safety Requirements

The following safety precautions must be observed when installing or operating the VM606x. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Special care shall be taken while handling the board: the heat sink can get very hot during operation.

Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

This board contains electrostatic-sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector pins or traces.
- We strongly recommend our customers to work in an environment equipped with anti-static workbenches with professional discharging equipments.

3.2. Board Identification

The VM606x boards are identified by labels fitted to the bottom side of the board.

Figure 9: VM606x Identification (Bottom Side)

(A) "Identification" label: Order Code, Serial Number, Variant, E.C. Level, Ethernet MAC addresses

The E.C. Level format is "xxxxxLy" where:

- The five digits "xxxxx" indicate the board E.C. Level (PCB revision included)
- "Ly" indicates the mechanical E.C. Level:
  - Letter "L" varies with the environment class ("A" for SA, "B" for WA, "C" for RA and "D" for RC)
  - Digit "y" gives the mechanical E.C. Level

See also section "Vital Product Data" in "VM606x AMI-BIOS User Reference Manual".

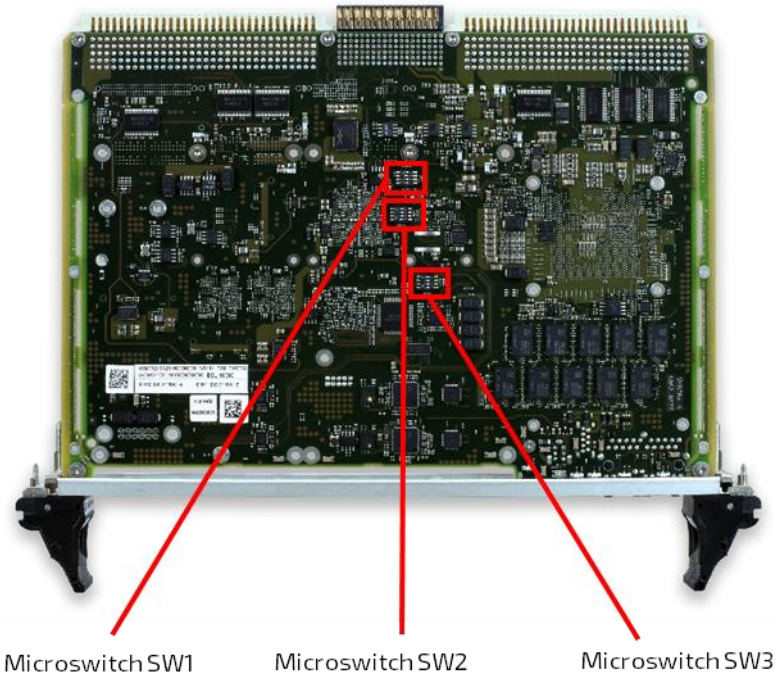
3.3. Package Contents

The package contents include:

- VM606x SBC
- A bag containing the mechanical parts for the assembly of a M.2 module on socket S1 or S3 and for the assembly of a MiniPCIe or mSATA card on socket S2 (this option is on demand).

3.4. Board Configuration

Figure 10: VM606x Board Configuration - Microswitches (Bottom view)



3.4.1. Microswitch SW1 Description

Table 11: Microswitch SW1

FUNCTION	DESCRIPTION	DEFAULT
1- Factory Test Mode	OFF: Normal Mode ON: Factory Test Mode	OFF
2 - Debug Mode	OFF: Normal Mode ON: Debug Mode	OFF
3 - Write Protection of EEPROMs: DDR4 SPD, VPD, i210IT	OFF: Write-protected ON: Writes allowed	OFF
4 - Write Protection of EEPROMs: BIOS SPI Flash (Main), BIOS SPI Flash (Rescue), FRAM	OFF: Writes allowed ON: Write-protected	OFF

Refer to section 4.8 for a detailed description of the EEPROM and Flash devices protection.

3.4.2. Microswitch SW2 Description

Table 12: Microswitch SW2

FUNCTION	DESCRIPTION	DEFAULT
1- System Boot Flash	OFF: Normal Mode ON: Rescue Mode	OFF
2 - BIOS FAILSAFE	OFF: Normal Mode ON: BIOS FAILSAFE Mode	OFF
3- Reserved	OFF: Reserved ON: Reserved	OFF
4 - Force PROCHOT	OFF: Normal Mode ON: SoC PROCHOT forced to low state; the processor core frequency is set to its lowest value.	OFF

3.4.3. Microswitch SW3 Description

Table 13: Microswitch SW3

FUNCTION	DESCRIPTION	DEFAULT
1- User Defined Switch 1	OFF: User Defined ON: User Defined	OFF
2- User Defined Switch 2	OFF: User Defined ON: User Defined	OFF
3- User Defined Switch 3	OFF: User Defined ON: User Defined	OFF
4- User Defined Switch 4	OFF: User Defined ON: User Defined	OFF

3.5. Board Insertion

ESD Sensitive Device! Precautions are listed in section "Safety Requirements".

Prerequisites:

- Board Configuration

Ensure that the board is configured in accordance with the application requirements. Refer to section "Board Configuration".

- Add-on cards installation

Ensure that all the needed add-on cards (PMC, XMC, M.2 modules, MiniPCIe/mSATA card) have been properly installed. Refer to section "

Installation of Expansion Cards and Mezzanines".

- Backplane and board checks

Ensure that no defect may damage the VM606x board or the backplane. In particular, a bent pin in a connector may damage the corresponding socket location which in turn could damage another connector pin etc. We advise to perfrom a quick inspection of the connectors on both the board and the backplane before insertion.

To insert the board into the chassis, proceed as follows:

1. Ensure that the chassis power supply is turned off.

2. Carefully insert the board until it makes contact with the backplane connectors. Be sure that the board is aligned with the backplane connectors.

3. Using the ejectors handles, engage the board with the backplane connectors. When the ejectors handles are locked, the board is fully installed.

4. Fasten the front panel retaining screws.

5. Connect and secure external interfacing cables to the board as required.

The VM606x is now ready for operation.

3.6. Board Removal

ESD Sensitive Device! Precautions are listed in chapter 3.1

To remove the board from the chassis, proceed as follows:

1. Turn off power.

2. Disconnect any interfacing cables that may be connected to the board.

3. Loosen the front panel retaining screws.

4. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.

5. After disengaging the board from the backplane, pull the board out of the slot.

HOT Surface!

Since the heat sink may be very hot, do not touch it when handling the board. Let the board cool to room temperature before further manipulation.

6. Dispose of the board as required.

3.7. Installation of Expansion Cards and Mezzanines

3.7.1. M.2 Module Insertion / Removal Instructions

- **Supported M.2 Modules Types**

The socket S1 is compliant with both SATA and PCIe x2 standards with autodetect connection.
This socket can host the following module types: 2242-XX-M and 2260-XX-M with XX = S1, S2, S3, D1, D2, D3, D4.

The socket S1 is not compliant with D5 form factor.

The socket S3 supports only SATA devices. PCIe is not supported.

This socket can host the following module types: 2242-XX-M with XX = S1, S2, S3, D1, D2, D3, D4, D5.

A M.2 module in S3 socket and the PMC1/XMC1 keep-out IO area overlap. This module and the PMC1/XMC1 mezzanine cannot be mounted at the same time.

- **Mechanical Parts**

The mechanical parts are supplied in a bag.

Mechanical parts for the assembly of a M.2 module on socket S1:

- Standoff socket S1 (H3.2): 1061-9015.
- Metallic washer: 1061-2434
- M2x6 Screw: 1058-7783

Mechanical parts for the assembly of a M.2 module on socket S3:

- Standoff socket S3 (H4.2): 1060-4972.
- Metallic washer: 1061-2434
- M2x6 Screw: 1058-7783

- **M.2 Module Assembly**

ESD Sensitive Device! Precautions are listed in chapter 3.1

To install a M.2 module, proceed as follows:

1. Turn off power.

2. Insert the module with an angle of 25° until it touches the ramp.

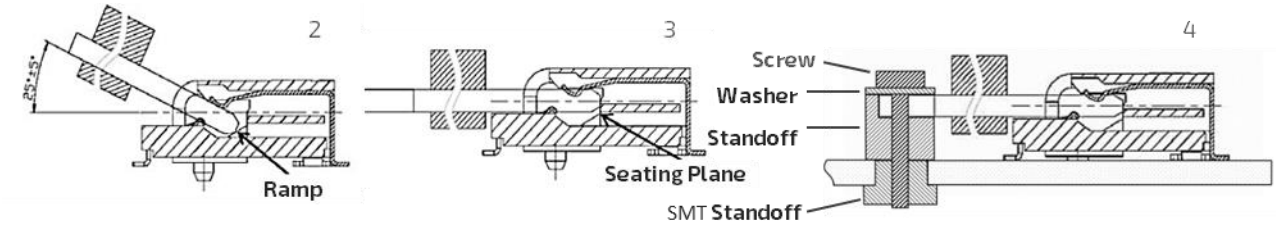
3. Rotate the module to horizontal position and make sure the card edge touches the seating plane.

4. Attach module to PCB

4.a Place stand-off between module and VM606x PCB.

4.b Add Washer and screw. Thread locker and torque as required by application.

Figure 11: M.2 Module Assembly



3.7.2. MiniPCIe / mSATA Card Insertion / Removal Instructions

The S2 socket for MiniCPIe or mSATA cards is an "on demand" option. Please contact Kontron.

Supported MiniPCIe Card Type

The MiniPCIe socket S2 can host full size MiniPCIe or mSATA cards. The MiniPCIe card type may be F1 or F2.

Mechanical Parts

The mechanical parts are supplied in a bag.

Mechanical parts for the assembly of a MiniPCIe or mSATA card on socket S2:

- Nylon washers M2.5x5.5x0.8mm: 2x 1058-0799
- M2x6 screws: 2x 1058-7783

MiniPCIe or mSATA Card Assembly

ESD Sensitive Device! Precautions are listed in chapter 3.1

To install a MiniPCIe or mSATA card, proceed as follows:

1. Turn off power.
2. Place the nylon washers on the SMT standoffs on PCB.
3. Start the card insertion (card notch aligned with connector key), then reduce the angle to about 25° and engage the card fully in connector.
4. Screw the two M2x6 screws. Thread locker and torque as required by application.

Figure 12: MiniPCIe Card Assembly

3.7.3. Battery Replacement

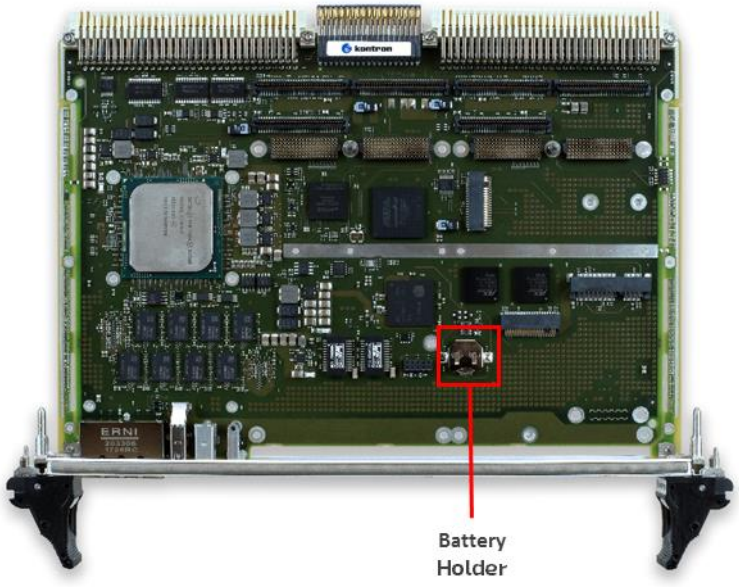
- Battery Part Number

Reference of the battery for VM606x-SA: RENATA CR1220 MFR (-30/+70°C)

Reference of the battery for VM606x-RA: RAYOVAC BR1225X-BA (-40/+85°C)

- Battery Replacement

Figure 13: Battery Holder Location



To replace the battery, proceed as follows:

1. Turn off power.
2. Use a thin plastic tool to push the battery out of its holder.

NOTICE Do not subject the holder to mechanical stress when inserting the tool to eject battery.

3. Remove the battery.
4. Place the new battery into the socket with positive side (+) upwards and negative side (-) closest to printed circuit board

⚠CAUTION **Danger of explosion when replacing with wrong type of battery. Replace only with the same or equivalent type recommended by the manufacturer. The lithium battery type must be UL recognized.**

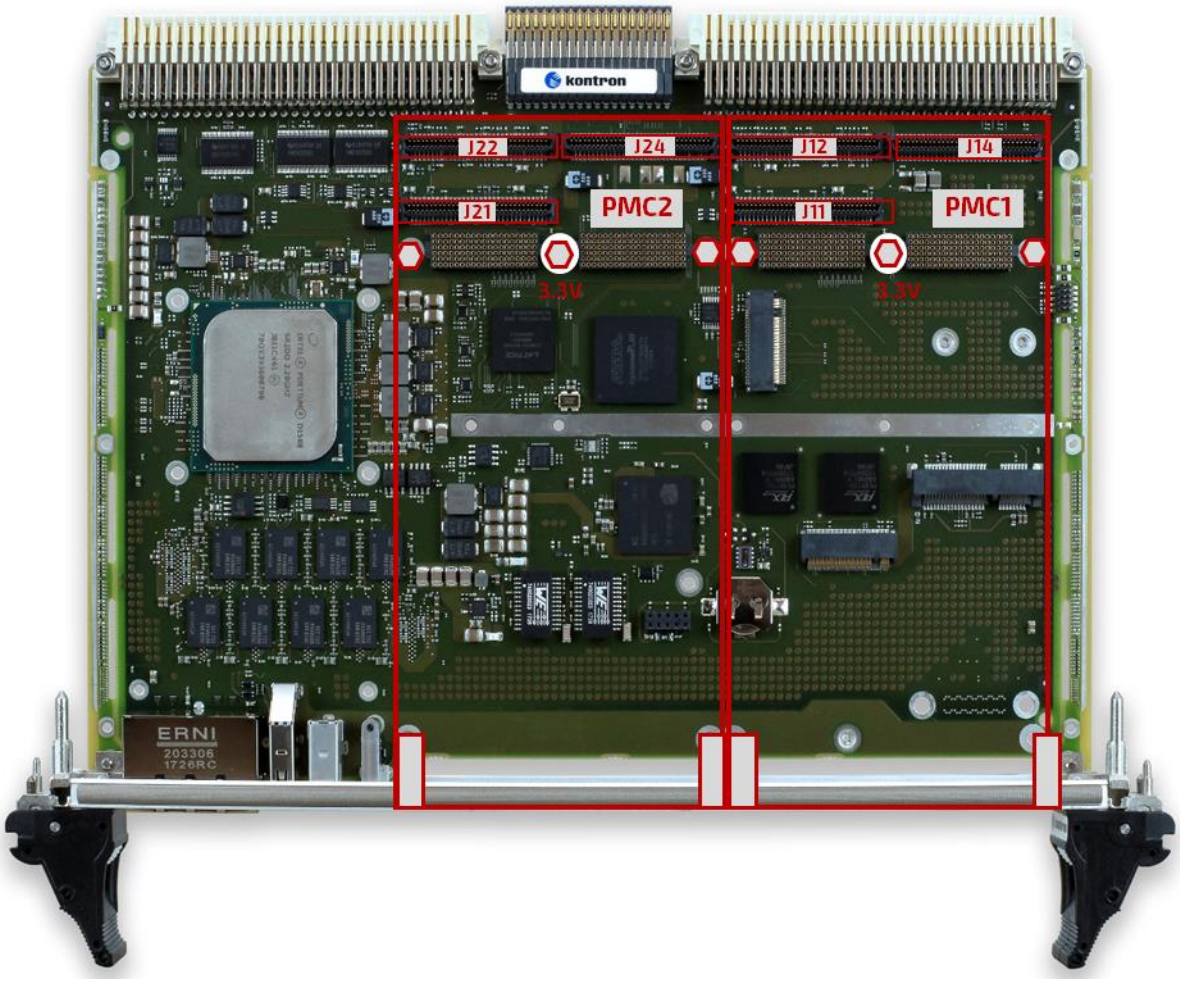
Do not dispose of lithium batteries in general trash collection. Dispose of the battery according to the local regulations dealing with the disposal of these special materials, (e.g. to the collecting points for dispose of batteries).

3.7.4. PMC Installation

- Supported PMC type

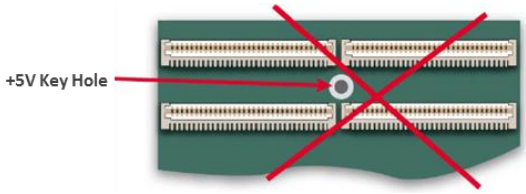
The VM606x supports 66 MHz, 32-bit PMCs (J23 is not equipped). The +5V keying pin is not present because +5V V(I/O) are not supported.

Figure 14: PMC1 & PMC2 Identification, PMC Connectors Location, +3.3V Keying Pins



+5V V(I/O) PMCs are not supported. Do not remove the +3.3V keying pin. Do not insert +5V V(I/O) PMCs as this may lead to electrical hazards and damage the PMC or the VM606x.

Figure 15: Identification of +5V V(I/O) PMCs



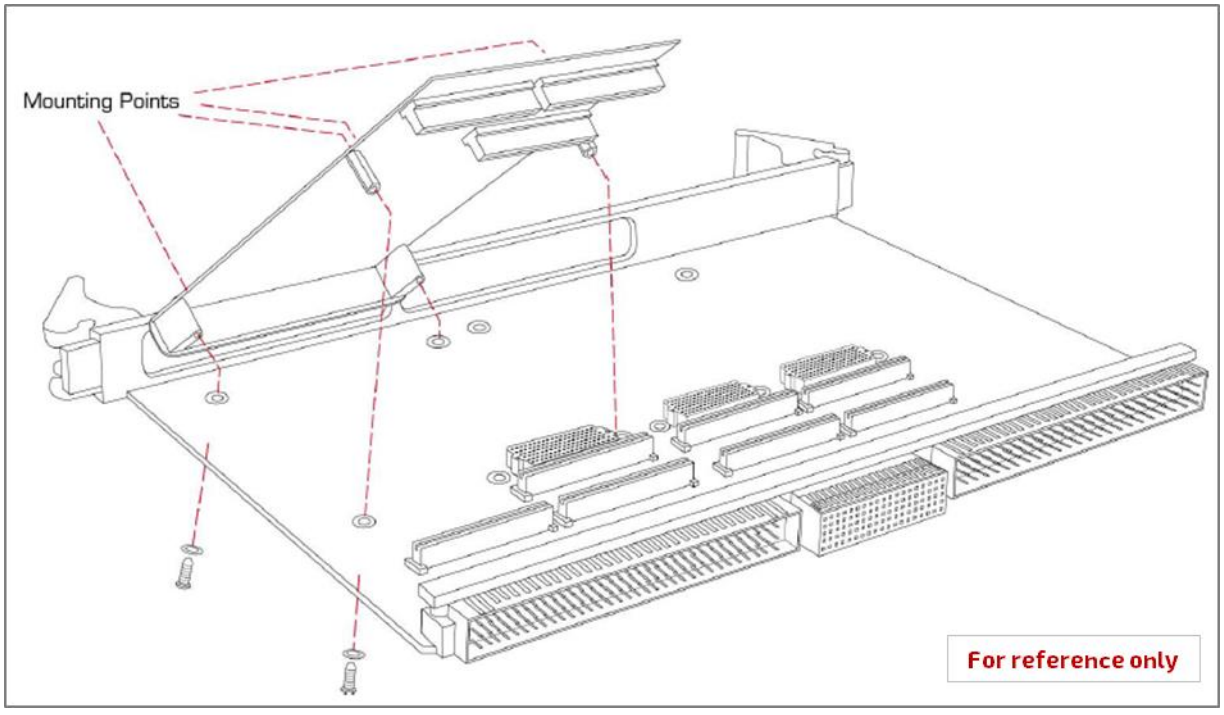
PMC installation

ESD Sensitive Device! Precautions are listed in chapter 3.1

To install a PMC, proceed as follows:

1. Turn off power.
2. Remove the blank PMC front panel.
3. Check that the standoffs are attached to the PMC.
4. Engage the PMC bezel into the front panel of the VM606x. Align the PMC connectors while ensuring that the 3.3V V(I/O) key on the VM606x does not prevent mating. Press to fully engage the PMC in the VM606x.
5. Screw the PMC in place using the four mounting points. Thread locker and torque as required by application.

Figure 16: PMC Installation



3.7.5. XMC Installation

- **Supported XMC type**

The default XMC connectors are VITA 42 compliant and support PCI-Express 2.0 signals.

The VM606x can be accommodated with VITA 61 XMC 2.0 compliant connectors which are designed for PCI-Express 3.0 support.

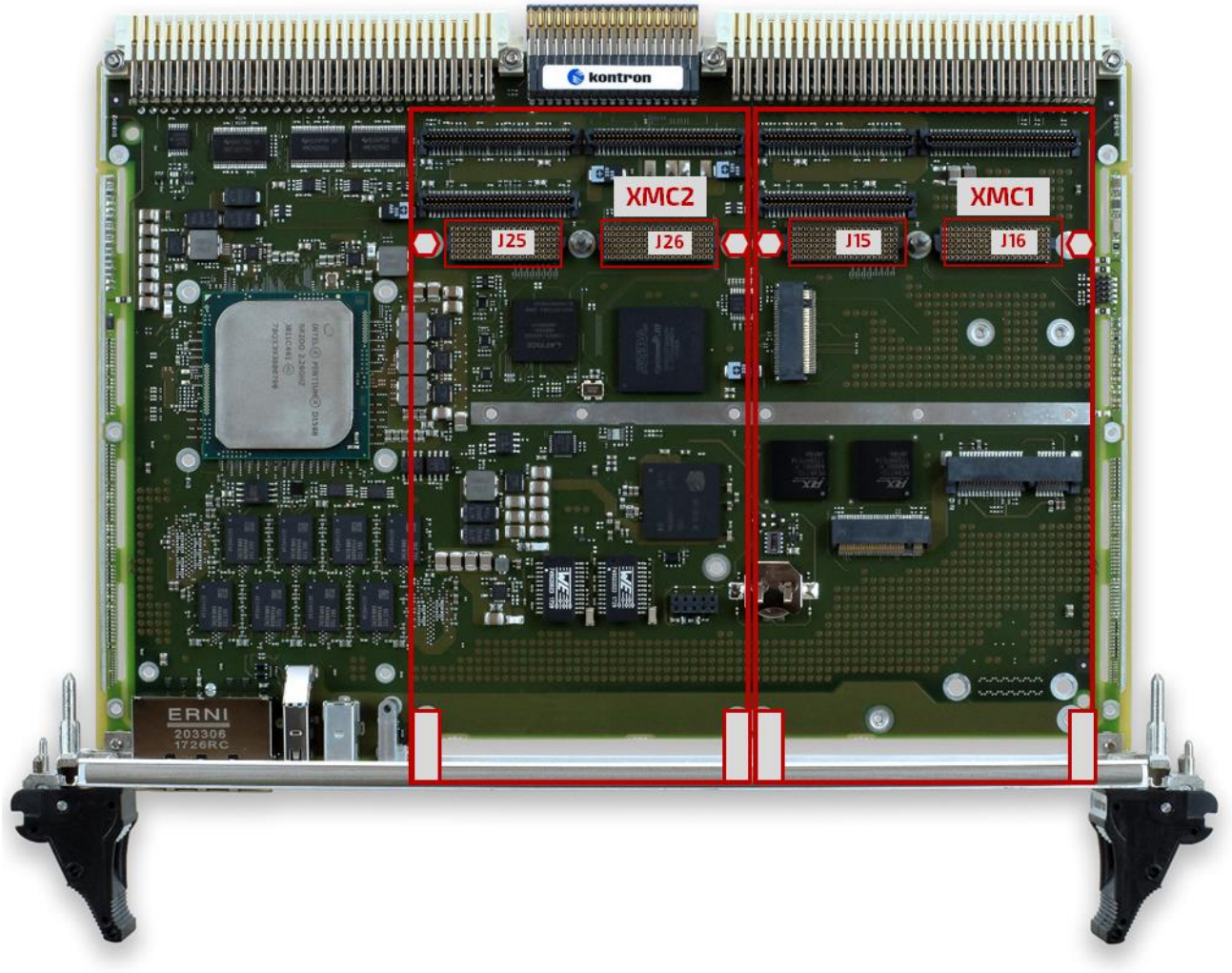
The VM606x supports two XMCs with a x4 and x8 PCIe interface for XMC1 and XMC2, respectively.

Both XMC IOs connectors (J16 & J26) are equipped. Refer to sections 5.3.1 & 5.3.3 for XMC IOs routing.

The XMC stack is 10 mm.

The connector type is VITA 42 (PCIe gen2). For a XMC2 i.e. VITA 61 (PCIE gen3) interface, please contact Kontron.

Figure 17: XMC1 & XMC2 Identification, XMC Connectors Location.



VITA 42 and VITA 61 XMC connectors are easily recognizable by their color:
Black for VITA 42 and white for VITA 61.

Figure 18: VITA 42 vs VITA 61 XMC Connectors

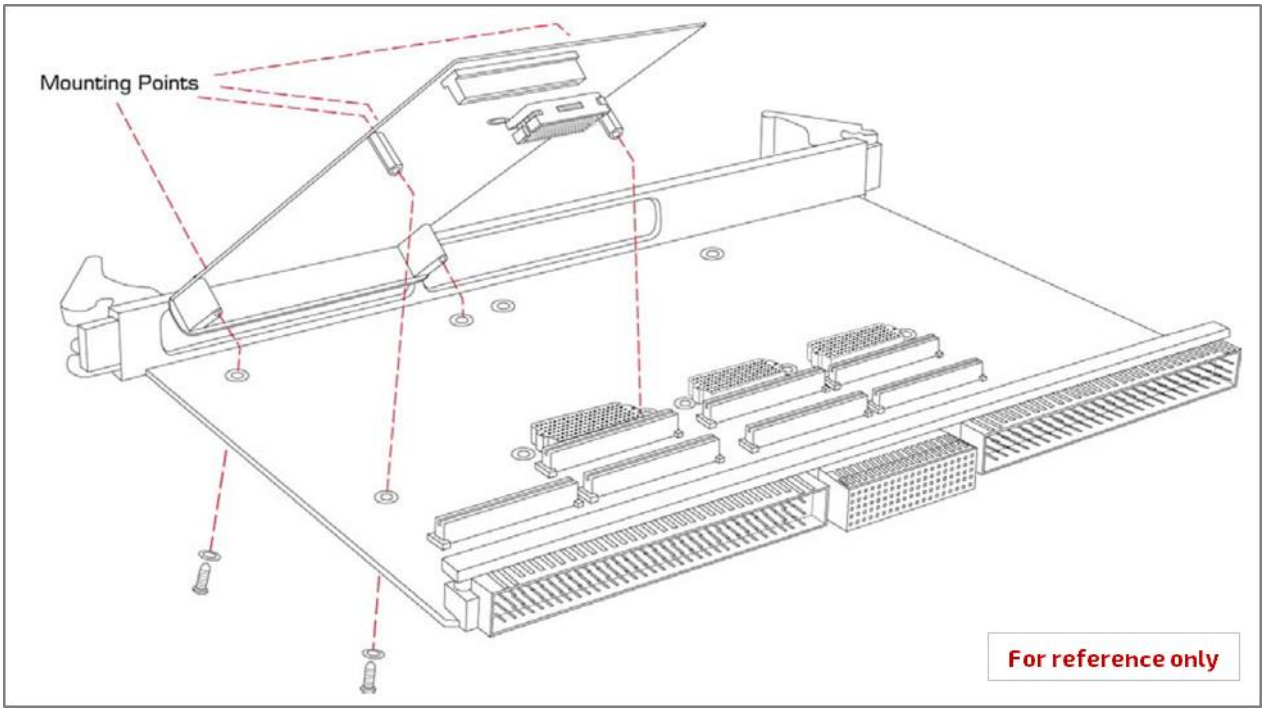
- XMC installation

ESD Sensitive Device! Precautions are listed in chapter 3.1

To install a XMC, proceed as follows:

1. Turn off power.
2. Remove the blank XMC front panel.
3. Check that the standoffs are attached to the XMC.
4. Engage the XMC bezel into the front panel of the VM606x. Align the XMC connectors. Press to fully engage the XMC in the VM606x.
5. Screw the XMC in place using the four mounting points.

Figure 19: XMC Installation



3.8. Software Installation

The installation of all onboard peripheral drivers is described in detail in the relevant Driver Kit files or Board Support Packages (BSP).

The installation of an operating system is dependent of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.

4/ Additional Board Features

4.1. RTC, Watchdog

4.1.1. Real-Time Clock (RTC)

Two Real Time Clocks (RTC) are available on the VM606x: one is embedded in the PCH of the SoC while the other is a standalone, high-precision, low-power component located on the SoC-SMBus (RV-8564 by Micro Crystal). The latter is more precise and is the only one powered when the board is off.

- **Standby power supplied to the RV-8564 RTC**

When the VM606x is powered off, the RTC is powered through Schottky diodes either by the onboard battery or the local 3.3V Standby power supply derived from the VME +5VSTDBY power rail or the VME V_BAT_EXT input (P0).

The maximum current drawn by the RTC is 500 nA at 25°C and 650 nA in -40°C/+85°C temperature range (VBAT= 3 V, no I2C activity).

The RTC present in the PCH of the SoC is never powered by the battery.

- **Internal PCH RTC**

The RTC module inside the SoC PCH provides a date and time keeping device with two banks of static RAM with 128 bytes each. The BIOS programs the RTC interrupt on Legacy IRQ8 that is never shared with other interrupts. It is clocked by the 32.768 kHz clock from the RV-8564 RTC.

- **Standalone low-power RTC RV-8564**

The RV-8564-C2/B RTC by Micro Crystal features an internal oscillator, date and time keeping module with programmable alarm, timer and interrupt functions. It has an ultra low-power consumption in time keeping mode: 250 nA, typical and 500 nA, maximum. Its stability is +/- 20 ppm at 25°C (equivalent to a drift of 10 mn per year). Its parabolic coefficient is 0.035 ppm/°C^2. It is connected to the SoC-SMBus. Its 32.768 kHz clock output drives the PCH RTC clock and the CPLD.

- **RTC management by BIOS and OS**

At each startup, the BIOS retrieves the date and time information from the high-precision RV-8564 RTC and copies it into the PCH RTC inside the SoC. This is necessary since the PCH RTC is not saved.

Any update of date and time in the BIOS settings will be done both in PCH RTC and RV-8564 RTC.

Regarding the RTC management by the OS, the OS should use the high-precision RV-8564 RTC driver. Failing to do so, the updates will be done only in PCH RTC and will not be saved.

If no power is applied on the RV-8564 RTC, the BIOS displays the BIOS build date and time instead of the current date and time.

- **Century flag**

For compatibility reasons, the BIOS implements the century flag for the high-precision RTC as follows:

- Century Flag C = 0 for 1900-1999 years
- Century Flag C = 1 for 2000-2099 years.

The user should check that the OS driver implements the same convention.

4.1.2. CPLD Watchdog

In addition to the standard watchdog timer included in the integrated PCH, the CPLD implements a hardware watchdog timer that can be used by the operating software to monitor the normal operation of the system.

It is enabled by hardware or software, and once enabled must be restarted at regular intervals. If not, its expiration sets off an interrupt (IRQ) to the local processor, a board reset or a board power-cycle.

The watchdog has the following features:

- Timeout programmable from 1 to 511 clock periods, by steps of 2 periods
- Clock periods of 1s or 1ms
- Lock bit: when set, can only refresh (restart) the watchdog, but not change its settings
- Four modes: timer, reset, interrupt or power-cycle
- Restart counter: can manage the remaining number of resets or power-cycles done by the watchdog before giving-up.

4.2. I2C Busses

See also Block Diagram in section 2.2.

- **Bus SoC-DDRI2C**

Description:

- SPD EEPROM access from the SoC.

Devices (8-bit add.):

- Master: SoC (DDR_SDA/SCL)
- SPD EEPROM - DDR0 @0xA0 (8-bit) @0x50 (7-bit)
- SPD EEPROM - DDR1 @0xA4 (8-bit) @0x52 (7-bit)

- **Bus SoC-SMBUS**

Description:

- Access to various local devices from the SoC.
- Three possible speeds: 100 kHz (Standard mode), 357 kHz (Fast mode), 750 kHz (Fast mode plus).

Devices (8-bit add.):

- Master: SoC (SMBDATA/CLK)
- Voltage sensor ADS7830 @0x96 (8-bit) @0x4B (7-bit)
- RTC RV-8564 @0xA2 (8-bit) @0x51 (7-bit)
- XMC1 @0xA4 (8-bit) @0x52 (7-bit)
- XMC2 @0xA8 (8-bit) @0x54 (7-bit)

- MiniPCIe socket S2

- **I2C bus CPLD-I2CLOC**

Description:
- Access to various local devices from the CPLD.
- Master: CPLD
- VPD EEPROM @0xA0 (8-bit) @0x50 (7-bit)
- OS EEPROM @0xA2 (8-bit) @0x51 (7-bit)
- FRAM @0xA4 0xA6 (8-bit) @0x52 @0x53 (7-bit)
- Nuvoton NCT7802Y @0x50 (8-bit) @0x28 (7-bit)
- Three temperature sensors LM73 @0x90 (8-bit) @0x48 (7-bit) / 0x92 (8-bit) @0x49 (7-bit) / 0x94 (8-bit) @0x4A (7-bit)

- **I2C bus VME-IPMBus**

Description:
- PMBus on VME backplane (P1)

Devices:
- Master/Slave: CPLD
- Connected to P1.B21/B22

- **I2C bus VME-SMBus**

Description:
- SMBus on VME backplane (P1)

Devices:
- Master: CPLD (and only if board is System Controller)
- Connected to P1.D19/D21

- **I2C bus SM750-I2CHDMI**

Description:
- Routed from SM750 to HDMI receptacle for display management.

Devices:
- Master: SM750
- HDMI receptacle (front panel)

4.3. Battery

- **Battery location and replacement**

Refer to section 3.7.3 Battery Replacement.

- **Battery Life**

Since the capacity of CR1220 MFR by Renata is 40 mAh, and the current drawn by RTC RV-8564-C2 is 500 nA at 25°C, the expected battery life is 9 years in the absence of external power.

4.4. CPLD features

4.4.1. Overview

The CPLD handles:

- Power-on/off management
- Onboard voltage regulators sequencing and monitoring
- Reset management
- LPC interface to processor
- I2C interface to rear SMBus and VME-IPMBus
- I2C interface to serial VPD EEPROM, OS EEPROM and FRAM device (PLD-I2CLOC @1.04MHz)
- I2C interface to Nuvoton monitor device NCT7802Y and LM73 temperature sensors (CPLD-I2CLOC @99.2kHz)
- Front LEDs for board status display
- Serial lines configuration (EIA-232 vs EIA-422/585)
- The direction of various dynamic switches which can be configured to front or rear: LAN switches of ETH0 and ETH1, USB switch of USB2[3] interface, graphics switch of HDMI interface.
- GPIOs
- Internal registers, board configuration (switches) and system management

The CPLD registers can be accessed by the processor on the LPC bus. The I2C registers 0x72 to 0x7B in the CPLD - which are described in the next chapter - can also be accessed from any master of the I2C bus VME-IPMBus.

For a detailed description of other CPLD registers, please contact Kontron.

4.4.2. CPLD I2C Registers

- **I2C0 and I2C1 interfaces:**

The two CPLD I2C interfaces I2C0 and I2C1 are connected to rear VME-IPMBus and VME-SMBus, respectively.
I2C0 is a master/slave interface while I2C1 is a master-only interface available only on the system controller board.

- **VME-IPMBus and VME-SMBus master interface:**

For information about how to handle the master interface of VME-IPMBus and VME-SMBus in the BSP, please contact Kontron.

- **VME-IPMBus slave interface:**

The VME-IPMBus slave register base address depends on the VME slot ID (geographical address of the slot):
VME Slot 1: slave interface base address is 0x30 (8-bit) or 0x18 (7-bit)

VME Slot 2: slave interface base address is 0x32 (8-bit) or 0x19 (7-bit)
VME Slot 3: slave interface base address is 0x34 (8-bit) or 0x1A (7-bit)
etc.

I2C Registers Overview

Table 14: I2C Registers of CPLD

OFFSET	REGISTER ID	DESCRIPTION	ACCESS
0x72	I2C_BOARD_STATUS	Board Status	RW
0x73	I2C_BOARD_CONTROL	Board Status and Control	RW
0x74	I2C_ERROR_STATUS	Board Error State	RW
0x75	Port_80	Port 80 lower byte	-
0x76	Reserved	-	-
0x77	Reserved	-	-
0x78	I2C_MISC	Miscellaneous Board Information	RW
0x79	POWER_ERROR_1	Power Good Signals - Part 1	RO
0x7A	POWER_ERROR_2	Power Good Signals - Part 2	RO
0x7B	POWER_ERROR_1	Power Good Signals - Part 2	RO
0xE	BOARD_ID_Extension	Board ID Extension	RO

Table 15: I2C_BOARD_STATUS @0x72

I2C_BOARD_STATUS @ 0x72 Can also be accessed from I2C0 slave interface with register offset 0				
Bit #	Bit ID	Description	Reset	Access
7	Power Status	**Power Status** (used by CMB board to read power status) 0: Power Stand By 1: Power ON (PWROK_STATE State just before S0	0	RO
6-5	Reset Origin	**Origin of Last Reset Detected** 00: Internal power supplies power-on 01: CPLD Watchdog expired 10: SYSRESET# (from VME) 11: Other Reset sources : Front Reset Push Button Soft Reset (bit 1 register @73) SoC Soft Reset (through register CF9h)	00	RO
4	Reset Status	**Reset Status** 0: PCH_PWROK not asserted OR one of the following Reset asserted: Front Reset Push Button Soft Reset (bit 1 register @73) 1: PCH_PWROK asserted AND Reset not asserted	0	RO
3-0	Boot Status	**Boot Status** 0x00 RESET : default hardware value 0x01 BIOS-BOOT : written by BIOS 0x02 BIOS : written by BIOS 0x03 PBIT : written by BIOS 0x04 OS-BOOT : written by BIOS	0000	RW

I2C_BOARD_STATUS @ 0x72 Can also be accessed from I2C0 slave interface with register offset 0				
Bit #	Bit ID	Description	Reset	Access
		0x05:OS-RUNNING : to be written by OS at the end of boot 0x06 COMPLETED: to be written by the final application when running 0x07 SHUTDOWN: to be written by OS when issuing a halt/shutdown 0x08 REBOOT: to be written by OS when rebooting 0x09 - 0x0B: Reserved 0x0C - 0x0F: Customer defined These bits are RO through I2C Slave Interface and RW through LPC Interface. The boot status is also reset at each board reset.		

Table 16: I2C_BOARD_CONTROL @0x73

I2C_BOARD_CONTROL @ 0x73 Can also be accessed from I2C0 slave interface with register offset 0x01				
Bit #	Bit ID	Description	Reset	Access
7-4	Board ID	**Board Identification** 1110: Board ID to be found in Board ID Extension register @ 0xE (same 8bit value as BOARD_ID@0x01, not accessible from LPC bus)	000	RO
3	Reserved	This bit must be left at 0. Do not write 1 in this register.	0	RW
2	Reserved	-	-	-
1	Reset	**Reset** 0: No Reset 1: Reset Asserted	0	RW
0	Power_OnOff	**Power On/Off Control** 0: Power Off (StandBy Mode) 1: Power On This bit can always be used to power on or off, and its default value is loaded when standby is applied from inverted VPD EEPROM offset 0x100 bit 1, if FACTORY mode is not enabled WARNING Setting this bit to 0 asserts VME SYSRESET (the board does not fully support standby because of Alma2f and its VME buffers)	*	RW

Table 17: I2C_ERROR_STATUS @0x74

I2C_ERROR_STATUS @ 0x74 Can also be accessed from I2C0 slave interface with register offset 0x02				
Bit #	Bit ID	Description	Reset	Access
7	ALERT	**Alert Detection** 0: no alert 1: alert pending from PLD_PECI_ALERT# or PLD_PCHHOT_CPU# See register ALERT_STATUS@5B bit 0 and 3 for current state on these signals See register SERIRQ_CONTROL@0xF bit 6 and 2 for interrupt Mask and Status	0	RO
6	POST_ERROR	**Power On Self Test Error** 0: no POST error 1: POST error This bit is set when PBIT has been run with errors (according to reg 0x2) Also set when RTC battery is low (according to reg 0x3 bit 0)	0	RO
5	POST_RTC	**RTC Power On Self Test Error** 0: no RTC POST error 1: RTC POST failed (weak or missing battery) This bit is a copy of reg 0x3 bit 0 (POST_RTC), that is set when RTC battery is low	0	RO
4-0	ERROR_CODE	**Error Code** 0x10: VMEPWRGD_UV 0x11: VMEPWRGD_OV 0x0C: PECI_CRIT# 0x0D: VRVCCIN_VRHOT# Or VR1V05_VRHOT 0x0E: THERMTRIP# 0x0F: CATERR# 0x1F: "Onboard PSUs Error" Other: Reserved When an unmasked fatal alert occurs, this register is updated, all internal PSUs are switched off and the error status is also reported on the front panel LEDs. See Also registers @7A and @7B	0	RO

Table 18: PORT_80 @ 0x75

PORT_80 @ 0x75 Can also be accessed from I2C0 slave interface with register offset 0x03				
Bit #	Bit ID	Description	Reset	Access
7	PORT 80	**Port 80 lower byte** The value of this register is automatically updated at each write access to port 0x80 (write snooping). It is cleared at each reset.	0	RW (LPC) RO (I2C)

Table 19: I2C_MISC @ 0x77

SCRATCHPAD @ 0x77 Can also be accessed from I2C0 slave interface with register offset 0x05				
Bit #	Bit ID	Description	Reset	Access
7	Scratch Pad	User Defined Register	0	RW

Table 20: I2C_MISC @ 0x78

I2C_MISC @ 0x78 Can also be accessed from I2C0 slave interface with register offset 0x06				
Bit #	Bit ID	Description	Reset	Access
7	FORCE_RESCUE_BIOS	**Force Rescue Boot Flash Device** 0: Boot Flash Device selected according to microswitch SW2.1. 1: Boot Flash Device forced to Rescue Boot Flash.	0	RW
6-0	Reserved	Reserved	-	-

Table 21: POWER ERROR part 1 @0x79

POWER_ERROR_1 @ 0x79 Can also be accessed from I2C0 slave interface with register offset 0x07				
Bit #	Bit ID	Description	Reset	Access
7-0	See description	Power Good Signals - Part 1 Bit 7 : 1V5 Bit 6 : 1V5_MPCIE Bit 5 : 3V3_M2 Bit 4 : 3V3_MPCIE Bit 3 : P3V30 Bit 2 : P3V3SB Bit 1 : VCCKRHV Bit 0 : VCCSCFUSESUS An error is reported if at least one power supply does not start within the expected delay (timeout) or fails after being up. This register is cleared by switching the board off (standby) or by turning off VME power rails.	0	RO

Table 22: POWER ERROR part 2 @0x7A

POWER_ERROR_2 @ 0x7A Can also be accessed from I2C0 slave interface with register offset 0x08				
Bit #	Bit ID	Description	Reset	Access
7-0	See description	Power Good Signals - Part 2 This register indicates what are the Power rails failed when apower error is detected (see also register @079) Bit 7 : VINT_ALMA2F Bit 6 : VR1V05 Bit 5 : VR1V2_DDR4 Bit 4 : VR1V5_PCH Bit 3 : VR2V5_DDR4 Bit 2 : VR3V3 Bit 1 : VR3V3SUS Bit 0 : VRVCCIN SoC An error is reported if at least one PSU does not start within the expected delay (timeout) or fails after being up. This register is cleared by switching the board off (standby) or by turning off VME power rails.	0	RO

Table 23: SAFETY_ALERTS @0x7B (Includes POWER_ERROR part 3 and Safety Errors)

POWER_ERROR_2 @ 0x7B Can also be accessed from I2C0 slave interface with register offset 0x09				
Bit #	Bit ID	Description	Reset	Access
7-6	See description	**Power Good Signals - Part 3** This register indicates what are the Power rails failed when a power error is detected (see also register @079) Bit 7 : VTT Bit 6 : WAKEUP Error An error is reported if at least one PSU does not start within the expected delay (timeout) or fails after being up. This register is cleared by switching the board off (standby) or by turning off VME power rails.	0	RO
5-0	See description	**Critical Error Status** Bit 5: Critical Alert (See register @74 for details) Bit 4 : THERMTRIP# Bit 3 : VRVCCIN_VRHOT# Bit 2 : VR1V05_VRHOT# Bit 1 : CATERR# Bit 0 : PECI_CRIT# When a fatal alert occurs, this register is updated. If ALERT_INHIB bit of register PWR_RST_CONFIG@04 is set to 0, all internal power supplies are switched off and the error status is also reported on the front panel LEDs. See Also registers @79 @7A.	0	RO

Table 24: BOARD_ID_Extension @0xE

BOARD_ID_Extension – No LPC access This register is an image of BOARD_ID@ 0x01 and can only be accessed from I2C0 slave interface with register offset 0x0E				
Bit #	Bit ID	Description	Reset	Access
7-0	BOARD_ID	0x63: VM6062 0x64: VM6064	-	RO

4.5. Serial Lines: EIA-422/485 Mode

The EIA-232 mode is the default mode for COM1 and COM2 serial lines. EIA-422/485 mode can be selected through BIOS settings along with an optional on-board 120-Ohm termination and a half-duplex option.

Table 25: Availability of EIA-232 and EIA-422/485 modes on COM serial ports.

MODE	FRONT PANEL CONNECTOR	P2 REAR CONNECTOR
EIA-232 (default)	COM1, COM2	COM1, COM2
EIA-422/485 (BIOS setting)	Contact Kontron.	COM1, COM2

For detailed pin assignment of front and rear connectors, refer to sections 5.1.1 and 5.3.3.

4.6. GPIOs

The VM606x features 14 GPIOs managed by the CPLD. For information about the GPIO driver, please contact Kontron.

- Three GPIOs are available on P0 connector: GPIO1, GPIO2 and GPIO3.
- Three GPIOs are available on P2 connector: GPIO4, GPIO5 and GPIO6.
- Two additional GPIOs on P2 come with manufacturing "Rear IOs P2" option 1 or 2: GPIO7 and GPIO8.
- On demand: Six additional GPIOs on P2 with manufacturing "Rear IOs P2" option 2: GPIO9 to GPIO14.

The GPIOs share the same interrupt in the CPLD.

Table 26: GPIOs

GPIO	Rear connection	Multiplexed with	Can be isolated from connector	Availability (equipment key)
GPIO1	P0.C10	not multiplexed	yes	Always
GPIO2	P0.D10	not multiplexed	yes	Always
GPIO3	P0.E10	not multiplexed	yes	Always
GPIO4	P2.D30	not multiplexed	no	Always
GPIO5	P2.D29	not multiplexed	no	Always
GPIO6	P2.Z31	not multiplexed	no	Always
GPIO7	P2.A32	PMC1_IO64	yes	Manufacturing Option "Rear IOs P2": Option 1 or 2

GPIO	Rear connection	Multiplexed with	Can be isolated from connector	Availability (equipment key)
GPIO8	P2.C32	PMC1_IO63	yes	Manufacturing Option "Rear IOs P2": Option 1 or 2
GPIO9	P2.D28	not multiplexed	yes	Manufacturing Option "Rear IOs P2": Option 2 on demand
GPIO10	P2.D27	not multiplexed	yes	Manufacturing Option "Rear IOs P2": Option 2 on demand
GPIO11	P2.D26	not multiplexed	yes	Manufacturing Option "Rear IOs P2": Option 2 on demand
GPIO12	P2.Z29	COM2_RX485+	yes	Manufacturing Option "Rear IOs P2": Option 2 on demand
GPIO13	P2.Z27	COM2_TX485+	yes	Manufacturing Option "Rear IOs P2": Option 2 on demand
GPIO14	P2.Z25	COM2_RX232_ RX485-	yes	Manufacturing Option "Rear IOs P2": Option 2 on demand

4.7. Reset

Except for the VME reset, the processor Watchdog Reset and the SoC Soft Reset, all the reset sources are managed by the CPLD. To generate a reset, the CPLD activates the SoC input SYS_RESET_N. This leads to the activation by the SoC of the platform reset signal PLTRST_N.

Table 27: Reset Sources Description

RESET SOURCE	RESET STATUS	NOTE
Internal Power Supplies Power On	CPLD register @0x72 accessed from local LPC bus or from rear VME-IPMBus	
Front panel reset push button		Refer to reset propagation options and masks in CPLD registers.
Activation of VME SYSRESET*		Refer to VME VITA 1 standard and ALMA2f documentation.
Rear VME-IPMBus soft reset (write to CPLD register @0x73 bit 1 from rear VME-IPMBus)		Base address on rear VME-IPMBus depends on Board slot number (VME Geographical Address)
CPLD soft reset (write to CPLD register @0x73 bit 1 from local processor via LPC bus)		Refer to register definition in this user guide
CPLD watchdog reset		Refer to software release notes
SoC soft reset (write to SoC Reset Control register CF9h)		
Processor watchdog reset	Intel® Xeon® D watchdog status registers	Refer to Intel® Xeon D-15xx watchdog control registers

4.8. EEPROMs and Flash Devices Write Protection

4.8.1. EEPROMs and Flash Devices Summary

There are three types of write-protection which define three groups of EEPROMs: SYS, USER, VPD. These groups are detailed in Table 28.

Table 28: EEPROM and Flash Devices Summary

Group	Name	Description	Function	Access	WP signal read back in CPLD	Related Switch
SYS	OS EEPROM	I2C 256-Kbit EEPROM	EEPROM used by PBITs	I2C bus CPLD-I2CLOC	CPLD 0x7D[6]	-
	XMC1	XMC EEPROM	XMC EEPROM	SMBus Soc-SMBUS	CPLD 0x7D[7]	-
	XMC2	XMC EEPROM	XMC EEPROM	SMBus Soc-SMBUS	CPLD 0x7D[7]	-
USER	Boot Main	128-Mbit SPI Flash	BIOS Boot Flash (Main)	SoC SPI0 interface	CPLD 0x7D[1]	SW1-4 ON=GND
	Boot Rescue	128-Mbit SPI Flash	BIOS Boot Flash (Rescue)	SoC SPI1 interface	CPLD 0x7D[1]	SW1-4 ON=GND
	FRAM	1-Mbit FRAM	FRAM	I2C bus CPLD-I2CLOC	CPLD 0x7D[2]	SW1-4 ON=GND
VPD	SPDs	I2C 4-kbit EEPROM	DDR Bank 0 SPD DDR Bank 1 SPD	I2C bus SoC-DDRI2C	CPLD 0x7D[4]	SW1-3 ON=GND
	VPD	I2C 256-kbit EEPROM	System (VPD) EEPROM	I2C bus CPLD-I2CLOC	CPLD 0x7D[5]	SW1-3 ON=GND
	i210IT	8-Mbit SPI Flash	ETH0 & ETH1 i210IT 1000BASE-T	Through i210 device	CPLD 0x7D[3]	SW1-3 ON=GND
	SM750	256-kbit SPI Flash	VBIOS of SM750 A	Through SM750 device	CPLD 0x7D[3]	SW1-3 ON=GND
	ALMA2f	64-Mbit SPI Flash	VME bridge	Through ALMA2f bridge	CPLD 0x7D[3]	SW1-3 ON=GND

4.8.2. Write protection SYS_WP

- **Description:**

This type of protection applies to the SYS group of EEPROMs and SPI Flash devices.
The priority defined from highest to lowest is:

- NVMRO high (provided that the factory mode switch SW1[1] is OFF),
- CPLD bit @0x09-Bit2 high.

- **Equation:**

Device protected when:
(NVMRO=1 & SW1[1]=OFF) | (NVMRO=0 & @0x09-Bit2=1)

- **Truth table:**

NVMRO	SW1[1]	CPLD @0x09-Bit2	PROTECTION
1	OFF	X	YES
1	ON	0	NO
1	ON	1	YES
0	X	0	NO
0	X	1	YES

X="don't care"

4.8.3. Write protection USER_WP

- **Description:**

This type of protection applies to the USER group of SPI Flash and FRAM devices. The priority defined from highest to lowest is:

  - NVMRO high (provided that the factory mode switch SW1[1] is OFF),
  - switch SW1[4] ON, CPLD bit @0x09-Bit3 high.

- **Equation:**

Device protected when

(NVMRO=1 & SW1[1]=OFF) | (NVMRO=0 & SW1[4]=ON) | (NVMRO=0 & SW1[4]=OFF & @0x09-Bit3=1)

- **Truth table:**

NVMRO	SW1[1]	SW1[4]	CPLD @0x09-Bit3	PROTECTION
1	OFF	X	X	YES
1	ON	ON	X	YES
1	ON	OFF	0	NO
1	ON	OFF	1	YES
0	X	ON	X	YES
0	X	OFF	0	NO
0	X	OFF	1	YES

X="don't care"

4.8.4. Write protection VPD_WP

- **Description:**

This type of protection applies to the VPD group of EEPROMs and SPI Flash devices. The protection is disabled when SW1[3] is ON. When SW1[3] is OFF, the priority defined from highest to lowest is:

  - NVMRO high (provided that the factory mode switch SW1[1] is OFF),
  - CPLD bit @0x09-Bit1 high.

- **Equation:**

Device protected when

SW1[3]=OFF & ((NVMRO=1 & SW1[1]=OFF) | (NVMRO=0 & @0x09-Bit1=1))

- **Truth table:**

SW1[3]	NVMRO	SW1[1]	CPLD @0x09-Bit1	PROTECTION
ON	X	X	X	NO
OFF	1	OFF	X	YES
OFF	1	ON	0	NO
OFF	1	ON	1	YES
OFF	0	X	0	NO
OFF	0	X	1	YES

X="don't care"

4.9. Security Devices

4.9.1. Trusted Platform Module

The TPM (Trusted Platform Module) is a security hardware device normalized by the Trusted Computing Group (TCG). It is accessed through the LPC bus using a standardized API.

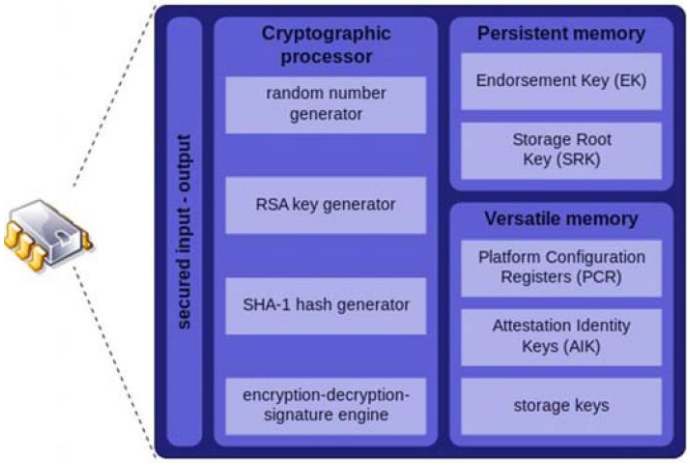
In the trusted boot usage, the TPM is active from the very first block of instructions executed after reset and during the entire boot. Unlike secure boot, the TPM does not block or restrict execution. Its role is rather to:

> Calculate a hash value on a set of submitted data using a dedicated algorithm (SHA-1 for TPM1.2).

> Provide a way of storing and using private keys without external manipulations.

> Deliver local and remote attestations based on the calculated hash value, certifying that the software run from reset to the end of boot has not been modified with respect to some reference code.

Figure 20: Trusted Platform Module



4.9.2. APPROTECT and the CodeMeter ASIC Technology by Wibu

APPROTECT is part of Kontron SEC-Line computer security offering. This secure element implements the CodeMeter ASIC technology by Kontron partner Wibu, to protect the application from the main security threats:

- Integrity: discourage persons from code tampering and checks circumventing.
- Confidentiality: prevent the information concerning application software from being snooped out of code execution (reverse engineering).
- Unauthorized copies: prevent copyright or licensing infringement.

Technical information:

- Security Hardware: Infineon SLM-97CUSIFX1M00 smart card chip
- Encryptions standards: 128 bit AES, SHA-256, 2048 bit RSA, 224 bit ECC

5/ Physical IOs

5.1. Front Panel Connectors

Figure 21: Front Panel Connectors

5.1.1. Serial Connector - COM1 & COM2

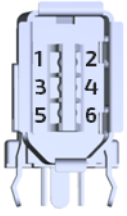
This section describes the IEEE 1394 front connector carrying serial ports COM1, COM2.

- Front Serial Connector Description

Table 29: Serial Connector Pin Assignment

Figure 22: Serial Connector (IEEE 1394 Type)

Pin	Signal
1	Reserved
2	GND
3	COM1 RXD / COM1 RXD-
4	COM2 RXD / COM1 RXD+
5	COM1 TXD / COM1 TXD-
6	COM2 TXD / COM1 TXD+



NOTICE

CAUTION: Serial lines are routed to both front panel connector and rear P2. Plugging a serial device to both connectors will lead to electrical contention. Be sure to use only one connector at a time.

Table 30: Serial Connector Signals Definition

Signal	Dir.	Definition
COM1 TXD / COM1 TXD-	O	EIA-232: Transmit Data of port COM1 EIA-485: Transmit Data minus of port COM1
COM1 RXD / COM1 RXD-	I	EIA-232 Receive Data of port COM1 EIA-485: Receive Data minus of port COM1
COM2 TXD / COM1 TXD+	O	EIA-232: Transmit Data of port COM2 EIA-485: Transmit Data plus of port COM1
COM2 RXD / COM1 RXD+	I	EIA-232: Receive Data of port COM2 EIA-485: Receive Data plus of port COM1

Signal	Dir.	Definition
Reserved	-	Reserved
GND	-	Logic ground
Shell	-	Chassis ground

Note: EIA-485 protocol requires special configuration. Contact Kontron.

- Serial Cable Description

Table 31: Serial Cable Description

Conn. A IEEE1394	Signal	Conn. B SUBD9
5	TXD	2
3	RXD	3
2	GND	5

5.1.2. Gigabit Ethernet Connector - Ports ETH0 & ETH1

This section describes the dual RJ45 front connector carrying 1000BASE-T Ethernet ports ETH0 & ETH1.

- Front Gigabit Ethernet Connector Description

Table 32: Gigabit Ethernet Connector Pin Assignment

Pin	Signal
1	TX+ / BI_DA+
2	TX- / BI_DA-
3	RX+ / BI_DB+
4	BI_DC+
5	BI_DC-
6	RX- / BI_DB-
7	BI_DD+
8	BI_DD-
Shell	Chassis Ground

Figure 23: RJ45 Tab-down Ethernet Connector

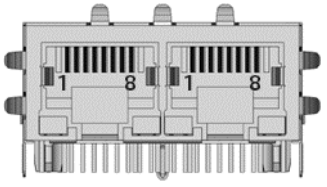


Table 33: Gigabit Ethernet Connector Signals Definition

Signal	Dir.	Definition
TX+/- / BI_DA+/-	I/O	10BASE-T & 100BASE-T: Transmit differential pair 1000BASE-T: BI_DA differential pair
RX+/- / BI_DB+/-	I/O	10BASE-T & 100BASE-T: Receive differential pair 1000BASE-T: BI_DB differential pair
BI_DC+/-	I/O	10BASE-T & 100BASE-T: NC 1000BASE-T: BI_DC differential pair

BI_DD+/-	I/O	10BASE-T & 100BASE-T: NC 1000BASE-T: BI_DD differential pair
Shell	-	Chassis ground

- **Ethernet Cable Description**

The Ethernet cable should be a CAT5e with a maximum length of 100 meters.

5.1.3. USB Connector

This section describes the USB front connectors carrying USB 3.0 ports USBSS.

Table 34: USB Connector Pin Assignment

Pin	Signal
1	VBUS
2	D-
3	D+
4	GND
5	STDA_SSRX-
6	STDA_SSRX+
7	GND_DRAIN
8	STDA_SSTX-
9	STDA_SSTX+

Figure 24: USB 3.0 Series A Receptacle

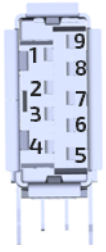


Table 35: Gigabit Ethernet Connector Signals Definition

Signal	Dir.	Definition
D+/-	I/O	Differential pair of USB 2.0 port FRONT_USB3. This port is connected to Xeon D USB 2.0 port 3. It is multiplexed with the rear USB 2.0 port P0_USB3. The multiplexor is controlled through CPLD.
GND	-	Logic ground.
GND_DRAIN	-	Mechanical Ground
STDA_SSRX+/-	I	SuperSpeed receiver differential pair
STDA_SSTX+/-	O	SuperSpeed transmitter differential pair
VBUS	O	+5V output rail. Protected by dedicated power switch (rated current: 1A, limit current: minimum 1.3A, typical 1.55A, maximum 1.8A).

5.1.4. HDMI Connector

Front HDMI Connector Description

This section describes the HDMI front connector carrying the port HDMI.

Table 36: HDMI Connector Pin Assignment

Pin	Signal
1	TMDS Data2+
3	TMDS Data2-
5	GND
7	TMDS Data0+
9	TMDS Data0-
11	GND
13	NC
15	SCL
17	GND
19	Hot plug detect

Signal	Pin
GND	2
TMDS Data1+	4
TMDS Data1-	6
GND	8
TMDS Clock+	10
TMDS Clock-	12
NC	14
SDA	16
+5V	18

Figure 25: Type A 19-position HDMI Receptacle

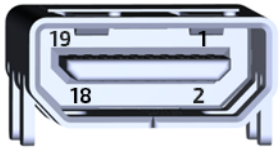


Table 37: HDMI Connector Signals Definition

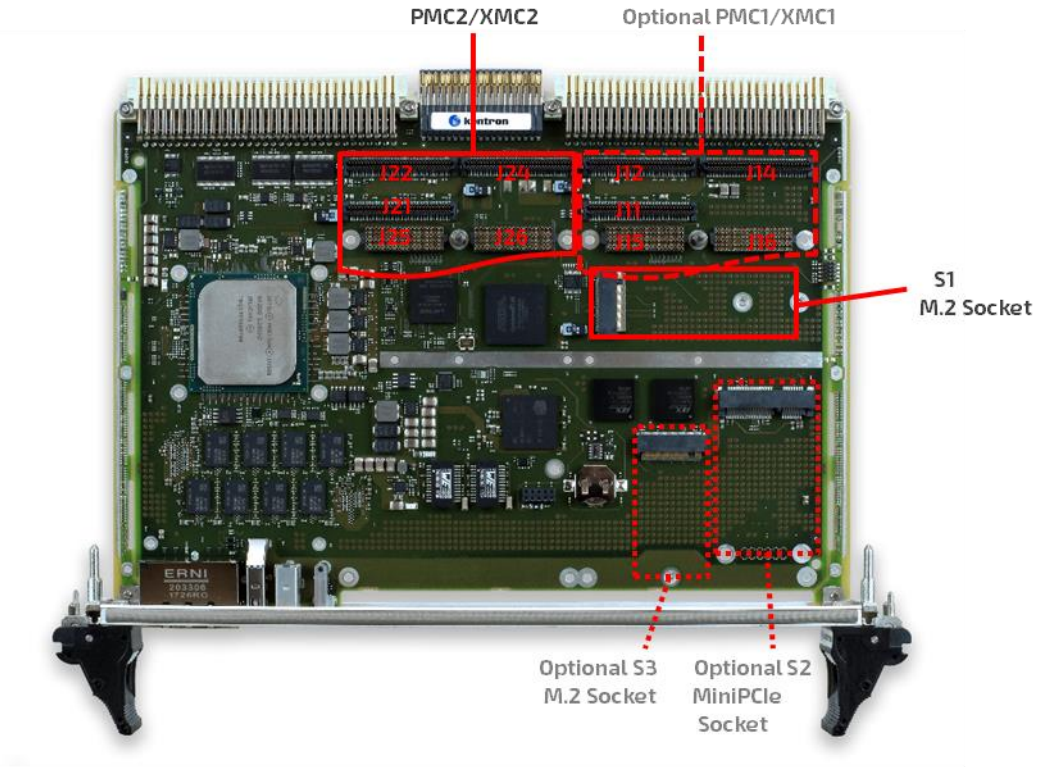
Signal	Dir.	Definition
SDA	I/O	I^2C serial clock for DDC
SCL	I/O	I^2C serial data for DDC
TMDS Data0+/-	I/O	TMDS 0 differential pair
TMDS Data1+/-	I/O	TMDS 1 differential pair
TMDS Data2+/-	I/O	TMDS 2 differential pair
TMDS Clock+/-	I/O	Clock differential pair
+5V	O	+5V output rail. Protected by 1A resettable fuse.
GND	-	Logic Ground
Hot plug detect	-	Hot plug detection.

HDMI Cable Description

A standard MicroHDMI-to-HDMI cable may be used.

5.2. Onboard Connectors

Figure 26: Onboard Connectors



5.2.1. PMC Connectors

5.2.1.1. PMC Connectors Jn1 & Jn2

This section describes the PMC connectors.

Table 38: PMC Connectors Jn1 & Jn2 Pin Assignment

Jn1 32-bit PCI			
Pin	Signal	Signal	Pin
1	TCK	-12V	2
3	GND	INTA#	4
5	INTB#	INTC#	6
7	BUSMODE1#	+5V	8
9	INTD#	NC	10
11	GND	+3.3V_SUS	12
13	CLK	GND	14
15	GND	GNT#	16
17	REQ#	+5V	18
19	V(I/O)	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	GND	24
25	GND	C/BE3#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	V(I/O)	AD[17]	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	DEVSEL#	+5V	38
39	PCIXCAP	LOCK#	40
41	SDONE#	SBO#	42
43	PAR	GND	44
45	V(I/O)	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	GND	C/BE0#	52
53	AD[06]	AD[05]	54
55	AD[04]	GND	56
57	V(I/O)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	GND	REQ64#	64

Jn2 32-bit PCI			
Pin	Signal	Signal	Pin
1	+12V	TRST	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	NC	8
9	NC	NC	10
11	BUSMODE2#	+3.3V	12
13	RST#	BUSMODE3#	14
15	+3.3V	BUSMODE4#	16
17	PME#	GND	18
19	AD[30]	AD[29]	20
21	GND	AD[26]	22
23	AD[24]	+3.3V	24
25	IDSEL	AD[23]	26
27	+3.3V	AD[20]	28
29	AD[18]	GND	30
31	AD[16]	C/BE2#	32
33	GND	IDSEL B	34
35	TRDY#	+3.3V	36
37	GND	STOP#	38
39	PERR#	GND	40
41	+3.3V	SERR#	42
43	C/BE1#	GND	44
45	AD[14]	AD[13]	46
47	M66EN	AD[10]	48
49	AD[08]	+3.3V	50
51	AD[07]	REQ B#	52
53	+3.3V	GNT B#	54
55	NC	GND	56
57	NC	EREADY	58
59	GND	NC	60
61	ACK64#	+3.3V	62
63	GND	NC	64

Table 39: PMC Connectors Jn1 & Jn2 Signals Definition

Signal	Dir.	Definition
AD[31:00]	I/O	Multiplexed address and data bus as per PCI standard.
ACK64#	Target Output	Acknowledge 64-bit Transfer as per PCI standard. On VM606x, pulled up to V (I/O).
BUSMODE1#	O	Bus Mode 1 as per PCI standard. On VM606x, handled by CPLD.
BUSMODE2#	O	Bus Mode 2 as per PCI standard. On VM606x, pulled up to V (I/O).
BUSMODE3#	O	Bus Mode 3 as per PCI standard. On VM606x, pulled down to GND.
BUSMODE4#	O	Bus Mode 4 as per PCI standard. On VM606x, pulled down to GND.
C/BE#[3:0]	Initiator Output	Command/Byte Enables as per PCI standard.
CLK	I	Clock as per PCI standard.
DEVSEL#	Target Output	Device Select as per PCI standard.
FRAME#	Initiator Output	FRAME as per PCI standard.
EREADY	I/O	EREADY as per PCI standard. On VM606x, not handled.
GNT#	I	PCI bus Grant as per PCI standard.
GNTB#	I	PCI bus Grant B (processor-PMC modules) as per PCI standard.
IDSEL	I	Initialization Device Select. as per PCI standard.
IDSEL B#	I	Initialization Device Select. (processor-PMC modules) as per PCI standard.
INTA# to INTD#	O	Interrupt lines. as per PCI standard.
IRDY#	Initiator Output	Initiator Ready. as per PCI standard.
LOCK#	Initiator Output	LOCK as per PCI standard.
M66EN	OD	66 MHZ Enable as per PCI standard.
PAR	I/O	Parity as per PCI standard.
PCIXCAP	OD	PCIXCAP as per PCI standard. On VM606x, pulled-down to GND. VM606x PMC1 & PMC2 sites are not PCIX capable.
PERR#	O	Parity Error as per PCI standard.
PMC-RSVD	-	Reserved as per PCI standard.. Do not connect this pin.
PME#	O	Power Management Event as per PCI standard.
REQ#	O	Bus request as per PCI standard.
REQ B#	O	Bus request (processor-PMC modules) as per PCI standard.
REQ64#	Initiator Output	64-bit transfer bus request as per PCI standard. On VM606x, not supported.
RST#	I	Reset as per PCI standard.
SBO#	Initiator Output	Snoop Backoff as per PCI standard.
SDONE#	Initiator Output	Snoop Done as per PCI standard.
SERR#	OD	System error as per PCI standard.
STOP#	Target Output	STOP as per PCI standard.
TCK	I	JTAG clock as per PCI standard. On VM606x, not implemented. Contact Kontron if needed.
TDI	I	JTAG Data In as per PCI standard. On VM606x, not implemented. Contact Kontron if needed.
TDO	O	JTAG Data Out as per PCI standard. On VM606x, not implemented. Contact Kontron if needed.
TMS	I	JTAG Mode Select as per PCI standard. On VM606x, not implemented. Contact Kontron if needed.
TRST#	I	JTAG Reset as per PCI standard. On VM606x, not implemented. Contact

Signal	Dir.	Definition
		Kontron if needed.
TRDY#	Target Output	Target Ready as per PCI standard.
V(I/O)	Power	Signalling power rail as per PCI standard. On VM606x, V(I/O) is set to +3.3 V and 5V V(I/O) PMCs are not supported.
+3.3V	Power	3.3 V power rail as per PCI standard.
+5V	Power	5 V power rail as per PCI standard.
+12V	Power	12 V power rail as per PCI standard.
-12V	Power	- 12 V power rail as per PCI standard.
GND	Power	Logic Ground

NOTICE

PMC sites PMC1 and PMC2 are not 5V-tolerant. V(I/O) must be +3.3 VDC.

5.2.1.2. PMC IO Connectors Jn4

This section describes the PMC IO connectors.

Table 40: PMC Connectors Jn4 Pin Assignment

Pin	Signal	Signal	Pin
1	PMC IO 01	PMC IO 02	2
3	PMC IO 03	PMC IO 04	4
5	PMC IO 05	PMC IO 06	6
7	PMC IO 07	PMC IO 08	8
9	PMC IO 09	PMC IO 10	10
11	PMC IO 11	PMC IO 12	12
13	PMC IO 13	PMC IO 14	14
15	PMC IO 15	PMC IO 16	16
17	PMC IO 17	PMC IO 18	18
19	PMC IO 19	PMC IO 20	20
21	PMC IO 21	PMC IO 22	22
23	PMC IO 23	PMC IO 24	24
25	PMC IO 25	PMC IO 26	26
27	PMC IO 27	PMC IO 28	28
29	PMC IO 29	PMC IO 30	30
31	PMC IO 31	PMC IO 32	32

Pin	Signal	Signal	Pin
33	PMC IO 33	PMC IO 34	34
35	PMC IO 35	PMC IO 36	36
37	PMC IO 37	PMC IO 38	38
39	PMC IO 39	PMC IO 40	40
41	PMC IO 41	PMC IO 42	42
43	PMC IO 43	PMC IO 44	44
45	PMC IO 45	PMC IO 46	46
47	PMC IO 47	PMC IO 48	48
49	PMC IO 49	PMC IO 50	50
51	PMC IO 51	PMC IO 52	52
53	PMC IO 53	PMC IO 54	54
55	PMC IO 55	PMC IO 56	56
57	PMC IO 57	PMC IO 58	58
59	PMC IO 59	PMC IO 60	60
61	PMC IO 61	PMC IO 62	62
63	PMC IO 63	PMC IO 64	64

Table 41: PMC Connectors Jn4 Signals Definition

Signal	Dir.	Definition
PMC IO [xx]	I/O	PMC IOs connected to P0 or P2.

5.2.2. XMC Connectors

5.2.2.1. XMC Connectors Jn5

This section describes the XMC connectors.

Table 42: XMC Connectors Jn5 Pin Assignment

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR
4	GND	GND	TCK	GND	GND	NC
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR
6	GND	GND	NC	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR
8	GND	GND	NC	GND	GND	-12V
9	NC	NC	NC	NC	NC	VPWR
10	GND	GND	NC	GND	GND	GA0
11	PER0p0	PER0n0	NC	PER0p1	PER0n1	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PER0p2	PER0n2	3.3V AUX	PER0p3	PER0n3	VPWR
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	NC	PER0p5	PER0n5	VPWR
16	GND	GND	NVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	NC	PER0p7	PER0n7	NC
18	GND	GND	NC	GND	GND	NC
19	REFCLK+0	REFCLK-0	NC	WAKE#	NC	NC

Table 43: XMC Connectors Jn5 Signals Definition

Signal	Dir.	Definition
GA[0..2]	O	I2C channel select as per VITA42.0.
GND	-	Logic ground.
MRSTI#		XMC Reset In as per VITA42.0 (10 ms pulse min.) and PCIe PERST# as per VITA42.3.
MSDA	I/O	I2C serial data as per VITA42.0.
MSCL	O	I2C serial clock as per VITA42.0.
NVMRO	O	XMC Write Prohibit as per VITA42.0.
PRESENT#	I	Module present as per VITA42.0.
TCK	O	JTAG Clock as per VITA42.0.
TDI	O	JTAG Data In as per VITA42.0.
TDO	I	JTAG Data Out as per VITA42.0.
TMS	O	JTAG Mode Select as per VITA42.0.
TRST#	O	JTAG Reset as per VITA42.0.
PET0p/n[0..7]	I	PCIe differential transmit pairs 0 to 7 (as per VITA 42.3).
PER0p/n[0..7]	O	PCIe differential receive pairs 0 to 7 (as per VITA 42.3) .
REFCLK+/-0	O	100MHz PCIe differential reference clock as per VITA 42.3.
VPWR	O	+5V or +12V power pins as per VITA42.0. On VM606x, defaults to +5V but may be set to +12V by optional equipment. Protected by a 4.5 A fuse which is common to the PMC and XMC located in the same site.
WAKE#	I	Open drain WAKE# signal
+12V	O	+12V power pin. Connected to VPWR by 0402 resistor. Protected by the same fuse as VPWR.
-12V	O	-12V power pin. Protected by 1.1A, resettable fuse.
3.3V	O	+3.3V power pin. Protected by 3.5A resettable fuse.
3.3V AUX	O	Auxiliary +3.3V.

5.2.2.2. XMC IO Connectors Jn6

This section describes the XMC IO connectors.

Table 44: XMC Connectors Jn6 Pin Assignment

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	XMC1 XMC IO DP1+ XMC2 XMC IO DP1+	XMC1 XMC IO DP1- XMC2 XMC IO DP1	XMC1 XMC IO S1 XMC2 XMC IO S1	XMC1 XMC IO DP2+ XMC2 XMC IO DP2+	XMC1 XMC IO DP2- XMC2 XMC IO DP2-	XMC1 XMC IO S2 XMC2 XMC IO S2
2	GND	GND	NC	GND	GND	NC
3	XMC1 XMC IO DP3+ XMC2 XMC IO DP3+	XMC1 XMC IO DP3- XMC2 XMC IO DP3-	XMC1 XMC IO S3 XMC2 XMC IO S3	XMC1 XMC IO DP4+ XMC2 XMC IO DP4+	XMC1 XMC IO DP4- XMC2 XMC IO DP4-	XMC1 XMC IO S4 XMC2 XMC IO S4
4	GND	GND	NC	GND	GND	NC
5	XMC1 XMC IO DP5+ XMC2 NC	XMC1 XMC IO DP5- XMC2 NC	XMC1 XMC IO S5 XMC2 XMC IO S5	XMC1 XMC IO DP6+ XMC2 NC	XMC1 XMC IO DP6- XMC2 NC	XMC1 XMC IO S6 XMC2 XMC IO S6
6	GND	GND	XMC1 XMC IO S21 XMC2 NC	GND	GND	XMC1 XMC IO S22 XMC2 NC
7	XMC1 XMC IO DP7+ XMC2 NC	XMC1 XMC IO DP7- XMC2 NC	XMC1 XMC IO S7 XMC2 XMC IO S7	XMC1 XMC IO DP8+ XMC2 NC	XMC1 XMC IO DP8- XMC2 NC	XMC1 XMC IO S8 XMC2 XMC IO S8
8	GND	GND	NC	GND	GND	NC
9	XMC1 XMC IO DP9+ XMC2 NC	XMC1 XMC IO DP9- XMC2 NC	XMC1 XMC IO S9 XMC2 XMC IO S9	XMC1 XMC IO DP10+ XMC2 NC	XMC1 XMC IO DP10- XMC2 NC	XMC1 XMC IO S10 XMC2 XMC IO S10
10	GND	GND	NC	GND	GND	NC
11	XMC1 XMC IO DP11+ XMC2 XMC IO DP11+	XMC1 XMC IO DP11- XMC2 XMC IO DP11-	XMC1 XMC IO S11 XMC2 XMC IO S11	XMC1 XMC IO DP12+ XMC2 XMC IO DP12+	XMC1 XMC IO DP12- XMC2 XMC IO DP12-	XMC1 XMC IO S12 XMC2 XMC IO S12
12	GND	GND	NC	GND	GND	NC
13	XMC1 XMC IO DP13+ XMC2 XMC IO DP13+	XMC1 XMC IO DP13- XMC2 XMC IO DP13-	XMC1 XMC IO S13 XMC2 XMC IO S13	XMC1 XMC IO DP14+ XMC2 XMC IO DP14+	XMC1 XMC IO DP14- XMC2 XMC IO DP14-	XMC1 XMC IO S14 XMC2 XMC IO S14
14	GND	GND	NC	GND	GND	NC
15	XMC1 XMC IO DP15+ XMC2 NC	XMC1 XMC IO DP15- XMC2 NC	XMC1 XMC IO S15 XMC2 XMC IO S15	XMC1 XMC IO DP16+ XMC2 NC	XMC1 XMC IO DP16- XMC2 NC	XMC1 XMC IO S16 XMC2 XMC IO S16
16	GND	GND	NC	GND	GND	NC
17	XMC1 XMC IO DP17+ XMC2 NC	XMC1 XMC IO DP17- XMC2 NC	XMC1 XMC IO S17 XMC2 NC	XMC1 XMC IO D1P8+ XMC2 NC	XMC1 XMC IO DP18- XMC2 NC	XMC1 XMC IO S18 XMC2 NC
18	GND	GND	XMC1 XMC IO S23 XMC2 NC	GND	GND	XMC1 XMC IO S24 XMC2 NC
19	XMC1 XMC IO DP19+ XMC2 NC	XMC1 XMC IO DP19- XMC2 NC	XMC1 XMC IO S19 XMC2 NC	XMC1 XMC IO DP20+ XMC2 NC	XMC1 XMC IO DP20- XMC2 NC	XMC1 XMC IO S20 XMC2 NC

Table 45: XMC Connectors Jn6 Signals Definition

Signal	Dir.	Definition
XMC1 XMC IO Sxx	I/O	XMC IO single-ended signal [xx]. Site XMC1.
XMC1 XMC IO DPxx+/-	I/O	XMC IO differential pair [xx]. Site XMC1.
XMC2 XMC IO Syy	I/O	XMC IO single-ended signal [yy]. Site XMC2.
XMC2 XMC IO Dyy+/-	I/O	XMC IO differential pair [yy]. Site XMC2.

5.2.3. M.2 Module Socket

This section describes the M.2 socket connectors.

Table 46: M.2 Sockets Pin Assignment

Socket S1

Pin	Signal (1)	Signal (1)	Pin
74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK (32kHz)	PEDET	69
	Connector Key	NC	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	NC	GND	57
56	NC	REFCLKP	55
54	PEWAKE#	REFCLKN	53
52	NC	GND	51
50	PERST#	PETp0 / SATA-A+	49
48	NC	PETn0 / SATA-A-	47
46	Reserved	GND	45
44	Reserved	PERp0 / SATA-B-	43
42	NC	PERn0 / SATA-B+	41
40	NC	GND	39
38	NC	PETp1	37
36	NC	PETn1	35
34	NC	GND	33
32	NC	PERp1	31
30	NC	PERn1	29
28	Reserved	GND	27
26	Reserved	NC	25
24	NC	NC	23
22	Reserved	GND	21
20	Reserved	NC	19
18	3.3V	NC	17
16	3.3V	GND	15
14	3.3V	NC	13
12	3.3V	NC	11
10	LED1# / DAS_DSS#	GND	9
8	NC	NC	7
6	NC	NC	5
4	3.3V	GND	3
2	3.3V	GND	1

Socket S3

Pin	Signal (1)	Signal (1)	Pin
74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK (32kHz)	PEDET	69
	Connector Key	NC	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	NC	GND	57
56	NC	REFCLKP	55
54	PEWAKE#	REFCLKN	53
52	NC	GND	51
50	PERST#	SATA-A+	49
48	NC	SATA-A-	47
46	NC	GND	45
44	NC	SATA-B-	43
42	NC	SATA-B+	41
40	NC	GND	39
38	NC	NC	37
36	NC	NC	35
34	NC	GND	33
32	NC	NC	31
30	NC	NC	29
28	NC	GND	27
26	NC	NC	25
24	NC	NC	23
22	NC	GND	21
20	NC	NC	19
18	3.3V	NC	17
16	3.3V	GND	15
14	3.3V	NC	13
12	3.3V	NC	11
10	DAS_DSS#	GND	9
8	NC	NC	7
6	NC	NC	5
4	3.3V	GND	3
2	3.3V	GND	1

(1) When PCI Express and SATA function coexist the following convention applies: PCI Express_function / SATA_function.

Table 47: M.2 Socket Signals Definition

Signal (1) PCI Express / SATA	Dir.	Definition
3.3V	O	+3.3V power supply. On VM606x, protected by dedicated 1.5A resettable fuse (one for each M.2 socket).
GND	-	Logic ground.
LED1# / DAS_DSS#	I	- PCI Express: LED_1# indicator as per PCI Express M.2 specification. On VM606x connected to dedicated CPLD pin. - SATA: Device Activity Signal /Disable Staggered Spinup as per SATA 3.2. On VM606x, DAS is not connected to a LED (which is the main purpose of this signal) and DSS is not used since the devices are SSD and not hard drives (no spinup). Signal connected to dedicated CPLD pin.
PEDET	I	PEDET (PCI Express Detect) as per PCI Express M.2 specification is driven low by SATA modules and high-Z by PCI Express modules (seen as a logic 1 due to on-board pull-up resistor). On VM606x, this signal is connected to a dedicated CPLD pin.
PERn0 / SATA-B+	I	- PCI Express: Receive differential signal minus as per PCI Express M.2 & PCI Express 3.0 specifications. - SATA: Receive differential signal plus as per SATA 3.2.
PERp0 / SATA-B-	I	- PCI Express: Receive differential signal plus as per PCI Express M.2 & PCI Express 3.0 specifications. - SATA: Receive differential signal minus as per SATA 3.2.
PERST#	O	- PCI Express: PCI Express PERST# as per PCI Express M.2 specification. On VM606x handled by CPLD. - SATA: NC.
PETp/n0 / SATA-A+/-	O	- PCI Express : Transmit differential pairs as per PCI Express M.2 & PCI Express 3.0 specifications. - SATA: Transmit differential pair as per SATA 3.2.
PEWAKE#	I	- PCI Express: Open drain WAKE# signal as per PCI Express M.2 specification. Driven by M.2 module to allow the platform to reactivate the link main power rails and reference clock. On VM606x, this signal is wire-ORed with other WAKE# signals from i210 controllers and M.2 modules in the same A or B part. It is connected to SoC WAKE_# and WAKELAN_# pins. - SATA: NC.
REFCLKP/N	O	- PCI Express: PCI Express differential reference clock (100 MHz) as per PCI Express M.2 & PCI Express 3.0 specifications. - SATA: NC.
SUSCLK	O	Suspend Clock for low power mode handling as per PCI Express M.2 specification (32.768 kHz, duty cycle between 30% and 70%, 200ppm). On VM606x, connected to SoC SUSCLK_GPIO62.

(1) When PCI Express and SATA function coexist the following convention applies: PCI Express_function / SATA_function.

5.2.4. MiniPCIe Socket S2

The socket S2 - also referred to in this document as the MiniPCIe socket - can host Mini Card PCI Express add-in cards or mSATA add-in cards.

Table 48: MiniPICe Sockets Pin Assignment

Pin	Signal (1)	Pin	Signal (1)
51	Presence Detection	52	+3.3V
49	DAS/DSS	50	GND
47	NC	48	+1.5V
45	NC	46	NC
43	PCIEDET	44	NC
41	+3.3V	42	NC
39	+3.3V	40	GND
37	GND	38	USB_D+
35	GND	36	USB_D-
33	PETp0 / +A	34	GND
31	PETn0 / -A	32	SMB_DATA
29	GND	30	SMB_CLK
27	GND	28	+1.5V
25	PERp0 / -B	26	GND
23	PERn0 / +B	24	+3.3V
21	GND	22	PERST#
19	NC	20	NC
17	NC	18	GND
Mechanical Key			
15	GND	16	NC
13	REFCLK+	14	NC
11	REFCLK-	12	NC
9	GND	10	NC
7	CLKREQ#	8	NC
5	NC	6	+1.5V
3	NC	4	GND
1	WAKE#	2	+3.3V

(1) When PCIe and SATA function coexist the following convention applies: PCIe_function / SATA_function.

Table 49: MiniPCIe Socket Signals Definition

Signal (1)	Dir.	Definition
+1.5V	I	+1.5V power supply.
+3.3V	I	- mPCIE: +3.3V auxiliary voltage source. - mSATA: +3.3V voltage source - On VM606x, connected to +3.3V internal voltage and always present.
GND	-	Logic ground
USB_D+/-	I/O	- MiniPCIe: USB 2.0 differential data pair. - mSATA: NC - On VM606x, connected to SoC USB 2.0 interface USB2[1].
PETp/n0	I	- MiniPCIe: Host transmit differential pair of PCIe x1 data interface. An input of the MiniPCIe card. - mSATA: Host transmit differential pair of SATA interface. An input of the mSATA card.
PERp/n0	O	- MiniPCIe: Host receive differential pair of PCIe x1 data interface. An output of the MiniPCIe card. - mSATA: Host receive differential pair of SATA interface. An output of the mSATA card.
PCIEDET#	O	- MiniPCIe: GND - mSATA: NC - On VM606x, used as a presence detect of MiniPCIe card.
W_DISABLE2# / Presence Detection	O	- MiniPCIe: Signal used by system to disable radio operation on module as per MiniPCIe specification. - mSATA: Presence Detection . Pulled down by mSATA card. - On VM606x, used as mSATA presence detection. This pin is discarded if PCIEDET# is active (MiniPCIe card detected).
SMB_DATA	I/O	- MiniPCIe or mSATA: SMBus data signal. - On VM606x, connected to bus SoC-SMBus.
SMB_CLK	I	- MiniPCIe or mSATA: SMBus clock signal. - On VM606x, connected to bus SoC-SMBus.
PERST#	I	- MiniPCIe: PCIe functional reset. - mSATA: NC - On VM606x, reset handled by CPLD.
REFCLK+/-	I	- MiniPCIe: PCIe differential reference clock (100 MHz). - mSATA: NC - On VM606x, 100 MHz differentia clock.
CLKREQ#	O	- MiniPCIe: Open drain request driven by miniPCIe card to the platform to request activation of the PCIe clock. - mSATA: NC - On VM606x, pulled-up to 3.3V because PCIe clock is always running.
WAKE#	O	- MiniPCIe: Open drain request to reactivate the link main power rails and reference clock. - mSATA: NC - On VM606x, this signal is wire-ORed with WAKE# signal from XMC connectors and connected to CPLD and SoC's PCH.

(1) When PCIe and SATA function coexist the following convention applies: PCIe_function / SATA_function.

5.3. Rear Connectors

tototo

Figure 27: Rear Connectors

Table 50: Connector P0 Pin Assignment

Pin	Row A (1)	Row B (1)	Row C (1)	Row D (1)	Row E (1)	Row F
1	PMC2 IO 39 [39] or XMC2 IO S9 [C9]	PMC2 IO 38 [38] or XMC2 IO S8 [F7]	PMC2 IO 37 [37] or XMC2 IO S7 [C7]	PMC2 IO 36 [36] or XMC2 IO S6 [F5]	PMC2 IO 35 [35] or XMC2 IO S5 [C5]	GND
2	ETH0 DA+	ETH0 DA-	GND	ETH0 DC+	ETH0 DC-	GND
3	ETH0 DB+	ETH0 DB-	GND	ETH0 DD+	ETH0 DD-	GND
4	ETH1 DA+	ETH1 DA-	GND	ETH1 DC+	ETH1 DC-	GND
5	ETH1 DB+	ETH1 DB-	GND	ETH1 DD+	ETH1 DD-	GND
6	RESET#	USB3 PWR	NVMR0	V_BAT_EXT	USB0 PWR	GND
7	USB3 D+	USB3 D-	GND	USB0 D+	USB0 D-	GND
8	SATA0 TX+ (2)	SATA0 TX- (2)	GND	SATA0 RX+ (2)	SATA0 RX- (2)	GND
9	SATA1 TX+ (2)	SATA1 TX- (2)	GND	SATA1 RX+ (2)	SATA1 RX- (2)	GND
10	PMC2 IO 34 [34] or XMC2 IO S4 [F3]	PMC2 IO 33 [33] or XMC2 IO S2 [F1]	GPIO1	GPIO2	GPIO3	GND
11	PMC2 IO 58 [58] or XMC2 IO DP1+ [A1]	PMC2 IO 60 [60] or XMC2 IO DP1- [B1]	PMC2 IO 46 [46] or XMC2 IO S1 [C1]	PMC2 IO 48 [48] or XMC2 IO DP11+ [A11]	PMC2 IO 50 [50] or XMC2 IO DP11- [B11]	GND
12	PMC2 IO 62 [62] or XMC2 IO DP2+ [D1]	PMC2 IO 64 [64] or XMC2 IO DP2- [E1]	PMC2 IO 45 [45] or XMC2 IO S3 [C3]	PMC2 IO 52 [52] or XMC2 IO DP12+ [D11]	PMC2 IO 54 [54] or XMC2 IO DP12- [E11]	GND
13	PMC2 IO 61 [61] or XMC2 IO DP3+ [A3]	PMC2 IO 63 [63] or XMC2 IO DP3- [B3]	PMC2 IO 56 [56] or XMC2 IO S11 [C11]	PMC2 IO 51 [51] or XMC2 IO DP13+ [A13]	PMC2 IO 53 [53] or XMC2 IO DP13- [B13]	GND
14	PMC2 IO 57 [57] or XMC2 IO DP4+ [D3]	PMC2 IO 59 [59] or XMC2 IO DP4- [E3]	PMC2 IO 55 [55] or XMC2 IO S13 [C13]	PMC2 IO 47 [47] or XMC2 IO DP14+ [D13]	PMC2 IO 49 [49] or XMC2 IO DP14- [E13]	GND
15	RPCIE RX0+ (2)	RPCIE RX0- (2)	GND	RPCIE TX0+ (2)	RPCIE TX0- (2)	GND
16	opt RPCIE RX1+ (2) opt GND	opt RPCIE RX1- (2) opt RHDMI HPD	GND	opt RPCIE TX1+ (2) opt RHDMI SCL	opt RPCIE TX1- (2) opt RHDMI SDA	GND
17	opt RPCIE RX2+ (2) opt RHDMI TMDS0+	opt RPCIE RX2- (2) opt RHDMI TMDS0-	GND	opt RPCIE TX2+ (2) opt RHDMI TMDS1+	opt RPCIE TX2- (2) opt RHDMI TMDS1-	GND
18	opt RPCIE RX3+ (2) opt RHDMI TMDS2+	opt RPCIE RX3- (2) opt RHDMI TMDS2-	GND	opt RPCIE TX3+ (2) opt RHDMI CLK+	opt RPCIE TX3- (2) opt RHDMI CLK-	GND
19	PMC2 IO 44 [44] or XMC2 IO S16 [F15]	PMC2 IO 43 [43] or XMC2 IO S15 [C15]	PMC2 IO 42 [42] or XMC2 IO S14 [F13]	PMC2 IO 41 [41] or XMC2 IO S12 [F11]	PMC2 IO 40 [40] or XMC2 IO S10 [F9]	GND

(1) Numbers in [ ] correspond to the pin number of the connector at the other end of the signal (J24 or J26).

(2) For rear SATA and PCIe interfaces with standard P0, please refer to section 2.3.3 P0 Part Number Change and its Impact on Rear SATA and PCIe Interfaces

Table 51: Connector P0 Signals Definition

Signal	Dir.	Definition
ETH0 DA+/-	I/O	1000BASE-T Thin Pipe Bidirectional Data A of port ETH0.
ETH0 DB+/-	I/O	1000BASE-T Thin Pipe Bidirectional Data B of port ETH0.
ETH0 DC+/-	I/O	1000BASE-T Thin Pipe Bidirectional Data C of port ETH0.
ETH0 DD+/-	I/O	1000BASE-T Thin Pipe Bidirectional Data D of port ETH0.
ETH1 DA+/-	I/O	1000BASE-T Thin Pipe Bidirectional Data A of port ETH1.
ETH1 DB+/-	I/O	1000BASE-T Thin Pipe Bidirectional Data B of port ETH1.
ETH1 DC+/-	I/O	1000BASE-T Thin Pipe Bidirectional Data C of port ETH1.
ETH1 DD+/-	I/O	1000BASE-T Thin Pipe Bidirectional Data D of port ETH1.
GND	-	Logic Ground.
GPIOx	I/O	GPIOx, x=1,2,3.
NVMRO	I	Non-Volatile Memory Read Only signal. When asserted (logical 1), prevents any non-volatile memory from being updated. Active high signal with a 2.7K pull-down on board, 3V3 signalling, not 5V tolerant.
opt RPCIE RXx+/-	I	Receive differential pair of lane x of PCIe 4x link RPCIE (x=0,1,2,3). Link 1x always available. Link 4x is optional (refer to option "Rear IOs P0" in Table 4).
opt RPCIE TXx+/-	I	Transmit differential pair of lane x of PCIe 4x link RPCIE (x=0,1,2,3). Link 1x always available. Link 4x is optional (refer to option "Rear IOs P0" in Table 4).
PMC2 IO xx	I/O	PMC IO xx from PMC site PMC2 (connector J24).
opt RHDMI CLKx+/-	I/O	Differential clock of Rear HDMI port RHDMI. Optional (refer to option "Rear IOs P0" in Table 4).
opt RHDMI HPD	I	Hot Plug Detect of Rear HDMI port RHDMI. Optional (refer to option "Rear IOs P0" in Table 4).
opt RHDMI SCL	O	I2C clock of Rear HDMI port RHDMI. Optional (refer to option "Rear IOs P0" in Table 4).
opt RHDMI SDA	I/O	I2C data of Rear HDMI port RHDMI. Optional (refer to option "Rear IOs P0" in Table 4).
opt RHDMI TMDSx+/-	I/O	TMDS differential pair x of Rear HDMI port RHDMI (x=0,1,2). Optional (refer to option "Rear IOs P0" in Table 4).
RESET#	I	Board Reset Input Signal. Same action as the front reset push button.
V_BAT_EXT	I	3.0 V external Battery source for RTC
SATAx RX+/-	I	Receive differential pair of port SATAx (x=0,1).
SATAx TX+/-	O	Transmit differential pair of port SATAx (x=0,1).
USB0 D+/-	I/O	Differential pair of USB 2.0 port USB0.
USB3 D+/-	I/O	Differential pair of USB 2.0 port P0_USB3. This port is connected to Xeon D USB 2.0 port 3. It is multiplexed with the front USB 2.0 port FRONT_USB3. The multiplexor is controlled through CPLD.
USBx PWR	O	USB +5V power associated to USB 2.0 port USBx (x=0,1). Protected by current-limiting device; limit current at 25°C: minimum 0.75 A, typical 1 A, maximum 1.25 A.
XMC2 IO Syy	I/O	Single ended XMC IO Syy from XMC site XMC2 (connector J26).
XMC2 IO DPyy+/-	I/O	Differential XMC IO Dyy+/- from XMC site XMC2 (connector J26).

Figure 28: Routing of PMC IOs to P0

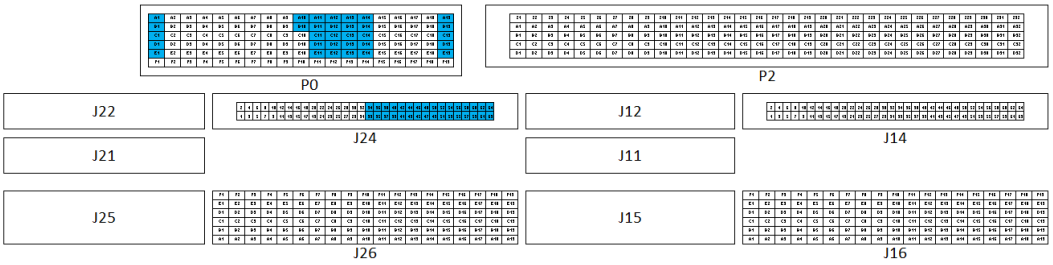


Figure 29: Routing of XMC IOs to P0

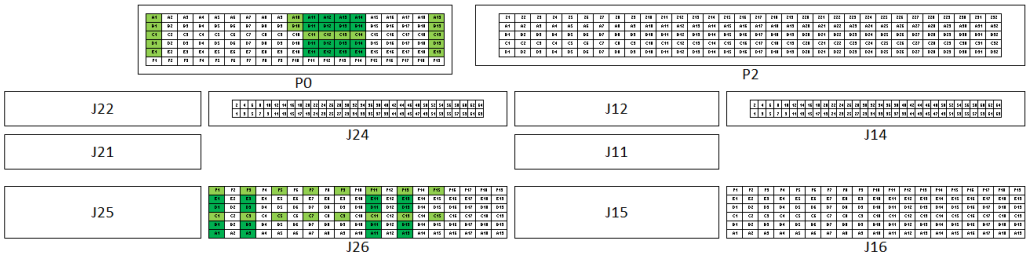
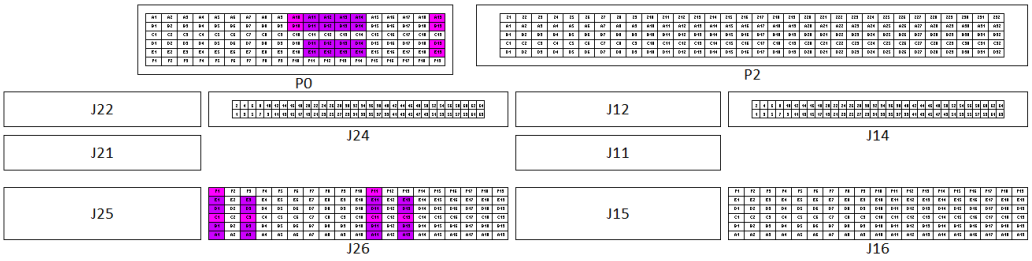


Figure 30: Routing of XMC IOs to P0 with XMC-GPU91 on Site XMC2



5.3.2. VME Connectors P1 & P2/Row B

Table 52: VME Connectors P1 & P2/Row B Pin Assignment

Pin	P1					P2
	Row Z	Row A	Row B	Row C	Row D	Row B
1	NC	D00	BBSY#	D08	+5 VDC	+5 VDC
2	GND	D01	BCLR#	D09	GND	GND
3	NC	D02	ACFAIL#	D10	NC	RETRY#
4	GND	D03	BG0IN#	D11	NC	A24
5	NC	D04	BG0OUT#	D12	NC	A25
6	GND	D05	BG1IN#	D13	NC	A26
7	NC	D06	BG1OUT#	D14	NC	A27
8	GND	D07	BG2IN#	D15	NC	A28
9	NC	GND	BG2OUT#	GND	GA5#	A29
10	GND	SYSCLK	BG3IN#	SYSFAIL#	GA0#	A30
11	NC	GND	BG3OUT#	BERR#	GA1#	A31
12	GND	DS1#	BR0#	SYSRESET#	+3.3 VDC	GND
13	NC	DS0#	BR1#	LWORD#	GA2#	+5 VDC
14	GND	WRITE#	BR2#	AM5	+3.3 VDC	D16
15	NC	GND	BR3#	A23	GA3#	D17
16	GND	DTACK#	AM0	A22	+3.3 VDC	D18
17	NC	GND	AM1	A21	GA4#	D19
18	GND	AS#	AM2	A20	+3.3 VDC	D20
19	NC	GND	AM3	A19	SMB_CLK	D21
20	GND	IACK#	GND	A18	+3.3 VDC	D22
21	NC	IACKIN#	IPMB_SCL	A17	SMB_DAT	D23
22	GND	IACKOUT#	IPMB_SDA	A16	+3.3 VDC	GND
23	NC	AM4	GND	A15	SMB_ALERT#	D24
24	GND	A07	IRQ7#	A14	+3.3 VDC	D25
25	NC	A06	IRQ6#	A13	NC	D26
26	GND	A05	IRQ5#	A12	+3.3 VDC	D27
27	NC	A04	IRQ4#	A11	NC	D28
28	GND	A03	IRQ3#	A10	+3.3 VDC	D29
29	NC	A02	IRQ2#	A09	NC	D30
30	GND	A01	IRQ1#	A08	+3.3 VDC	D31
31	NC	-12 VDC	+5VSTDBY	+12 VDC	GND	GND
32	GND	+5 VDC	+5 VDC	+5 VDC	+5 VDC	+5 VDC

Table 53: VME Connectors P1 & P2/Row B Signals Definition

Signal	Definition
A01 to A31	VME address bus as per VITA 1.
ACFAIL#	AC failure as per VITA 1.
AM0 to AM5	Address modifiers as per VITA 1.
AS*	Address Strobe as per VITA 1.
BBSY*	Bus Busy as per VITA 1.
BCLR*	Bus Clear as per VITA 1.
BERR*	Bus Error as per VITA 1.
BG0IN* to BG3IN*	Bus Grant In 0 to 3 as per VITA 1.
BG0OUT* to BG3OUT*	Bus Grant Out 0 to 3 as per VITA 1.
BR0* to BR3*	Bus Request In 0 to 3 as per VITA 1.
D00 to D31	Data bus as per VITA 1.
DS0*, DS1*	Data Strobes 0 and 1 as per VITA 1.
DTACK*	Data Transfer Acknowledge as per VITA 1.
GA0* to GA4* , GAP*	Geographical addressess and parity as per VITA 1.
GND	Logic Ground.
IACK*	Interrupt Acknowledge as per VITA 1.
IACKIN*	Interrupt Acknowledge In as per VITA 1.
IACKOUT*	Interrupt Acknowledge Out as per VITA 1.
IPMB_SCL	Intelligent Platform Management Bus - I2C clock.
IPMB_SDA	Intelligent Platform Management Bus - I2C data.
IRQ1* to IRQ7*	Interrupt Request (1 to 7) as per VITA 1.
LWORD*	Longword as per VITA 1.
SMB_ALERT*	System Management Bus Alert as per VITA 1.
SMB_SCL	System Management Bus serial clock.
SMB_SDA	System Management Bus serial data.
SYSCLK	System Clock as per VITA 1.
SYSFAIL*	System Fail as per VITA 1.
SYSRESET*	System Reset as per VITA 1.
WRITE*	Write as per VITA 1.
+3.3 VDC	+3.3 Volts DC power as per VITA 1.
+5 VDC	+5 Volts DC power as per VITA 1.
+5VSTDBY	+5 Volts DC Standby power as per VITA 1.
+12 VDC	+12 Volts DC power as per VITA 1. This power rail is not used on VM606x and directly routed to PMC1, PMC2, XMC1 and XMC2 sites. (1)
-12 VDC	-12 Volts DC power as per VITA 1. This power rail is not used on VM606x and directly routed to PMC1, PMC2, XMC1 and XMC2 sites.

(1) The main power rail of XMC1 or XMC2 may be connected to the +12 VDC power rail. Please contact Kontron.

5.3.3. Rear Connector P2 (except Row B)

Table 54: Connector P2 (except Row B) Pin Assignment

Pin	Row Z	Row A (1)	Row C (1)	Row D
1	PMC2 IO2	PMC1 IO2 [2] or XMC1 XMC IO DP5- [B5]	PMC1 IO1 [1] or XMC1 XMC IO DP5+ [A5]	PMC2 IO1
2	GND	PMC1 IO4 [4] or XMC1 XMC IO DP6- [E5]	PMC1 IO3 [3] or XMC1 XMC IO DP6+ [D5]	PMC2 IO3
3	PMC2 IO5	PMC1 IO6 [6] or XMC1 XMC IO S22 [F6]	PMC1 IO5 [5] or XMC1 XMC IO S21 [C6]	PMC2 IO4
4	GND	PMC1 IO8 [8] or XMC1 XMC IO DP7- [B7]	PMC1 IO7 [7] or XMC1 XMC IO DP7+ [A7]	PMC2 IO6
5	PMC2 IO8	PMC1 IO10 [10] or XMC1 XMC IO DP8- [E7]	PMC1 IO9 [9] or XMC1 XMC IO DP8+ [D7]	PMC2 IO7
6	GND	PMC1 IO12 [12] or XMC1 XMC IO DP9- [B9]	PMC1 IO11 [11] or XMC1 XMC IO DP9+ [A9]	PMC2 IO9
7	PMC2 IO11	PMC1 IO14 [14] or XMC1 XMC IO DP10- [E9]	PMC1 IO13 [13] or XMC1 XMC IO DP10+ [D9]	PMC2 IO10
8	GND	PMC1 IO16 [16] or XMC1 XMC IO DP15- [B15]	PMC1 IO15 [15] or XMC1 XMC IO DP15+ [A15]	PMC2 IO12
9	PMC2 IO14	PMC1 IO18 [18] or XMC1 XMC IO S19 [C19]	PMC1 IO17 [17] or XMC1 XMC IO S23 [C18]	PMC2 IO13
10	GND	PMC1 IO20 [20] or XMC1 XMC IO DP16- [E15]	PMC1 IO19 [19] or XMC1 XMC IO DP16+ [D15]	PMC2 IO15
11	PMC2 IO17	PMC1 IO22 [22] or XMC1 XMC IO DP17- [B17]	PMC1 IO21 [21] or XMC1 XMC IO DP17+ [A17]	PMC2 IO16
12	GND	PMC1 IO24 [24] or XMC1 XMC IO S18 [F17]	PMC1 IO23 [23] or XMC1 XMC IO S17 [C17]	PMC2 IO18
13	PMC2 IO20	PMC1 IO26 [26] or XMC1 XMC IO DP18- [E17]	PMC1 IO25 [25] or XMC1 XMC IO DP18+ [D17]	PMC2 IO19
14	GND	PMC1 IO28 [28] or XMC1 XMC IO DP19- [B19]	PMC1 IO27 [27] or XMC1 XMC IO DP19+ [A19]	PMC2 IO21
15	PMC2 IO23	PMC1 IO30 [30] or XMC1 XMC IO S20 [F19]	PMC1 IO29 [29] or XMC1 XMC IO S24 [F18]	PMC2 IO22
16	GND	PMC1 IO32 [32] or XMC1 XMC IO DP20- [DE19]	PMC1 IO31 [31] or XMC1 XMC IO DP20+ [D19]	PMC2 IO24
17	PMC2 IO26	PMC1 IO34 [34] or XMC1 XMC IO S4 [F3]	PMC1 IO33 [33] or XMC1 XMC IO S2 [F1]	PMC2 IO25
18	GND	PMC1 IO36 [36] or XMC1 XMC IO S6 [F6]	PMC1 IO35 [35] or XMC1 XMC IO S5 [C5]	PMC2 IO27
19	PMC2 IO29	PMC1 IO38 [38] or XMC1 XMC IO S8 [F7]	PMC1 IO37 [37] or XMC1 XMC IO S7 [C7]	PMC2 IO28
20	GND	PMC1 IO40 [40] or XMC1 XMC IO S10 [F9]	PMC1 IO39 [39] or XMC1 XMC IO S9 [C9]	PMC2 IO30
21	PMC2 IO32	PMC1 IO42 [42] or XMC1 XMC IO S14 [F13]	PMC1 IO41 [41] or XMC1 XMC IO S12 [F11]	PMC2 IO31
22	GND	PMC1 IO44 [44]	PMC1 IO43 [43]	COM1 TXD / COM1 TXD-

Pin	Row Z	Row A (1)	Row C (1)	Row D
		or XMC1 XMC IO S16 [F15]	or XMC1 XMC IO S15 [C15]	
23	COM2 TXD / COM2 TXD-	PMC1 IO46 [46] or XMC1 XMC IO S1 [C1]	PMC1 IO45 [45] or XMC1 XMC IO S3 [C3]	COM1 RXD / COM1 RXD-
24	GND	PMC1 IO48 [48] or XMC1 XMC IO DP11+ [A11]	PMC1 IO47 [47] or XMC1 XMC IO DP14+ [D13]	COM1 TXD+
25	COM2 RXD / COM2 RXD-	PMC1 IO50 [50] or XMC1 XMC IO DP11- [B11]	PMC1 IO49 [49] or XMC1 XMC IO DP14- [E13]	COM1 RXD+
26	GND	PMC1 IO52 [52] or XMC1 XMC IO DP12+ [D11]	PMC1 IO51 [51] or XMC1 XMC IO DP13+ [A13]	NC
27	COM2 TXD+	PMC1 IO54 [54] or XMC1 XMC IO DP12- [E11]	PMC1 IO53 [53] or XMC1 XMC IO DP13- [B13]	NC
28	GND	PMC1 IO56 [56] or XMC1 XMC IO S11 [C11]	PMC1 IO55 [55] or XMC1 XMC IO S13 [C13]	NC
29	COM2 RXD+	PMC1 IO58 [58] or XMC1 XMC IO DP1+ [A1]	PMC1 IO57 [57] or XMC1 XMC IO DP4+ [D3]	GPIO5
30	GND	PMC1 IO60 [60] or XMC1 XMC IO DP1- [B1]	PMC1 IO59 [59] or XMC1 XMC IO DP4- [E3]	GPIO4
31	GPIO6	PMC1 IO62 [62] or XMC1 XMC IO DP2+ [D1]	PMC1 IO61 [61] or XMC1 XMC IO DP3+ [A3]	GND
32	GND	PMC1 IO64 [64] or XMC1 XMC IO DP2- [E1] opt GPIO7	PMC1 IO63 [63] or XMC1 XMC IO DP3- [B3] opt GPIO8	+5 VDC

(1) Numbers in [ ] correspond to the pin number of the connector at the other end of the signal (J14 or J16).

Table 55: Connector P2 (except Row B) Signal Definition

Signal	Definition
PMC1 IOxx	PMC IO xx from site PMC1.
PMC2 IOxx	PMC IO xx from site PMC2.
COMx TXD / COMx TXD-	EIA-232: Transmit Data of serial port COMx, x=1,2. EIA-485: Transmit Data Minus of serial port COMx, x=1,2.
COMx TXD+	EIA-485: Transmit Data Plus of serial port COMx, x=1,2.
COMx RXD / COMx RXD-	EIA-232: Receive Data of serial port COMx, x=1,2. EIA-485: Receive Data Minus of serial port COMs, x=1,2.
COMx RXD+	EIA-485: Receive Data Plus of serial port COMx, x=1,2.
opt GPIOx	GPIOx handled by CPLD. Optional (refer to option "Rear IOs P2" in Table 4).
XMC1 IOxx	XMC IO xx from site PMC1.
+5 VDC	+5 Volts DC power as per VITA 1.

Figure 31: Routing of PMC IOs to P2

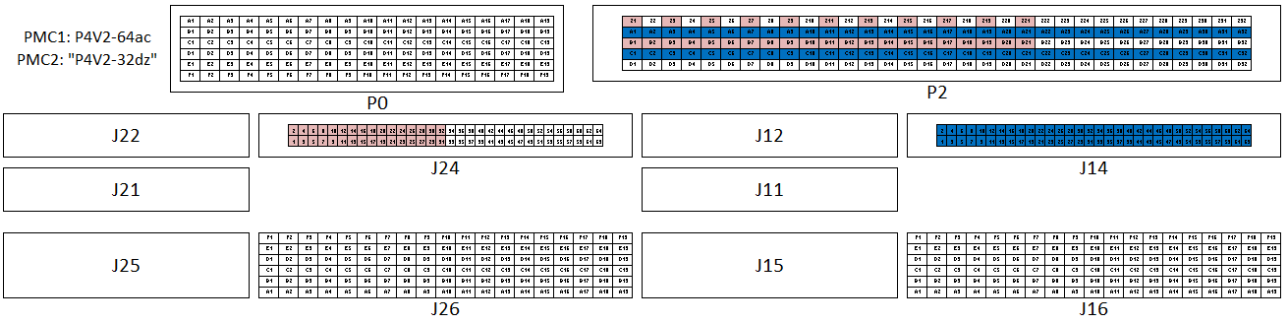
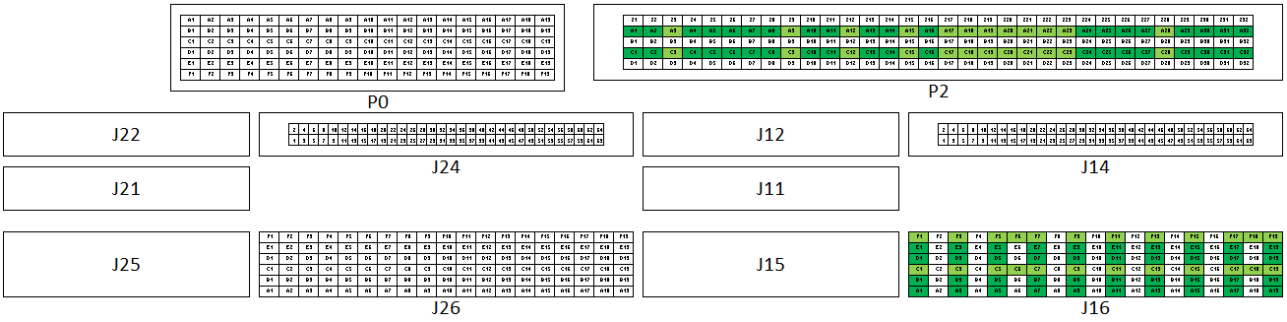


Figure 32: Routing of XMC IOs to P2



5.4. LEDs

Status LEDs on front panel

There are five bicolor LEDs (Red/Green/Orange) on the front panel numbered L1 to L5 from left to right.

Figure 33: Front Panel Status LEDs

LED states

There are eight different states for each LED.

Table 56: LED states

Symbol	State Description
○	LED OFF
●	Steady Red
●	Steady Green
●	Steady Orange (both Red and Green at the same time)
B	Blinking Red
B	Blinking Green
B	Blinking Orange
B	Blinking. The color is not relevant. Color and blinking states are totally independant.

LEDs Meaning

LEDs Meaning in Normal Operation

Table 57: LEDs meaning

LED 1	LED 2	LED 3	LED 4	LED 5	Meaning
●	-	-	-	-	Permanent system error: the internal power supplies are turned off. In this state, LED2 to LED5 do not carry the meaning described in this table but an error code detailed later in this section.
● B					Steady: At least one of the two 1GbE links ETH0, ETH1 is up in 1GbE speed. Blinking: activity on this interface.
● B					Steady: At least one of the two 1GbE links ETH0, ETH1 is up but not in 1GbE speed. Blinking: activity on this interface.
○					The two Ethernet interfaces ETH0 ETH1 are down (no link).
	●				Reserved
	●				1GbE ETH0 routed to front.
	●				1GbE ETH0 routed to backplane.
		●			Internal power supplies are on (all PowerGood signals asserted) and reset signal is asserted (board is in reset).
		●			Internal power supplies are on (all PowerGood signals asserted) and reset signal is de-asserted (normal operation).
		●			Internal power supplies are on (all PowerGood signals asserted) but the SoC output PROCPWRGD_PCH is not activated, indicating that the SoC internal power is not valid.
		B B			Fast blinking Red: Activity on VME-IPMBus/VME-SMBus (LED blinking) and Platform Reset asserted by CPLD (LED is red). Fast blinking Green: Activity on VME-IPMBus/VME-SMBus (LED blinking) and Platform Reset de-asserted by CPLD (LED is green). Slow blinking Green (1Hz, 50% duty cycle): internal power supplies are OFF (board in standby)
			●		Board not in factory test mode and no CPLD watchdog expired. (Normal operation)
			●		Board in factory test mode
			●		CPLD Watchdog expired
			B		Blinking (color not relevant and keeps its steady state meaning): M.2 activity on socket S1.
				●	Processor hot event (PROCHOT) (1). Supersedes 1GbE routing information coded in green or orange.
				●	1GbE link ETH0 routed to front.
				●	1GbE link ETH0 routed to VME backplane
				B	Blinking (color not relevant and keeps its steady state meaning): M.2 activity on socket S3.

(1) LED is lit red only if PROCHOT signal is activated by SoC to indicate over temperature condition, it is not lit up red if PROCHOT has been asserted by CPLD to force SoC in low frequency operation.

LEDs Error Codes

Table 58: Error codes displayed by LEDs

LED1	LED2	LED3	LED4	LED5	Code	Cause
●	○	○	○	○	LEDERR 00	VME +5V VDC not present
●	○	○	○	●	LEDERR 01	Internal Power Supply Failure
●	○	○	●	○	LEDERR 02	Internal Power Supply Failure
●	○	○	●	●	LEDERR 03	Internal Power Supply Failure
●	●	●	○	○	LEDERR 0C	Xeon SoC hangs in Reset state (PLTRST#)
●	●	●	○	●	LEDERR 0D	Xeon SoC hangs due to PowerGood timeout (PROCPWRGD_PCH)
●	●	●	●	○	LEDERR 0E	Xeon SoC hangs due to Wake Up timeout (SLP_S4#)
●	B	B	B	B	LEDERR BBO	Internal Power Supply Failure
●	○	○	○	●	LEDERR 11	VME +5VDC or +3.3VDC undervoltage
●	○	○	●	●	LEDERR 11.5	VME +5VDC or +3.3VDC undervoltage and VME +5VDC or +3.3VDC overvoltage
●	○	○	●	○	LEDERR 12	VME +5VDC or +3.3VDC overvoltage
●	○	○	●	●	LEDERR 13	Internal Power Supply Failure
●	○	●	○	○	LEDERR 14	Internal Power Supply Failure
●	○	●	○	●	LEDERR 15	Internal Power Supply Failure
●	○	●	●	○	LEDERR 16	Internal Power Supply Failure
●	○	●	●	●	LEDERR 17	Internal Power Supply Failure
●	●	○	○	○	LEDERR 18	Internal Power Supply Failure
●	●	○	○	●	LEDERR 19	Internal Power Supply Failure
●	●	○	●	○	LEDERR 1A	Internal Power Supply Failure
●	●	○	●	●	LEDERR 1B	Internal Power Supply Failure
●	●	●	○	○	LEDERR 1C	Internal Power Supply Failure
●	●	●	○	●	LEDERR 1D	Internal Power Supply Failure
●	●	●	●	○	LEDERR 1E	Internal Power Supply Failure
●	●	●	●	●	LEDERR 1F	Internal Power Supply Failure
B	B	-	-	-	LEDERR BBR	Error during Power down sequence. L3, L4 and L5 code the power_down sequence phases

- Critical Errors

Table 59: Critical Errors Encoding

LED 1	LED 2	LED 3	LED 4	LED 5	Critical Errors	Cause
B	●	●	●	●	LEDERR C1	Xeon Critical Over-temperature Condition
●	B	●	●	●	LEDERR C2	Temperature Alert from internal SoC VCCIN rail
●	●	B	●	●	LEDERR C3	Temperature Alert from internal 1.05V rail
●	●	●	B	●	LEDERR C4	Xeon Catastrophic Error (CATERR_N)
●	●	●	●	B	LEDERR C5	Critical Temperature Alert from Nuvoton NCT7802

6/ Electrical Specifications

6.1. VME Input Power Rails

VME Input Power Rails

The VM606x is powered by the +5 VDC and +3.3 VDC VME power rails as defined by VITA 1 and VITA 1.1 standards.
The manufacturing option "Power Supply" may be set to 5 for 5V-only option. Then the +3.3 VDC rail is no longer needed.
The +12 VDC and -12 VDC power rails are not used internally by the VM606x. They are directly routed to PMC and XMC sites.
Note: the +12 VDC voltage may be used as the XMC1 or XMC2 main power (VPWR).

By specific equipment, the +12 VDC voltage may be used as the XMC1 or XMC2 main power (VPWR). Please contact Kontron for more information.

Power Rails Specification

The VM606x is designed to operated according to the power supplies specifications summarized in Table 60. The +5VSTDBY rail is addressed in section 6.2.

Table 60: VME Input Power Rails Specification

Input Rail	Voltage				Ripple / Noise		Power-up		Power-down	
	Min	Nominal	Max	Source	Value	Source	Rise time value	Source	Minimum OFF duration (1)	Source
+5 VDC	4.875 V	5.0 V	5.25 V	VITA 1	50 mV peak-to-peak below 10 MHz	VITA 1	Monotonic rise. Rise Time 10/90: 1 ms to 25 ms.	Kontron	No undershoot below 0V. OFF duration: 1 sec min	Kontron
+3.3 VDC	3.25 V	3.3 V	3.45 V	VITA 1.1	Noise and ripple below 20 Mhz included.	VITA 1.1	Monotonic rise. Rise Time 10/90: 1 ms to 25 ms.	Kontron	No undershoot below 0V. OFF duration: 1 sec min	Kontron
+12 VDC	11.64 V	12.0 V	12.6 V	VITA 1	50 mV peak-to-peak below 10 MHz	VITA 1	Monotonic rise. Rise Time 10/90: 1 ms to 25 ms.	Kontron	No undershoot below 0V. OFF duration: 1 sec min	Kontron
-12 VDC	-12.6 V	-12.0 V	-11.64 V	VITA 1	50 mV peak-to-peak below 10 MHz	VITA 1	Monotonic rise. Rise Time 10/90: 1 ms to 25 ms.	Kontron	No undershoot below 0V. OFF duration: 1 sec min	Kontron

(1) The minimum OFF duration is the duration a power rail should remain in the OFF state before being powered ON again.

VME Input Power Rails Monitoring

The voltage sensor NCT7802Y by Nuvoton is programmed by BIOS to monitor +5V and +3.3V rails and asserts the signal PLD_PECI_ALERT# whenever one of these input voltages gets out of the safe operating range. This alert is routed to a maskable interrupt in the CPLD.

A second voltage sensor - LTC2913 by Linear Technology - also monitors the +5V and +3.3V rails. The thresholds are set by hardware and correspond to critical operating values. Under voltage and over voltage conditions are reported to the CPLD which will in turn shut down all VM606x internal power supplies. There is no software mechanism for masking these alerts.

Table 61: VME Input Power Rails Monitoring

Input Rail	HW Threshold LTC2913			SW Alert NCT7802			VITA Specification			SW Alert NCT7802			HW Threshold LTC2913		
	Min	Nom.	Max	Min	Nom.	Max	Min	Nom.	Max	Min	Nom.	Max	Min	Nom.	Max
+5 VDC	4.41V	4.49V	4.58V	4.67V	4.68V	4.69V	4.87V	5.00V	5.25V	5.30V	5.31V	5.32V	5.39V	5.49V	5.59V
+3.3 VDC	3.03V	3.09V	3.14V	3.17V	3.18V	3.19V	3.25V	3.30V	3.45V	3.50V	3.51V	3.52V	3.57V	3.61V	3.67V

6.2. Input Standby Rail +5VSTDBY

- VME +5VSTDBY and the internal standby power rails

The VM606x implements an ideal diode which forwards either +5VSTDBY or +5 VDC to the internal standby power rail V_5V0SB. This power rail generates in turn the V_3V3SB. The components powered by these standby power rails are the CPLD, VME-IPMBus & VME-SMBus buffers, voltage and temperature sensors, the VPD and OS EEPROMs, the FRAM and the external RTC RV-8564. If neither +5VSTDBY or +5 VDC, only the RTC will be powered through the onboard 3.0V battery.

- +5VSTDBY Specification

Table 62: VME +5V STDBY Input Power Rail Specification

Input Rail	Voltage				Ripple / Noise		Current	
	Min	Nom.	Max	Source	Value	Source	Minimum current	Source
+5V STDBY	4.875 V	5.0 V	5.25 V	VITA 1	50 mV peak-to-peak below 10 MHz	VITA 1	0.5 A	Kontron

- +5VSTDBY and V_3V3SB Monitoring

The +5VSTDBY rail is not monitored but its 3.3V counterpart V_3V3SB is monitored by the Reset controller TPS3808 which will reset the board if V_3V3SB falls below 2.92 V.

6.3. Input Battery Rail V_BAT_EXT

- A battery voltage rail on rear P0

If V_BAT_EXT is present on P0, it will take over onboard battery and P1 +5VSTDBY to power the RV-8564 RTC when these supplies are not available. Refer to detailed RTC description in 4.1.1.

- V_BAT_EXT Specification

Voltage: 3.0 V typical, 2.55 V minimum, 3.5 V maximum.

6.4. Input Power Rails Protection

The input power rails are protected on the VM606x by fuse as described in Table 63.

To prevent safety hazards, the chassis power supply must never exceed the Voltage Rating and Interrupt Rating of the fuse.

Table 63: Input Powers Protection

Power rail	Location	Voltage	Protection	Rated Current	Trip current	Typical melt I^2t or hold current	Voltage rating	Interrupting rating	Manufacturer / PN
+5 VDC	P1, P2	+5.0 V	Non resettable fuse	20 A	-	48.6 A²s	24 V	150 A	EATON / 3216FF20-R
+3.3 VDC	P1	+3.3 V	Non resettable fuse	20 A	-	48.6 A²s	24 V	150 A	EATON / 3216FF20-R
+5V STDBY	P1	+5.0 V	Resettable fuse	0.5 A	0.75 A min @60°C 1.1 A typ @25°C 1.24 A max @0°C	0.35 A min @60°C 0.50 A typ @25°C 0.61 A max @0°C	13.2 V	35 A	TE Connectivity / NANOSMDC050F/13.2

6.5. Output Power Supplies Protection

On the VM606x, all the output power supplies provided on connectors are protected by fuse or current-limiting devices as described in Table 64.

Table 64: Output Powers Protection

Port	Function	Location	Signal	Voltage	Protection	Hold or Rated Current	Typical Melt I^2t or Trip current	Characteristics
USBSS	USB 3.0	Front	V_VBUS	+5 V	Current limited power switch	1 A	0.908 A min 0.989 A typ 1.081 A max	Reverse voltage protection Thermal shutdown: 135°C Response time: 2 µs FAULT reported to SoC
HDMI	HDMI	Front	+5 V	+5 V	Current limited power switch		0.100 A min 0.116 A typ 0.147 A max	Reverse current blocking
USB0 USB1	USB 2.0	Rear P0	USB0 PWR USB1 PWR	+5 V	Current limited power switch	1 A	0.908 A min 0.989 A typ 1.081 A max	Reverse voltage protection Thermal shutdown: 135°C Response time: 2 µs FAULT reported to SoC
PMC1, PMC2	PMC, XMC	On board J11, J21	V (I/O)	+3.3 V	Non resettable fuse	4.5 A	0.405 A^2S	Time to trip: 1 s
PMC1, PMC2, XMC1, XMC2	PMC, XMC	On board J11, J15, J21, J25	+5V	+5 V	Non resettable fuse	4.5 A	0.405 A^2S	Time to trip: 1 s
PMC1, PMC2, XMC1, XMC2	PMC, XMC	On board J12, J15, J22, J25	+3.3V	+3.3 V	Non resettable fuse	4.5 A	0.405 A^2S	Time to trip: 1 s
M.2 socket S1 MiniPCIe	M.2 socket	On board S1	3.3V	+3.3 V	Current protection inside voltage regulator		3.6 A min 4.2 A typ 4.9 A max	
M.2 socket S3	M.2 & MiniPCIe	On board S2 & S3	3.3V	+3.3 V	Current protection inside voltage		3.6 A min	One protection for the two

Port	Function	Location	Signal	Voltage	Protection	Hold or Rated Current	Typical Melt I^2t or Trip current	Characteristics
MiniPCIe socket S2	socket				regulator		4.2 A typ 4.9 A max	sockets S2 & S3.
MiniPCIe socket S2	M.2 & MiniPCIe socket	On board S2 & S3	+1.5V	+1.5 V	Current protection inside voltage regulator		5 A typ	

6.6. GPIOs

GPIOs Electrical Characteristics

The CPLD features LVCMOS33 cells (0 - 3.3 V), with a drive strength of 8 mA (sink or source), a clamp diode which is not 5 V tolerant and an hysteresis of 250 mV. The CPLD does not implement any internal pull-up or pull-down. A 22-Ω series resistor connects each GPIOs from P0 or P2 to the CPLD.

NOTICE

GPIOs are not 5 V tolerant. Maximum voltage on GPIOs is 3.6 V. Absolute maximum voltage is 3.75 V and is not suitable for continuous operation. Appropriate voltage reduction (through resistor divider for instance) must be made to avoid permanent damage to the board.

GPIOs Pull-ups

On the VM606x board, all GPIOs have a pull-up of 47 kΩ to internal standby 3.3V rail V_3V3SB.

7/ Power and Thermal Management

7.1. Intel® Turbo Boost Technology 2.0

Intel® Turbo Boost Technology automatically allows processor cores to run faster than the base operating frequency if it is operating below power, current, and temperature specification limits.

Dynamically increasing performance: Turbo Boost Technology is activated when the Operating System (OS) requests the highest processor performance state (P0).

The maximum frequency of Turbo Boost is dependent on the number of active cores. The amount of time the processor spends in the Intel® Turbo Boost state depends on the workload and operating environment.

Any of the following can set the upper limit of Turbo Boost on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency will dynamically increase until the upper limit of frequency is reached. Turbo Boost has multiple algorithms operating in parallel to manage current, power, and temperature to maximize performance and energy efficiency

Intel® Turbo Boost Technology 2.0 allows the processor to operate at a power level that is higher than its rated upper power limit (TDP) for short durations to maximize performance.

Learn more about Turbo Boost Technology: http://www.intel.com/technology/turboboost/

- Turbo Boost is handled by the BIOS through the Advanced Power Management Configuration menu.

Refer to the AMI BIOS documentation for VM606x - User Reference Manual, section “IntelRCSetup Menu”.

7.2. Xeon® D Power Consumption

The Xeon® D core frequency and the dissipated power at package level are closely related. They can be measured using the following tools:

- Intel® Performance Tuning Utility tool (PTU) for Xeon-D processors. The core load may be set between 0 and 100%. This is a major tool for characterizing the thermal behavior of a board in a system. In addition, PTU indicates the power dissipated, the temperature and frequency of each core. For PTU tool availability, contact Intel.

- Turbostat, an open-source linux tool which provides monitoring of the temperature, the frequency and the load of each core. Unlike PTU, Turbostat does not generate any core activity and power dissipation must be defined and controlled through user's programs or applications.

7.3. Power Consumption Specification

Worst Case VM606x Power Consumption

Table 65 gives the worst case continuous current values in three different configurations.

Table 65: VM606x Maximum Current

VM606x	Max Continuous Current	Max Continuous Power	Test Conditions
VM6062-SA28-05000100	8 A / +5VDC +3.3VDC: NA	40 W / +5VDC +3.3VDC: NA	5V-only configuration, no PMC/XMC, PTU 100%.
VM6062-SA28-05000100	10 A / +5VDC +3.3VDC: NA	50 W / +5VDC +3.3VDC: NA	5V-only configuration, full functionnal complex test (FFT, DDR4, IOs), Ethernet PMC and Ethernet XMC installed and exercised.
VM6062-SA28-00000100	9.4 A / +5VDC 1 A / +3.3VDC	46.7 W / +5VDC 3.3 W / +3.3VDC	Full functionnal complex test (FFT, DDR4, IOs), Ethernet PMC and Ethernet XMC installed and exercised.

VM606x Power Consumption Examples in Two Typical Configurations

Table 66 shows the power consumptions in two actual and typical configurations: maximum power consumption with Turbo Boost mode off and low power consumption with minimum frequency and activity.

Table 66: VM606x Power Consumption Examples

VM606x	Power Mode	Total Current	Total Power (1)	Xeon® SoC Power (2)	Rest of the board (3) (4)	Test conditions
VM606x Xeon® D @2.2GHz	Turbo Off, Max Processor power, TDP 25W@2.2Ghz	7 A / +5VDC 0.7 A / +3.3VDC	37 W	25 W	12 W	Full Functionnal Tests (all functions except VME and rear IOs). No Turbo. Fixed Frequency 2.2 GHz.100% load. No throttle.
	Linux idle Linux «on demand» mode Processor frequency 2.2 GHz	4.6 A / +5VDC	23 W	Not measured	Not measured	Linux idle. 5V-only configuration.

(1) The value of the total power dissipated by VM606x is obtained through VME input rails current measurements.

(2) The Xeon® SoC power dissipation is measured through PTU tool. It is the full package power dissipation, including cores and uncore modules.

(3) The "Rest of the board" dissipation is the difference between Total Power and Xeon® SoC Power.

(4) The configuration does not include any PMC or XMC.

Available Current and Power for PMC and XMC mezzanines

According to IEEE 1386, the PMC maximum power consumption is set to 7.5W. On VM606x, higher power consumptions may be possible depending on thermal configuration and performance. The 7.5W budget may be distributed over any of the available power rails as long as the overall power consumption stays within budget.

Regarding the XMC sites, VITA 42 does not specify a maximum power consumption other than the connector maximum current per pin which leads to a theoretical 100 W. Practically, the XMC power consumption is limited by the VM606x power rails capability and the thermal performance. Each XMC may be powered either from the +5V rail (default) or from the +12V rail (on-demand option).

Table 67: PMC and XMC Mezzanines Maximum Current and Power

VM606x	PMC1 or PMC2		XMC1 or XMC2	
	Standard Limit Current	VM606x Design Limit Current	VM606x Design Limit Current VPWR = +5V (default)	VM606x Design Limit Current VPWR = +12V (on demand)
VM6062-SA28-00200100	1.5 A / +5V 2.3 A / +3.3V 0.5 A / +12V 0.4 A / -12V	3 A / +5V 4.6 A / +3.3V 1 A / +12V 1 A / -12V	3 A / VPWR +5V 4.6 A / +3.3V 1 A / +12V 1 A / -12V	2 A / VPWR +12V 4.6 A / +3.3V 1 A / +12V 1 A / -12V

Available Current and Power for M.2 modules and the MiniPCIe/mSATA card

In the M.2 Electromechanical Specification a maximum current of 0.5A per pin is specified. The maximum power consumption is therefore 2.5 A on five 3.3 V pins (8.25 W).

The PCI Express Mini Card standard defines a maximum normal (continuous) power of 1.1 A for +3.3Vaux and 375 mA for +1.5V.

As for PMC/XMC power dissipation, it is likely that the limiting factor may actually be the thermal performance of the board and system configuration.

Table 68: M.2 Modules and MiniPCIe/mSATA Maximum Current and Power

VM606x	M.2 socket S1		MiniPCIe Socket S2 and M.2 Socket S3		
	Standard Max Current	VM606x Max Current	Standard Max Current MiniPCIe Socket S2	Standard Max Current M.2 Socket S3	VM606x Max Current
VM6062-RA2G-10200100	2.5 A / +3.3V	3.6 A / +3.3V	1.1 A / +3.3V 0.375 A / +1.5V	2.5 A / +3.3V	3.6 A / +3V (S2 & S3) 5 A / +1.5V (S2)

7.4. Temperature Monitoring

7.4.1. Processor Temperature

The Xeon® D SoC features an integrated heat spreader (IHS) which interfaces the die with the board cooling device.

To allow optimal operation and long-term reliability, the Xeon® D must remain within the temperature specifications as defined by Intel®.

For the dual and quad core processors of the Intel® Xeon® Processor D-1500 Product Family - which are primarily selected for the VX606x SBC - the internal temperature measured by the Digital Thermal Sensor (DTS) should not exceed 104°C. Since some margin is necessary to account for silicon disparity, DTS accuracy and test environment variations Kontron advises not to exceed 100°C.

System thermal design must ensure that the Xeon D internal temperature measured by the SoC DTS does not exceed 100°C.

Further information may be found in "Intel® Xeon® Processor D-1500 Product Family External Design Specifications (EDS), Volume One: Core and Uncore Architecture" where the following supported features are described: Digital Thermal Sensor (DTS), Intel Adaptive Thermal Monitor, THERMTRIP and PROCHOT_N support, On-Demand Mode, Memory Thermal Throttling.

7.4.2. Board Temperature

Four temperature sensors

The VM606x implements the temperature sensor NCT7802Y by Nuvoton and three LM73 sensors by Texas Instruments. They are managed through the CPLD and its I2C bus CPLD-I2CLOC @99.2kHz. They can be accessed via the EFI shell command "ksensors" or the Linux command "sensors".

Figure 34: LM73 Sensors U2605 @0x94 (8-bit) @0x4A (7-bit) and U2606 @0x90 (8-bit) @0x48 (7-bit) on Top Side

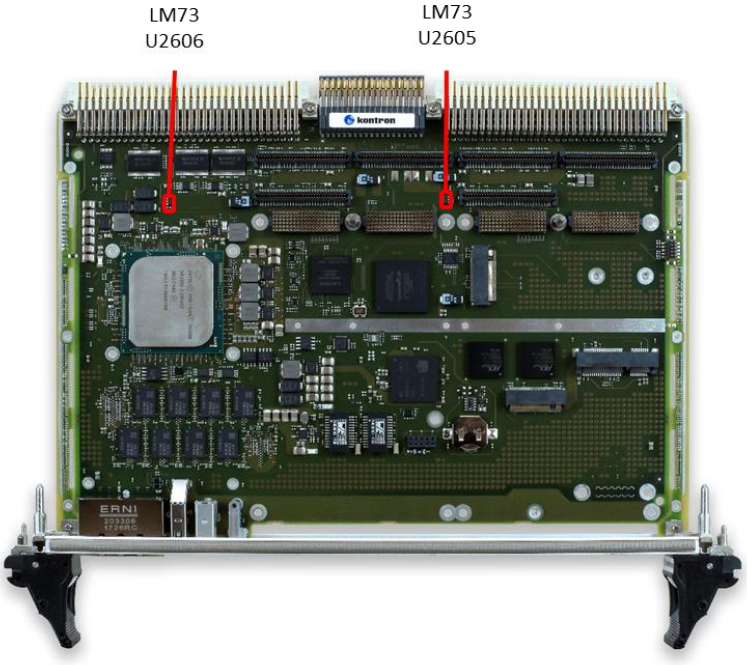
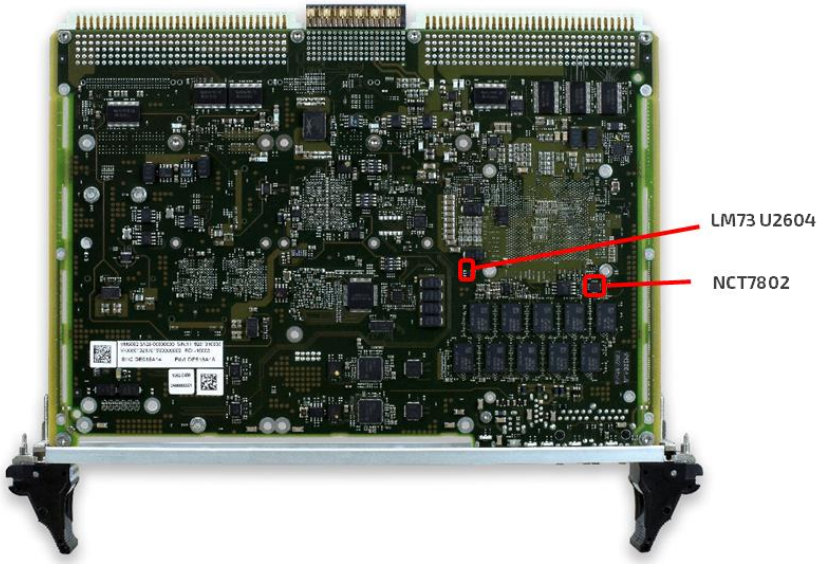


Figure 35: Sensors LM73 U2604 @0x92 (8-bit) @0x49 (7-bit) and NCT7802Y @0x50 (8-bit) @0x28 (7-bit) on Bottom Side



The NCT7802Y sensor

The NCT7802Y has two alarm outputs connected to the CPLD:

- ALERT# (NCT7802): logged in CPLD reg @0x5B to generate a maskable interrupt. The high threshold is set by BIOS to +85°C for Standard Air-cooled Class (SA) and to +90°C for all other classes (WA, RA, RC). The low threshold is set by BIOS to -45°C for all classes.
- T_CRIT#: logged in CPLD reg @0x74, leads to fatal error with all internal power supplies being switched off and the error status being displayed on the front panel LEDs. The T_CRIT# threshold is set to BIOS to +95°C for Standard Air-cooled Class (SA) and to +100°C for all other classes (WA, RA, RC).

The characteristics of the temperature sensor inside the NCT7802Y are:

- Accuracy (25~70°C): +/- 2°C typ.
- Resolution: 1 °C.

The LM73 sensors

The open-drain outputs ALERT# of each LM73 sensor are connected together and routed to the CPLD. ALERT# is activated when the temperature exceeds a programmed limit. The CPLD then generates an interrupt to the SoC.

- TEMP_ALERT# (LM73): logged in CPLD reg @0x5B. The high threshold is set by BIOS to +95°C for all LM73 sensors and all classes (SA, WA, RA, RC) except for LM73 U2604 on bottom for which the high threshold is set to +85°C in SA Class. The low threshold is set by BIOS to -45°C for all LM73 sensors and all classes.

The characteristics of the LM73 sensors are:

- Accuracy (-10~80°C): +/- 1°C maximum.
- Resolution: 0.25°C (default, 11 bits) to 0.03125°C (14 bits).

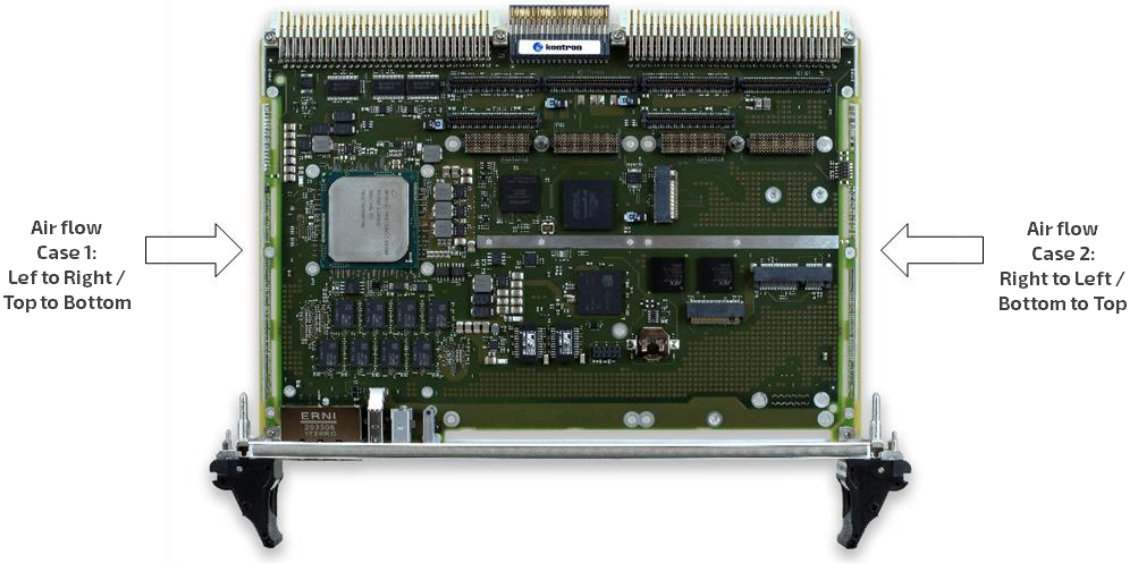
On Linux, the sensors thresholds may be modified via sensors.conf file. Refer to SD.DT.G53.

7.5. Air Flow Specification

7.5.1. Air Flow Direction

The VME standard does not define a specific air flow direction. Air may flow from right to left (bottom to top) or left to right (top to bottom) as shown on Figure 36. The VM606x has been mostly tested and characterized in the former configuration which is the least favorable since the PMCs/XMCs tend to prevent air from flowing smoothly to the SoC heatsink.

Figure 36: Two Possible Air Flow Directions



7.5.2. Power Dissipation vs Air Flow: Thermal Safe Operating Areas

Recommended Air Flow

Table 69: Recommended Thermal Operating Points for Air-Cooled VM606x

Class	VM606x Order Codes	Incoming Air Temp.	PMC/XMC	Board Power	Air Flow (1)	Configuration & Test conditions
SA	VM6062-SA28-00200100 VM6062-SA28-00000100	55°C	None	33 W	8 CFM	- Xeon D-1508, TDP 25W, No Turbo. Fixed Frequency 2.2 GHz. 80 % load. - Full Functionnal Tests (all functions except VME and rear IOs).
			1x 7.5 W	41 W	10 CFM	
			2x 7.5 W	48 W	13 CFM	
SA	VM6064-SA4G-00300100	55°C	None	43 W	11 CFM	- Xeon D-1527, TDP 35W, No Turbo. Fixed Frequency 2.2 GHz. 80% load. - Full Functionnal Tests (all functions except VME and rear IOs).
			1x 7.5 W	51 W	13 CFM	
			2x 7.5 W	58 W	16 CFM	
RA	VM6062-RA2G-10200100	70°C	None	33 W	15 CFM	- Xeon D-1508, TDP 25W, No Turbo. Fixed Frequency 2.2 GHz. 80% load. - Full Functionnal Tests (all functions except VME and rear IOs).
			1x 7.5 W	41 W	18 CFM	
			2x 7.5 W	48 W	22 CFM	

(1) These recommended air flow figures are based on thermal characterization performed in laminar flow bench according to Kontron procedure. Air flow direction is from right to left.

Thermal Operating Limit Curves and Thermal Safe Operating Areas

The thermal characterization of the VM606x in air-cooled configurations is based on the measurement and normalization of maximum thermal operating limits. These limits are used to define the Thermal Operating Limit Curves and the related Thermal Safe Operating Areas (ThSOA) for the VM606x at 55°C (SA Class, Figures 37) and 70°C (RA Class, Figure 38).

To build the curves, the power dissipation and air flow were varied in the following manner:

- The overall power dissipation was varied with the processor activity, the presence of add-on PMC or XMC, their number and power grade.
- The Xeon® junction temperature (Tj) was set to a fixed value of 100°C ie 4°C below the specified maximum of 104°C. This margin was necessary to account for silicon disparity, DTS accuracy and test setup variation.
- The air flow was set to the necessary value to stabilize Tj at 100°C despite the presence and number of PMC or XMC mezzanines.
- Test conditions: The Xeon® load was 100% without throttling, no turbo mode, fixed frequency 2.2 GHz. Full Functionnal Tests (all functions except VME and rear IOs). No Turbo. Fixed Frequency 2.2 GHz. 100% load. No throttle.

The Thermal Safe Operating Areas (ThSOA) are the regions located below these worst-case curves.

Adjusting the airflow and power dissipation to stay within the ThSOA will ensure that the Xeon® never enters throttling mode and therefore that the performance and predictability of the application will not be impacted. Nevertheless, to ensure long-term reliability it is strongly advised to operate as far as possible from the defined limits and to set the airflow at a significantly higher rate than strictly necessary. A 30% to 50% margin would be a good starting point.

The difference between a real system and the equipment used for this characterization is also to be taken into account: in the test setup, pressure losses are reduced to their minimum and the air flow is as laminar as possible because of the length of the pipes installed before and after the DUT. These conditions cannot be met in real systems and an increased air flow must therefore compensate for this difference.

Figure 37: Overall Board Power Dissipation vs. Air Flow @55°C - Thermal Operating Limits -Safe Operating Areas

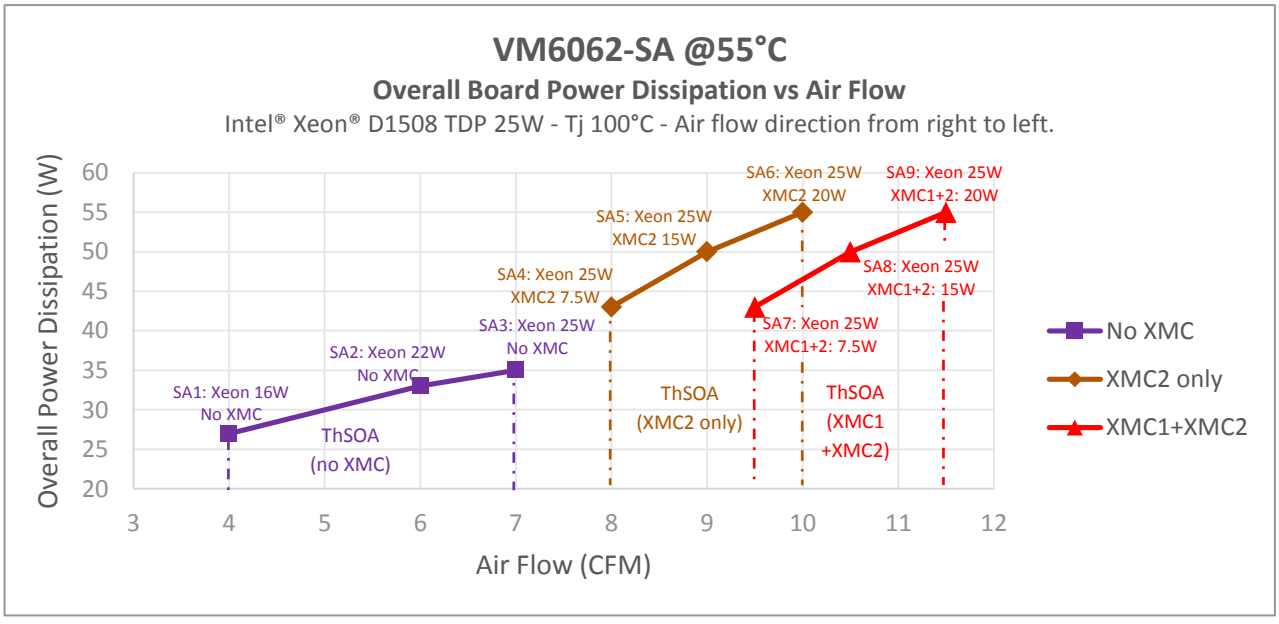
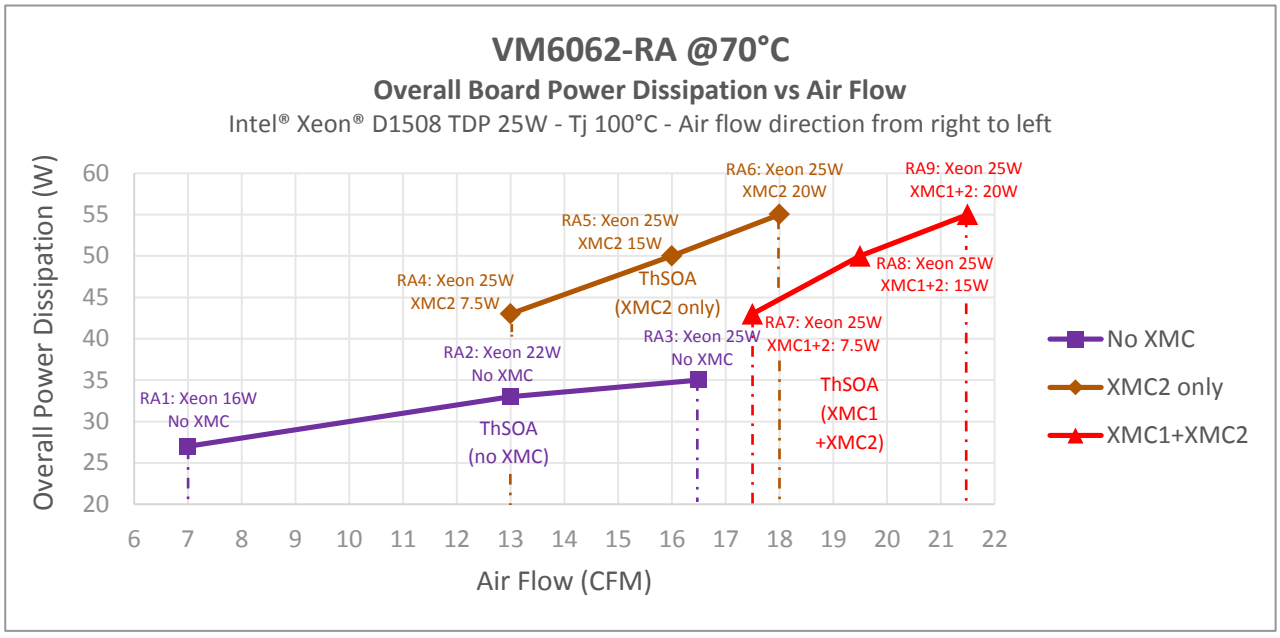


Figure 38: Overall Board Power Dissipation vs. Air Flow @70°C - Thermal Operating Limits -Safe Operating Areas



8/ Conduction-Cooled VM606x-RC

The VM606x is also available in a conduction-cooled configuration referred to as VM606x-RC. This section covers its key features.

8.1. VM606x-RC Overview

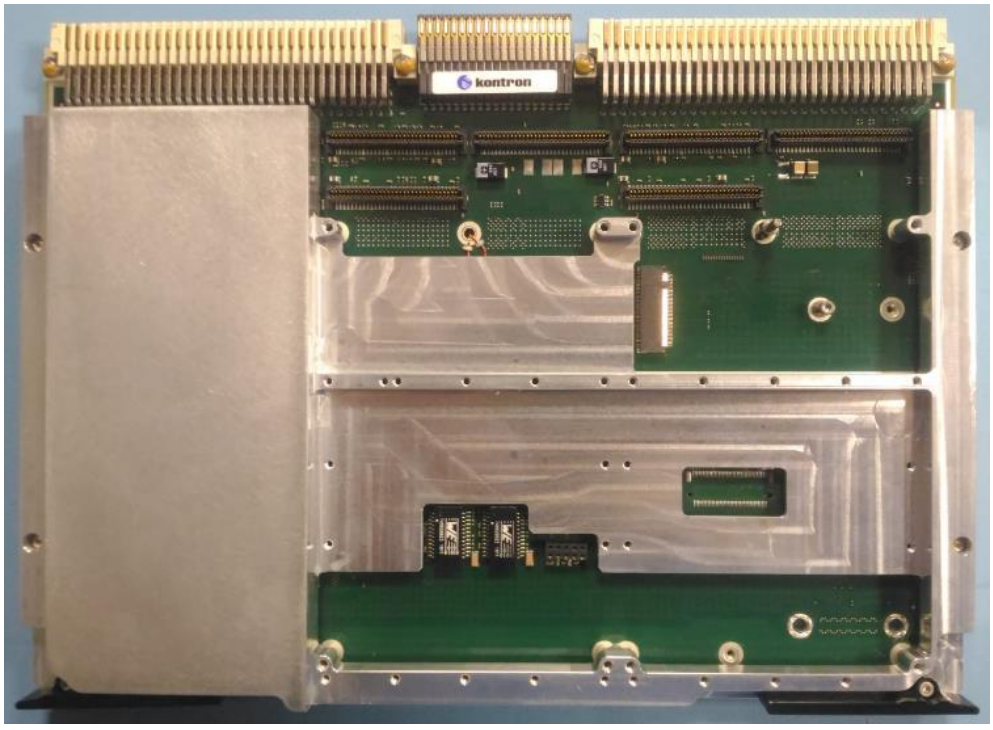
The Kontron-designed thermal frame or "ruggedizer" combines thermal efficiency and mechanical robustness to offer:

- Two different ranges of operating temperature depending on the Xeon® Thermal Design Power (TDP):
  - RC3: from -40°C to +70°C (35W TDP)
  - RC4: from -40°C to +85°C (25W TDP)
- VITA 47 / MIL-STD-810-G high levels of shocks and vibrations specification.
- Enhanced reliability and MTBF.

Moreover, the VM606x-RC retains all the I/Os and add-on cards flexibility provided by the standard VM606x (with the sole exception of the MiniPCI Express card option).

This versatility added to the excellent Xeon® process power and the harsh environment features briefly listed above make the VM606x-RC an ideal solution for numerous applications in defense and industrial sectors.

Figure 39: VX606x-RC Overview



8.2. VM606x-RC Order Codes

Table 70: VM606x-RC Order Codes

Order Code	Description
VM6064-RC4G-00301100	6U VME Single Board Computer 4-core Intel® processor D-1527, 2.2 GHz, TDP 35W, 6 MB cache 32GB dual-bank DDR4 Secure element : TPM Two PMC/XMC sites, two M.2 socket (PMC1/XMC1 and M.2 module in S3 mutually exclusive) Standard P0: 1000BASE-T ETH0 & ETH1 ports, USB 2.0 USB3 & USB0 ports, rear HDMI port, GPIOs, PMC/XMCIOx, utility signals. (1) 6 GPIOs, COM1 & COM2, PMC1 IOs 64ac Battery not equipped Rugged Conduction-cooled RC3 (-40°C to +70°C) Conformal coating

(1) For rear SATA and PCIe interfaces with standard P0, please refer to section 2.3.3 P0 Part Number Change and its Impact on Rear SATA and PCIe Interfaces.

Other SKU and other temperature ranges, including RC4 (-40°C to +85°C), are available on demand. Please contact Kontron.

8.3. VM606x-RC Board Identification

The VM606x-RC identification includes order code, variant, serial number, E. C. Level and Ethernet MAC addresses. It is stored in the VPD EEPROM and labelled in the same manner as the standard VM606x-SA. See "Board Identification" section.

8.4. VM606x-RC Specifications

Table 71: Mechanical Specifications

MECHANICAL SPECIFICATIONS	RC - RUGGED CONDUCTION-COOLED
Plug-in unit type (VITA 48.2)	Type 2, secondary side retainers
Dimensions	6U form factor: 233.35 x 160.0 mm
Height	Single slot
Weight	770 g

Table 72: Environmental Specifications

ENVIRONMENTAL SPECIFICATIONS	RC - RUGGED CONDUCTION-COOLED
Conformal coating	Standard
Cooling method	Conduction
Operating Temperature	RC3: -40°C to +70°C (1) RC4: -40°C to +85°C (2)
Storage Temperature	-50°C to +100°C
Sine Wave Vibration (Operating)	5 to 22 Hz : Displacement 2.5 mm 22 Hz to 2000 Hz: 5 g Sweep rate : 1 octave / minute
Random Vibration (Operating)	5 Hz to 100 Hz: +3dB/octave 100 Hz to 1000 Hz: 0.1 g^2/Hz 1000 Hz to 2000 Hz: -6dB/octave
Shock (Operating)	40 g, 11 ms, half-sine
Altitude (Operating)	-1 500 ft to 60 000 ft
Relative Humidity	95% without condensation

(1) The RC3 temperature range of -40°C/+70°C applies to boards supporting 35W TDP Xeon® SoCs. Temperature should be measured on the left card edge as described in section "VM606x-RC Thermal ".

(2) The RC4 temperature range of -40°C/+85°C applies to boards supporting 25W TDP Xeon® SoCs. Temperature should be measured on the left card edge as described in section "VM606x-RC Thermal ".

8.5. VM606x-RC Peripheral Connectivity and Daughter Cards

As expected for a board in conduction-cooled configuration, the VM606x-RC does not support any front I/O connector. Nevertheless, it retains the front LED indicators and reset push-button.

The equipment of the rear connectors is unchanged.

The VM606x-RC includes all the daughter cards and mezzanines defined on the standard VM606x-SA except the MiniPCIe socket which is not supported.

8.6. VM606x-RC Board Installation and Removal

NOTICE

Running the VM606x-RC at high temperature without tightening the wedgelocks to the cold plate may result in permanent damage to the board.

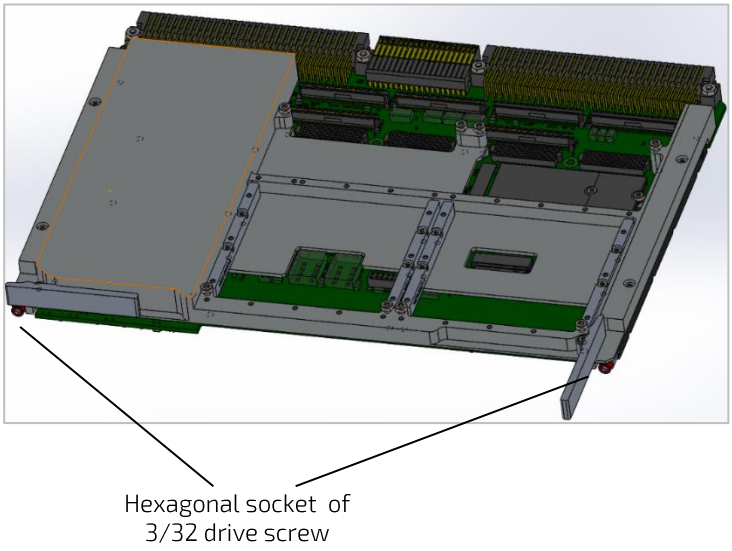
- **Board Insertion and Removal**

The insertion and removal instructions are identical to those applying to the standard VM606x except for the tightening of the wedgelocks described hereafter. Refer to sections "Board Insertion" and "Board Removal".

Wedgelocks Tightening

After inserting the board into the chassis, tighten the wedgelock drive screws (Calmark serie 265) using a 3/32 Allen wrench with a torque value set to 0.9 N.m.

Figure 40: Wedgelocks Tightening



8.7. VM606x-RC Battery Option

On VM606x-RC, the battery is available only as an on-demand option.

8.8. VM606x-RC Thermal Management

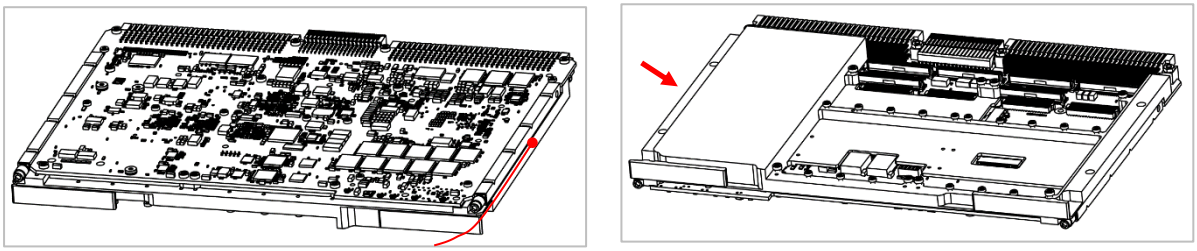
Secondary Side Attachment

To enhance thermal efficiency, the heatsink implements the secondary side attachment defined by VITA 48.2. This type of attachment increases the edge surface area available for thermal exchanges with the cold plate.

Temperature Monitoring - Thermocouple Location

The thermocouple used for monitoring the card edge temperature must be installed at a precise location for the temperature being measured to be consistent with the thermal design. As shown on Figure 41, the thermocouple must be positionned along the left side of the heatsink (when board is horizontal) and halfway between the rear connector and the front of the board.

Figure 41: Thermocouple Location for Board Temperature Monitoring



Add-on Mezzanines and Power Budget

When dimensionning the system, the power dissipated by add-on cards - PMC or XMC essentially - could be significant and should be carefully taken into account. For example a VM606x-RC board with a 25W-TDP Xeon will dissipate at most 35W to 37W. A standard 7.5W PMC will therefore add 20% to the budget.

Thermal Management

The user must set and monitor several parameters to optimize thermal management:

- **Turbo Mode**: for a better control of thermal performance, it is advised to disable this mode.
- **Processor Load**: Kontron advises to keep some margin for real time behavior and stay within 80% of processor load.
- **Card Edge Temperature:** It is the card edge temperature which has been used for the thermal design and the definition of the specified temperature ranges (RC3 up to 70°C or RC4 up to 85°C). Therefore it should be measured as described above and monitored during system qualification to ensure that the board operates in its specified range.
- **Processor Temperature:** As mentionned in section "Temperature Monitoring", the junction temperature as measured by the Xeon® Digital Thermal Sensor (DTS) should not exceed 100°C. This will be the case as long as the temperature operating range specification is met. Nevertheless, in situations where extra power is needed whether from increased performance (turbo mode on, cores running at full load) or from some higher grade XMC, the processor temperature will be the key parameter and the card edge temperature will have to be lowered below the specified temperature to keep the processor junction temperature below 100°C.

Thermal Operating Points

Table 73 below provides some practical thermal operating points in conduction-cooled configurations.
Case 1 deals with a full-load 35W TDP Xeon® board, specified for RC3 temperature range (-40°C/+70°C) and with the processor running full load at Tj max of 100°C. The card edge temperature is measured at 82°C which is well above the specified 70°C. This difference gives some leeway for expansion cards power dissipation or for the necessary margin the processor need in terms of load and junction temperature.

Table 73: VM606x-RC Thermal Operating Points in Conduction-Cooled Configuration

VM6064-RC4G-00301100 - Xeon® D-1527 TDP 35W 2.2GHz								
Case	Temp. Range Specification	Card Edge Temp. (1)		Xeon® Power	Xeon® Tj	Expansion cards & mezzanines	Board Power	Test conditions
		Left	Right					
Case 1	RC3: -40/+70°C	83°C	73°C	35 W	100 °C	No card	49 W	PTU tool rev1.6 : 100% processor load

(1) Test conditions according to Kontron procedure.

8.9. VM606x-RC BIOS Default Configuration

Some BIOS settings have been specifically defined for the VM606x-RC and programmed during production:

- Processor C-States disabled.
- Turbo mode disabled.
- Double refresh rate on DDR4 interface enabled (this setting is mandatory at high temperature).
- 1000BASE-T ports ETH0 and ETH1 routed to rear.
- All PCIe buses that are Gen3 capable (8GT/s) are forced in Gen2 mode (5GT/s).
- All SATA interfaces that are SATA III capable (6Gbps) are forced in SATA II (3Gbps).

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About Kontron – An S&T Company

Kontron is a global leader in IoT/Embedded computing technology (ECT). As a part of technology group S&T, Kontron offers a combined portfolio of secure hardware, middleware and services for Internet of Things (IoT) and Industry 4.0 applications. With its standard products and tailor-made solutions based on highly reliable state-of-the-art embedded technologies, Kontron provides secure and innovative applications for a variety of industries. As a result, customers benefit from accelerated time-to-market, reduced total cost of ownership, product longevity and the best fully integrated applications overall.

For more information, please visit: **www.kontron.com**

CORPORATE OFFICES

FRANCE

150, rue Marcelin Berthelot
ZI de Toulon-Est - BP 244
83078 Toulon Cedex 9 - France
Tel: +33 4 98 16 34 00
Fax: +33 4 98 16 34 01
sales.KFR@kontron.com

GLOBAL HEADQUARTERS

Lise-Meitner-Str. 3-5
86156 Augsburg
Germany
Tel.: +49 821 4086-0
Fax: +49 821 4086-111
info@kontron.com

NORTH AMERICA

9477 Waples Street, Suite 150
San Diego, CA 92121
USA
Tel.: + 1 888 294 4558
Fax: + 1 858 677 0898
info@us.kontron.com

ASIA PACIFIC

1~2F, 10 Bldg, Nº 8 Liangshuihe 2nd Str.
Economical & Techno. Develop. Zone,
Beijing, 100176, P.R. China
Tel.: + 86 10 63751188
Fax: + 86 10 83682438
info@kontron.cn