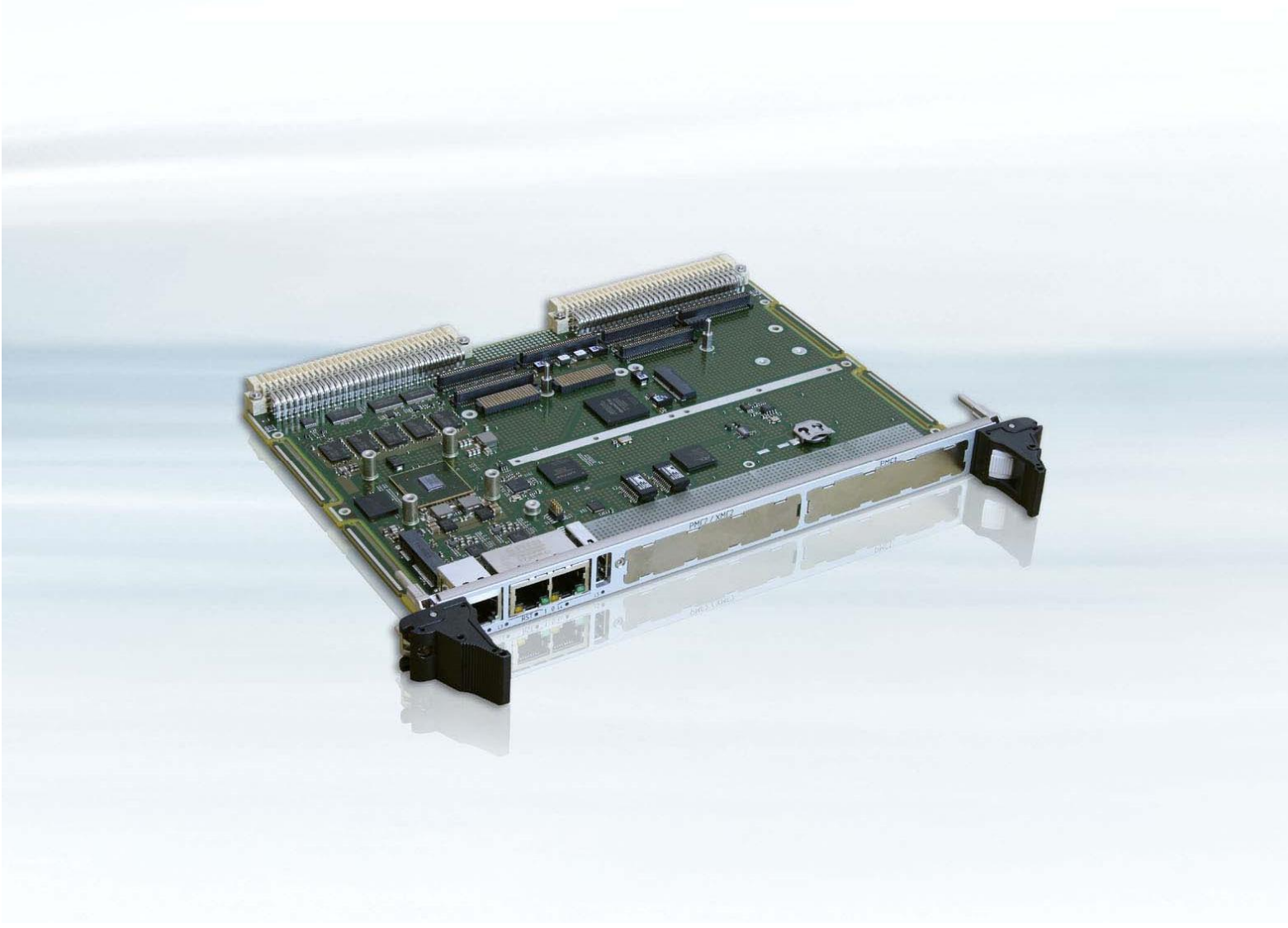
USER GUIDE



VM6103

6U VME Single Board Computer

CA.DT.B38-2e - March 2020

VM6103 - User Guide

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Customer Support

Please contact our support team at support.KFR@kontron.com

Customer Service

As a trusted technology innovator and global solutions provider, Kontron extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly-experienced support enables Kontron to provide exceptional peace of mind to build and maintain successful products.

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Symbols

The following symbols may be used in this user guide

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
NOTICE	NOTICE indicates a property damage message.
	**Electric Shock!** This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	**ESD Sensitive Device!** This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	**HOT Surface!** Do NOT touch! Allow to cool before servicing.
	**Laser!** This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol indicates important information which must be read carefully.
	This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!

Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

General Instructions on Usage

In order to maintain Kontron's product warranty and CE compliance, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty and CE compliance.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Environmental protection is a high priority with Kontron.

Kontron follows the WEEE directive

You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

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For contact information, refer to the corporate offices contact information on the last page of this user guide or visit our website CONTACT US.

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1/ Introduction

The VM6103 is the first member of a full range of High-Performance, Low Power dissipation Kontron range of products featuring QorIQ 'Layerscape' multicore ARM processors coupled with up to 8 GB DDR4 memory.

The VM6103 Connectivity Engine provides a flexible off-the-shelf method for quickly developing and deploying cost-conscious high-performance with low power dissipation tailored systems.

The low power consumption of the powerful Dual-Core ARM Cortex-A53 makes the VM6103 well suited to critical environments such as industrial, transportation and defense applications and offers a straightforward upgrade path for both new customers and existing legacy QorIQ Power Architecture e500, e600 users.

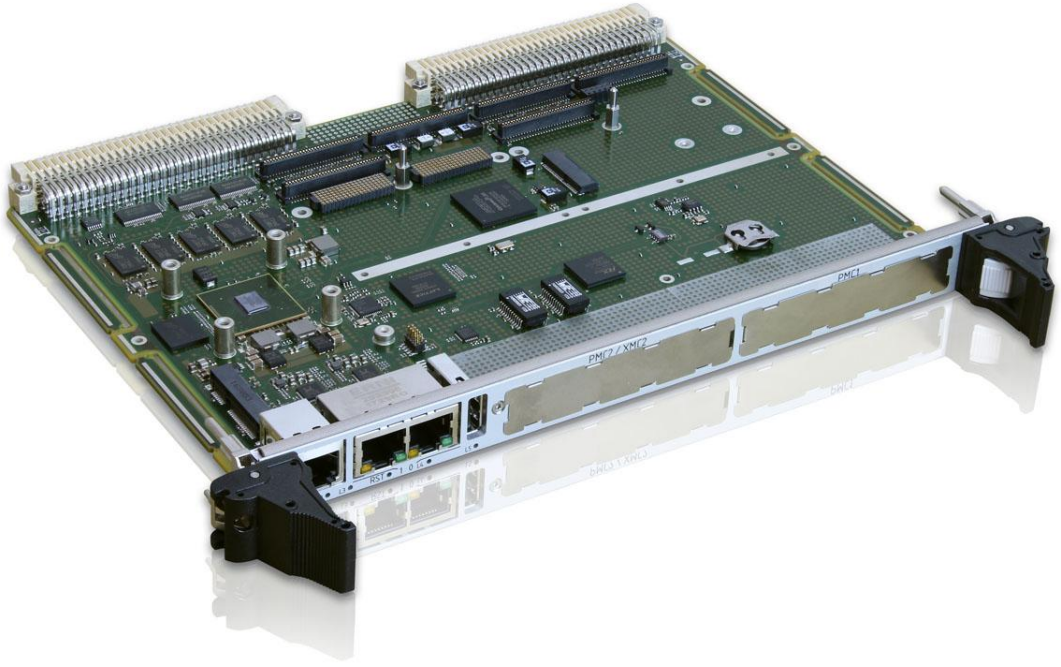
The outstanding flexibility of the design of VM6103 provides numerous I/O expansion slots and the processing upgrade using pinout compatible 4-core processors.

The VM6103 board comes with u-boot firmware and supports Linux. It is covered by Kontron's long-term supply program, which guarantees customers multi-year supply of the product beyond its active life.

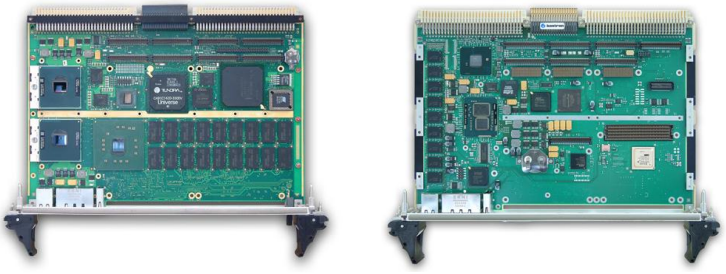
The VM6103 provides exceptional I/O capabilities onboard and outstanding flexibility by being a 6U VME board to provide support for PMC, XMC, miniPCIe and M.2 storage mezzanine cards.

The VM6103's high performance, 2eSST, VME interface helps customers preserve their investment in legacy VME equipment.

Figure 1: VM6103-SA 6U VME Overview



VM6103 are designed to be I/O compatible with the previous generation of x86 6U VME SBC from Kontron. See section 2 - Board Overview for more information on this.



1.1. Manual Overview

1.1.1. Objective

This guide provides general information, hardware instructions, operating instructions and functional description of the VM6103 board. The onboard programming, onboard firmware and other software (e.g. drivers and BSPs) are described in detail in separate guides (see section 1.6"Related Publications").

This hardware technical documentation reflects the most recent version of the product. The "Hardware release Notes" (see section 1.6"Related Publications") keeps track of the successive product evolutions.

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

1.1.2. Audience

This guide is written to cover, as far as possible the range of people who will handle or use the VM6103, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers.

Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, system, cabling, grounding and communications.

1.1.3. Scope

This guide describes all variants of the VM6103 series. It does not cover any PMC/XMC modules which are described in specific guides.

1.1.4. Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are

- 1 - Introduction
- 2 - Installation
- 3 - Additional Board Features
- 4 - Physical I/Os
- 5 - Power and Thermal Specifications
- 6 - VM6103-WA - Characteristics
- 7 - VM6103-SA - Characteristics
- 8 - VM6103-RA - Characteristics
- 9 - VM6103-RC - Characteristics
- 10 - VM6103-RTM - Characteristics

1.1.5. Terminology, Definitions and Abbreviations

In this document, the term:

- **VM6103 will be associated to the 6U VME board including VM6103 modules.**
  - VM6103-SA will be associated to the standard air-cooled commercial version of the board.
  - VM6103-WA will be associated to the extended air-cooled temperature version of the board.
  - VM6103-RA will be associated to the rugged air-cooled version of the board
  - VM6103-RC will be associated to the rugged conduction-cooled version of the board
- **VM6103-RTM will be associated to the 6U VME Rear Transition Module (RTM).**

1.2. Board Overview

1.2.1. Main Features

NXP QorIQ 'Layerscape' LS1023A Architecture

QorIQ LS1023A is a cost-effective, power-efficient, and highly integrated System-on-Chip (SoC) design that extends the reach of the line of QorIQ communications processors, featuring extremely power-efficient 64-bit ARM® Cortex®-A53 cores with ECC-protected L1 and L2 cache memories for high reliability, running from 1.0 GHz up to 1.6 GHz. The LS1023A processor coupled with a DDR4-1600 memory includes a Neon SIMD Co-processor and DP FPU.

The VM6103 running the Dual-Core 1 GHz LS1023A processor features the outstanding performance of 4600 DMIPS/5240 64b CoreMark in a power dissipation budget which does not exceed 10 W.

Soldered DDR4 Memories with the Support of ECC

The processor accesses one memory-channels (36-bit) having a total size of 4 or 8 GB. The DDR4 memory technology used operates at 1,600 MT/s. A 4-bit ECC memory is implemented to detect and correct errors.

Numerous Storage Interface and Non Volatile Memories

The following storage features are available:

- An onboard eMMC 4.5 Flash with 32 GB capacity (Multiple Levels Cell).
- Redundant 128 Mbits serial NOR flash memories are used to store firmware code.
- Two serial 256 Kbits EEPROMs are dedicated to system and VPD data storage.
- A 1 Mbits ferroelectric, non-volatile random access memory allows the backup of critical data when the board is powered off. This 1 Mbits ferroelectric RAM is a user memory device.

All the Flash and non volatile memories onboard have a write protect mechanism taking into account the NVMRO (Non Volatile Memory read Only) signal.

Backplane Switch

Two Gigabit Ethernet links are available on P0 connector. P0 Ethernet routing supports section 2 of VITA 31.1 backplane networking.

Extensive I/O Connectivity

The VM6103 is equipped with the ALMA2f VME controller supporting the VME64x and 2eSST protocols offering up to 320 MB/s peak throughput.

The VM6103 provides two 10/100/1000BASE-T(X) Ethernet interfaces configurable either on front or rear on P0 connector, four EIA-232 serial lines, up to 8 general purpose I/Os (GPIO), three USB 2.0 links, one SATA M.2 storage slot, one miniPCIe slot.

Two onboard mezzanine sites support PCI and one of them supports PCI-Express cards.

Legacy Compatibility

The VM6103 has been designed to offer front and rear legacy I/O compatibility with Kontron's line of x86 and Power VME SBCs, supporting the same Rear Transition Module. The net effect of this fit form function compatibility is to allow our customers an easy line replacement policy of the SBC in deployed systems.

Software

Kontron is one of the few VME and VPX vendors providing in-house support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software manufacturers, Kontron is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

Finally, Kontron grants his customer owners of a maintenance agreement a hotline software support and regular software updates. A dedicated web site is also available for online updates and release downloads. The VM6103 is delivered with the U-BOOT firmware.

The VM6103 supports Yocto framework for creating Linux distribution for embedded applications. In addition, Kontron offers a turn-key USB stick solution based on a BSP Debian Jessie, this solution allows to easily and quickly evaluate VM6103 product.

Contact Kontron for further information regarding other operating systems and software support.

Harsh Environments

Designed specifically for harsh environments, the VM6103 is ideal for applications where high reliability and survivability are a must. Available in Kontron air- and conduction-cooled ruggedization levels, the VM6103 also aims Natural Convection cooled applications.

10-year Long Life Cycle

Investing in a new project is always a challenge and risky. Maximizing the lifetime of an application is therefore a critical issue when it comes to saving development investments.

The VM6103 has been designed with long life cycle components. Beyond the use of standard commercially available components, Kontron offers longevity of supply services (LTS) which are designed to make the VM6103 available for over 15 years.

A comprehensive Health Management is optionally available to support easy field maintenance. All this makes the VM6103 the ideal candidate for long term programs.

Rear Transition Module

The VM6103 supports the VM6103-RTM, a 6U VME Rear Transition Module compliant to PMC I/O Module Standard VITA36 - 199x Draft 0.1 July 19, 1999 (mechanical and PIM format).

Security Features

One of the key features of this new VME embedded computing board is digital security. The VM6103 includes a secure element that enables the support of Kontron's Approtect:

- APPROTECT: protect application integrity and confidentiality with hardware secure Element

Learn more about Security Solution - SEC-Line

1.2.2. Block Diagram

Figure 2: VM6103-Block Diagram

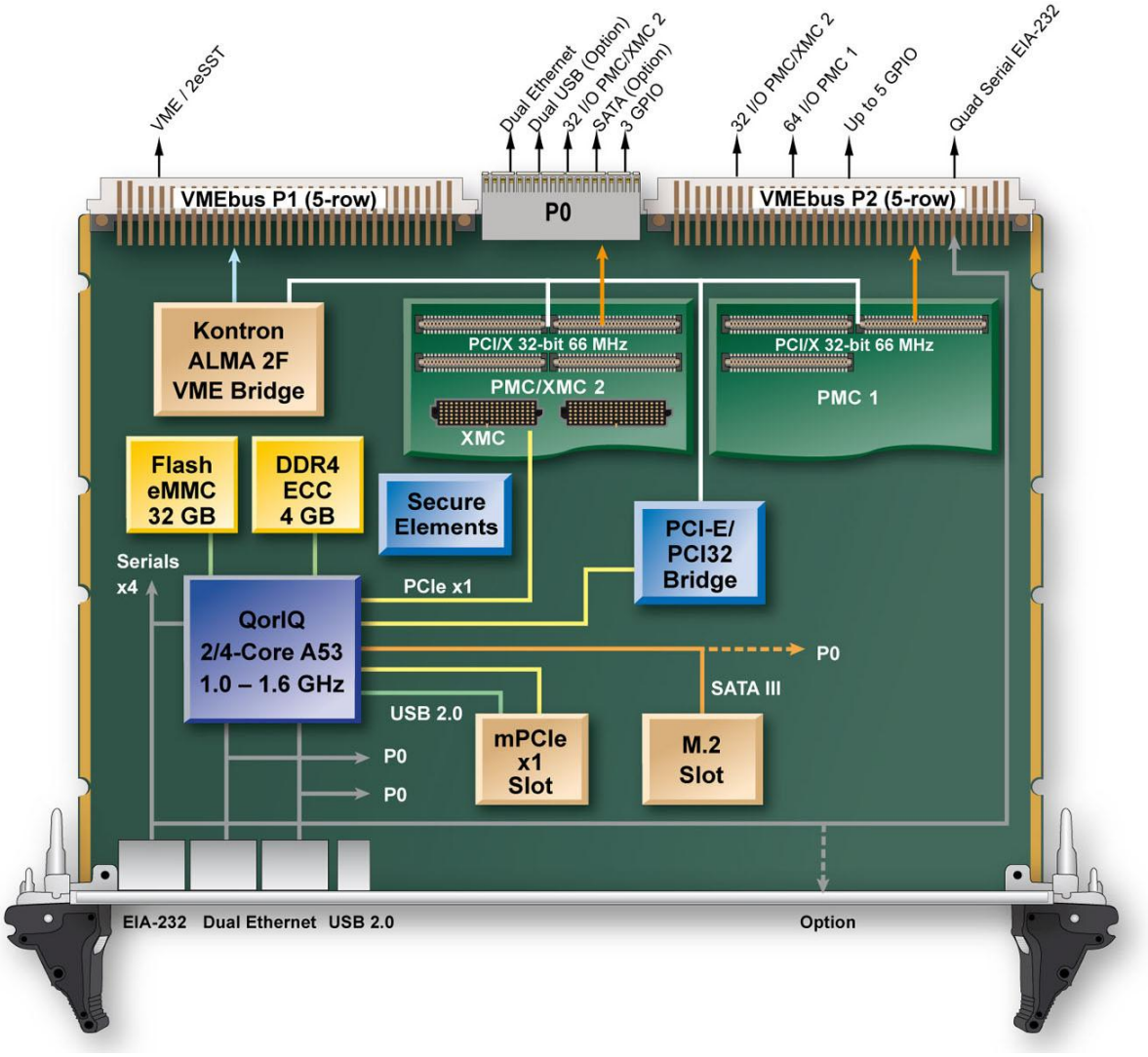
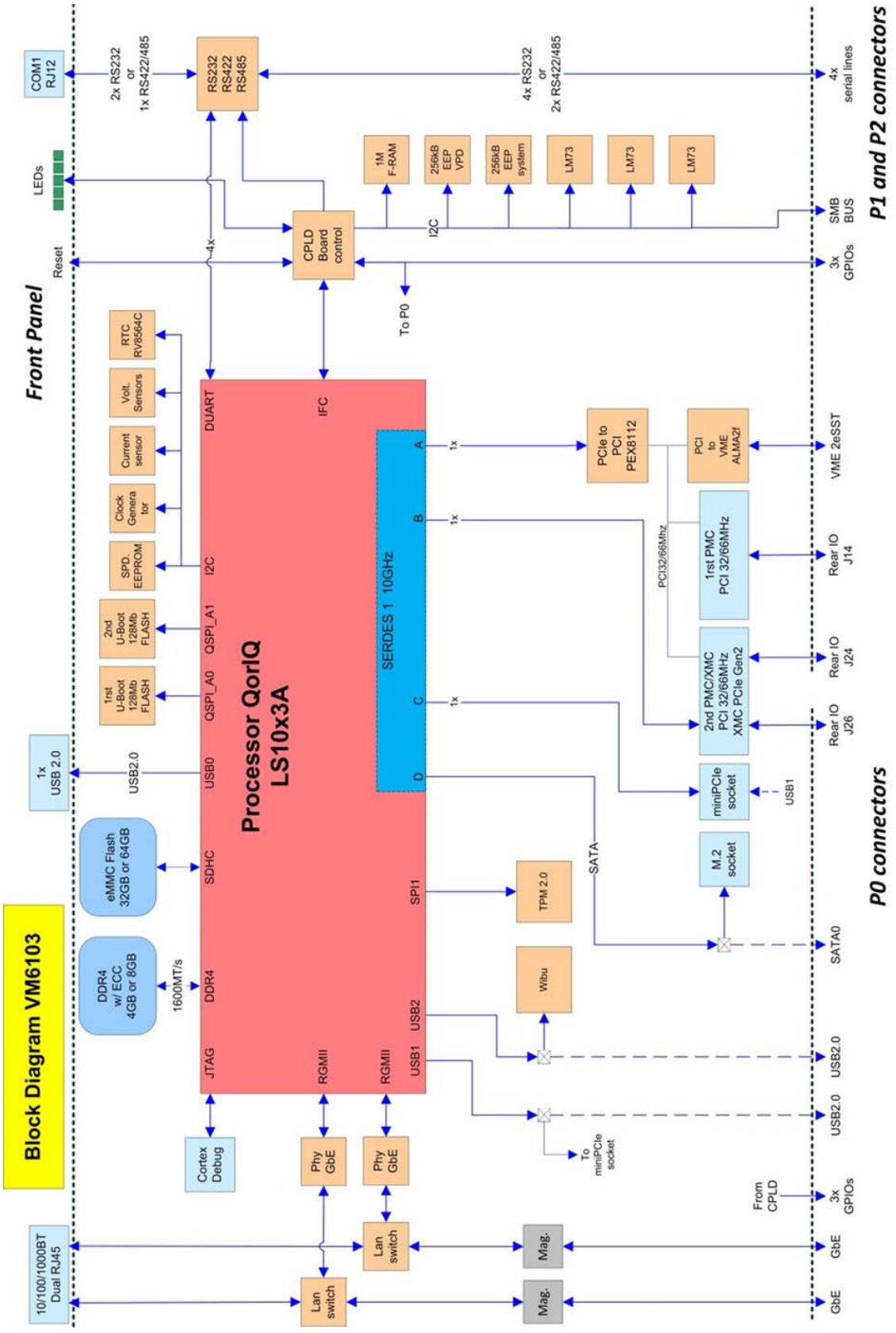


Figure 3: VM6103 Functional Block Diagram



1.2.3. Ordering Information

Manufacturing Options

- CPU Frequency: 1.0 GHz (dual-core)
  1.6 GHz (quad-core)
- DDR4 SDRAM Size: 4 GB total onboard
  8 GB total onboard
- Ruggedization Levels: Standart Air-Cooled (SA)
  Extended Temperature (WA)
  Rugged Air-Cooled (RA) [1]
  Rugged Conduction-Cooled (RC) [1]
- eMMC Flash Size: 32 GB
  64 GB
- P0 connector: Present (including 3GPIOs, two USB ports, 2 Ethernet)
  Absent
- Expansion Slot: Dual PMC, XMC, M.2 and mPCIe Expansion Slots
  Dual PMC, XMC only
- Secure Element: TPM/Wibu
  TPM 2.0
  Wibu (exclusive with USB2.0 port 2 on P0 connector)
  Not equipped
- Battery: Present
  Absent (including holder)
- Serial line / GPIOs: four null-modem serial line (COM1 to COM4)
  Two serial line (COM1 and COM2) with handshaking
- Power-on Built-In-Test: Absent
  PBIT object run time
- Coating (for SA only)

Table 1: VM6103 Order Codes

ORDER CODE		DESCRIPTION
VM6103-SA	VM6103-SA24-00000000	6U Single slot 4HP (0,8") VME SBC -Air-Cooled 'SA' (0°C to 55°C) - LS1023A Dual ARM A53 1.0GHz QorIQ LayerScape Processor - 4 GB soldered SDRAM with ECC - Soldered Flash 32GB eMMC Flash - Dual PMC, XMC, M.2 and mPCIe Expansion Slots - Without P0 connector - - No secure element - - no PBIT - No Coating
VM6103-SA	VM6103-SA24-00100000	6U Single slot 4HP (0,8") VME SBC -Air-Cooled 'SA' (0°C to 55°C) - LS1023A Dual ARM A53 1.0GHz QorIQ LayerScape Processor - 4 GB soldered SDRAM with ECC - Soldered Flash 32GB eMMC Flash - Dual PMC, XMC, M.2 and mPCIe Expansion Slots - With P0 connector - - No secure element - - no PBIT - No Coating
VM6103-WA	VM6103-WA24-00000000	6U Single slot 4HP (0,8") VME SBC -Air-Cooled 'WA' (-20°C to +65°C) with conformal coating - LS1023A Dual ARM A53 1.0GHz QorIQ LayerScape Processor - 4 GB soldered SDRAM with ECC - Soldered Flash 32GB eMMC Flash - Dual PMC, XMC, M.2 and mPCIe Expansion Slots - Without P0 connector - - No secure element - no PBIT - Conformal Coating
VM6103-RA	VM6103-RA24-00000000	6U Single slot 4HP (0,8") VME SBC -Rugged Air-Cooled 'RA' (-40°C to +70°C) with conformal coating - LS1023A Dual ARM A53 1.0GHz QorIQ LayerScape Processor - 4 GB soldered SDRAM with ECC - Soldered Flash 32GB eMMC Flash - Dual PMC, XMC, M.2 and mPCIe Expansion Slots - Without P0 connector - - No secure element - no PBIT - Conformal Coating
VM6103-RC	VM6103-RC24-00100000	6U Single slot 4HP (0,8") VME SBC -Rugged Conduction-Cooled 'RC-4' (-40°C to +85°C) conformal coating - LS1023A Dual ARM A53 1.0GHz QorIQ LayerScape Processor - 4 GB soldered SDRAM with ECC - Soldered Flash 32GB eMMC Flash - Dual PMC, XMC, M.2 and mPCIe Expansion Slots - With P0 connector - - No secure element - no PBIT - Conformal Coating

Table 2: Associated Product Order Codes

ASSOCIATED PRODUCT		
ORDER CODE		DESCRIPTION
RTM	PBV36-P0-VM6-00	6U VME Air-Cooled Rear Transition Module, 2 PIMs, no face-plate to use with PIM-2DP-00
Console Cable	KIT-RJ12DB9	Adaptation Cable RJ-12 <-> DB-9

1.2.4. I/O Interfaces

Table 3: I/O Interfaces

FUNCTION	DESCRIPTION
Ethernet	2x Realtek single port Gigabit Ethernet PHY transceivers with synchronous Ethernet and RGMII interfaces: Two 10/100/1000BASE-T(X) ports available on RJ-45 front panel connectors or on P0 connector (dynamically selectable by software)
VME	ALMA2f VME bridge based on ALTERA Cyclone III FPGA compliant with VITA-1 and VITA-1.1 specifications
USB	Three USB 2.0 channels ▸ USB0 One USB port available on the VM6103 front panel ▸ USB1 USB port available on miniPCIe slot or on rear P0 connector ▸ USB2 USB port available on Wibu secure element or on rear P0 connector
Serial ATA (SATA)	One SATA port is available on M.2 slot (Gen3) or on rear P0 connector (Gen2)
Serial Ports	Four serial ports EIA-232 (or two EIA-422/485) ▸ COM1 EIA-232 with handshaking or EIA-422/485 port on RJ-12 front panel connector or on rear P2 connector ▸ COM2 EIA-232 with handshaking or EIA-422/485 port on rear P2 connector ▸ COM3 EIA-232 null-modem port on rear P2 connector ▸ COM4 EIA-232 null-modem port on rear P2 connector
GPIO	Three General Purpose I/Os on rear P2 connector Three General Purpose I/Os on rear P0 connector (depending on build option) Two extra General Purpose I/Os on rear P2 connector (exclusive with PMC IO).
LED	Five status LEDs on front panel: L1, L2, L3, L4, L5
Reset	One reset button on front panel.
PMC/XMC	One PMC/XMC slot, PCI 32-bit 66Mhz, no 5V tolerant, XMC 1x lane compliant with Gen2 (5 GT/s) PCIe frequency One PMC slot, PCI 32-bit 66 Mhz, no 5V tolerant
miniPCIe	One full size miniPCIe slot type F1/F2 with PCIe and USB 2.0 interfaces.
M.2	One M.2 slot 2242/2260 Type M for SSD module with SATA III interface.

Table 4: Peripheral Connectivity

FUNCTION	VM6103		VM6103-RTM	
	FRONT PANEL	ONBOARD	FRONT PANEL	ONBOARD
Gigabit Ethernet	Y (x2)	-	Y (x2)	-
USB0	Y	-	-	-
USB1 (depending on build option)	-	Y	-	-
USB2 (depending on build option)	-	-	Y	-
SATA (depending on build option)	-	Y	Y	-
COM1	Y	-	-	Y (10-pin)
COM2	-	-	-	Y (10-pin)
COM3	Y	-	-	Y
COM4	-	-	-	Y
GPIOs (depending on build option)	-	-	-	Y (up to 8)
LED	Y (x5)	-	-	-
Reset Button	Y	-	-	Y
SMB	-	-	-	Y
PCIe (miniPCIe)	-	Y	-	-

▸ Front Interfaces

Not available on RC (Rugged Conduction-Cooled) boards

Figure 4: Front Panel Connectors

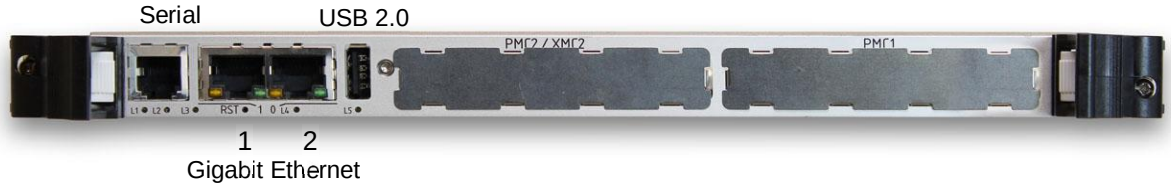
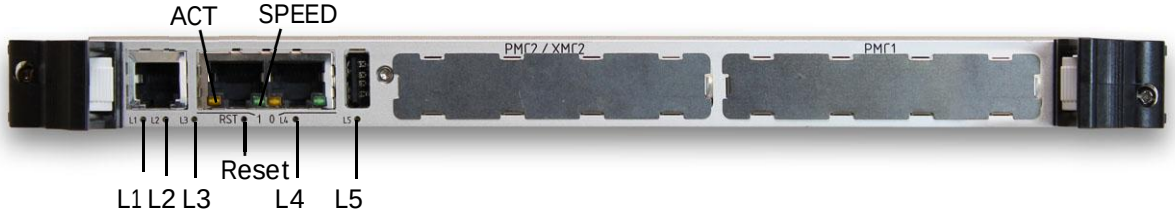


Table 5: VM6103-SA 6U VME Overview

Function	Description	See Also
Serial Ports	COM: 1x EIA-232/EIA-485 UART interface for CPU on RJ-12 connector.	Section 4.1.1 for Pin Assignment
Gigabit Ethernet	Two 10/100/1000BASE-T(X) ports on RJ45	Section 4.1.2 for Pin Assignment
USB	USB 2.0 interface	Section 4.1.3 for Pin Assignment
Reset	Reset push button	Figure 5
LEDs	5 LEDs reporting the board CPU health status and activity	Section 4.4 for LEDs Description
PMC/XMC	2x PMC/XMC slots	Sections 4.2.3 & 4.2.4 for PMC/XMC Description

Figure 5: Reset Button and LEDs



1.2.5. Components Layout

Figure 6: VM6103 Components Layout (Top view)

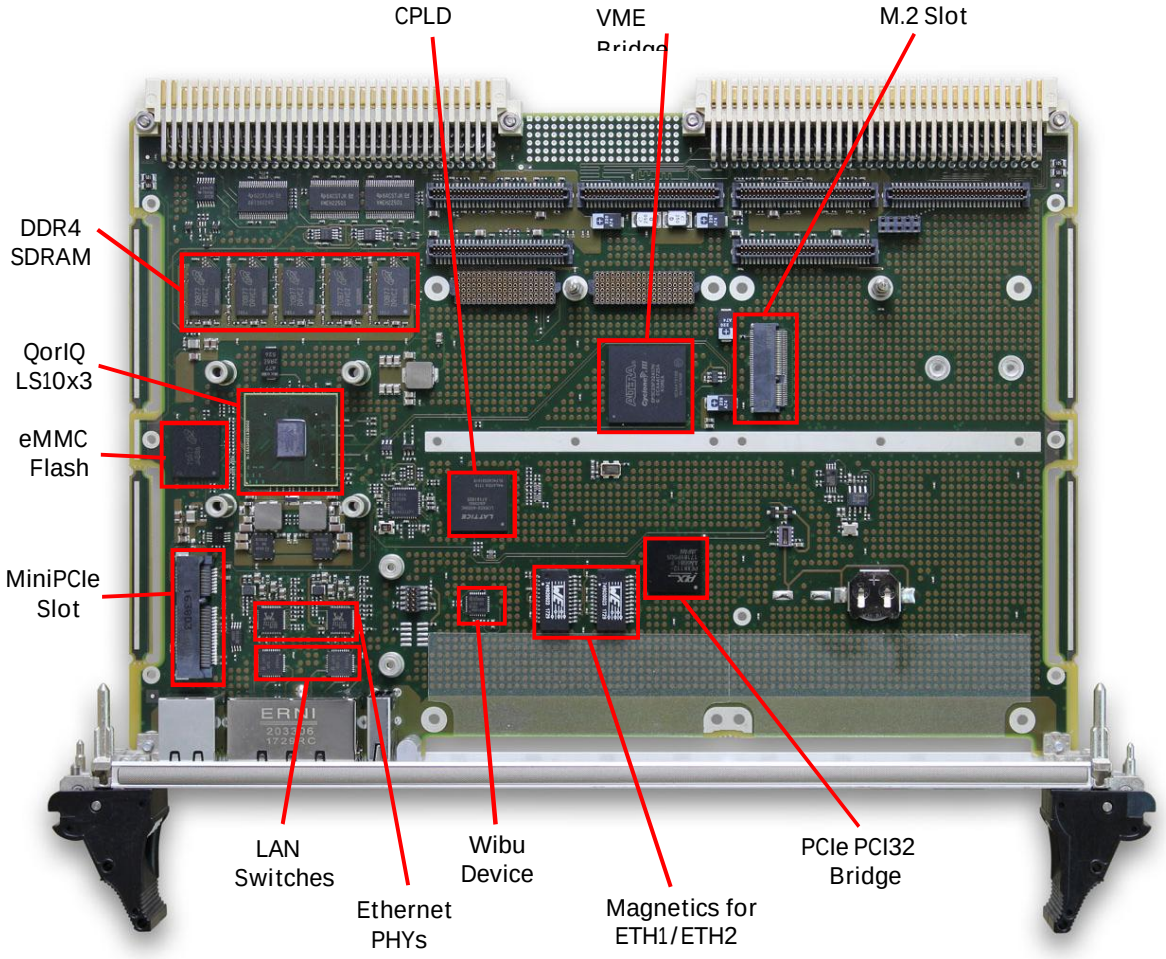
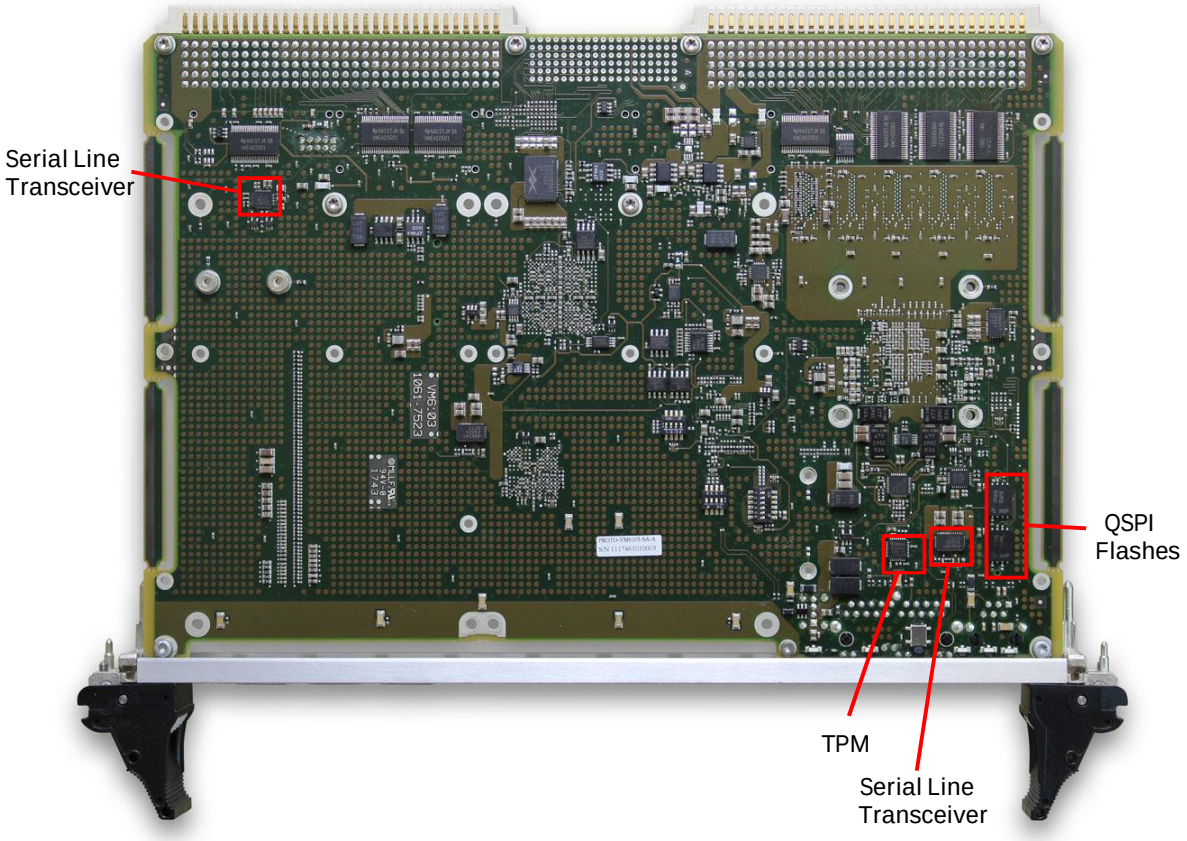


Figure 7: VM6103 Components Layout (Bottom view)



1.2.6. Technical Specification

Table 6: VM6103-SA 6U VME Overview

Form Factor	
Form Factor	6U VME, single slot, 0.8 inch pitch
SoC: QorIQ Layerscape	
Processor	One NXP QorIQ Layerscape LS1023A dual-core or LS1043A quad-core 64-bit ARM® Cortex®-v8 A53 based processor speed up to 1.6 GHz. 1 MB L2 cache Neon SIMD Co-processor Power dissipation lower than 10 W for dual-core 1 GHz version. 28-nanometer silicon technology.
Memory Controller	Integrated 36 bits DDR4 memory controller with ECC support up to 1600 MT/s.
PCI Express 2.0 Interface	1 lane PCIe to PCIe/ PCI bridge to PMC1, PMC2 and VME bridge 1 lane 5 GT/s gen2 PCIe to XMC2 1 lane 5 GT/s gen2 PCIe to miniPCIe slot
SATA	Up to 6 Gb/s integrated Serial ATA host controllers 1 SATA port on M.2 socket (or P0 depending on build option)
USB	1 USB 2.0 port on miniPCIe socket (or P0 depending on build option) 1 USB 2.0 port on WIBU device (or P0 depending on build option) 1 USB 2.0 port on the front panel
Gigabit Ethernet Controller	One Gigabit MAC with two RGMII Interfaces
eMMC Controller	Compatible with the MMC system specification version 4.5
QSPI	Connects to two QSPI flash devices (64 Mbytes each)
IFC	16-bit 100 MHz, for CPLD link
DUART	2 DUART interfaces offering 4 simplified Tx/Rx serial lines
Package	23 mm X 23 mm, 0.8 mm pitch, 780 pin FC-PBGA Unlidded
Memory / Storage	
System Memory	Up to 8 GB DDR4 SDRAM at 1600 MT/s, one memory channel. 4 GB is standard option, 8 GB build option available
SPI Flash	Firmware Boot Device, 2x 64 Mbytes.
eMMC Flash	32 GB 4-bit eMMC 4.5 MLC flash
F-RAM	F-RAM 1 Mbit of non-volatile ferroelectric RAM
EEPROM	One serial 256 Kbit EEPROM dedicated to VPD data One serial 256 Kbit EEPROM dedicated to system data
On-board Controller	
Watchdog	Five watchdog timer with configurable timeout counter with timeout periods from 0.5 to 128 seconds, generates IRQ or reset or IRQ/reset cascaded (cPLD implementation) cPLD watchdog also available.
Ethernet PHY	Ethernet PHY with 2 Ethernets 10/100/1000 BASE-T(X) ports. The Ethernet PHY is connected to the SoC through 2x RGMII links. Each port is software configurable either on front panel (RJ-45) or on rear P0 connector.
System CPLD	One CPLD Board controller for power sequencing, reset handling, monitoring, failure detection, VME I2C communication. Provides configuration/status registers on IFC interface
VME	ALMA2f VME controller with 2eSST
PCI/XMC slot	
PCI	PCI32 @ 66 MHz

XMC	PCIe x1, Gen2 (only for slot 2, no XMC interface on slot 1)
Mezz. Power Supply	+5V, +3.3V,+12V,-12V
Mezz. Max consumption	7.5 W on 5 V, 7.5 W on 3.3 V, 5 W on 12 V, 5 W on -12 V (7.5 W max for the total of 5 V / 3.3 V / 12 V / -12 V)
Mechanical format	PMC IEEE1386 type, SA and RC
Thermal	Air-cooled and conductive, via middle panel (7.5W max.)
VIO	VI/O is fixed and set to 3.3V
miniPCIe slot	
PCIe	PCIe x1, Gen2
USB	USB 2.0 (should be exclusive with P0 build option)
miniPCIe Power Supply	+1.5 V, +3.3 V
miniPCIe Max consumption	2.3 W on 1.5 V
Mechanical format	Full-mini card 52 pin count
Thermal	28.1°C/W
M.2 slot	
SATA	Gen3 (should be exclusive with P0 connector)
PCIe	Not implemented
M.2 Power Supply	+3.3 V ±5%
M.2 Max consumption	2.5A
Mechanical format	Type 2242, 2260, Key M, not compatible with D5 type
Thermal	TDP 1.74W
System Rear Interconnection	
Gigabit Ethernet	2 x 10/100/1000 BASE-T(X) on P0.
USB Ports	2 x high-speed USB Ports on P0.
SATA Ports	1x SATA Ports on P0.
Serial Ports	4 x RS232 null-modem Serial Ports rear panel on P2.
GPIO	3 x GPIOs on P0 and 5 x GPIOs on P2 depending on build option
PMC slot 1 I/Os	I/Os available on P2
PMC/XMC slot 2 I/Os	32 I/Os available on P2 32 I/Os available on P0
VME SMB buses	Two SMB 100KHz buses from cPLD: one master/slave and one master only available on P1.
Front Interface	
Gigabit Ethernet	2 x 10/100/1000Base-T(X) on RJ45 connectors.
Serial Port	1 x RS232 UART interfaces, RJ12 connector.
USB Port	1 x USB 2.0 port for storage or keyboard/mouse
Reset	One Reset button and Shelf Manager control (SMB command on VME)
LEDs	Five Bicolor LEDs on front panel.
Various Interfaces	
CPU debug Interface	JTAG debug connector for CodeWarrior TAP
Board Temperature	ADT7461A on-chip thermal sensor and remote processor thermal diode. Three LM73 thermal sensors.
Misc	
Battery	CR1220 on board holder
Firmware	U-Boot 2016.092.0+g2735535
Backplane Power Supply	+5 V +5%/-3% only fully protected by fuse. +12 V +5%/-3% for PMC/XMC slot. +5 V +5%/-3% standby optional voltage -12 V +5%/-3% for PMC/XMC slot.

Power Consumption	About 10W without mezzanines, without options, without peripherals/devices. This does not include the power dissipation due to the DC/DC efficiency when mezzanines, options and external peripherals/devices are used. VME MAX current: +5 V: 9 VME pins, 11,25 A +3.3 V: 10 VME pins, 12,5 A +12 V: 1 VME pin, 1,25 A -12 V: 1 VME pin, 1,25 A
Operating temperature Range	0.8'' SA: 0°C to +55ºC with 1 slot 0.8" passive module heat sink, forced system airflow (depending on the processor frequency). 0.8" WA: -20°C to +65ºC with 1 slot 0.8" passive module heat sink, forced system airflow (depending on the processor frequency).
Humidity	SA class: 90% RH (non condensing) WA class: 95% RH (non condensing)
Options / Companion board	
RTM	PBV36-P0-VM6-00
M.2	TBD
miniPCIe	TBD
CodeWarrior TAP	CPU JTAG emulator probe

1.3. Environmental Specifications

Table 7: Environmental Specifications

	SA Standard Commercial			WA Extended Temperature			RA Rugged Air-Cooled	RC Rugged Conduction-Cooled
Conformal Coating	Optional			Standard			Standard	Standard
Cooling Method	Convection			Convection			Convection	Conduction
Operating Temperature	0° to +55°C			-20° to +65°C			-40° to +70°C	-40° to +85°C
Storage Temperature	-40° to +85°C			-45° to +100°C			-50° to +100°C	-50° to +100°C
Vibration Sine (Operating)	5Hz to 20Hz 1.25mm displacement 20Hz to 500 Hz - 2g Acceleration / Frequency Range						5Hz to 19Hz 2mm displacement 19-2,000 Hz - 3g Acceleration / Frequency Range	5hz to 22Hz 2.5mm displacement 22Hz-2,000Hz - 5g Acceleration / Frequency Range
Random	5Hz to 100Hz PSD: 0.04g²/Hz						5Hz to 100Hz PSD: +3dB/octave 100Hz to 1000Hz PSD: 0.04g²/Hz 1000Hz to 2000Hz PSD: -6dB.octave	5Hz to 100Hz PSD: +3dB/octave 100Hz to 1000Hz PSD: 0.1g²/Hz 1000Hz to 2000Hz PSD: -6dB/octave
	f (Hz)	10	40	100	200	2000		
	PSD (g²/Hz)	0.01	0.01	0.0007	0.0007	0.00005		
Shock (Operating)	20g/11 ms Peak Acceleration./ Shock Duration Half Sine						20g/11 ms Peak Acceleration / Shock Duration Half Sine	40g/11 ms Peak Acceleration / Shock Duration Half Sine
Altitude (Operating)	-1,500 to 60,000 ft			-1,500 to 60,000 ft			-1,500 to 60,000 ft	-1,500 to 60,000 ft
Relative Humidity	90% non-condensing			95% non-condensing			95% non-condensing	95% non-condensing

1.4. Mechanical Specifications

Table 8: Board Weight Specifications

Technical Specifications			
VM6103	SA / WA Standard Commercial	RA Rugged Air-Cooled	RC Rugged Conduction-Cooled
Board Weight	~400 g	~430 g	~550 g

1.5. MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

Table 9: VM6103-SA24-00000000 MTBF Data

	GB (Hours)		AIC (Hours)	NS (Hours)		ARW (Hours)
	25°C	40°C	40°C	25°C	40°C	55°C
MTBF (Hours)	406 970 h	296 040 h	32 640 h	65 890 h	46 830 h	6 300 h

1.6. Related Publications

The following publications contain information relating to this product:

Table 10: Related Publications

PRODUCT/STANDARD	PUBLICATION	
VM6103 Boards	VM6103 EFT Release Notes VM6103 PBIT User's Guide VM6103 U-Boot User Manual Yocto Linux for VM6103 Release Notes VxWorks7 for VM6103 Release Notes	CA.DT.B39 SD.DT.Gxx SD.DT.G83 SD.DT.G84 SD.DT.G91
CNET	MIL HDBK 217F, CNET RDF93 and CNET RDF2000 Reliability models	
EN	EN55022 Class A: EN61000-6-2: EN61000-3-2: EN61000-3-3: EN60950-1:	Information technology equipment - Radio disturbances characteristics - Limits and methods of measurements Electromagnetic compatibility (EMC) - Part 6-2: Generic standards – Immunity for industrial environments Electromagnetic compatibility (EMC) - Part 3-2 : limits - Limits for harmonic current emissions Electromagnetic compatibility (EMC) - Part 3-3: Limits - Limitation of voltage changes, voltage fluctuations and flicker in public low-voltage supply systems, for equipment with rated current ≤ 16 A per phase and not subject to conditional connection Information technology equipment - Safety - Part 1: General requirements
IEEE	IEEE Std 1101.2-1992 IEEE P1386-2001 IEEE P1386.1-2001	IEEE Standard for Machanical Core Specifications for Conduction Cooled Eurocards Common Mezzanine Card Family CMC Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)
Serial ATA	Serial ATA 3.0 specification, revision 3.0	
VITA	VITA 1-1994 VITA 1.1-199x VITA 35-199x VITA 31.1-200x VITA 20-2000x VITA 38-2003 VITA 47	VME64 Specification VME64 Extension Draft Specification PMC-P4 Pin Out Mapping to VME-P0 and VME64x-P2 Draft Standard Gigabit Ethernet on VME64x Backplane Draft Standard Conduction Cooled PCI mezzanine Card (CCPMC) System Management on VME Environmental, Design and Construction, Safety, and Quality for Plug-In Units

PRODUCT/STANDARD	PUBLICATION	
Underwriters Laboratories	UL94-V0	Standard Physical and environmental Mayers for PCI Mezzanine Cards (PMC)
Mini PCIe	PCI Express® Mini Card Electromechanical Specification, Revision 2.0, April 21, 2012	
M.2	PCI Express M.2 Specification, Revision 1.1	

2/ Installation

The VM6103 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

2.1. Safety Requirements

The following safety precautions must be observed when installing or operating the VM6103. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Special care shall be taken while handling the board: the heat sink and the heat frame can get very hot during operation. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

This board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector pins or traces.
- We strongly recommend our customers to work in an environment equipped with anti-static workbenches with professional discharging equipments.

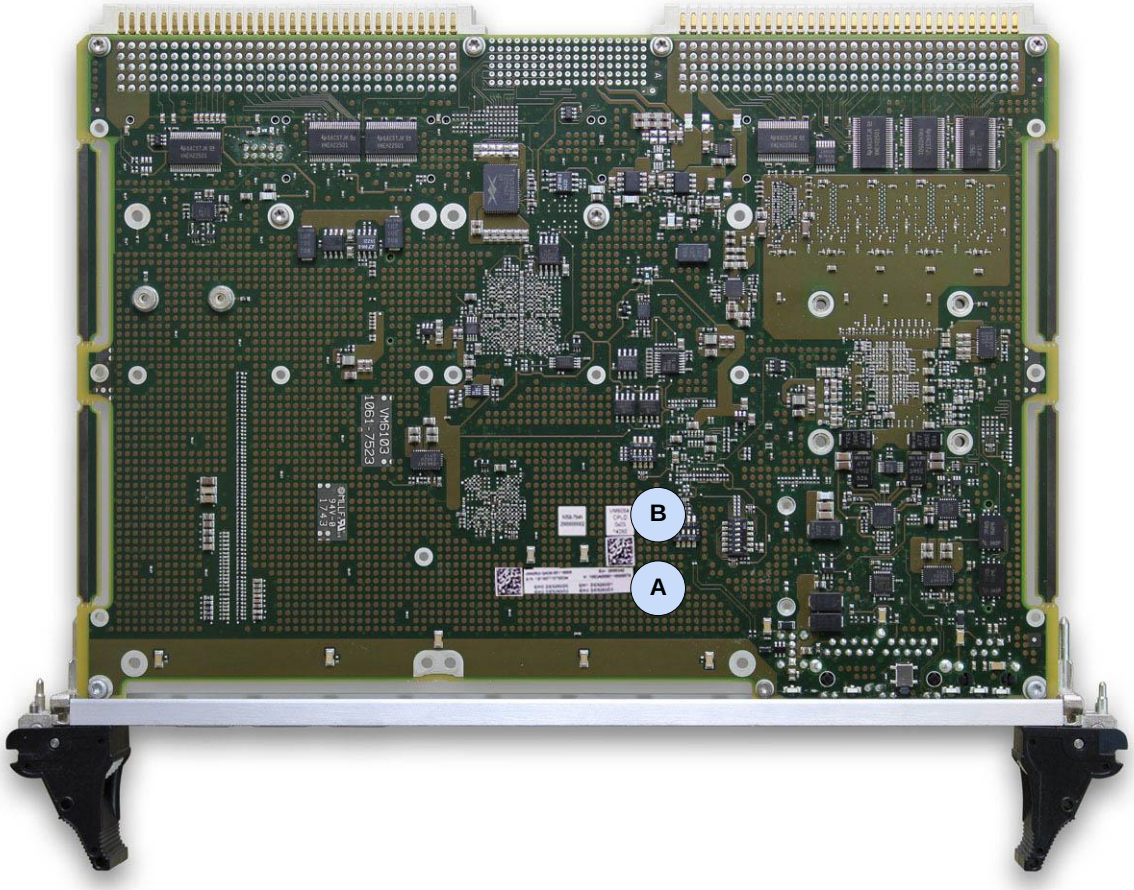
2.2. Board Identification

The VM6103 board is identified by labels fitted to the bottom side of the board.

Figure 8: VM6103 Identification (Bottom Side)

A "Identification" label: Order Code, Serial Number, Variant, E.C. Level, Ethernet MAC addresses

B CPLD Label



The E.C. Level format is “xxxxxLy” where:

- The five digits “xxxxx” indicate the board E.C. Level (PCB revision included)
- “Ly” indicates the mechanical E.C. Level:
  - Letter “L” varies with the environment class (“A” for SA, “B” for WA, “C” for RA and “D” for RC)
  - Digit “y” gives the mechanical E.C. Level

See also section “Vital Product Data” in “VM6103 U-Boot User Manual” - SD.DT.G83 to display the VPD information stored in VM6103 EEPROM.

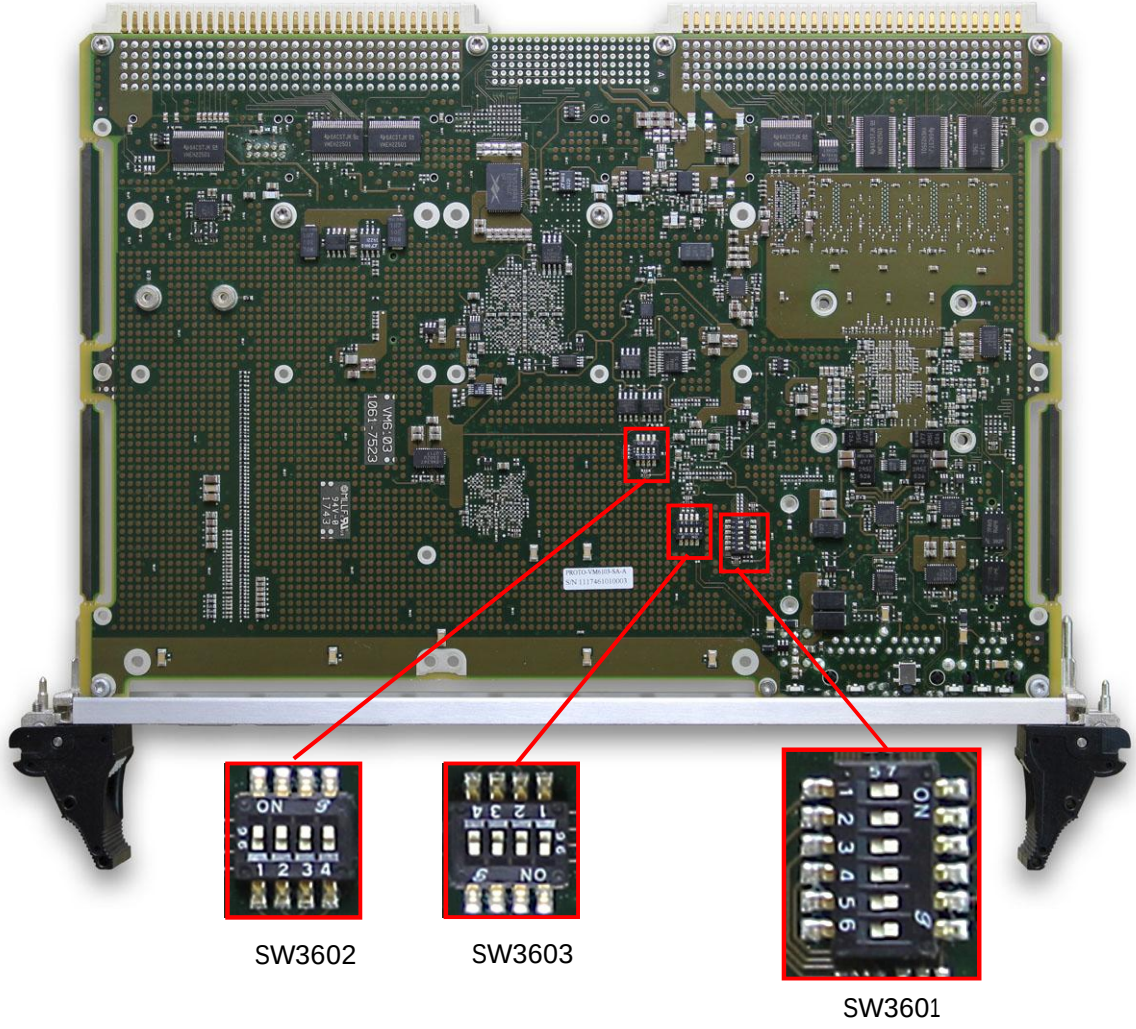
2.3. Package Content

The VM6103 is packaged with several components. The packing contents of the VM6103 Series may vary depending on customer requests.

- CPU Module:
  - Order Code: refer to section 1.2.3 “Order Codes Table” :
    - Processor specifications differ depending on Order Code.
    - Heat sink assembled on the board.
    - Battery assembled on the board
    - Screw kits for peripheral devices
  - Serial adaptation cable RJ-12 <-> DB-9 (Order Code: refer to section 1.2.3 “Order Codes Table”)
- Rear Transition Module:
  - Order Code: refer to section 1.2.3 “Order Codes Table”.

2.4. Board Configuration

Figure 9: VM6103 Micro switches (Bottom side)



2.4.1. Micro switches Description

Table 11: SW3601 Micro switch

PORT	FUNCTION	DESCRIPTION
1	Factory Test Mode	on: Factory test mode is selected off: Normal operation
2	VPD (Vital Product Data) EEPROMs write protect	on: VPD 32Kx8 EEPROM(1), SPD EEPROM and XMC (NVMRO on XMC connector) are write protected. off: VPD 32Kx8 EEPROM, SPD EEPROM and XMC (NVMRO on XMC connector) are not write protected unless signal NVMRO is active (logic 1).
3	System EEPROM write protect	on: System 32Kx8 EEPROM and both QSPI firmware boot flash are write protected(2) off: System 32Kx8 EEPROM and both QSPI firmware boot flash are not write protected unless signal NVMRO is active (logic 1).
4	FRAM (Ferroelectric RAM) write protect	on: 128Kx8 User FRAM is write protected off: 128Kx8 User FRAM is not write protected unless signal NVMRO is active (logic 1).
5	Reserved	
6	Debug mode for onboard power supplies and SPD	on: Debug mode active off: Normal operation

(1) The VPD EEPROM also stores the PBIT detailed results and non-volatile CPLD setup. If this EEPROM is write-protected, these data will not be updated.

(2) Firmware setup modifications will not be saved if SW3601.3 is ON.

All protections are enabled when NVMRO is active, regardless the state of the switches.

Table 12: SW3602 Micro switch

PORT	FUNCTION	DESCRIPTION
1	Rescue Boot Flash	on: CPU boots the firmware from its rescue flash. off: Normal operation. CPU boots the firmware from its non-rescue flash.
2	Firmware Failsafe Boot	on: Boot firmware with default manufacturing settings off: Normal operation.
3	Reserved	
4	Reserved	

Table 13: SW3603 Micro switch

PORT	FUNCTION	DESCRIPTION
1:4	User	The state of each switch (ports 1 to 4) can be read from I/O port @0x80E (cPLD register 0xE), bits 3,4,5,6. on: 1 off: 0

2.5. Initial Installation Procedures

The following procedures are applicable only for the initial installation of the VM6103 in a system. Procedures for standard removal operations are found in their respective chapters.

To perform an initial installation of the VM6103 in a system proceed as follows:

1. Ensure that the safety requirements indicated in Section 2.1 are observed.

Failure to comply with the instruction below may cause damage to the board or result in improper system operation

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the VM6103 refer to Chapter 5. For the installation of VM6103 specific peripheral devices and Rear I/O devices refer to the appropriate sections in current Chapter.

Care must be taken when applying the procedures below to ensure that neither the VM6103 nor other system boards are physically damaged by the application of these procedures.

To install the VM6103 perform the following:

1. Ensure that no power is applied to the system before proceeding.

When performing the next step, DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors

2. Ensure that P0 connector is not damaged. Check that tongue on the bottom of P0 connector is not missing or bent. Check that female pins of P0 connector of VM6103 are intact. Ensure also that the pins of J0 of the backplane are not bent.
3. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.
4. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
5. Fasten the front panel retaining screws.
6. Connect all external interfacing cables to the board as required.
7. Ensure that the board and all required interfacing cables are properly secured.

The VM6103 is now ready for operation. For operation of the VM6103, refer to appropriate VM6103 specific software, application, and system documentation.

2.6. Standard Removal Procedure

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Section 1.2.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

Care must be taken when applying the procedures below to ensure that neither the VM6103 nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.
5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.

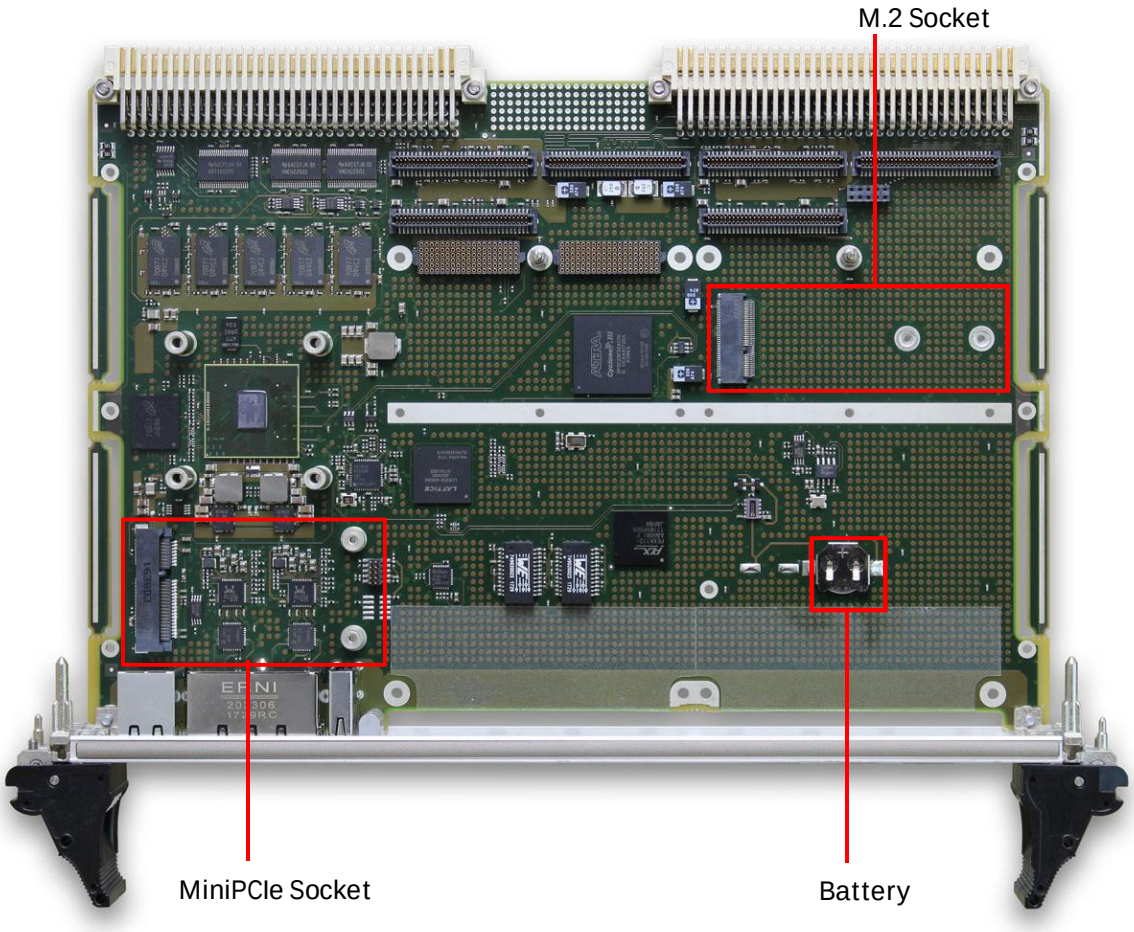
Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

7. Dispose of the board as required.

2.7. Installation of Peripheral Devices

The VM6103 is designed to accommodate a variety of peripheral devices whose installation varies considerably. The following sections provide information regarding installation aspects and not detailed procedures.

Figure 10: VM6103 Peripheral Devices



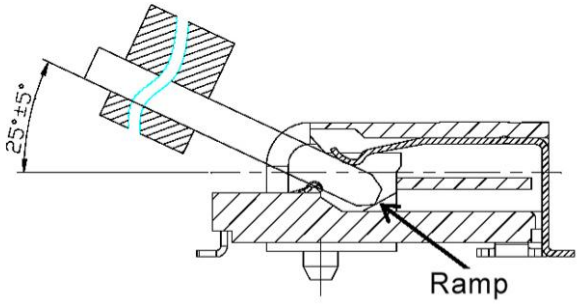
2.7.1. M.2 Module Installation

The VM6103 is equipped with a M.2 socket, supporting one M.2 22 x 42 mm (M key) or one M.2 22 x 60 mm (M key) form factor.

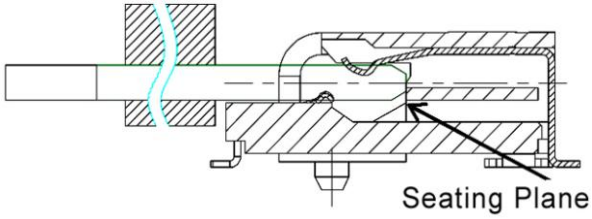
To install a M.2 card:

1. Align the notch at the edge of the M.2 card with the key in the connector.

Insert the M.2 card into the connector with angle 25° until module touch HSG ramp.



Rotate the module to horizon by hand and make sure the card's edge touch HSG seating plane..



Use the provided kit screw to secure the card on the system board.

2.7.2. MiniPCIe Device Installation

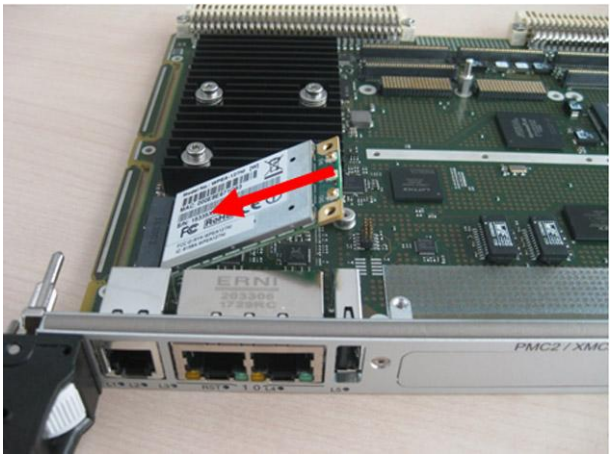
The system board is equipped with 1 Mini PCIe slot. This slot authorizes the insertion of miniPCIe card compliant with full size F1 and F2 Type.

- **miniPCIe Slot Dimension:**

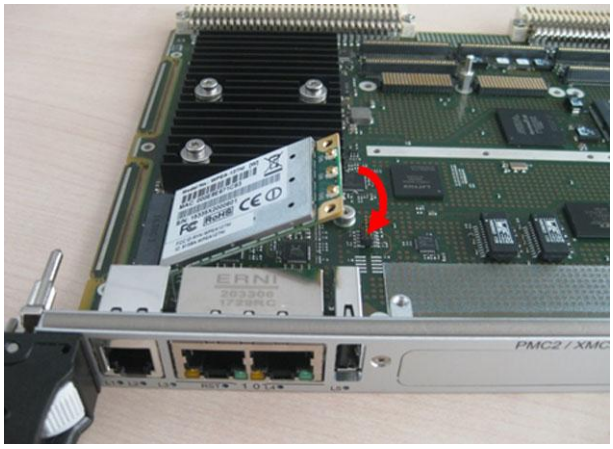
- Maximum top height of miniPCIe card is limited to 6.55mm in order to satisfy the maximum height requirement (13.71mm) defined in VME standard.
- Maximum bottom height of miniPCIe card is limited to 1.35mm by M.2 standard.

Installation Procedure:

1. Grasp the Mini PCIe card by its edges and align the notch of the PCIe card with the key in the connector on the system board.

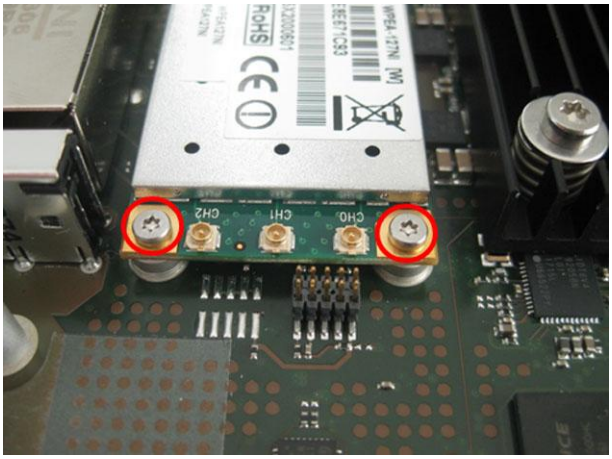


2. Push down on the other end of the Mini PCIe card



The insertion of each module is done obliquely as shown on the figure above. The module should be leaned on the fixing spacer before screwing the mounting screws.

3. Use the provided mounting screws to secure the card on the system board.



Each module is mounted with two M2.5 hexalobular screws of 6 mm length without washers, tighten with a torque of 0.5N.m [+/-0.05N.m]) with help of a T8 screwdriver. Apply “Loctite 222e” threadlock on each screw.

2.7.3. Battery Replacement

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. The battery is used to run a time of day clock during the absence of power. Operation without the battery is possible but the date and time will not be retained in the absence of power. Alternatively, the VME RTC_BAT signal on P0 can provide a 3.3V voltage from the backplane to retain the date and time.

Make sure not to remove the battery support, this could damage the heatsink.

To replace the battery, proceed as follows:

- Turn off power.
- Use a thin plastic tool to push the battery outside the safety cache. Push from the right or left top side of the safety cache.
- Remove the battery.
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

⚠CAUTION

Danger of explosion when replacing with wrong type of battery. Replace only with the same or equivalent type recommended by the manufacturer. The lithium battery type must be UL recognized.

Do not dispose of lithium batteries in general trash collection. Dispose of the battery according to the local regulations dealing with the disposal of these special materials, (e.g. to the collecting points for dispose of batteries).

Reference of the battery used on the VM6103: RENATA CR1220MFR
The design of an electronic circuit powered by a component class battery requires the designer to consider two interacting paths that determine a battery's life: consumption of active electrochemical components and thermal wear-out.

Refer to section 6.3, “Battery Replacement”, page 93, for the reference of the battery used on VM6103-RA. Indeed, because of low temperature constraints, a battery with extended temperature grade must be used.

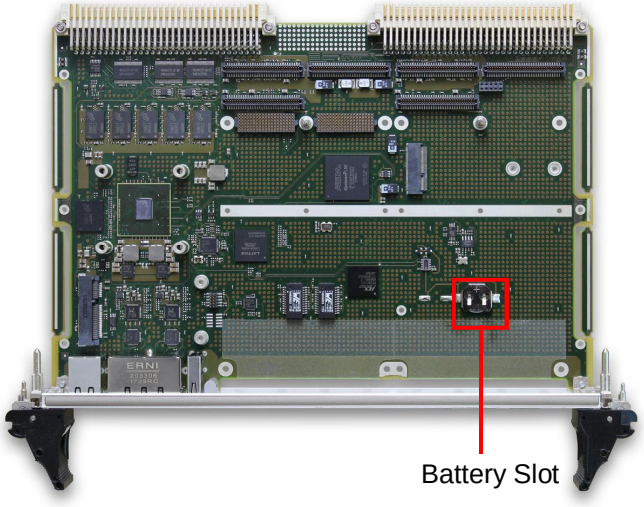
Battery Life

The RTC circuit power consumption is specified at 500 nA, giving an expected duration of more than 8 years in the absence of external power. In case of storage temperature or operating temperature is higher than 55°C or lower than 0°C, the battery life is reduced to 7 years in worst case.

Battery Use

Battery is used to save the date and the hour parameter of external RTC.
See also section 3.1 “RTC, Watchdog, Timers” page 48. Firmware parameter are saved on system flash EEPROM.

Figure 11: Battery Slot



2.8. PMC Installation

PMC modules are delivered with a full kit of parts for mounting them, and the user guide for the module normally contains instructions on how to fit the module.

The installation of the PMC on the VM6103 conforms to the IEEE P1386.1 standard.

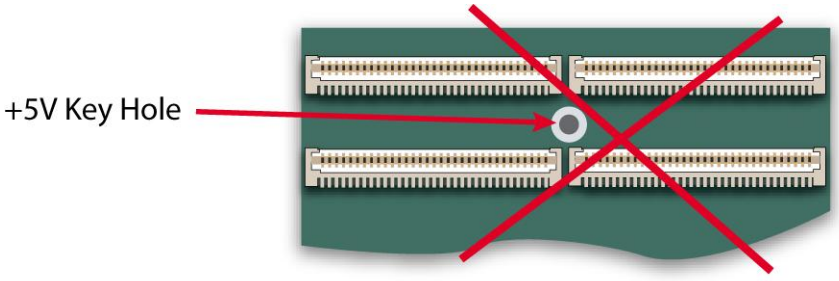
To install the XMC/PMC module, refer to Figure 12 to Figure 15 and follow the steps below:

To avoid ESD damage, wear an antistatic wrist strap to discharge static electricity while performing any part of the installation that involves touching the VM6103 board or the XMC/PMC.

If you can't wear an antistatic wrist strap, touch one hand to the bare metal surface to provide grounding.

1. Place carefully the VM6103 with the backplane connectors facing you on a static dissipative surface connected to a common ground by a low-resistance connection. Do not slide the board over any surface.
2. Remove the blanking plate from the appropriate XMC/PMC slot of the VM6103.
3. Check that the standoffs are attached to the XMC/PMC.
4. Install the XMC/PMC, component-side down, aligning the PCI connectors with their mating connectors on the VM6103 and the XMC connector if available. Press them together so that the friction from the pins holds them together. Insert the standoff plug mounted on the VM6103 into the keyhole. The module's bezel will fill the slot and provide a connection to the module.

Make sure not to remove the battery support, this could damage the heatsink.



5. Screw the XMC/PMC in place using the 4 mounting points, on the bottom side of the VM6103. You need a Phillips screwdriver for this stage.
6. The XMC/PMC attachment is now complete.
7. Insert the VM6103 into the chassis making sure it is plugged into the backplane.

Figure 12: PMC Installation on PMC Site 1

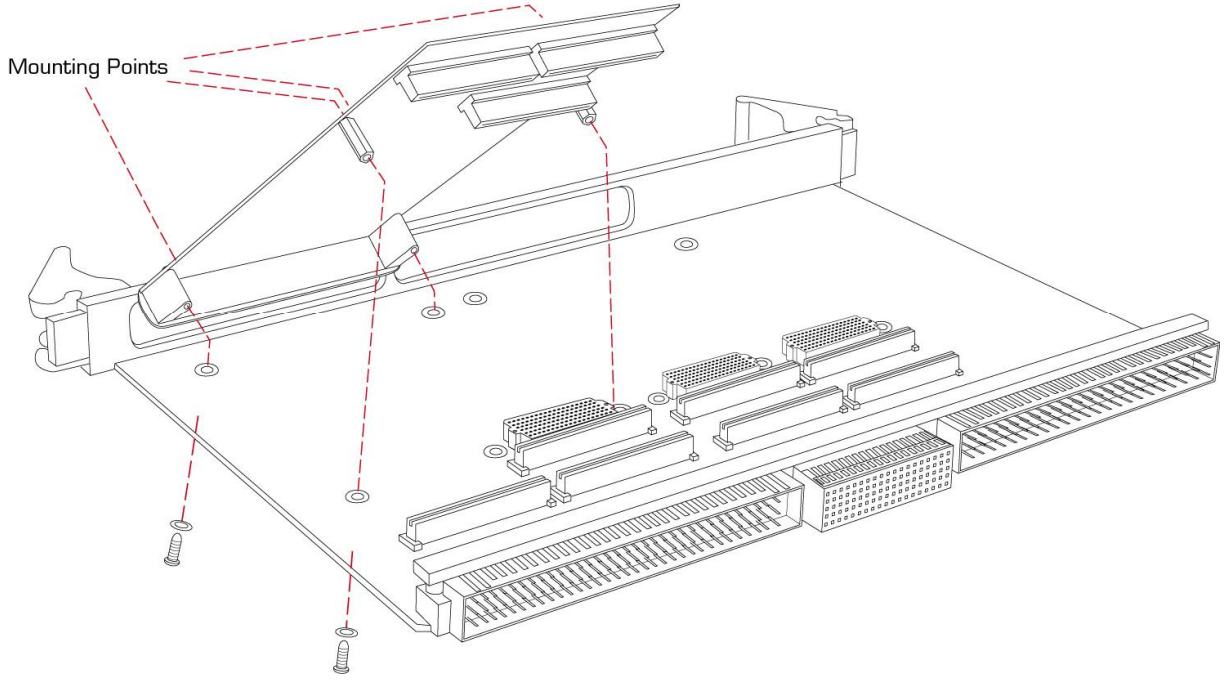
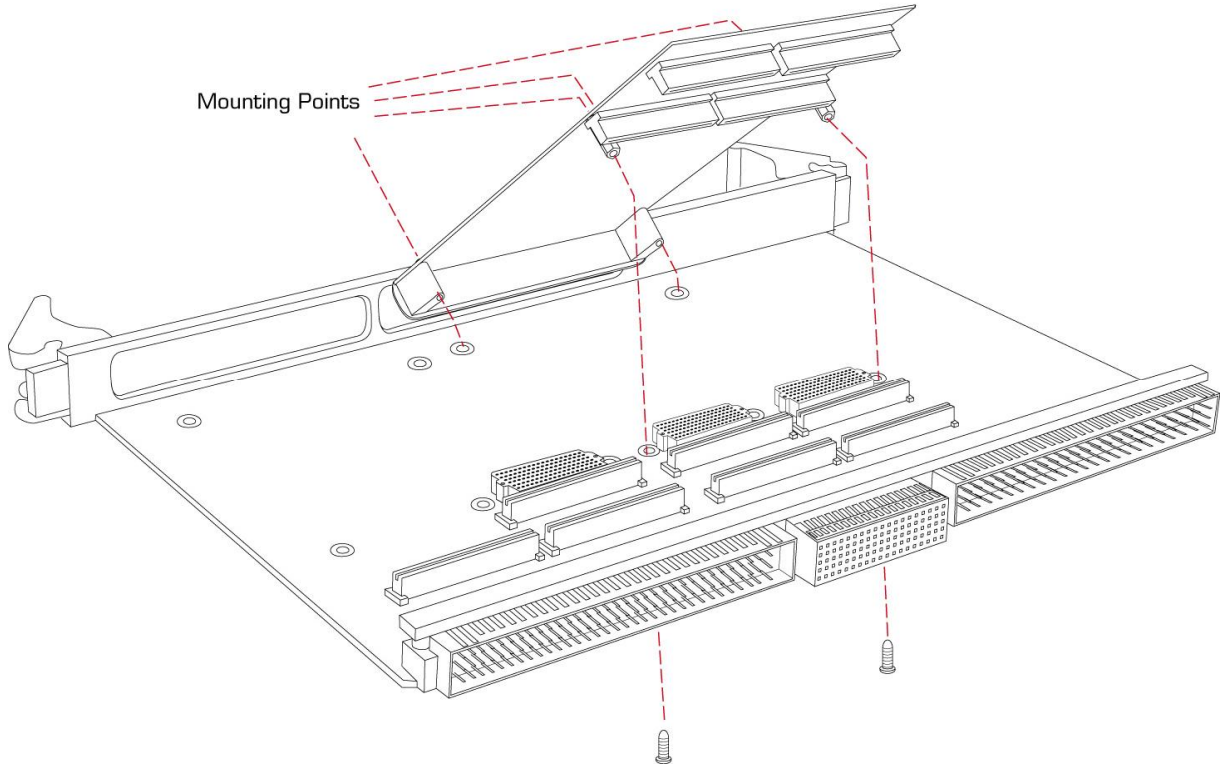


Figure 13: PMC Installation on PMC Site 2



2.9. XMC Installation

The XMC board standard is based on the PMC mechanical definition, and occupies the same board area.

The XMC board add one new connector to the connectors already on a PMC. The new connectors support high-speed differential signals for fabric communications.

Figure 14 shows a XMC fitted only with the XMC connector.

Figure 14: Example of XMC Board

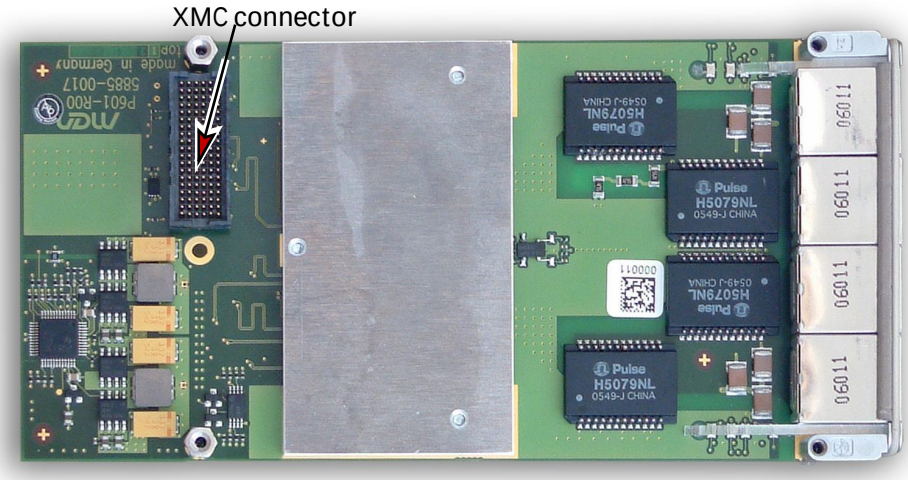
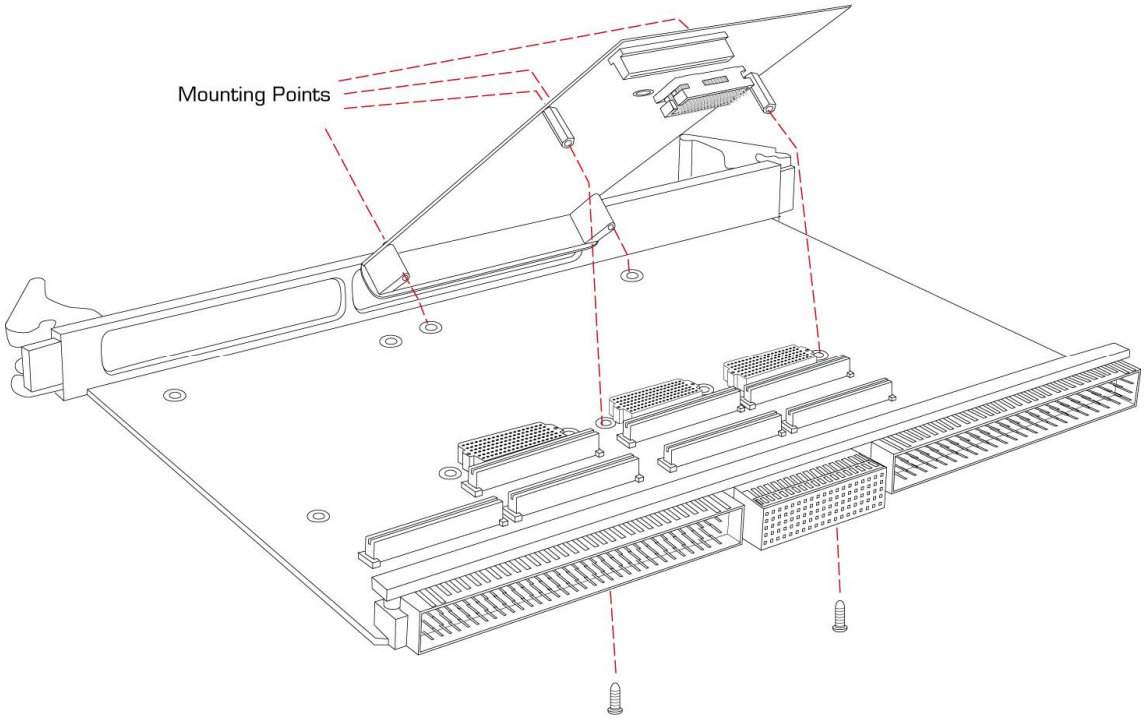


Figure 15: XMC Installation on PMC Site 2



2.10. Software Installation

The installation of all onboard peripheral drivers is described in detail in the relevant Driver Kit files or Board Support Packages (BSP).

The installation of an operating system is dependent of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.

3/ Additional Board Features

3.1. RTC, Watchdog, Timers

3.1.1. Real-Time Clock (RTC)

The VM6103 offers a standalone, high-precision and low-power Real Time Clocks (RTC) component located on the QorIQ I2C bus (RV8564 by Micro Crystal).

Standby power supplied to the RV8564 RTC

When the VM6103 is powered off, the RTC is powered by the onboard battery. On customer request, the RTC could also be powered either through the 5.0V_STANDBY rail or the VBAT rail on the VME backplane.

To ensure data retention in the RV8564 RTC, VBAT must be set in the range [2.5V - 5.5V]. The maximum current drawn over the -40°C/+85°C temperature range is 500nA (VBAT= 3V, no I2C activity) or 550 nA (VBAT=5V, no I2C activity).

Standalone low-power RTC RV8564

The RV8564C2/B RTC by Micro Crystal features an internal oscillator, date and time keeping module with programmable alarm, timer and interrupt functions. It has an ultra low-power consumption in time keeping mode: 250 nA, typical and 500 nA, maximum. Its stability is 20 ppm at 25°C. It is connected to the QorIQ I2C bus.

RTC Management by Firmware and OS

At each startup, the Firmware retrieves the date and time information from the high-precision RV8564 RTC.

Any update of date and time in the Firmware settings will be done in RV8564 RTC. Regarding the RTC management by the OS, the OS should use the high-precision RV8564 RTC driver.

If no power is applied on the RV8564 RTC, the Firmware displays the Firmware build date and time instead of the current date and time.

Century flag

For compatibility reasons, the Firmware implements the century flag for the high-precision RTC as follows:

- Century Flag C = 0 for 1900-1999 years
- Century Flag C = 1 for 2000-2099 years.

The user should check that the OS driver implements the same convention.

3.1.2. QorIQ Watchdog Timer

The QorIQ processor of VM6103 offers five watchdog timers. The timers are enabled by software. Once enabled it must be restarted at regular intervals. If servicing does not take place, the timer times out. Upon timeout, the watchdog timer asserts the timeout signal as reset request to COP.

There is also a provision for watchdog timer signal assertion by time out counter expiration. There is an option of programmable interrupt generation before the counter actually times out. The time at which the interrupt needs to be generated prior to counter time out is programmable.

All watchdog timer modules use 32 KHz clock, driven at device input RTC pin for their counters.

The watchdog has the following features:

- Configurable timeout counter with timeout periods from 0.5 to 128 seconds,
- Time resolution of 0.5 seconds
- Programmable interrupt generation prior to timeout
- The duration between interrupt and timeout events can be programmed from 0 to 127.5 seconds in steps of 0.5 seconds.

3.1.3. CPLD Watchdog

In addition to the standard watchdog timer included inside the QorIQ, the cPLD includes a hardware watchdog timer that can be used by the operating software to monitor the normal operation of the system.

It is enabled by software, and once enabled must be restarted at regular intervals.

If not, its expiration sets off an interrupt (IRQ) to the local processor, a board reset, or a board power-cycle.

The watchdog has the following features:

- Timeout programmable from 1 to 511 periods, by steps of 2 periods
- Periods of 1s or 1mS
- Lock bit: when set, can only refresh (restart) the watchdog, but not change its settings
- 4 modes: timer, reset, interrupt, or power-cycle
- Restart counter: can manage the remaining number of resets or power-cycles done by the watchdog before giving-up.

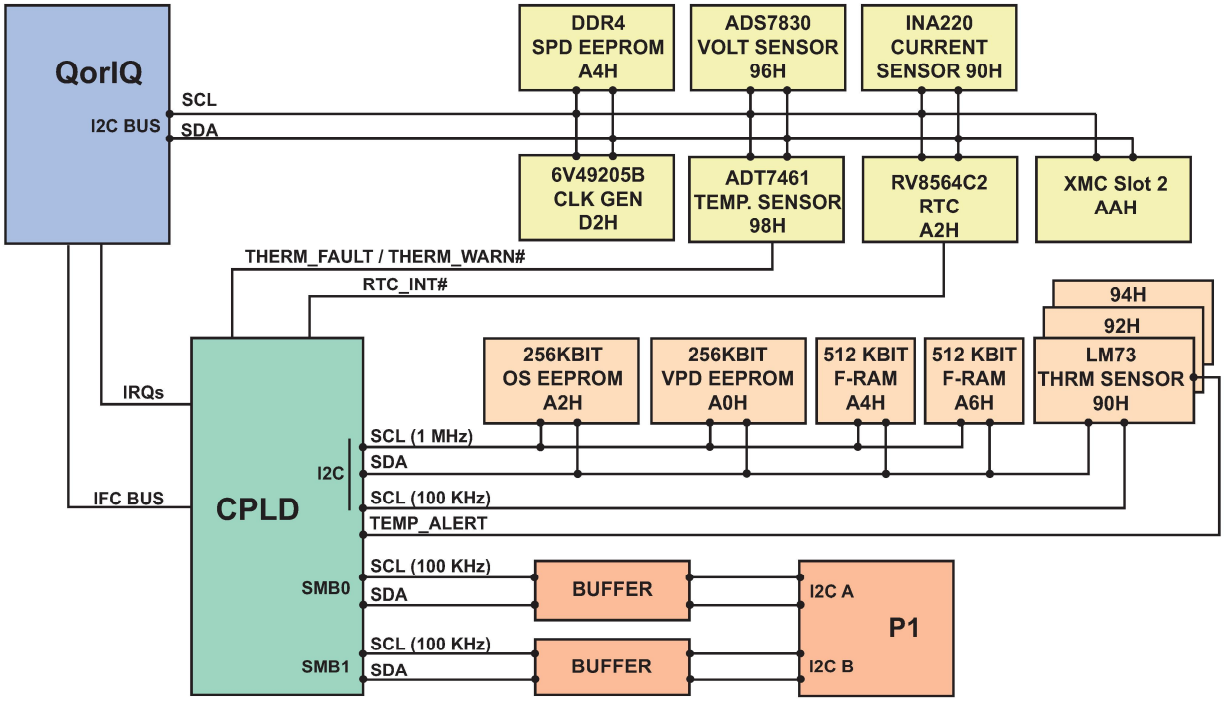
3.2. I2C Structure

The VM6103 board features four I2C busses.

- The first one is attached to the QorIQ processor.
- The remaining i2C busses are handled by the CPLD device. The Figure 27 “I2C Diagram” shows the component attached to the different I2C buses.

I2c addresses shown below are 8-bit values with read/write bit. Shift one bit right to get 7-bit addresses.

Figure 16: I2C Diagram



I2C PLD DEVICE	7-BIT I2C ADDRESS	I2C ADDRESS BYTE
LM73 on TOP	0x4A	0x94 / 0x95
LM73 on Top (close to CPU)	0x48	0x90 / 0x91
LM73 on BOTTOM	0x49	0x92 / 0x93
VPD EEPROM	0x50	0xA0/0xA1
SYS EEPROM	0x51	0xA2/0xA3
FRAM 128Kx8	0x52/0x53	0xA4/0xA5 / 0xA6/0xA7

CAUTION: The FRAM memory of 128Kx8 is seen as two devices of 64Kx8 on the I2C bus.

3.3. CPLD Features

The CPLD manages following features:

- Power-on/off control
- Reset control
- Local environmental control/monitoring
- LPC interface to processor
- I2C interfaces to local I2C bus, and backplane I2C busses (rear P1)
- LEDs control
- Serial lines multiplexer
- Serial VPD and user memories
- User and system GPIOs
- Internal registers that allow system management

3.3.1. VM6103 I2C Interface

The VM6103 implements two SMBus on backplane P1.

- VME SMbus 0/1 master interfaces:

I2C bus 1 master interface is only available if the board is VME system controller.
I2C bus 0/1 master interfaces software tools are described in Fedora Release Note.

- VME I2C bus 0 slave interface

The VM6103 board SMBus 0 slave address depends on VME slot ID (slot geographical address = GA):

- VME Slot 1: slave address is 0x18 (I2C 7bits addressing)
- VME Slot 2: slave address is 0x19 (I2C 7bits addressing)
- VME Slot 3: slave address is 0x1A (I2C 7bits addressing) And so on.

Each board mapped at a unique I2C address implements 7 registers. The register to access is selected by sending a 1 byte "register offset" from 0x0 to 0x6, following the I2C address byte.

These registers can also be accessed from CPU through LPC bus at I/O address 0x872 to 0x878 (cPLD registers 0x72 to 0x78).
Only registers accessible from the I2C are describe in this documentation.

3.3.2. cPLD registers definition:

3.3.2.1. Overview

These registers can be accessed from CPU through LPC bus at I/O address 0x800+offset.

Registers 0x72 to 0x78 can also be accessed from I2C bus 0 (register offset 0 to 6) by an external I2C master.

OFFSET	NAME	ACCESS	REGISTER DESCRITPTION
0x72	I2C_BOARD_STATUS	RW	VME Registers facilities
0x73	I2C_BOARD_CONTROL	RW	VME Registers facilities
0x74	I2C_ERROR_STATUS	RW	VME Registers facilities
0x75	I2C_CHECKPOINT	RW	VME Registers facilities
0x76	I2C_FAILCODE	RW	VME Registers facilities
0x77	I2C_SCRATCHPAD	RW	VME Registers facilities
0x78	I2C_MISC	RW	VME Registers facilities

3.3.2.2. Detailed Description

- **VME backplane I2C bus registers**

I2C_BOARD_STATUS @ 0x72 Can also be accessed from I2C0 slave interface with register offset 0				
Bit#	Name	Description	Reset	Type
7	PowerStatus	Power Status 0: :Power Stand By 1: :Power ON	0	RO
6-5	Reset Source	Last Reset Source 0x00 Internal PSUs power-on 0x01 Watchdog expired 0x10 SYSRESET (from VME) 0x11 Local reset: reset switch, reset from I2C (reg 0x73), or reset by software	0	RO
4	Reset Status	Reset Status Side A 0 Reset asserted 1 Reset unasserted	0	RO
3-0	Boot Status	Boot Status 0x00: RESET: default hardware value 0x01: BIOS-BOOT: written by BIOS 0x02:BIOS: written by BIOS 0x03:PBIT: written by BIOS 0x04: OS-BOOT: written by BIOS 0x05:OS-RUNNING: to be written by OS at the end of boot 0x06:COMPLETED: to be written by the final application when running 0x07:SHUTDOWN: to be written by OS when issuing a halt/shutdown 0x08: REBOOT: to be written by OS when rebooting 0x09 - 0x0B: Reserved 0x0C - 0x0F: Customer defined These bits are Read Only through I2C Slave Interface and R/W through LPC Interface The boot status is also reset at each board reset.	0	RW

I2C_BOARD_CONTROL @ 0x73 Can also be accessed from I2C0 slave interface with register offset 1				
Bit #	Name	Description	Reset	Type
7-4	Board Id	Board Identification 1011 VM6103	0	RO
3-2	Reserved	Reserved	0	RW
1	Reset	Reset 0: No reset 1: Reset asserted	0	RW
0	Power_OnOff	Power On/Off Control 0: Power Off (StandBy) 1: Power On This bit can always be used to power on or off, and its default value is loaded when standby is applied from inverted VPD EEPROM offset 0x100 bit 1, if FACTORY mode is not enabled **WARNING** Setting this bit to 0 asserts VME SYSRESET (the board does not fully support standby because of Alma2f and its VME buffers)	*	RW

I2C_ERROR_STATUS @ 0x74 Can also be accessed from I2C0 slave interface with register offset 2				
Bit#	Name	Description	Reset	Type
7	Temp Alert	Temperature alert on sensor or CPU 0: no temperature alert 1: temperature alert pending	0	RO
6	POST_Error	POST Error 0: no error 1: error This bit is set when PBIT has been run with errors (according to reg 0x2)	0	RO
5	POST_RTC	POST RTC 0: POST OK 1: POST FAILED (weak or missing battery) This bit is a copy of reg 0x3 bit 0 (POST_RTC), that is set when RTC battery islow	0	RO
4-0	Temp Alert	Reserved	0	RW

I2C_CHECKPOINT @ 0x75 Can also be accessed from I2C0 slave interface with register offset 3				
Bit#	Name	Description	Reset	Type
7-0	Checkpoint	Last checkpoint written to cPLD register	0	RO

I2C_FAILCODE @ 0x76 Can also be accessed from I2C0 slave interface with register offset 4				
Bit#	Name	Description	Reset	Type
7-0	Reserved	Reserved for future use	0	RO

I2C_SCRATCHPAD @ 0x77 Can also be accessed from I2C0 slave interface with register offset 5				
Bit#	Name	Description	Reset	Type
7-0	Scratchpad	Scratchpad register The purpose of this register is not defined	0	RW

I2C_MISC @ 0x78 Can also be accessed from I2C0 slave interface with register offset 6				
Bit#	Name	Description	Reset	Type
7	Force_rescue_BIOS	Force rescue Firm 0=not forced (default) 1=forced	0	RW
6	Disable_OS_boot	Disable OS Boot 0=not disabled (normal boot) 1=disabled	0	RW
5-3	Power_CUR	Current power profile This field is updated by the board (Firm/OS) according to its current power profile 000: power profile unsupported other value: see below	000	RO
2-0	Power_REQ	Requested power profile This filed is expected to be set by a shelf-manager (such as CMB) or another board, and used by the board (Firm/OS) to set its power profile. 000: uncontrolled : the board uses its onboard switches and/or Firm settings to set a power profile Other: reserved	000	RW

3.4. Lines EIA-422/485 Additional Modes

The VM6103 features up to 4 serial lines in EIA-232 mode and up to 2 serial lines in EIA-422/485.

EIA-232 serial lines mode are available on front panel RJ12 and P2 connectors.

See section 4.1.1 page 56 - “Serial Connector - COM” and section 4.3.3 page 78 - “P2 Connector” for more information on pin assignments.

EIA-232 serial lines mode is the default mode, but EIA-422/485 mode can also be set for COM1 and COM2 only with the following pin assignment:

MODE	RJ-12 FRONT PANEL CONNECTOR	P2 REAR CONNECTOR	RJ-12 FRONT PIN ASSIGNMENT	P2 REAR PIN ASSIGNMENT
EIA-232 (default)	EIA-232: COM1, COM3	EIA-232: COM1, COM2, COM3, COM4	COM1 TXD: pin 3 COM1 RXD: pin 4 COM3 TXD: pin 1 COM3 RXD: pin 6	COM1 TXD: pin D-22 COM1 RXD: pin D-23 COM2 TXD: pin Z-23 COM2 RXD: pin Z-25 COM3 TXD: pin D-24 COM3 RXD: pin D-25 COM4 TXD: pin Z-27 COM4 RXD: pin Z-29
EIA-232 with handshaking(1)	EIA-232: COM1	EIA-232: COM1, COM2	COM1 TXD: pin 3 COM1 RXD: pin 4 COM1 RTS: pin 1 COM1 CTS: pin 6	COM1 TXD: pin D-22 COM1 RXD: pin D-23 COM1 RTS: pin D-24 COM1 CTS: pin D-25 COM2 TXD: pin Z-23 COM2 RXD: pin Z-25 COM2 RTS: pin Z-27 COM2 CTS: pin Z-29
EIA-422/485	EIA-422/485: COM1	EIA-422/485: COM1, COM2	COM1 TXD-: pin 3 COM1 TXD+: pin 1 COM1 RXD-: pin 4 COM1 RXD+: pin 6	COM1 TXD+: pin D-24 COM1 TXD-: pin D-22 COM1 RXD:+ pin D-25 COM1 RXD-: pin D-23 COM2 TXD+: pin Z-27 COM2 TXD-: pin Z-23 COM2 RXD+: pin Z-29 COM2 RXD-: pin Z-25

(1) This mode requires to modify RCW and to reset the Firmware to be taken into account.

3.5. GPIOs

There are up to 8 GPIOs on VM6103 board and they are managed by CPLD. Refer to Yocto Linux Release Notes for further details.

- 3 GPIOs are available on P0 connector, GPIO [1-3] (option)
- 3 GPIOs are available on P2 connector, GPIO [4-6]
- 2 GPIOs are available on P2 connector on customer request, GPIO [7-8], these both GPIOs take PMC1 IO [63-64]’s place
- LVCMOS33 (0 - 3V3)
- Drive strength is 4 mA; can sink or source up to 4 mA simultaneously on all GPIOs.
- Clamping diode, but NOT 5V tolerant. So any voltage above 3.3V must be scaled by a voltage divider or limiter before being applied to a GPIO. Maximum voltage is 3.6V. Absolute maximum voltage is 3.75V (value not suitable for continuous operation).

No clamping diode for GPIO7 and GPIO8.

- Weak pull-up (to 3V3SB board's internal standby power): 47K.
  This pull-up is to prevent GPIOs from floating if left unconnected. It is not configurable, but can be overridden by an additional stronger pull-down if a pull-down is required instead.
- Hysteresis: 250 mV

GPIOs are NOT 5V tolerant. Absolute maximum voltage on GPIOs is 3.75V (value not suitable for continuous operation). So any voltage above 3.6V must be reduced using a bridge made of two resistors before being applied to a GPIO.

3.6. Security Features

The VM6103 provides digital security features with hardware enforced root of trust (secure elements). The VM6103 supports SEC-Line computer security offering, APPROTECT:

- APPROTECT:Application integrity, confidentiality, only authorized copies

If required customers can customize the solution to meet specific needs. For more information contact Kontron Technical Support.

The APPROTECT solution, using a security technology from Wibu, a Kontron partner, protects the application from the main security threats with the security of a dedicated hardware secure element located on the VM6103 board.

The main security threats at the application level are:

- Integrity: the running application might be hacked or patched in binary, on the disk or in memory, to modify its behavior or work around some checks.
- Confidentiality: the way the application code is working could be analyzed in details by looking at the execution code, in order to learn or to reproduce its behavior.
- Unauthorized copies: the embedded systems (software application or full equipment) suffer the risk of being cloned without authorization.

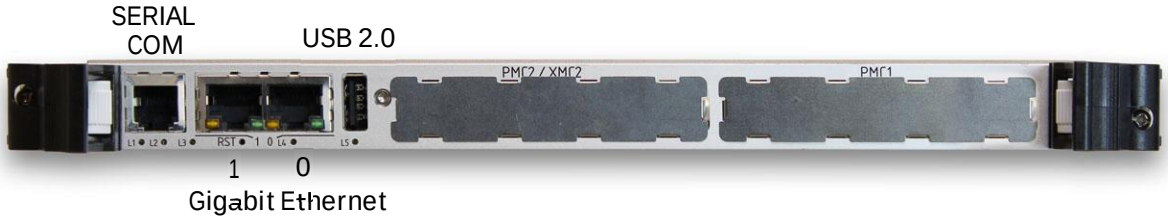
Technical information:

- Security Hardware: Infineon SLM-97CUSIFX1M00 smart card chip
- Encryptions standards: 128 bit AES, SHA-256, 2048 bit RSA, 224 bit ECC

4 / Physical I/Os

4.1. Front Panel Connectors

Figure 17: Location of the Front Panel Connectors



4.1.1. Serial Connector - COM

The VM6103 integrates up to four serial communications ports, COM1 to COM4 in PC parlance.

COM1 to COM4 are available on rear via the P2 connector. COM1 and COM3 are also available via the front panel connector.

- COM1: EIA-232/485 port on RJ-12 front panel connector or on the rear P2 connector
- COM2: EIA-232/485 port on the rear P2 connector
- COM3: EIA-232 port on RJ-12 front panel connector or on the rear P2 connector
- COM4: EIA-232 port on the rear P2 connector

COM1 and COM2 serial ports are configurable via Firmware commands and CPLD as EIA-232 or EIA-422 or EIA-485. Each port operates in full duplex mode or in half duplex mode. Fast slew rate is the default mode in EIA-485 mode.

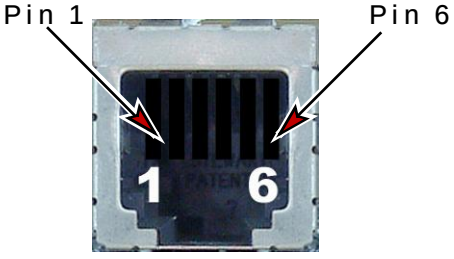
The signaling level of EIA-485 is compatible with EIA-422, so full duplex EIA-485 may also be used for point-to-point communications with an EIA-422 serial port. When port is operating in EIA-485 mode software may configure the termination for V.35, V11 or unterminated using CPLD.

In EIA-232 mode the port is always unterminated register.

Table 14: Serial Connector Pin Assignment

PIN	SIGNAL
1	TXD3 / RTS / TXD1+
2	Shell
3	TXD1/TXD1-
4	RXD1/RXD1-
5	GND
6	RXD3 / CTS / RXD1+

Figure 18: Serial Connector



A serial line should only be used via one connector at the same time, either the Serial front panel connector or the P2 connector.

Table 15: Serial Connector Signal Description

signal	DESCRIPTION
RXD3 / CTS / RXD1+	COM3 EIA-232 Receive Data / COM1 EIA-232 Clear-To-Send / COM1 EIA-485 Receive Data
TXD3 / RTS / TXD1+	COM3 EIA-232 Transmit Data / COM1 EIA-232 Ready-To-Send / COM1 EIA-485 Transmit Data
RXD1/RXD1	COM1 EIA-232Receive Data / COM1 EIA-485 Receive Data
TXD1/TXD1-	COM1 EIA-232 Transmit Data / COM1 EIA-485 Transmit Data
GND	Ground
Shell	Chassis Ground

Serial Cable Designation

Serial cable is:

- RJ-14 (6 pin, 4 conductor) for a simple EIA-232 without handshake support.
- RJ-12 (6 pin, 6 conductor) for EIA-232 with handshaking.

A RJ-12 to DB9/DB25 male or DB9/DB25 female adapter is available from multiple sources, such as:

- Kontron Order Code KIT-RJ12DB9
- Triangle Cable https://www.trianglecables.com/

Table 16: Connectors Pin Assignment

PIN CONNECTOR DB9	SIGNAL	PIN CONNECTOR RJ-12
1	N.C.	1
2	TXD	3
3	RXD	4
4	N.C.	6
5	GND	5

Rj-12 Cable

DB9 Female Adapter

4.1.2. Gigabit Ethernet Connectors

The Ethernet transmission should operate using a CAT5e cable with a maximum length of 50 m.

The Ethernet connectors are available as RJ-45 connectors with tab down. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

Table 17: Gigabit Ethernet Connectors Pin Assignment

PIN	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-		I/O	BI_DC+
5	-	-	-		I/O	BI_DC-
6	I	RX-	I	RX-	I/O	BI_DB-
7	-	-	-		I/O	BI_DD+
8	-	-	-		I/O	BI_DD-
Shell	Chassis Ground					

Figure 19: Ethernet Connector

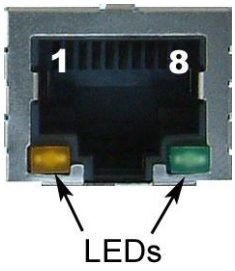


Table 18: Ethernet LEDs Status Definition

STATUS		SPEED LED YELLOW	ACT LED GREEN
Ethernet Link is not established		OFF	OFF
10 Mbps	Ethernet Link Established	OFF	ON
	Ethernet Link Activity	OFF	BLINK
100 Mbps	Ethernet Link Established	OFF	ON
	Ethernet Link Activity	OFF	BLINK
1000 Mbps	Ethernet Link Established	ON	ON
	Ethernet Link Activity	ON	BLINK

- **ACT (green)**

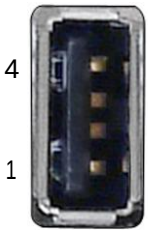
This LED monitors network connection and activity. The LED lights up when a valid link (cable connection) has been established. The LED goes temporarily off if network packets are being sent or received through the RJ-45 port. When this LED remains off, a valid link has not been established due to a missing or a faulty cable connection.

4.1.3. USB Connector

Table 19: USB Connector Pin Assignment

Pin	Signal	Function	I/O
1	VCC (+5V Protected)	VCC	--
2	USB_D-	Differential USB-	I/O
3	USB_D+	Differential USB+	I/O
4	GND	GND	--

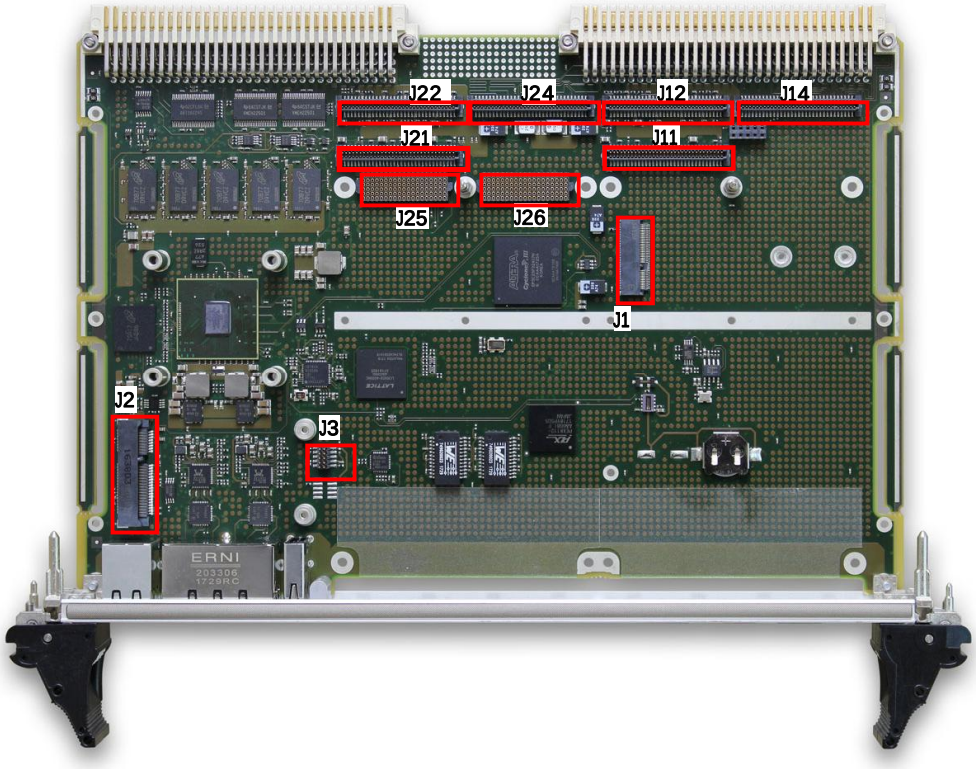
Figure 20: USB Connector



USB

4.2. Onboard Connectors

Figure 21: Onboard Connector (Top Side)



4.2.1. M2 Module Socket

The M.2 socket (J1 connector) is used to connect a M.2 module, key M for SATA SSD storage only. The M.2 socket supports only 2242 and 2260 form factors. This M.2 slot is compliant with S1, S2, S3, D3, D4 type module component heights per defined in PCIe M.2 Specification allowing simultaneous insertion of a M.2 card and a PMC/XMC card.

The following figure and table provide pinout information for the M.2 key M connector:

Table 20: M.2 Module Socket Pin Assignment

PIN	SIGNAL	SIGNAL	PIN
		GND	75
74	3.3V	GND	73
72	3.3V	GND	71
70	3.3V	PEDET	69
68	SUSCLK (32 kHz)	N.C.	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N.C.	GND	57
56	N.C.	N.C.	55
54	N.C.	N.C.	53
52	N.C.	GND	51
50	N.C.	SATA-A+	49
48	N.C.	SATA-A-	47
46	N.C.	GND	45
44	N.C.	SATA-B-	43
42	N.C.	SATA-B+	41
40	N.C.	GND	39
38	DEVSLP	N.C.	37
36	N.C.	N.C.	35
34	N.C.	GND	33
32	N.C.	N.C.	31
30	N.C.	N.C.	29
28	N.C.	GND	27
26	N.C.	N.C.	25
24	N.C.	N.C.	23
22	N.C.	GND	21
20	N.C.	N.C.	19
18	3.3V	N.C.	17
16	3.3V	GND	15
14	3.3V	N.C.	13
12	3.3V	N.C.	11
10	N.C.	GND	9
8	N.C.	N.C.	7
6	N.C.	N.C.	5
4	3.3V	GND	3
2	3.3V	GND	1

Figure 22: M.2 Socket 3 (M, H3.2)

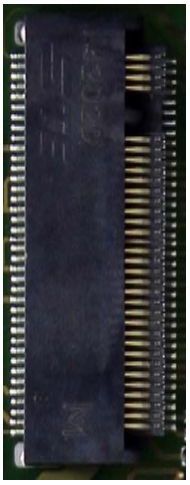


Table 21: M.2 Module Socket Signal Description

SIGNAL SATA	DIRECTION	DEFINITION
3.3V	Output	+3.3V power supply.
GND	-	Logic ground.
SUSCLK	Output	Suspend Clock for low power mode handling per PCI Express M.2 specification. Not used on VM6103.
N.C.	-	Not Connected on VM6103
DEVSLP	Output	DEVSLP (Device Sleep) per SATA 3.2 indicates the module that it must enter a very low power mode (including transceiver circuitry). Not used on VM6103.
PEDET	Input	PEDET (PCI Express Detect) per PCI Express M.2 specification is driven low by SATA modules and high-Z by PCI Express modules (seen as a logic 1 due to on-board pull-up resistor). On VM6103, this signal is not used.
SATA-A+/-	Output	Transmit differential pair per SATA 3.2.
SATA-B+/-	Output	Receive differential pair per SATA 3.2.

For other aspects such as performance/wear leveling/lifetime, that depend heavily on the mission profile, FLASH users are encouraged to use application specific means to verify that the storage device meets the application needs along its life time or use device unique ID and low level health data information or mechanism (such as SMART) to monitor their installed base. Kontron can also offer specific 'frozen BOM" services for customers willing to guarantee their installed base homogeneity across deliveries and time.

4.2.2. MiniPCIe Connector

The VM6103 supports mini-PCI Express module F1 and F2 full size type as defined per PCIE Express card Electromechanical Specification through on board J2 connector. This socket offers PCIe x1 Gen2 interface by default and USB2.0 interface depending on build option.

The following figure and table provide pinout information for the MiniPCIe connector:

Table 22: MiniPCIe Socket Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
51	N.C.	52	+3.3Vaux
49	N.C.	50	GND
47	N.C.	48	+1.5V
45	N.C.	46	N.C.
43	GND	44	N.C.
41	+3.3Vaux	42	N.C.
39	+3.3Vaux	40	GND
37	GND	38	USB_D+
35	GND	36	USB_D-
33	PETp0	34	GND
31	PETn0	32	SMB_DATA
29	GND	30	SMB_CLK
27	GND	28	+1.5V
25	PERp0	26	GND
23	PERn0	24	+3.3Vaux
21	GND	22	PERST#
19	N.C.	20	N.C.
17	N.C.	18	GND
Mechanical Key			
15	GND	16	N.C.
13	REFCLK+	14	N.C.
11	REFCLK-	12	N.C.
9	GND	10	N.C.
7	CLKREQ#	8	N.C.
5	N.C.	6	1.5V
3	N.C.	4	GND
1	WAKE#	2	+3.3Vaux

Figure 23: MiniPCIe Socket (H3.2)

Table 23: MiniPCIe Connector Socket Signal Description

SIGNAL SATA	DIRECTION	DEFINITION
+1.5V	Ouput	+1.5V power supply.
+3.3Vaux	Ouput	+3.3V auxiliary voltage source. Connected to +3.3V internal voltage on VM6103.
GND	-	Ground
N.C.	-	Not Connected or not used pin.
USB_D+/-	I/O	Differential USB 2.0
PETp0 / PETn0	Ouput	High-speed Differential transmit PCIe pair
PERp0 / PERn0	Input	High-speed Differential receive PCIe pair
SMB_DATA	I/O	b SMBus data for optional management feature. Not used on VM6103.
SMB_CLK	Output	SMBus clock for optional management feature. Not used on VM6103.
PERST#	Output	PCI Express PERST# per PCI Express Card Electromechanical Specification. On VM6103 handled by CPLD.
REFCLK+/-	Output	PCIe differential reference clock (100 MHz) per PCI Express Card Electromechanical Specification.
CLKREQ#	Input	Open drain CLKREQ# signal per PCI Express Card Electromechanical Specification. Driven by miniPCIe module to request the platform to activate the PCI Express clock.
WAKE#	Input	Open drain WAKE# signal per PCI Express Card Electromechanical Specification. Driven by miniPCIe module to allow the platform to reactivate the link main power rails and reference clock. On VM6103, this signal is wire-ORed with WAKE# signal from XMC connector. It is connected to CPLD

4.2.3. PMC Connectors

4.2.3.1. PMC J11 and J21 Connector Pin Assignments

Table 24: PMC J11 and J21 Conne4ctor Pin Assignment

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	TCK	17	REQ#	33	FRAME#	49	AD[09]
2	-12V	18	+5V	34	GND	50	+5V
3	GND	19	V(I/0) (1)	35	GND	51	GND
4	INTA#	20	AD[31]	36	IRDY#	52	C/BE0#
5	INTB#	21	AD[28]	37	DEVSEL#	53	AD[06]
6	INTC#	22	AD[27]	38	.+5V	54	AD[05]
7	BUSMODE1#	23	AD[25]	39	PCIXCAP	55	AD[04]
8	+5V	24	GND	40	LOCK#	56	GND
9	INTD#	25	GND	41	SDONE#	57	V(I/O) (1)
10	N.C.	26	C/BE3#	42	SBO#	58	AD[03]
11	GND	27	AD[22]	43	PAR	59	AD[02]
12	+3.3V_SUS	28	AD[21]	44	GND	60	AD[01]
13	CLK	29	AD[19]	45	V(I/O) (1)	61	AD[00]
14	GND	30	+5V	46	AD[15]	62	+5V
15	GND	31	V(I/0) (1)	47	AD[12]	63	GND
16	GNT#	32	AD[17]	48	AD[11]	64	REQ64#

(1) V(I/O) is 3.3V only.
PCI signals active when low.

4.2.3.2. PMC J12 and J22 Connector Pin Assignments

Table 25: PMC J12 and J22 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	+12V	17	PME#	33	GND	49	AD[08]
2	TRST	18	GND	34	IDSEL B (1)	50	+3.3V
3	TMS	19	AD[30]	35	TRDY#	51	AD[07]
4	TDO	20	AD[29]	36	+3.3V	52	REQ B# (1)
5	TDI	21	GND	37	GND	53	+3.3V
6	GND	22	AD[26]	38	STOP#	54	GNT B# (1)
7	GND	23	AD[24]	39	PERR#	55	PMC-RSVD
8	N.C.	24	+3.3V	40	GND	56	GND
9	N.C.	25	IDSEL	41	+3.3V	57	PMC-RSVD
10	N.C.	26	AD[23]	42	SERR#	58	EREADY
11	BUSMODE2#	27	+3.3V	43	C/BE1#	59	GND
12	+3.3V	28	AD[20]	44	GND	60	N.C.
13	RST#	29	AD[18]	45	AD[14]	61	ACK64#
14	GND	30	GND	46	AD[13]	62	+3.3V
15	+3.3V	31	AD[16]	47	M66EN	63	GND
16	BUSMODE4#	32	C/BE2#	48	AD[10]	64	N.C.

(1) IDSEL B, REQ B# and GNT B# are provided for use by dual-function PMC modules or processor-PMC modules
PCI signals active when low.

4.2.3.3. J14 and J24 Connector Pin Assignment

Table 26: J24 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	PMC IO 01	17	PMC IO 17	33	PMC IO 31	49	PMC IO 49
2	PMC IO 02	18	PMC IO 18	34	PMC IO 34	50	PMC IO 50
3	PMC IO 03	19	PMC IO 19	35	PMC IO 35	51	PMC IO 51
4	PMC IO 04	20	PMC IO 20	36	PMC IO 36	52	PMC IO 52
5	PMC IO 05	21	PMC IO 21	37	PMC IO 37	53	PMC IO 53
6	PMC IO 06	22	PMC IO 22	38	PMC IO 38	54	PMC IO 54
7	PMC IO 07	23	PMC IO 23	39	PMC IO 39	55	PMC IO 55
8	PMC IO 08	24	PMC IO 24	40	PMC IO 40	56	PMC IO 56
9	PMC IO 09	25	PMC IO 25	41	PMC IO 41	57	PMC IO 57
10	PMC IO 10	26	PMC IO 26	42	PMC IO 42	58	PMC IO 58
11	PMC IO 11	27	PMC IO 27	43	PMC IO 43	59	PMC IO 59
12	PMC IO 12	28	PMC IO 28	44	PMC IO 44	60	PMC IO 60
13	PMC IO 13	29	PMC IO 29	45	PMC IO 45	61	PMC IO 61
14	PMC IO 14	30	PMC IO 30	46	PMC IO 46	62	PMC IO 62
15	PMC IO 15	31	PMC IO 31	47	PMC IO 47	63	PMC IO 63
16	PMC IO 16	32	PMC IO 32	48	PMC IO 48	64	PMC IO 64

4.2.3.4. PMC Signal Description

Table 27: PMC Signal Description

MNEMONIC	SIGNAL DESCRIPTION
AD[00] to AD[63]	Address/Data bits. Multiplexed address and data bus. AD32 to AD63 are specifics to 64-bit bus extension.
ACK64#	Acknowledge 64-bit Transfer. Driven low by the device to indicate that the target is willing to transfer data using 64 bits.
BUSMODE1#	Bus Mode 1. Driven low by a PMC module to indicate that it supports the current bus mode
BUSMODE2#	Bus Mode 2. Driven low by a PMC module to indicate that it supports the current bus mode
BUSMODE4#	Bus Mode 4. Driven low by a PMC module to indicate that it supports the current bus mode
C/BE0# to C/BE7#	Command/Byte Enables. During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase the signals are byte enables that specify the active bytes on the bus. C/BE4# to C/BE7# are specifics to 64-bit bus extension.
CLK	Clock. Except RST*, the 64-bit PCI bus signals are synchronous to 33 or 66 MHz clock.
DEVSEL#	Device Select. Driven low by a PCI agent to signal that it has decoded its address as the target of the current access.
FRAME#	FRAME. Driven low by the current master to signal the start and duration of an access.
EREADY	EREADY. Output of non-monarch PPMCs that indicates it has completed its onboard initialization and can respond to PCI bus enumeration by the monarch via configuration cycles. Input to the monarch PPMC that indicates all non-monarch PPMCs have completed their onboard initialization and can respond to PCI bus enumeration by the monarch via configuration cycles.
GNT#	Grant. Driven low by the arbiter to grant PCI bus ownership to a PCI agent.
GNT B#	Grant. GNT B# is provided for use by dual-function PMC modules or processor-PMC modules.

MNEMONIC	SIGNAL DESCRIPTION
IDSEL	Initialization Device Select. Device chip select during configuration cycles.
IDSEL B#	Initialization Device Select. IDSEL B is provided for use by dual-function PMC modules or processor-PMC modules.
INTA# to INTD#	Interrupt lines. Level-sensitive, active-low interrupt requests.
IRDY#	Initiator Ready. Driven low by the initiator to signal its ability to complete the current data phase.
LOCK#	LOCK. Driven low to indicate an atomic operation that may require multiple transactions to complete.
M66EN	66 MHZ Enable. Indicates to a device if the bus segment is operating at 66 or 33 MHz. If it is high then the bus speed is 66 MHz and if it is low then the bus speed is 33 MHz.
N.C.	This pin is not connected.
PAR	Parity. Parity protection bit for AD0 to AD31 and C/BE0# to C/BE3#.
PAR64	Parity Upper DWORD. Parity protection bit for AD32 to AD63 and C/BE4# to C/BE7#.
PERR#	Parity Error. Driven low by a PCI agent to signal a parity error.
PMC IO 01 to PMC IO 64	64-bit PCI bus PMC 64 signals. Used to transmit I/O signals from PCI 64 PMC connector (J14) to P2 connector.
PMC-RSVD	Reserved. Do not connect this pin.
PME	
REQ#	Request. Driven low by a PCI agent to request ownership of the PCI bus.
REQ B#	Request. REQ B# is provided for use by dual-function PMC modules or processor-PMC modules.
REQ64#	Request 64-bit Transfer. Driven low by the current bus master, indicates that it desires to transfer data using 64 bits.
RST#	Reset. Driven low to reset the PCI bus.
SBO#	Snoop Backoff. Indicates a hit of a modified line asserted.
SDONE#	Snoop Done. Indicates the status of the snoop for the current access.
SERR#	System Error. Driven low by a PCI agent to signal a system error.
STOP#	STOP. Driven low by a PCI target to signal a disconnect or target-abort.
TCK	JTAG Clock.
TDI	JTAG Data In
TDO	JTAG Data Out
TMS	JTAG Mode Select
TRDY#	Target Ready. Driven low by the current target to signal its ability to complete the current data phase.
TRST	JTAG Reset.
V(I/O)	Power supply delivered by the board. On the PCI 64 PMC slots, +3.3 Volts power is supplied. +5 Volts signaling PMCs are not supported. Contact Kontron for more information.
+3.3V	+3.3 Volts DC power
+5V	+5 Volts DC power
+12V	+12 Volts DC power
-12V	-12 Volts DC power

4.2.4. XMC Connectors

4.2.4.1. XMC J25 Connector Pin Assignments

One XMC sites is provided to allow the installation of VITA 42.3, PCI-Express mezzanine cards. The signals assignments are as shown in the following table. The encoding for GA[2:0] should not conflict with other SMbus/IPMI devices.

Table 28: XMC J25 Connector Pin Assignment

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	PET0p0	PET0n0	3.3V	N.C.	N.C.	VPWR (1)
2	GND	GND	TRST#	GND	GND	MRSTI#
3	N.C.	N.C.	3.3V	N.C.	N.C.	VPWR (1)
4	GND	GND	TCK	GND	GND	N.C.
5	N.C.	N.C.	3.3V	N.C.	N.C.	VPWR (1)
6	GND	GND	TMS	GND	GND	+12V
7	N.C.	N.C.	3.3V	N.C.	N.C.	VPWR (1)
8	GND	GND	TDI	GND	GND	-12V
9	RFU	RFU	N.C.	RFU	RFU	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	PER0p0	PER0n0	N.C.	N.C.	N.C.	VPWR (1)
12	GND	GND	GA1	GND	GND	MPRESENT#
13	N.C.	N.C.	3.3V AUX	N.C.	N.C.	VPWR (1)
14	GND	GND	GA2	GND	GND	MSDA
15	N.C.	N.C.	N.C.	N.C.	N.C.	VPWR (1)
16	GND	GND	NVMRO	GND	GND	MSCL
17	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
18	GND	GND	N.C.	GND	GND	N.C.
19	REFCLK+0	REFCLK-0	N.C.	N.C.	N.C.	N.C.

(1) VPWR is connected to +5V via a fuse.
The 12V option is available, please contact Kontron for more information on this topic.

Signals active when low.

4.2.4.2. XMC J26 Connector Pin Assignment

Table 29: XMC J26 Connector Pin Assignment

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	XMCIO_DP_P<1>	XMCIO_DP_N<1>	XMCIO_S<1>	XMCIO_DP_P<2>	XMCIO_DP_N<2>	XMCIO_S<2>
2	GND	GND	N.C.	GND	GND	N.C.
3	XMCIO_DP_P<3>	XMCIO_DP_N<3>	XMCIO_S<3>	XMCIO_DP_P<4>	XMCIO_DP_N<4>	XMCIO_S<4>
4	GND	GND	N.C.	GND	GND	N.C.
5	N.C.	N.C.	XMCIO_S<5>	N.C.	N.C.	XMCIO_S<6>
6	GND	GND	N.C.	GND	GND	N.C.
7	N.C.	N.C.	XMCIO_S<7>	N.C.	N.C.	XMCIO_S<8>
8	GND	GND	N.C.	GND	GND	N.C.
9	N.C.	N.C.	XMCIO_S<9>	N.C.	N.C.	XMCIO_S<10>
10	GND	GND	N.C.	GND	GND	N.C.
11	XMCIO_DP_P<11>	XMCIO_DP_N<11>	XMCIO_S<11>	XMCIO_DP_P<12>	XMCIO_DP_N<12>	XMCIO_S<12>
12	GND	GND	N.C.	GND	GND	N.C.
13	XMCIO_DP_P<13>	XMCIO_DP_N<13>	XMCIO_S<13>	XMCIO_DP_P<14>	XMCIO_DP_N<14>	XMCIO_S<14>
14	GND	GND	N.C.	GND	GND	N.C.
15	N.C.	N.C.	XMCIO_S<15>	N.C.	N.C.	XMCIO_S<16>
16	GND	GND	N.C.	GND	GND	N.C.
17	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
18	GND	GND	N.C.	GND	GND	N.C.
19	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.

Refer to Table 33 page 72 for the mapping of XMC J26 connector or P0 rear connector.

4.2.4.3. XMC Signal Description

Table 30: XMC Signal Description

MNEMONIC	SIGNAL DESCRIPTION
GA[0..2]	I2C channel select. These signals allow a carrier to address a specific XMC slot on an IPMI I2C bus shared by multiple XMCs.
GND	Ground
MPRESENT	Module present. This signal allows the carrier to determine whether an XMC is present.
MRSTI	XMC Reset In. When this signal is asserted low by the carrier, the mezzanine card shall initialize itself into a known state.
MSCL	IPMI I2C serial clock.
MSDA	IPMI I2C serial data.
NVMRO	XMC Write Prohibit. When this signal is asserted high, the XMC shall disable writes to non-volatile memory on the XMC.
N.C.	Not Connected. Do not Used
PET0p/n[0..7]	Link 0 Differential Transmit. These signals are used by the XMC to receive high-speed protocol-specific data TO the carrier over the PCI Express interface.
PER0p/n[0..7]	Link 0 Differential Receive. These signals are used by the XMC to receive high-speed protocol-specific data FROM the carrier over the PCI Express interface.
REFCLK+/-0	Differential reference clock for Link 0 PCI Express interface.
RFU	Reserved for Future Use
TCK	JTAG Clock.
TDI	JTAG Data In
TDO	JTAG Data Out
TMS	JTAG Mode Select
TRST	JTAG Reset.
VPWR	Power pins. These signals carry either 12V or 5V power from the carrier to the XMC. 5V by default
3.3V	
3.3V AUX	
+/-12V	
XMCIO_DP_P/N [1...13]	XMC differential pair. Used to transmitt differential pair IO signals from secondary XMC connector (J26) to P0 connector
XMCIO_S [1...16]	XMC single ended IO. Used to transmitt single ended IO signals from secondary XMC connector (J26) to P0 connector

4.2.5. Cortex Debug Connector

The VM6103 implements legacy 10-pin Cortex-M Debug connector. This connector supports JTAG debug for QorIQ processor by enabling the connection of CodeWarrior TAP target system debugging tool. The CodeWarrior TAP allows you to debug and control of the QorIQ processor using the CodeWarrior IDE.

For further information about CodeWarrior TAP, visit NXP web site: https://www.nxp.com

Table 31: Cortex Debug connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
9	GND Detect	10	RESET#
7	N.C.	8	TDI
5	GND	6	TDO
3	GND	4	TCK
1	1.8V	2	TMS

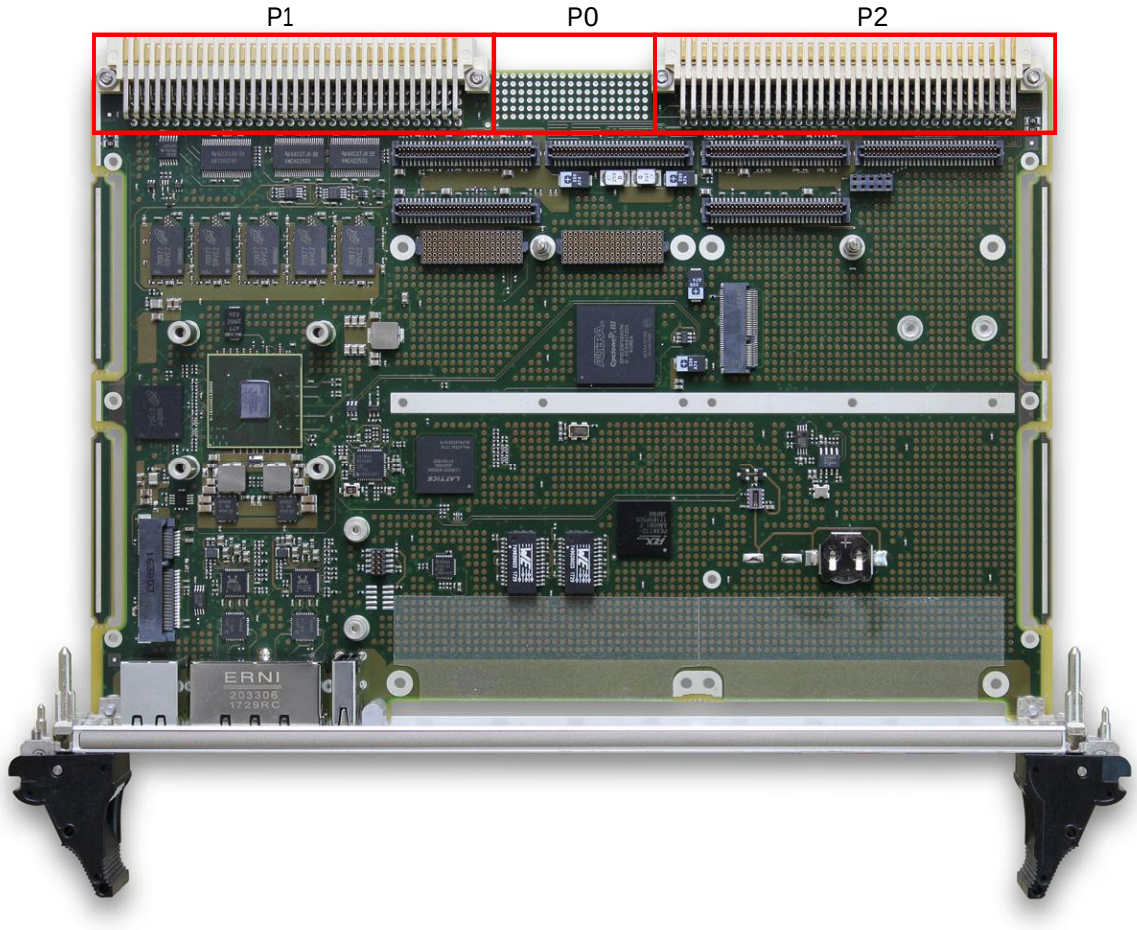
Figure 24: Cortex Debug Connector

Table 32: Cortex Debug connector Signal Description

SIGNAL SATA	DIRECTION	DEFINITION
1.8V	Ouput	+1.8V power supply.
GND	-	Logic Ground
TDI	Input	JTAG TDI for QorIQ processor
TDO	Output	JTAG TDO for QorIQ processor
TCK	Input	JTAG TCK for QorIQ processor
TMS	Input	JTAG TMS for QorIQ processor
GND Detect	Input	GNDDetect is an optional board feature. Not used on VM6103.
RESET#	Input	Processor reset from CodeWarrior TAP.

4.3. Rear Connectors

Figure 25: VME Connectors



4.3.1. P0 Connector

4.3.1.1. P0 connector Pin Assignment

Table 33: P0 Connector Pin Assignment

PIN #	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F[2]
1	PMC2 IO 39 or XMC2 IO S9[1]	PMC2 IO 38 or XMC2 IO S8[1]	PMC2 IO 37 or XMC IO S7[1]	PMC2 IO 36 or XMC2 IO S6[1]	PMC2 IO 35 or XMC2 IO S5[1]	GND
2	ETH0_DA+	ETH0_DA–	GND	ETH0_DC+	ETH0_DC–	GND
3	ETH0_DB+	ETH0_DB–	GND	ETH0_DD+	ETH0_DD–	GND
4	ETH1_DA+	ETH1_DA–	GND	ETH1_DC+	ETH1_DC–	GND
5	ETH1_DB+	ETH1_DB–	GND	ETH1_DD+	ETH1_DD–	GND
6	RESET#	USB3_PWR	NVMRO[3] or PWR-DOWN	RTC_BAT	USB2_PWR	GND
7	USB3_DA+	USB3_DA-	GND	USB2_DA+	USB2_DA-	GND
8	N.C. or SATA0_TX+[5]	N.C. or SATA0_TX-[5]	GND	N.C. or SATA0_RX+[5]	N.C. or SATA0_RX–[5]	GND
9	N.C.	N.C.	GND	N.C.	N.C.	GND
10	PMC2 IO 34 or XMC2 IO S4[1]	PMC2 IO 33 or XMC2 IO S2[1]	GPIO1 [1]	GPIO2 [1]	GPIO3 [1]	GND
11	PMC2 IO 58 or XMC2 IO DP1+	PMC2 IO 60 or XMC2 IO DP1-	PMC2 IO 46 or XMC2 IO S1 or GND[4]	PMC2 IO 48 or XMC2 IO DP11+	PMC2 IO 50 or XMC2 IO DP11-	GND
12	PMC2 IO 62 or XMC2 IO DP2+	PMC2 IO 64 or XMC2 IO DP2-	PMC2 IO 45 or XMC2 IO S3 or GND[4]	PMC2 IO 52 or XMC2 IO DP12+	PMC2 IO 54 or XMC2 IO DP12-	GND
13	PMC2 IO 61 or XMC2 IO DP3+	PMC2 IO 63 or XMC2 IO DP3-	PMC2 IO 56 or XMC IO S11 or GND[4]	PMC2 IO 51 or XMC2 IO DP13+	PMC2 IO 53 or XMC2 IO DP13-	GND
14	PMC2 IO 57 or XMC2 IO DP4+	PMC2 IO 59 or XMC2 IO DP4-	PMC2 IO 55 or XMC2 IO S13 or GND[4]	PMC2 IO 47 or XMC2 IO DP14+	PMC2 IO 49 or XMC2 IO DP14-	GND
15	N.C.	N.C.	GND	N.C.	N.C.	GND
16	N.C.	N.C.	GND	N.C.	N.C.	GND
17	N.C.	N.C.	GND	N.C.	N.C.	GND
18	N.C.	N.C.	GND	N.C.	N.C.	GND
19	PMC2 IO 44 or XMC2 IO S16 [1]	PMC2 IO 43 or XMC2 IO S15 [1]	PMC2 IO 42 or XMC2 IO S14 [1]	PMC2 IO 41 or XMC2 IO S12 [1]	PMC2 IO 40 or XMC2 IO S10 [1]	GND

(1) In the column 1, 10 and 19, they may be signals or Not Connected (N.C.). The default is the signals listed. The N.C. option is made available by removing three, 0-ohm resistor packs. Please contact Kontron for more information on this topic.

(2) The F row is the metal shielded on the outside P0 connector.

(3) The default is NVMRO signal. This signal has a pull down of 2K7 Ohms on the board. This signal is active high.

(4) It is possible to have this pin connected to GND. Please contact Kontron to have this pin connected to GND.

(5) The default setting is N.C. when P0 connector is present. SATA port 0 is set on M.2 on-board module for standard VM6103 all classes.

NVMRO on P0 is 3V3 signaling, this signal is not 5V tolerant.

4.3.1.2. P0 Connector Signal Description

Table 34: P0 Connector Signal Description

MNEMONIC	SIGNAL DESCRIPTION
ETHx BI_DA+/-	Ethernet x: First pair of Transmit/Receive data.
ETHx BI_DB+/-	Ethernet x: Second pair of Transmit/Receive data.
ETHx BI_DC+/-	Ethernet x: Third pair of Transmit/Receive data.
ETHx BI_DD+/-	Ethernet x: Fourth pair of Transmit/Receive data.
GND	Ground
GPIOx	General Purpose I/O x
NVMRO	Non Volatile Memory Read Only signal
PMC2 IO yy	PMC Site #2 I/0 signal yy
PWR-DOWN	Power Down board signal
RESET	Board Reset Signal
RTC-BAT	External Battery source for RTC
SATA0 RX+/RX- TX+/TX-	Serial ATA 0 Receive +/- Transmit +/-
USB2 DA+/- USB3 DA+/-	Differential Data Pair of USB Line x
USBx PWR	+5VDC USB power Line x
XMC2 IO yy	XMC Site #2 differential and single IO Signal yy

4.3.2. P1 Connector

4.3.2.1. P1 and P2 Row B (VMEbus) Connector Pin Assignment

Table 35: P1 and P2 (Row B) Connector Pin Assignment

PIN	P1					P2
	ROW Z	ROW A	ROW B	ROW C	ROW D	ROW B
1	N.C.	D00	BBSY*	D08	+5V	+5V
2	GND	D01	BCLR*	D09	GND	GND
3	N.C.	D02	ACFAIL*	D10	N.C.	RETRY*
4	GND	D03	BG0IN*	D11	N.C.	A24
5	N.C.	D04	BG0OUT*	D12	N.C.	A25
6	GND	D05	BG1IN*	D13	N.C.	A26
7	N.C.	D06	BG1OUT*	D14	N.C.	A27
8	GND	D07	BG2IN*	D15	N.C.	A28
9	N.C.	GND	BG2OUT*	GND	GAP* (1)	A29
10	GND	SYSCLK	BG3IN*	SYSFAIL*	GA0* (1)	A30
11	N.C.	GND	BG3OUT*	BERR*	GA1* (1)	A31
12	GND	DS1*	BR0*	SYSRESET*	+3.3V	GND
13	N.C.	DS0*	BR1*	LWORD*	GA2* (1)	+5V
14	GND	WRITE*	BR2*	AM5	+3.3V	D16
15	N.C.	GND	BR3*	A23	GA3* (1)	D17
16	GND	DTACK*	AM0	A22	+3.3V	D18
17	N.C.	GND	AM1	A21	GA4* (1)	D19
18	GND	AS*	AM2	A20	+3.3V	D20
19	N.C.	GND	AM3	A19	SMB_SCL	D21
20	GND	IACK*	GND	A18	+3.3V	D22
21	N.C.	IACKIN*	IPMB_SCL	A17	SMB_SDA	D23
22	GND	IACKOUT*	IPMB_SDA	A16	+3.3V	GND
23	N.C.	AM4	GND	A15	SMB_ALERT*	D24
24	GND	A07	IRQ7*	A14	+3.3V	D25
25	N.C.	A06	IRQ6*	A13	N.C.	D26
26	GND	A05	IRQ5*	A12	+3.3V	D27
27	N.C.	A04	IRQ4*	A11	N.C.	D28
28	GND	A03	IRQ3*	A10	+3.3V	D29
29	N.C.	A02	IRQ2*	A09	N.C.	D30
30	GND	A01	IRQ1*	A08	+3.3V	D31
31	N.C.	-12V	+5V_STANDBY	+12V	GND	GND
32	GND	+5V	+5V	+5V	+5V	+5V

* VME signals active when low.

(1) Geographical address pins, refer to section 4.3.2.2 page 75 for more information.

Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. Only use the VM6103 in VME IEEE1014x or VME64 backplanes that supply power on both P1 and P2 connectors. Failure to observe this warning may result in damage to the board.

4.3.2.2. Geographical Address Pin Assignment

The 6 geographical address pins (GA0*, GA1*, GA2*, GA3*, GA4* and GAP*) shall be tied to ground or left open (floating) on the backplane P1 connector as defined in the table below.

SLOT NUMBER	GAP* PIN	GA4* PIN	GA3* PIN	GA2* PIN	GA1* PIN	GA0* PIN
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
10	GND	Open	GND	Open	GND	Open
11	Open	Open	GND	Open	GND	GND
12	GND	Open	GND	GND	Open	Open
13	Open	Open	GND	GND	Open	GND
14	Open	Open	GND	GND	GND	Open
15	GND	Open	GND	GND	GND	GND
16	Open	GND	Open	Open	Open	Open
17	GND	GND	Open	Open	Open	GND
18	GND	GND	Open	Open	GND	Open
19	Open	GND	Open	Open	GND	GND
20	GND	GND	Open	GND	Open	Open
21	Open	GND	Open	GND	Open	GND

The device that samples the levels of the geographical address pins will read the inverted value of the slot number into which the board is plugged. When the board is powered on without being plugged into a VME/VME64 backplane the slot number will be zero with a parity error (GAP* open).

4.3.2.3. VMEbus Signal Description

The VMEbus signals occupy rows a, b and c of the P1 connector and row b of the P2 connector

Table 36: VME Signal Description

MNEMONIC	SIGNAL DESCRIPTION
A01 to A15	Address Bus (bits 1 to 15). Address lines that are used to broadcast a short standard or extended address.
A16 to A23	Address Bus (bits 16 to 23). Address lines that are used in conjunction with A01-A15 to broadcast a standard or extended address.
A24 to A31	Address Bus (bits 24 to 31). Address lines that are used in conjunction with A01-A23 to broadcast an extended address.
ACFAIL*	AC Failure. This signal indicates when the AC input to the power supply is no longer being provided or that the required AC input voltage levels are not being met.
AM0 to AM5	Address Modifier (bits 0 to 5). These signals are used to broadcast information such as the address size, cycle type, master identification or any combination of these.
AS*	Address Strobe. This signal indicates when a valid address has been placed on the address bus.
BBSY*	Bus Busy. This signal is driven low by the requester associated with the current bus master to indicate that its master is using the bus.
BCLR*	Bus Clear. This signal is generated by an arbiter to indicate that there is a higher priority request for the bus than the one being processed. This signal requests the current master to release the bus.
BERR*	Bus Error. This signal is generated by a slave or bus timer to tell the master that the data transfer was not completed.
BG0IN* to BG3IN*	Bus Grant (0 to 3) In. These signals are generated by the arbiter to tell the board receiving it that if it is requesting the bus on that level, then it has been granted use of the bus. Otherwise the board should pass the signal down the daisy chain. The BGxIN*/BGxOUT* signals form the bus grant daisy chain, i.e. the BGxOUT* of one board forms the BGxIN* of the next board in the daisy chain.
BG0OUT* to BG3OUT*	Bus Grant (0 to 3) Out. These signals are generated by requesters to tell the next board in the daisy chain that if it is requesting the bus on that level, then it may use the bus. Otherwise the board should pass the signal down the daisy chain.
BR0* to BR3*	Bus Request (0 to 3). A low level, generated by a requester, on one of these lines, shows that some master needs to use the bus.
D00 to D31	Data Bus (0 to 31). These signals are used to transfer data between masters and slaves, and status/ID information from interrupters to interrupt handlers.
DS0*, DS1*	Data Strobe 0, 1. These signals are used with LWORD* and A01 to show how many byte locations are being accessed (1, 2, 3 or 4). Also, during a write cycle, the falling edge of the first data strobe shows that valid data is available on the bus. On a read cycle, the rising edge of the first data strobe shows that data has been accepted from the data bus.
DTACK*	Data Transfer Acknowledge. This signal is generated by a slave. The falling edge shows that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle. The rising edge shows that the slave has released the data bus at the end of a read cycle.
GA0* to GA4* and GAP*	Geographical address pins (refer to the table in section 4.3.2.2). These pins indicate to the VME board which one of the backplane slot it currently uses (0 to 21).
GND	The DC voltage reference for the system.
IACK*	Interrupt Acknowledge. This signal is used by the interrupt handler to acknowledge an interrupt request. It is routed to the IACKIN* pin of slot 1, where it is monitored by the IACK daisy chain driver.
IACKIN*	Interrupt Acknowledge In. This signal tells the board receiving it that board can respond to the interrupt acknowledge cycle in process or pass it down the daisy chain. IACKIN*/IACKOUT* form the interrupt acknowledge daisy chain.
IACKOUT*	Interrupt Acknowledge Out. This signal is sent by a board to tell the next board in the daisy chain that it can respond to the interrupt acknowledge cycle in progress.
IPMB_SCL	Intelligent Platform Management Bus - Clock I2C
IPMB_SDA	Intelligent Platform Management Bus - Data I2C
IRQ1* to IRQ7*	Interrupt Request (1 to 7). These signals are driven low by interrupters to request an interrupt on the corresponding level.

MNEMONIC	SIGNAL DESCRIPTION
LWORD*	Longword. This signal is used with DS0*, DS1* and A01 to select which byte location(s) within the 4-byte group are accessed during the data transfer.
N.C.	This pin is not connected.
SMB_ALERT*	System Management Bus - Alert
SMB_SCL	System Management Bus - Serial clock line from the SMBus master to SMBus slave devices.
SMB_SDA	System Management Bus - Bi-directional serial data line between the SMBus master and the SMBus slave device.
SYSCLK	System Clock. This signal provides a constant 16 MHz clock signal that is independent of any other bus timing.
SYSFAIL*	System Fail. This signal shows that a failure has occurred in the system. It can be generated by any board in the system. It is also asserted after a reset and released when the board reset self-tests are passed successfully.
SYSRESET*	System Reset. When this signal is low, it causes the system to be reset.
WRITE*	Write. This signal is generated by a master to show whether the data transfer cycle is a read or a write.
+3.3V	+3.3 Volts DC power
+5V	+5 Volts DC power
+12V	+12 Volts DC power
-12V	-12 Volts DC power

4.3.3. P2 Connector

4.3.3.1. P2 Connector Pin Assignment

The VMEbus signals occupy rows a, b and c of the P1 connector and row b of the P2 connector. Refer to section 4.3.2.1 page 74 for a detailed description of the row b of the P2 connector.

Table 37: P2 Connector Pin Assignment

PIN	ROW Z	ROW A	ROW B	ROW C	ROW D
1	PMC2 IO 02	PMC1 IO 02	+5V	PMC1 IO 01	PMC2 IO 01
2	GND	PMC1 IO 04	GND	PMC1 IO 03	PMC2 IO 03
3	PMC2 IO 05	PMC1 IO 06	RETRY*	PMC1 IO 05	PMC2 IO 04
4	GND	PMC1 IO 08	V_A<24>	PMC1 IO 07	PMC2 IO 06
5	PMC2 IO 08	PMC1 IO 10	V_A<25>	PMC1 IO 09	PMC2 IO 07
6	GND	PMC1 IO 12	V_A<26>	PMC1 IO 11	PMC2 IO 09
7	PMC2 IO 11	PMC1 IO 14	V_A<27>	PMC1 IO 13	PMC2 IO10
8	GND	PMC1 IO 16	V_A<28>	PMC1 IO 15	PMC2 IO12
9	PMC2 IO 14	PMC1 IO 18	V_A<29>	PMC1 IO 17	PMC2 IO 13
10	GND	PMC1 IO 20	V_A<30>	PMC1 IO 19	PMC2 IO 15
11	PMC2 IO 17	PMC1 IO 22	V_A<31>	PMC1 IO 21	PMC2 IO 16
12	GND	PMC1 IO 24	GND	PMC1 IO 23	PMC2 IO 18
13	PMC2 IO 20	PMC1 IO 26	+5V	PMC1 IO 25	PMC2 IO 19
14	GND	PMC1 IO 28	V_D<16>	PMC1 IO 27	PMC2 IO 21
15	PMC2 IO 23	PMC1 IO 30	V_D<17>	PMC1 IO 29	PMC2 IO 22
16	GND	PMC1 IO 32	V_D<18>	PMC1 IO 31	PMC2 IO 24
17	PMC2 IO 26	PMC1 IO 34	V_D<19>	PMC1 IO 33	PMC2 IO 25
18	GND	PMC1 IO 36	V_D<20>	PMC1 IO 35	PMC2 IO 27
19	PMC2 IO 29	PMC1 IO 38	V_D<21>	PMC1 IO 37	PMC2 IO 28
20	GND	PMC1 IO 40	V_D<22>	PMC1 IO 39	PMC2 IO 30
21	PMC2 IO 32	PMC1 IO 42	V_D<23>	PMC1 IO 41	PMC2 IO 31
22	GND	PMC1 IO 44	GND	PMC1 IO 43	S1_TX or S1_TX- (1)
23	S2_TX or S2_TX- (1)	PMC1 IO 46	V_D<24>	PMC1 IO 45	S1_RX or S1_RX- (1)
24	GND	PMC1 IO 48	V_D<25>	PMC1 IO 47	S3_TX or S1_RTS or S1_TX+ (3)
25	S2_RX or S2_RX- (1)	PMC1 IO 50	V_D<26>	PMC1 IO 49	S3_RX or S1_CTS or S1_RX+ (3)
26	GND	PMC1 IO 52	V_D<27>	PMC1 IO 51	N.C.
27	S4_TX or S2_RTS or S2_TX+ (2)	PMC1 IO 54	V_D<28>	PMC1 IO 53	N.C.
28	GND	PMC1 IO 56	V_D<29>	PMC1 IO 55	N.C.
29	S4_RX or S2_CTS or S2_RX+ (2)	PMC1 IO 58	V_D<30>	PMC1 IO 57	GPIO5
30	GND	PMC1 IO 60	V_D<31>	PMC1 IO 59	GPIO4
31	GPIO6	PMC1 IO 62	GND	PMC1 IO 61	GND
32	GND	PMC1 IO 64 or GPIO7 (4)	+5V	PMC1 IO 63 or GPIO8 (4)	+5V

* Signals active when low.

(1) The serial I/O TX and RX pins act as either single-ended signal for EIA-232 or one side differential pair forEIA-422/485.

(2) The serial I/O TX and RX pins act as either CTS and RTS respectively in COM2 handshaking mode or differential pair for Rx and Tx respectively in COM2 EIA-422/485 modes.

(3) The serial I/O TX and RX pins act as either CTS and RTS respectively in COM1 handshaking mode or differential pair for Rx and Tx respectively in COM1 EIA-422/485 modes.

(4) Extra GPIO 7 and 8 are available on P2. The default signal is PMC IO. Please contact Kontron for more information on this feature.

4.3.3.2. P2 Connector Signal Description

The VME signals (row b) are described in section 4.3.2.3.

Table 38: P2 Connector Signal Description

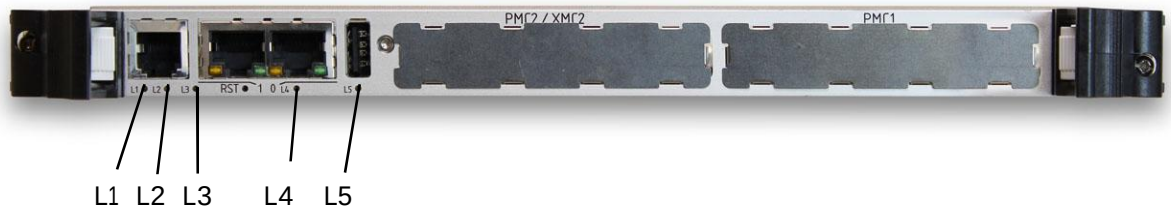
MNEMONIC	SIGNAL DESCRIPTION
GND	Ground
GPIO	General Purpose I/O x
PMC *x* IO yy	PMC Site *x* I/O signal *yy*
S*x*_CTS	Channel EIA-232 *x* - Clear-To-Send
S*x*_RTS	Channel EIA-232 *x* - Ready-To-Send
S*x*_RX	Channel EIA-232 *x* - Receive Data
S*x*_TX	Channel EIA-232 *x* - TransmitData
Sx_RX+/-	Channel EIA-422/485 x - Receive Data
Sx_TX+/-	Channel EIA-422/485 x – Transmit Data
+5V	+5 Volts DC power

4.4. LEDs

Status LEDs Normal Operation

There are five bicolor LEDs (Red/Green) on the front panel of the VM6103 6U VME board.

Figure 26: LEDs Front panel



By default (normal mode), the state of L3, L4 and L5 is according to the table below. But these LEDs can also be switched to user mode with the color and blinkling mode controlled by software.

When L1 is red (permanent error), the meaning of the other LEDs no more comply to the states listed in the table below, but report an error code as listed in the table at next paragraph.

Table 39: LEDs Description

CPU LED	COLOR	DESCRIPTION
L1	RED	Permanent error on subsystem
	GREEN	Standby (board's power supplies are off).
	AMBER	Reset state on subsystem
	BLINKING	CPLD activity (IFC access to CPLD, or backplane I2C activity).
	OFF	Normal operation: no error, no reset, no CPLD activity
L2	RED	CPLD watchdog reset timer expired
	GREEN	Normal operation mode
	AMBER	Factory test mode
	BLINKING	SATA activity
L3	RED	Temperature alert (processor hot)
	GREEN	1000BASE-T rear LAN link
	AMBER	10/100BASE-T(X) rear LAN link
	BLINKING	LAN activity on rear
	OFF	No error
L4	RED	PBIT failed
	GREEN	PCI activity
	AMBER	ALMA2f VME FPGA downloading
	OFF	No error, no PCI activity
L5	RED	Unused
	GREEN	VME activity
	OFF	No error

Status LEDs for permanent error

	L1	L2	L3	L4	L5	
ERR_THERM_FAULT	R	-	R	R	R	CPU Critical thermal error
ERR_VME_UV_PWRGD	R	-	-	-	O	Over voltage on backplane
ERR_VME_OV_PWRGD	R	R	-	-	O	Under voltage on backplane
ERR_INTERNAL_PSU	R	x	x	x	x	Board's internal PSU error

R : red
O : amber (orange)
- : off
x : any other combination of LEDs not already listed above

5/ Power and Thermal Specifications

5.1. Power Considerations

5.1.1. System Power

The considerations presented in the ensuing sections must be taken into account by system integrators when specifying the VM6103 system environment.

5.1.1.1. VM6103 Baseboard

The VM6103 board has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the VM6103 should be carefully tested to ensure compliance with these ratings.

Table 40: Maximum Input Power

SUPPLY VOLTAGE	MAXIMUM PERMIT VOLTAGE
+5 VDC	+6 V
+12 V / -12 VDC (1)	+14 V / -14 V

(1) if required for mezzanine.
+12 V and -12 V are necessary if required by PMC or XMC board

CAUTION: The maximum permitted voltage indicated in the table above must not be exceeded. Failure to comply with these figures may result in damage to your board.

The following table specifies the range of the different input power voltages within the board is functional. The VM6103 is not guaranteed to function if the board is not operating within the prescribed limits.

Table 41: DC Operational Input Voltage Ranges

INPUT SUPPLY VOLTAGE	ABSOLUTE RANGE
+3.3V	3.25V min. to 3.45V max.
+5V	4.875V min to 5.25V max.
+12V (1)	11.64V min. to 12.6V max.
-12V (1)	-12.6V min. to -11.64V max.

(1) if required for mezzanine.

5.1.1.2. Backplane

Backplanes to be used with the VM6103 must be adequately specified. The backplane must provide optimal power distribution for the +5 V and +12 V power inputs. It is recommended to use only backplanes which have at least +5 V power planes voltage.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided.

5.1.1.3. Power Supply Units

Power supplies for the VM6103 must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires.

An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for die resistance variations.

Tolerance

The following table provides information regarding the required characteristics for each board input voltage.

Table 42: Input Voltage Characteristics

VOLTAGE	NOMINAL VALUE	TOLERANCE	MAX. RIPPLE (P-P)	REMARKS
5V	+5.0 VDC	+5%/-3%	50 mV	Main voltage
+12V	+12 VDC	+5%/-5%	240 mV	Required
-12V	-12 VDC	+5%/-5%	240 mV	Not Required
GND	Ground, not directly connected to potential earth (PE)			

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

PMC site 1 and 2 are no 5V tolerant. VIO voltage must be +3.3 VDC.

Regulation

The power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it went below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

5.1.2. Power Consumption

The power consumption tables below list the voltage and power specifications for the VM6103 board. The values were measured using an 8-slot passive VME backplane.

Table 43: VM6103 Thermal Power: board power based on current measurements

POWER MODE	MAX CPU POWER	MAX TOTAL POWER CONSUMPTION	CURRENT DRAWN	TEST CONDITION
VM6103 QorIQ LS1023A 1.0GHz				
Normal mode	3.6 W	9.4 W	1.9 A / 5.0 VDC	Linux, CoreMark® 100%, processor junction temperature lower than 90°C, 2x Gigabit Ethernet links, 4 GB single bank DDR4-1600 memory configuration, no module on-board.
Low power saving mode	TBD	8.1 W	1.6 A / 5.0 VDC	Linux low power mode requested, 55°C ambient temperature, 1,2 m/s inlet airflow, 2x Gigabit Ethernet links, 4 GB single bank DDR4-1600 memory configuration, no module on-board.
Linux idle	TBD	8.1 W	1.6 A / 5.0 VDC	Linux, 55°C ambient temperature, 1,2 m/s inlet airflow, 2x Gigabit Ethernet links, 4 GB single bank DDR4-1600 memory configuration, no module on-board.
Uboot shell prompt	TBD	8.1 W	1.6 A / 5.0 VDC	Uboot, 55°C ambient temperature, 1,2 m/s inlet airflow, 2x Gigabit Ethernet links, 4 GB single bank DDR4-1600 memory configuration, no module on-board.
VM6103 QorIQ LS1043A 1.6GHz				
Normal mode	4.0 W	10.5 W	2.1 A / 5.0 VDC	Linux, CoreMark® 100%, processor junction temperature lower than 90°C, 2x Gigabit Ethernet links, 4 GB single bank DDR4-1600 memory configuration, no module on-board.
Low power saving mode	3.3 W	9.1 W	1.8 A / 5.0 VDC	Linux low power mode requested, 55°C ambient temperature, 1,2 m/s inlet airflow, 2x Gigabit Ethernet links, 4 GB single bank DDR4-1600 memory configuration, no module on-board.
Linux idle	3.2 W	9.1 W	1.8 A / 5.0 VDC	Linux, 55°C ambient temperature, 1,2 m/s inlet airflow, 2x Gigabit Ethernet links, 4 GB single bank DDR4-1600 memory configuration, no module on-board.
Uboot shell prompt	3.2 W	9.1 W	1.8 A / 5.0 VDC	Uboot, 55°C ambient temperature, 1,2 m/s inlet airflow, 2x Gigabit Ethernet links, 4 GB single bank DDR4-1600 memory configuration, no module on-board.

Table 44: Rail Current Draw

PROCESSOR	5V RAIL CURRENT DRAW	
	MAXIMUM	PEAK
LS1023A @1.0 GHz	TBD	TBD

Maximum and peak current draw are intended as with enabled Turbo mode and without mezzanine card or USB device plugged on board.

5.1.3. Maximum Power Consumption of M.2 Module

The M.2 socket 3, key M on VM6103 supports up to 2.5 A of current consumption on 3.3 V rail per defined in PCI Express M.2 Specification (maximum highest averaged current value over any 100-microsecond period).

The following table resumes the current consumption limit on M.2 module.

Table 45: Current of M.2 module

VOLTAGE	STANDARD LIMIT CURRENT	DESIGN LIMIT CURRENT
3.3 V	2.5 A	2.5 A

M.2 module can be installed simultaneously with a PMC module on slot 1. Users should carefully review the power ratings, cooling capacity and airflow requirements in the application prior to installation both a M.2 module and a PMC module, slot 1, on the VM6103.

5.1.4. Maximum Power Consumption of miniPCIe Module

The miniPCIe socket on VM6103 supports respectively up to 2.75 A and 0.5 A of current consumption on 3.3 V rail and 1.5 V rail per defined in PCI Express Mini card Specification (maximum highest averaged current value over any 100-microsecond period).

The following table resumes the current consumption limit on M.2 module.

Table 46: Current of miniPCIe module

VOLTAGE	STANDARD LIMIT CURRENT	DESIGN LIMIT CURRENT
3.3 V	2.75 A	2.75 A
1.5 V	0.5 A	0.5 A

5.1.5. Maximum Power Consumption of PMC Module

A maximum power of 7.5W is available on each PMC slot. This is in accordance with the draft standard P1386/Draft 2.4a. The maximum power of 7.5W can be arbitrarily divided on the 3.3V and 5V voltage lines.

PMC site 1 and 2 are no 5V VIO tolerant. PMC VIO voltage must be +3.3 VDC.

The following table indicates the current of a PMC module.

Table 47: Current of a PMC Module

VOLTAGE	STANDARD LIMIT CURRENT	DESIGN LIMIT CURRENT
3.3V	2.27A	4.6A
5V	1.5A	3A
+12V	0.5A	2A
-12V	0.4A	1A

Standard limit current is the limit current defined by P1386 standard. PMC should be able to dissipate at maximum 7.5W per voltage rail (3.3V and 5V).

Design limit current is the limit current defined by the board design, the current that not be exceed to avoid board damage.

5.1.6. Maximum Power Consumption of XMC Modules

A maximum power of 7.5 W is available on each XMC slot and it can be arbitrarily divided on the 3.3 V and 5 V (VPWR) voltage lines. XMC modules are based on 3.3 V power along with variable power (VPWR) defined as either 5 V or 12 V in the ANSI/VITA 42.0-200x XMC Switched Mezzanine Card Auxiliary Standard specification. On the VM6103, the VPWR is configured to 5 V.

The following table indicates the current of a XMC module.

Table 48: Current of a XMC Module

VOLTAGE	STANDARD LIMIT CURRENT	DESIGN LIMIT CURRENT
3.3V	0.75A	4.6A
5V (VPWR)	2.5A	3A
+12V (including VPWR option)	0.75A	2A
-12V	0.4A	1A

XMC integrators should carefully review the power ratings, cooling capacity and airflow requirements in the application prior to installation of an XMC module on the VM6103.

5.1.7. Processor Power Monitoring and Management

The VM6103 implements a current sensor on processor core power supply, this device (INA220) accessible from the processor I2C bus gives the current draw by the processor core voltage.

The QorIQ processor supports following power management features that can be used to save power:

- CPU idle (enabled by default), this feature dynamically puts a CPU core in low-power states when there is nothing left to be done on that CPU, and automatically wakes up the core when there is a task to be done.
- CPU hotplug, this feature allows removal and insertion of a CPU statically into the Linux system during runtime
- Dynamic Frequency Scaling (DFS or CPU freq), this features enables changes to the working frequency of CPU/cores at runtime.

Power management can NOT reduce maximum power consumption when the system is fully loaded. Therefore, the system designer still has to provision a power supply that needs to support the peak demands of the system according to the hardware specifications.

5.2. Thermal Considerations

The following sections provide system integrators with the necessary information to satisfy thermal and airflow requirements when implementing VM6103 applications.

5.2.1. Board Thermal Monitoring

To ensure optimal and long-term reliability of the VM6103, all onboard components must remain within the maximum temperature specifications. The most critical components on the VM6103 are the processor and the memory. Operating the VM6103 above the maximum operating limits will result in permanent damage to the board.

The VM6103 includes several temperature sensors to measure the onboard temperature values:

- Thermal Sensors integrated in the processor
- Four onboard temperature sensors (including processor remote sensor)

Three of onboard temperature sensors (Texas Instrument LM73) are located on the I2C bus, and managed by the CPLDs (SMBus master interface), the fourth onboard temperature sensors (On semiconductor ADT7461A) is located on I2C bus of processor. Refer to Figure 16 “I2C Diagram” page 49.

Key Features of the Remote Temperature Sensors

ADT7461A supports local and remote temperature sensor. ADT7461A supports two alarm outputs: ALERT#, THERM# signals to activate system protection, connected to cPLD for event reporting.

- Remote temperature resolution / accuracy (80 – 105°C) : 0.25°C / ±4°C
- Local temperature resolution / accuracy : 1°C / ±2.5°C
- Operating temperature: –40°C to +155°C

Key Features of the onboard Temperature Sensors

- Local temperature accuracy: +/- 2°C.
- Operating temperature: -40 °C / +150°C.
- I2C address:

Table 49: Thermal board sensors I2C address

BOARD SENSORS	#1	#2	#3	#4
I2C address (CPLD SMBus)	90	92	94	-
I2C address (CPU I2C bus)	-	-	-	98

Location of the onboard Temperature Sensors

Figure 27: VX305x-SA 3U VPX Overview

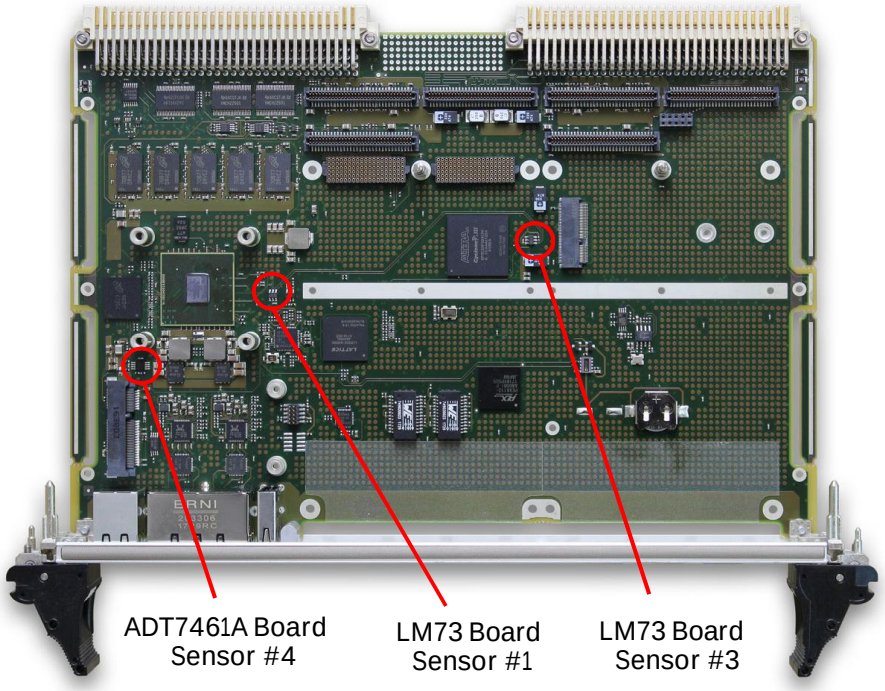
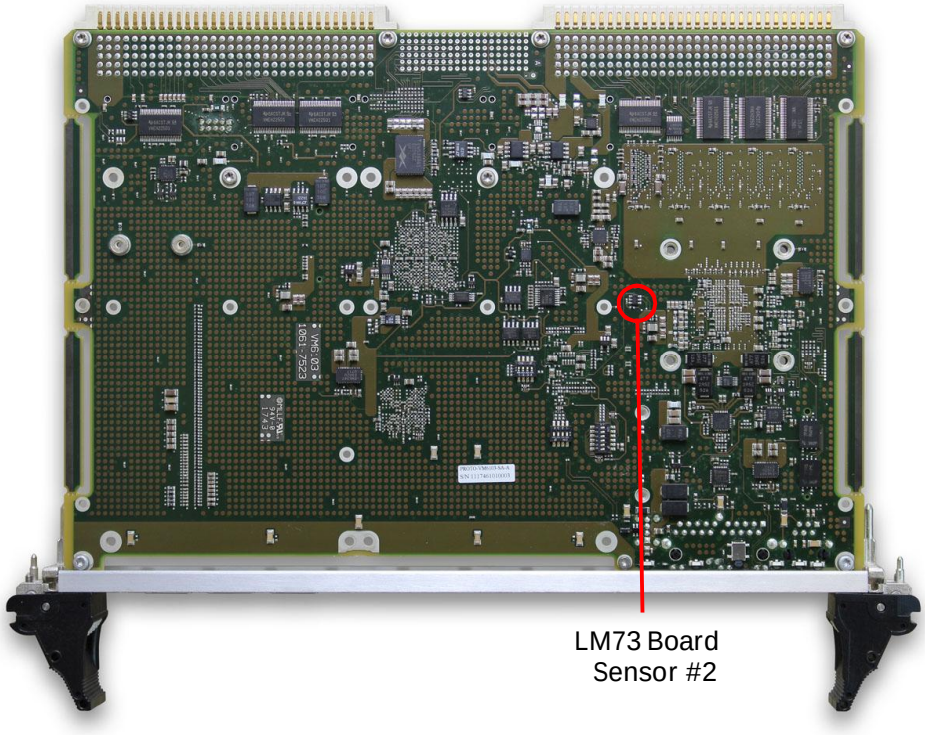


Figure 28: Board Temperature Sensors Location on bottom side of the Board



5.2.2. Processor Thermal Monitoring

To allow optimal operation and long-term reliability of the VM6103, the QorIQ Layerscape processor must remain within the maximum die temperature specification. The maximum operating temperature for the processor die (TJMAX) is 105°C.

The QorIQ processor implements a Thermal Monitoring Unit (TMU) to monitor and report the temperature from one or more remote temperature measurement sites located on processor.

- One Temperature Sensor near DDR controller
- One Temperature Sensor near SerDes
- One Temperature Sensor near Frame manager
- One Temperature Sensor near ARM A53 core

The TMU monitors these sensor sites and signals an alarm if a programmed threshold is ever exceeded. The current and average temperatures are continuously captured for each temperature sites and logged in resister set.

When the LED3 on the front panel is lit red after boot-up, it indicates that one of the processor temperature sites is above this programmed threshold value.

Catastrophic Cooling Failure Sensor

The Catastrophic Cooling Failure Sensor protects the processor from catastrophic overheating.

The Catastrophic Cooling Failure Sensor threshold is set to 110°C. When the junction temperature of processor will exceed this value, the processor will send an interrupt to CPLD for performing a shutdown of the internal power supplies. Once activated, the event remains latched until the VM6103 undergoes a power-on restart (all power off and then on again).

5.2.3. External Thermal Regulation

To ensure the best possible basis for operational stability and long-term reliability, the VM6103 is equipped with a heat sink (excepted RC class). Coupled together with system chassis, which provides variable configurations for forced airflow, controlled active thermal energy dissipation is guaranteed.

The physical size, shape, and construction of the heat sink ensure the lowest possible thermal resistance. In addition, the VM6103 has been specifically designed to efficiently support forced airflow as found in modern VME systems.

Thermal Characteristics Tables

The thermal characteristic table shown in the following sections illustrates the maximum ambient air temperature as a function of the volumetric airflow rate for the processor frequency indicated.

The table is intended to serve as guidance for reconciling board and system with the required computing power/frequency considering the thermal aspect.

There are two values representing the recommended and upper levels working points. These values are based on processor frequency and on processor junction temperature. When operating below the recommended value, the CPU and critical components run steadily without any intervention of thermal supervision. When operated above the maximal junction temperature of 105°C, thermal protection mechanisms take effect resulting in an emergency stop in order to protect the CPU and critical components from thermal destruction.

How to read the Table

Select a board class, a processor frequency and choose a working point just above the recommended. For a given flow rate there is a maximum airflow input temperature (= ambient temperature) provided. Between this operating point and the maximum, thermal supervision will not be activated. Above the maximal operating point, thermal supervision will become active protecting the CPU and the critical components from thermal destruction. The minimum airflow rate provided must be included between the recommended operating point and the maximum specified in the table to guarantee a correct cooling.

Values indicated in this table are issued from Coremark® benchmark with 100% of processor core workload.

Volumetric Flow Rate

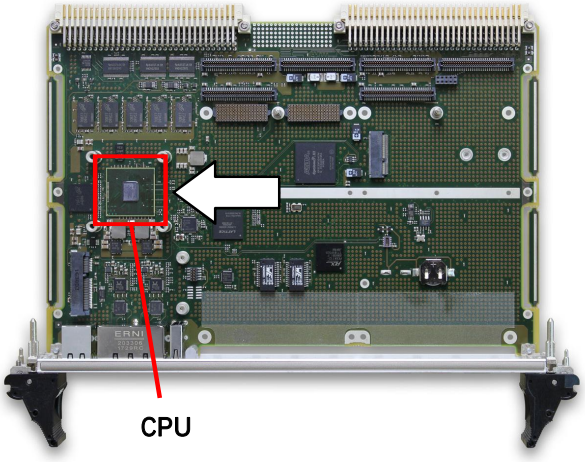
The volumetric flow rate refers to an airflow through a fixed cross-sectional area (i.e. slot width x depth). The volumetric flow rate is specified in cfm (cubic-feet per- minute).

Airflow

At a given cross-sectional area and a required flow rate, an average, homogeneous airflow speed can be calculated using the following formula: Airflow = Volumetric Flow Rate / Area

The airflow is specified in m/s (meter-per-second).

Figure 29: Airflow Direction



5.2.3.1. Thermal Operating Limits for VM6103

The following table indicates the operational limits of the VM6103 taking into consideration processor frequency vs. ambient air temperature vs. airflow rate. The measurements were made based on a 4HP slot (0.8 inch height) and using thermal benchmark from Coremark® with 100% of processor workload.

Table 50: VM6103 Thermal operating limits

CLASS	BOARD	TJMAX ALL CORES	TAMB	MIN AIRFLOW	CALCULATED INPUT AIR SPEED FOR 0,8" INPUT SECTION
SA Class	VM6103 SA LS1023A @ 1.0 GHz	< 65°C	55°C	9 CFM	2,3 m/s
		< 105°C	55°C	4 CFM	1,0 m/s
	VM6103 SA LS1043A @ 1.6 GHz	< 65°C	55°C	12 CFM	3,0 m/s
		< 105°C	55°C	4 CFM	1,0 m/s
WA Class	VM6103 WA LS1023A @ 1.0 GHz	< 65°C	65°C	17 CFM	4,3 m/s
		< 105°C	65°C	4 CFM	1,0 m/s
	VM6103 WA LS1043A @ 1.6 GHz	< 65°C	65°C	NA	NA
		< 105°C	65°C	4 CFM	1,0 m/s
RA Class	VM6103 RA LS1023A @ 1.0 GHz	< 85°C	70°C	18 CFM	4,5 m/s
		< 105°C	70°C	4 CFM	1,0 m/s
	VM6103 RA LS1043A @ 1.6 GHz	< 85°C	70°C	NA	NA
		< 105°C	70°C	TBD	TBD

The above table indicates the minimum air flow required for VM6103 cooling. Be careful, these values are intended as without mezzanine board presence (XMC/PMC card or M.2 module or mPCIe module).

5.2.3.2. Peripherals

When determining the thermal requirements for a given application, peripherals to be used with the VM6103 must also be considered. Devices such as M.2 module, miniPCIe module, PMC modules and XMC modules which are directly attached to the VM6103 must also be capable of being operated at the temperatures foreseen for the application. It may very well be necessary to revise system requirements to comply with operational environment conditions.

In most cases, this will lead to a reduction in the maximum allowable ambient operating temperature or even require active cooling of the operating environment.

As Kontron assumes no responsibility for any damage to the VM6103 or other equipment resulting from overheating of the CPU, it is highly recommended that system integrators as well as end users confirm that the operational environment of the VM6103 complies with the thermal considerations set forth in this document.

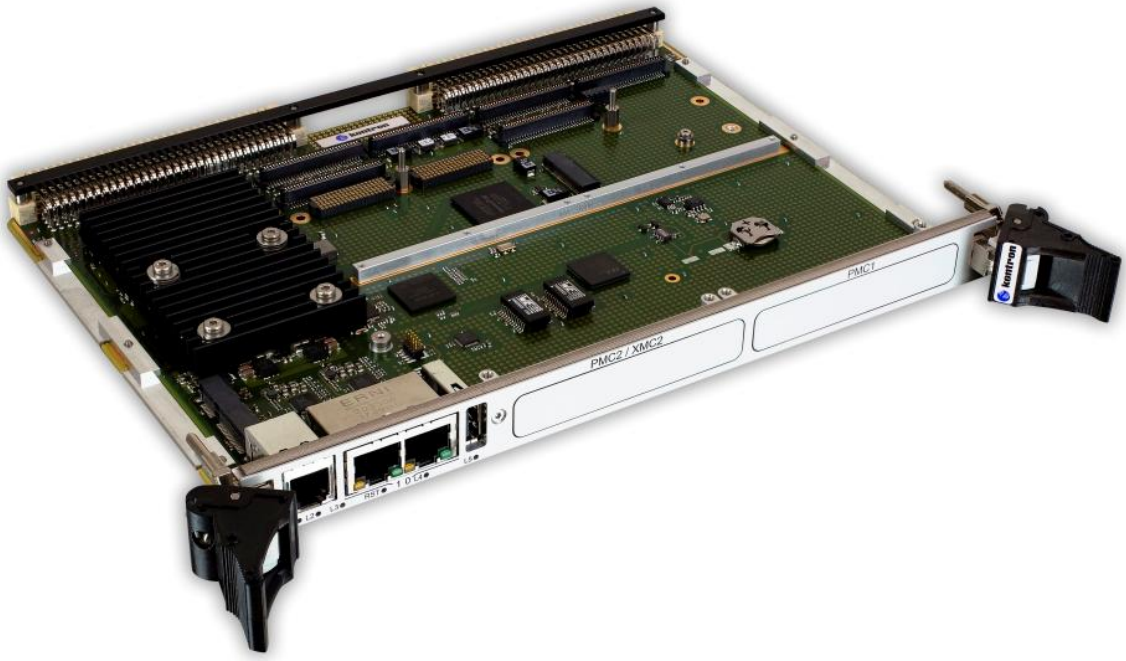
6/ VM6103-RA Characteristics

With an operational temperature range from -40º C up to +70º C and its mechanical environmental performances, the VM6103-RA are designed for severe environmental applications with high levels of shock and vibration, small space envelope and restricted cooling such as required in military, marine, avionics, sheltered and industrial applications. Unlike VM6103-SA and VM6103-WA, the VM6103-RA board uses mechanical stiffeners to meet the requirements for harsh environments.

Table 51: VM6103-RA Order Code

PRODUCT	ORDER CODE	DESCRIPTION
VM6103-RA	VM6103-RA24-00000000	6U Single slot 4HP (0,8") VME SBC -Rugged Air-Cooled 'RA' (-40°C to +70°C) with conformal coating - LS1023A Dual ARM A53 1.0GHz QorIQ LayerScape Processor - 4 GB soldered SDRAM with ECC - Soldered Flash 32GB eMMC Flash - Dual PMC, XMC, M.2 and mPCIe Expansion Slots - Without P0 connector - - No secure element - no PBIT - Conformal Coating

Figure 30: VM6103-RA – Overview



6.1. VM6103-RA Specificities

The VM6103-RA board has the same features as the VM6103-SA board, except for the following items which are fully described in associated sections below:

Table 52: VM6103-RA Specificities

FUNCTION	SEE ALSO
Battery Replacement	Section 6.3 page 93
Board Identification	Section 6.4 page 94
Environmental Specifications	Section 6.5 page 95
Mechanical Specifications	Section 6.6 page 96
MTBF	Section 6.7 page 97

6.2. VM6103-RA Thermal Consideration

As for the SA and WA classes, the VM6103-RA is equipped with a heat sink to ensure the best possible basis for operational stability and long-term reliability. The thermal characteristic table shown in the section 5.2.3.1 “Thermal Operating Limits for VM6103”, page 91 illustrates the maximum ambient air temperature as a function of the volumetric airflow rate for the processor frequency indicated. Refer to this section for further information about thermal consideration of VM6103-RA.

6.3. Battery Replacement

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer (Rayovac BR1225X-BA).
Unlike VM6103-SA board, battery with extended grade temperature must be installed in order to satisfy the thermal constraints.

To replace the battery, proceed as described in section 2.7.3, “Battery Replacement”, page 42.

⚠CAUTION

Danger of explosion when replacing with wrong type of battery. Replace only with the same or equivalent type recommended by the manufacturer. The lithium battery type must be UL recognized.

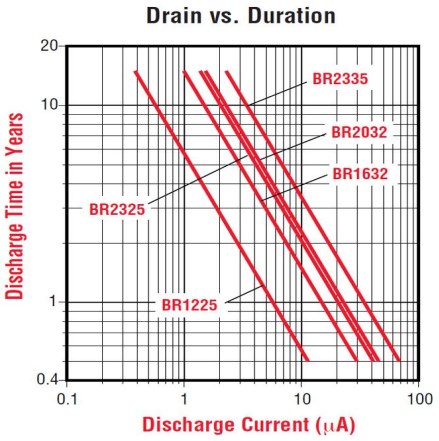
Do not dispose of lithium batteries in general trash collection. Dispose of the battery according to the local regulations dealing with the disposal of these special materials, (e.g. to the collecting points for dispose of batteries).

Reference of the battery used on the VM6103: RAYOVAC BR1225X-BA
The design of an electronic circuit powered by a component class battery requires the designer to consider two interacting paths that determine a battery’s life: consumption of active electrochemical components and thermal wear-out.

Battery Life

Figure 31 gives an estimate of years of service at various discharge currents for BR Lithium coin cells at room temperature. The RTC circuit power consumption is specified at 500 nA, giving an expected duration of more than 9 years in the absence of external power. In case of storage temperature or operating temperature is higher than 55°C or lower than 0°C, the battery life is reduced to 7 years in worst case.

Figure 31: Battery Life



For further information about the battery (battery used, battery installation and battery slot), refer to section section 2.7.3, “Battery Replacement”, page 42.

6.4. Board Identification

The VM6103-RA boards are identified by labels fitted to the bottom side. These labels are at the same location and have the same meaning (except the “Board Identification" label) as the VM6103-SA board labels (refer to the section 2.2 – “Board Identification”, page 34 for more information).

6.5. Environmental Specifications

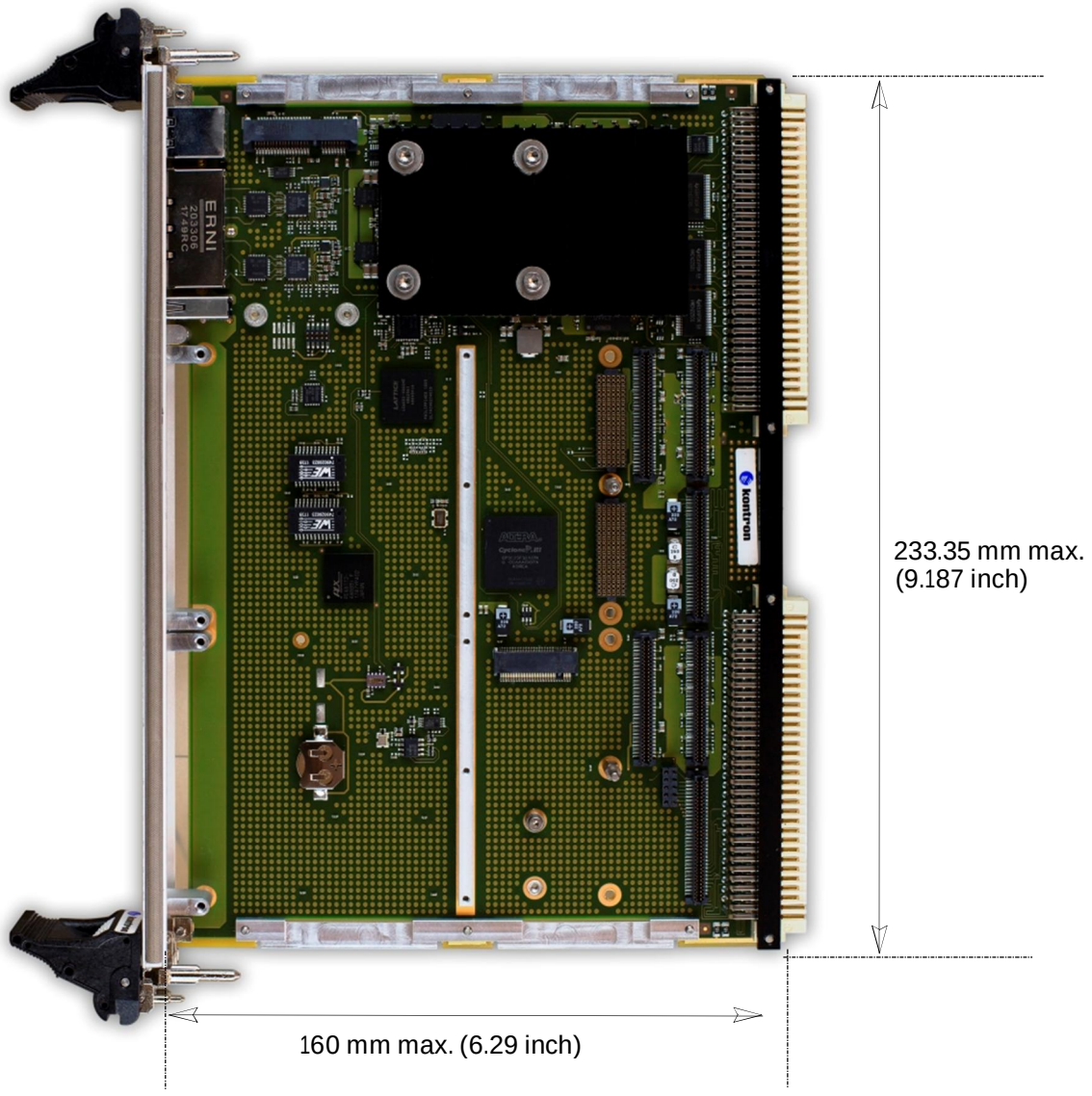
Table 53: VM6103-RA Environmental Specifications

	VM6103-RA RUGGED AIR-COOLED
Conformal Coating	Standard
Airflow	Higher than 4CFM for LS1023A@1GHz (see Table 50, page 91)
Operating Temperature	-40°C to +70°C Design to meet VITA 47-Class AC3
Cooling Method	Convection
Storage Temperature	-50°C to +100°C, except battery that must be stored within -40°C / +85°C
Vibration Sine (Operating)	5 Hz to 19 Hz - 2mm displacement 19 Hz to 2,000 Hz / 3g frequency range / acceleration
Random	VITA 47-Class V2
Shock (Operating)	20g / 11 ms peak acceleration / shock duration half sine
Altitude (Operating)	-1,500 to 60,000 ft
Relative Humidity	95% non-condensing

6.6. Mechanical Specifications

The VM6103-RC board is built on a multi-layer double Eurocard and conforms to the dimensions specified in the ANSI/VITA VME64 1-1994. The dimensions shown below are in millimeters, with inches (in parentheses) for general guidance only.

Figure 32: VME Dimensions



- **Length**: 233.35 mm max.
- **Depth**: 160 mm max.
- **Height**: 1 VME slot compatible
- **Weight**: ~430 g (approximatively)

6.7. MTBF

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

Table 54: VM6103-RA24-00000000 MTBF Data

	GB (Hours)		AIC (Hours)	NS (Hours)		ARW (Hours)
	25°C	40°C	40°C	25°C	40°C	55°C
MTBF (Hours)	TBD	TBD	TBD	TBD	TBD	TBD

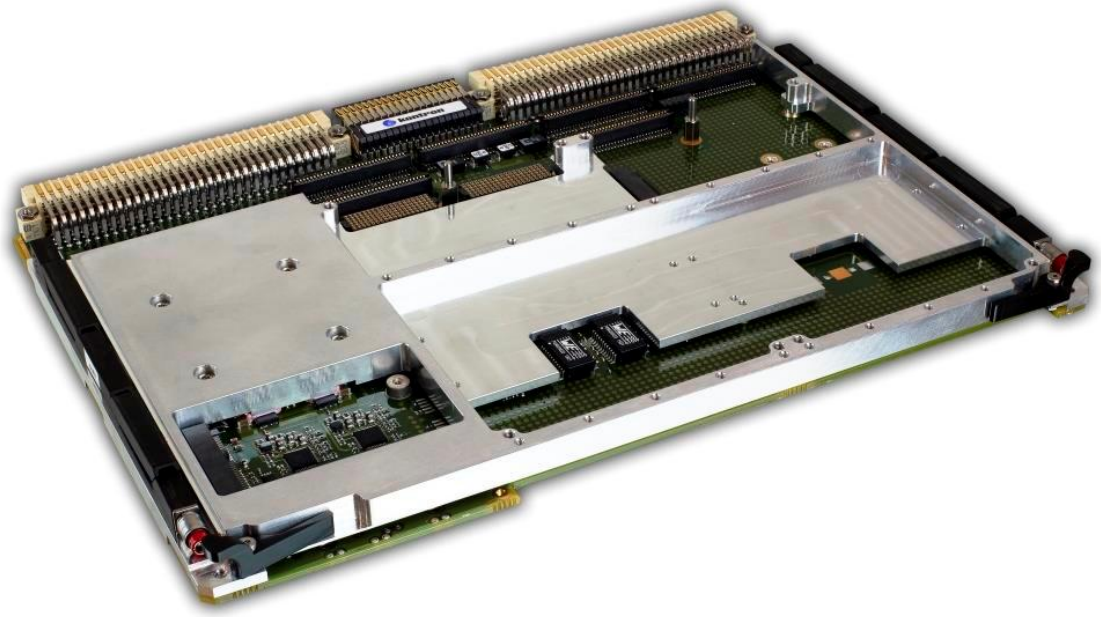
7/ VM6103-RC Characteristics

The VM6103-RC board uses “The Ruggedizer", a Kontron proven technology to meet the requirements for harsh environments. With an operational temperature range from -40º C up to +85º C and its mechanical environmental performances, the VM6103-RC is designed for severe environmental applications with high levels of shock and vibration, small space envelope and restricted cooling such as required in military, marine, avionics, sheltered and industrial applications.

Table 55: VM6103-RC Order Code

PRODUCT	ORDER CODE	DESCRIPTION
VM6103-RC	VM6103-RC24-00100000	6U Single slot 4HP (0,8") VME SBC -Rugged Conduction-Cooled 'RC-4' (-40°C to +85°C) conformal coating - LS1023A Dual ARM A53 1.0GHz QorIQ LayerScape Processor - 4 GB soldered SDRAM with ECC - Soldered Flash 32GB eMMC Flash - Dual PMC, XMC, M.2 and mPCIe Expansion Slots - With P0 connector - - No secure element - no PBIT - Conformal Coating

Figure 33: VM6103-RC – Overview



7.1. VM6103-RC Specificities

The VM6103-RC board has the same features as the VM6103-SA board, except for the following items which are fully described in associated sections below:

Table 56: VM6103-RC Specificities

FUNCTION	SEE ALSO
Thermal Considerations	Section 7.2 page 99
Battery Option	Section 7.3 page 101
Board Identification	Section 7.4 page 101
Environmental Specifications	Section 7.5 page 101
Mechanical Specifications	Section 7.6 page 102
MTBF	Section 7.7 page 103
Peripheral Connectivity	Section 7.8 page 103
PMC/XMC Installation	Section 7.9 page 105

7.2. VM6103-RC Thermal Consideration

The VM6103-RC is equipped with a heat frame to ensure the best possible basis for operational stability and long-term reliability. The heat frame is designed to ensure in the cooling of processor and other components.

The Table 57 illustrates the card edge temperature limits of the VM6103 to not exceed ensuring the processor and critical component enough cooling in operational condition. The measurements were made using thermal benchmark from Coremark® with 100% of processor workload taking into consideration processor frequency and core number (dual or quad core).

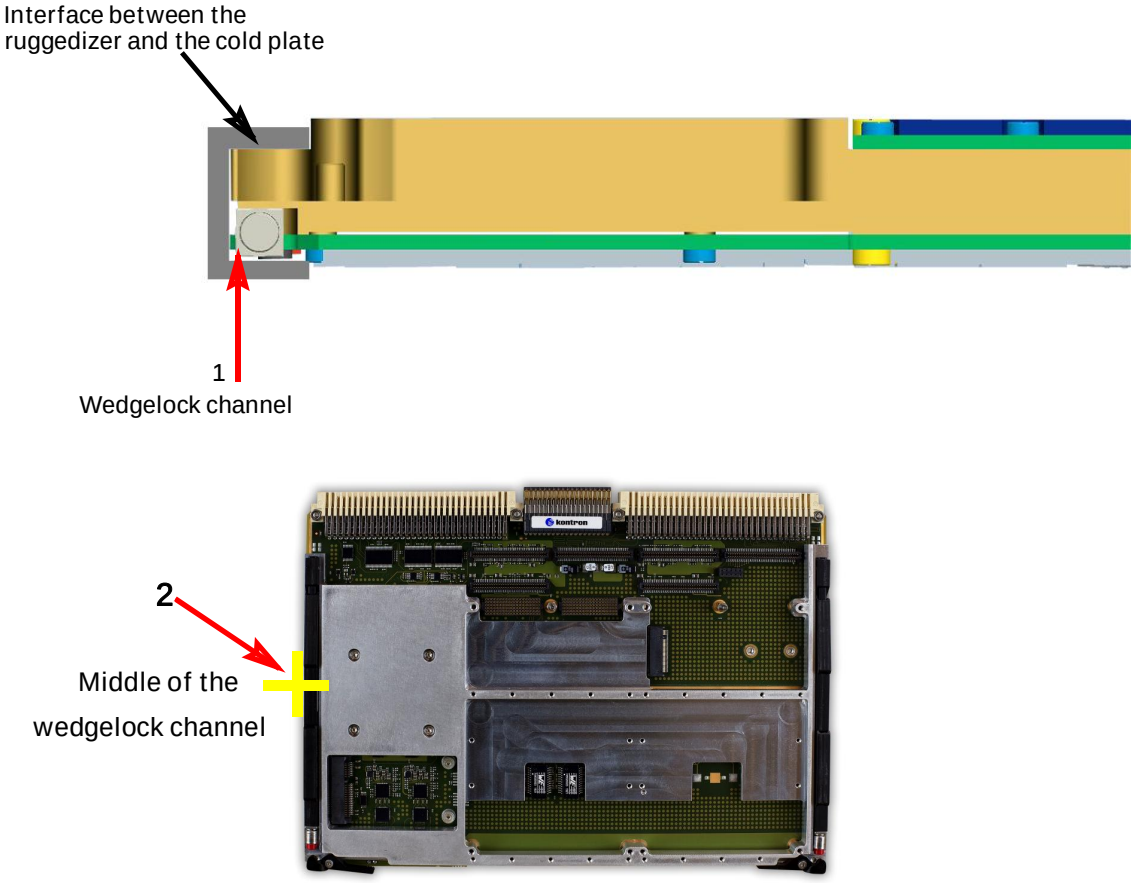
Table 57: VM6103-RC Thermal Operating Points

BOARD	CPU POWER DISSIPATION	TJMAX ALL CORES	CARD EDGE TEMPERATURE	NOTES
VM6103 SA LS1023A @ 1.0 GHz	4W	< 95°C	+85°C	Coremark® with 100% of processor workload

The value indicates in the Table 57 are intended as without mezzanine cards and modules presence. System integrators as well as end users shall confirm that the operational environment of the VM6103 complies with the thermal considerations set forth in this document.

CAUTION: The standard operating range is -40° to +85°C for the VM6103-RC. The card edge temperature check point is measured as follows: the middle point in the wedgelock channel on the ruggedizer. The wedgelock channel is the channel between the edge of the ruggedizer and the cold wall of the rack. Refer to arrows numbers 1 and 2 in following pictures.

Figure 34: Measuring the Temperature



According to ANSI/VITA 47 standard, the plug-in unit edge surface temperature is measured on the plug-in unit.

7.3. Battery Option

The lithium battery and its holder are not present on standard Rugged Conduction-cooled product. Nevertheless, customer requiring this option can contact Kontron support to know the term of availability for it.

Given the battery is not equipped, Time and Date cannot be maintained in RTC when board is power off if 3V3 standby power rail is not present on the chassis. On board power on, Time and Date values of u-boot built date are set in RTC.

7.4. Board Identification

The VM6103-RC boards are identified by labels fitted to the bottom side. These labels are at the same location and have the same meaning (except the “Board Identification" label) as the VM6103-SA board labels (refer to the section 2.2 – “Board Identification”, page 34 for more information).

7.5. Environmental Specifications

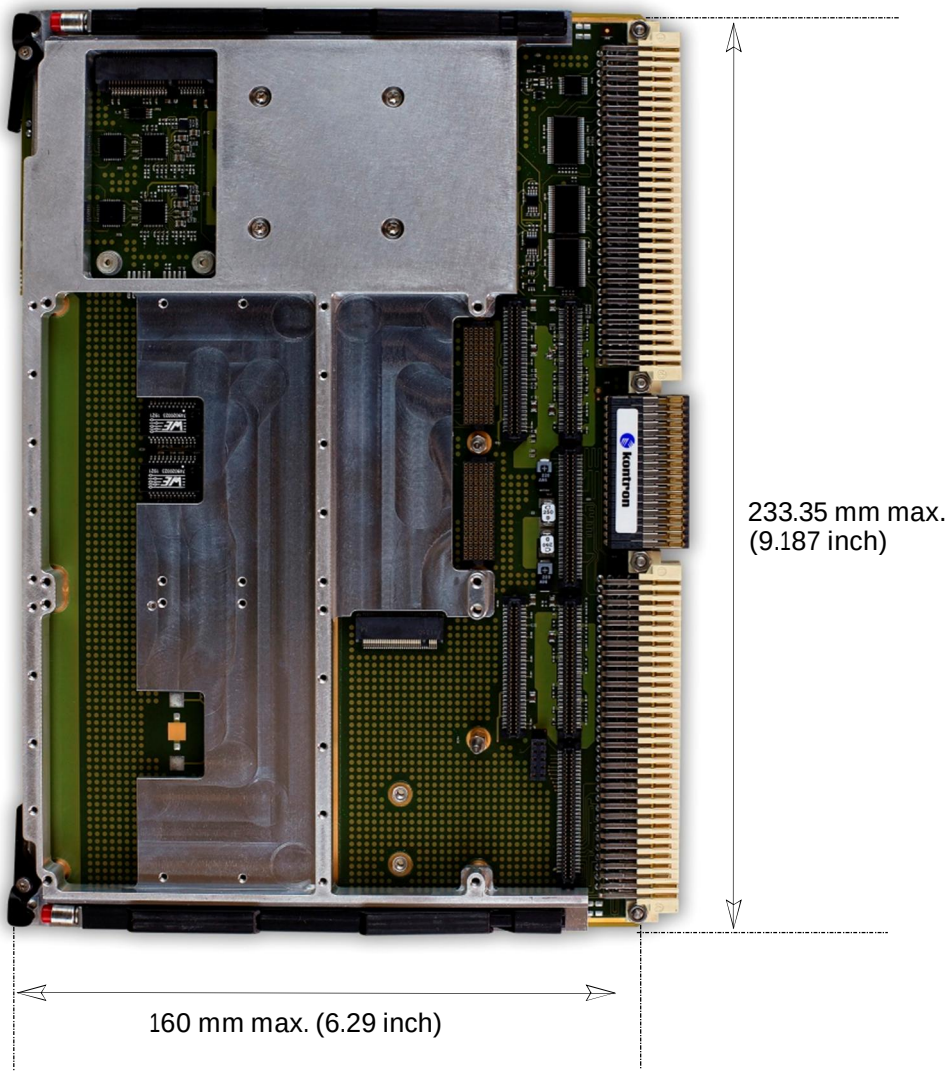
Table 58: VM6103-RC Environmental Specifications

	VM6103-RC RUGGED CONDUCTION-COOLED
Conformal Coating	Standard
Cooling Method	Conduction
Operating Temperature	-40°C to +85°C Design to meet VITA 47-Class CC4
Storage Temperature	-50°C to +100°C
Vibration Sine (Operating)	5 Hz to 22 Hz – 2.5mm displacement 22 Hz to 2,000 Hz / 5g frequency range / acceleration
Random	VITA 47-Class V3
Shock (Operating)	40g / 11 ms peak acceleration / shock Duration Half Sine
Altitude (Operating)	-1,500 to 60,000 ft
Relative Humidity	95% non-condensing

7.6. Mechanical Specifications

The VM6103-RC board is built on a multi-layer double Eurocard and conforms to the dimensions specified in the ANSI/VITA VME64 1-1994. The dimensions shown below are in millimeters, with inches (in parentheses) for general guidance only.

Figure 35: VME Dimensions



- **Length**: 233.35 mm max.
- **Depth**: 160 mm max.
- **Height**: 1 VME slot compatible
- **Weight**: ~550 g (approximatively)

7.7. MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

Table 59: VM6103-RC24-00100000 MTBF Data

	GB (Hours)		AIC (Hours)	NS (Hours)		ARW (Hours)
	25°C	40°C	40°C	25°C	40°C	55°C
MTBF (Hours)	TBD	TBD	TBD	TBD	TBD	TBD

7.8. Peripheral Connectivity

The VM6103-RC board features the same peripheral connectivity and connectors as the VM6103-SA except that:

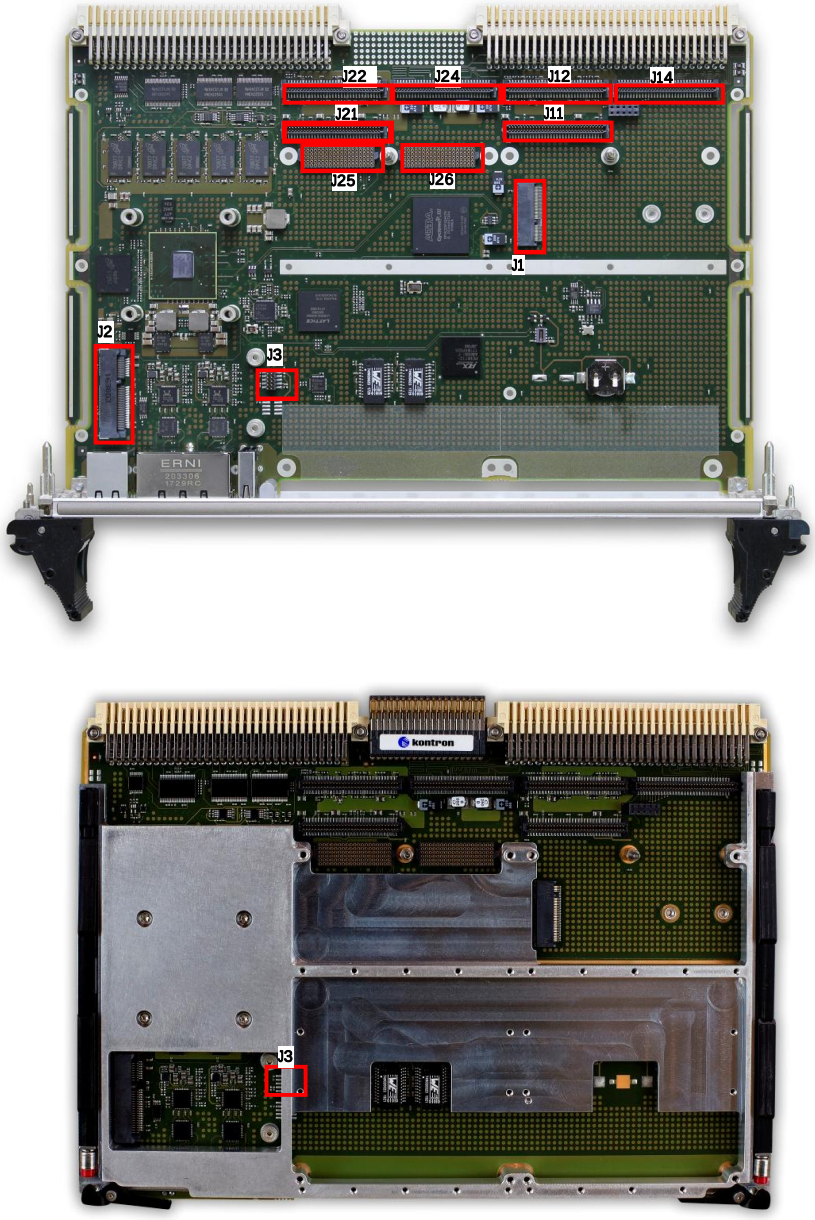
- the front panel connectors are absents:
  - serial lines COM1/COM2 are always routed to P2 connector,
  - ETH0 and ETH1 Ethernet interfaces are dynamically routed to P0 connector,
  - USB port 0 is no more available.
- the USB port 1 is always routed to P0 connector instead of miniPCIe J2 socket
- the J3 onboard Cortex debug connector is not populated on the VM6103-RC board.,

On VM6103 boards featuring P0 connector such VM6103-RC, SATA interface is routed by default to M.2 J1 socket in order to host SATA M.2 SSD modules.
Contact Kontron support to know the availability of SATA interface on P0 connector.

For detailed information about the peripheral connectivity on the VM6103, refer to section 1.2.4 – “I/O Interfaces” page 23.

For detailed information about the connectors located on the VM6103, refer to section 4.2 – “Onboard Connectors”, page 59.

Figure 36: VM6103-RC on-board Connector



7.9. PMC/XMC Installation

To install PMC/XMC mezzanine on VM6103-RC boards, use the Installation Fastenings Kit delivered with the VM6103-RC board. For each PMC/XMC location, it includes:

- 4x VIS-CZX-M2.5X6-INOX For the PMC/XMC assembly on the board **red** marks below
- 10x VIS-CZX-M2X6-INOX For the PMC/XMC assembly on the board **blue** marks below

Standard Anchorage Points

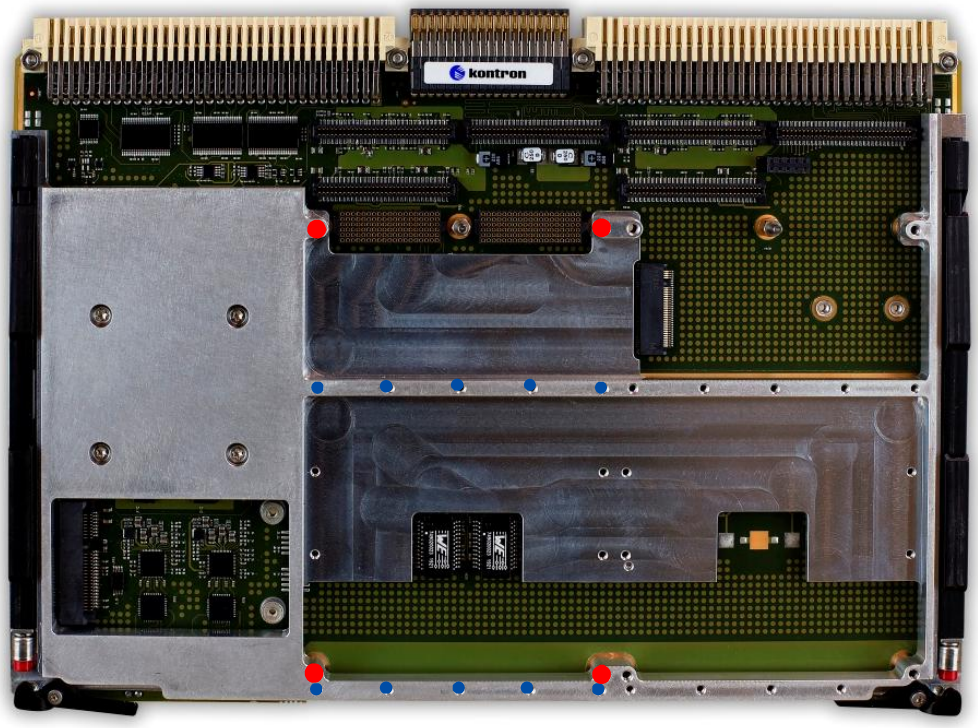
Install the XMC/PMC to the VM6103-RC according to the following steps.

To avoid ESD damage, wear an antistatic wrist strap to discharge static electricity while performing any part of the installation that involves touching the VM6103 board or the XMC/PMC.

If you can't wear an antistatic wrist strap, touch one hand to the bare metal surface to provide grounding.

1. Place carefully the VM6103 with the backplane connectors facing you on a static dissipative surface connected to a common ground by a low-resistance connection. Do not slide the board over any surface.
2. Remove the standoffs of the PMC/XMC if they are attached to. Align the standoffs and the holes at the front, the middle and the rear of the PMC with the matching holes on the VM6103x-RC board.
3. Install the XMC/PMC component side down, aligning the mezzanine board connectors into their mating connectors on the VM6103-RC. Press them together so that the friction from the pins holds the mezzanine board in place.
4. Screw the XMC/PMC in place using mounting screws (5+2 at the front of the board, 5 in the middle of the board and 2 at the rear of the board). Tighten with a torque of 0.383 N.m. (3.389 Lb-In). Figure 37 shows the location of the standard anchorage points on a VM6103-RC board.

Figure 37: Standard Anchorage Points on VM6103-RC Board



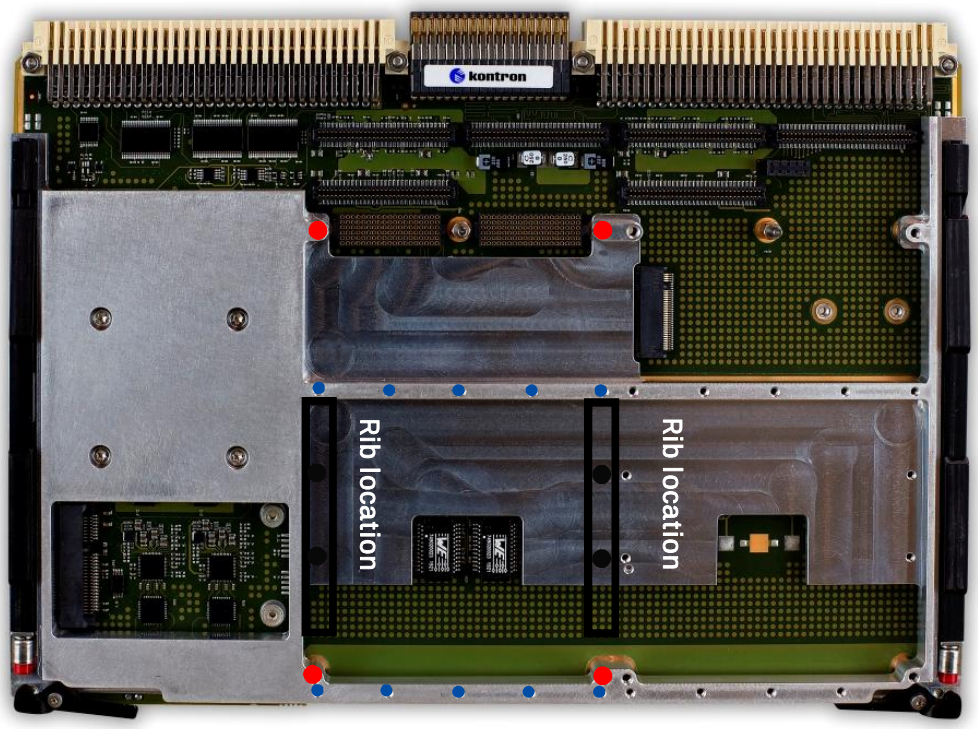
Fastening Kit

An optional secondary thermal interface ribs should be used to get the specified module thermal performance.

Order Code: **KIT-RIBPMC1V01-1**

2x RIB-PMC-1-V01	Two additional ribs	
4x VIS-CZX-M2X5-INOX	For the ribs assembly on the board	**black** marks below
10x VIS-CZX-M2.5X6-INOX	For the PMC assembly on the ribs (6x) For the PMC assembly on the board (4x)	**red** marks below
10x VIS-CZX-M2X6-INOX	For PMC assembly on the board	**blue** marks below

Figure 38: Usage of Fastenings Kit Ribs on VM6103-RC Board



7.10. Inserting and Removing the Board

Before inserting or removing VM6103-RC board , ensure that safety precautions are observed as per section 2.1 – “Safety Requirements”, page 33.

CAUTION: Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

Inserting the Board

1. Ensure that no power is applied to the system before proceeding.
2. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors. Then, simply push the board into the backplane connectors.
3. Engage the board with the backplane. When the ejector handle is against the heat frame, the board is engaged.
4. Tight the wedgelocks to the cold plate. A torque of 0.8 N.m must be applied to the both hexagonal wedgelock screws (Calmark serie 265) using 3/32 Allen wrench. See Figure 39

Removing the Board

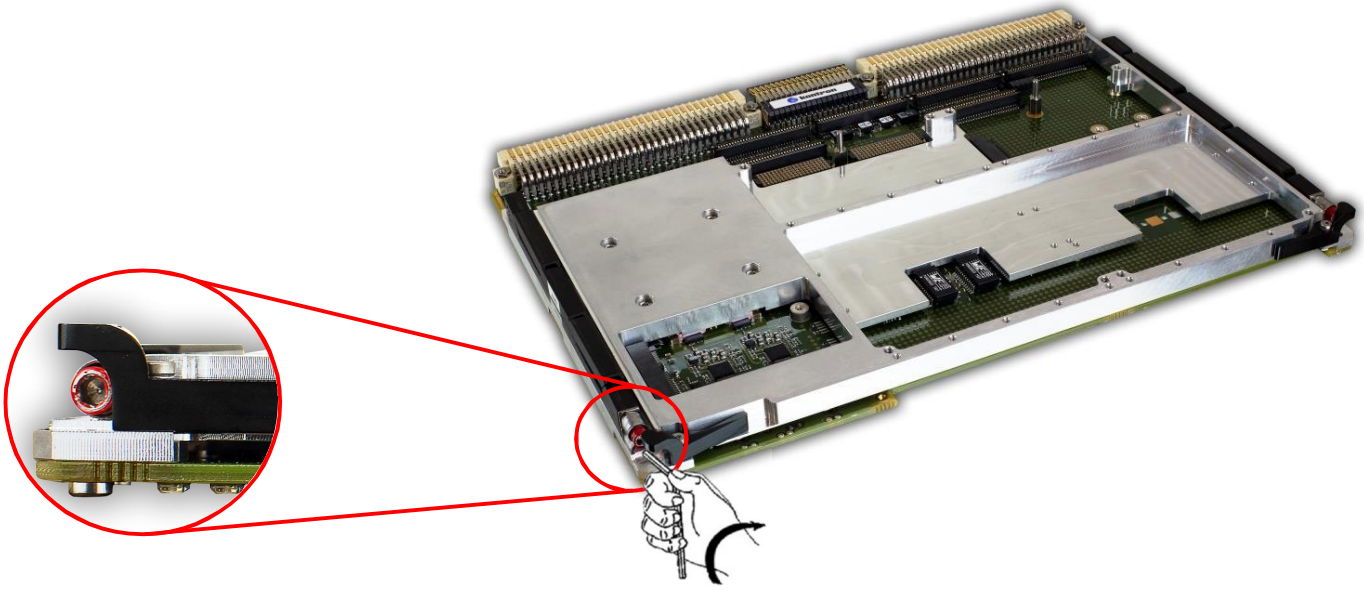
1. Ensure that no power is applied to the system before proceeding.
2. To remove VM6103-RC, loosen the wedgelocks to the cold plate by unscrewing the both hexagonal socket drive 3/32.
3. Disengage the board from the backplane using the board ejector handle, pull the handle until the board is disengaged.
4. After disengaging the board from the backplane, pull the board out of the slot.

Do not touch the heat frame while removing the board from a rack because it can get very hot. Do not place the board on any surface or in any form of storage container until the board and its heatsink have cooled down to room temperature.

⚠CAUTION

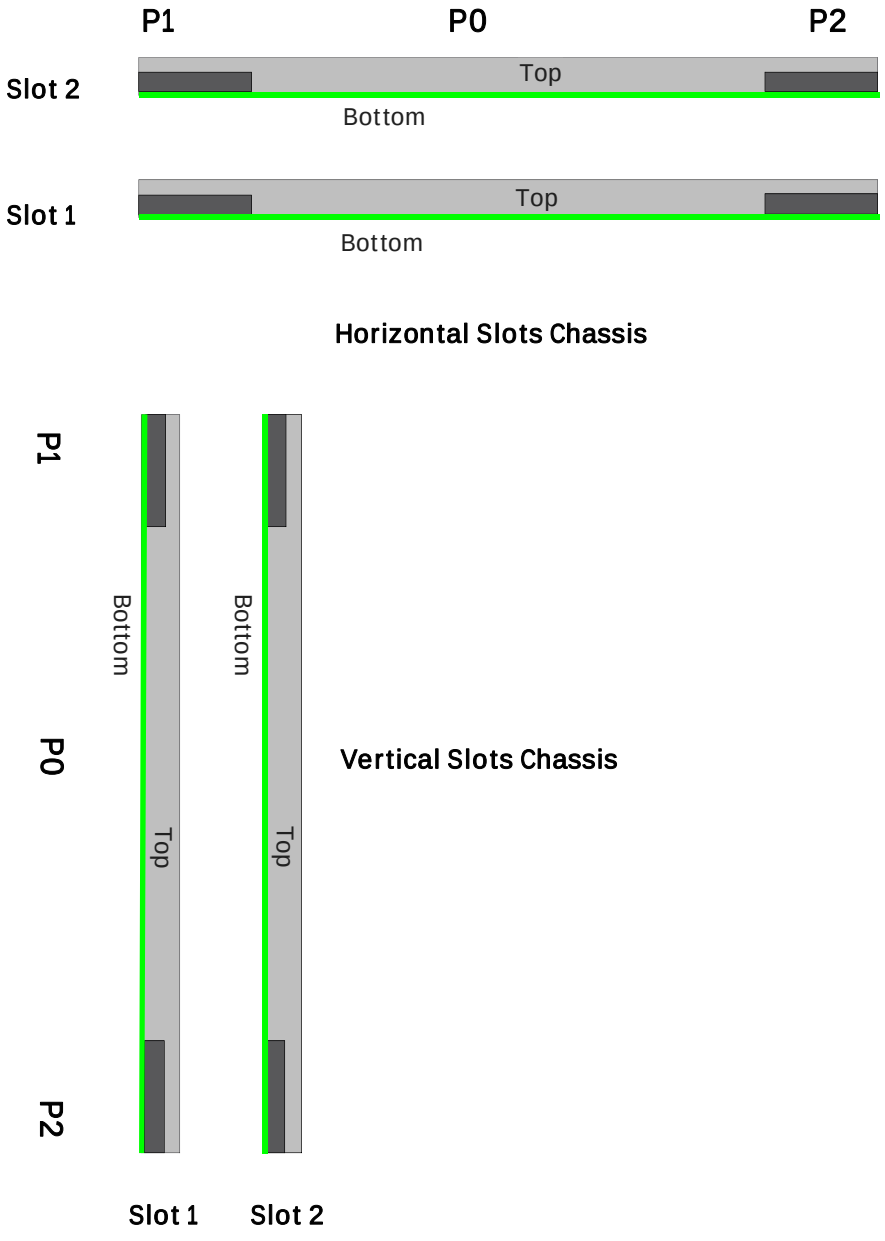
Running the board at high temperature without tightening the wedgelocks to the cold plate may result in permanent damage to the board.

Figure 39: VM6103-RC – Lock the board



Depending on the chassis type (horizontal slots or vertical slots), make sure to insert the board correctly, as shown below:

Figure 40: VM6103-RC - Slots Orientation



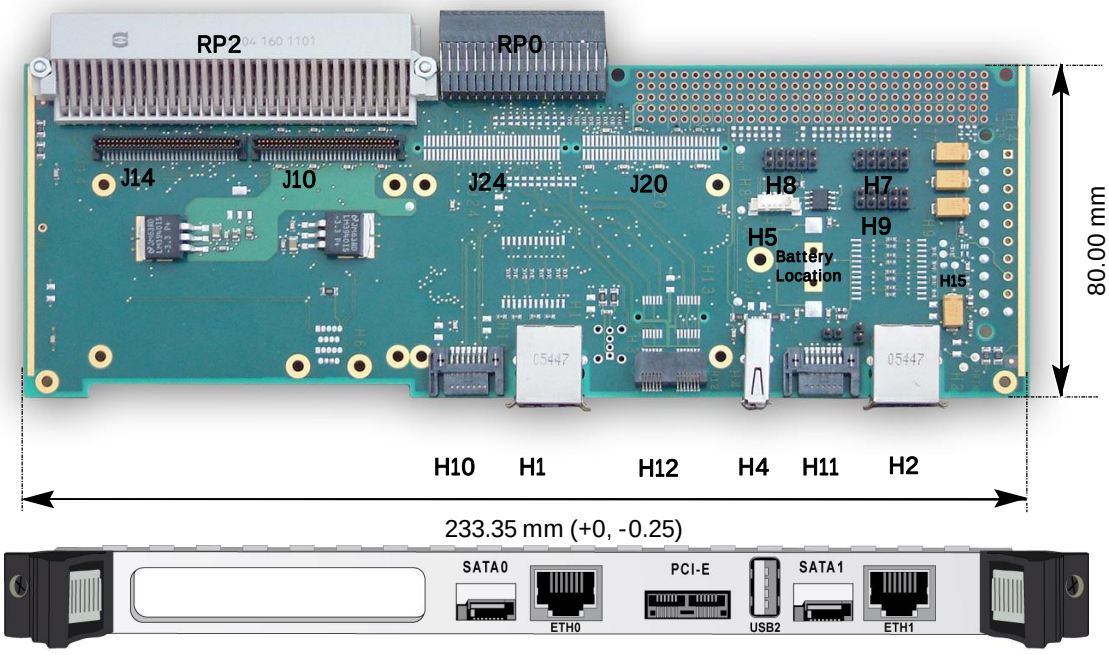
8/ VM6103-RTM Characteristics

The RTM (Order Code: PBV36-P0-VM6-00 rear transition module is compliant to PMC I/O Module Standard VITA 36 - 199x Draft 0.1 July 19, 1999 (mechanical and PIM format).

The main functionalities of the rear transition module are:

- Two 10/100/1000BASE-T Ethernet interface, H1 and H2 connectors on Figure 44
- One USB connector, H4 on Figure 45
- One SMB connector, H5 on Figure 45
- Two Serial lines ports available on two HE10 connectors (H7, H8 on Figure 44)
- Three GPIOs signals available through an HE10 connector, H9 connector on Figure 44
- Two Serial ATA connectors, H10 and H11 connector on Figure 45
- One PCI Express connector, H12 connector on Figure 45
- PMC Site 1[64:1] I/O routed to J14[32:1] connector from RP2 connector
- PMC Site 2[64:1] I/O routed to J24[32:1] connector from RP2 connector (only on PBV36-P0-VM6-00 Rev. C)

Figure 41: VX305x-SA 3U VPX Overview



8.1. Installation of the Rear Transition Module

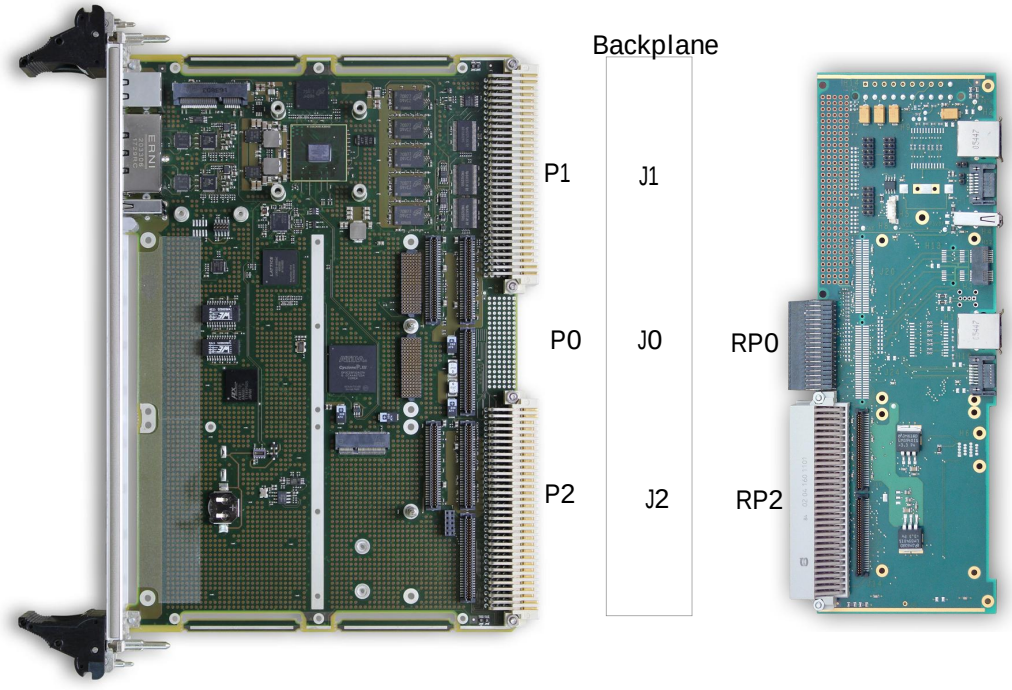
The RTM module is designed to be used with a VME64 extensions backplane. Each slot in the backplane contains two 160-pin connectors and one connector with 95 user-defined pins. The top connector in each slot is designed J1, the middle connector is J0 and the bottom connector is J2.

The VM6103 rear transition module plugs into the J0, J1 and J2 connectors, on the back side of the VMEbus backplane, in the same slot as the VM6103 board (see Figure 42).

To install the rear transition module:

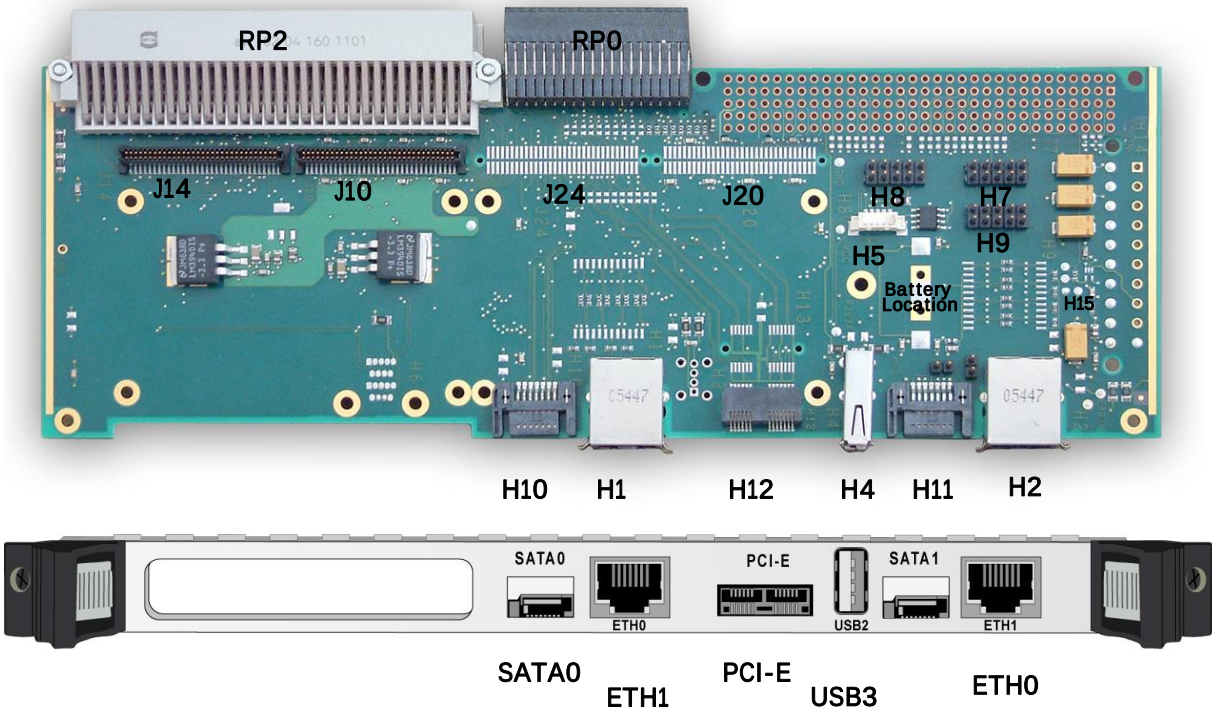
1. Make sure the system and peripheral equipment power are off.
2. Install the cables into the appropriate connectors on the transition module (see section 8.2 page 112).
3. Line-up the RP0 and RP2 connectors (also named P0 and P2 in this chapter) on the rear transition module with the J0 and J2 connectors on the backplane.
4. Press the outer edge of the transition module until the board is firmly seated in the connector.
5. Connect any additional cables.
6. Turn on system power.

Figure 42: Installing the VM6103-RTM



8.2. Connectors

Figure 43: RTM Connectors Location



8.2.1. RP0 Connector Pin Assignment

The RP0 connector has the same pin assignment as the P0 connector of the VM6103 board.

Refer to the “VME Bus Interface - P0 Connector" in section 4.3.1 page 72 for a complete information about the pin assignments of the RP0 connector.

8.2.2. RP2 Connector Pin Assignment

The RP2 connector has the same pin assignment as the P2 connector of the VM6103 board.

Refer to the “VME Bus Interface - P2 Connector" in section 4.3.3 page 78 for a complete information about the pin assignments of the RP2 connector.

8.2.3. H1 (ETHERNET 1) & H2 (ETHERNET 0) - Gigabit ETHERNET Connector

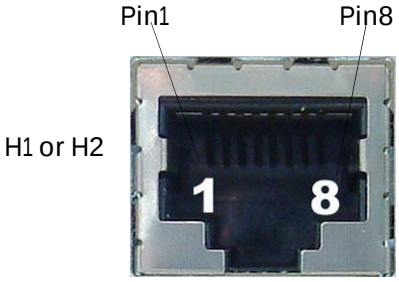
Routed from P0 to **H1** and **H2**, RJ-45 connectors (AMP - Part Number 106066-2).
Ethernet port 1 and 0 are respectively available through the **ETH0** and **ETH1** RTM front panel connectors.

Connector Pin Assignmen

PIN	SIGNAL	PIN	SIGNAL
1	BI_DA+	2	BI_DA-
3	BI_DB+	4	BI_DC+ (*)
5	BI_DC- (*)	6	BI_DB-
7	BI_DD+ (*)	8	BI_DD- (*)
9	Chassis Ground		

(*) : In 10BASE-T or 100BASE-T these signals are not used.

Type of Connector



Signal Description

MNEMONIC	SIGNAL DESCRIPTION
BI_DA+/-	In 1000BASE-T: First pair of Transmit/receive data In 10BASE-T/100BASE-T: Pair of Transmit data
BI_DB+/-	In 1000BASE-T: Second pair of Transmit/receive data In 10BASE-T/100BASE-T: Pair of Receive data
BI_DC+/-	In 1000BASE-T: Third pair of Transmit/receive data In 10BASE-T/100BASE-T: Unused.
BI_DD+/-	In 1000BASE-T: Fourth pair of Transmit/receive data In 10BASE-T/100BASE-T: Unused.

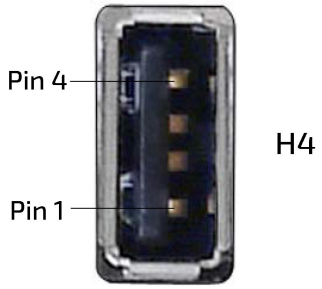
8.2.4. H4 (USB3) - USB Connector

Routed from P0 to H4, a vertical USB connector.
Available through the USB RTM front panel connectors.

Connector Pin Assignment

PIN	SIGNAL
1	+5 V Fused
2	USB3 DATA-
3	USB3 DATA+
4	GND
CASE	M GND

Type of Connector



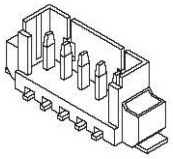
8.2.5. H5 - SMB Connector

Routed from P1 to H5 (MOLEX - Part Number 53398-0590)

Connector Pin Assignment

PIN	SIGNAL
1	SMB_SCL
2	GND
3	SMB_SDA
4	N.C.
5	SMB_ALERT#

Type of Connector



H5

Signal Description

MNEMONIC	SIGNAL DESCRIPTION
GND	Ground
N.C.	Not Connected
SMB_ALERT	System Management Bus - Alert
SMB_SCL	System Management Bus - Serial clock line from the SMBus master to SMBus slave devices.
SMB_SDA	System Management Bus - Bi-directional serial data line between the SMBus master and the SMBus slave device.

8.2.6. H7 & H8 SERIAL Connectors

Routed from P2 to H7 and H8; individual 10-pin HE10 connectors

A serial line should only be used via one connector at the same time, either the Serial front panel connector or the P2 connector.

H7 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	N.C.	2	S1_RX
3	S1_TX	4	N.C.
5	GND	6	N.C.
7	S3_TX or S1_RTS	8	S3_RX or S1_CTS
9	N.C.	10	N.C.

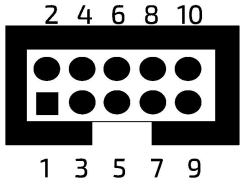
H8 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	GPIO4	2	S2_RX
3	S2_TX	4	GPIO6
5	GND	6	GPIO5
7	S4_TX or S2_RTS	8	S4_RX or S2_CTS
9	N.C.	10	N.C.

COM3 and COM4 are the default settings. Handshaking on COM1 and COM2 can be set from u-boot command.

Type of Connector

Right angle HE10 10-pin connector, male, with board lock.



H7 & H8

The H7 and H8 connectors can be connected via a NULL MODEM adapter on a VT100 console.

8.2.7. H9 - GPIOs and MISC Signals

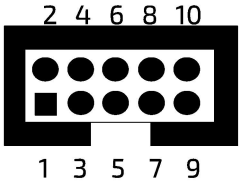
Routed from P0 to H9; individual 10 pins HE10 connector.

Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	GPIO1	2	N.C.
3	GPIO2	4	N.C.
5	GPIO3	6	N.C.
7	N.C.	8	GND
9	N.C.	10	GND

Type of Connector

Right angle HE10 10-pin connector, male, with board lock.



H9

Signal Meaning

MNEMONIC	SIGNAL DESCRIPTION
GPIO*x*	GPIO *x* from cPLD
GND	Ground
N.C.	Not Connected

8.2.8. H10 (SATA0) and H11 (SATA1) - Serial ATA Connector

Routed from P0 to H10 and H11; SATA connector, right angle version with metal latch (MOLEX - Part Number 47080-4001)

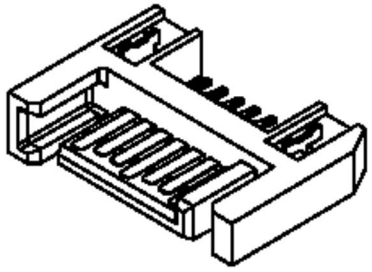
Available through the SATA0 and SATA1 RTM front panel connectors.

Only one SATA port is available through the SATA0 RTM front panel connectors on VM6103 board. Depending on build option.

Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	SATA*x* TX+
3	SATA*x* TX-	4	GND
5	SATA*x* RX-	6	SATA*x* RX+
7	GND		

Type of Connector



Signal Description

MNEMONIC	SIGNAL DESCRIPTION
GND	Ground
SATA*x* RX+/RX-	Serial ATA *x* Receive +/-
SATA*x* TX+/TX-	Serial ATA *x* Transmit +/-

8.2.9. H12 - PCI Express Connector

No PCIe available on VM6103 board.

8.2.10. PCI 64 PIM Site 1 Connector

J14 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	PMC64 IO 01	2	PMC64 IO 02
...		...	
61	PMC64 IO 61	62	PMC64 IO 62
63	PMC64 IO 63 or GPIO7 (*)	64	PMC64 IO 64 or GPIO8 (*)

(*) depending on VM6103 build option.

Signal Description

MNEMONIC	SIGNAL DESCRIPTION
PMC64 IO *xx*	I/O 01 through 64 of the motherboard PMC: J14[01 ... 64] for PMC Site 1
GPIOx	GPIOx from CPLD
N.C.	Not Connected

Known Limitations

- 4.8 mm height components have been placed under PIM site 1. This transgresses the VITA 36 standard which specifies 2.5 mm. Some PIMs may not fit in this site.

J10 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	N.C.	2	N.C.
3	N.C.	4	N.C.
5	+5 V	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	+3.3 V
11	N.C.	12	N.C.
13	GND	14	N.C.
15	N.C.	16	N.C.
17	N.C.	18	GND
19	N.C.	20	N.C.
21	+5 V	22	N.C.
23	N.C.	24	N.C.
25	N.C.	26	+3.3 V
27	N.C.	28	N.C.
29	GND	30	N.C.
31	N.C.	32	N.C.
33	N.C.	34	GND
35	N.C.	36	N.C.
37	-5 V	38	N.C.
39	N.C.	40	N.C.
41	N.C.	42	+3.3 V
43	N.C.	44	N.C.
45	GND	46	N.C.
47	N.C.	48	N.C.
49	N.C.	50	GND
51	N.C.	52	N.C.
53	-5 V	54	N.C.
55	N.C.	56	N.C.
57	N.C.	58	+3.3 V
59	N.C.	60	N.C.
61	N.C.	32	N.C.
63	N.C.	64	N.C.

8.2.11. PCI 64 PIM Site 2 Connector

Installation of a PIM on the Site 2 of a PBV36-P0-VM6-00 Rev C. requires specific adjustments:

- removing H10 (SATA0), H1 (ETH1) and H12 (PCI-E) connector on the RTM,
- usage of a RTM specific front panel.

Contact your Kontron representative for more information on this topic.

J24 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	PMC64 IO 01	2	PMC64 IO 02
...		...	
63	PMC64 IO 63	64	PMC64 IO 64

Signal Description

MNEMONIC	SIGNAL DESCRIPTION
PMC64 IO *xx*	I/O 01 through 64 of the motherboard PMC: J14[01 ... 64] for PMC Site 2
N.C.	Not Connected

Known Limitations

- The RTM does not include the 3 mm recess at the rear card edge on the area of PIM Site as required by VITA 36 standard. This may require removal or loosening of the rear panel in order to remove and install a PIM at Site 2.

J20 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	N.C.	2	N.C.
3	N.C.	4	N.C.
5	+5 V	6	N.C.
7	N.C.	8	N.C.
9	N.C.	10	+3.3 V
11	N.C.	12	N.C.
13	GND	14	N.C.
15	N.C.	16	N.C.
17	N.C.	18	GND
19	N.C.	20	N.C.
21	+5 V	22	N.C.
23	N.C.	24	N.C.
25	N.C.	26	+3.3 V
27	N.C.	28	N.C.
29	GND	30	N.C.
31	N.C.	32	N.C.
33	N.C.	34	GND
35	N.C.	36	N.C.
37	-5 V	38	N.C.
39	N.C.	40	N.C.
41	N.C.	42	+3.3 V
43	N.C.	44	N.C.
45	GND	46	N.C.
47	N.C.	48	N.C.
49	N.C.	50	GND
51	N.C.	52	N.C.
53	-5 V	54	N.C.
55	N.C.	56	N.C.
57	N.C.	58	+3.3 V
59	N.C.	60	N.C.
61	N.C.	32	N.C.
63	N.C.	64	N.C.

8.2.12. Reset

The front panel reset toggle switch can be set to the RESET position to generate an hard reset.

8.2.13. Mechanical Ground

One HE10 2-pin connector is placed on the board to allow to hard connect electrical (GND) and mechanical (EARTH) grounds.

While adding a jumper on connector, both ground signals are tighten together.

H15 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	EARTH	2	GND

Signal Meaning

MNEMONIC	SIGNAL DESCRIPTION
EARTH	Electrical Ground
GND	Mechanical Ground

A metalized mechanical hole (3mm diameter) is located on the board to allow to fix an electrical pod in order to bring the mechanical ground from the chassis.

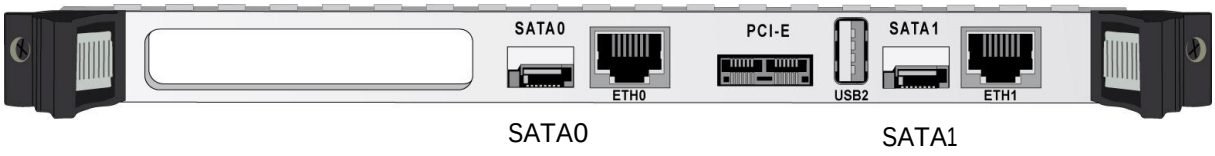
8.2.14. Power Supplies

- Two 800 mAmp voltage regulators are used on the board to provide 3.3V power supply to each PIM site.
- A standard lithium battery to supply CPU board's RTC is also available on customer request.

8.3. Cables

8.3.1. SATA Cable

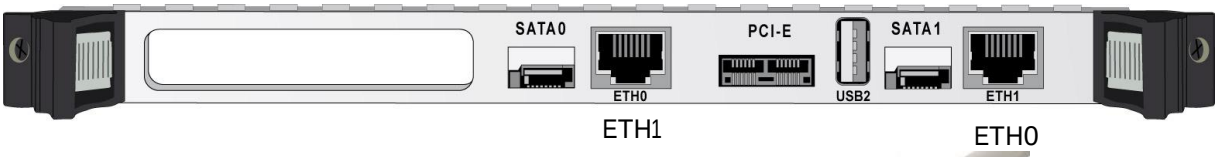
Figure 44: Serial ATA Cable



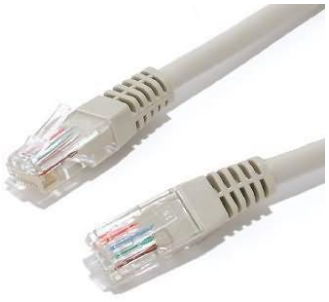
Serial ATA standard cable

8.3.2. Ethernet Cable

Figure 45: Gigabit Ethernet Cable

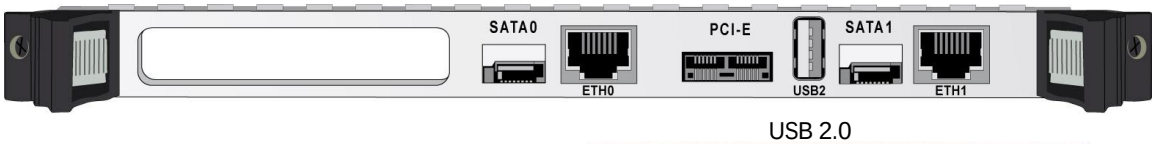


Gigabit Ethernet standard cable:
1000BASE-T requires category 5e, 5+ or 6 copper cable, with a maximal length of 100m for an UTP or FTP cable, and 150m for a STP or FSTP cable.

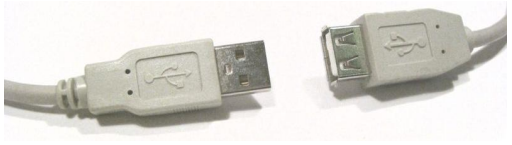


8.3.3. USB 2.0 Cable

Figure 46: USB 2.0 Cable



USB 2.0 standard cable



USB series “A" plug and receptacle

About Kontron – An S&T Company

Kontron is a global leader in IoT/Embedded computing technology (ECT). As a part of technology group S&T, Kontron offers a combined portfolio of secure hardware, middleware and services for Internet of Things (IoT) and Industry 4.0 applications. With its standard products and tailor-made solutions based on highly reliable state-of-the-art embedded technologies, Kontron provides secure and innovative applications for a variety of industries. As a result, customers benefit from accelerated time-to-market, reduced total cost of ownership, product longevity and the best fully integrated applications overall.

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