Kontron HARTMANN-WIENER VPX360DMS

3U / 5HP / 600W

SOSA aligned VPX Power Supply

Manual

General Remarks

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1 General Description

The Kontron HARTMANN-WIENER VPX360DMS is a COTS, single stage, wide range 28V to 48V DC input voltage based, conduction cooled VPX power supply with 600W output power. Being aligned to the SOSA™standard it offers a 12V cintric output power configuration while matching the ANSI/VITA 62.0 specification. The power supply can be used to power a SOSA™ 3U VPX chassis and will fit into the standard envelope defined by VITA 46.0 specifications.

High efficiency and wide input voltage range is achieved by using state of the art switching power technology. No wet electrolytic capacitors are used. An embedded microprocessor allows monitoring and control via two independent I^2C communication with VITA 46.11 conform intelligent power-

management interface (IPMI 2.0).

The 600W VPX power supply mechanical dimensions are 3U x 5HP (1.0" slot). It is outfitted with connectors, keying and alignment mechanism as per VITA 62.

The VPX360DMS is designed in compliance with relevant MIL STD 461, 704 and 1275.

1.1 Overview

1.2 Functional description

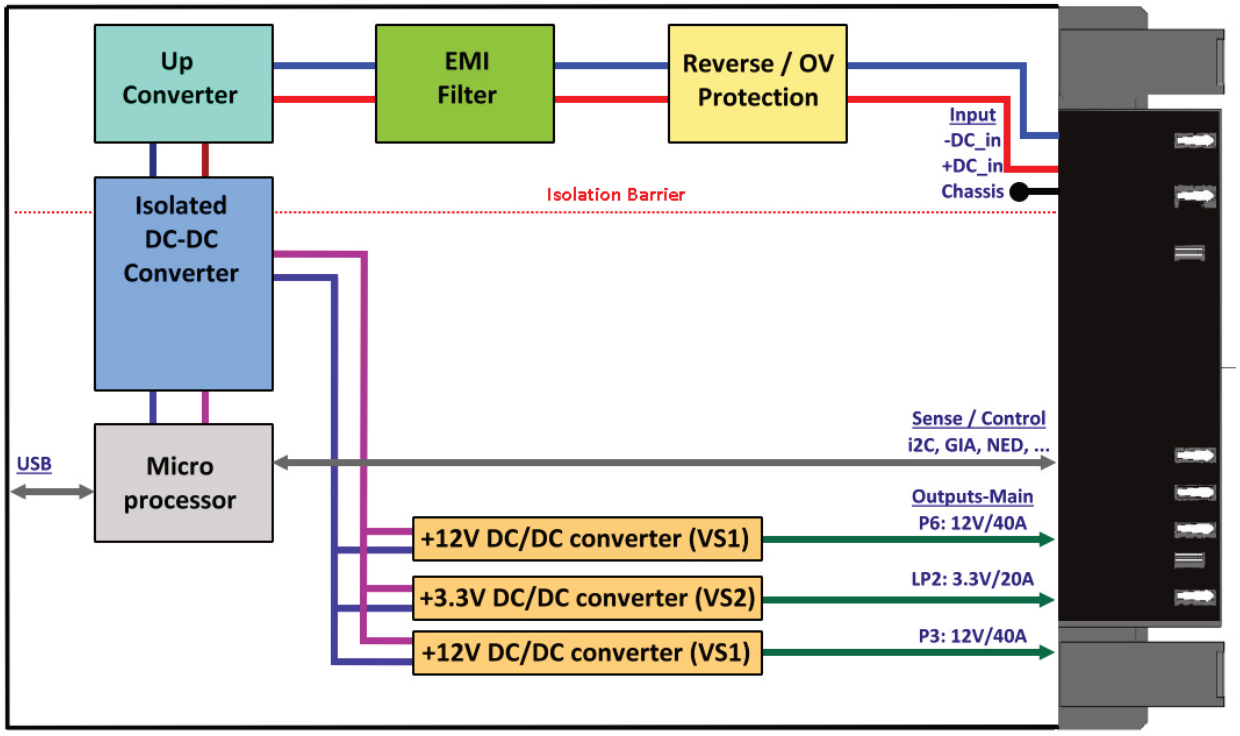


Figure 1: VPX-360DMS Block-Diagram

WARNING: VPX360DMS is a conduction cooled power supply intended to be used with a wedge-lock heat sink and VITA 62 backplane. Failure to properly regulate wedge-lock temperature within the specified limits may result in damage to the power supply.

NOTICE: VITA 62 (4.6.3.12) systems support Remote Sense & Sense Return Pins that are used to accommodate for power distribution losses (i.e. voltage drops across the connector and PCB traces). VPX360DMS contains three sense lines (12V, 12V, 3.3V_aux) and one sense return line (SENSE_RETURN) that require connection to the backplane in order provide point of load voltage regulation. The connection is typically provided through a jumper (e.g. 0Ω resistor) located on the backplane. Refer to backplane documentation to ensure the necessary sense and sense return jumpers are installed.

NOTICE: VITA 62 (4.6.3.10) systems support a Signal Return Pin (SIGNAL_RETURN) that is used as the return path for digital signals distributed across the backplane. VPX360DMA requires SIGNAL_RETURN to be connected to the backplane's ground plane. This connection is typically provided through a jumper (e.g. 0Ω resistor) located on the backplane. Refer to backplane documentation to ensure SIGNAL_RETURN jumper is installed.

Figure 1.1: Block Diagram of VPX360DMS and VITA 62 Power Backplane. VPX360DMS requires PO1_SENSE, PO2_SENSE, PO3_SENSE, SENSE_RETURN, & SIGNAL RETURN to be terminated on the VITA 62 Power Backplane. Further both 12V sense lines (PO1_SENSE and PO3_SENSE) need to be connected to each other (red line on power backplane)! Verify that these connections are made on your VPX Power Backplane.

RECOMMENDATION: VPX360DMS has been successfully tested and deployed with VITA46/62 VPX Power Backplanes and conduction cooled chassis manufactured by Hartmann Electronics.
Hartmann Electronics has over 35 years of experience designing high-speed backplanes, please see:

https://www.hartmann-electronic.com/

Support for power supply specific signals: ENABLE*, INHIBIT*, FAIL* and UD (user defined) signals. These input/output signals are low current open collector circuits with electrical characteristics defined per VITA 46 section 4.8.12.1.

NOTICE: NED (C3), NED_RETURN (D3), UD2-4 (B1, C1, D1), SM2-3 (A6, B6), VBAT (A2), & PO1-3_SHARE (A7, B7, C7) are open circuit/no connection on VPX360DMS.

Control Inputs		Power Outputs	
ENABLE*	INHIBIT*	3.3V_AUX	PO1, PO2, PO3, +12V_AUX, and -12V_AUX
High	High	Off	Off
High	Low	Off	Off
Low	High	On	On
Low	Low	On	Off

Communication interface: I^2C communication interface via SM0 (C5) and SM1 (D5). Additional I^2C connection at UD0 (A1) and UD1 (B1) is set by internal jumper (can be removed by factory).

Communication Features (see paragraph 4):

- Remote On / Off
- DC-IN status and measured voltage and current

- Global status, Temperatures
- Voltage, current and status of individual output power modules

2 Specifications

2.1 Standard Input Voltage Specification

+28 V or 48V DC nominal, 12 V … 70 V DC input range

UV lockout at 8 V

Outfitted with Reverse Polarity Protection

2.2 Output Voltage, Current & Power Specification

VPX standard outputs as per VITA 62, different power configurations are possible:

VPX360DMA

VPX360DMA	Voltage	Current	Power
VS1	+12.00 V	30 A	360 W
VS1 (on P3)	+12.00 V	30 A	360 W
VS2	+3.30 V	20 A	66 W
Total max			**600W**

Maximum output power: limited to 600 W

Noise and ripple (PARD) as per VITA 62 specification:

+3.3 V: 50 mV, see [VITA 46.0] Rule 3-6 / 3-9]

+12 V: <120 mV peak-to-peak, measured over a range of 0 to 20 MHz.

Input to Output Insulation: 500 V

Overall Efficiency: ~85% …92% (dependent on output power distribution),
~88% at full load of 600W with power distributed across all outputs.

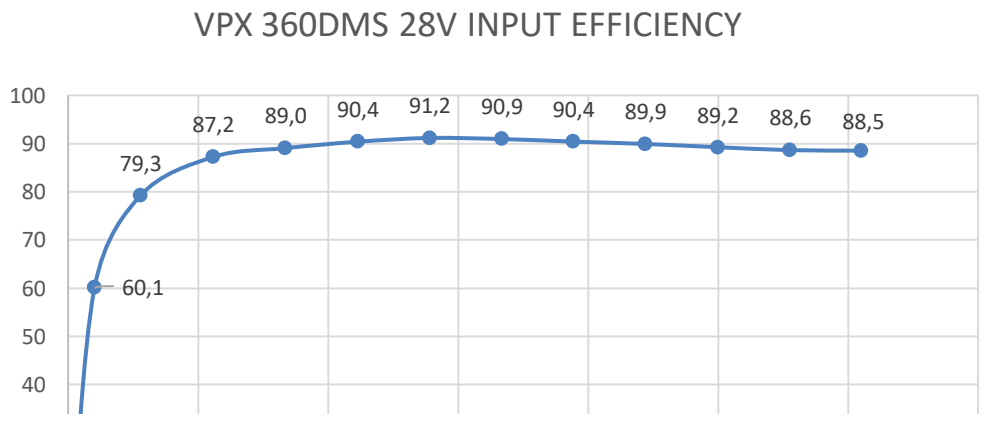


Figure 2: VPX-360DMS Efficiency versus Output Power for VITA 62 nominal input voltage 28V.
VPX360DMA is designed to operate with input voltage 28V DC or 48V DC.
Efficiency curve was generated from empirical data with power distributed across PO1, PO2, & PO3 outputs. (preliminary)

2.3 Technical Specification Table

Form Factor	*3U VPX CC*
Pitch	*5HP / 1.0 inch*
Weight	*0.82 kg / 1.8 Lbs*
Storage Temperature	*-55 °C to 105 °C*
Operating Temperature	*-40 °C to 85 °C (Operating Temperature is referenced at wedge-lock. Failure to regulate wedge-lock temperature may result in damage)*
Input to Output Insulation	*500 V*
Input to Case Ground Isolation	*500 V*
Output to Case Ground Isolation	*500 V*
Maximum Output Power	*600 W*
Maximum Input Power	*~660 W*
Maximum Dissipated Power @ max. Power	*~60 W*
Minimum Turn ON Voltage	*12 V*
Minimum Turn OFF Voltage	*8 V*
Maximum Continuous/Peak Input Voltage	*70 V / ± 250 V (<1 ms spike)*
Input Overvoltage Protection:	*Outputs disable if input voltage exceeds 70 VDC for > 600 ms (10 second auto-restart)*
Temperature Protection Sensing Point (internal)	*125 °C (Outputs disable when internal PCB temperature exceeds threshold)*
Maximum Internal Working Temperatures	*125 °C*

Case Ground to Safety Ground Resistance	*< 10 mΩ (preliminary)*
Maximum Input Line Inductance	*10µH (preliminary)*

Main Power

Maximum Currents 12V / 3V3	*60 A / 20 A*
Fixed Switching Frequencies 12V / 3V3	*520 kHz / 520 kHz*
Peak Efficiencies 12V / 3V3	*93% / 82%*
Max. Output Ripple and Noise: 12V / 3V3	*<120 mVpp / <50 mVpp*
(0-20 MHz Bandwidth)	*Typical < 30 mVpp / <25 mVpp*
Line Regulation: 12V / 3V3	*<10 mV / <10 mV*
Vin=Vin,min to Vin,max, Io and Tc fixed	*< 0.1%*
Load Regulation: 12V / 3V3	*<10 mV / <10 mV*
Maximum output voltage (sense lines open)	*12.0 V / 3.3 V*
Load Transient Recovery Time (no load to full load change condition)	*~1 ms*

2.4 MIL STD 810 (Shock / Vibe / Ambient Temperature / Environment)

Ruggedized construction to meet shock and vibration requirements, levels to be specified and tested on request.

Storage Temperature: -55 °C to 105 °C

Operating Temperature: -40 °C to 85 °C *(derating to be defined)*

Standard acrylic conformal coating (e.g. HumiSeal Type 1B31 or similar) to withstand sand, dust and salt atmosphere. Alternate conformal coating options as for instance Parylene are available upon request.

2.5 MIL-STD-461F (EMI) Compliance

Designed to be in compliance with sections CE102, CS101, CS114, CS115, CS116. **Compliance tests to be performed**.

EMC STANDARD:	TEST CONDITIONS: LINE, LOAD, EXTERNAL FILTER	RESULT:
MIL-STD-461F CE102	Input Voltage = 28V, Output Power = 600W, No external filter needed	
MIL-STD-461F CS101	Input Voltage = 28V, Output Power = 40W, No external filter needed	
MIL-STD-461F CS114	Input Voltage = 28V, Output Power = 600W, No external filter needed	
MIL-STD-461F CS115	Input Voltage = 28V, Output Power = 600W, No external filter needed	
MIL-STD-461F CS116	Input Voltage = 28V, Output Power = 600W, No external filter needed	

2.6 MIL-STD-704 Compliance

Designed to be in compliance for normal and abnormal transients and distortion spectrum. External hold-up circuit optional. **Compliance tests to be performed**.

EMC STANDARD:	TEST CONDITIONS: LINE, LOAD, EXTERNAL FILTER	RESULT:
MIL-STD-704F LDC105 Normal Voltage Transients	Input Voltage = 28V, Output Power = 192W, No external filter needed	
MIL-STD-704F LDC302 Abnormal Voltage Transients	Input Voltage = 28V, Output Power = 192W, No external filter needed	
MIL-STD-704F LDC103 Voltage Distortion Spectrum	Input Voltage = 28V, Output Power = 192W, No external filter needed	

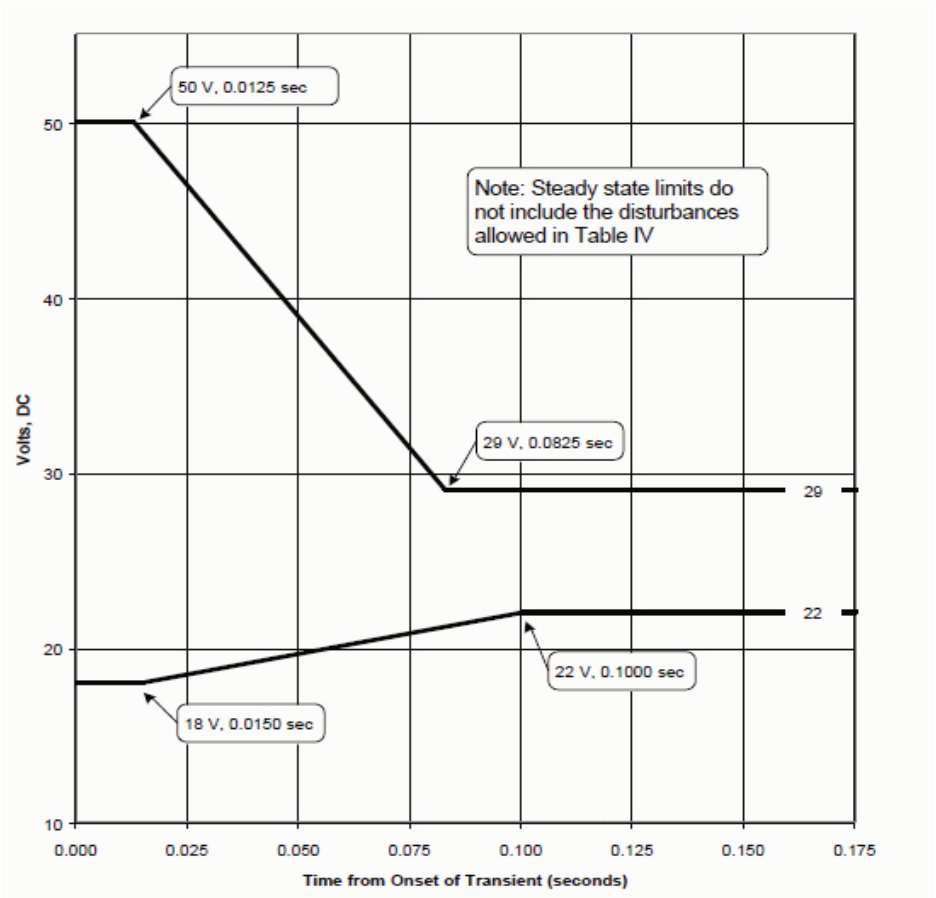


Figure 4: *MIL-STD-704F Envelope for normal voltage transients for 28 VDC Systems*

2.7 MIL-STD-1275D Compliance

Designed to be in compliance for ripple, surge, & spikes. **Compliance tests to be performed**.

EMC STANDARD:	**TEST CONDITIONS: LINE, LOAD, EXTERNAL FILTER**	**RESULT:**
MIL-STD-1275D 5.3.2.2 Exported Voltage Spikes	Input Voltage = 28V, Output Power = 600W, No external filter needed	
MIL-STD-1275D 5.3.2.3 Imported Voltage Spikes	Input Voltage = 28V, Output Power = 600W, No external filter needed, Normal Mode & Generator Mode	
MIL-STD-1275D 5.3.2.4 Imported Voltage Surges	Input Voltage = 28V, Output Power = 600W, No external filter needed, Normal Mode & Generator Mode	
MIL-STD-1275D 5.3.2.5 Imported Ripple Voltage	Input Voltage = 28V, Output Power = 40W, No external filter needed	

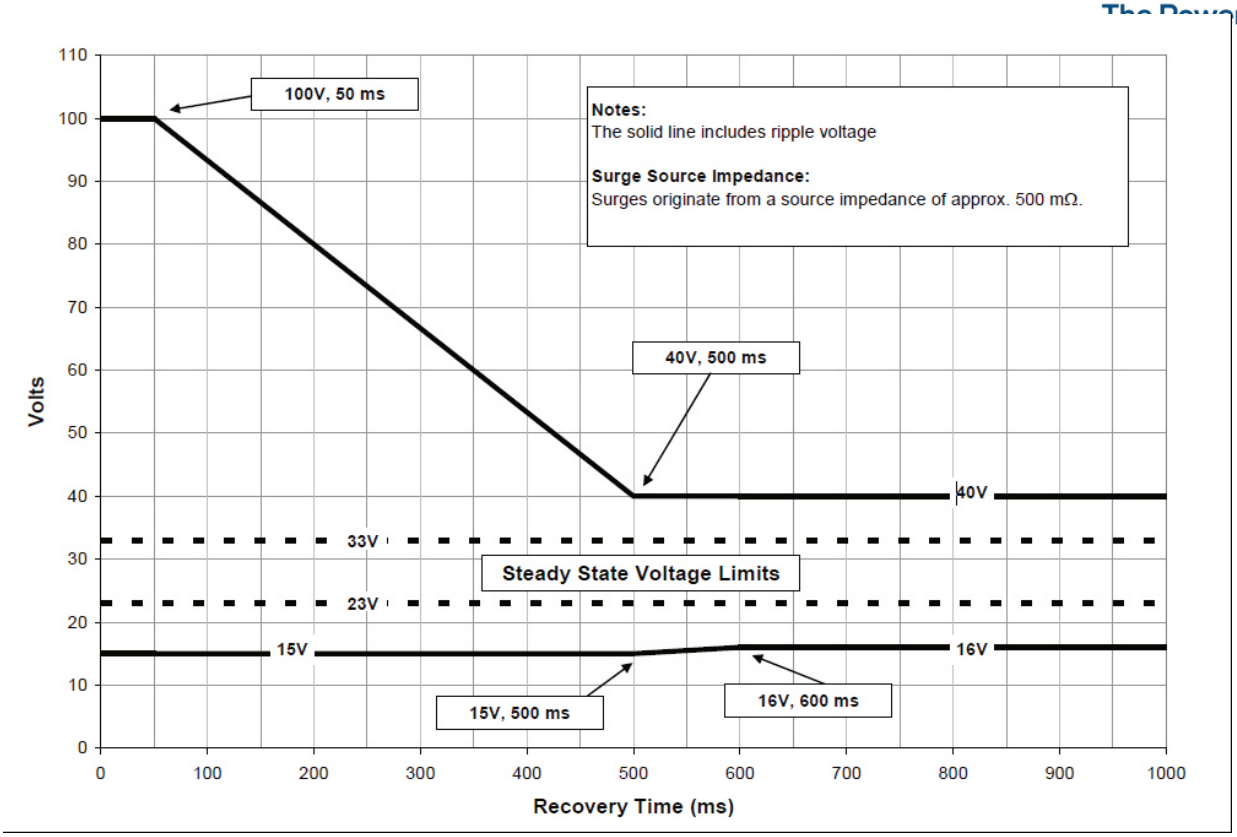


Figure 5: *MIL-STD-1275D Envelope of surges in Generator-only Mode for 28 VDC Systems.*

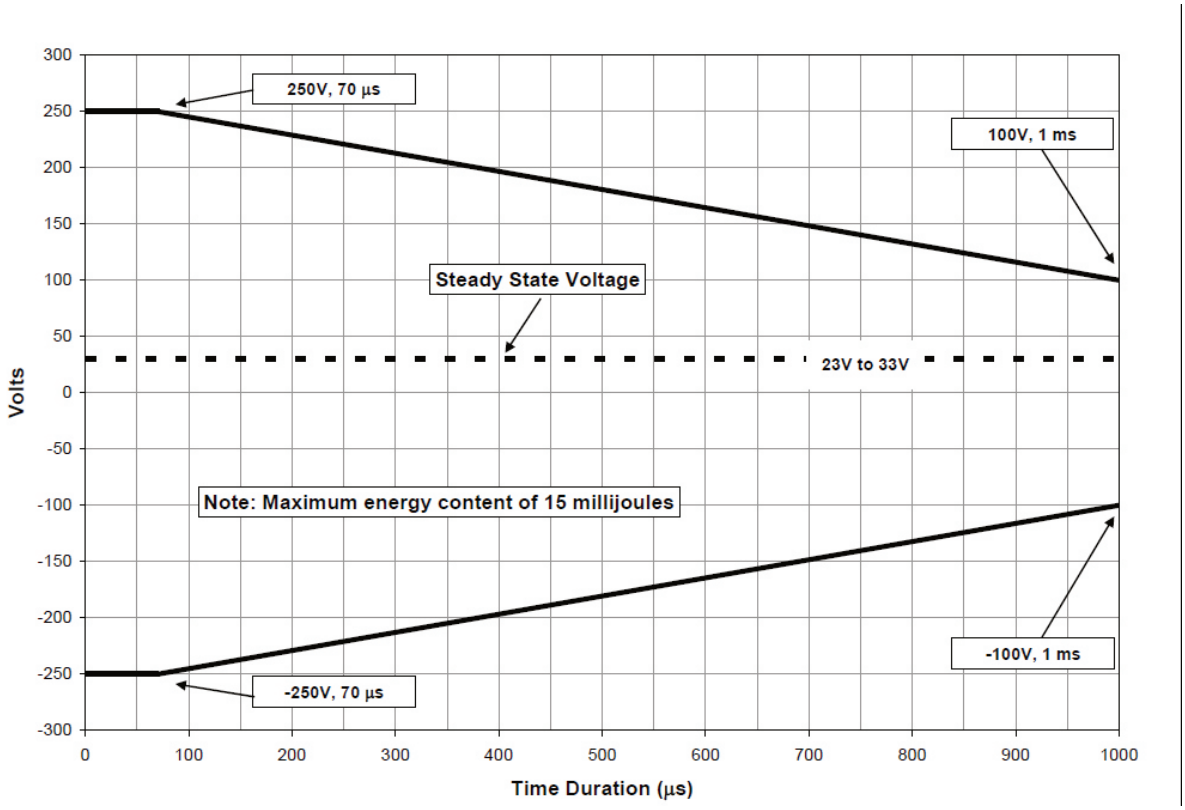
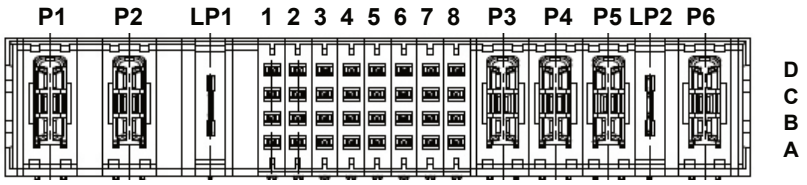


Figure 6: *MIL-STD-1275D Envelope of spikes in Generator-only Mode for 28 VDC Systems.*

2.8 P0 Connector Pin-Layout (as per VITA62)

P0 (3U)	TE Connectivity	Foxconn
Power Supply	6450849-7	HM811C3-B84F
Backplane	1-6450869-4	HM826B3-B64F



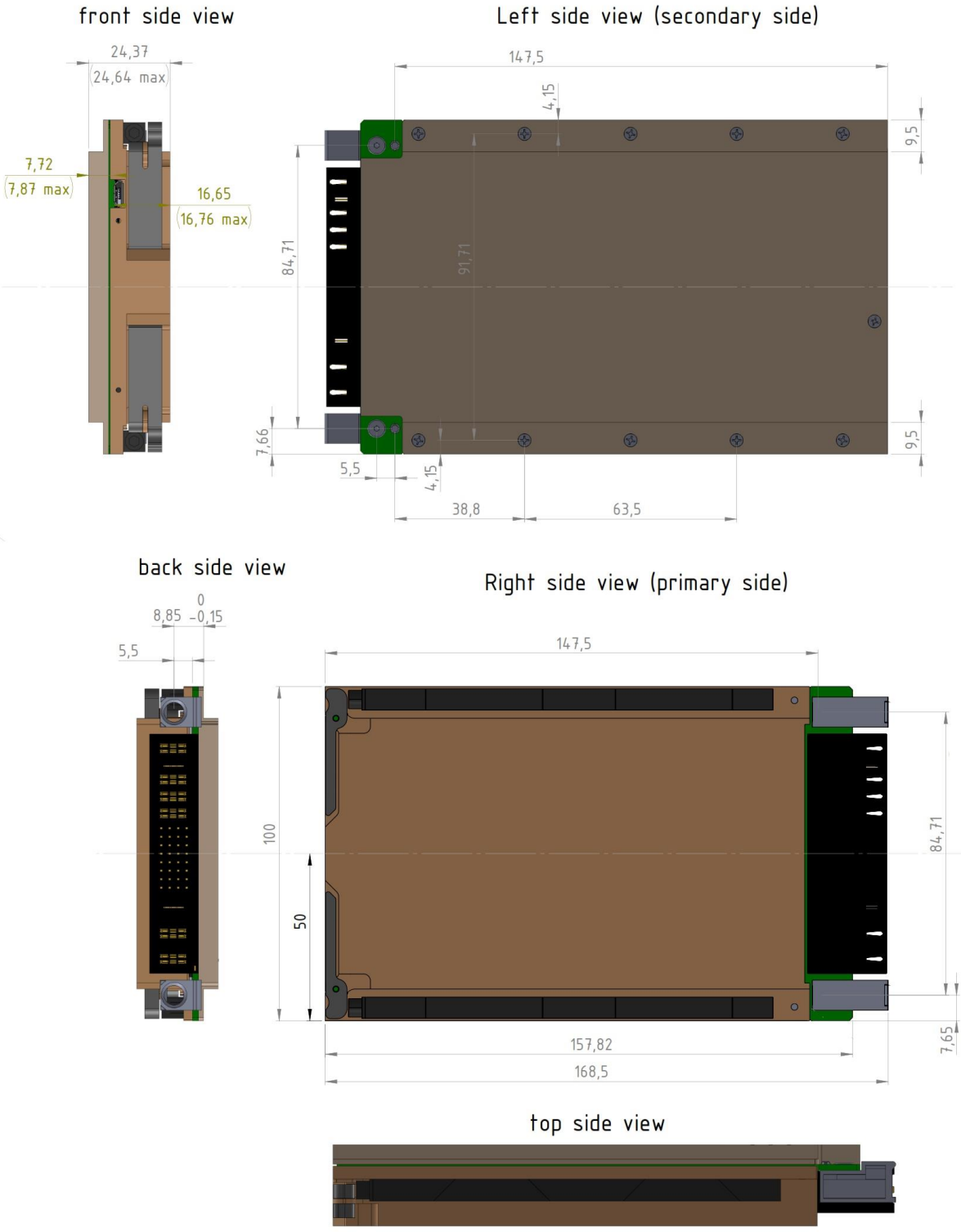
Pin Number	Rated Current (A)	Pin Name
P1	40A	- DC_IN
P2	40A	+ DC_IN
LP1	20A	CHASSIS
A1	<1A	SYNC_OUT
B1	<1A	NVMRO
C1	<1A	GA2*
D1	<1A	Reserved
A2	<1A	VBAT
B2	<1A	FAIL*
C2	<1A	INHIBIT*
D2	<1A	ENABLE*
A3	<1A	UD0: SYNC_IN
B3	<1.5A	Reserved
C3	<1A	NED
D3	<1A	NED_RETURN
A4	<1.5A	Reserved
B4	<1.5A	Reserved
C4	<1.5A	Reserved
D4	<1.5A	Reserved
A5	<1A	GA0*
B5	<1A	GA1*
C5	<1A	SM0
D5	<1A	SM1
A6	<1A	SM2
B6	<1A	SM3
C6	<1.5A	Reserved
D6	<1A	SYSRESET*
A7	<1A	PO1_SHARE (VS1)
B7	<1A	PO2_SHARE (VS2)
C7	<1A	PO3_SHARE (VS3)
D7	<1A	SIGNAL_RETURN
A8	<1A	PO1_SENSE +12VDC (VS1)
B8	<1A	PO2_SENSE +3.3V_AUX
C8	<1A	PO3_SENSE 12VDC (VS3)
D8	<1A	SENSE_RETURN
P3	40A	PO3: +12VDC (VS1)
P4	40A	POWER_RETURN
P5	40A	POWER_RETURN
LP2	20A	PO2: +3.3V_AUX
P6	40A	PO1: +12VDC (VS1)

2.9 USB Connector & LED Status Indicator

VPX360DMS is outfitted with a USB-C 2.0 connector. This interface enables communication with a Windows PC running User Software. See section 4.5 of this manual for details on User Software.

VPX360DMS is equipped with a multi-color LED Status Indicator: Flashing GREEN LED indicates that the firmware is running. Solid BLUE LED indicates that the VITA 62 ENABLE* Switch is active (i.e. all outputs are energized). Normal operation is a flashing GREEN LED & Solid BLUE LED on (when ENABLE* active). Contact Kontron HARTMANN-WIENER for support if LED Status indicates otherwise.

3 Mechanical Layout



NOTICE: VPX360DMA is a VITA 62 “1.0 PITCH 3U CONDUCTION COOLED PLUG-IN MODULE”. See VITA 62 FIGURE A-2 “3U Conduction Cooled Module Layout” for additional mechanical details.

4 I2C Documentation Version 1.2

4.1 Device Setup

- 7-Bit Addressing
- Slave Mode
- Address Auto Increment

4.2 I2C Device Address Byte

Accessing the device requires an 8-bit Device Address word following a Start condition to enable the device for a Read or Write operation. Since multiple slave devices can reside on the serial bus, each slave device must have its own unique address so the Master can access each device independently. The most significant four bits of the Device Address word is referred to as the device type identifier. The device type identifier '11001' is required in bits seven through three of the Device Address byte. Following the 2-bit Hardware Slave Address Bits GA1* (Pin B5) and GA0* (Pin A5). GA1* and GA0 both have an internal pull-up resistor of 10k to VCC.

A HIGH level on these pins gives a "0" on the GA pin.

A LOW level on these pins gives a "1" on the GA pin.

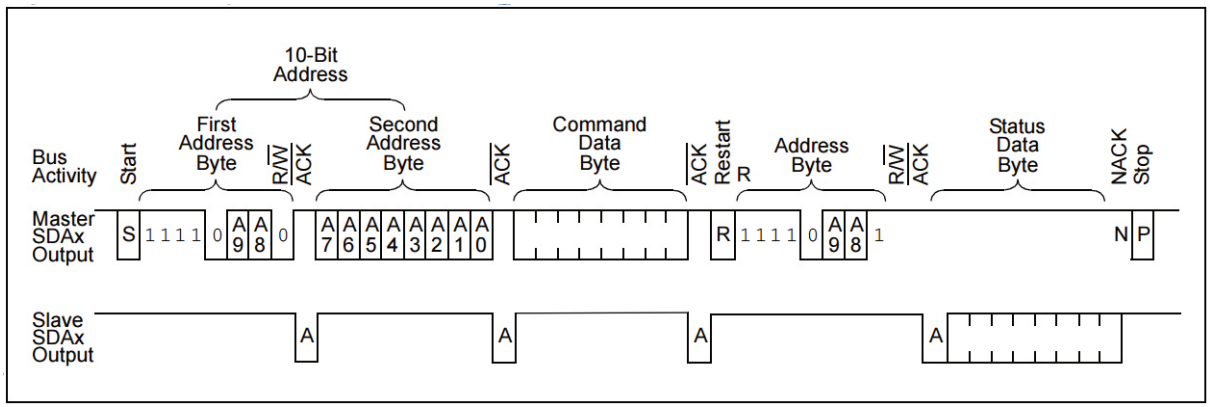
Device Type Identifier					Hardware Slave Address Bits		Read / Write
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	0	0	1	GA1	GA0	R/$\bar{W}$

4.3 Device Access

Reading the device requires a write to the desired memory address of the Slave Device followed by a Read. Since ADC Data has 16-bit values, ADC values are split in high and low bytes. The address pointer will automatically increase after one read cycle.

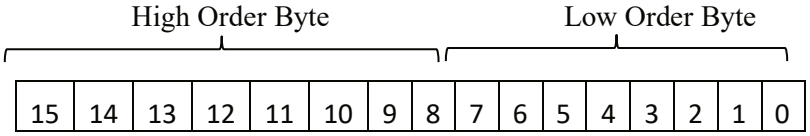
4.3.1 A Typical Slave I2C™ Message: Multiprocessor Command/Status

Note: This example uses 10-Bit Address instead of 7-Bit Address



- All Status bits are high active.

- Data size per address is 1 Byte
- All Registers are read only
- Module description :
    - Module0: **PO1:12VP** (12V Main Power)
    - Module1: **PO3:5V** (5V Main Power)
    - Module2: **PO2:3V3** (3.3V Main Power)
    - Module3: **VIN** (Input Voltage)
    - Module4: **12VN AUX** (-12V Auxiliary Voltage)
    - Module5: **3V3 Aux** (3.3V Auxiliary Voltage)
    - Module6: **12VP Aux** (+12V Auxiliary Voltage)
- All data is stored in Little Endian order



    - 16 Bit DataValue = [[High Byte][Low Byte]]

Command Data Byte	Register Name	Type	Description
0x00	PS Global Status Low Byte (Bit field)	uint8_t (Bit field)	B0: PO On B1: AUX On B2: Global Failure B3-B7: Reserved B8-B15: Reserved
0x01	PS Global Status High Byte (Bit field)		
0x02	Reserved		
0x03	Reserved		
0x04	Module 0 Status Low Byte (Bit field)	uint8_t (Bit field)	B0: Is On B1: Overvoltage B2: Undervoltage B3: Overcurrent B4: Overtemperature B5-B15: Reserved
0x05	Module 0 Status High Byte (Bit field)		
0x06	Module 0 Output Voltage Low Byte	int16_t	Calculation in [V]: U0 = DataValue / (2^11)
0x07	Module 0 Output Voltage High Byte		
0x08	Module 0 Output Current Low Byte	int16_t	Calculation in [A]: I0 = DataValue / (2^8)
0x09	Module 0 Output Current High Byte		

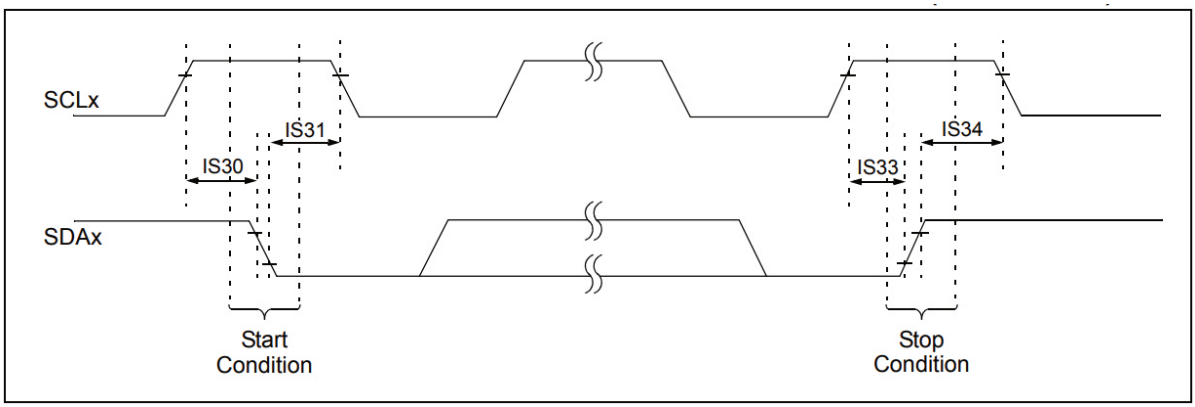
0x0A	Module 0 Temperature Low Byte	int16_t	T0 is 16bit singed integer in degree
0x0B	Module 0 Temperature High Byte		
0x0C	Module 1 Status Low Byte (Bit field)	uint8_t (Bit field)	B0: Is On B1: Overvoltage B2: Undervoltage B3: Overcurrent B4: Overtemperature B5-B15: Reserved
0x0D	Module 1 Status High Byte (Bit field)		
0x0E	Module 1 Output Voltage Low Byte	int16_t	Calculation in [V]: U1 = DataValue / (2^12)
0x0F	Module 1 Output Voltage High Byte		
0x10	Module 1 Output Current Low Byte	int16_t	Calculation in [A]: I1 = DataValue / (2^8)
0x11	Module 1 Output Current High Byte		
0x12	Module 1 Temperature Low Byte	int16_t	T1 is 16bit singed integer in degree
0x13	Module 1 Temperature High Byte		
0x14	Module 2 Status Low Byte (Bit field)	uint8_t (Bit field)	B0: Is On B1: Overvoltage B2: Undervoltage B3: Overcurrent B4: Overtemperature B5-B15: Reserved
0x15	Module 2 Status High Byte (Bit field)		
0x16	Module 2 Output Voltage Low Byte	int16_t	Calculation in [V]: U2 = DataValue / (2^12)
0x17	Module 2 Output Voltage High Byte		
0x18	Module 2 Output Current Low Byte	int16_t	Calculation in [A]: I2 = DataValue / (2^9)
0x19	Module 2 Output Current High Byte		
0x1A	Module 2 Temperature Low Byte	int16_t	Reserved
0x1B	Module 2 Temperature High Byte		
0x1C	Module 3 Status Low Byte (Bit field)	uint8_t (Bit field)	B0: Is On B1: Overvoltage B2: Undervoltage B3: Overcurrent B4: Overtemperature B5-B15: Reserved
0x1D	Module 3 Status High Byte (Bit field)		
0x1E	Module 3 Output Voltage Low Byte	int16_t	Calculation in [V]: U3 = DataValue / (2^8)
0x1F	Module 3 Output Voltage High Byte		

0x20	Module 3 Output Current Low Byte	int16_t	Calculation in [A]:
0x21	Module 3 Output Current High Byte		I3 = DataValue / (2^9)
0x22	Module 3 Temperature Low Byte	int16_t	Reserved
0x23	Module 3 Temperature High Byte		
0x24	Module 4 Status Low Byte (Bit field)	uint8_t	B0: Is On
0x25	Module 4 Status High Byte (Bit field)	(Bit field)	B1: Overvoltage B2: Undervoltage B3: Overcurrent B4: Overtemperature B5-B15: Reserved
0x26	Module 4 Output Voltage Low Byte	int16_t	Calculation in [V]:
0x27	Module 4 Output Voltage High Byte		U4 = DataValue / (2^10)
0x28	Module 4 Output Current Low Byte	int16_t	Calculation in [A]:
0x29	Module 4 Output Current High Byte		I4 = DataValue / (2^12)
0x2A	Module 4 Temperature Low Byte	int16_t	Reserved
0x2B	Module 4 Temperature High Byte		
0x2C	Module 5 Status Low Byte (Bit field)	uint8_t	B0: Is On
0x2D	Module 5 Status High Byte (Bit field)	(Bit field)	B1: Overvoltage B2: Undervoltage B3: Overcurrent B4: Overtemperature B5-B15: Reserved
0x2E	Module 5 Output Voltage Low Byte	int16_t	Calculation in [V]:
0x2F	Module 5 Output Voltage High Byte		U5 = DataValue / (2^12)
0x30	Module 5 Output Current Low Byte	int16_t	Calculation in [A]:
0x31	Module 5 Output Current High Byte		I5 = DataValue / (2^11)
0x32	Module 5 Temperature Low Byte	int16_t	Reserved
0x33	Module 5 Temperature High Byte		
0x34	Module 6 Status Low Byte (Bit field)	uint8_t	B0: Is On
0x35	Module 6 Status High Byte (Bit field)	(Bit field)	B1: Overvoltage B2: Undervoltage B3: Overcurrent B4: Overtemperature B5-B15: Reserved

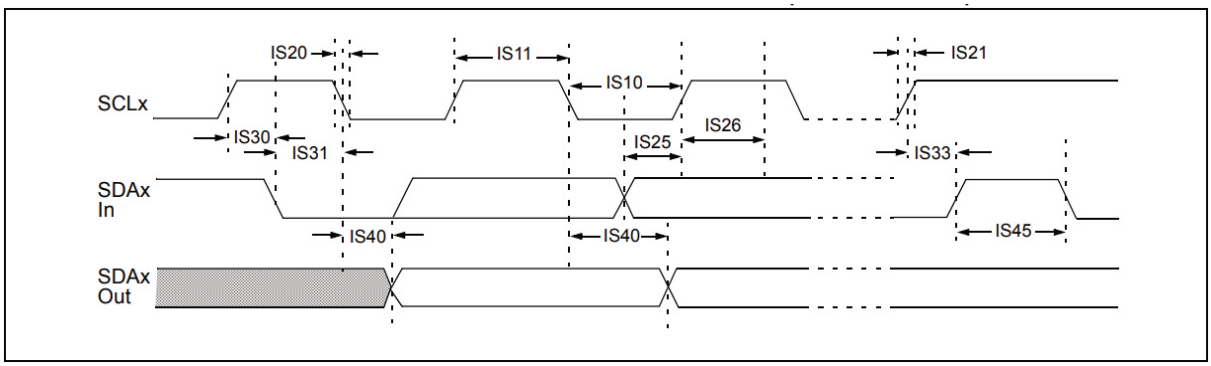
0x36	Module 6 Output Voltage Low Byte	int16_t	Calculation in [V]: U6 = DataValue / (2^11)
0x37	Module 6 Output Voltage High Byte		
0x38	Module 6 Output Current Low Byte	int16_t	Calculation in [A]: I6 = DataValue / (2^12)
0x39	Module 6 Output Current High Byte		
0x3A	Module 6 Temperature Low Byte	int16_t	Reserved
0x3B	Module 6 Temperature High Byte		

4.4 Timing

4.4.1 I2C™ BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)



4.4.2 I2C™ BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)



4.4.3 I2C™ BUS DATA TIMING REQUIREMENTS (SLAVE MODE)

These parameters are characterized, but not tested in manufacturing.

Characteristic		Min	Max	Units	Conditions
Clock Low Time	100 kHz mode	4.7	-	µs	
	400 kHz mode	1.3	-	µs	
Clock High Time	100 kHz mode	4.0	-	µs	
	400 kHz mode	0.6	-	µs	
SDA and SCL Fall Time	100 kHz mode	-	300	ns	CB is specified to be from 10 to 400pF
	400 kHz mode	20 + 0.1 CB	300	ns	
SDA and SCL Rise Time	100 kHz mode	-	1000	ns	CB is specified to be from 10 to 400pF
	400 kHz mode	20 + 0.1 CB	300	ns	
Data Input Setup Time	100 kHz mode	250	-	ns	
	400 kHz mode	100	-	ns	
Data Input Hold Time	100 kHz mode	0	-	ns	
	400 kHz mode	0	0.9	µs	
Start Condition Setup Time	100 kHz mode	4.7	-	µs	Only relevant for Repeated Start condition
	400 kHz mode	0.6	-	µs	
Start Condition Hold Time	100 kHz mode	4.0	-	µs	After this period, the first clock pulse is generated
	400 kHz mode	0.6	-	µs	
Stop Condition Setup Time	100 kHz mode	4.7	-	µs	
	400 kHz mode	0.6	-	µs	
Stop Condition Hold Time	100 kHz mode	4	-	µs	
	400 kHz mode	0.6	-	µs	
Output Valid From Clock	100 kHz mode	0	3500	ns	
	400 kHz mode	0	1000	ns	
Bus Free Time	100 kHz mode	4.7	-	µs	Time the bus must be free before a new transmission can start
	400 kHz mode	1.3	-	µs	
Bus Capacitive Loading		-	400	pF	
Pulse Gobbler Delay		65	390	ns	The typical value for this parameter is 130 ns.

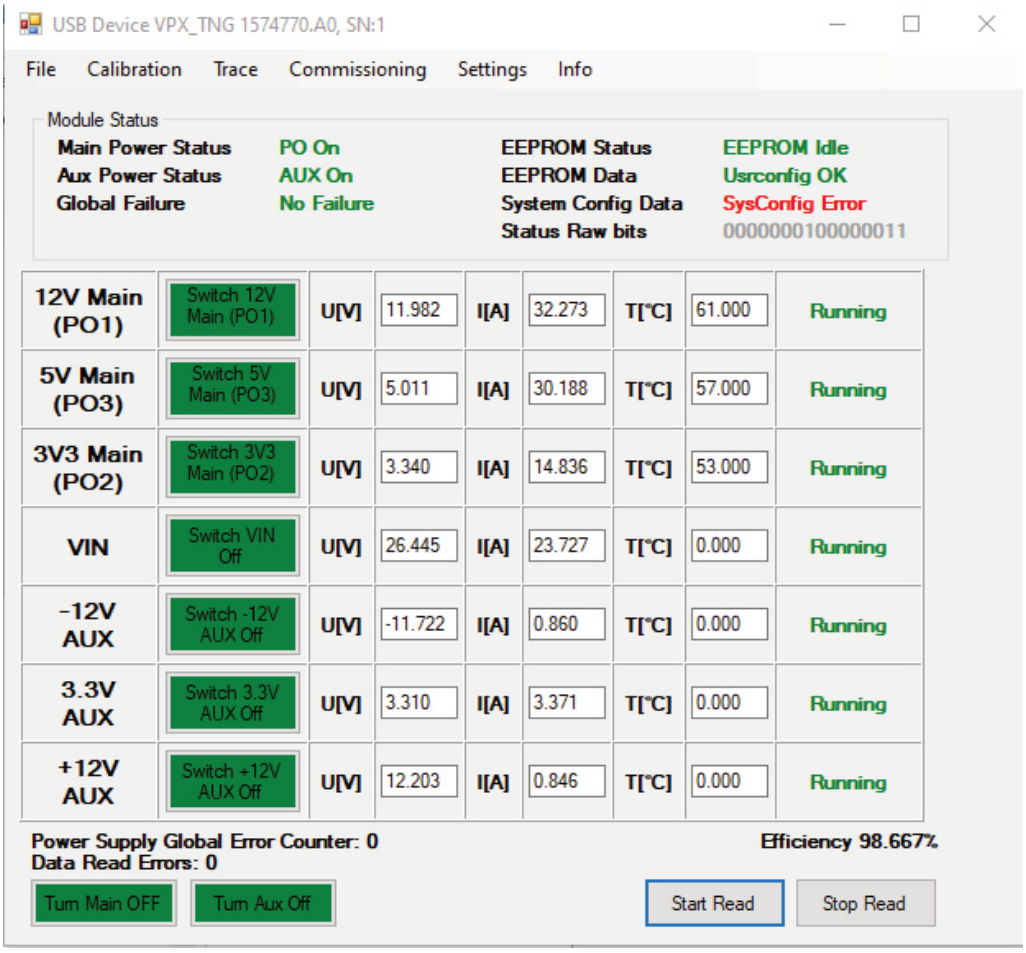
4.5 User Software

MS Windows program with GUI to monitor and control VPX360DMA power supply via USB or I2C Note: USB device driver or I2C interface (e.g. Microchip ADM00559) are required.

Features include:

- Global status
- Remote On / Off
- DC-IN status and measured voltage and current
- 2 internal Temperatures
- Voltage, current and status of individual output power modules (all channels)
- Calibration / setup and diagnostics

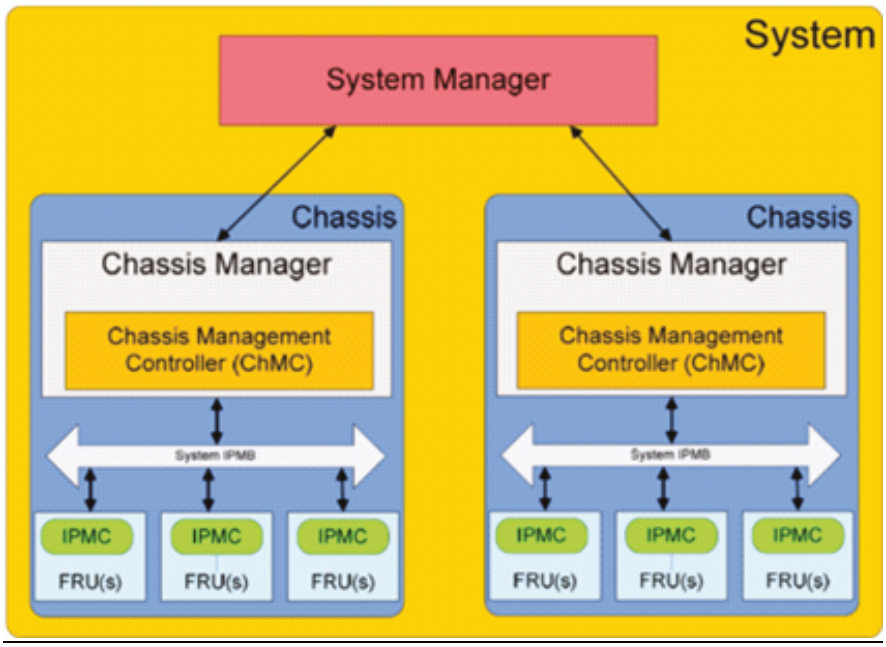
Download VPX Tool 2.0.xxxx from http://file.wiener-d.com/software/VPX/



IPMB Communication Protocol

The IPMB protocol is in compliance with VITA 46.11 and SOSA® for VPX power supplies. For further information, please refer to VITA 46.11 specification.

Overview



The Chassis Manager communicates inside the chassis with Intelligent Platform Management Controllers (IPMCs), each of which is responsible for local management of one or more Field Replaceable Units (FRUs).
Management communication within a chassis occurs primarily over the Intelligent Platform Management Bus (IPMB), which is implemented in an optionally dual redundant basis as the System IPMB in VITA 46.11. (If the IPMB is redundant you distinguish between IPMB A and IPMB B)

Every FRU has an own Hardware address (7 Bit). Every Hardware address should be unique within a chassis.
Aside from that, every FRU has its own physical address, which is build from a Site Type and a Site Number (detailed description in VITA 46.11 4.1.3.3)

IPMB Communication Protocol

IPMB Addressing

The IPMB Address is defined by the Hardware Address. There are three Geographical Address Pins GA0*, GA1* and GA2* available. (VITA46.11 Rule 4.1.3.1.2-1)
GA0*, GA1* and GA2* are inverted logic inputs with internal 10kOhm pullup.
The Hardware Address of a Module is given by adding 20h to the Geographical Address. (VITA46.11 Rule 4.1.3.1.1-7, Table 4.1.3.1-2)
To calculate the IPMB Address simply multiply the Hardware Address with 2 (or shift the bits 1 left) (VITA46.11 Rule 4.1.3.2-2)

GA2*	GA1*	GA0*	Hardware Address	IPMB Adresse
U	U	U	20h	40h
U	U	G	21h	42h
U	G	U	22h	44h
U	G	G	23h	46h
G	U	U	24h	4Eh
G	U	G	25h	4Ah
G	G	U	26h	4Ch
G	G	G	27h	4Eh

U = Unconnected; signal is pulled-up on the module and results in a logical “0”
G = Biased to Ground on the Backplane; results in a logical “1”

For programming use the following instruction:
20h = 0b0010 0000
For a 7-bit Address:
HARDWARE_MSB_ADDR = 0b01000 // 5 MSB bits from 20h, GA1, GA0
-> shift left
-> if GA2* 0, add 1
-shift left
-> if GA1* 0, add 1
-> shift left
-> if GA0 == 0 add 1
Physical Address

The physical Address is a description of the tangible location of a FRU within a Chassis. It is intended to aid an operator in locating a FRU wihtin a Chassis.
It consists of a pair of Values: Site Type and Site Number.

Site Type
The Site Type describes the identity of the FRU (for example: The Site Type of a Front Loading VITA 62 Module is 0Dh)
A full list of Site Types can be found in VITA 46.11 Rule 4.1.3.3-1, Table 4.1.3.3-1

Site Number
The Site Number identifies a specific FRU within a chassis in case that multiple modules of the same type are installed. Therefore, the Site Number needs to be a unique Number for every FRU of a specific Site Type in the Chassis.
The Site Number is equivalent so the Geographical Address for the FRU, interpreted as a numeric field.

GA2*	GA1*	GA0*	Site Number
U	U	U	1
U	U	G	2
U	G	U	3
U	G	G	4
G	U	U	5
G	U	G	6
G	G	U	7
G	G	G	8

IPMB Commands

Global Commands

Command Name	CMD	Additional informations
Get Device ID	01h	
Cold Reset	02h	
Get Self-Test Result	04h	
Broadcast "Get Device ID"(3)	01h	

Event Commands

Command Name	CMD	Additional informations
Set Event Receiver	00h	
Get Event Receiver	01h	
Get Sensor Event Enable	29h	
Get Sensor Event Status	2Bh	
Platofrm Event ("Event Message")	02h	

Sensor Device Commands

Command Name	CMD	Additional informations
Get Device SDR Info	20h	
Get Device SDR	21h	
Reserve Device SDR Repository	22h	
Get Sensor Hysteresis	25h	
Get Sensor Threshold	27h	
Get Sensor Type	28h	
Get Sensor Reading	2Dh	

Command Name	CMD	Additional informations
Get FRU Inventory Area Info	10h	
Read FRU Data	11h	
Write FRU Data	12h	

[2] Additional constraints apply, see appropriate IPMI v1.5 section for details.
[3] This command is sent using the Broadcast format on IPMB. See command description for details.

VITA 46.11 Commands

Command Name	CMD	Additional informations
Get VSO Capabilities	00h	
Set IPMB State	09h	
Set FRU StatePolicy Bits	0Ah	

Get FRU State Policy Bits	0Bh	
Get Device Locator Record ID	0Dh	
FRU Control Capabilities	1Eh	
Get FRU Address Info	40h	
Get Mandatory Sensor Numbers	44h	

SOSA Commands

For the SOSA Standard a few additional Commands needs to be Implemented.
The List is down below.

The SOSA Standard also requires a redundant IPMB (IPMB-A and IPMB-B)
The match this requirement the second I2C Interface on the µC needs to be accessible.
If the Hardware provides a redundant IPMB the Firmware needs to alternate

IPMI Messages between these two Interfaces.

Command Name	NetFn	CMD	Additional informations
FRU Control	2Ch	04h	
Set FRU StatePolicy Bits	2Ch	0Ah	
Get FRU State Policy Bits	2Ch	0Bh	
Set FRU Activation	2Ch	0Ch	
Get Mandatory Sensor Numbers	2Ch	44h	
Get SEL Info	0Ah	40h	
Reserve SEL	0Ah	42h	
Get SEL Entry	0Ah	43h	
Get SEL Time	0Ah	48h	
Set SEL Time	0Ah	49h	