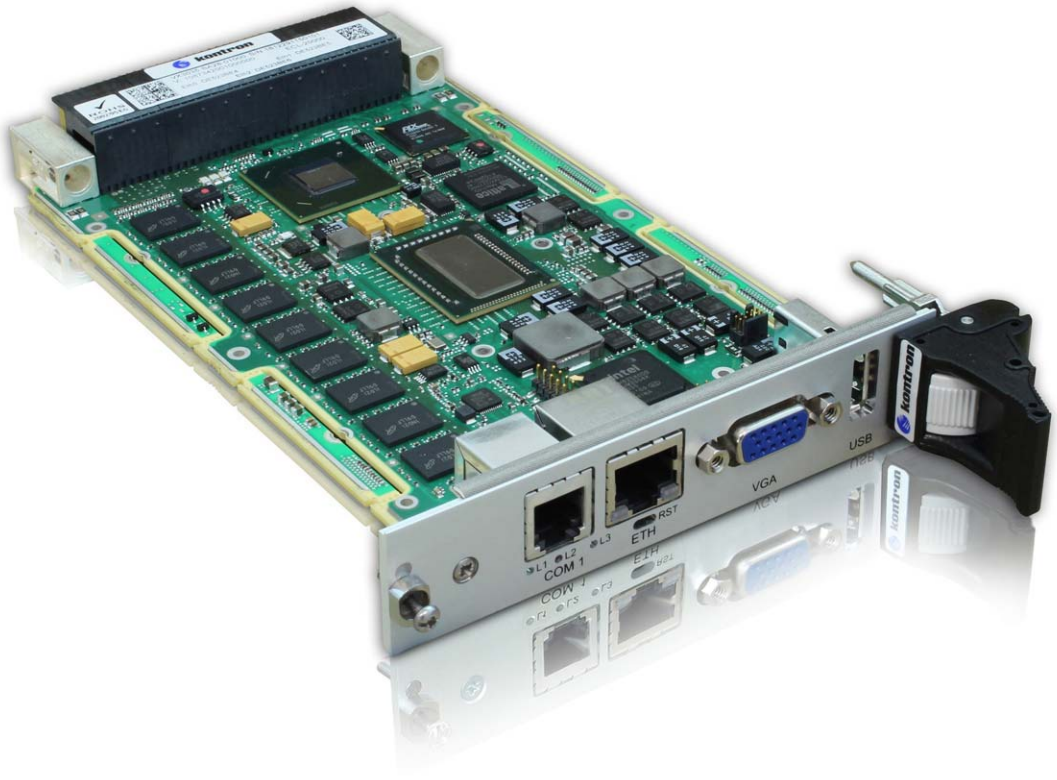
kontron

» VX3035 «



3U VPX Computing Node
User's Guide

CA.DT.A95-4e - June 2013

Revision History

Publication Title:	VX3035 User's Guide	
Doc. ID:	CA.DT.A95-4e	
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4e	Update of sections: - 1.6 - MTBF Data - 2.7.1 - USB or SATA NAND Flash Device Installation - 2.7.2 - Optional Battery Replacement - 4.1.1 - Serial Connector COM - 4.3.4 - XPD - 4.4 - LEDs - 5.1 - Power Specifications - 5.3 - CPU Thermal Monitoring	06-2013
3e	New photos Update of Chapters: - 1 - Introduction - 2 - Installation - 3 - Additional Board Features - 5 - Power and Thermal Specifications - 7 - VX3035 RTM Characteristics	10-2012
2e	Add a new order code (VX3035-SA12-01000) Description of the SATA NAND Flash Mezzanine Option	02-2012
1e	Update of “P0 Signal Definition” Table	01-2012
0e	Preliminary Version	10-2011

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This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

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Environmental protection is a high priority with Kontron.

Kontron follows the DEEE/WEEE directive.

You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- reduce waste arising from electrical and electronic equipment (EEE)
- make producers of EEE responsible for the environmental impact of their products, especially when they become waste
- encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- improve the environmental performance of all those involved during the lifecycle of EEE

Conventions

This guide uses several types of notice: Note, Caution, ESD.

Note: this notice calls attention to important features or instructions.


Caution: this notice alert you to system damage, loss of data, or risk of personal injury.


ESD: This banner indicates an Electrostatic Sensitive Device.

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix `0x' shows a hexadecimal number, following the `C' programming language convention.

The multipliers `k', `M' and `G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when `K', `M' and `G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

When describing transfer rates, `k' `M' and `G' mean $*10^3$, $*10^6$ and $*10^9$ *not $*2^{10}$ $*2^{20}$ and $*2^{30}$.*

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and CompactPCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Signal names ending with an asterisk (*) or a hash (#) denote active low signals; all other signals are active high.

Signal names follow the PICMG 2.0 R3.0 CompactPCI Specification and the PCI Local Bus 2.3 Specification.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions


Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.


Caution, Electric Shock!
Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Chapter 1 - Introduction

The Kontron VX3035 is a 3U VPX computing blade for data and signal processing application focusing on application domains such as Military & Aerospace, Transportation and Energy/Industry.

The Kontron VPX blade VX3035 is the ideal building block for intensive parallel computing workloads where a cluster of Kontron VX3035s can be used in switched OpenVPX environments or redundant configurations.

The VX3035 implements Intel's next generation high performance embedded processor with integrated memory controller and Intel® HD graphics - the Intel® Core™ i7 2nd Generation processor - coupled with the highly integrated Intel® Platform Controller Hub (PCH) QM67 with numerous Gigabit Ethernet, SATA, USB 2.0 and PCIe channels.

The VX3035 board comes with EFI BIOS and supports Linux, VxWorks, and other operating systems running on x86 CPU architecture. It is covered by Kontron's long term supply program, which guarantees customers multi-year supply of the product beyond its active life.

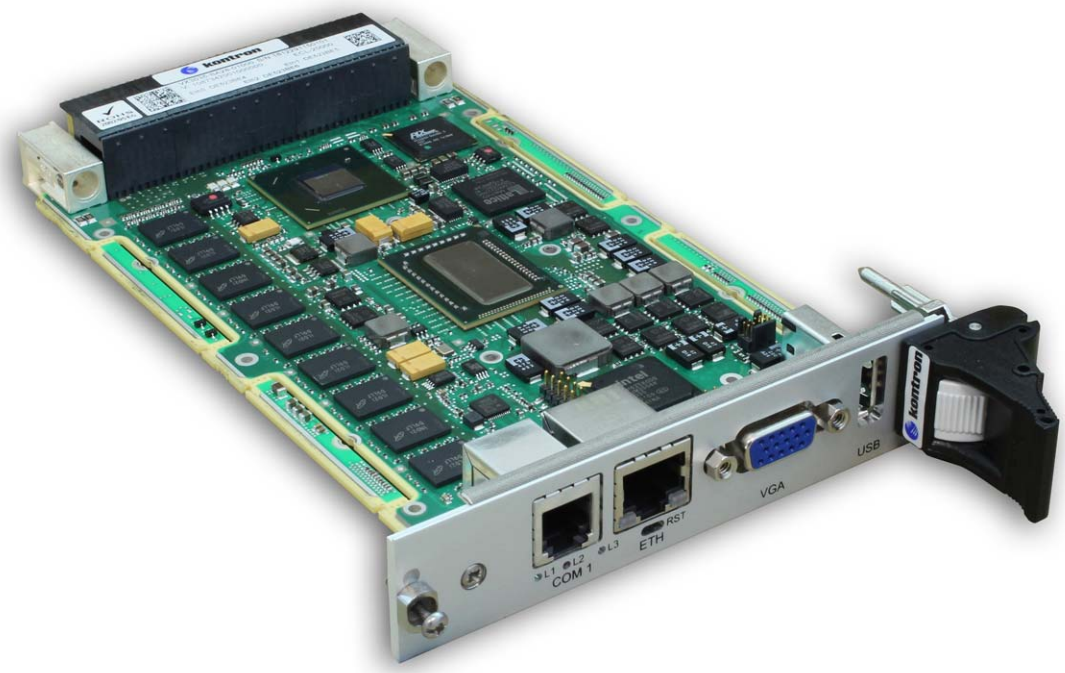


Figure 1: VX3035-SA 3U VPX Overview

1.1 Manual Overview

1.1.1 Objective

This guide provides general information, hardware instructions, operating instructions and functional description of the VX3035 board. The onboard programming, onboard firmware and other software (e.g. drivers and BSPs) are described in detail in separate guides (see section 1.7 "Related Publications").

This hardware technical documentation reflects the most recent version of the product. The "Hardware release Notes" (see section 1.7 "Related Publications") might help to keep track of potential evolutions.

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

1.1.2 Audience

This guide is written to cover, as far as possible the range of people who will handle or use the VX3035, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, system, cabling, grounding and communications.

1.1.3 Scope

This guide describes all variants of the VX3035 series.

1.1.4 Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- Chapter 1 - Introduction (this chapter)
- Chapter 2 - Installation
- Chapter 3 - Additional Board Features
- Chapter 4 - Physical In/Out
- Chapter 5 - Power and Thermal Specifications
- Chapter 6 - Backplane Suggestions
- Chapter 7 - VX3035-RTM Characteristics

1.1.5 Terminology, Definitions and Abbreviations

In this document, the term:

- VX3035 will be associated to the 3U VPX board
  - VX3035-SA will be associated to the standard air-cooled commercial version of the board.

- VX3035-RTM will be associated to the 3U VPX Rear Transition Module (RTM).

1.2 VPX Overview

VPX (VITA 46) specifications establish a new direction for the next revolution in bus boards. VPX is an ANSI standard which breaks out from the traditional connector scheme of VMEbus to merge the latest in connector and packaging technology with the latest in bus and serial fabric technology. VPX combines best-in-class technologies to assure a very long technology cycle similar to that of the original VMEbus solutions. Traditional parallel VMEbus will continue to be supported by VPX through bridging schemes that assure a solid migration pathway.

For further information regarding this standards and its use, visit the home page of the VITA - Open Standards, Open Markets (http://www.vita.com)

1.3 Board Overview

1.3.1 Main Features

» Intel® Core™ i7 2nd Generation Architecture

The VX3035 computing node is a VPX computing blade for parallel data and signal processing application. The VX3035 is the ideal building block for intensive parallel computing workloads where a cluster of VX3035s is used in full mesh or switched OpenVPX environments. Target applications include radar, sonar, imaging systems, airborne fighters, and unmanned aerial vehicle (UAV) radar, as well as rugged multi-display consoles. It is also well suited for transport applications.

The processing node of the VX3035 implements an Intel® Core™ i7 2nd Generation processor coupled with single or dual channel DDR3 memory. The highly integrated Intel® QM67 Express platform hub provides numerous Gigabit Ethernet, SATA, USB 2.0 and PCIe channels. The 3U-format VX3035 is available in standard air-cooled version.

The frequency of the CPU is nominally 2.2 GHz; however, the processor Intel® Core™ i7 2nd Generation is equipped with the Turbo Boost technology, which allows increasing the frequency up to 3.2 GHz when the total on chip power allows it (depending on second core and graphics activity). Operation can be limited down to 0.8 GHz by user configuration to decrease the power consumption.

» Soldered DDR3 Memories with the Support of ECC

The processor accesses two memory-channels (2 x 72-bit) having a total size of 4 or 8 GB. The DDR3 memory technology used operates at 1,333 Gbits/s. An 8-bit ECC memory is implemented to detect and correct errors.

The memory actually equiped onboard can be limited to one bank depending on board version.

» Numerous Storage Interface and Non Volatile Memories

The following storage features are available :

- A USB 2.0 Flash drive slot is available onboard supporting low profile USB 2.0 Flash disk modules up to 16 GB.
- Redundant 32 Mbits NOR flash memories are used to store firmware code.
- Two serial 256 Kbits EEPROMs are dedicated to system and application data storage.
- A 512 Kbits ferro magnetic, non-volatile random access memory allows the backup of critical data when the board is powered off.

All the Flash and non volatile memories onboard have a write protect mechanism taking into account the NVMRO (Non Volatile Memory read Only) VPX signal.

» Software

Kontron is one of the few compact PCI, VME and VPX vendors providing in-house support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software editors, Kontron is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

Finally, Kontron offers to its customers owners of a maintenance agreement a hotline software support and regular software updates. A dedicated web site is also available for online updates and release downloads.

The VX3035 is delivered with the UEFI BIOS from AMI.

The VX3035 supports Linux Fedora 14 distribution.

Please contact Kontron for further information regarding other operating systems and software support.

Harsh Environments

The VX3035 has been designed to use the same PCB for both air and conduction-cooled boards. Build variants span a complete range of temperature, shock and vibration requirements as specified in the VITA 47 standards.

Rear Transition Module

The VX3035 supports the VX3035-RTM (Order Code: PB-VX3-011), a 3U VPX Rear Transition Module compliant with the definition of the Rear Transition Module on VPX standard - VITA 46.10.

It offers connectivity on the rear for:

- one RJ-45 Ethernet 1000Base-T
- two SATA ports
- two serial COM ports
- two USB ports
- two GPIOs

1.3.2 Block Diagram

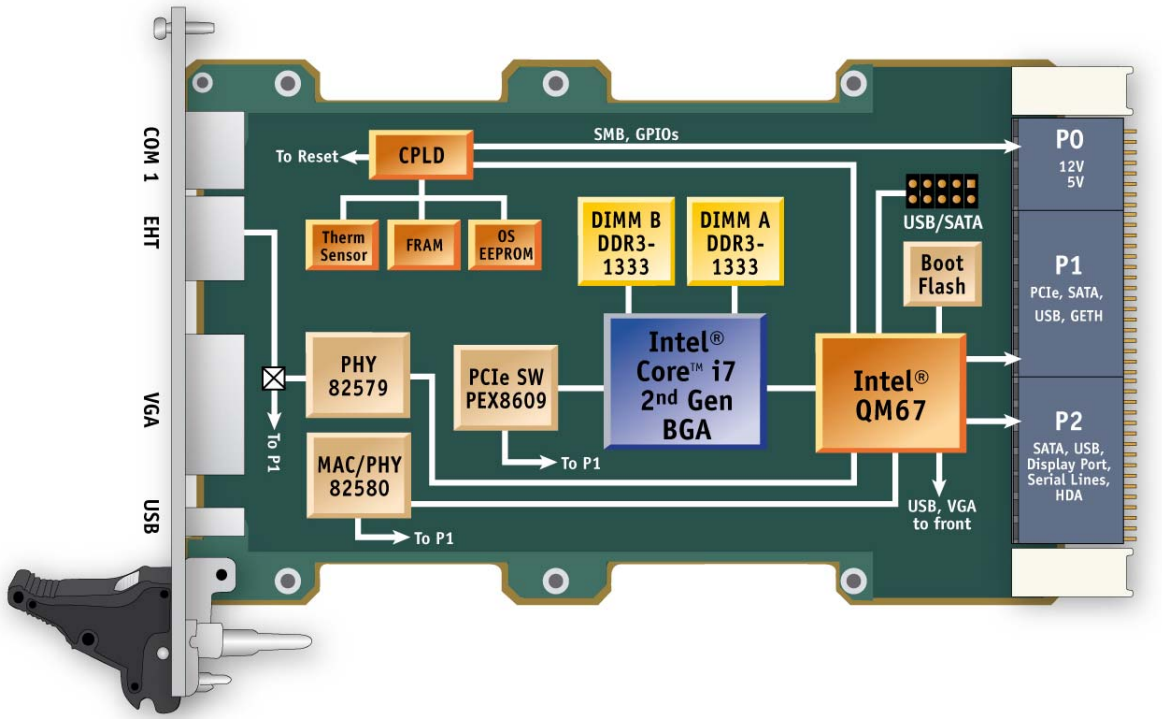


Figure 2: VX3035 Block Diagram

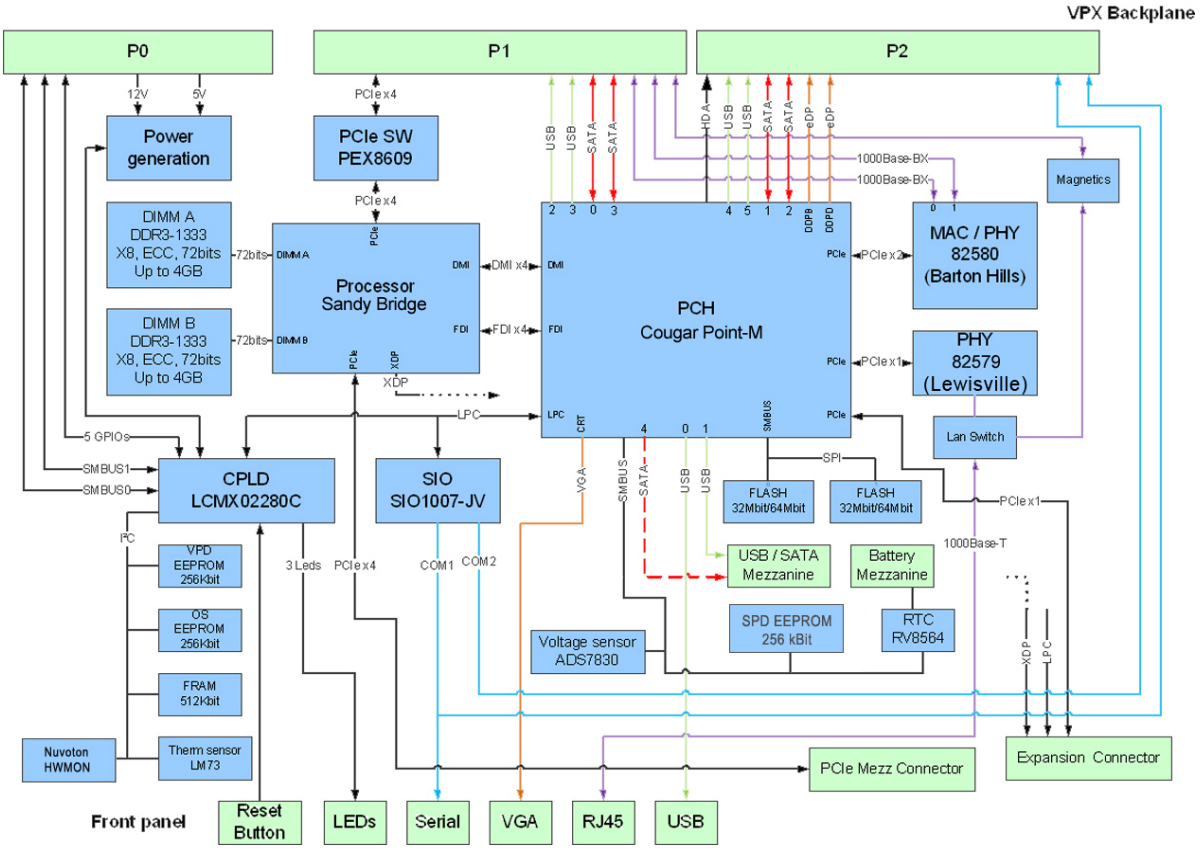


Figure 3: VX3035 Functional Block Diagram

1.3.3 Ordering Information

Manufacturing Options

- CPU Frequency: . . . . . 2.2 GHz (default)
- DDR3 SDRAM Size: . . . . . 2 GB total onboard
  . . . . . 4 GB total onboard
  . . . . . 8 GB total onboard
- Ruggedization Levels: . . . . . Standard Air-Cooled (SA)
- Front Panel . . . . . 0.8"
  . . . . . 1.0" (default)

Order Code Available

Order Code		Description
VX3035-SA	VX3035-SA24-01000	Air-cooled 3U VPX Single Board Computer, 2.2 GHz Intel® Core™ i7 2nd Gen, 4 GB DDR3-SDRAM, front: 1"
VX3035-SA	VX3035-SA24-00000	Air-cooled 3U VPX Single Board Computer, 2.2 GHz Intel® Core™ i7 2nd Gen, 4 GB DDR3-SDRAM, front: 0.8"
VX3035-SA	VX3035-SA12-01000	Air-cooled 3U VPX Single Board Computer, 2.2 GHz Intel® Core™ i7 2nd Gen, 2 GB DDR3-SDRAM /single bank, front: 1", no PCIe on VPX, no P2 VPX I/O connector.
VX3035-SA	VX3035-SA28-01000	Air-cooled 3U VPX Single Board Computer, 2.2 GHz Intel® Core™ i7 2nd Gen, 8 GB DDR3-SDRAM, front: 1"
VX3035-SA	VX3035-SA28-00000	Air-cooled 3U VPX Single Board Computer, 2.2 GHz Intel® Core™ i7 2nd Gen, 8 GB DDR3-SDRAM, front: 0.8"
VX3035-RTM	PB-VX3-011	3U VPX Rear Transition Module compatible with the VX3035
USB Flash Module	FDM-USB-*x*GB-2MM-IV	USB Flash Device (*x* GB)
SATA Flash Module	FDM-SATA-32GB-C0V	32 GBytes MLC device, commercial temperature
SATA Flash Module	FDM-SATA-8GB-I0V	8 GBytes SLC device, industrial temperature
SATA Flash Module	FDM-SATA-4GB-I0	4 GBytes SLC device, industrial temperature
Serial Cable	KIT-2X-RJ12DB9	Serial cable adapter
Test equipment	OT-XDP-VX3035-A-00	XDP test equipment for attachment of test probe

Table 1: Order Code

1.3.4 I/O Interfaces

Front Interfaces

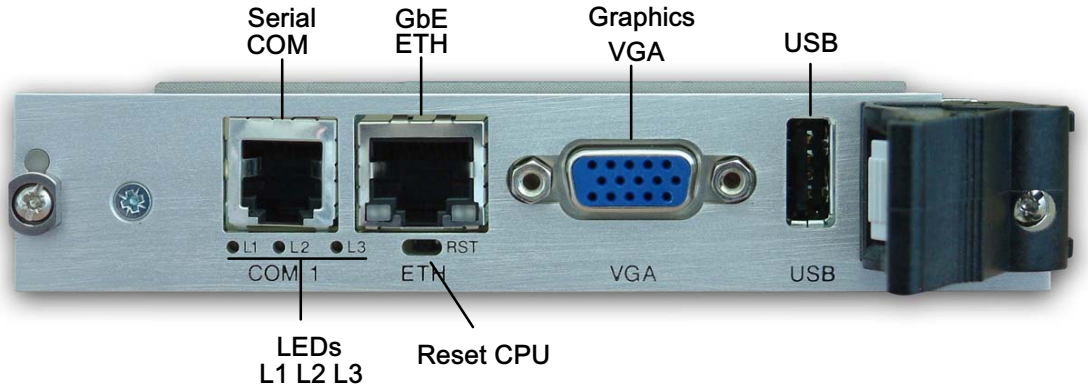


Figure 4: VX3035 Front Panel I/O Interfaces

Function	Description	See also
Serial Ports	**COM**: 1x EIA-232/EIA-485 UART interface for CPU on RJ-12 connector.	Section 4.1.1 for Pin Assignment
Gigabit Ethernet	1000BASE-T on RJ-45 connectors: **Note**: this port is configurable from the BIOS to be routed to the VPX P1 connector instead of the front connector ETH	Section 4.1.2 for Pin Assignment
USB	USB 2.0 interface	Section 4.1.3 for Pin Assignment
Graphics	**VGA**: VGA connector	Section 4.1.4 for Pin Assignment
Reset	Reset push button	Figure 4
LEDs	3 LEDs reporting the board CPU health status and activity	Section 4.4 for LEDs Description

Table 2: Front I/O Interfaces

Rear Interfaces

Compliant with:

- VITA 46.0 (Standard VPX)
- VITA 46.4 (PCI Express on VPX)
- VITA 46.9 (I/O and Gigabit Ethernet on VPX)
- VITA 65 (OpenVPX System specification)

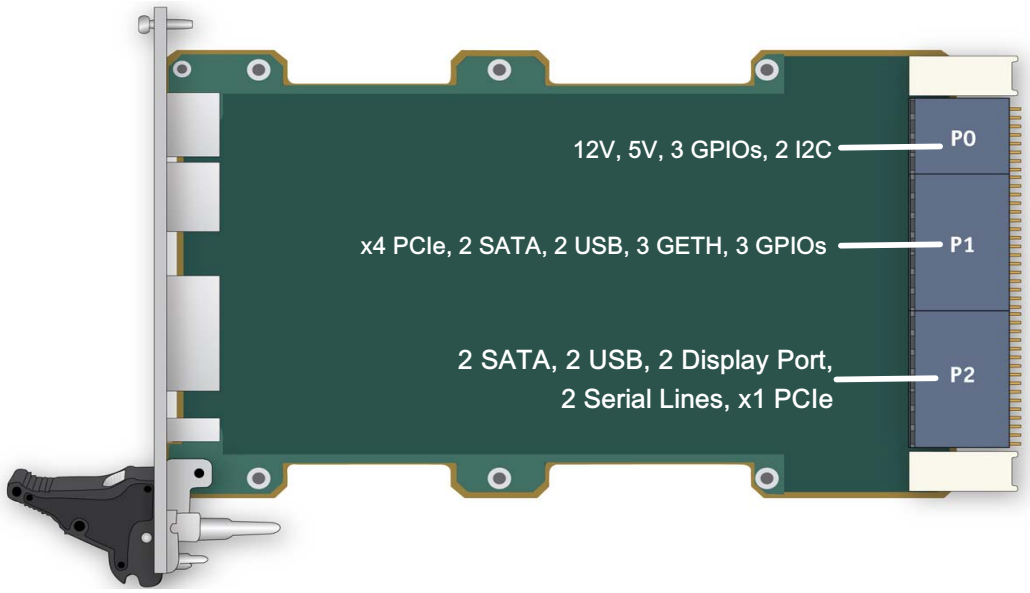


Figure 5: VX3035 Rear I/O Distribution

Function	Description	See also
PCI Express	> 1 x4 gen2 PCIe non transparent capability, on P1. Optional use of PCIe common reference clock feature. > 1 x1 additional PCIe interface, gen2, on P2	Section 4.3 for VPX Connectors Description
SATA Storage	> 2 SATA II link on P1 > 2 additional SATA II links on P2	
USB	> 2USB 2.0 link on P1 > 2 additional USB 2.0 link on P2	
Gigabit Ethernet	> 2 SerDes 1000BASE-BX on P1 > one 1000Base-T on P1	
Serial	> 2 asynchronous EIA-232/EIA-485 RX/TX serial line, on P2	
GPIOs	> 3 User GPIOs on P1, including OpenVPX GDISCRETE1, and MASKABLE RESET > 3 additional GPIOs on P0, replacing unused optional JTAG pins	Section 4.3 for VPX Connectors Description
DisplayPort	2 embedded DisplayPort on P2	Section 4.3 for VPX Connectors Description
Utilities	On P0 and P1: SYSRESET, SYSCON, 6 Geographical Addresses	Section 4.3 for VPX Connectors Description
Clocks	On P0: 25 MHz Refclock, 1 PPS Auxclock, optional PCIe 100 MHz clock	
Power Supplies	On P0: VS1=12V, VS3=5V, VS2 not connected 3.3V_AUX optional, +12V_AUX not connected,	

Table 3: Rear I/O Interfaces

1.3.5 Components Layout

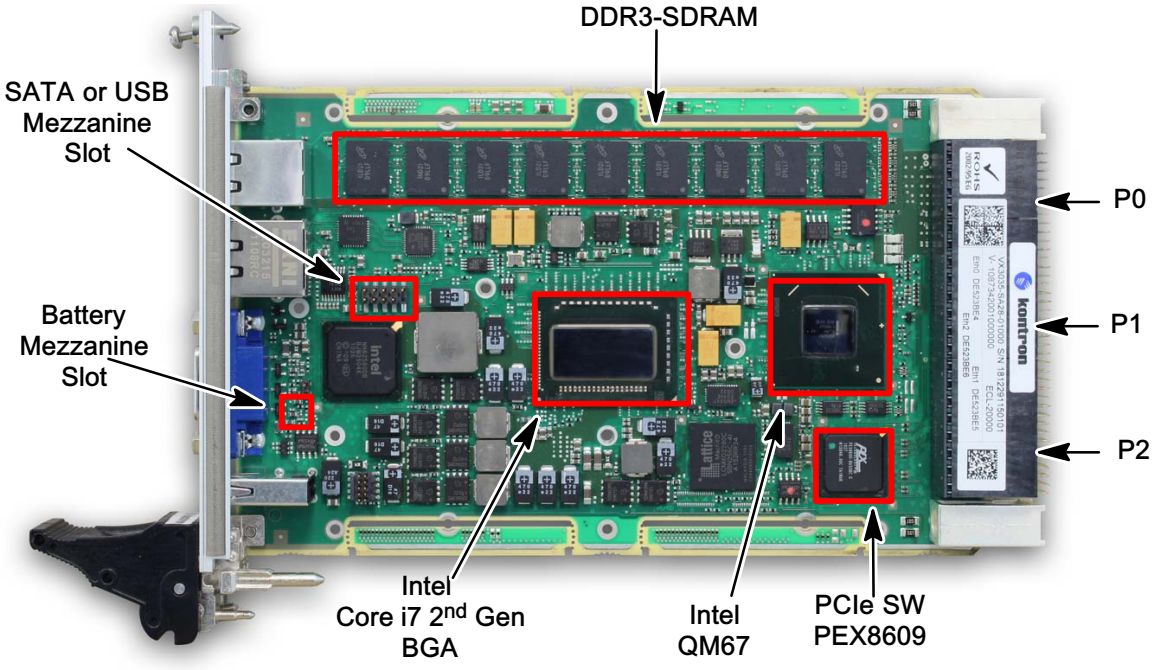


Figure 6: VX3035 Components Layout (Top view)

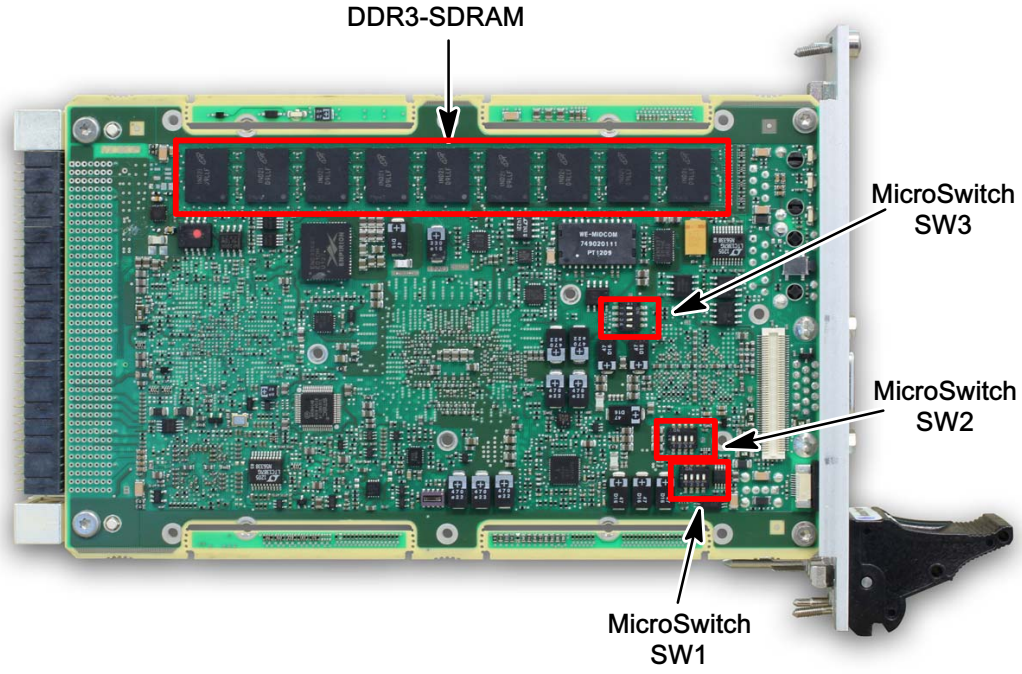


Figure 7: VX3035 Components Layout (Bottom view)

1.3.6 Technical Specification

Form Factor	
Form Factor	3U VPX, single slot, 0.8 inch or 1 inch pitch for Standard Air (SA).
Processor: Intel® Core™ i7	
Processor	Intel® Core™ i7 -2655LE at 2.2 GHz. 4M cache, 2 execution cores, 4 threads. 32-nanometer silicon technology.
Cache Structure	32 KB L1, 256 KB L2 per core, 4 MB L3 shared between cores.
Memory Controller	Integrated DDR3 memory controller with ECC support, 1333 Mbits/s. Two memory channels of 72 bits each. Equipment of one or two memory channels.
Graphics Core	Integrated Graphics Core
PCI Express Interface	2.5 GT/s (gen1) or 5 GT/s (gen2) PCIe. One 4 lane PCIe to the backplane through PEX8609 Non Transparent (NT) bridge for PCIe backplane links.
DMI Interface	x4 5 GT/s point-to-point DMI interface to Platform Controller Hub (PCH).
FDI Interface	Carries display traffic from the integrated graphics controller to the PCH for generation of external display protocols (VGA, DP, ...)
PCH: Cougar Point	
PCI Express Interface	2 lane PCIe to 1000BASE-BX dual-ethernet controller 1 lane PCIe to VPX backplane for CPU
SPI Interface	Connects to two SPI flash devices (4 MBytes)
LPC	33 MHz LPC, for SuperIO and CPLD connection
SATA	Up to 3 Gb/s integrated Serial ATA host controllers 4 ports on rear VPX connectors, 1 port for onboard Flash mezzanine connector
USB	4 USB 2.0 ports on the VPX connectors, 1 USB 2.0 port for onboard Flash mezzanine connector One front USB 2.0
VGA and Display Ports	One VGA front panel interface Two embedded display port available on VPX backplane
Memory	
System Memory	Up to 8 GB DDR3 SDRAM at 1333 MHz, two memory channels
SPI Flash	Firmware Boot Device
NAND Flash	Up to 16 GB USB Nand Flash storage socket (for USB Nand Flash modules) or 32 GB MLC/ 8 GB SLC / 4GB SLC SATA NAND drive socket.
F-RAM	512 Kbit of non volatile ferromagnetic RAM
EEPROM	One serial 256 Kbit EEPROM dedicated to system data One serial 256 Kbit EEPROM dedicated to application data

Onboard Controllers	
Gigabit Ethernet Controller	One i82580 Gigabit MAC/PHY connecting two SerDes links on VPX backplane
Gigabit Ethernet PHY	One i82579 PHY connected on front panel or VPX backplane (user selectable)
System CPLD	One CPLD Board controller for power sequencing, reset handling, monitoring, failure detection, VPX I2C communication. Provides configuration/status registers on LPC interface
SIO	SIO1007 provides two serial lines
Onboard Interfaces	
CPU Debug Interface	XDP port for CPU extended debug port connection (available on debug connector and needs additional test equipment OT-XDP-VX3035-A-00 for XDP access)

Table 4: VX3035 Main Characteristics

1.4 Environmental Specifications

ENVIRONMENTAL SPECIFICATIONS	
	SA - Standard Commercial
Conformal Coating	Optional
Airflow	2.5 m/s (1") and 3 m/s (0.8")
Temperature	VITA 47-Class AC1
Cooling Method	Convection
Operating	0°C to +55°C
Storage	-45°C to +85°C
Vibration Sine (Operating)	2g / 20-500 Hz acceleration / frequency range
Random	VITA 47-Class V1
Shock (Operating)	20g / 11 ms peak accel. / shock duration half sine
Altitude (Operating)	-1,640 to 15,000 ft
Relative Humidity	90% non-condensing (95% with coating)

Table 5: Environmental Specifications

1.5 Board Weight

	Weight
VX3025-SA12-01000 1", no battery, no FDM-SATA/USB mezzanine	330g
VX3035-SA28-01000 1", battery on, no FDM-SATA/USB mezzanine	360g

1.6 MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

VX3035-SA24-00000

	GB (Hours)		AIC (Hours)	NS (Hours)		ARW (Hours)
	25°C	40°C	40°C	25°C	40°C	55°C
MTBF (hours)	284 805h	199 518h	37 629h	52 645h	43 170h	10 014h

Table 6: VX3035-SA24-00000 MTBF Data

VX3035-SA28-01000

	GB (Hours)		AIC (Hours)	NS (Hours)		ARW (Hours)
	25°C	40°C	40°C	25°C	40°C	55°C
MTBF (hours)	315 231h	231 125h	39 382h	55 652h	46 405h	10 819h

Table 7: VX3035-SA28-01000 MTBF Data

VX3035-SA12-01000

	GB (Hours)		AIC (Hours)	NS (Hours)		ARW (Hours)
	25°C	40°C	40°C	25°C	40°C	55°C
MTBF (hours)	342 360h	249 228h	42 495h	60 302h	49 796h	11 302h

Table 8: VX3035-SA12-01000 MTBF Data

1.7 Related Publications

The following publications contain information relating to this product:

PRODUCT	PUBLICATION	
Standard		
ANSI/VITA 46.0	VPX Baseline Standard - ANSI/VITA 46.0-2007	
ANIS/VITA 46.4	PCI Express® on VPX Fabric Connector - VITA Draft Standard for Trial Use	
ANSI/VITA 46.6	Gigabit Ethernet Control Plane on VPX - VITA Draft Standard	
ANSI/VITA 46.10	Rear Transition Module for VPX - ANSI/VITA 46.10-2009	
Serial ATA	Serial ATA 1.0a Specification	
Hardware		
VX3035 Boards	VX3035 Hardware Release Notes	CA.DT.A96
Firmware		
VX3035 Boards	AMI-BIOS User Reference Manual	FT.DT.F97
Software		
VX3035 Boards	Release Note Fedora 14 on VX3035	SD.DT.F82
Systems		
VX3035 Boards	EZ3-VX3035- Getting Started EZ3-VX3035- Quick Start	FT.DT.G05 SD.DT.F95

Table 9: Related Publications

Chapter 2 - Installation

The VX3035 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

2.1 Safety Requirements

The following safety precautions must be observed when installing or operating the VX3035. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Special care shall be taken while handling the board: firstly, the heat sink can get very hot and secondly, since the heat sink attachment uses springs, any reckless pressure on the heat sink could be transmitted to the processor die and damage it. Do not touch the heat sink when installing or removing the board. In addition, the board should not be placed on any surface or in any form of storage container before the board and heat sink have cooled down to room temperature.

This board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:
Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector pins or traces.
- We strongly recommend our customers to work in an environment equipped with anti-static workbenches with professional discharging equipments.

2.2 Board Identification

The VX3035 boards are identified by labels fitted to the top side of the board.

Top Side

A "Identification" label: Order Code, Serial Number, Variant, E.C. Level, Ethernet MAC addresses

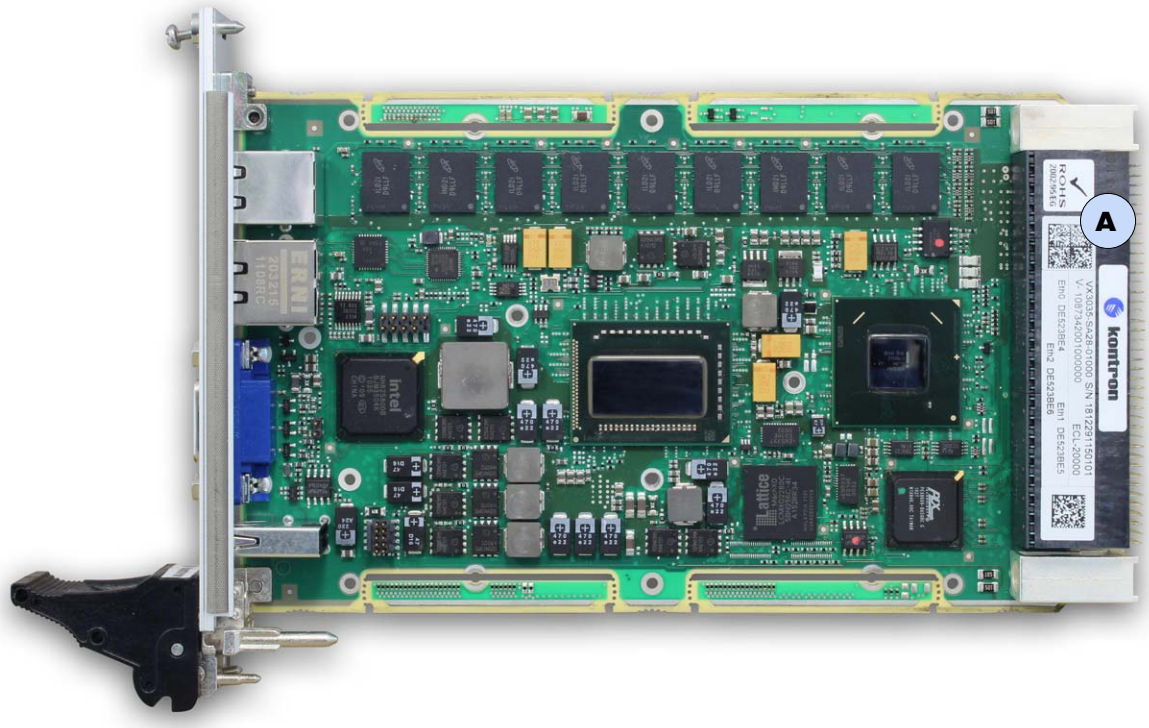


Figure 8: VX3035 Identification (Top Side)

2.3 Board Configuration

Microswitches

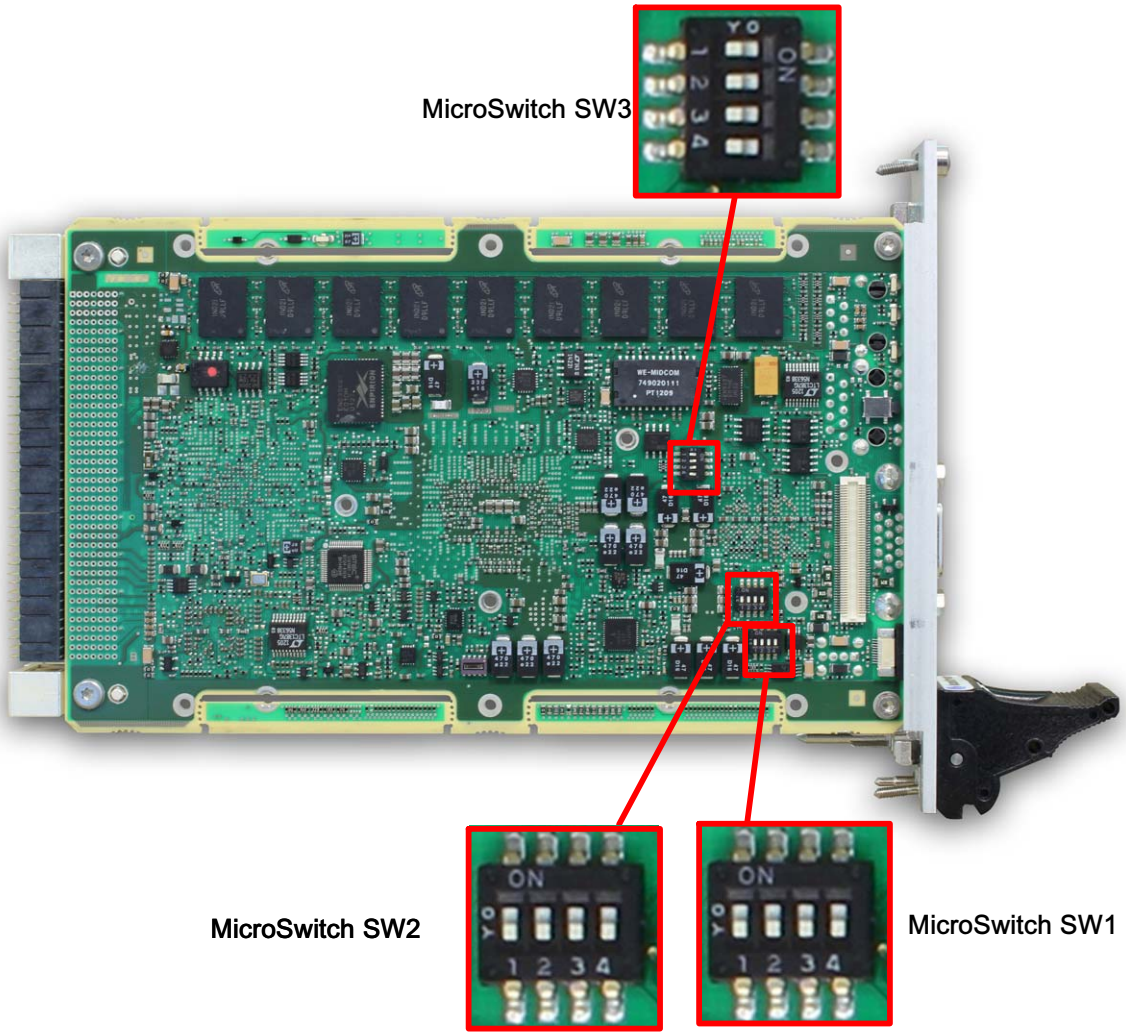


Figure 9: VX3035 Board Configuration (Bottom view)

Three 4-bit microswitches are available on the VX3035: SW1, SW2 and SW3

2.3.1 Microswitch SW1 Description

Function	Description	Default
1 - Factory Test Mode	**on**: factory test mode is selected **off**: normal operation	off
2 - VPD (Vital Product Data) EEPROM write protect	**on**: VPD 32Kx8 EEPROM is write protected **off**: VPD 32Kx8 EEPROM is not write protected unless VPX signal NVMRO is active (logic 1)	on
3 - System (base software parameters) EEPROM write protect	**on**: System 32Kx8 EEPROM is write protected **off**: System 32Kx8 EEPROM is not write protected unless VPX signal NVMRO is active (logic 1)	off
4 - FRAM (Ferro Magnetic RAM) write protect	**on**: 64Kx8 User FRAM is write protected **off**: 64Kx8 User FRAM is not write protected whatever the level of the NVMRO VPX signal is	off

Table 10: Microswitches SW1

2.3.2 Microswitch SW2 Description

Function	Description	Default
1 - Rescue Boot Flash	**on**: CPU boots the BIOS from its rescue flash. **off**: Normal operation. CPU boots the BIOS from its non rescue flash.	off
2 - Power on wait	**on**: VX3035 card waits for an I2C command from the VPX bus to start internal power on. **off**: Normal operation. VX3035 card automatically powers on.	off
3 - CPU performance/power limitation	**on**: Forced to 0.8 GHz. **off**: Normal operation.	off
4 - Reserved		off

Table 11: Microswitches SW2

2.3.3 Microswitch SW3 Description

Function	Description	Default
1 - VPX PCI-E port size	**on**: four x1 ports on VPX PI **off**: one x4 port on VPX P1	off
2 - Maximum PCI-E link speed on VPX	**on**: Gen 2 (5 GT/s), will achieve Gen 2 speed transfers if link partner is advertising Gen 2 capability **off**: Gen 1 (2.5 GT/s), to be used with low speed capability backplane	off
3 - LEDs power debug mode	**on**: Power debug status on front panel LEDs **off**: normal LEDs mode	off
4 - SPD debug mode	**on**: DDR3 SPD debug mode **off**: normal operation	off

Table 12: Microswitches SW3

2.4 Package Content

The VX3035 is packaged with several components. The packing contents of the VX3035 Series may vary depending on customer requests.

- CPU Module:
  - Order Code: refer to section 1.3.3 “Order Code Table” :
    - Processor specifications differ depending on Order Code.
    - Heat sink assembled on the board.
- Rear Transition Module:
  - Order Code: refer to section 1.3.3 “Order Code Table”.
- NAND Flash Disk Module:
  - Order Code: refer to section 1.3.3 “Order Code Table”.
- CD-ROM - Technical Documentation.

2.5 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the VX3035 in a system. Procedures for standard removal operations are found in their respective chapters.

To perform an initial installation of the VX3035 in a system proceed as follows:

1. Ensure that the safety requirements indicated in Section 2.1 are observed.

Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the VX3035 refer to Chapter 5. For the installation of VX3035 specific peripheral devices and Rear I/O devices refer to the appropriate sections in current Chapter.

Care must be taken when applying the procedures below to ensure that neither the VX3035 nor other system boards are physically damaged by the application of these procedures.

3. To install the VX3035 perform the following:
    1. Ensure that no power is applied to the system before proceeding.

When performing the next step, DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

    2. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.
    3. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
    4. Fasten the front panel retaining screws.
    5. Connect all external interfacing cables to the board as required.
    6. Ensure that the board and all required interfacing cables are properly secured.

The VX3035 is now ready for operation. For operation of the VX3035, refer to appropriate VX3035 specific software, application, and system documentation.

2.6 Standard Removal Procedure

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Section 2.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

Care must be taken when applying the procedures below to ensure that neither the VX3035 nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.
5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.

Due care should be exercised when handling the board: firstly, the heat sink can get very hot and secondly, since the heat sink attachment uses springs, any reckless pressure on the heat sink could be transmitted to the processor die and damage it. Do not touch the heat sink when changing the board.

7. Dispose of the board as required.

2.7 Installation of Peripheral Devices

The VX3035 is designed to accommodate a variety of peripheral devices whose installation varies considerably. The following sections provide information regarding installation aspects and detailed procedures.

> Section 2.7.1 page 23 NAND Device Installation
> Section 2.7.2 page 28 Battery Replacement

2.7.1 USB or SATA NAND Drive Flash Device Installation

The onboard USB or SATA device is used to connect a USB Flash Disk or a SATA Flash Mezzanine.

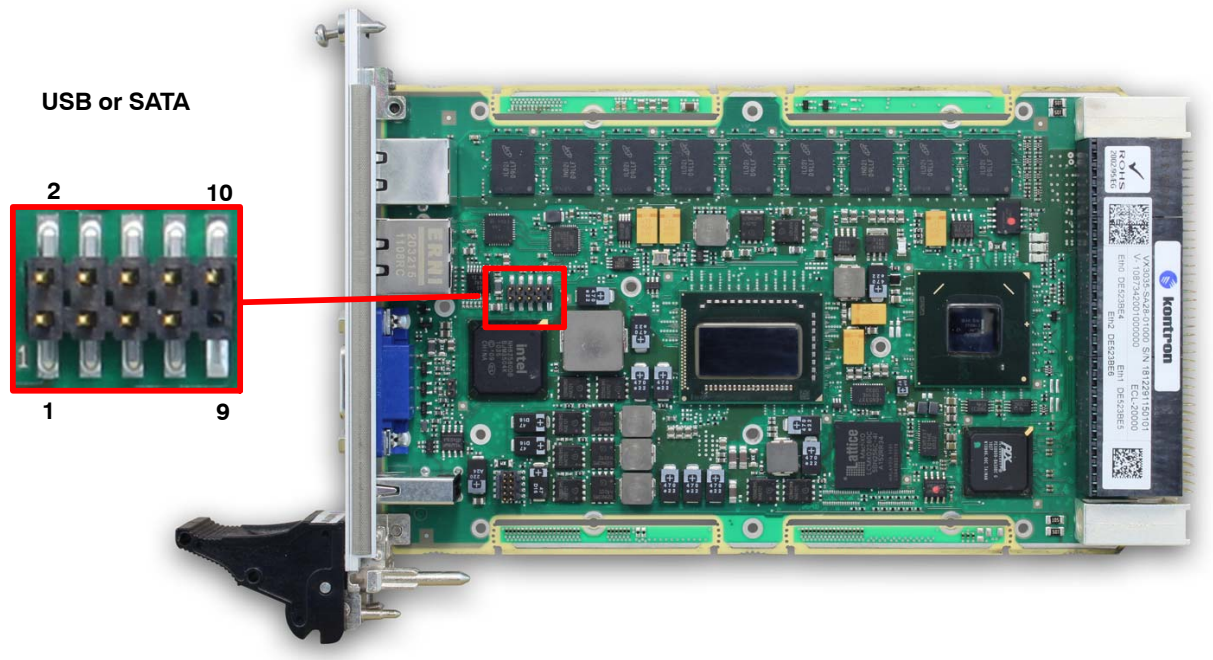


Figure 10: USB or SATA Mezzanine Connector Location

Depending on VX3035 board type, there are two possible holders for mounting the NAND device :

Mounting NAND device with SUP-MEZFLASH-1-V02 :

Use the retainers BRIDE-FDMUSB-1 as shown in Figure 11 to mount the NAND device onto the holder. Make sure to have the retainer oriented with its boss close to the holder.

Use the following screws for the assembly:

- one M3 8mm stainless steel screw (Kontron P/N VISTEB-M3X8- INOX-A2)
- one M3 4mm stainless steel screw (Kontron P/N VISTEB-M3X4-INOX-A2).

Kontron recommends Loctite 222 thread adhesive on the screws.

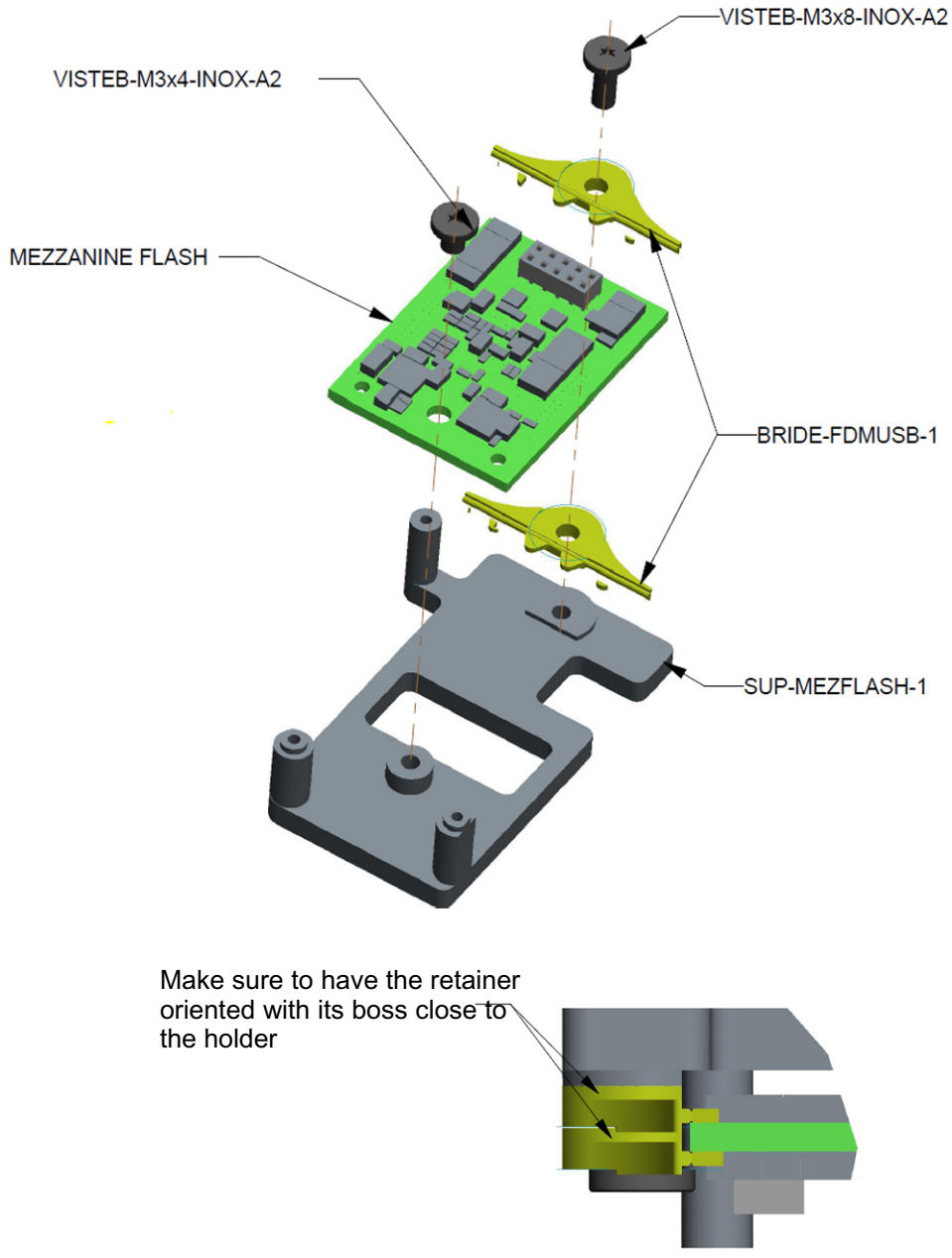


Figure 11: Mounting the NAND Device onto the holder with SUP-MEZFLASH-1-V02

Then mount the holder and the NAND device onto the board with three M2 8 mm stainless steel screws (Kontron P/N VIS-CZX-M2X8-INOX) as shown in Figure 12.

Kontron recommends Loctite 222 thread adhesive on the screws.

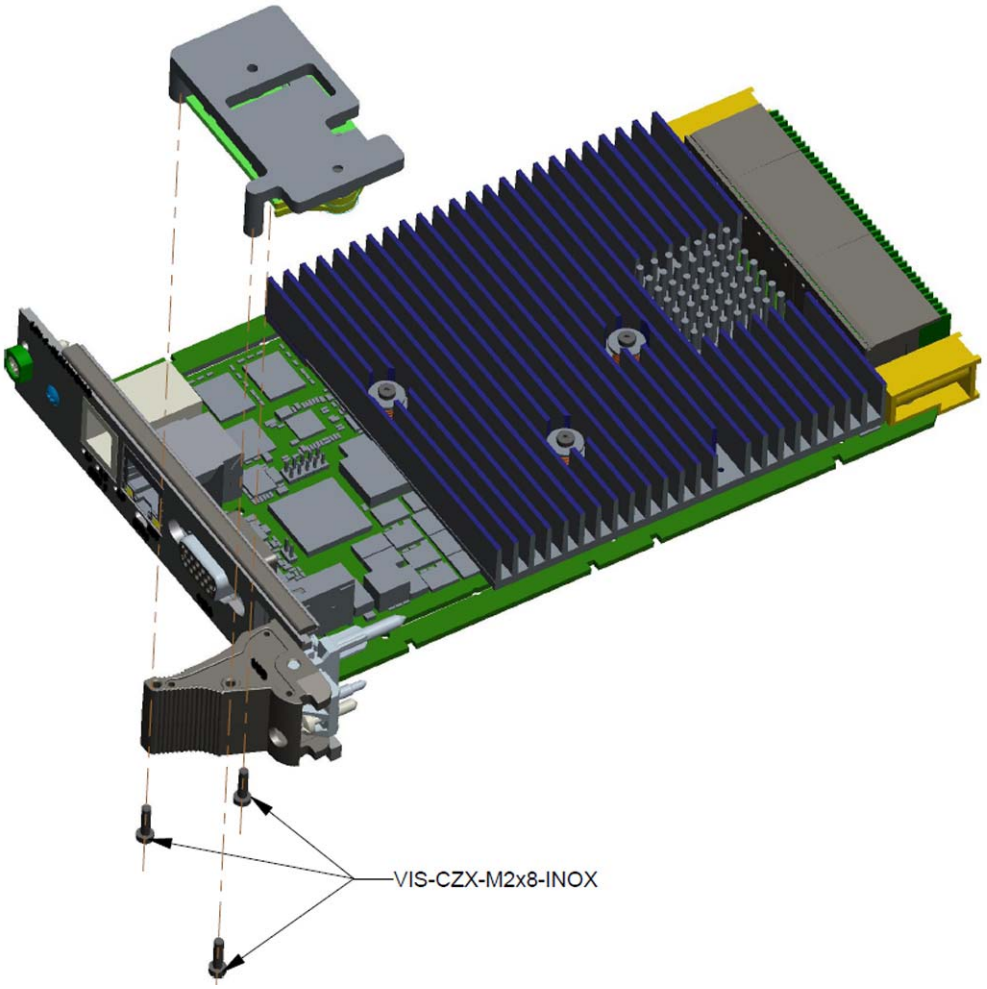


Figure 12: Mounting the holder SUP-MEZFLASH-1-V02 and the NAND Device onto the VX3035 board

Mounting NAND device with SUP-MEZFLABAT-1-V02

Use the 3 standoffs ENT-CL2.3X5X3-NYLON as shown in Figure 13 to mount the NAND device onto the holder.

Use the following screws for the assembly of the NAND device :

- one M3 4mm stainless steel screw (Kontron P/N VISTEB-M3X4-INOX-A2),
- three washers (Kontron P/N ROND2.5X5X0.3-NYLON), three M2 8mm stainless steel screws .

Note Two M2 8mm stainless steel screws are used in the figure below for the battery mezzanine attachment.

Kontron recommends Loctite 222 thread adhesive on the screws.

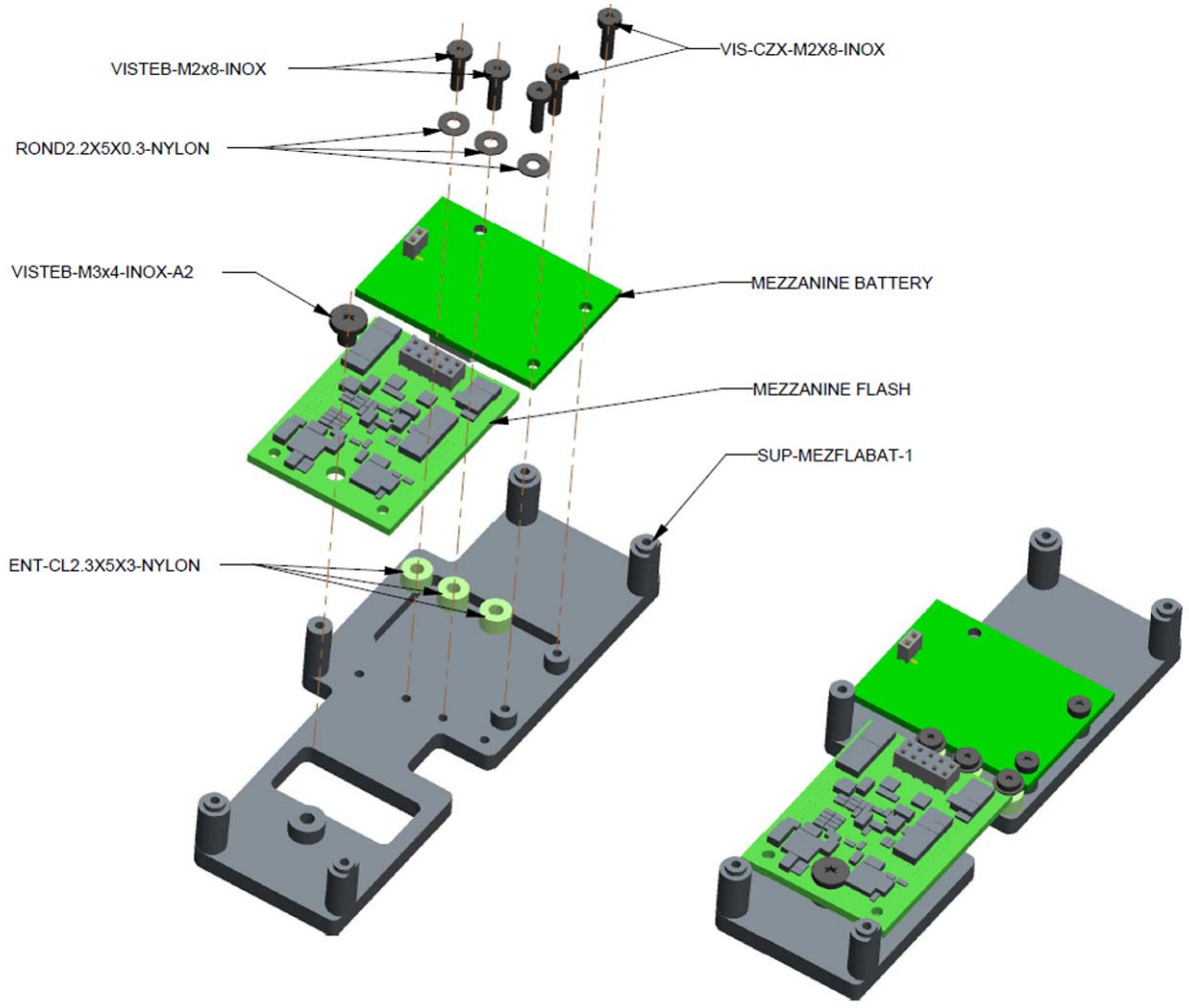


Figure 13: Mounting NAND device and/or battery mezzanine onto the holder with SUP-MEZFLABAT-1-V02

Then mount the holder and the NAND device onto the board with five M2 8mm stainless steel screws (Kontron P/N VIS-CZX-M2X8-INOX) as shown in Figure 14.

Kontron recommends Loctite 222 thread adhesive.

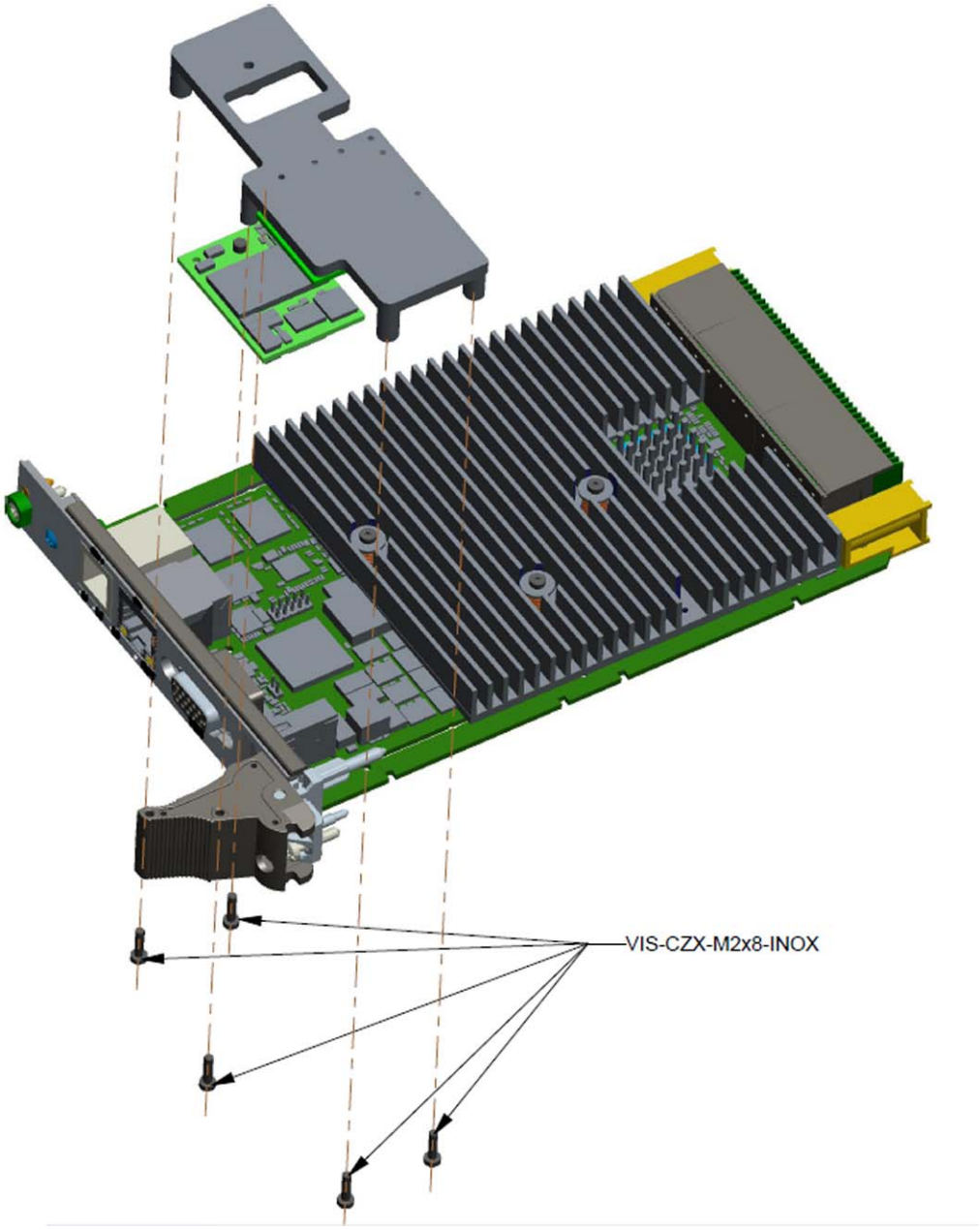


Figure 14: Mounting the holder SUP-MEZFLABAT-1-V02 with NAND device and/or battery mezzanine onto the VX3035 board

Order Code of the USB flash disk:

FDM-USB-*x*GB-2MM-IV: industrial version with conformal coating for use with rugged versions (*x* = up to 16 GB)

Order Code of the SATA NAND drive flash disk:

FDM-SATA-32GB-C0V: 32 GBytes MLC device, commercial grade

FDM-SATA-8GB-I0V: 8 GBytes SLC device, industrial grade

FDM-SATA-4GB-I0: 4 GBytes SLC device, industrial grade

Note For 16 GB and 32 GB SLC devices, please contact Kontron.

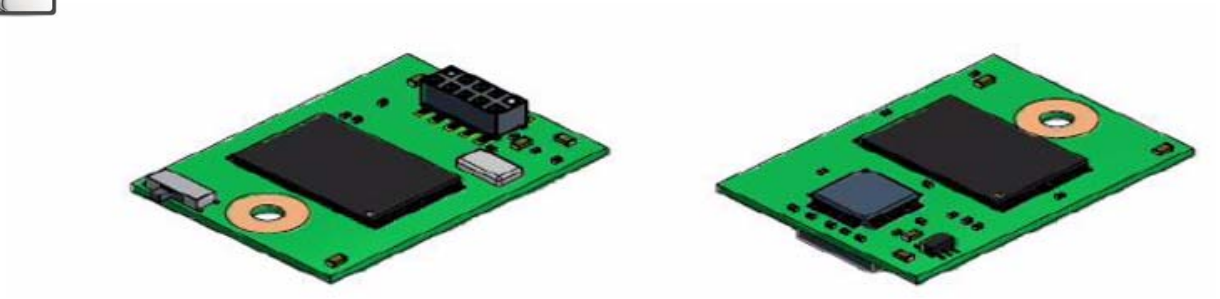


Figure 15: NAND Flash Disk Overview

2.7.2 Optional Battery Replacement

The lithium battery, when fitted, must be replaced with an identical battery or a battery type recommended by the manufacturer.

To replace the battery, proceed as follows:

> Turn off power.

> Unmount the holder (unscrew the five M2, 8mm, stainless steel screws) as shown in Figure 14 page 27.

> Unmount the battery mezzanine from the holder (unscrew the five M2, 8mm, stainless steel screws) as shown in Figure 13 page 26.

> Use a thin plastic tool to push the battery outside the safety cache. Push from the right or left top side of the safety cache.

> Remove the battery.

> Place the new battery in the socket.

> Make sure that you insert the battery the right way round. The positive pole (+) must be is on the top side (i.e. opposite to the mezzanine printed circuit).

> Mount back the battery mezzanine onto the holder as shown in in Figure 13 page 26.

> Mount back the holder onto the VX3035 board as shown in Figure 14 page 27.

Note Care must be taken to ensure that the battery is correctly replaced.
The battery should be replaced only with an identical or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Note Reference of the battery used on the VX3035: RAYOVAC BR2032
The design of an electronic circuit powered by a component class battery requires the designer to consider two interacting paths that determine a battery's life: consumption of active electrochemical components and thermal wear-out.

Battery Life

Figure 16 gives an estimate of years of service at various discharge currents for BR Lithium coin cells at room temperatures.

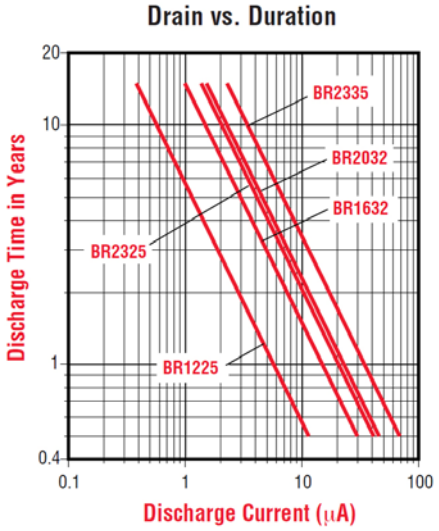


Figure 16: Battery Life

2.8 Software Installation

The installation of all onboard peripheral drivers is described in detail in the relevant Driver Kit files or Board Support Packages (BSP).

The installation of an operating system is dependent of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.

Chapter 3 - Additional Board Features

3.1 RTC, Watchdog, Timers

3.1.1 Real-Time Clock (RTC)

Two Real Time Clocks (RTC) are available on the VX3035 : one is embedded in the PCH while the other is a standalone, low power module located on the PCH I2C bus.

» Two date and time keeping schemes

The RTC can be used in two different ways, depending on build options:

RTC	Option IRTC (ie Internal RTC - default)	Option ERTC (ie External RTC - build option)
PCH RTC module	Keeps date and time when board is either powered on or powered off.	Keeps date and time when board is powered on. Not powered when board is powered off.
Standalone low power RTC module (RV8564C2/B)	Not used	Updated along with the PCH RTC when board is powered on. Keeps date and time when board is powered off.

» Standby power supplied to RTC

When the VX3035 is powered off, the RTC are powered either by the onboard battery (optional battery mezzanine) or through the 3.3V_AUX rail on the VPX backplane.

» Internal PCH RTC

The PCH RTC module provides a date and time keeping device with two banks of static RAM with 128 bytes each. Three interrupts are available. The power consumption in time keeping mode is 6 µA.

It is clocked by an external 32.768 KHz oscillator with a parabolic coefficient of 0.4 ppm/°C² and a stability of +/-20 ppm at 25°C. A 20 ppm stability is equivalent to a 10 mn/year drift.

» Standalone low power RTC RV8564

The RV8564C2/B RTC by Micro Crystal features an internal oscillator, date and time keeping module with programmable alarm, timer and interrupt functions. It has an ultra low power consumption in time keeping mode: 250 nA, typical and 500 nA, maximum. Its stability is 20 ppm at 25°C. It is connected to the PCH I2C bus.
.

3.1.2 CPLD Watchdog

The PLD includes a hardware Watchdog timer that can be used by the operating software to monitor the normal operation of the system.

The watchdog is enabled by software. Once enabled it must be restarted at regular intervals. If it is not restarted the watchdog will expire and cause an interrupt (IRQ) to the local processor or a board reset.

The watchdog module has following features:

- Watchdog refresh logic
- Two watchdog clocks: 1 KHz or 1 Hz
- Watchdog timeout:

  The watchdog timeout is programmable ranging from **1 clock period to 510 clock periods** by steps of 2 clock periods in the Watchdog Timer Control register
- Watchdog expiration mode management:

  The expiration mode is chosen in the Watchdog Timer Control register.

  There are 3 expiration modes:

  a. Timer only mode
  b. Reset mode
  c. Interrupt mode

3.2 I2C Structure

Two I2C busses allow access to several devices:

- One I2C bus driven by the PCH connecting to the SPD EEPROM holding the memory parameters, the standalone low power RTC, the ADS voltage sensor and the XDP debug interface.
- One I2C bus driven by the cPLD connecting to the Operating System EEPROM, the Vital Product Data EEPROM, a 512 kbit F-RAM, the LM3 thermal sensor and Nuvoton Hardware Monitoring device. All the devices on this bus are clocked at 100 KHz except for the F-RAM which is clocked at 1 MHz to optimise bandwith.

Two additionnal I2C busses, SMB0 and SMB1, are featured by the cPLD and buffered to P0.

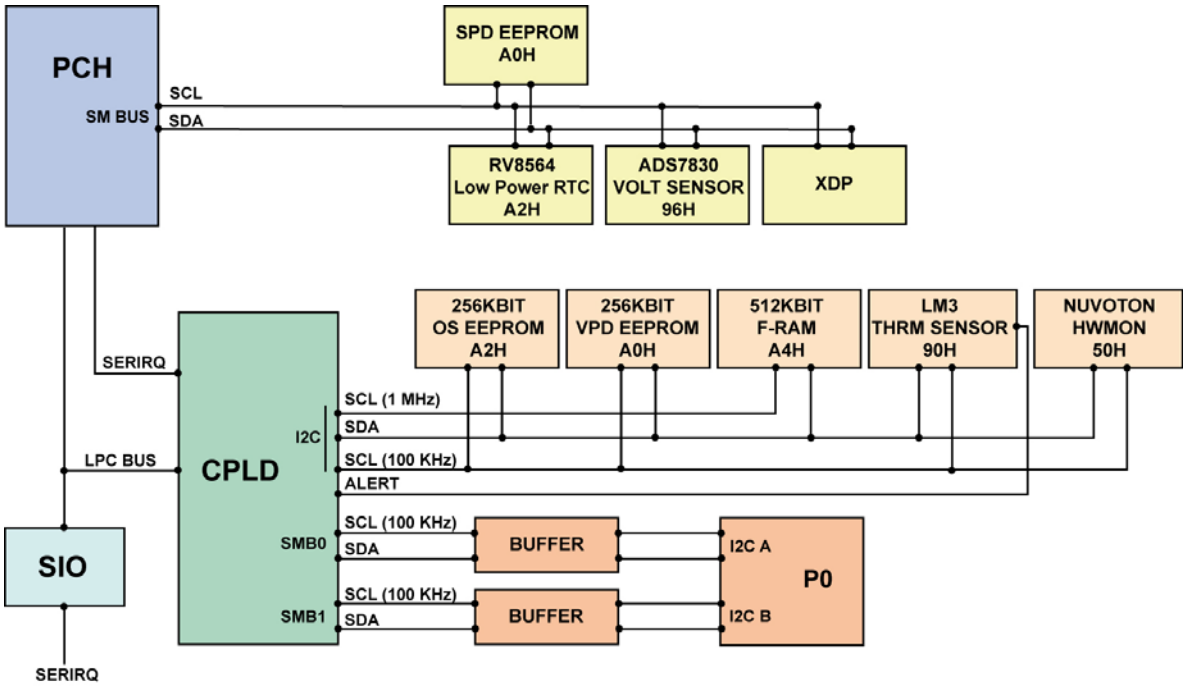


Figure 17: I2C Diagram

3.3 CPLD Features

The CPLD manages following features:

- Power-on/off control
- Reset control
- Local environmental control/monitoring
- LPC interface to processor
- I2C interfaces to I2C bus IPMB A/B (rear P0)
- LEDs control
- Serial lines multiplexer
- Serial VPD and user memories
- User and system GPIOs
- Internal registers that allow system management

VX3035 VPX I2C interfaces

VX3035 implements two I2C buses connected to P0 VPX connector (see P0 pin assignments):

I2C0 : CLK signal on pin P0/B5, DATA signal on pin P0/ A5

I2C1: CLK signal on pin P0/G4, DATA signal on pin P0/ F4

I2C bus 0 is a master/slave interface .

I2C bus 1 is a master only interface .

- **VPX I2C bus 0 / 1 master interfaces:**

VX3035 board slave address depends on VPX slot ID (slot geographical address = GA):

VPX Slot 1 (syscon): VX3035 slave address is 0x18 (I2C 7bits addressing)

VPX Slot 2: VX3035 slave address is 0x19 (I2C 7bits addressing)

VPX Slot 3: VX3035 slave address is 0x1A (I2C 7bits addressing)

And so on…..

Each board mapped at a unique I2C address implements two registers at register offset 0 (I2C_BOARD_STATUS) and offset 1 (I2C_BOARD_CONTROL). The register offset is sent to the board as a single byte I2C write.

These registers can also be accessed from CPU through LPC bus at I/O address 0x872 (I2C_BOARD_STATUS) and 0x873 (I2C_BOARD_CONTROL)

> I2C bus 0 slave registers definition :

I2C_BOARD_STATUS – When bit 3 of Register I2C_BOARD_CONTROL is set to 0				
Bit#	Name	Description	Reset	Type
7	Power Status	**Power Status** 0 Power Stand By 1 Power ON	0	RO
6-5	Reset Source	**Last Reset Source** 0x00 Internal PSUs power-on 0x01 Watchdog expired 0x10 SYSRESET (from VPX or VME) 0x11 Local reset : GPIO2 (maskable reset), reset switch, reset from I2C (reg I2C_BOARD_CONTROL), or reset by software asserting PLD_PLTRST_n (see bugzilla 6505)	0	RO
4	Reset Status	**Reset Status Side A** 0 No PWOK or reset asserted 1 PWOK and reset unasserted	0	RO
3-0	Boot Status	**Boot Status** 0x00 : RESET : default hardware value 0x01 : BIOS-BOOT : written by BIOS 0x02 : BIOS : written by BIOS 0x03 : PBIT : written by BIOS 0x04 : OS-BOOT : written by BIOS 0x05 : OS-RUNNING : to be written by OS at the end of boot 0x06 : COMPLETED : to be written by the final application when running 0x07 : SHUTDOWN : to be written by OS when issuing a halt/ shutdown 0x08 : REBOOT : to be written by OS when rebooting 0x09 - 0x0B : Reserved 0x0C - 0x0F : Customer defined These bits are Read Only through I2C Slave Interface and R/W through LPC Interface	0	RW

I2C_BOARD_STATUS – when bit 3 register I2C_BOARD_CONTROL is set to 1				
Bit#	**Name**	**Description**	**Reset**	**Type**
7-0	Power Debug 1	**This register indicates the level latched on the powergood signals when a power error is reported (Power Error bit set in reg I2C_BOARD_CONTROL).** Bit 7 : PWRGD_DDR Bit 6 : PWRGD_GFXCORE Bit 5 : PWRGD_P1V0 Bit 4 : PWRGD_P1V0PEX Bit 3 : PWRGD_P1V05IBEX Bit 2 : PWRGD_P1V05S Bit 1 : PWRGD_VCORE Bit 0 : PWRGD_0V85 These bits are **only valid once a power error is reported** (Power Error bit set in reg I2C_BOARD_CONTROL). ▸ the error is cleared by switching the board off (standby) or by removing VPX power ▸ an error is reported if the PSUs do not start within the expected delay (timeout). ▸ an error is reported if a PSU fails after being OK On older versions : ▸ the error is cleared only by removing VPX power. ▸ no PSU timeout is implemented (wait forever) ▸ an error is reported if a PSU fails after being OK	0	RO

I2C_BOARD_CONTROL – when Bit 3 of this register is set to 0				
Bit#	**Name**	**Description**	**Reset**	**Type**
7-4	Board Id	**Board Identification** 0011 VX3030 0101 VM6050 0110 VX6060 0111 VX3035 1000 VX3040 family	0	RO
3	Check_Errors	**Error Status Selection** 0 Default meaning for register I2C_BOARD_STATUS and register I2C_BOARD_CONTROL 1 Select Error Status for register I2C_BOARD_STATUS and register I2C_BOARD_CONTROL	0	RW
2	Reserved	**Reserved**	0	RW
1	Reset_3UA	**Reset Side A** 0 No Reset 1 Reset Assert	0	RW
0	Power_OnOff	**Power On/Off Control** 0 = Power Off (StandBy) 1 = Power On This bit can always be used to set power on or off, and its default value is set according to POWER_MODE Dip Switch (SW2[2]); 1 if switch is off; 0 if on.	N.A.	RW

I2C_BOARD_CONTROL - when Bit 3 of this register is set to 1				
Bit#	**Name**	**Description**	**Reset**	**Type**
7-4	Error Status	**Error Status** Bit 7 : PWRGD_3V3 Bit 6 : Power Error Bit 5 : Fatal Alert Bit 4 : Power Timeout ▸ PWRGD_3V3 : **only valid if a power error is reported**. As the signal 3UA_PLD_THRM_3V3PG_PROT# also reports a thermal alert, a thermal alert may be reported instead of a power error if alerts are not masked. ▸ Fatal alert is a thermal alert, a thermal trip or catastrophic error.	0	RO
3	Check_Errors	**Error Status Selection** 0 Select Board Identification for bits 7-4 of this register 1 Select Error Status for bits 7-4 of this register	0	RW
2-0	Power Debug 2	Bit 2 : PWRGD_P1V8S Bit 1 : PWRGD_VPX_OV Bit 0 : PWRGD_VPX_UV These bits are **only valid if a power error is reported** (Power Error bit set in I2C_BOARD_CONTROL)	0	RW

3.4 Serial Lines EIA-422/485 Additional Modes

A total of 2 serial lines are available on VX3035 product.

EIA-232 serial lines mode are available on front panel RJ12 and P2 connectors.

See section 4.1.1 page 39 - “Serial Connector” and section 4.3.3 page 49 - “P2 Connector” for more information on pin assignments.

EIA-232 serial lines mode is the default mode, but EIA-422/485 mode can also be set with the following mode:

Mode	RJ12 fron panel connector	P2 rear connector	RJ12 front pin assignment	P2 rear pin assignment
Default EIA-232	EIA-232: COM1	EIA-232: COM1, COM2	COM1 TXD: pin 3 COM1 RXD: pin 4 COM1 RTS: pin 1 COM1 CTS: pin 6	COM1 TXD: pin G3 COM1 RXD: pin G7 COM1 RTS: pin G1 COM1 CTS: pin G5 COM2 TXD: pin G11 COM2 RXD: pin G15
EIA-422/485 on COM1	EIA-422/485: COM1	EIA-422/485: COM1 EIA-422/485: COM2	COM1 TXD: pin 3 COM1 RXD: pin 4 COM1 TXD+: pin 1 COM1 RXD+: pin 6	COM1 TXD: pin G3 COM1 RXD: pin G7 COM1 TXD+: pin G1 COM1 RXD+: pin G5 COM2 TXD: pin G11 COM2 RXD: pin G15 COM2 TXD+: pin G9 COM2 RXD+: pin G13

Chapter 4 - Physical I/O

4.1 Front Panel Connectors

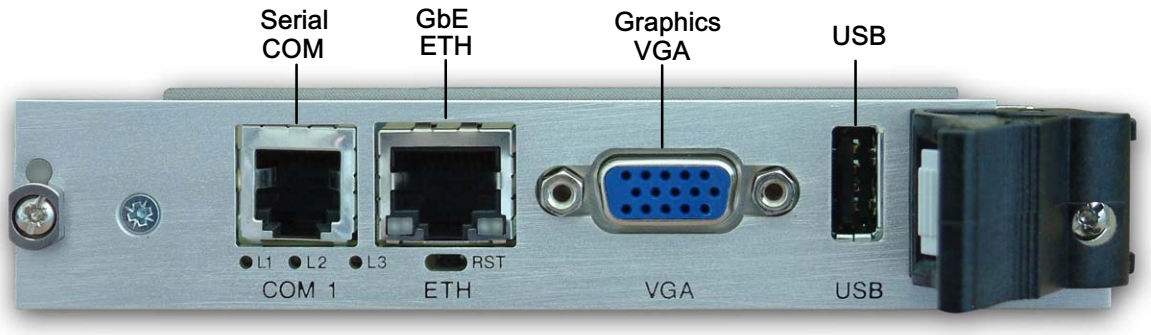


Figure 18: Location of the Front Panel Connectors

4.1.1 Serial Connector - COM

The VX3035 integrates two serial communications ports, COM1 and COM2 in PC parlance. COM1 and COM2 are available via the VPX P2 connector.

COM1 is also available via the front panel connector.

- COM1: EIA-232/485 (simplified RX/TX) port on RJ-12 front panel connector or on the rear P2 connector
- COM2: EIA-232/485 (simplified RX/TX) port on the rear P2 connector

Each serial port is configurable via the CPLD as EIA-232 or EIA-485. Each port operates in full duplex mode. Fast slew rate is the default mode in EIA-485 mode.

The signaling level of EIA-485 is compatible with EIA-422, so full duplex EIA-485 may also be used for point-to-point communications with an EIA-422 serial port.

Refer to section 4.3.3 “ P2 Connector” page 49 for more information on the serial lines wafer assignment on P2 connector.

Pin Assignment

PIN	SIGNAL
1	RTS/TXDb
2	Shell
3	TXD/TXDa
4	RXD/RXDa
5	GND
6	CTS/RXDb

Table 13: Serial Connector Pin Assignment

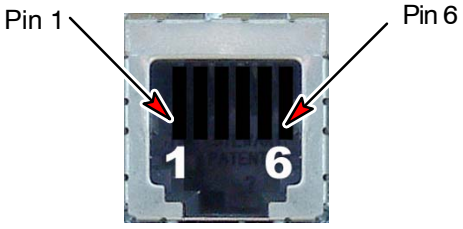


Figure 19: Serial Connector

A serial line should only be used via one connector at the same time, either the Serial front panel connector or the P2 connector.

MNEMONIC	DESCRIPTION
CTS/RXDb	EIA-232 Clear To Send / EIA-485 Receive Data (pair b)
RTS/TXDb	EIA-232 Request To Send / EIA-485 Transmit Data (pair b)
RXD/RXDa	EIA-232Receive Data / EIA-485 Receive Data (pair a)
TXD/TXDa	EIA-232 Transmit Data / EIA-485 Transmit Data (pair a)
GND	Ground
Shell	Chassis Ground

Table 14: Serial Connector Signal Description

Serial Cable

Kontron offers a RJ-12 solution without handshake support (no RTS/CTS signal) :

- Kontron Order Code KIT-2X-RJ12DB9
- Cable description:

Pin Connector DB9	Signal	Pin Connector RJ-12
2	TXD	3
3	RXD	4
5	GND	5

Other solutions including RJ-14 (6 pins, 4 conductors) or RJ-12 (6 pins, 6 conductors) can be found from multiple sources. For instance : http://www.trianglecables.com/db9m-rj12.html

4.1.2 Gigabit Ethernet Connectors

The Ethernet transmission should operate using a CAT5 cable with a maximum length of 100 m.

The Ethernet connectors are available as RJ-45 connectors with tab down. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

Pin Assignment

PIN	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-		I/O	BI_DC+
5	-	-	-		I/O	BI_DC-
6	I	RX-	I	RX-	I/O	BI_DB-
7	-	-	-		I/O	BI_DD+
8	-	-	-		I/O	BI_DD-
Shell	Chassis Ground					

Table 15: Gigabit Ethernet Connectors Pin Assignment

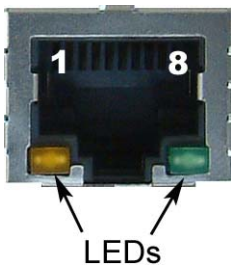


Figure 20: Ethernet Connector

Ethernet LEDs Status

- LNK/ACT (green)
  This LED monitors network connection and activity. The LED lights up when a valid link (cable connection) has been established. The LED goes temporarily off if network packets are being sent or received through the RJ-45 port. When this LED remains off, a valid link has not been established due to a missing or a faulty cable connection.
- SPEED LED (yellow/green)
  This LED indicates the link speed (10, 100, 1000 Mbps).

STATUS		SPEED LED yellow/green	LNK/ACT LED green
Ethernet Link is not established		OFF	OFF
10 Mbps	Ethernet Link Established	OFF	ON
	Ethernet Link Activity	OFF	BLINK
100 Mbps	Ethernet Link Established	ON (green)	ON
	Ethernet Link Activity	ON (green)	BLINK
1000 Mbps	Ethernet Link Established	ON (yellow)	ON
	Ethernet Link Activity	ON (yellow)	BLINK

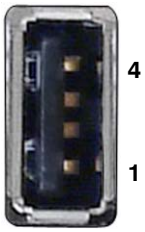
Table 16: Ethernet LEDs Status Definition

4.1.3 USB Connector

Pin Assignment

PIN	SIGNAL	FUNCTION	I/O
1	VCC (+5V Protected)	VCC	--
2	USB_D-	Differential USB-	I/O
3	USB_D+	Differential USB+	I/O
4	GND	GND	--

Table 17: USB Connector Pin Assignment



USB

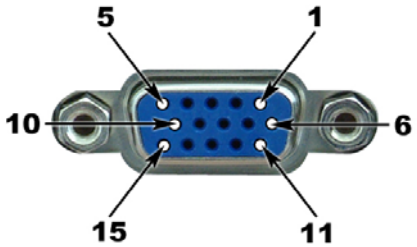
Figure 21: USB Connector

4.1.4 VGA Connector

Pin Assignment

PIN	SIGNAL	FUNCTION	I/O
1	Red	Red Video Signal Output	O
2	Green	Green Video Signal Output	O
3	Blue	Blue Video Signal Output	O
4	N.C.	Not Connected	-
5	GND	Ground Signal	-
6	GND	Ground Signal	-
7	GND	Ground Signal	-
8	GND	Ground Signal	-
9	VCC	Power +5V 1.5 A fuse protection	O
10	GND	Ground Signal	-
11	N.C.	Not Connected	-
12	Sdata	I2C Data	I/O
13	Hsync	Horizontal Sync	TTL Out
14	Vsync	Vertical Sync	TTL Out
15	Sclk	I2C Clock	I/O

Table 18: VGA Connector Pin Assignment



VGA

Figure 22: VGA Connector

4.2 Onboard Connectors

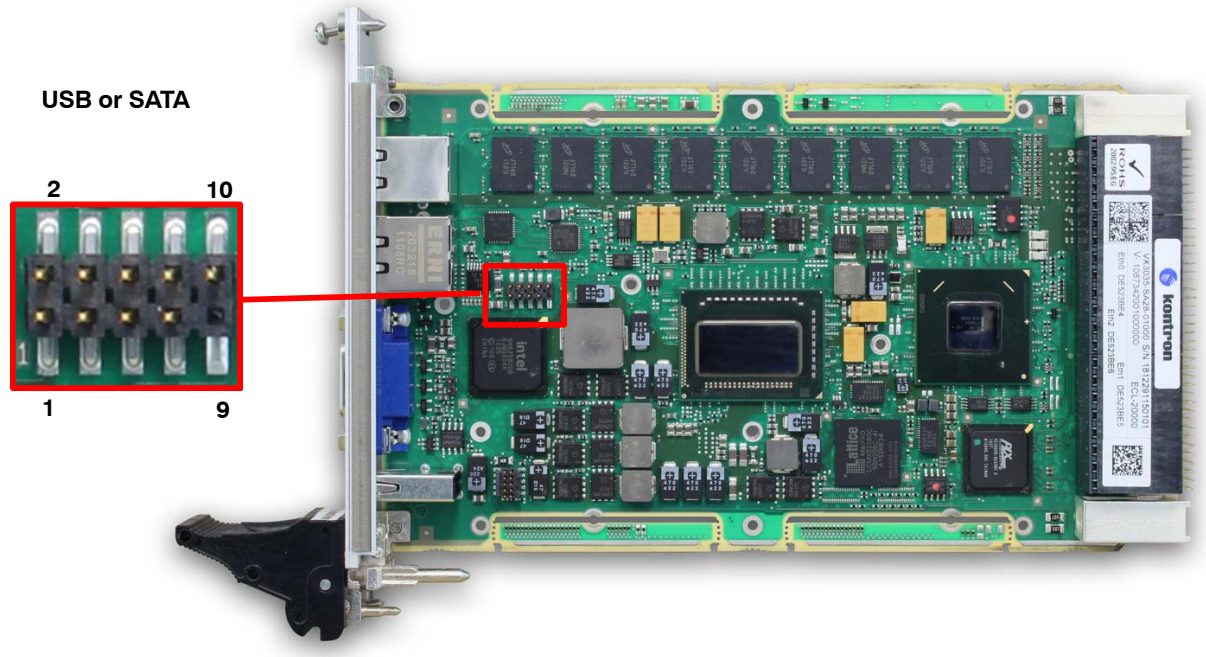


Figure 23: Onboard Connectors

Onboard NAND Flash Connector

The onboard NAND flash connector provides both a USB interface and a SATA interface for attaching either a USB Flash Disk Module (low profile USB flash mezzanine card,2 mm connector) or a SATA NAND Flash module.

The following table provides pinout information for both interfaces:

PIN	SIGNAL	FUNCTION	I/O
1	PWR	VCC	-
2	SATA RX+	SATA VX3035 receive+	I
3	Data-	Differential USB-	I/O
4	SATA RX-	SATA VX3035 receive-	I
5	Data+	Differential USB+	I/O
6	RSV	GND	-
7	GND	Ground	-
8	SATA TX+	SATA VX3035 transmit+	O
9	N.C.	Not Connected	-
10	SATA TX-	SATA VX3035 transmit-	O

Table 19: Onboard NAND Flash Pin Assignment

4.3 Rear Connectors

VPX Bus Interface

The complete 3U VPX connector configuration comprises three connectors named P0 to P2:

- P0: 8-wafer 7-row connector.
- P1 - P2: 16-wafer 7-row differential connectors.

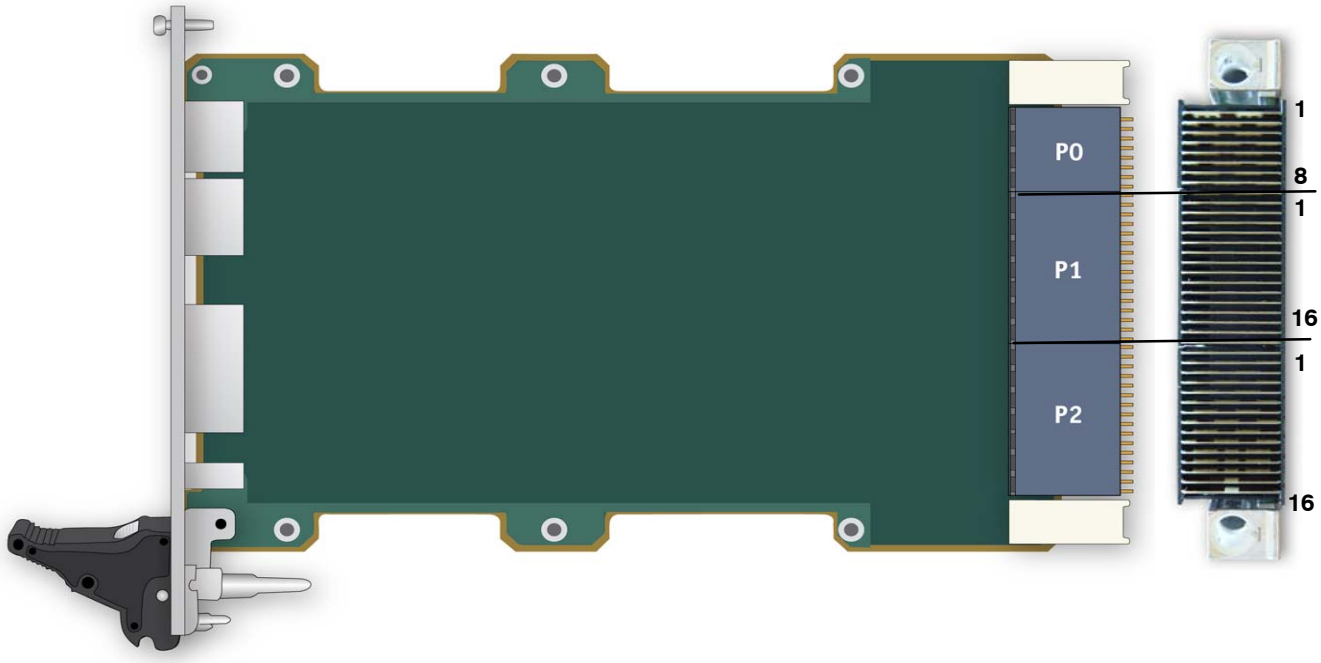


Figure 24: VPX Connectors

4.3.1 P0 Connector

P0 Wafer Assignment

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	+12V	+12V	+12V	NC	NC	NC	NC
2	+12V	+12V	+12V	NC	NC	NC	NC
3	+5V	+5V	+5V	NC	+5V	+5V	+5V
4	I2C1 CLK	I2C1 DAT	GND	NC (-12V_AUX)	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3V3_AUX	GND	I2C0 CLK	I2C0 DAT
6	GA3*	GA2*	GND	NC (+12V_AUX)	GND	GA1*	GA0*
7	GPIO5 (TCK)	GND	PCIe_CLK- (TDO)	PCIe_CLK+ (TDI)	GND	GPIO3 (TMS)	GPIO4 (TRST)
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND
CASE	GND						

* signal active when low

Table 20: VPX Connector P0 Wafer Assignment

P0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
+12V	+12 Volts DC power (VS1 VPX supply). NC (+12V) pins are not connected (VS2 VPX supply)
+5V	+5 Volts DC power (VS3 VPX supply)
+3V3	NC
NVMRO	Non-Volatile Memory Read Only. When asserted (logical 1), prevents any non-volatile memory from being updated.
GAi	Geographical address pins
GAP	Geographical address parity
GND	Ground
GPIO	General Purpose I/Ox (handled by the CPLD A). JTAG signals are not used on P0.
I2C0	I2C Bus 0
I2C1	I2C Bus 1
REF_CLK+/-	The Reference Clock is a bussed differential pair. Output if the VX3035 is plugged in the system controller slot, input otherwise. It enables the entire system to synchronize to a common time reference if desired. Counter/timer in the CPLD can use this clock
AUX_CLK+/-	1 PPS (one pulse per second) clock input. Can be programmed as an output on system controller slot. Can be used to phase the CPLD timer/counter clocked by REF_CLK+/-.
PCIe_CLK+/-	Optional Common Reference PCI Express Clock input. Can also be programmed as an output.
SYSRESET*	System Reset. Input and open collector output.

Table 21: VPX Connector P0 Signal Definition

4.3.2 P1 Connector

P1 Wafer Assignment

> Legend for Table 22:

P1_VBAT	Battery Voltage	USB2/3	USB links 2 and 3 from PCH
P1_SYS_CON*	System Controller	SATA0/3	SATA links 0 and 3 from PCH
P1_REFCLK0-SE	Single ended Reference Clocks	ETHx TX/RX	1000BASE-BX links 0 and 1 from Dual GbE i82580
PCIe0 LxRX | LxTX	x4 or 4x1 PCI-Express from CPU	ETH DA/DB/DC/DD	1000BASE-T link from GbE i82577

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	GDISCRETE1	GND	PCIe0 L0-TX-	PCIe0 L0-TX+	GND	PCIe0 L0-RX-	PCIe0 L0-RX+
2	GND	PCIe0 L1-TX-	PCIe0 L1-TX+	GND	PCIe0 L1-RX-	PCIe0 L1-RX+	GND
3	VBAT	GND	PCIe0 L2-TX-	PCIe0 L2-TX+	GND	PCIe0 L2-RX-	PCIe0 L2-RX+
4	GND	PCIe0 L3-TX-	PCIe0 L3-TX+	GND	PCIe0 L3-RX-	PCIe0 L3-RX+	GND
5	SYS_CON*	GND	NC	NC	GND	NC	NC
6	GND	NC	NC	GND	NC	NC	GND
7	P1-REF_CLK_SE	GND	NC	NC	GND	NC	NC
8	GND	NC	NC	GND	NC	NC	GND
9	USB2 PWR	GND	SATA0 TX-	SATA0 TX+	GND	SATA0 RX-	SATA0 RX+
10	GND	SATA3 TX-	SATA3 TX+	GND	SATA3 RX-	SATA3 RX+	GND
11	USB3 PWR	GND	NC	NC	GND	NC	NC
12	GND	USB2 DA-	USB2 DA+	GND	USB3 DA-	USB3 DA+	GND
13	GPIO1	GND	ETH DB-	ETH DB+	GND	ETH DA-	ETH DA+
14	GND	ETH DD	ETH DD+	GND	ETH DC-	ETH DC+	GND
15	Maskable Reset* or GPIO2	GND	ETH1 TX-	ETH1 TX+	GND	ETH1 RX-	ETH1 RX+
16	GND	ETH0 TX-	ETH0 TX+	GND	ETH0 RX-	ETH0 RX+	GND
CASE	GND						

* signal active when low

Table 22: VPX Connector P1 Wafer Assignment

P1 Signal Definition

MNEMONIC	SIGNAL DEFINITION
P1-REF_CLK_SE	Reserved
PCIe0 L*x*-RX+/-	x4 PCI Express Link. Receive +/- Can also be used as a 4 x1 links
PCIe0 Lx-TX+/-	x4 PCI Express Link. Transmit +/- Can also be used as a 4 x1 links.
SATAx RX+/-	Serial ATA. Receive +/- link x
SATAx TX+/-	Serial ATA. Transmit +/- link x
USBx PWR	USB Power link x
USBx D+/-	Differential Data pair of USB link x
ETH DA+/-	Ethernet 1000BASE-T: First pair of transmit/receive data.
ETH DB+/-	Ethernet 1000BASE-T: Second pair of transmit/receive data
ETH DC+/-	Ethernet 1000BASE-T: Third pair of transmit/receive data.
ETH DD+/-	Ethernet 1000BASE-T: Fourth pair of transmit/receive data
ETHx RX+/-	1000BASE-BX Ethernet x: Receive data +/-
ETHx TX+/-	1000BASE-BX Ethernet x: Transmit data +/-
GPIOx	General Purpose I/Ox (handled by the CPLD)
Maskable Reset*	Optional reset input for this module. May be left unconnected if not used.
GND	Ground
SYS_CON*	System Controller Slot Indication
VBAT	Battery Voltage Input, 3V. Optional alternated source for RTC backup voltage.

Table 23: VPX Connector P1 Signal Definition

4.3.3 P2 Connector

P2 Wafer Assignment

> Legend for Table 24:

COM1/2	Simplified Serial Lines	PCIe_TX/RX	Additionnal PCI express x1 link from PCH
USB4/5	USB links from PCH	PCIe_CLK	Additionnal PCI express clock from PCH
SATA1/2	SATA links from PCH		
eDP-A/B	Digital ports A and B from PCH		

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	COM1_RTS or COM1 TXD+	GND	SATA1 TX-	SATA1 TX+	GND	SATA1 RX-	SATA1 RX+
2	GND	SATA2 TX-	SATA2 TX+	GND	SATA2 RX-	SATA2 RX+	GND
3	COM1 TXD	GND	USB4 PWR	USB4 PWR	GND	USB5 PWR	USB5 PWR
4	GND	USB4 DA-	USB4 DA+	GND	USB5 DA-	USB5 DA+	GND
5	COM1 CTS or COM1 RXD+	GND	eDP-A 1-	eDP-A 1+	GND	eDP-A 0-	eDP-A 0+
6	GND	eDP-A 3-	eDP-A 3+	GND	eDP-A 2-	eDP-A 2+	GND
7	COM1 RXD	GND	eDP-B HPD	eDP-A HPD	GND	eDP-A AUX-	eDP-A AUX+
8	GND	eDP-B 1-	eDP-B 1+	GND	eDP-B 0-	eDP-B 0+	GND
9	COM2 TXD+	GND	eDP-B 3-	eDP-B 3+	GND	eDP-B2-	eDP-B 2+
10	GND	PCIe CLK-	PCIe CLK+	GND	eDP-B AUX-	eDP-B AUX+	GND
11	COM2 TXD	GND	PCIe TX-	PCIe TX+	GND	PCIe RX-	PCIe RX+
12	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
13	COM2 RXD+	GND	Reserved	Reserved	GND	Reserved	Reserved
14	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
15	COM2 RXD	GND	Reserved	Reserved	GND	Reserved	Reserved
16	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
CASE	GND						

* signal active when low

Table 24: VPX Connector P2 Wafer Assignment

P2 Signal Definition

MNEMONIC	SIGNAL DEFINITION
COMx	Serial Lines, EIA-232/EIA-485
USBx PWR	USB Power link x
USBx D+/-	Differential Data pair of USB link x
SATAx RX+/-	Serial ATA. Receive +/- link x
SATAx TX+/-	Serial ATA. Transmit +/- link x
eDPx	embedded Display Port
PCIe1 TX/RX	Additional PCI-Express x1 link
PCIe1 CLK	Common Reference Clock Output for PCIe1
Reserved	Reserved, do not connect
GND	Ground

Table 25: VPX Connector P2 Signal Definition

4.3.4 XDP

Standard XDP debug connector can be made available through a dedicated adapter board:

- For VX3035 boards with E.C. Level 20xxx to 20006: OT-XDP-VX3035-A-00
- For VX3035 boards with E.C. Level 20007 or 30xxx: OT-XDP-VX3035-A-01

Pin	MNEMONIC	SIGNAL DEFINITION	Pin	MNEMONIC	SIGNAL DEFINITION
1	GND	Ground	2	GND	Ground
3	3UA_ETH1_BH_MDI0_P	Ethernet 1000BASE-T ETH1: pair 0	4	3UA_ETH0_BH_MDI0_P	Ethernet 1000BASE-T ETH0: pair 0
5	3UA_ETH1_BH_MDI0_N	Ethernet 1000BASE-T ETH1: pair 0	6	3UA_ETH0_BH_MDI0_N	Ethernet 1000BASE-T ETH0: pair 0
7	GND	Ground	8	GND	Ground
9	3UA_ETH3_BH_MDI0_P	Ethernet 1000BASE-T ETH3: pair 0	10	3UA_ETH2_BH_MDI0_P	Ethernet 1000BASE-T ETH2: pair 0
11	3UA_ETH3_BH_MDI0_N	Ethernet 1000BASE-T ETH3: pair 0	12	3UA_ETH2_BH_MDI0_N	Ethernet 1000BASE-T ETH2: pair 0
13	GND	Ground	14	GND	Ground
15	3UA_ETH1_BH_MDI1_P	Ethernet 1000BASE-T ETH1: pair 1	16	3UA_ETH0_BH_MDI1_P	Ethernet 1000BASE-T ETH0: pair 1
17	3UA_ETH1_BH_MDI1_N	Ethernet 1000BASE-T ETH1: pair 1	18	3UA_ETH0_BH_MDI1_N	Ethernet 1000BASE-T ETH0: pair 1
19	GND	Ground	20	GND	Ground
21	3UA_ETH3_BH_MDI1_P	Ethernet 1000BASE-T ETH3: pair 1	22	3UA_ETH2_BH_MDI1_P	Ethernet 1000BASE-T ETH2: pair 1
23	3UA_ETH3_BH_MDI1_N	Ethernet 1000BASE-T ETH3: pair 1	24	3UA_ETH2_BH_MDI1_N	Ethernet 1000BASE-T ETH2: pair 1
25	GND	Ground	26	GND	Ground
27	3UA_ETH1_BH_MDI2_P	Ethernet 1000BASE-T ETH1: pair 2	28	3UA_ETH0_BH_MDI2_P	Ethernet 1000BASE-T ETH0: pair 2
29	3UA_ETH1_BH_MDI2_N	Ethernet 1000BASE-T ETH1: pair 2	30	3UA_ETH0_BH_MDI2_N	Ethernet 1000BASE-T ETH0: pair 2
31	GND	Ground	32	GND	Ground
33	3UA_ETH3_BH_MDI2_P	Ethernet 1000BASE-T ETH3: pair 2	34	3UA_ETH2_BH_MDI2_P	Ethernet 1000BASE-T ETH2: pair 2
35	3UA_ETH3_BH_MDI2_N	Ethernet 1000BASE-T ETH3: pair 2	36	3UA_ETH2_BH_MDI2_N	Ethernet 1000BASE-T ETH2: pair 2
37	GND	Ground	38	GND	Ground
39	3UA_ETH1_BH_MDI3_P	Ethernet 1000BASE-T ETH1: pair 3	40	3UA_ETH0_BH_MDI3_P	Ethernet 1000BASE-T ETH0: pair 3

Pin	MNEMONIC	SIGNAL DEFINITION	Pin	MNEMONIC	SIGNAL DEFINITION
41	3UA_ETH1_BH_MDI3_N	Ethernet 1000BASE-T ETH1: pair 3	42	3UA_ETH0_BH_MDI3_N	Ethernet 1000BASE-T ETH0: pair 3
43	GND	Ground	44	GND	Ground
45	3UA_ETH3_BH_MDI3_P	Ethernet 1000BASE-T ETH3: pair 3	46	3UA_ETH2_BH_MDI3_P	Ethernet 1000BASE-T ETH2: pair 3
47	3UA_ETH3_BH_MDI3_N	Ethernet 1000BASE-T ETH3: pair 3	48	3UA_ETH2_BH_MDI3_N	Ethernet 1000BASE-T ETH2: pair 3
49	GND	Ground	50	GND	Ground
51	Reserved	Reserved. Do not connect.	52	Reserved	Reserved. Do not connect.
53	Reserved	Reserved. Do not connect.	54	Reserved	Reserved. Do not connect.
55	GND	Ground	56	GND	Ground
57	Reserved	Reserved. Do not connect.	58	Reserved	Reserved. Do not connect.
59	Reserved	Reserved. Do not connect.	60	GND	Ground
61	GND	Ground	62	3UA_ITPCLK_P	XDP interface
63	3UA_PM_CLKRUN#	LPC interface	64	3UA_ITPCLK_N	XDP interface
65	3UA_P2701_1V05S	XDP interface	66	3UA_F2701C	+5V
67	3UA_XDP_PREQ#	XDP interface	68	3UA_F2701C	+5V
69	3UA_XDP_PRDY#	XDP interface	70	3UA_XDP_SMB_CLK	LPC interface
71	GND	Ground	72	GND	Ground
73	3UA_XDP_DBR#	XDP interface	74	3UA_XDP_SMB_DAT	LPC interface
75	3UA_R_CPUPWRGD	XDP interface	76	3UA_XDP_TDI	XDP interface
77	3UA_XDP_TDO	XDP interface	78	3UA_XDP_TRST#	XDP interface
79	3UA_XDP_TCK	XDP interface	80	GND	Ground
81	GND	Ground	82	3UA_XDP_TMS	XDP interface
83	3UA_DLPC_LAD0	LPC interface	84	XDP_CFG0_CONN	ECLevel 20xxx: NC EClevel 30xxx: ETH1 activity LED
85	3UA_DLPC_LAD1	LPC interface	86	3UA_F2701A	+12V
87	3UA_DLPC_LAD3	LPC interface	88	ECLevel 20xxx : 3UA_F2701A EClevel 30xxx : DP_CPU_CFG0	ECLevel 20xxx : +12V EClevel 30xxx : XDP interface
89	3UA_DLPC_LAD2	LPC interface	90	Reserved	Reserved. Do not connect.
91	3UA_DLPC_FRAME#	LPC interface	92	GND	Ground
93	3UA_DLPC_SERIRQ	LPC interface	94	3UA_F2701B	+3.3V
95	GND	Ground	96	3UA_F2701B	+3.3V
97	3UA_DLPC_CLK	LPC interface	98	3UA_R_CPURST#	ECLevel 20xxx : NC ECLevel 30xxx : ETH1 link LED
99	3UA_PM_SUS_STAT#	LPC interface	100	3EA_R_PLD_RESETOUT#	LPC interface

Table 26: XDP Connector Pin Assignment and Signal Definition

4.4 LEDs

Status LEDs Default Setting

There are three bicolor LEDs (Red/Green) on the front panel of the VX3035 3U VPX board. A third color (orange) is emitted by adding red and green lights.

Figure 25: LEDs Front panel

CPU LED	COLOR	DESCRIPTION
L1	RED	Permanent error
	GREEN	Internal power OFF (standby)
	ORANGE	Reset state
	BLINK (GREEN)	Blinking during CPLD activity
	OFF	Internal Power OK
L2 (1)	RED	CPLD watchdog reset timer has expired
	GREEN	Normal operation mode
	ORANGE	Factory test mode
	BLINK (GREEN)	Blinking during SATA activity
L3 (1)	RED	Processor hot, may trigger processor performance limitations
	GREEN	Ethernet ETH connector valid on front panel
	ORANGE	Ethernet ETH link directed to backplane
	BLINK (GREEN)	Blinking during ETH link activity

(1) The color of these LEDs may also be fixed by software through CPLD registers

Table 27: LEDs Description

Chapter 5 - Power and Thermal Specifications

5.1 Power Specifications

All frequency and power data have been measured with Intel Thermal Analysis Tool (TAT) software on actual Sandy Bridge processor silicons. The Kontron BSP Fedora 14 was running TAT 100% on all cores, standard glxgears test, and memory, FFT, SATA, LPC and FRAM benchmarks.

Connected peripherals were 2 SATA devices, USB keyboard/mouse, front Gigabit Ethernet and VGA interface, rear 1000BASE-BX and PCIe links. The memory configuration was a dual bank DDR3.

5.1.1 VX3035 Thermal Power

The following data show processor's and board power consumptions in different test configurations. These data, meant to help defining the thermal power dissipation budget, come from measurements done in operational conditions on early field Sandy Bridge parts.

VX3035-SA24-00000			
Power mode	CPU Power Consumption	Max Total Power Consumption	Test Conditions (Turbo Mode Disabled)
Idle Linux, 0.8 GHz	5.5W	27W	Idle Linux. No interfaces
Complex tests, typical load configuration, 2.2 GHz	20W	45W	Standard interfaces: VGA, DP, front 1000BASE-T, 1x SATA, keyboard/mouse, CPU running FFT, DDR, SATA)
Complex tests, maximum load configuration, 2.2 GHz	20.5W	49W	Standard interfaces : VGA, DP, front 1000Base-T, 2x SATA, 3 USB, keyboard/ mouse, CPU running FFT, DDR, SATA, Ethernet, X11 perf)
TAT 100%, 2.2 GHz	24W	46W	TAT Intel Software Tool
TAT 1.4 GHz	16W	33W	TAT Intel Software Tool

Table 28: VX3035 Power Consumption

5.1.2 VX3035 Maximum Currents

The following data provide maximum current values on VPX VS1 (12V) and VS3 (5V) power rails. The VPX VS2 (3.3V) is not connected.

Power mode	Max Current on VS1 (12V)	Max Current on VS3 (V)	Test Conditions (Turbo Mode Disabled)
Idle Linux, 0.8 GHz	1.2A	2.5A	Idle Linux. No interfaces
Complex tests, typical load configuration, 2.2 GHz	2.6A	2.6A	Standard interfaces: VGA, DP, front 1000BASE-T, 1x SATA, keyboard/mouse, CPU running FFT, DDR, SATA)
Complex tests, maximum load configuration, 2.2 GHz	2.7A	3.2A	Standard interfaces: VGA, DP, front 1000BASE-T, 2x SATA, 3 USB, keyboard/ mouse, CPU running FFT, DDR, SATA, Ethernet, X11 perf)
TAT 100%, 2.2 GHz	2.7A	2.8A	TAT Intel Software Tool
TAT 1.4 GHz	1.6A	2.6A	TAT Intel Software Tool

Table 29: VX3035 Maximum Currents

5.1.3 Power supplies specifications at power-up and during power-off.

At power-up, a monotonic rise time between 20 and 150 ms is required on VPX VS1 (12V) and VS3 (5V) power rails.

For a power-off condition to be valid, the VPX power supplies should remain at 0V for at least one second.

5.2 Board Thermal Monitoring

To ensure optimal and long-term reliability of the VX3035, all onboard components must remain within the maximum temperature specifications. The most critical components on the VX3035 are the processor and the memory. Operating the VX3035 above the maximum operating limits will result in permanent damage to the board.

The VX3035 includes two temperature sensors, the LM73CIMK-0 by National Semiconductor on top side of the board and the NCT7802Y by Nuvoton on bottom side, both managed by the CPLD through its I2C bus. Refer to Figure 17 “I2C Diagram” page 31.

Key Features of the Temperature Sensors

Sensor	Sensor accuracy	Operating Temperature Range
National Semiconductor LM73CIMK-0	+/- 2°C	-40 °C / +150°C
Nuvoton NCT7802Y	+/- 2°C	-40°C / +85°C

Location of the Temperature Sensors

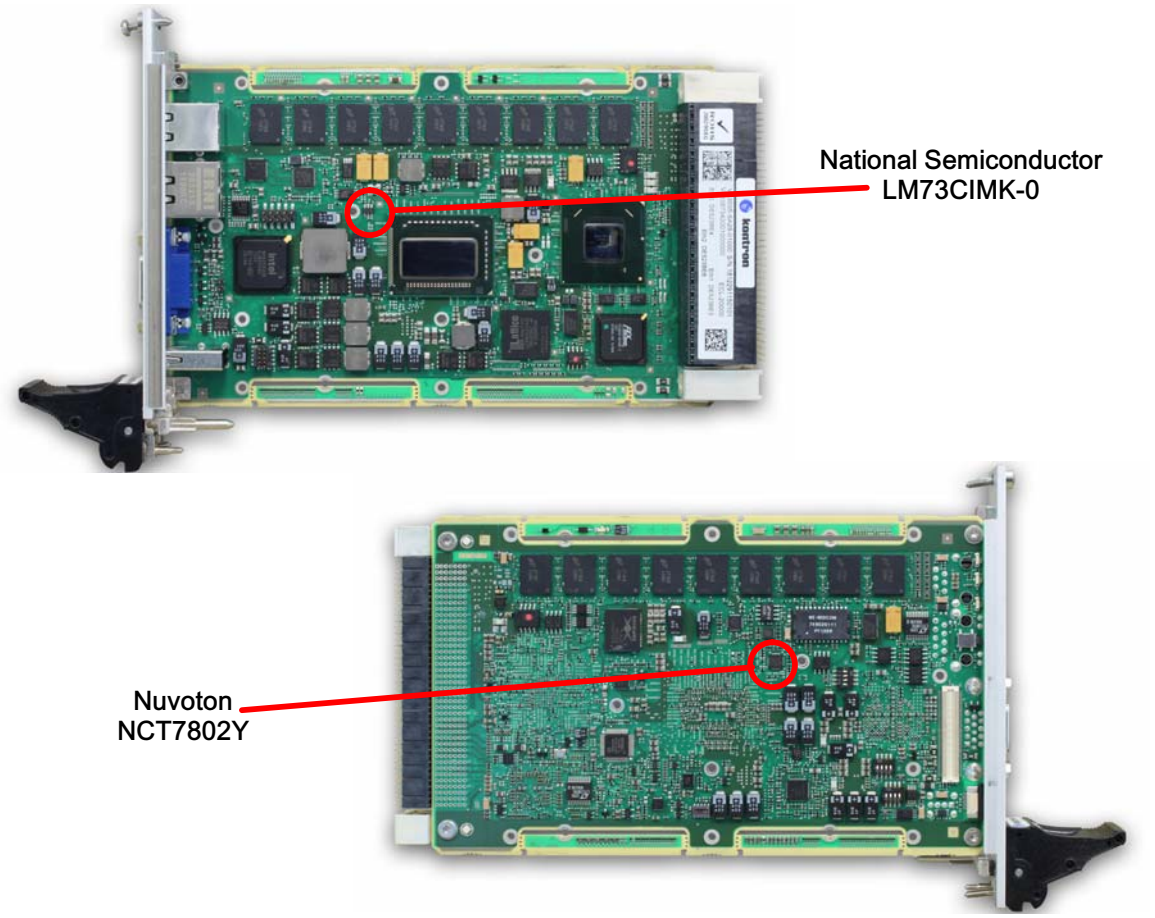


Figure 26: Board Temperature Sensors Location

5.3 CPU Thermal Monitoring

CPU Temperature

The maximum specified junction temperature of the processor, TjMAX, is set to 100°C for the SandyBridge processor. Attempts to operate above this temperature will cause the processor to throttle which will result in automatic reduction of the core frequency but may eventually cause irreversible damage to the board.

A VX3035-SA28-01000 in a 1 inch slot, at 55°C, and operating at 2.2 GHz needs a 2 m/s controlled linear airflow. Considering that most chassis will display some airflow differences from one slot to another, and that the fans will not deliver a truly linear airflow, it is advised to target an airflow of 2.5 m/s.

For a VX3035-SA28-00000 in a 0.8 inch slot, at 55°C, and operating at 2.2 GHz, a controlled linear airflow of 2.5 m/s is required (3 m/s in a chassis).

Please contact Kontron for detailed figures.

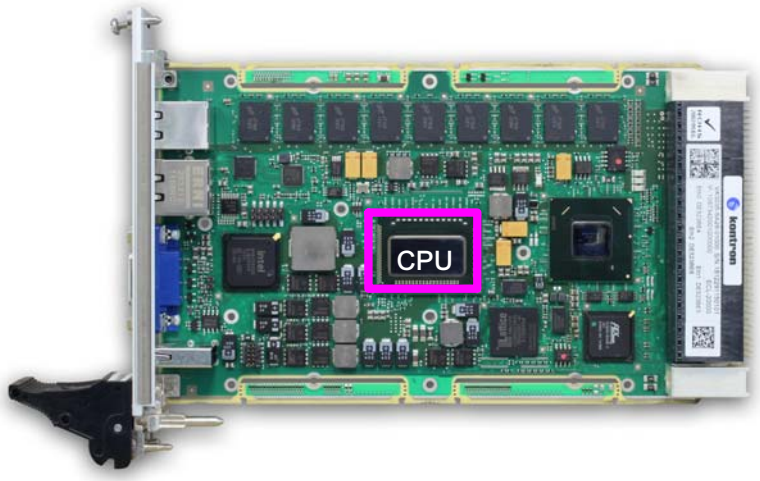
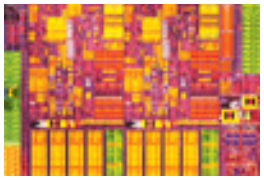


Figure 27: VX3035 Thermal Performance for 1" slot

The CPU temperature is also accessible through the Linux sensors driver. Refer to the Release Notes for BSP Fedora 12 (SD.DT.F72), section “BSP Specific Features - Sensors” for more information on this topic.

Intel® Turbo Boost Technology



Intel® Turbo Boost Technology is one of the many exciting features that Intel has built into latest-generation Intel® microarchitecture. It automatically allows processor cores to run faster than the base operating frequency if it's operating below power, current, and temperature specification limits.

Dynamically increasing performance

Intel Turbo Boost Technology is activated when the Operating System (OS) requests the highest processor performance state (P0).

The maximum frequency of Intel Turbo Boost Technology is dependent on the number of active cores. The amount of time the processor spends in the Intel Turbo Boost Technology state depends on the workload and operating environment.

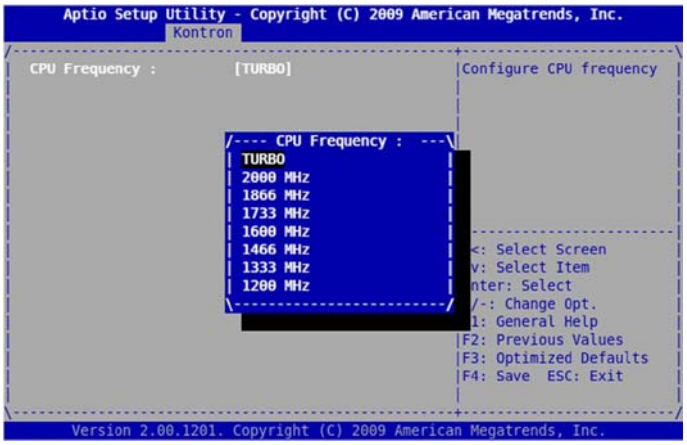
Any of the following can set the upper limit of Intel Turbo Boost Technology on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency will dynamically increase by 133 MHz on short and regular intervals until the upper limit is met or the maximum possible upside for the number of active cores is reached.

Learn more about Intel Turbo Boost Technology: http://www.intel.com/technology/turboboost/

> The Intel Turbo Boost is handled by the BIOS through the CPU configuration menu.



Refer to the AMI BIOS for VX3035 - User Reference Manual (SD.DT.F97), section “CPU Configuration”.

The default setting of turbo mode is ON. To operate at constant frequency, disable turbo mode in BIOS settings. Refer to "VX3035 - AMI BIOS User Reference Manual" SD.DT.F97.

Chapter 6 - Backplane Suggestions

Kontron can offer for development or deployment of the VX3035 the following backplane models:

» Single Star x4

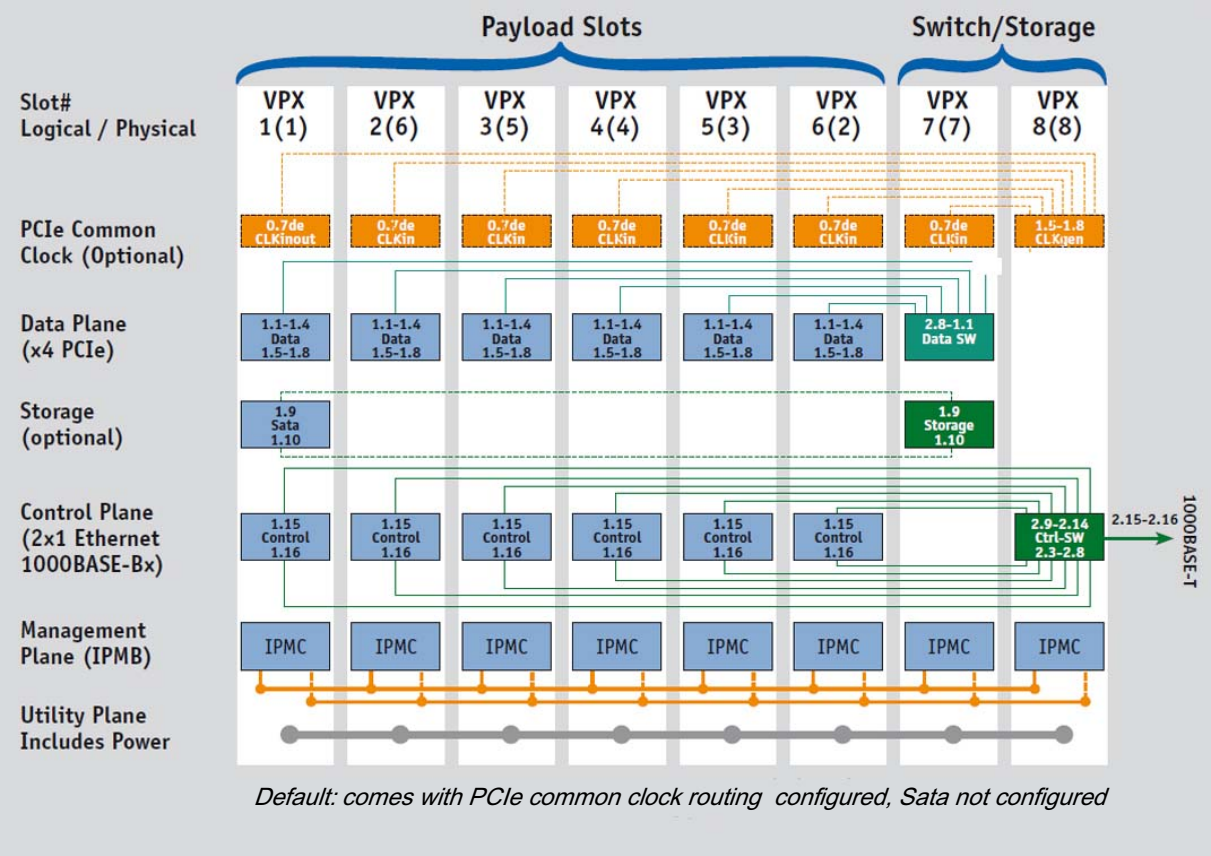


Figure 28: Single Star x4 Topology

Dual Star x4

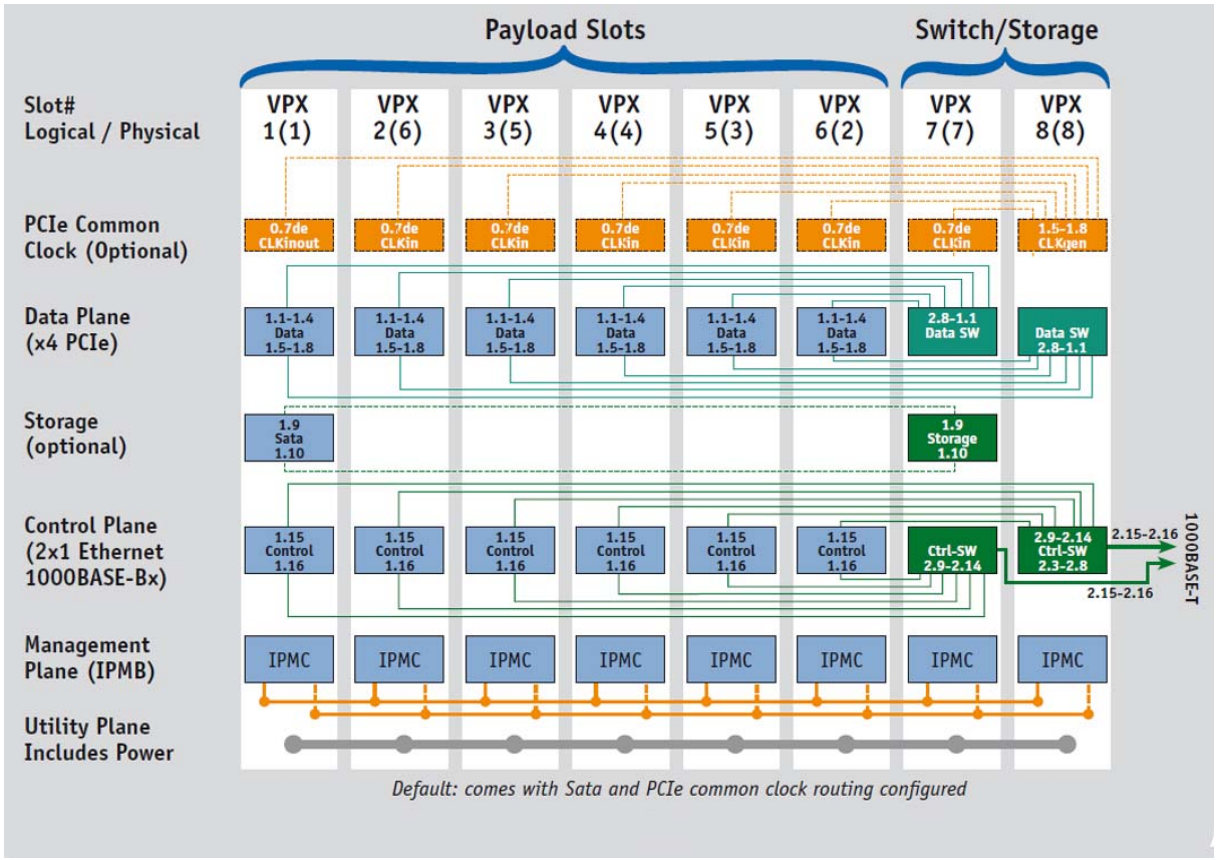


Figure 29: Dual Star x4 Topology

Chapter 7 - VX3035-RTM Characteristics

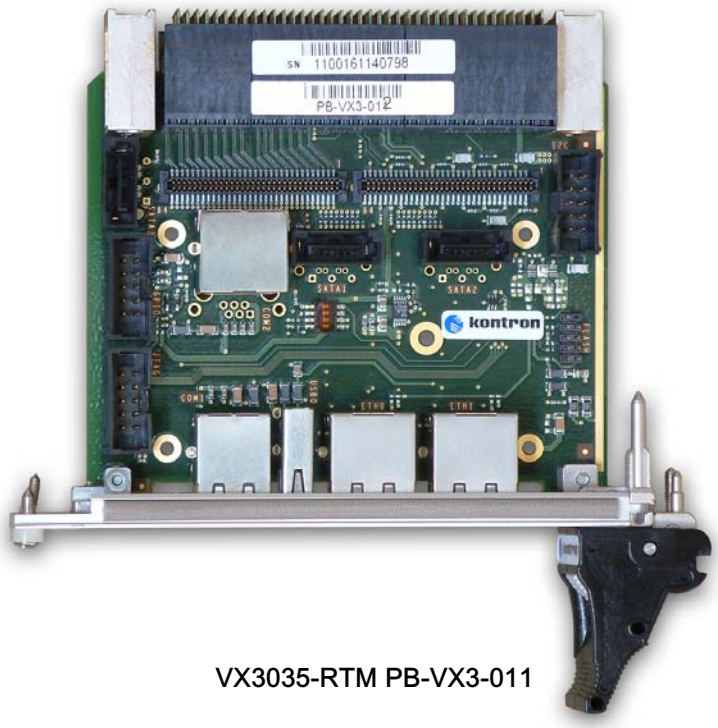
7.1 VX3035-RTM Overview

The VX3035 provides optional Rear I/O connectivity for peripherals, a feature which may be particularly useful in specialized VPX systems. Some standard PC interfaces are implemented and assigned to the front panel and to the Rear I/O connector J2 on the VX3035.

When the VX3035-RTM is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus, the VX3035 Rear Transition Module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

The VX3035-RTM provides the following functions:

- VPX Rear I/O
- Two USB 2.0 ports
- One Gigabit Ethernet ports without LED signals
- Two COM (Serial) ports
- Two SATA ports
- Two GPIOs
- One Reset Button
- One I2C Bus connector
- One JTAG connector



VX3035-RTM PB-VX3-011

Figure 30: VX3035-RTM Overview

7.2 VX3035-RTM Technical Specifications

VX3035-RTM		SPECIFICATIONS
Front Panel Interfaces	USB	One USB 2.0 interface: 4-pin connector
	Ethernet	One Gigabit Ethernet interface implemented as dual RJ-45 connector without LEDs
	COM	One serial port (COM1), RS-232 simplified, RJ-12 connector
	Reset	One Push Button
Onboard Interfaces	SATA	Two SATA interfaces; SATA1 and SATA2
	VPX	VPX connector for connecting Rear I/O to the backplane
	COM	One serial port (COM2) implemented as a RJ-12 onboard connector, RS-232 simplified
	GPIOs	Two General Purpose I/Os
	USB	One USB interface used to connect a Flash disk
	I2C Bus	
	JTAG	
General	Temperature Range	Operational: 0°C to +55°C Storage: -55°C to +85°C
	Climatic Humidity	99% non-condensing
	Dimensions	Dimensions: 99.85 mm x 82.54 mm
	Board Weight	120g

Table 30: VX3035-RTM Main Specifications

7.3 VX3035-RTM Configuration

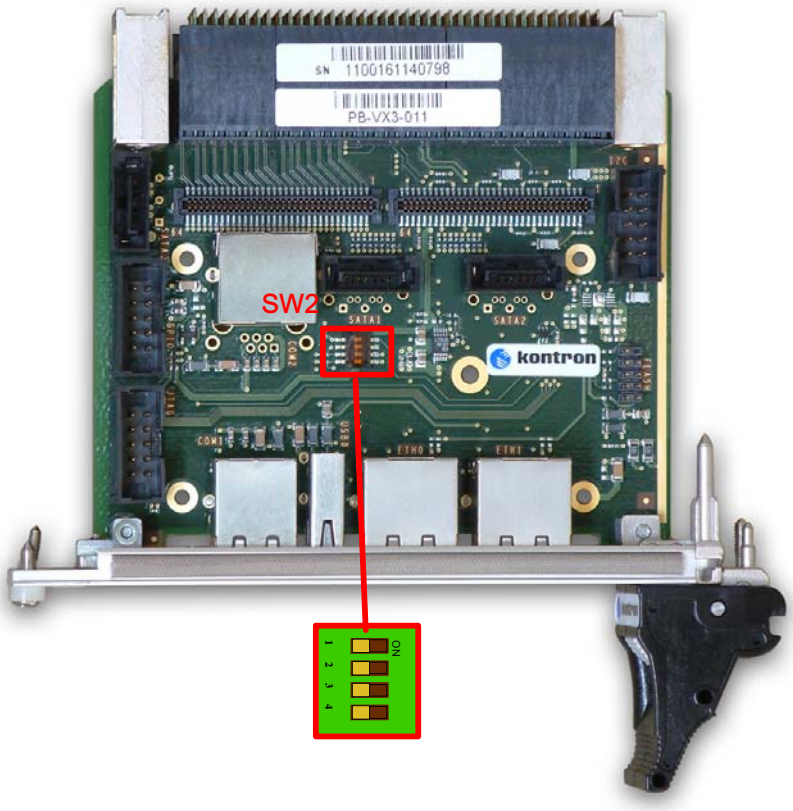


Figure 31: VX3035-RTM MicroSwitch Location

MicroSwitch SW2	Function	Description
1	NVMRO Non-Volatile Memory Read Only	ON (0) Set NVMRO VPX signal to Ground OFF (1) No action on NVMRO VPX signal **Default setting**
2	Reserved	Reserved
3	COM1 Differential Termination	ON (0) Connect a 100 Ohms parallel termination between RXD+ and RXD- OFF (1) No differential termination/mode **Default setting**
4	COM2 Differential Termination	ON (0) Connect a 100 Ohms parallel termination between RXD+ and RXD- OFF (1) No differential termination/ mode **Default setting**

7.4 VX3035-RTM Connectors

7.4.1 RTM Connectors Identification

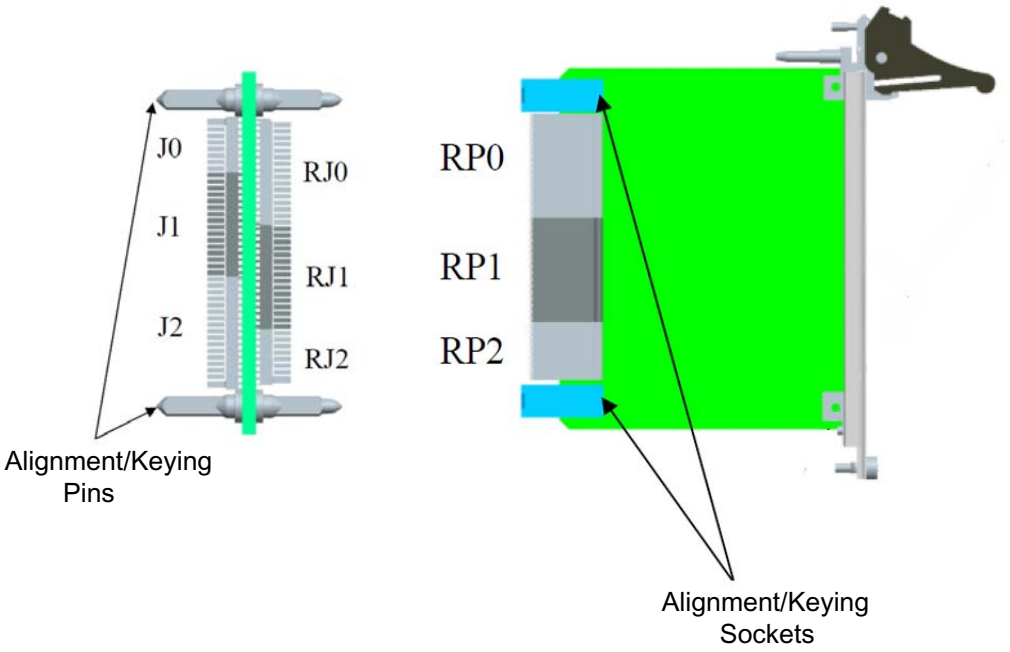


Figure 32: Connector Identification for 3U RTM

7.4.2 Front Panel Connectors

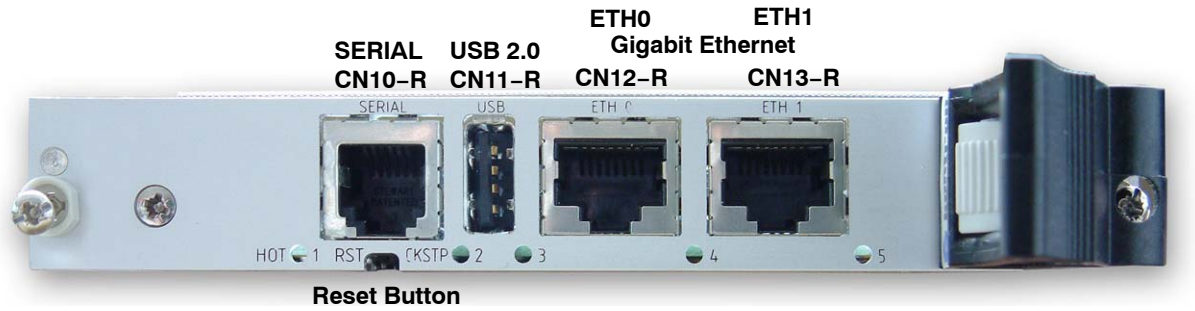


Figure 33: VX3035-RTM Front Panel Connectors

LED 1 to LED 5 are not connected.

ETH0 Gigabit Ethernet CN12-R is not used

7.4.3 Onboard Connectors

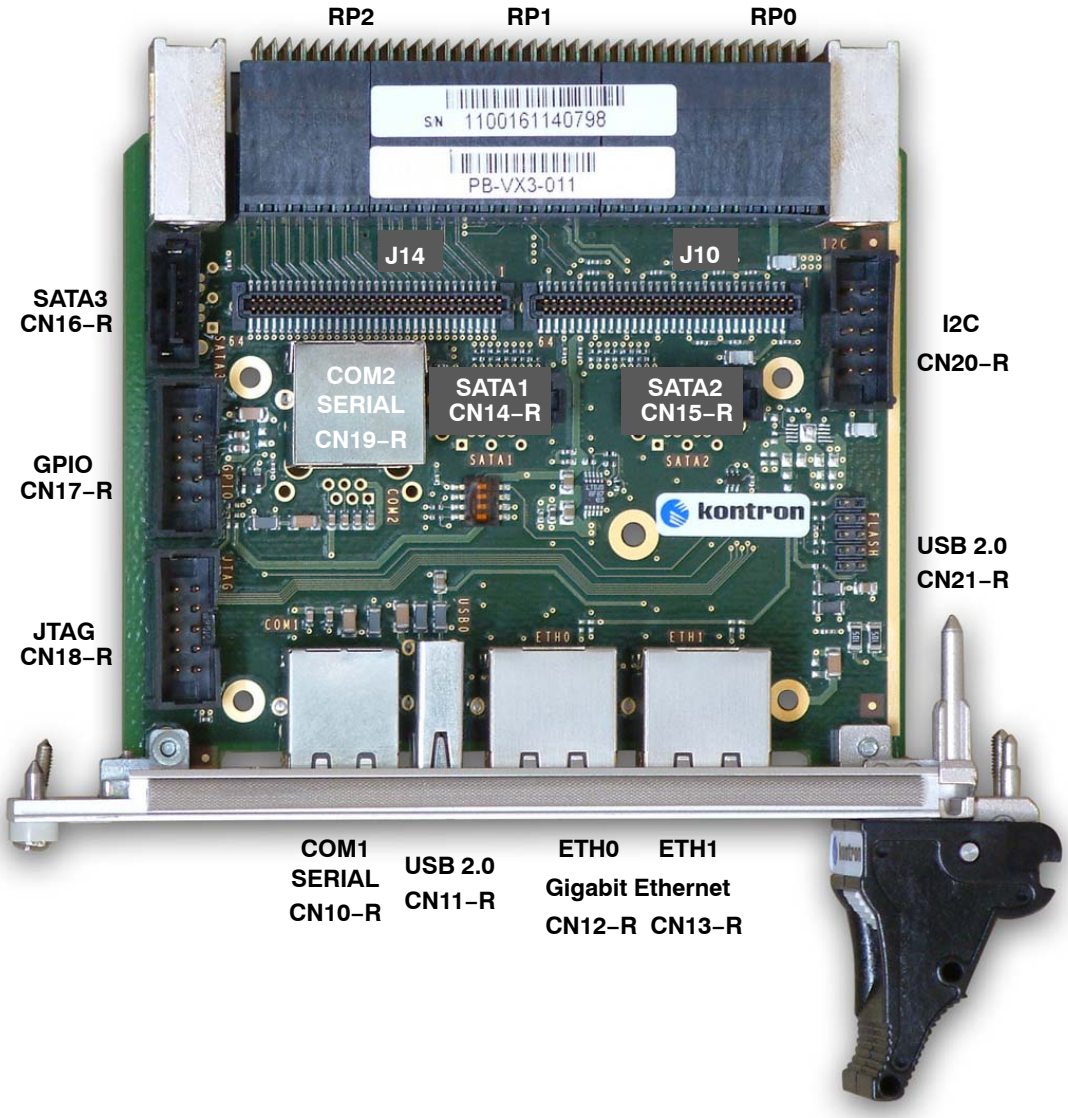


Figure 34: VX3035-RTM Onboard Connectors

SATA3 CN16-R is not used

7.5 VX3035-RTM Modules Interfaces

7.5.1 COM Interfaces

The VX3035-RTM provides two COM (COM1 and COM2) ports for connecting devices to the VX3035-RTM.

> COM1 serial port RJ-12 connector is located on the front panel of the RTM.

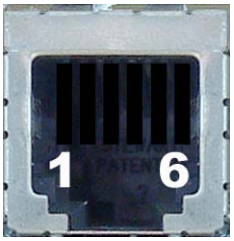
> COM2 serial port RJ-12 connector is located onboard.

» COM1 - EIA-232 Simplified

The following figure and table provide pinout information for the 6-pin RJ-12 COM1 connector CN10-R located on the front panel.

PIN	SIGNAL	FUNCTION
1	RTS/TXDb	EIA-232 Request To Send / EIA-485 Transmit Data (pair b)
2	Shell	Chassis Ground
3	TXD/TXDa	EIA-232 Transmit Data / EIA-485 Transmit Data (pair a)
4	RXD/RXDa	EIA-232Receive Data / EIA-485 Receive Data (pair a)
5	GND	Ground
6	CTS/RXDb	EIA-232 Clear-To-Send / EIA-485 Receive Data (pair b)

Table 31: Front Panel Serial Port Connector Pinout



CN10–R

Figure 35: Serial Port Connector

> Serial Cable Designation

Serial cable can be either RJ-14 or RJ-12:

- RJ-14 (6 pin, 4 conductor) for a simple EIA-232 without handshake support.
- RJ-12 (6 pin, 6 conductor) for EIA-232 with handshaking.

  A RJ-12 to DB9/DB25 male or DB9/DB25 female adapter is available from multiple sources, such as:

  - Kontron Order Code KIT-2X-RJ12DB9
  - Triangle Cable http://www.trianglecables.com/db9m-rj12.html

COM2 - EIA-232 Simplified

The following figure and table provide pinout information for the 6-pin RJ-12 COM2 connector CN19-R located onboard.

PIN	SIGNAL	FUNCTION
1	-	Not used
2	Shell	Chassis Ground
3	TXD/TXDa	EIA-232 Transmit Data / EIA-485 Transmit Data (pair a)
4	RXD/RXDa	EIA-232Receive Data / EIA-485 Receive Data (pair a)
5	GND	Ground
6	-	Not used

Table 32: Onboard Serial Port Connector Pinout

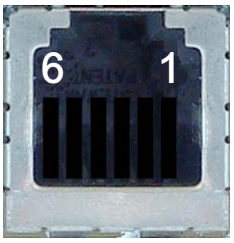


Figure 36: Serial Port Connector

7.5.2 USB Interfaces

There are two USB 2.0 ports available on the VX3035-RTM, each with a maximum transfer rate of 480 Mb/s provided for connecting USB devices.

- One interface is available on the VX3035-RTM front panel. One USB peripheral may be connected to this port. To connect more USB devices, an external hub is required.
- The second USB interface is onboard and used to connect a Flash disk.

USB Front Panel

The following figure and table provide pinout information for the CN11-R connector located on the front panel.

PIN	SIGNAL	FUNCTION	I/O
1	VCC	VCC	--
2	UV0-	Differential USB-	I/O
3	UV0+	Differential USB+	I/O
4	GND	GND	--

Table 33: Front Panel USB Connector Pinout

Figure 37: Front Panel USB Connector

The USB host interfaces on the VX3035-RTM can be used with maximum 500 mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short-circuit protection is provided. All the signal lines are EMI-filtered.

The Rear I/O interface supports the USB 1.1 and USB 2.0 standards. For USB 2.0 it is strongly recommended to use a cable length not exceeding 3 meters.

USB Onboard

The onboard USB device (CN21-R connector) is used to connect a USB flash disk module. The following figure and table provide pinout information for the onboard USB connector.

PIN	SIGNAL	FUNCTION	I/O
1	USB_PWR	VCC	--
2	N.C.	Not Connected	--
3	USB_D-	Differential USB-	I/O
4	N.C.	Not Connected	--
5	USB_D+	Differential USB+	I/O
6	N.C.	Not Connected	--
7	GND	GND	--
8	N.C.	Not Connected	--
9	N.C.	Not Connected	--
10	N.C.	Not Connected	--

Table 34: Onboard USB Connector Pinout

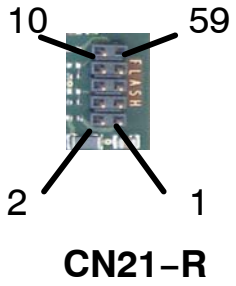


Figure 38: Onboard USB Connector

The USB Flash module is fixed to the board, by using on one side the CN21-R connector, and on the other side, a standoff screwed to the VX3035-RTM board and to the USB Flash module.

Figure 39: USB Flash Disk Overview

Order Code for the USB flash disk:

FDM-USB-*x*GB-2MM-IV: industrial version with conformal coating for use with rugged versions (*x* = up to 16 GB)

USB Flash Disk Layout:

- The maximum space reserved for the USB flash disk is 36.9 mm x 26.6 mm (LxW)
- The distance between the connector and the screw hole is 27.3 mm~27.9mm
- The maximum allowable connector height is 3.68 mm

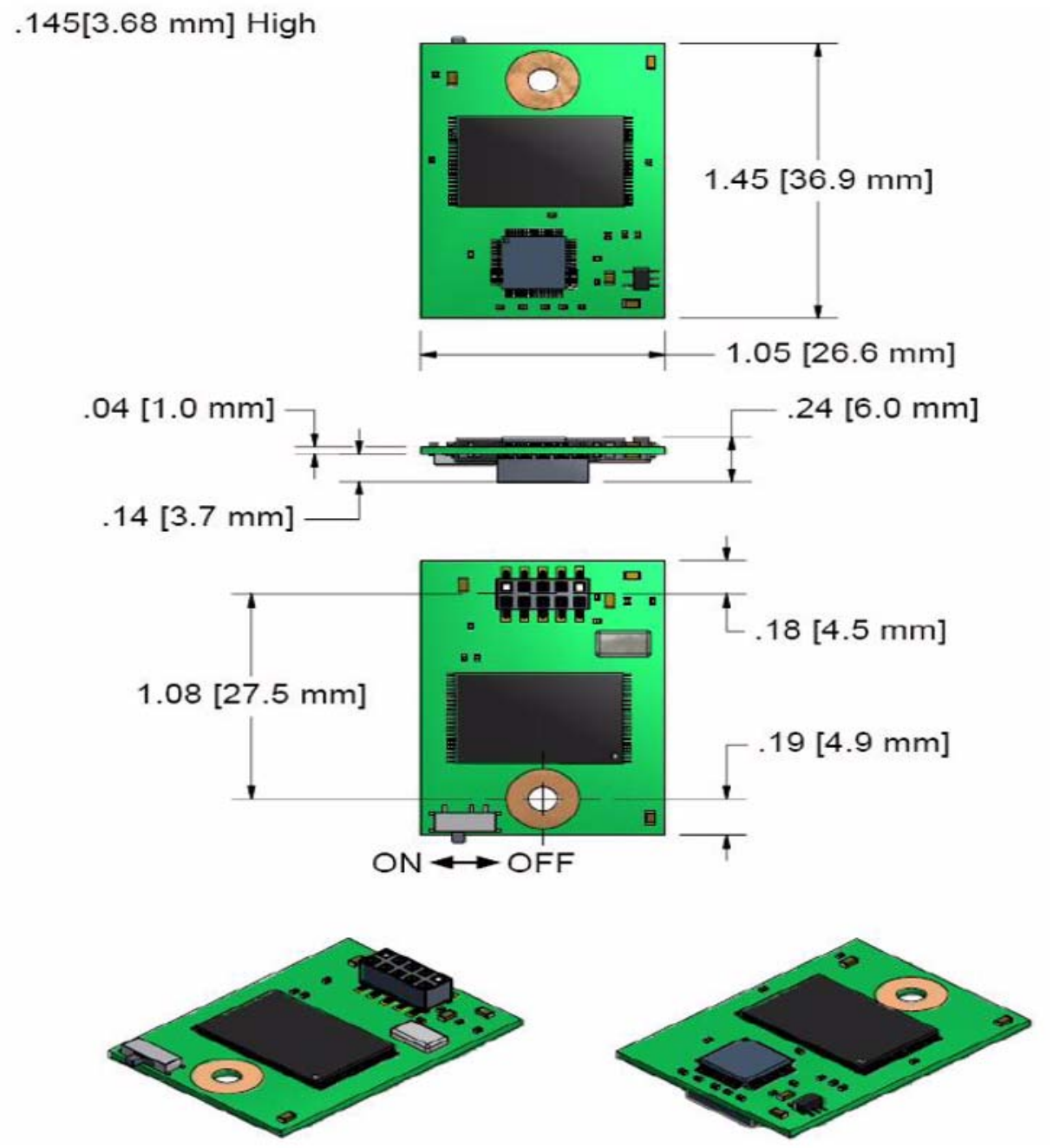


Figure 40: USB Flash Disk Layout

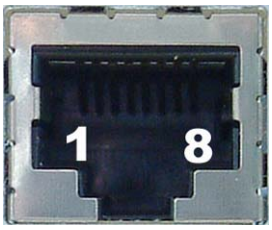
» Corresponding USB ports on VX3035 and RTM:

Connector or RTM	Signal on RP1	Port on VX3035 PCH
CN11-R	USB2*xx*	port10
CN21-R	USB3*xx*	port13

7.5.3 Gigabit Ethernet Interfaces

The Ethernet connector is a RJ-45 connector. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

CN13–R



ETH1

Figure 41: Gigabit Ethernet Connector

The RJ-45 ethernet port signal assigment is described below.

MDI/STANDARD ETHERNET CABLE						PIN	MDIX/CROSSED ETHERNET CABLE					
10BASE-T		100BASE-TX		1000BASE-T			10BASE-T		100BASE-TX		1000BASE-T	
I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL		I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
O	TX+	O	TX+	I/O	BI_DA+	1	I	RX+	I	RX+	I/O	BI_DB+
O	TX-	O	TX-	I/O	BI_DA-	2	I	RX-	I	RX-	I/O	BI_DB-
I	RX+	I	RX+	I/O	BI_DB+	3	O	TX+	O	TX+	I/O	BI_DA+
-	-	-	-	I/O	BI_DC+	4	-	-	-	-	I/O	BI_DD+
-	-	-	-	I/O	BI_DC-	5	-	-	-	-	I/O	BI_DD-
I	TX-	I	RX-	I/O	BI_DB-	6	O	TX-	O	TX-	I/O	BI_DA-
-	-	-	-	I/O	BI_DD+	7	-	-	-	-	I/O	BI_DC+
-	-	-	-	I/O	BI_DD-	8	-	-	-	-	I/O	BI_DC-

Table 35: Gigabit Ethernet Connector Pin Assignment

The Ethernet transmission can operate effectively using a CAT5 cable or higher specifications.

ETH0 Gigabit Ethernet CN12-R is not used.

7.5.4 Serial ATA Interfaces

The onboard Serial ATA connectors CN14-R and CN15-R allow the connection of standard HDDs and other Serial ATA devices to the VX3035 Rear Transition Module.

SATA connectors description

The following figure and table provide pinout information for the SATA connectors CN14-R and CN15-R.

PIN	SIGNAL	DESCRIPTION	I/O
1	GND	Ground signal	--
2	SATA_TX+	Differential Transmit +	O
3	SATA_TX-	Differential Transmit -	O
4	GND	Ground signal	--
5	SATA_RX-	Differential Receive -	I
6	SATA_RX+	Differential Receive +	I
7	GND	Groudn Signal	--

Table 36: Onboard SATA Connectors Pinout

Figure 42: Onboard SATA Connectors

When using a Serial ATA cable, it is recommended to use a special right-angled Serial ATA cable due to possible space limitations within the system. For further information, contact Kontron's Technical Support.

SATA3 CN16-R is not used.

Corresponding SATA ports on VX3035 and RTM

Connector	Signal on RP1	Port on VX3035 PCH
SATA1 RTM: CN14-R	SATA0	port 0
SATA2 RTM:CN15-R	SATA3	port 3

7.5.5 GPIO Connector

Routed from RP1 to CN17-R connector (right angle HE10 10-pin connector male).

PIN	SIGNAL	DESCRIPTION
1	Reserved	
2	Reserved	
3	GND	Ground
4	GND	Ground
5	Reserved	
6	Reserved	
7	GPIO1(*)	General Purpose IO
8	GND	Ground
9	GPIO2	General Purpose IO or Maskable Reset
10	GND	Ground

(*) Signals available when RTM is connected to VX3035 product

Table 37: Onboard GPIO Connector Pinout

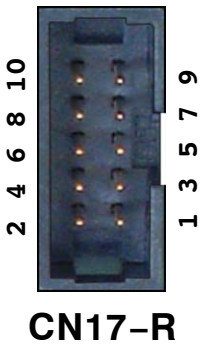


Figure 43: Onboard GPIO Connector

7.5.6 JTAG Connector

When connected to a VX3035, the JTAG connector CN18-R of the RTM card carries GPIOs routed from RP0. The CN18-R connector is a right angle HE10 10-pin male connector with the following pinout:

PIN	SIGNAL	DESCRIPTION
1	GPIO5 (*)	General Purpose IO
2	GND	Ground
3	Reserved	
4	3.3V sense	
5	GPIO3 (*)	General Purpose IO
6	N.C.	Not Connected
7	N.C.	Not Connected
8	GPIO4 (*)	General Purpose IO
9	Reserved	
10	GND	Ground

(*) Signals available when RTM is connected to VX3035 product

Table 38: Onboard JTAG Connector Pinout

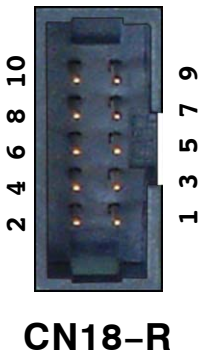


Figure 44: Onboard JTAG Connector

7.5.7 I2C System Management Connector

Routed from RP0 to CN20-R connector (right angle HE10 10-pin connector male).

PIN	SIGNAL	DESCRIPTION
1	SMB0 CLK	SM Bus 0 Serial Clock
2	SMB1 CLK	SM Bus 1 Seria Clock
3	GND	Ground
4	GND	Ground
5	SMB0 DAT	SM Bus 0 bi-directional Serial Data
6	SMB1 DAT	SM Bus 1 bi-directional Serial Data
7	+3V3_AUX	+3.3V auxiliary power supply
8	+3V3_AUX	+3.3V auxiliary power supply
9	N.C.	Not Connected
10	Reserved	

Table 39: Onboard I2C Connector Pinout

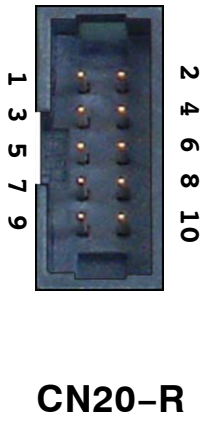
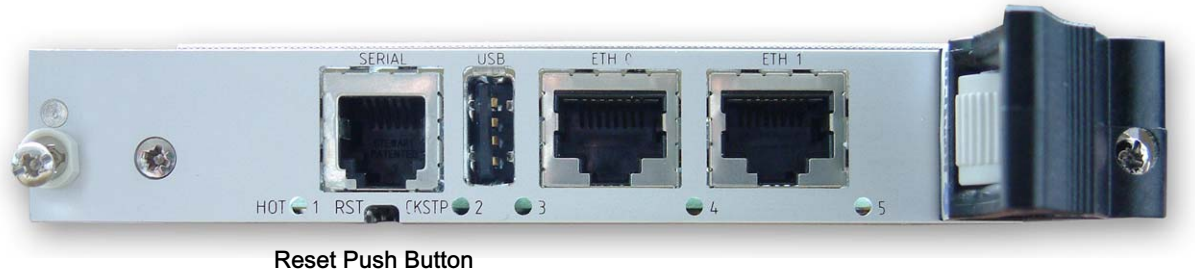


Figure 45: Onboard JTAG Connector

7.6 VX3035-RTM Reset



Reset Push Button

Figure 46: VX3035-RTM Reset Push Button

Reset and SW1 Reset Switch

The VX3035-RTM generates a system reset signal on the VPX bus at each +5V power-on for a duration of 140 ms to 560 ms.

In addition, the front panel reset push button of the VX3035-RTM is used to generate a VPX bus reset with the same minimum duration.

LEDs

The five LEDs are not connected, and unused.

7.7 VX3035-RTM Power Consideration

Only the 5V main power from the VPX is used. The 3.3V and 12V VPX power rails are not used in order to accomodate 3U VPX backplane.

Auxiliary VPX voltages 3.3V (I2C connector), +/- 12V (PIM J10 connector) are used.

The 3.3V power supply on the J10 connector is regulated from the 5V input through a 1.5A max linear regulator.

7.8 VX3035-RTM Rear I/O Interfaces

The VX3035 Rear Transition Module conducts a wide range of I/O signals through the Rear I/O connectors RP0, RP1 and RP2.

- RP0: one 15-wafer 7-row connector
- RP1: one 16-wafer 7-row connector
- RP2: one 8-wafer 7-row connector

To support the Rear I/O feature a special backplane is necessary. Do not plug a Rear I/O configured board in a non-system slot Rear I/O backplane. Failure to comply with the above may result in damage to your board.

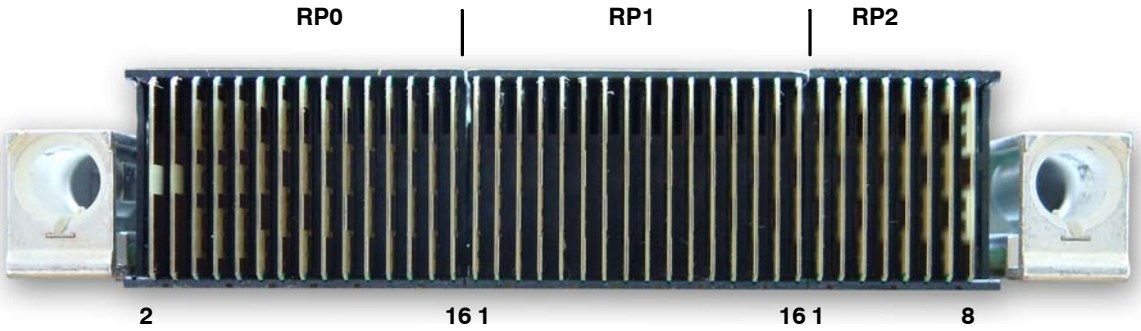


Figure 47: Rear I/O VPX Connectors

The VX3035-RTM provides the following interfaces:

- Two USB 2.0 ports (USB2 and USB3 via RP1 connector)
- One Gigabit Ethernet port without LED signals (ETH via RP1 connector)
- Two SATA ports (SATA0 and SATA3 via RP1 connector)
- Two EIA-232 COM ports (COM1 via RP1 connector, COM1 via RP2 connector)

7.8.1 RP2 Connector

> Legend for Table 40

COM1/2	Simplified Serial Lines
PCIe_CLK	Additionnal PCI express clock from PCH
PCIe_TX/RX	Additionnal PCI express x1 link from PCH
eDP-A/B	Digital ports A and B from PCH

RP2 Wafer Assignment

RPM Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A	Board Wafer
1	COM2 TXD+	GND	eDP-B 3-	eDP-B 3+	GND	eDP-B2-	eDP-B 2+	P2 w09
2	GND	PCIe CLK-	PCIe CLK+	GND	eDP-B AUX-	eDP-B AUX+	GND	P2 w10
3	COM2 TXD	GND	PCIe TX-	PCIe TX+	GND	PCIe RX-	PCIe RX+	P2 w11
4	GND	Reserved	Reserved	GND	Reserved	Reserved	GND	P2 w12
5	COM2 RXD+	GND	Reserved	Reserved	GND	Reserved	Reserved	P2 w13
6	GND	Reserved	Reserved	GND	Reserved	Reserved	GND	P2 w14
7	COM2 RXD	GND	Reserved	Reserved	GND	Reserved	Reserved	P2 w15
8	GND	Reserved	Reserved	GND	Reserved	Reserved	GND	P2 w16
CASE	GND							

Table 40: Rear I/O VPX Connector RP2 Wafer Assignment

RP2 Signal Definition

Mnemonic	Signal Definition
COMx	Serial Lines, EIA-232/EIA-485
eDPx	embedded Display Port
PCIe1 TX/RX	Additional PCI-Express x1 link
PCIe1 CLK	Common Reference Clock Output for PCIe1
Reserved	Reserved, do not connect
GND	Ground

Table 41: Rear I/O VPX Connector RP2 Signal Definition

7.8.2 RP1 Connector

RP1 Wafer Assignment

> Legend for Table 42

USB2/3	USB links 2 and 3 from PCH	SATA0/3	SATA links 0 and 3 from PCH
ETHx TX/RX	1000BASE-BX links 0 and 1 from Dual GbE i82580	ETH DA/DB/DC/DD	1000BASE-T link from GbE i82577
COM1/2	Simplified Serial Lines	eDP-A/B	Digital ports A and B from PCH
USB4/5	USB links from PCH	SATA1/2	SATA links from PCH

RPM Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A	Board Wafer
1	USB2 PWR	GND	SATA0 TX-	SATA0 TX+	GND	SATA0 RX-	SATA0 RX+	P1 w09
2	GND	SATA3 TX-	SATA3 TX+	GND	SATA3 RX-	SATA3 RX+	GND	P1 w10
3	USB3 PWR	GND	NC	NC	GND	NC	NC	P1 w11
4	GND	USB2 DA-	USB2 DA+	GND	USB3 DA-	USB3 DA+	GND	P1 w12
5	GPIO1	GND	ETH DB-	ETH DB+	GND	ETH DA-	ETH DA+	P1 w13
6	GND	ETH DD	ETH DD+	GND	ETH DC-	ETH DC+	GND	P1 w14
7	Maskable Reset* or GPIO2	GND	ETH1 TX-	ETH1 TX+	GND	ETH1 RX-	ETH1 RX+	P1 w15
8	GND	ETH0 TX-	ETH0 TX+	GND	ETH0 RX-	ETH0 RX+	GND	P1 w16
9	COM1_RTS or COM1 TXD+	GND	SATA1 TX-	SATA1 TX+	GND	SATA1 RX-	SATA1 RX+	P2 w01
10	GND	SATA2 TX-	SATA2 TX+	GND	SATA2 RX-	SATA2 RX+	GND	P2 w02
11	COM1 TXD	GND	USB4 PWR	USB4 PWR	GND	USB5 PWR	USB5 PWR	P2 w03
12	GND	USB4 DA-	USB4 DA+	GND	USB5 DA-	USB5 DA+	GND	P2 w04
13	COM1 CTS or COM1 RXD+	GND	eDP-A 1-	eDP-A 1+	GND	eDP-A 0-	eDP-A 0+	P2 w05
14	GND	eDP-A 3-	eDP-A 3+	GND	eDP-A 2-	eDP-A 2+	GND	P2 w06
15	COM1 RXD	GND	eDP-B HPD	eDP-A HPD	GND	eDP-A AUX-	eDP-A AUX+	P2 w07
16	GND	eDP-B 1-	eDP-B 1+	GND	eDP-B 0-	eDP-B 0+	GND	P2 w08
CASE	GND							

Table 42: Rear I/O VPX Connector RP1 Wafer Assignment

RP1 Signal Definition

Mnemonic	Signal Definition
SATAx RX+/-	Serial ATA. Receive +/- link x
SATAx TX+/-	Serial ATA. Transmit +/- link x
USBx PWR	USB Power link x
USBx D+/-	Differential Data pair of USB link x
ETH DA+/-	Ethernet 1000BASE-T: First pair of transmit/receive data.
ETH DB+/-	Ethernet 1000BASE-T: Second pair of transmit/receive data
ETH DC+/-	Ethernet 1000BASE-T: Third pair of transmit/receive data.
ETH DD+/-	Ethernet 1000BASE-T: Fourth pair of transmit/receive data
ETHx RX+/-	1000BASE-BX Ethernet x: Receive data +/-
ETHx TX+/-	1000BASE-BX Ethernet x: Transmit data +/-
GPIOx	General Purpose I/Ox (handled by the CPLD)
Maskable Reset*	Optional reset input for this module. May be left unconnected if not used.
COMx	Serial Lines, EIA-232/EIA-485
	Differential Data pair of USB link x
eDPx	embedded Display Port
Reserved	Reserved, do not connect
GND	Ground

Table 43: Rear I/O VPX Connector RP1 Signal Definition

7.8.3 RP0 Connector

RP0 Wafer Assignment

RPM Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A	Board Wafer
2	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	P0 w02
3	+5V	+5V	+5V	+5V	+5V	+5V	+5V	P0 w03
4	Reserved	Reserved	GND	-12V_AUX	GND	SYSRESET*	NVMRO	P0 w04
5	N.C.	N.C.	GND	3V3_AUX	GND	Reserved	Reserved	P0 w05
6	N.C.	N.C.	GND	N.C.	GND	N.C.	N.C.	P0 w06
7	TCK	GND	Reserved	Reserved	GND	Reserved	Reserved	P0 w07
8	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	P0 w08
9	Reserved	GND	N.C.	N.C.	GND	N.C.	N.C.	P1 w01
10	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	P1 w02
11	N.C.	GND	N.C.	N.C.	GND	N.C.	N.C.	P1 w03
12	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	P1 w04
13	N.C.	GND	N.C.	N.C.	GND	N.C.	N.C.	P1 w05
14	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	P1 w06
15	N.C.	GND	N.C.	N.C.	GND	N.C.	N.C.	P1 w07
16	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	P1 w08
CASE	GND							

* signal active when low

Table 44: Rear I/O VPX Connector RP0 Wafer Assignment

RP0 Signal Definition

Mnemonic	Signal Definition
+/-12V_AUX	Auxiliary Power Supplies
3V3_AUX	3.3V Auxiliary Power, System Management
+5V	+5V Power Input
GND	Ground
NVMRO	Non-Volatile Memory Read Only
N.C.	Not Connected
SYSRESET*	System Reset

Table 45: Rear I/O VPX Connector RP0 Signal Definition

7.9 PCI 64 PIM Connector

7.9.1 J14 Connector

» J14 Connector Pin Assignment

Pin	Signal	Pin	Signal
1	SATA1 TX-	33	eDP-B 3-
2	SATA1 RX-	34	eDP-B2-
3	SATA1 TX+	35	eDP-B 3+
4	SATA1 RX+	36	eDP-B 2+
5	SATA2 TX-	37	PCIe CLK-
6	SATA2 RX-	38	eDP-B AUX-
7	SATA2 TX+	39	PCIe CLK+
8	SATA2 RX+	40	eDP-B AUX+
9	USB4 PWR	41	PCIe TX-
10	USB5 PWR	42	PCIe RX-
11	USB4 PWR	43	PCIe TX+
12	USB5 PWR	44	PCIe RX+
13	USB4 DA-	45	Reserved
14	USB5 DA-	46	Reserved
15	USB4 DA+	47	Reserved
16	USB5 DA+	48	Reserved
17	eDP-A 1-	49	Reserved
18	eDP-A 0-	50	Reserved
19	eDP-A 1+	51	Reserved
20	eDP-A 0+	52	Reserved
21	eDP-A 3-	53	Reserved
22	eDP-A 2-	54	Reserved
23	eDP-A 3+	55	Reserved
24	eDP-A 2+	56	Reserved
25	eDP-B HPD	57	Reserved
26	eDP-A AUX-	58	Reserved
27	eDP-A HPD	59	Reserved
28	eDP-A AUX+	60	Reserved
29	eDP-B 1-	61	Reserved
30	eDP-B 0-	62	Reserved
31	eDP-B 1+	63	Reserved
32	eDP-B 0+	64	Reserved

Signal Description

Mnemonic	Description
eDPx	embedded Display Port
PCIe1 TX/RX	Additional PCI-Express x1 link
PCIe1 CLK	Common Reference Clock Output for PCIe1
SATAx RX+/-	Serial ATA. Receive +/- link x
SATAx TX+/-	Serial ATA. Transmit +/- link x
USBx PWR	USB Power link x
USBx D+/-	Differential Data pair of USB link x
Reserved	Reserved, do not connect

7.9.2 J10 Connector

J10 Connector Pin Assignment

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
01	N.C.	02	+12V_AUX	03	N.C.	04	N.C.
05	+5V	06	N.C.	07	N.C.	08	N.C.
09	N.C.	10	+3.3V	11	N.C.	12	N.C.
13	GND	14	N.C.	15	N.C.	16	N.C.
17	N.C.	18	GND	19	N.C.	20	N.C.
21	+5V	22	N.C.	23	N.C.	24	N.C.
25	N.C.	26	+3.3V	27	N.C.	28	N.C.
29	GND	30	N.C.	31	N.C.	32	N.C.
33	N.C.	34	GND	35	N.C.	36	N.C.
37	+5V	38	N.C.	39	N.C.	40	N.C.
41	N.C.	42	+3.3V	43	N.C.	44	N.C.
45	GND	46	N.C.	47	N.C.	48	N.C.
49	N.C.	50	GND	51	N.C.	52	N.C.
53	+5V	54	N.C.	55	N.C.	56	N.C.
57	N.C.	58	+3.3V	59	N.C.	60	N.C.
61	-12V_AUX	62	N.C.	63	N.C.	64	N.C.

Signal Description

Mnemonic	Description
+/-12V-AUX	Auxiliary Power Supplies
+3.3V	+3.3V Power Input
+5V	+5V Power Input
GND	Ground
N.C.	Not Connected

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