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» VX305x-SA «

3U VPX Computing Node
User's Guide

CA.DT.B25-0e - June 2015

Revision History

Publication Title:	VX305x-SA User's Guide	
Doc. ID:	CA.DT.B25-0e	
Rev.	Brief Description of Changes	Date of Issue
0e	Preliminary Version	06-2015

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This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Environmental protection is a high priority with Kontron.

Kontron follows the DEEE/WEEE directive.

You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- reduce waste arising from electrical and electronic equipment (EEE)
- make producers of EEE responsible for the environmental impact of their products, especially when they become waste
- encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- improve the environmental performance of all those involved during the lifecycle of EEE

Conventions

This guide uses several types of notice: Note, Caution, ESD.

Note: this notice calls attention to important features or instructions.


Caution: this notice alert you to system damage, loss of data, or risk of personal injury.


ESD: This banner indicates an Electrostatic Sensitive Device.

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix `0x' shows a hexadecimal number, following the `C' programming language convention.

The multipliers `k', `M' and `G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when `K', `M' and `G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

When describing transfer rates, `k' `M' and `G' mean $*10^3$, $*10^6$ and $*10^9$ *not $*2^{10}$ $*2^{20}$ and $*2^{30}$.*

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and CompactPCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Signal names ending with an asterisk (*) or a hash (#) denote active low signals; all other signals are active high.

Signal names follow the PICMG 2.0 R3.0 CompactPCI Specification and the PCI Local Bus 2.3 Specification.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions


Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.


Caution, Electric Shock!
Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction.

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Chapter 1 - Introduction

The Kontron VX305x-SA is a 3U VPX computing blade for data and signal processing application focusing on application domains such as Military & Aerospace, Transportation and Energy/Industry.

The Kontron VPX blade VX305x-SA is the ideal building block for intensive parallel computing workloads where a cluster of Kontron VX305x-SAs can be used in switched OpenVPX environments.

The VX305x-SA board comes with EFI BIOS and supports Linux. It is covered by Kontron's long term supply program, which guarantees customers multi-year supply of the product beyond its active life.

Featuring the Intel® Xeon® D processor family (formerly Broadwell- DE), the VX305x-SA is the first 8-core multiprocessing board of the Kontron 3U VPX ecosystem. The highly integrated 8-core architecture with Dual 10 Gigabit Ethernet, high bandwidth PCI Express 3.0, high speed DDR4 memory, and versatile mezzanine options, is consequently SWaP-C optimized and simply the best choice for high performance embedded computing platforms.

VX305x-SA provides two 10GBASE-KR ports and 8 lanes Gen3 PCI Express to the backplane. Kontron VxFabric™ technology provides a TCP/IP protocol over the PCI Express infrastructure towards the application. A 10 Gigabit Ethernet switch and a PCI Express Switch can be complemented with two single star data planes, for 10 GETH and for PCI Express, respectively. A unique API with TCP/IP sockets makes it a powerful, leading edge Multi-CPU computing node architecture.

The M.2 top/bottom slots can be used for storage or for integration of customized personality modules. A 2-D graphic module is available, based on the Silicon Motion SM750 graphic controller.

Front-I/O module options are selectable for DVI/HDMI or Ethernet or other interfaces.

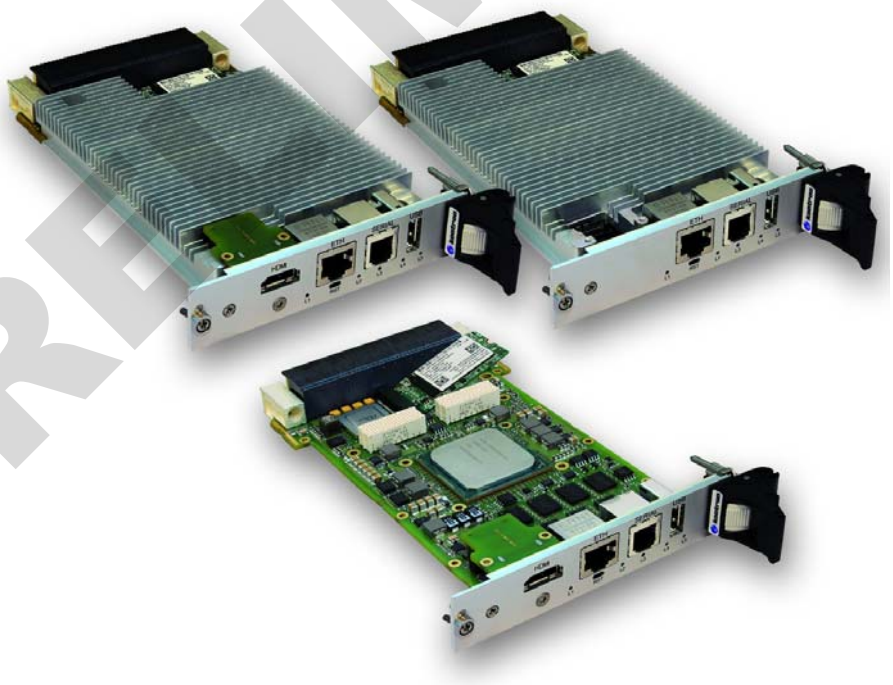


Figure 1: VX305x-SA-SA 3U VPX Overview

1.1 Manual Overview

1.1.1 Objective

This guide provides general information, hardware instructions, operating instructions and functional description of the VX305x-SA board. The onboard programming, onboard firmware and other software (e.g. drivers and BSPs) are described in detail in separate guides (see section 1.7 "Related Publications").

This hardware technical documentation reflects the most recent version of the product. The "Hardware release Notes" (see section 1.7 "Related Publications") might help to keep track of potential evolutions.

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

1.1.2 Audience

This guide is written to cover, as far as possible the range of people who will handle or use the VX305x-SA, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, system, cabling, grounding and communications.

1.1.3 Scope

This guide describes all variants of the VX305x-SA series.

1.1.4 Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- Chapter 1 - Introduction (this chapter)
- Chapter 2 - Installation
- Chapter 3 - Additional Board Features
- Chapter 4 - Physical I/O
- Chapter 5 - Power and Thermal Specifications
- Chapter 6 - Backplane Suggestions

1.1.5 Terminology, Definitions and Abbreviations

In this document, the term:

- VX305x-SA will be associated to the 3U VPX board family, including VX3052 dual core and VX3058 octo core module.

1.2 VPX Overview

VPX (VITA 46) specifications establish a new direction for the next revolution in bus boards. VPX is an ANSI standard which breaks out from the traditional connector scheme of VMEbus to merge the latest in connector and packaging technology with the latest in bus and serial fabric technology. VPX combines best-in-class technologies to assure a very long technology cycle similar to that of the original VMEbus solutions. Traditional parallel VMEbus will continue to be supported by VPX through bridging schemes that assure a solid migration pathway.

For further information regarding this standards and its use, visit the home page of the VITA - Open Standards, Open Markets (http://www.vita.com)

1.3 Board Overview

1.3.1 Main Features

» Intel® Xeon® Architecture

The VX305x-SA computing node is a VPX computing blade for parallel data and signal processing application. The VX305x-SA is the ideal building block for intensive parallel computing workloads where a cluster of VX305x-SAs is used in full mesh or switched OpenVPX environments. Target applications include radar, sonar, imaging systems, airborne fighters, and unmanned aerial vehicle (UAV) radar, as well as rugged multi-display consoles. It is also well suited for transport applications.

The processing node of the VX305x-SA implements a Xeon® Processor D coupled with single or dual channel DDR4 memory. The highly integrated Intel® QM77 platform hub provides numerous Ethernet, SATA, USB and PCIe channels. The 3U-format VX305x-SA is available in standard air-cooled version.

Frequency of the CPU:

- 45W 8 cores: TBD GHz
- 35W 8 cores: TBD GHz

However, the processor Xeon® Processor D is equipped with the Turbo Boost technology, which allows increasing the frequency when the total on chip power allows it.

Technical Specifications	
Processor	Fifth Generation Intel® Xeon® D Octo Core™, 35W, 1.6 GHz (8 execution cores, 16 threads, 12 MB) DDR4 dual channel memory with ECC, 2133 MT/s over 144 bits, up to 16 Gbytes Integrated dual 10G Ethernet controller PCIe gen3 x8 ports to VPX and XMC(*), up to 8 GT/s
Integrated Platform Controller Hub	PCI Express* Base Specification, Revision 2.0 support for up to eight ports with transfers up to 5 GT/s Integrated Serial ATA host controllers with independent DMA operation on up to six ports xHCI USB controller provides support for up to 8 USB ports, of which four can be configured as SuperSpeed USB 3.0 ports Two Integrated serial lines
Onboard Controller	
Gigabit Ethernet	One I210 Ethernet controller connected on front panel or VPX backplane (user selection) for 1000BASE-T operation 2nd I210 Ethernet controller connected on VPX backplane for 1000BASE-T operation, and optionally to the front panel (user selection) if the I/O profile option for “2nd RJ-45 Ethernet 1000BASE-T to the front option” is selected.
Watchdog	PLD-based, timeout ranging from 2 µs to 510s, IRQ, Reset, dual-stage One CPLD Board controller for power sequencing, reset handling, monitoring, failure detection, VPX I2C communication. Provides configuration/status registers on LPC interface
RTC	Separated low power RTC with optional onboard battery
System cPLD	Power - on/ off control, Reset control, Local environmental control/monitoring, I2C interfaces to I2C bus IPMB A/B (rear P0), LEDs control, Serial lines multiplexer, Serial VPD and user memories, User and system GPIOs, Internal registers that allow system management
Memory	
System Memory	Up to 16 GB dual channel DDR4 SDRAM running at 2133 MT/s, with ECC, soldered
Flash (uEFI BIOS)	2x16 MB FLASH, with recovery image and uEFI BIOS settings

(*) XMC slot option is on demand only

Technical Specifications	
EEPROM	One serial 256 Kbit EEPROM dedicated to system data One serial 256 Kbit EEPROM dedicated to application data
M.2 SSD option	M.2 SSD module option: Type M, 22 mm x 42 mm
Front Interfaces 5HP (1")	
USB	1x USB 2.0 port
Gigabit Ethernet	1x RJ-45 connector: 10/100/1000BASE-T Ethernet Note: This port is configurable from the BIOS to be routed to the VPX rear connector instead
HDMI (option)	HDMI connector as option. This includes a HDMI front-I/O module and a M.2 mezzanine for 2D graphics. Remark: HDMI front I/O and XMC(*) support are exclusive.
Serial	1x RJ-11 connector: Two EIA-232 interfaces or one EIA-485 interface from CPU, without hardware flow control
LEDs	5 LEDs reporting the board CPU health status and activity
Reset	Reset push button
Onboard Interfaces	
CPU Debug Interface	Bottom Debug connector for Port80, Spare x1 PCIe link with clock
M.2 module interface	Top M.2 slot for a 2D graphic module or a SSD module, compatible with a 12mm stacking height XMC(*) slot. M.2 type M standard ping mapping for SSD module or 2D graphic module option Bottom M.2 slot for SSD module. Supported module: Type M, 22 mm x 42 mm.
XMC(*) Slot option	One x8 PCIe 2 provision for XMC(*) slot option. X8d+X4s VITA 46.9 XMC(*) I/O routing, 8 differential pairs plus 4 single ended pins For XMC(*) slot option, please contact us because of thermal aspects.
VPX Interface	
Slot Profiles	SLT3-PAY-2F2U-14.2.3 SLT3-PAY-1F1F2U-14.2.4 SLT3-PAY-1F1U-14.2.10
Rear I/O via P0/P1/P2	x8 PCIe 3.0, non transparent capability, on P1. Configurable as 1 x8, 2 x4, or 4 x2. 2 SATA 6 Gb/s links on P1, 2 additional SATA 6 Gb/s links on P2 2 USB 2.0 and 1 USB 3.0 port on P1, 1 additional USB 2.0 link on P2 2 serial lines (Rx, Tx only) on P2, for RS-232 or RS-422/485 by using dynamic configuration 2 10GBASE-KR, or SFP+/SFI, or 1000BASE-KX on P1 1 1000BASE-T on P1, 2nd 1000BASE-T on P2 (both front/rear switchable, onboard magnetics) GPIOs on P1: GPIO1, GPIO2/Maskable reset, OpenVPX GDISCRETE1, VBAT, SYSCON. 2x multiplexed GPIO3/4 or SFI I2C on P0 DVI port on P2 as option. This includes a M.2 mezzanine for 2D graphics.
Supervisory Functions	Non Maskable RESET NVMRO, Master SMBus and Master/Slave SMBus interfaces for system management. Compatible with Kontron CMB (Monitoring Board), temperature and voltage sensors on the board PCIe optional use of common reference clock feature
Power Supplies	On P0: VS1=12V; VS2 not used; VS3=5V not used; 3.3V_AUX optional, -12V_AUX for XMC(*) slot option
OS Support	Linux Fedora 21, ask for: Windows, VxWorks

(*) XMC slot option is on demand only

All the Flash and non volatile memories onboard have a write protect mechanism taking into account the NVMRO (Non Volatile Memory read Only) VPX signal.

Software

Kontron is one of the few compact PCI, VME and VPX vendors providing in-house support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software editors, Kontron is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

Finally, Kontron offers to its customers owners of a maintenance agreement a hotline software support and regular software updates. A dedicated web site is also available for online updates and release downloads.

The VX305x-SA is delivered with the UEFI BIOS from AMI.

The VX305x-SA supports Linux Fedora distribution.

Please contact Kontron for further information regarding other operating systems and software support.

Rear Transition Module

The VX305x-SA supports the PB-VX3-400, a 3U VPX Rear Transition Module compliant with the definition of the Rear Transition Module on VPX standard - VITA 46.10.

It offers connectivity on the rear for:

- 4 HP Version
  - one Ethernet SFP+ cage operating at 1 or 10 Gbits/s.
  - one Ethernet 1000BASE-T port
  - two SATA III ports
  - two serial COM ports
  - one USB3 / USB2 port
  - two GPIOs
- 8 HP Version additionnal I/O:
  - 1 additionnal USB 2
  - 2 additional Sata II

1.3.2 Block Diagram

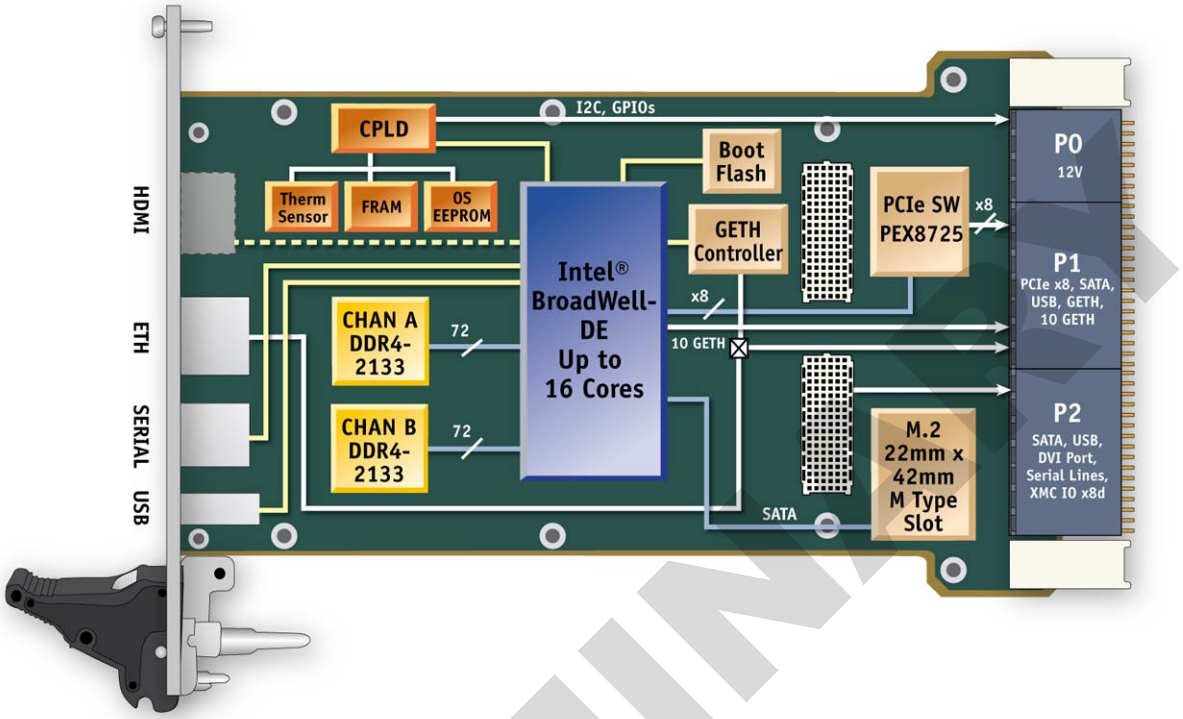


Figure 2: VX305x-SA Block Diagram

1.3.3 Ordering Information

Manufacturing Options

- CPU Frequency: . . . . . .
- Processor TDP . . . . . 35W and 45W
- DDR4 SDRAM Size: . . . . . 8 GB
  . . . . . 16 GB
- BOTTOM 22 mmx42 mm M.2 SATA slots: support 2242-S1-M, 2242-S2-M, 2242-S3-M, 2242-D1-M, 2242-D2-M, 2242-D3-M, 2242-D4-M, SATA link up to 6 Gb/s.
- TOP 22 mm x 42 mm M.2 slot: . . 2242-D4-M module with SM750 16MB graphic controller (MODP-GM2-SM750 module code or idem bottom M.2)
  Support also same storage modules as define above for the bottom slot.
- Trusted Platform Module . . . . . on demand
- Supercap . . . . . on demand
- Ruggedization Levels: . . . . . Standard Air-Cooled (SA)
- Front Panel . . . . . 1.0"
- XMC Slot (VITA 61/XMC 2.0 12mm) XMC slot option is a nonstandard option because of thermal impacts and product restrictions with XMC slot - On demand only

Available Order Codes

Order Code		Description
VX3058	VX3058SA881150000	3U single slot 5 HP (1.0") VPX CPU Blade with 8-core Intel® Xeon® D processor, TBD GHz, 35W, 8 GB dualbank DDR4, Base Front-I/O, fully switched x8 PCIe 3, Air cooled 0°C to +55°C, no XMC slot option
VX3058	VX3058SA881151000	3U single slot 5 HP (1.0") VPX CPU Blade with 8-core Intel® Xeon® D processor, TBD GHz, 35W, 8 GB dualbank DDR4, additional graphics HDMI front /rear, fully switched x8 PCIe 3, Air cooled 0°C to +55°C, no XMC slot option
VX3052	VX3052SA880150000	3U single slot 5 HP (1.0") VPX CPU Blade with 2-core Intel® Xeon® D processor, TBD GHz, 35W, 8 GB dualbank DDR4, Base Front-I/O, fully switched x8 PCIe 3, Air cooled 0°C to +55°C, no XMC slot option
VX3052	VX3052SA880151000	3U single slot 5 HP (1.0") VPX CPU Blade with 2-core Intel® Xeon® D processor, TBD GHz, 35W, 8 GB dualbank DDR4, additional graphics HDMI front /rear, fully switched x8 PCIe 3,Air cooled 0°C to +55°C, no XMC slot option
RTM	PB-VX3-400	3U VPX Rear Transition Module (without PIM module) 4 TE or 5 TE
RTM	PB-VX3-410	3U VPX Rear Transition Module (with PIM module) 8 TE
Serial Cable	KIT-2X-RJ12DB9	Serial cable adapter

Table 1: VX305x-SA Order Codes

1.3.4 I/O Interfaces

Front Interfaces (Models without XMC)

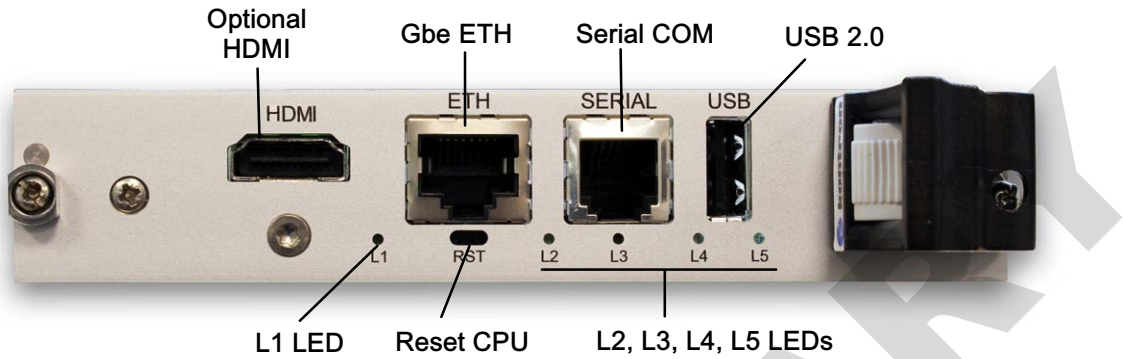


Figure 3: VX305x-SA Front Panel I/O Interfaces

Function	Description	See also
Serial Ports	COM: 2x EIA-232 or 1x EIA-485 UART interface for CPU on RJ-12 connector.	Section 4.1.1 for Pin Assignment
Gigabit Ethernet	1000BASE-T on RJ-45 connectors: **Note**: this port is configurable from the BIOS to be routed to the VPX P1 connector instead of the front connector ETH	Section 4.1.2 for Pin Assignment
USB 2.0	USB 2.0 interface	Section 4.1.3 for Pin Assignment
Graphics	HDMI (DVI) option	Section 4.1.4 for Pin Assignment
Reset	Reset push button	Figure 3
LEDs	5 LEDs reporting the board CPU health status and activity	Section 4.4 for LEDs Description

Table 2: Front I/O Interfaces

Rear Interfaces

Compliant with:

- VITA 46.0 (Standard VPX)
- VITA 46.4 (PCI Express on VPX)
- VITA 65 (OpenVPX System specification)

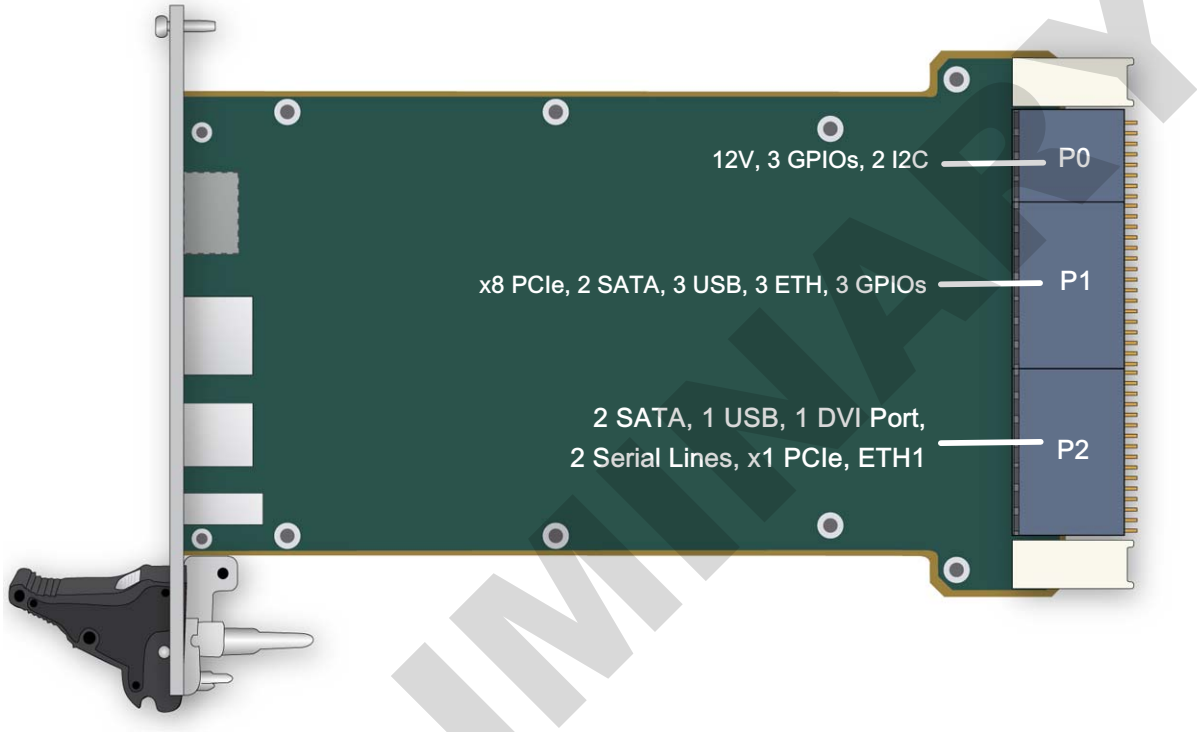


Figure 4: VX305x-SA Rear I/O Distribution

Function	Description	See also
PCI Express	> 1 x8 gen3 PCIe, non transparent capability, on P1. Optional use of PCIe common reference clock feature. > 1 x1 additional PCIe interface, gen2, on P2	Section 4.3 for VPX Connectors Description
SATA Storage	> 2 SATA 3 links on P1 > 2 additional SATA 2 links on P2	
USB	> 2 USB 2.0 and 1 USB 3.0 links on P1 > 1 additional USB 2.0 links on P2	
Gigabit Ethernet	> 2 SerDes 10GBASE-KR or 1000BASE-BX on P1 > 1 1000BASE-T on P1 > 2nd 1000BASE-T on P2	
Serial	> 2 asynchronous EIA-232/EIA-485 RX/TX serial line, on P2	
GPIOs	> 3 User GPIOs on P1, including OpenVPX GDISCRETE1, and MASKABLE RESET > 3 additional GPIOs on P0, replacing unused JTAG pins	Section 4.3 for VPX Connectors Description
Additional graphics HDMI front/rear	Front HDMI/DVI port and one rear DVI port on P2	Section 4.3 for VPX Connectors Description
Utilities	On P0 and P1: SYSRESET, SYSCON, 6 Geographical Addresses	Section 4.3 for VPX Connectors Description
Clocks	On P0: 25 MHz Refclock, 1 PPS Auxclock, optional PCIe 100 MHz clock input	
Power Supplies	VS1=12V; VS2 not used; VS3=5V not used; +12V_AUX is optional in VITA 46 and not connected on VX305x-SA. -12V_AUX is optional in VITA 46. It is not used internally on VX305x-SA except for the XMC (2) 3.3V_AUX is mandatory in VITA 46. However, if absent, it will be generated internally.	

Table 3: Rear I/O Interfaces

(1) Please refer to chapter 3.1 “The Backplane Power Supplies and their Monitoring” page 28 for tolerance and monitoring.

(2) XMC slot option is on demand only - If an XMC mezzanine is to be used on VX305x-SA and needs -12V, -12V_AUX must be provided on backplane.

1.3.5 Components Layout

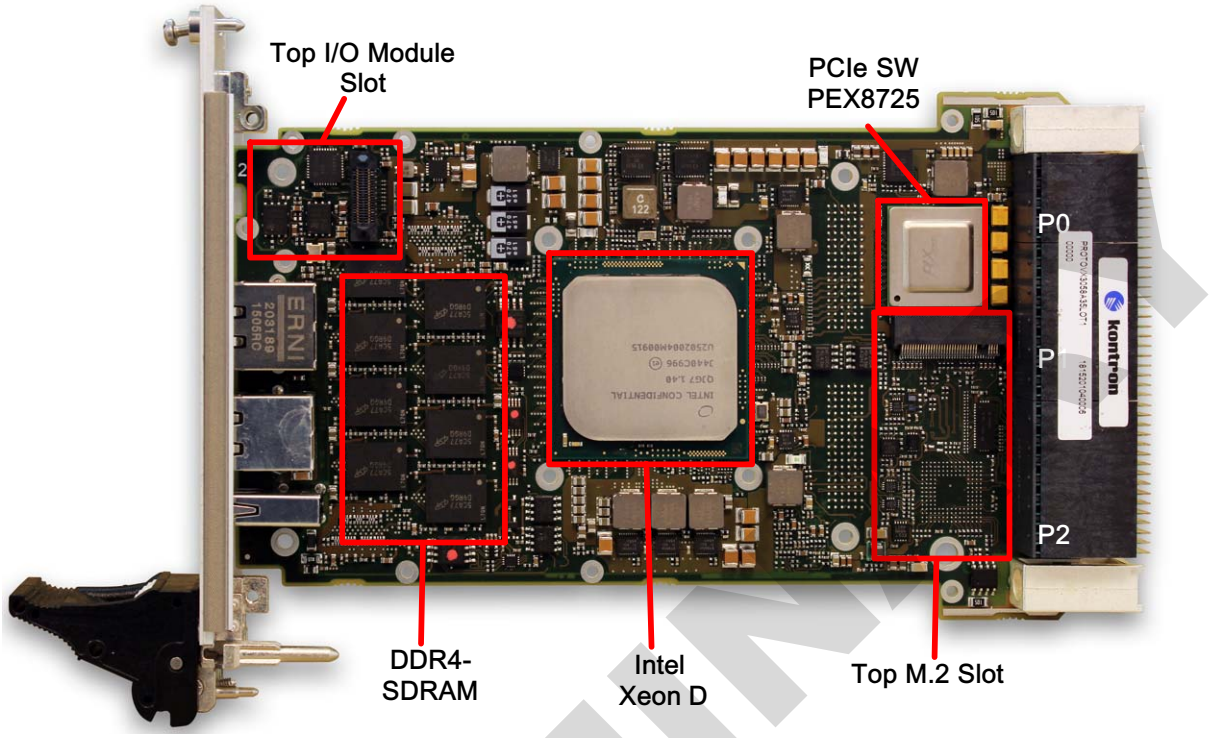


Figure 5: VX305x-SA Components Layout (Top view)

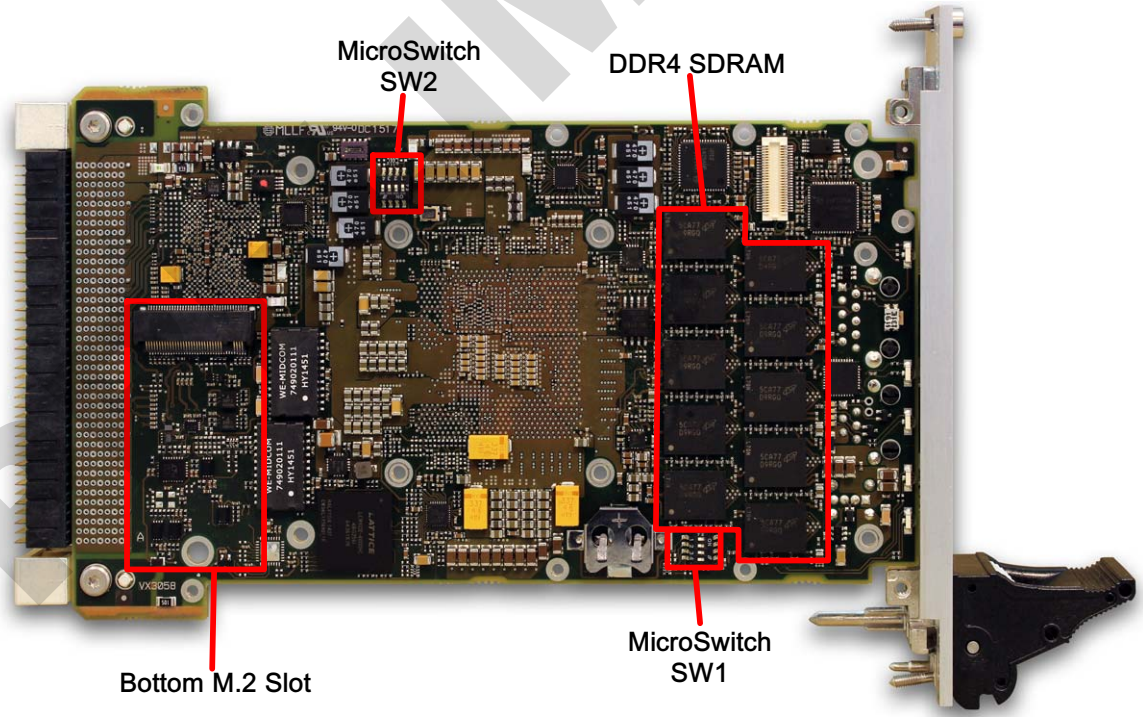


Figure 6: VX305x-SA Components Layout (Bottom view)

1.3.6 Technical Specification

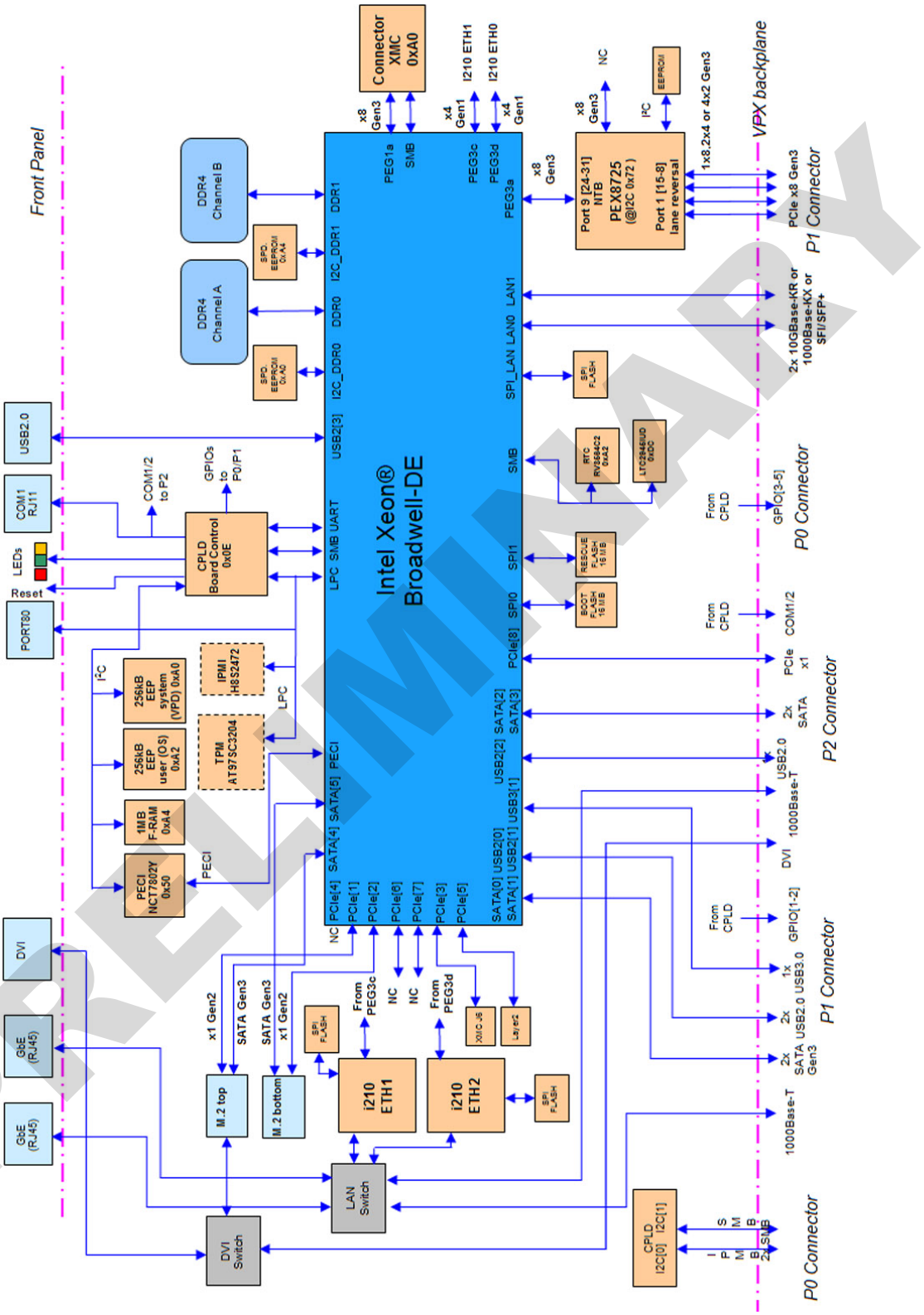


Figure 7: VX305x-SA Functional Block Diagram

1.4 Environmental Specifications

ENVIRONMENTAL SPECIFICATIONS	
	SA - Standard Commercial (1" single height passive module heat sink, forced air) No XMC slot option
Conformal Coating	Optional
Airflow	TBD
Cooling Method	Convection
Operating	0°C to +55°C
Storage	-45°C to +85°C
Vibration Sine (Operating)	2g / 20-500 Hz acceleration / frequency range
Random (Operating)	VITA 47-Class V1
Shock (Operating)	20g / 11 ms peak accel. / shock duration half sine
Altitude (Operating)	-1,500 to 60,000 ft
Relative Humidity	90% non-condensing

Table 4: Environmental Specifications

1.5 Technical Specifications

Board Weight	
SA - Standard Commercial	
VX3058-SA without optional modules	≈ 400g

Table 5: Technical Specifications

1.6 MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

MTBF	MILHDBK217F						IEC62380
	GB (Hours)		NS (Hours)		ARW (Hours)	AIC (Hours)	Typical Railway Mission Profile
	25°C	40°C	25°C	40°C	55°C	40°C	
VX3058-SA	TBD	TBD	TBD	TBD	TBD	TBD	TBD
VX3052-SA	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Table 6: VX305x-SA-SA MTBF Data

1.7 Related Publications

The following publications contain information relating to this product:

PRODUCT	PUBLICATION	
Standard		
ANSI/VITA 46.0	VPX Baseline Standard - ANSI/VITA 46.0-2007	
ANIS/VITA 46.4	PCI Express® on VPX Fabric Connector - VITA Draft Standard for Trial Use	
ANSI/VITA 46.6	Gigabit Ethernet Control Plane on VPX - VITA Draft Standard	
ANSI/VITA 46.7	Ethernet on VPX Fabric Connector VITA Draft Standard	
ANSI/VITA 46.9	XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules- VITA	
ANSI/VITA 46.10	Rear Transition Module for VPX - ANSI/VITA 46.10-2009	
ANSI/VITA 65	OpenVPX™ System Specification ANSI/VITA 65-2010	
Serial ATA	Serial ATA 1.0a Specification	
Hardware		
VX305x-SA Boards	VX305x-SA Hardware Release Notes	CA.DT.Bxx
Firmware		
VX305x-SA Boards	AMI-BIOS User Reference Manual	SD.DT.Gxx
VX305x-SA Boards	PBIT User's Guide	SD.DT.Gxx
Software		
VX305x-SA Boards	Release Note Fedora on VX305x-SA	SD.DT.Gxx
Systems		
VX305x-SA Boards	EZ3-VX305x-SA- Getting Started EZ3-VX305x-SA Quick Start	SD.DT.Gxx SD.DT.Gxx

Table 7: Related Publications

Chapter 2 - Installation

The VX305x-SA has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

2.1 Safety Requirements

The following safety precautions must be observed when installing or operating the VX305x-SA. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Special care shall be taken while handling the board: the heat sink can get very hot during operation. Do not touch the heat sink when installing or removing the board.
In addition, the board should not be placed on any surface or in any form of storage container before the board and heat sink have cooled down to room temperature.

This board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:
Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector pins or traces.
- We strongly recommend our customers to work in an environment equipped with anti-static workbenches with professional discharging equipments.

2.2 Board Identification

The VX305x-SA boards are identified by labels fitted to the top side of the board.

The E.C. Level format is "xxxxxLy" where

- The five digits "xxxxx" indicate the board E.C. Level (PCB revision included)
- "Ly" indicates the mechanical E.C. Level:
  - letter "L" varies with the environment class ("A" for SA, "B" for WA, "C" for RA and "D" for RC)
  - digit "y" gives the mechanical E.C. Level.

Top Side

A "Identification" label: Order Code, Serial Number, Variant, E.C. Level

Ethernet MAC addresses

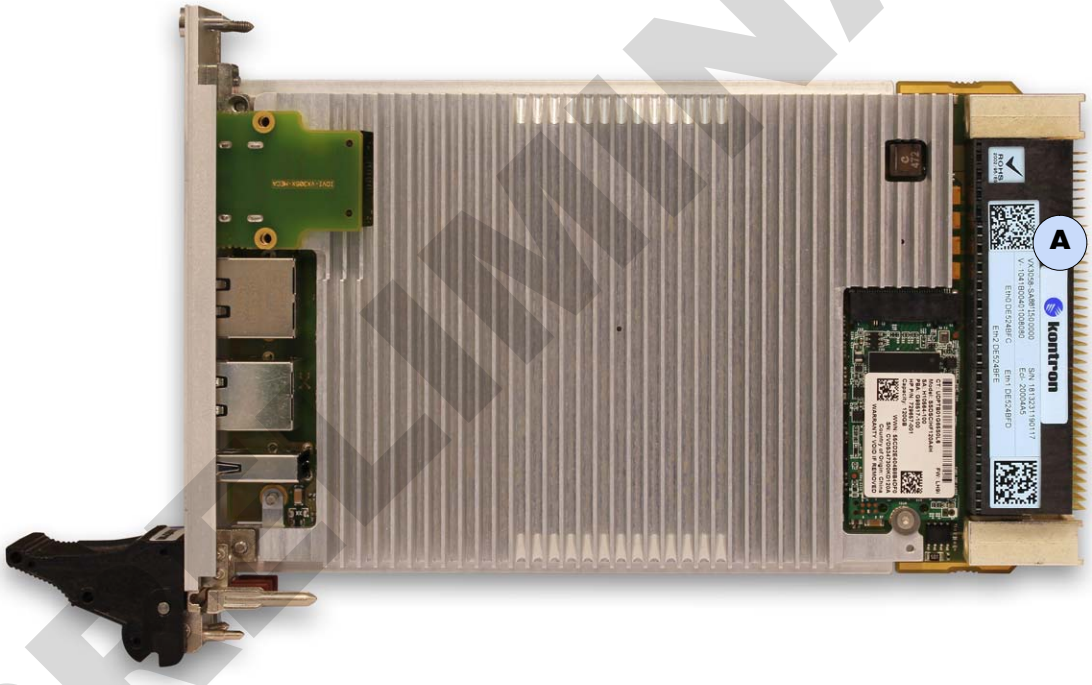


Figure 8: VX305x-SA Identification (Top Side)

2.3 Board Configuration

2.3.1 Microswitches

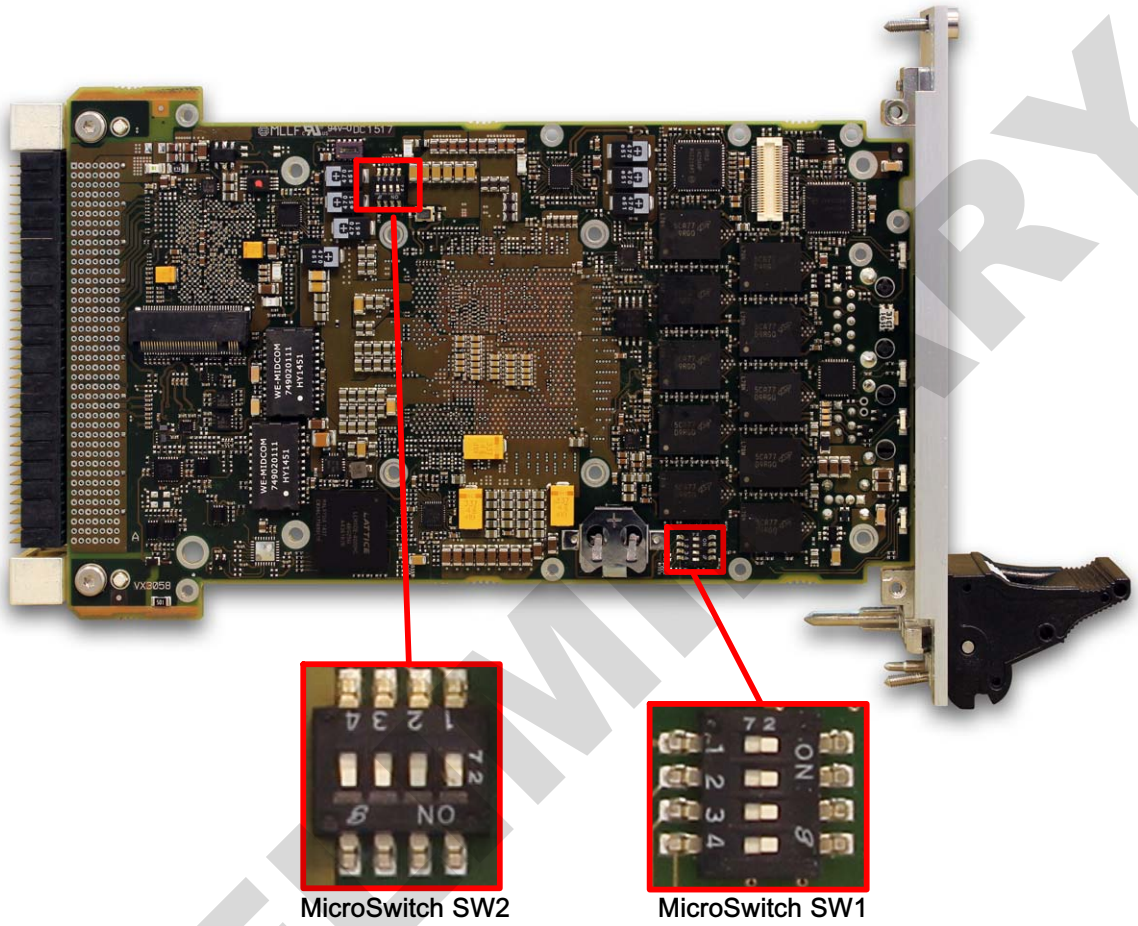


Figure 9: VX305x-SA Board Configuration (Bottom view)

Two microswitches are available on the VX305x-SA: SW1 and SW2.

2.3.2 SW1 Microswitch Description

Function	Description
1 - Factory Mode	off: Normal Mode on: Factory Mode
2 - Debug Mode	off: Normal Mode on: Debug Mode
3 - VPD Write Protection (VPD and SPD eeprom devices)	off: VPD Write protected on: VPD Writes are allowed
4 - User Write Protection (User FRAM device)	off: User FRAM writes are allowed on: User FRAM write protected

Table 8: SW1 Microswitch Description

2.3.3 SW2 Microswitch Description

Function	Description
1 - System Boot Flash	off: Normal Mode on: Rescue Mode
2 - BIOS Failsafe	off: Normal Mode on: BIOS Failsafe Mode
3 - PCIe Switch Failsafe Mode	off: Normal Mode on: PCIe Switch Failsafe Mode
4 - Force PROCHOT	off: Standard Mode on: Processor PROCHOT force to low state

Table 9: SW2 Microswitch Description

2.4 Package Content

The VX305x-SA is packaged with several components. The packing contents of the VX305x-SA Series may vary depending on customer requests.

- CPU Module:
  - Order Code: refer to section 1.3.3 “Order Code Table” :
    - Processor specifications differ depending on Order Code.
    - Heat sink assembled on the board.
- Rear Transition Module:
  - Order Code: refer to section 1.3.3 “Order Code Table”.

2.5 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the VX305x-SA in a system. Procedures for standard removal operations are found in their respective chapters.

To perform an initial installation of the VX305x-SA in a system proceed as follows:

1. Ensure that the safety requirements indicated in Section 2.1 are observed.

Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the VX305x-SA refer to Chapter 5. For the installation of VX305x-SA specific peripheral devices and Rear I/O devices refer to the appropriate sections in current Chapter.

Care must be taken when applying the procedures below to ensure that neither the VX305x-SA nor other system boards are physically damaged by the application of these procedures.

3. To install the VX305x-SA perform the following:
    1. Ensure that no power is applied to the system before proceeding.

When performing the next step, DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

    2. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.
    3. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
    4. Fasten the front panel retaining screws.
    5. Connect all external interfacing cables to the board as required.
    6. Ensure that the board and all required interfacing cables are properly secured.

The VX305x-SA is now ready for operation. For operation of the VX305x-SA, refer to appropriate VX305x-SA specific software, application, and system documentation.

2.6 Standard Removal Procedure

To remove the board from the chassis proceed as follows:

1. Ensure that the safety requirements indicated in Section 2.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

Care must be taken when applying the procedures below to ensure that neither the VX305x-SA nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.
5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

7. Dispose of the board as required.

2.7 Battery Replacement

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. The battery is used to run a time of day clock during the absence of power. Operation without the battery is possible but the date and time will not be retained in the absence of power. Alternatively, the VPX VBAT signal on P0 can provide a 3.3V voltage from the backplane to retain the date and time.

Make sure not to remove the battery support, this could damage the heatsink.

To replace the battery, proceed as follows:

> Turn off the power.

> Get the battery outside of its holder:

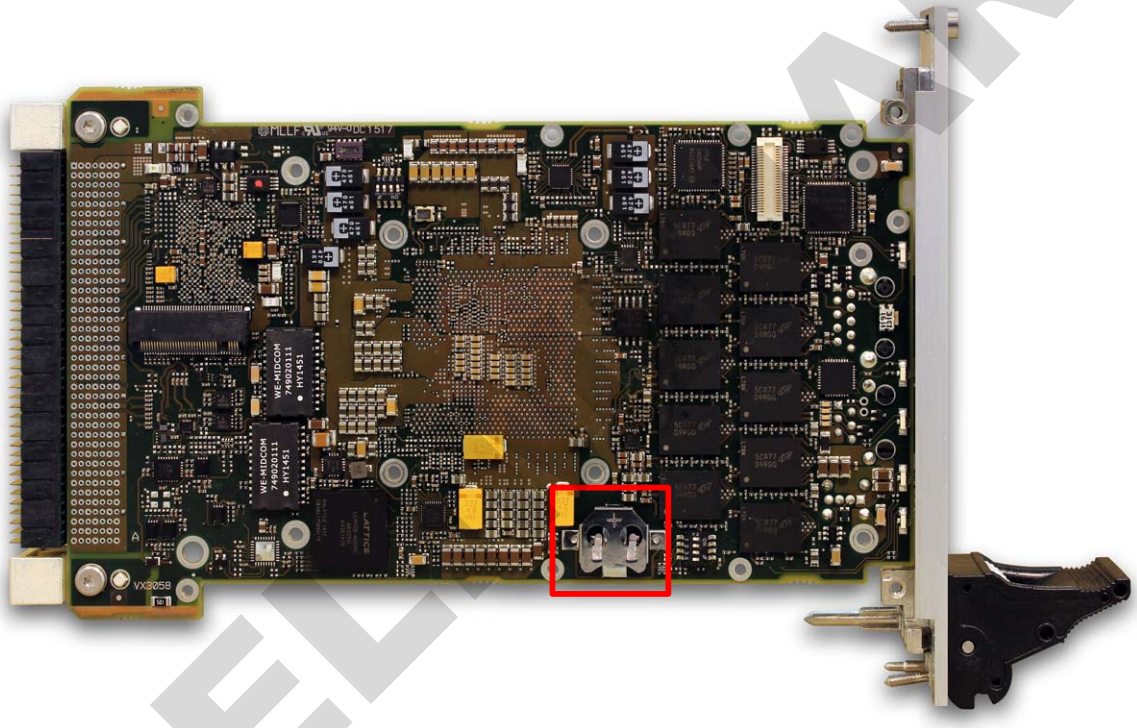


Figure 10: Battery Replacement on VX305x-SA Board

> Place the new battery in the socket with the plus pole facing upwards.

Note Care must be taken to ensure that the battery is correctly replaced.
The battery should be replaced only with an identical or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Note Reference of the battery used on the VX305x-SA: RAYOVAC BR1225A
The design of an electronic circuit powered by a component class battery requires the designer to consider two interacting paths that determine a battery's life: consumption of active electrochemical components and thermal wear-out.

2.8 XMC Module Insertion / Removal Instructions

XMC slot option is a nonstandard option because of thermal impacts and product restrictions with XMC slot - on demand only.

Mating

These connectors should be mated straight. Align the connectors and when the keys start to enter the keyways, push at the approximate center of the connector into the mating connector until the face of the receptacle cover bottoms on the face of the plug. Because of the asymmetric keying, reverse mating is impossible (the key end of the receptacle cannot be inserted into the non-keyway end of the plug). Both connectors have a lead-in around the perimeter that will allow blind mating.

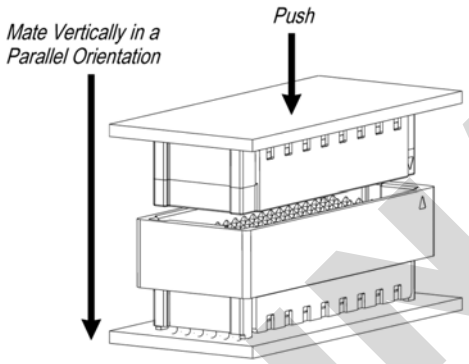


Figure 11: XMC Module Insertion

Unmating

These connectors can be unmated by pulling them straight apart or by “rocking” the connectors from side-to-side while pulling them apart.

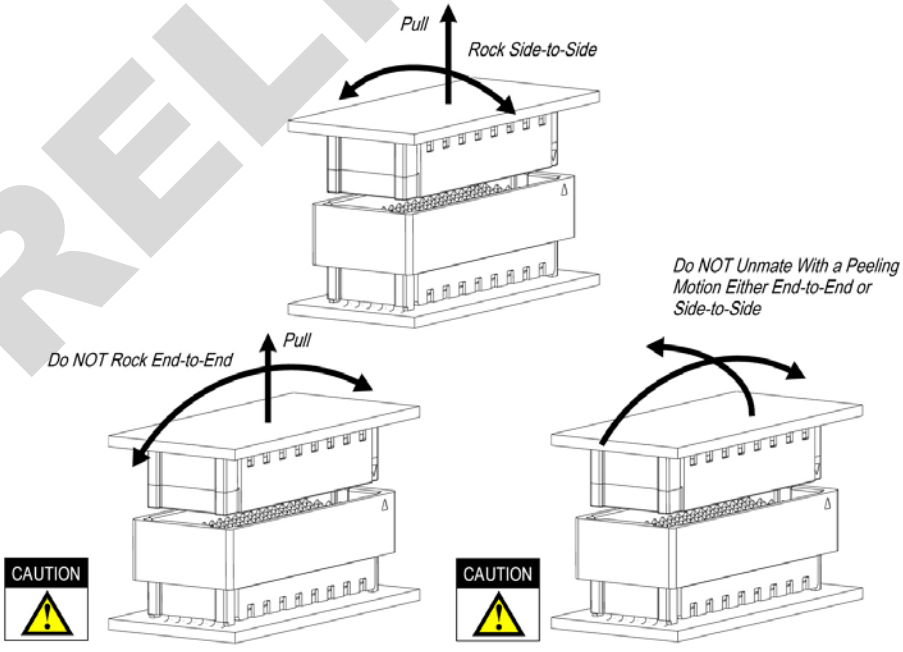


Figure 12: XMC Module Removal

2.9 M.2 Module Insertion / Removal Instructions

M.2 Module Insertion Process

1. Insert the module with angle 25°±5° until module touch HSG ramp.
2. Rotate the module to horizon by hand and make sure the card's edge touch HSG seating plane.
3. Fix the module with PCB by screw by hand.

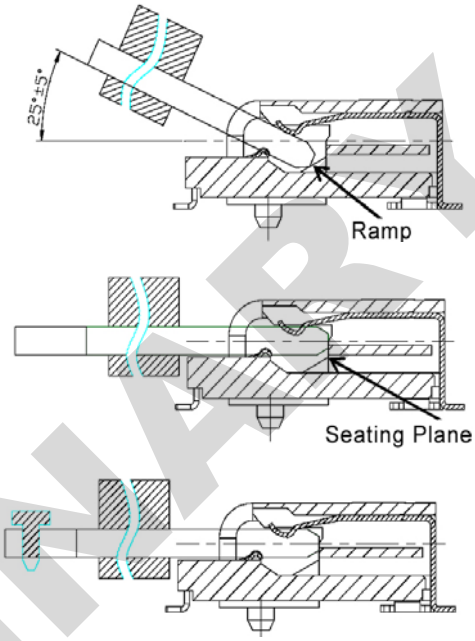


Figure 13: M.2 Module Insertion Process

M.2 Module Removal Process

1. Loose the screw by hand and the module will be rotated automatically due to connector contact's counterforce at the same time.
2. Take away the module by hand.

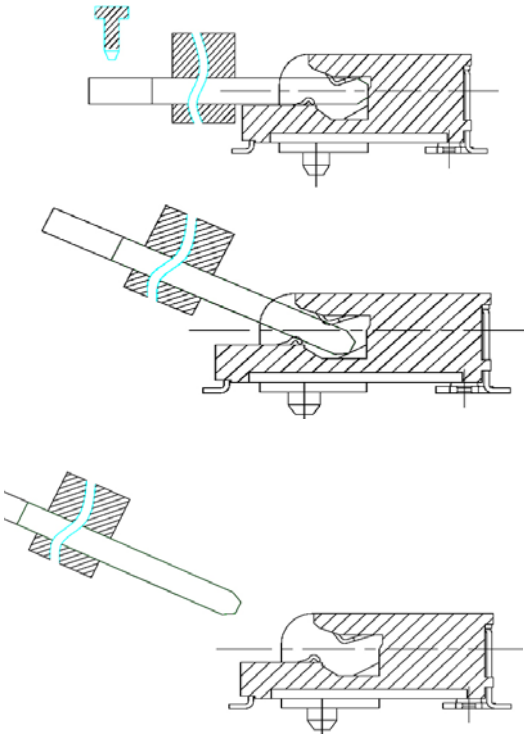


Figure 14: M.2 Module Removal Process

2.10 Software Installation

The installation of all onboard peripheral drivers is described in detail in the relevant Driver Kit files or Board Support Packages (BSP).

The installation of an operating system is dependent of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.

Chapter 3 - Additional Board Features

3.1 The Backplane Power Supplies and their Monitoring

The VITA46.0 standard specifies the backplane power supplies VS1 as follows:

- VS1: 12V +/- 5% inclusive of ripple (11.4V to 12.6V).

At Power On, a monotonic rise time no longer than 25 ms is required for VS1.

To ensure a valid Power Off, VS1 should remain at 0V for at least one second.

The voltage sensor NCT7802Y by Nuvoton is programmed by BIOS to monitor VS1 and asserts the signal PLD_PECI_ALERT_n whenever either voltage gets out of its VITA 46 specified range. This alert is routed to a maskable interrupt in the cPLD. There is no setup or UEFI command to modify the thresholds value in BIOS.

A second voltage sensor, the LTC2913 by Linear Technology monitors these voltages with a 10% tolerance. The thresholds are set by hardware on the board. Undervoltage and overvoltage conditions on VS1 are reported to the cPLD which in turn shuts down all VX305x-SA internal power supplies. There is no mechanism for masking these alerts.

3.2 RTC, Watchdog, Timers

3.2.1 Real-Time Clock (RTC)

Two Real Time Clocks (RTC) are available on the VX305x-SA: one is embedded in the PCH while the other is a standalone, high-precision, low-power component located on the integrated PCH SMBus (RV8564 by Micro Crystal). The latter is more precise and is powered when the board is off.

» Standby power supplied to the RV8564 RTC

When the VX305x-SA is powered off, the RTC is powered either by the onboard battery or through the 3.3V_AUX rail or the VBAT rail on the VPX backplane.

To ensure data retention in the RV8564 RTC, VBAT must be set in the range [2.5V - 5.5V]. The maximum current drawn over the -40°C/+85°C temperature range is 500nA (VBAT= 3V, no I2C activity) or 550 nA (VBAT=5V, no I2C activity).

The RTC present in the Panther Point PCH chipset is never powered by the battery.

» Internal Integrated PCH RTC

The integrayed PCH RTC module provides a date and time keeping device with two banks of static RAM with 128 bytes each. The BIOS programs the RTC interrupt on Legacy IRQ8 that is never shared with other interrupts. It is clocked by an external 32.768 KHz oscillator with a parabolic coefficient of 0.4 ppm/°C² and a stability of +/-20 ppm at 25°C. A 20 ppm stability is equivalent to a 10 mn/year drift.

Standalone low-power RTC RV8564

The RV8564C2/B RTC by Micro Crystal features an internal oscillator, date and time keeping module with programmable alarm, timer and interrupt functions. It has an ultra low-power consumption in time keeping mode: 250 nA, typical and 500 nA, maximum. Its stability is 20 ppm at 25°C. It is connected to the integrated PCH SMBus

RTC management by BIOS and OS

At each startup, the BIOS retrieves the date and time information from the high-precision RV8564 RTC and copies it into the integrated PCH RTC. This is necessary since the integrated PCH RTC is not saved.

Any update of date and time in the BIOS settings will be done both in integrated PCH RTC and RV8564 RTC.

Regarding the RTC management by the OS, the OS should use the high-precision RV8564 RTC driver. Failing to do so, the updates will be done only in integrated PCH RTC and will not be saved.

If no power is applied on the RV8564 RTC, the BIOS displays the BIOS build date and time instead of the current date and time.

Century flag

For compatibility reasons, the BIOS implements the century flag for the high-precision RTC as follows:

- Century Flag C = 0 for 1900-1999 years
- Century Flag C = 1 for 2000-2099 years.

The user should check that the OS driver implements the same convention.

3.2.2 CPLD Watchdog

In addition to the standard watchdog timer included in the integrated PCH, the cPLD implements a hardware watchdog timer that can be used by the operating software to monitor the normal operation of the system.

It is enabled by software, and once enabled must be restarted at regular intervals. If not, its expiration sets off an interrupt (IRQ) to the local processor, a board reset or a board power-cycle.

The watchdog has the following features:

- timeout programmable from 1 to 511 clock periods, by steps of 2 periods
- clock periods of 1s or 1ms
- lock bit: when set, can only refresh (restart) the watchdog, but not change its settings
- 4 modes: timer, reset, interrupt or power-cycle
- restart counter: can manage the remaining number of resets or power-cycles done by the watchdog before giving-up.

3.3 Battery and Supercap

Battery, supercap and VPX VBAT.

The industrial-grade battery BR1225A by RAYOVAC is mounted in a socket loacted on the board for air-cooled version.

Battery Life

Figure 15 gives an estimate of years of service at various discharge currents for BR Lithium coin cells at room temperatures. The RTC circuit power consumption is specified at 500 nA, giving an expected duration of more than 10 years in the absence of external power.

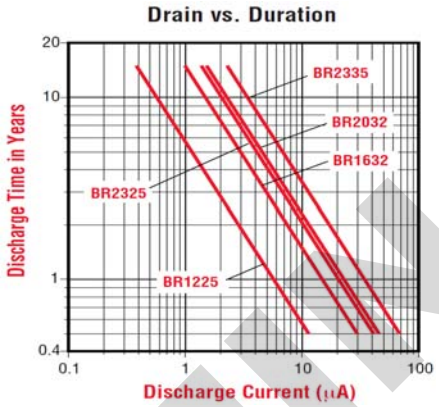


Figure 15: Battery Life

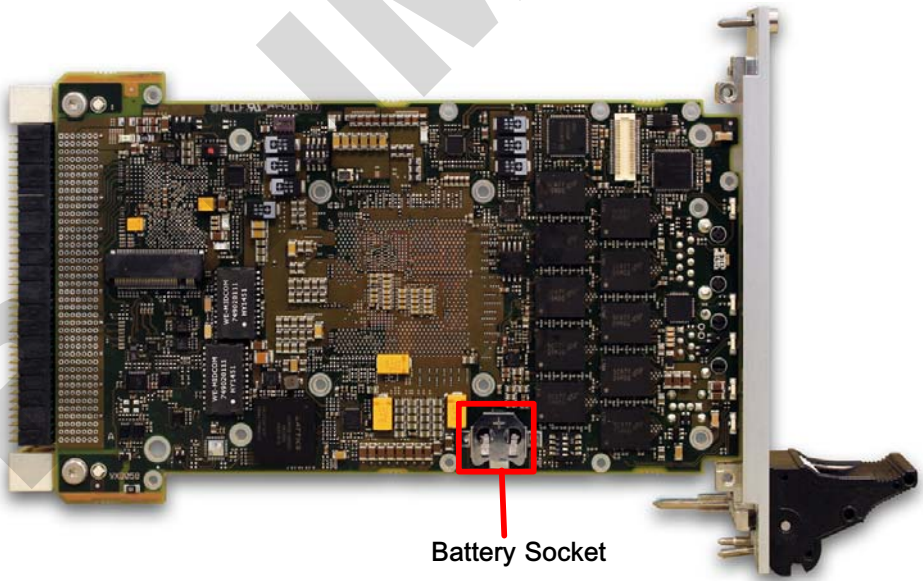


Figure 16: Battery Socket

Supercap

On demand.

3.4 I2C Structure

The VX305x-SA features three I2C busses.

> One is attached to the integrated Platform Hub Controller and controls the DDR4 SPD EEPROM and the low-power RTC.

> The other two are handled by the CPLD device according to Figure 17 “I2C Diagram”.

Note The I2C addresses shown are 8 bit values which include a read/write bit. Shift one bit to the right to get the 7-bit addresses.

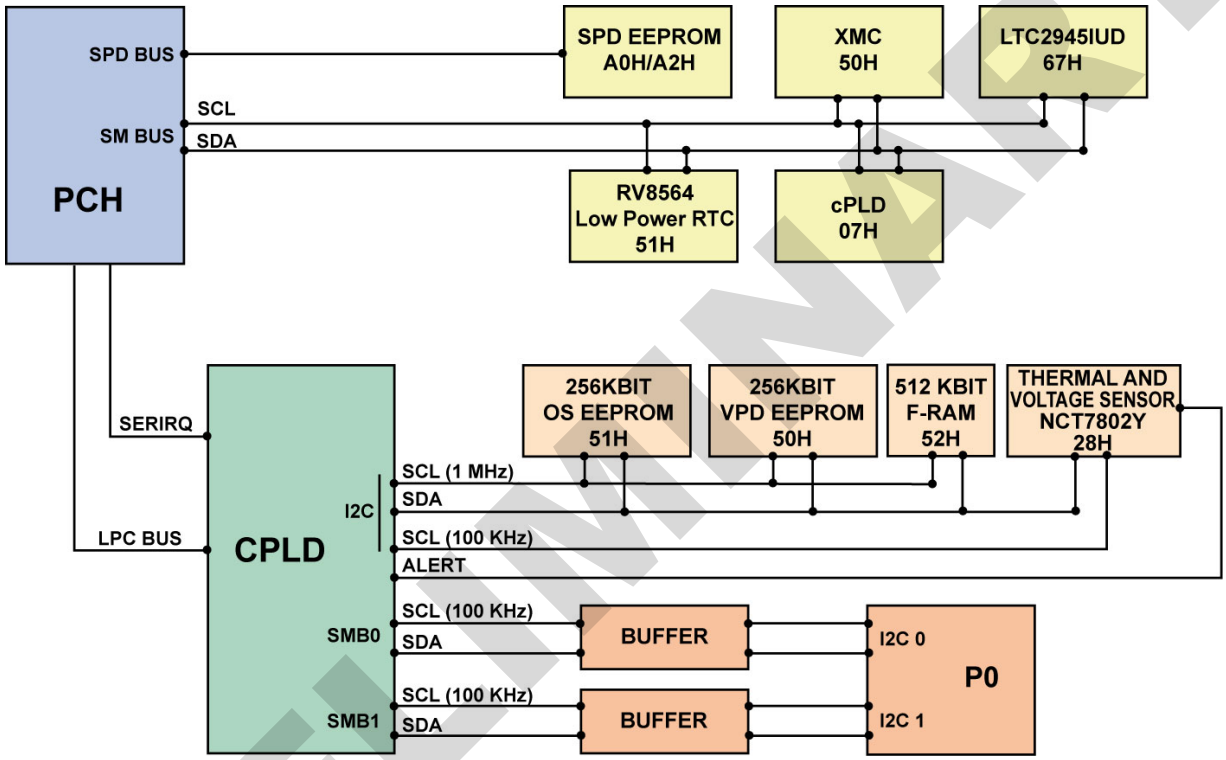


Figure 17: I2C Diagram

PCH SMBus (100 KHz)

Slave Devices on SOC SMBus Interface	SMBus 7-bit Base Address	Features
cPLD	07H (0x07)	System cPLD
LTC2945IUD	67H (0x67)	VS1 Current Monitoring
RV8564C2	51H (0x51)	External RTC Device
XMC Slot	50H (0x50)	To XMC Mezzanine SMBus

cPLD I2C Bus (100 KHz)

Slave Devices on cPLD SMBus Interface	SMBus 7-bit Base Address	Features
NCT7802Y sensor	28H (0x28)	Nuvoton Voltage / Temperature Sensor
24FC256-I/SN VPD EEPROM	50H (0x50)	256 Kbits VPE EEPROM
24FC256-I/SN OS EEPROM	50H (0x51)	256 Kbits OS EEPROM
FM24V10-G	52H (0x52)	1 Mbits User FRAM

3.5 CPLD Features

The CPLD manages the following features:

- Power-on/off control
- Reset control
- Local environmental control/monitoring
- LPC interface to processor
- I2C interfaces to I2C bus IPMB A/B (rear P0)
- LEDs control
- Serial lines multiplexer
- Serial VPD and user memories
- User and system GPIOs
- Internal registers that allow system management

3.5.1 cPLD Registers Definition:

3.5.1.1 Overview

These registers can be accessed from CPU through LPC bus at I/O address 0x800+offset.

Registers 0x72 to 0x78 can also be accessed from I2C bus 0 (register offset 0 to 6) by an external I2C master.

Offset	Name	Purpose	Access
0x72	I2C_BOARD_STATUS	Board state (from I2C)	RW
0x73	I2C_BOARD_CONTROL	Board state and control (from I2C)	RW
0x74	I2C_ERROR_STATUS	Board error state (from I2C)	RW
0x75	I2C_PORT80	PORT80 value (from I2C)	RW
0x76	I2C_FAILCODE	PEX8725 EEPROM CRC error status (from I2C)	RW
0x77	I2C_SCRATCHPAD	Not yet defined	RW
0x78	I2C_MISC	Miscellaneous board information (from I2C)	RW

Table 10: cPLD Registers Definition - Overwiew

For a detailed description of the CPLD registers, please contact Kontron.

3.5.1.2 Detailed Description

VX305x-SA VPX I2C interfaces

VX305x-SA implements two I2C buses connected to P0 VPX connector (see P0 pin assignments):

I2C0 : CLK signal on pin P0/B5, DATA signal on pin P0/ A5

I2C1: CLK signal on pin P0/G4, DATA signal on pin P0/ F4

I2C bus 0 is a master/slave interface .

I2C bus 1 is a master only interface .

> **VPX I2C bus 0 / 1 master interfaces:**

I2C bus 0/1 master interfaces software tools are described in Fedora relase note.

> **VPX I2C bus 0 slave interface:**

VX305x-SA board I2C bus 0 slave register base address depends on VPX slot ID (slot geographical address):

VPX Slot 1 (syscon): VX305x-SA slave I2C base address is 0x18 (I2C 7bits addressing)

VPX Slot 2: VX305x-SA slave I2C base address is 0x19 (I2C 7bits addressing)

VPX Slot 3: VX305x-SA slave I2C base address is 0x1A (I2C 7bits addressing)

And so on…..

> **I2C bus 0 slave registers definition :**

I2C_BOARD_STATUS : This Register can be accessed from I2C0 Slave interface :

- I2C_SLAVE_ADDR = 7'b0010_111 + GA
- Register offset (1 byte) = 0

Bits meaning during read access is controlled by bit 3 of register @73.

I2C_BOARD_STATUS @0x72 Can also be accessed from I2C0 slave interface with register offset 0 (or 0x10)				
Bit#	Name	Description	Reset	Type
7	Power Status	**Power Status** 0: Power Stand By 1: Power ON (S0 State)	0	RO
6-5	Reset Root	**Root cause of Last Reset Detected** 0x00 Internal PSUs power-on 0x01 Watchdog expired 0x10 SYSRESET (from VPX or VME) 0x11 Local reset : GPIO2 (maskable reset) reset switch reset from I2C (reg 0x73) reset by software asserting PLD_PLTRST_n	0	RO

I2C_BOARD_STATUS @0x72 Can also be accessed from I2C0 slave interface with register offset 0 (or 0x10)				
Bit#	Name	Description	Reset	Type
4	Reset Status	**Reset Status Side A** 0: No PWOK or reset asserted 1: PWOK and reset unasserted	0	RO
3-0	Boot Status	**Boot Status** 0x00: RESET : default hardware value 0x01: BIOS-BOOT : written by BIOS 0x02: BIOS : written by BIOS 0x03: PBIT : written by BIOS 0x04: OS-BOOT : written by BIOS 0x05: OS-RUNNING : to be written by OS at the end of boot 0x06: COMPLETED : to be written by the final application when running 0x07: SHUTDOWN : to be written by OS when issuing a halt/shutdown 0x08: REBOOT : to be written by OS when rebooting 0x09 - 0x0B: Reserved 0x0C - 0x0F: Customer defined These bits are Read Only through I2C Slave Interface and R/W through LPC Interface. The boot status is also reset at each board reset.	0	RW

Table 11: I2C_BOARD_STATUS @0x72

I2C_BOARD_CONTROL: This Register can be accessed from I2C0 Slave interface

- I2C_SLAVE_ADDR = 7'b0010_111 + GA
- Register offset (1 byte) = 1

I2C_BOARD_CONTROL @0x73 Can also be accessed from I2C0 slave interface with register offset 1 (or 0x11)				
Bit#	Name	Description	Reset	Type
7-4	Board Id	**Board Identification** 0001 VX6080 0010 VX6070 0011 VX3030 0100 VM6052/VM6054 0101 VM6050 0110 VX6060 0111 VX3035 1000 VX3040 family (VX3042/VX3044) **1001 VX305x family (VX3052/VX3058)** 1111 Reserved for non-SBC boards (switches, ...)	0	RO
3	Reserved	RESERVED	0	RW
2	Reserved	RESERVED	0	RW

I2C_BOARD_CONTROL @0x73 Can also be accessed from I2C0 slave interface with register offset 1 (or 0x11)				
Bit#	Name	Description	Reset	Type
1	Reset	0: No Reset 1: Reset Assert	0	RW
0	Power_OnOff	Power On/Off Control 0: Power Off (StandBy Mode) 1: Power On This bit can be used to do a Power OFF or control the Power-On sequence when Standby Power is applied. The default value is loaded when standby is applied from inverted SYSTEM EEPROM offset 0x100 bit 1, if FACTORY mode is not enabled WARNING: Setting this bit to 0 asserts VPX reset (SYSRESET_OUT#) if register 0x70 bit 0 (LOC2VPX) is set to 0 When this bit is used to do a Power Off (reset to 0), set this bit to 1 is not enough to do a Power-On : VPX PSUs must be switched Off and restarted.	*.	RW

Table 12: I2C_BOARD_CONTROL @0x73

I2C_ERROR_STATUS @0x74 Can also be accessed from I2C0 slave interface with register offset 2 (or 0x12)				
Bit#	Name	Description	Reset	Type
7	Alert	Alert 0: no alert 1: alert pending from PLD_PECI_ALERT# or PLD_PCHHOT_CPU# See register ALERT_STATUS@5B bit 0 and 3 for current state on these signals See register SERIRQ_CONTROL@0xF bit 6 and 2 for interrupt Mask and Status	0	RO
6	POST_Error	POST Error 0: no error 1: error This bit is set when PBIT has been run with errors (according to reg 0x2) Also set when RTC battery is low (according to reg 0x3 bit 0)	0	RO

I2C_ERROR_STATUS @0x74 Can also be accessed from I2C0 slave interface with register offset 2 (or 0x12)				
Bit#	Name	Description	Reset	Type
5	POST RTC	POST RTC 0: POST OK 1: POST FAILED (weak or missing battery) This bit is a copy of reg 0x3 bit 0 (POST_RTC), that is set when RTC battery is low	0	RO
4-0	Error_Status	Safety Error status Bit 4: THERMTRIP# Bit 3: VRVCCIN_VRHOT# Bit 2: VR1V05_VRHOT# Bit 1: CATERR# Bit 0: PECI_CRIT# When an **unmasked fatal alert** occurs, this register is updated, all internal PSUs are switched off and the error status is also reported on the front panel LEDs See also registers @79 @7A	0	RO

Table 13: I2C_ERROR_STATUS @0x74

I2C_PORT80 @ 0x75 Can also be accessed from I2C0 slave interface with register offset 3 (or 0x13)				
Bit#	Name	Description	Reset	Type
7-0	Port_80	Port 80 value The value of this register is automatically updated at each write access to port 0x80 (write snooping). It is cleared at each reset.	0	RW (LPC) RO (I2C)

Table 14: I2C_PORT80 @ 0x75

I2C_FAILCODE @ 0x76 Can also be accessed from I2C0 slave interface with register offset 4 (or 0x14)				
Bit#	Name	Description	Reset	Type
6-0			0	RW (LPC) RO (I2C)
0	PEX_EEPROM_ CRC_ERROR	PEX EEPROM CRC error 0: no error 1: error This bit is set by BIOS when a CRC error is detected on the PEX EEPROM	0	RW(LPC) RO (I2C)

Table 15: I2C_FAILCODE @ 0x76

I2C_SCRATCHPAD @ 0x77 Can also be accessed from I2C0 slave interface with register offset 5 (or 0x15)				
Bit#	Name	Description	Reset	Type
7-0	Scratchpad	**Scratchpad register** The purpose of this register is not defined	0	RW

Table 16: I2C_SCRATCHPAD @ 0x77

I2C_MISC @ 0x78 Can also be accessed from I2C0 slave interface with register offset 6 (or 0x16)				
Bit#	Name	Description	Reset	Type
7	Force_rescue	**Force Rescue Mode for System Flash Boot.** 0: not forced (default) 1: forced Changing this bit will take effect at next board reset (LPC reset) and override the Switch configuration. Register @09 bit 7 indicates the current Flash selected.	0	RW
6	Force_EFI_Shell	**Force stop at EFI shell.** 0: not forced (default) 1: forced	0	RW
5-3	Power_CUR	**Current power profile.** This field is updated by the board (BIOS/OS) according to its current power profile (power/TDP budget) 000: power profile unsupported other value: see below	000	RW (LPC) RO (I2C)
2-0	Power_REQ	**Requested power profile.** This filed is expected to be set by a shelf-manager (such as CMB) or another board, and used by the board (BIOS/OS) to set its power profile: 000: uncontrolled : the board uses its onboard switches and/or BIOS settings to set a power profile 001: low TDP 010: normal TDP 011: high TDP	000	RW

Table 17: I2C_MISC @ 0x78

POWER ERROR part 1 @ 0x79 Can also be accessed from I2C0 slave interface with register offset 7 (or 0x17)				
Bit#	Name	Description	Reset	Type
7-0	Power Error Part 1	This register indicates what are the Power rails failed when a power error is detected (see also register @7A) Bit 7: PWRGD_VPX Bit 6: PWRGD_VR5V0 Bit 5: VPXPWRGD_UV Bit 4: VPXPWRGD_OV Bit 3: VCCSCFUSESUS Bit 2: VCCKRHV Bit 1: VR1V05 Bit 0: VR2V5_DDR4 An error is reported if at least one PSU does not start within the expected delay (timeout) or fails after being OK. This register is cleared by switching the board off (standby) or by removing VPX power.	0	RO

Table 18: POWER ERROR part 1 @ 0x79

POWER ERROR part 2 @ 0x7A Can also be accessed from I2C0 slave interface with register offset 8 (or 0x18)				
Bit#	Name	Description	Reset	Type
7-0	Power Error Part 2	This register indicates what are the Power rails failed when a power error is detected (see also register @79) Bit 7: VR1V2 Bit 6: VTT Bit 5: Reserved Bit 4: VR1V5_PCH Bit 3: VRPEX Bit 2: VR3V3 Bit 1: VRVCCIN Bit 0: Safety_Alert (see register @74 for details) An error is reported if at least one PSU does not start within the expected delay (timeout) or fails after being OK. This register is cleared by switching the board off (standby) or by removing VPX power.	0	RO

Table 19: POWER ERROR part 2 @ 0x7A

3.6 Serial Lines EIA-422/485 Additional Modes

A total of 2 serial lines are available on VX305x-SA product.

EIA-232 serial lines are available on front panel RJ12 and P2 connectors.

See section 4.1.1 page 43 - “Serial Connector” and section 4.3.3 page 57 - “P2 Connector” for more information on pin assignments.

EIA-232 serial lines mode is the default mode, but EIA-422/485 mode can also be set with the following mode:

Mode	RJ12 fron panel connector	RJ12 front pin assignment	P2 rear connector	P2 rear pin assignment
Default EIA-232	EIA-232: COM1, COM2	COM1 TXD: pin 3 COM1 RXD: pin 4 COM2 TXD: pin 1 COM2 RXD: pin 6	EIA-232: COM1, COM2	COM1 TXD: pin G3 COM1 RXD: pin G7 COM2 TXD: pin G11 COM2 RXD: pin G15
EIA-422/485 on COM1	EIA-422/485: COM1	COM1 TXD+: pin 3 COM1 RXD+: pin 4 COM1 TXD-: pin 1 COM1 RXD-: pin 6	EIA-422/485: COM1	COM1 TXD+: pin G3 COM1 RXD+: pin G7 COM1 TXD-: pin G11 COM1 RXD-: pin G15

Table 20: Serial Lines Additional Modes

The mode EIA-232 or EIA-422/485 is selected in the BIOS by the user. When EIA-422/485 is selected, an optional on board 120 Ohms termination can be activated from the BIOS Menu, as well as a half duplex mode.

3.7 GPIOs and GDISCRETE1

GPIOs

The VX305x-SA features 5 GPIOs managed by the CPLD. Please refer to Fedora Release Note chapter 7.7 for further details on the GPIO driver.

- 3 GPIOs are available on P0 connector: GPIO3, GPIO4 and GPIO5. Refer to section 4.3.1 “P0 Connector” page 53 for detailed pinout.
- 2 GPIOs are available on P1 connector, GPIO1, GPIO2. Refer to section 4.3.2 “P1 Connector” page 55 for detailed pinout.

GPIO electrical characteristics: The CPLD features LVCMOS33 cells (0-3V3), drive strength = 8 mA (sink or source), a clamp diode which is not 5V tolerant, an hysteresis of 250mV. The CPLD does not implement any internal pull-up or pull-down.

On the VX305x-SA board, a pull-up of 47 kOhms is connected to GPIO1 to GPIO5.

GPIOs are not 5V tolerant. Maximum voltage on GPIOs is 3.6 V. Absolute maximum voltage is 3.75V and is not suitable for continuous operation. Appropriate voltage reduction (through resistor divider for instance) must be made to avoid permanent damage to the board.

The GPIOs share the same interrupt in the CPLD.

GDISCRETE1

GDISCRETE1 is a bussed open-collector GPIO defined by OpenVPX VITA 65 and available on P1. Refer to section 4.3.2 “P1 Connector” page 55 for detailed pinout.

It is handled by the CPLD and buffered by a SN74LVC1G125 wired as an Open Collector to meet the electrical characteristics defined in VITA 65.

It has a dedicated interrupt in the CPLD.

Chapter 4 - Physical I/O

4.1 Front Panel Connectors

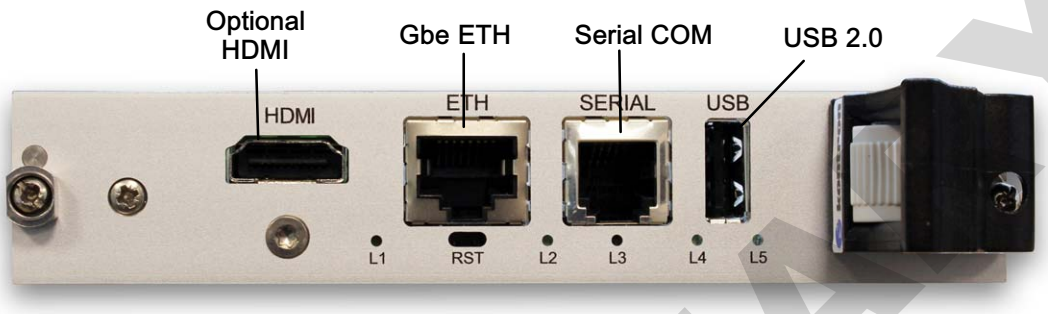


Figure 18: Location of the Front Panel Connectors

4.1.1 Serial Connector - COM

The VX305x-SA integrates two serial communication ports, COM1 and COM2 in PC parlance. COM1 and COM2 are available via the VPX P2 connector.

Default serial mode is simplified serial line mode Rx/Tx only, 115200bauds.

COM1 is also available via the front panel connector.

> COM1: EIA-232 or EIA-485 (simplified RX/TX) port on RJ-12 front panel connector or on the rear P2 connector

> COM2: EIA-232 or EIA-485 (simplified RX/TX) port on the rear P2 connector

Each serial port is configurable via the CPLD as EIA-232 or EIA-485. Each port operates in full duplex mode. Fast slew rate is the default mode in EIA-485 mode.

The signaling level of EIA-485 is compatible with EIA-422, so full duplex EIA-485 may also be used for point-to-point communications with an EIA-422 serial port.

Refer to section 4.3.3 “ P2 Connector” page 57 for more information on the serial lines wafer assignment on P2 connector.

» Pin Assignment

PIN	SIGNAL
1	COM2 TXD / COM1TXD-
2	Shell
3	COM1 TXD/TXD+
4	COM1 RXD/RXD+
5	GND
6	COM2 RXD/COM1 RXD-

Table 21: Serial Connector Pin Assignment

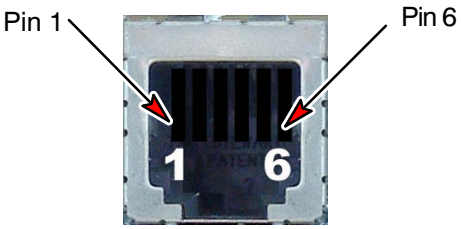


Figure 19: Serial Connector

A serial line should only be used via one connector at the same time, either the Serial front panel connector or the P2 connector.

MNEMONIC	DESCRIPTION
COM2 RXD/COM1 RXD-	COM2 Receive Data (EIA-232) / COM1 Receive Data minus (EIA-485)
COM2 TXD/COM1 TXD-	COM2 Transmit data (EIA-232) / COM1Transmit Data minus (EIA-485)
COM1 RXD/RXD+	COM1 Receive Data (EIA-232) / Receive Data plus (EIA-485)
COM1 TXD/TXD+	COM1 Transmit Data (EIA-232) / Transmit Data plus (EIA-485)
GND	Ground
Shell	Chassis Ground

Table 22: Serial Connector Signal Description

Serial Cable Designation

Serial cable is:

- RJ-14 (6 pin, 4 conductor) for a simple EIA-232 without handshake support.
- RJ-12 (6 pin, 6 conductor) for EIA-232 with handshaking.

  A RJ-12 to DB9/DB25 male or DB9/DB25 female adapter is available from multiple sources, such as:

  - Kontron Order Code KIT-2X-RJ12DB9
  - Triangle Cable http://www.trianglecables.com/db9m-rj12.html

DB9 Pin Connector	Signal	RJ-12 Pin Connector
1	RTS	1
2	TXD	3
3	RXD	4
4	CTS	6
5	GND	5

Table 23: Serial Cable Pin Assignment

Figure 20: Serial Cable

4.1.2 Gigabit Ethernet Connector

The Ethernet transmission should operate using a CAT5 cable with a maximum length of 100 m.

The Ethernet connectors are available as RJ-45 connectors with tab down. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

Pin Assignment

PIN	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-		I/O	BI_DC+
5	-	-	-		I/O	BI_DC-
6	I	RX-	I	RX-	I/O	BI_DB-
7	-	-	-		I/O	BI_DD+
8	-	-	-		I/O	BI_DD-
Shell	Chassis Ground					

Table 24: Gigabit Ethernet Connector Pin Assignment

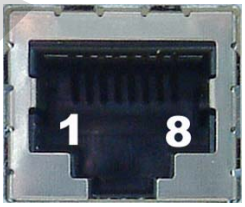


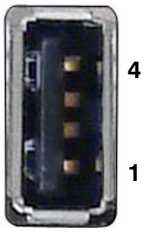
Figure 21: Ethernet Connector

4.1.3 USB Connector

Pin Assignment

PIN	SIGNAL	FUNCTION	I/O
1	VCC (+5V Protected)	VCC	--
2	USB_D-	Differential USB-	I/O
3	USB_D+	Differential USB+	I/O
4	GND	GND	--

Table 25: USB Connector Pin Assignment



USB

Figure 22: USB Connector

4.1.4 HDMI Port

PIN	SIGNAL
1	TMDS Data2+
2	TMDS Data2 Shield
3	TMDS Data2-
4	TMDS Data1+
5	TMDS Data1 Shield
6	TMDS Data1-
7	TMDS Data0+
8	TMDS Data0 Shield
9	TMDS Data0-
10	TMDS Clock+
11	TMDS Clock Shield
12	TMDS Clock-
13	N.C.
14	N.C.
15	SCL
16	SDA
17	GND
18	+5V
19	Hot Plug Detect

Table 26: HDMI Port Pin Assignment

Figure 23: HDMI Port Cable

4.2 Onboard Connectors

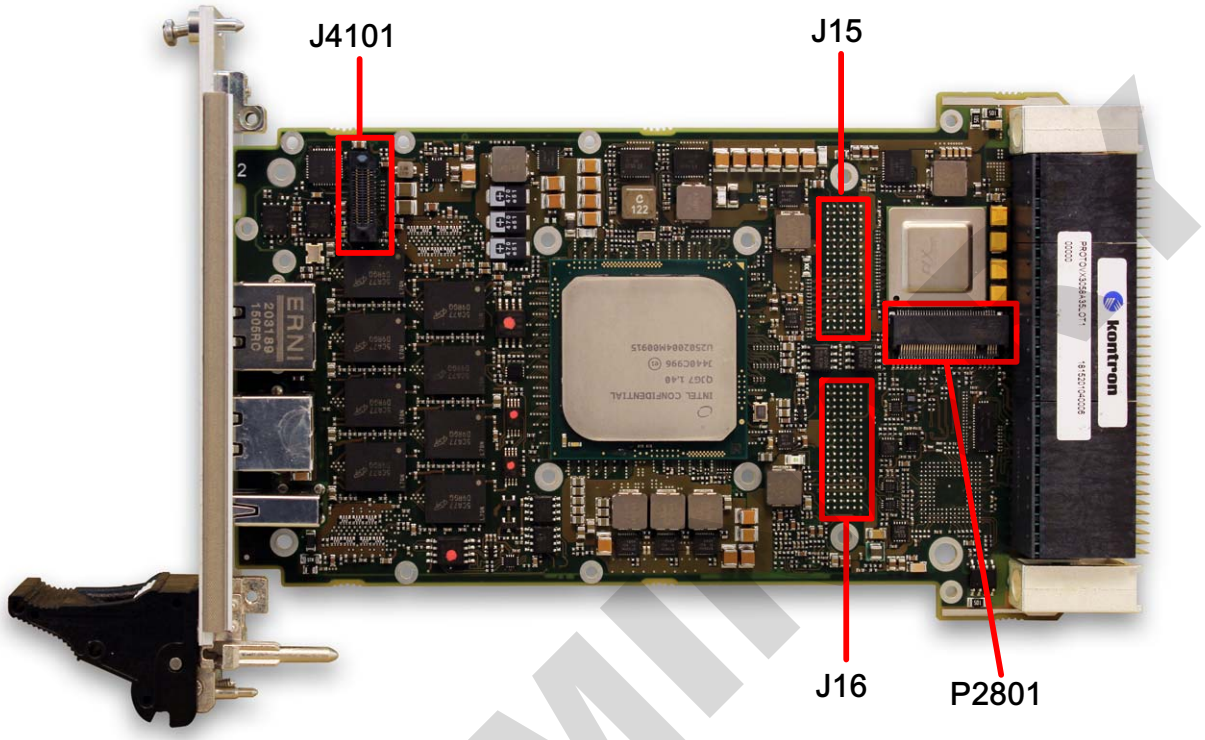


Figure 24: Onboard Connectors

4.2.1 XMC J15 Connector Pin Assignments

XMC slot option is a nonstandard option because of thermal impacts and product restrictions with XMC slot - on demand only.

The pin assignment of the J15 XMC PCI Express connector is pin compatible with VITA 42.0 and VITA 42.3. This interface is a PCI Express with 8 lanes coming from the PEX8725 PCIe switch.

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR (1)
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR (1)
4	GND	GND	TCK	GND	GND	NC
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR (1)
6	GND	GND	TMS	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR (1)
8	GND	GND	TDI	GND	GND	-12V
9	RFU	RFU	N.C.	RFU	RFU	VPWR (1)
10	GND	GND	TDO	GND	GND	GA0
11	PER0p0	PER0n0	NC	PER0p1	PER0n1	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT #
13	PER0p2	PER0n2	3.3V AUX	PER0p3	PER0n3	VPWR (1)
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	N.C.	PER0p5	PER0n5	VPWR (1)
16	GND	GND	NVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	N.C.	PER0p7	PER0n7	N.C.
18	GND	GND	N.C.	GND	GND	N.C.
19	REFCLK+0	REFCLK-0	N.C.	N.C.	N.C.	N.C.

(1) VPWR is connected to +5V via a fuse.
The 12V option is available, please contact Kontron for more information on this topic.

Signals active when low.

Table 27: XMC J15 Connector Pin Assignments

4.2.2 XMC J16 Connector Pin Assignment

XMC slot option is a nonstandard option because of thermal impacts and product restrictions with XMC slot - on demand only.

XMC I/O signals are routed to the VPX P2 connector according VITA 46.9 x8d for differential pairs (8 pairs) and x38s for single ended (4 last signals).

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	XMCIO_DP1-	XMCIO_DP1+	NC	XMCIO_DP2-	XMCIO_DP2+	NC
2	GND	GND	NC	GND	GND	NC
3	XMCIO_DP3-	XMCIO_DP3+	NC	XMCIO_DP4-	XMCIO_DP4+	NC
4	GND	GND	NC	GND	GND	NC
5	NC	NC	NC	Reserved	Reserved	NC
6	GND	GND	NC	GND	GND	NC
7	NC	NC	NC	NC	NC	NC
8	GND	GND	NC	GND	GND	NC
9	NC	NC	NC	NC	NC	NC
10	GND	GND	NC	GND	GND	NC
11	XMCIO_DP5-	XMCIO_DP5+	NC	XMCIO_DP6-	XMCIO_DP6+	NC
12	GND	GND	NC	GND	GND	NC
13	XMCIO_DP7-	XMCIO_DP7+	NC	XMCIO_DP8-	XMCIO_DP8+	NC
14	GND	GND	NC	GND	GND	NC
15	Reserved	Reserved	NC	Reserved	Reserved	NC
16	GND	GND	Reserved	GND	GND	Reserved
17	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
18	GND	GND	XMCIO_SE3	GND	GND	XMCIO_SE4
19	Reserved	Reserved	XMCIO_SE1	Reserved	Reserved	XMCIO_SE2

Table 28: XMC J16 Connector Pin Assignment

- XMCIO signals are routed to VPX P2 connector, please refer to VPX P2 pin assignment figure.
- NC pins are not connected on VX305x-SA board

4.2.3 J4101 Connector Pin Assignment

J0401 is dedicated to Front /IO module options.

PIN	SIGNAL	FUNCTION
1	GND	
2	GND	
3	DVI_SCL	Optional Front DVI Port
4	ETH2_MDI3 -	Optional 2nd Ethernet MDI Interface
5	DVI_SDA	Optional Front DVI Port
6	ETH2_MDI3 +	Optional 2nd Ethernet MDI Interface
7	GND	
8	GND	
9	DVI_C_CLK +	Optional Front DVI Port
10	ETH2_MDI2 -	Optional 2nd Ethernet MDI Interface
11	DVI_C_CLK -	Optional Front DVI Port
12	ETH2_MDI2 +	Optional 2nd Ethernet MDI Interface
13	GND	
14	GND	
15	DVI_C_TMDS0 +	Optional Front DVI Port
16	ETH2_MDI1 -	Optional 2nd Ethernet MDI Interface
17	DVI_C_TMDS0 -	Optional Front DVI Port
18	ETH2_MDI1 +	Optional 2nd Ethernet MDI Interface
19	GND	
20	GND	
21	DVI_C_TMDS1+	Optional Front DVI Port
22	ETH2_MDI0 -	Optional 2nd Ethernet MDI Interface
23	DVI_C_TMDS1 -	Optional Front DVI Port
24	ETH2_MDI0 +	Optional 2nd Ethernet MDI Interface
25	GND	
26	GND	
27	DVI_C_TMDS2 +	Optional Front DVI Port
28	Reserved	
29	DVI_C_TMDS2 -	Optional Front DVI Port
30	Reserved	
31	GND	
32	GND	
33	DVI_HPD	
34	Reserved	
35	RST#	
36	Reserved	
37	Reserved	
38	GND	
39	Reserved	
40	V_FRONTIO	

Table 29: J4101 Connector Pin Assignment

4.2.4 P2701/P2801 Connector Pin Assignment

P2701/P2801 are the top/bottom M.2 slot connectors.

PIN	SIGNAL	PIN	SIGNAL
1	GND_1	2	3V3_2
3	GND_3	4	3V3_4
5	PER3_N	6	Reserved
7	PER3_P	8	Reserved
9	GND_9	10	DAS/DSS#LED1#
11	PET3_N	12	3V3_12
13	PET3_P	14	3V3_14
15	GND_15	16	3V3_16
17	PER2_N	18	3V3_18
19	PER2_P	20	Reserved
21	GND_21	22	Reserved
23	PET2_N	24	Reserved
25	PET2_P	26	Reserved
27	GND_27	28	Reserved
29	PER1_N	30	Reserved
31	PER1_P	32	UART_RXD
33	GND_33	34	Reserved
35	PET1_N	36	Reserved
37	PET1_P	38	DEVSLP
39	GND_39	40	Reserved
41	PER0_N/SATA-B+	42	Reserved
43	PER0_P/SATA-B-	44	Reserved
45	GND_45	46	Reserved
47	PET0_N/SATA-A-	48	Reserved
49	PET0_P/SATA-A+	50	PERST#
51	GND_51	52	CLKREQ#
53	REFCLK_N	54	PEWAKE#
55	REFCLK_P	56	Reserved
57	GND_57	58	Reserved
59	CONNECTOR_KEY_59	60	CONNECTOR_KEY_60
61	CONNECTOR_KEY_61	62	CONNECTOR_KEY_62
63	CONNECTOR_KEY_63	64	CONNECTOR_KEY_64
65	CONNECTOR_KEY_65	66	CONNECTOR_KEY_66
67	NC_67	68	SUSCLK
69	PEDET	70	3V3_70
71	GND_71	72	3V3_72
73	GND_73	74	3V3_74
75	GND_75		

Table 30: P2801 Connector Pin Assignment

4.3 Rear Connectors

VPX Bus Interface

The complete 3U VPX connectors configuration comprises three connectors named P0 to P2:

- P0: 8-wafer 7-row connector.
- P1 - P2: 16-wafer 7-row differential connectors.

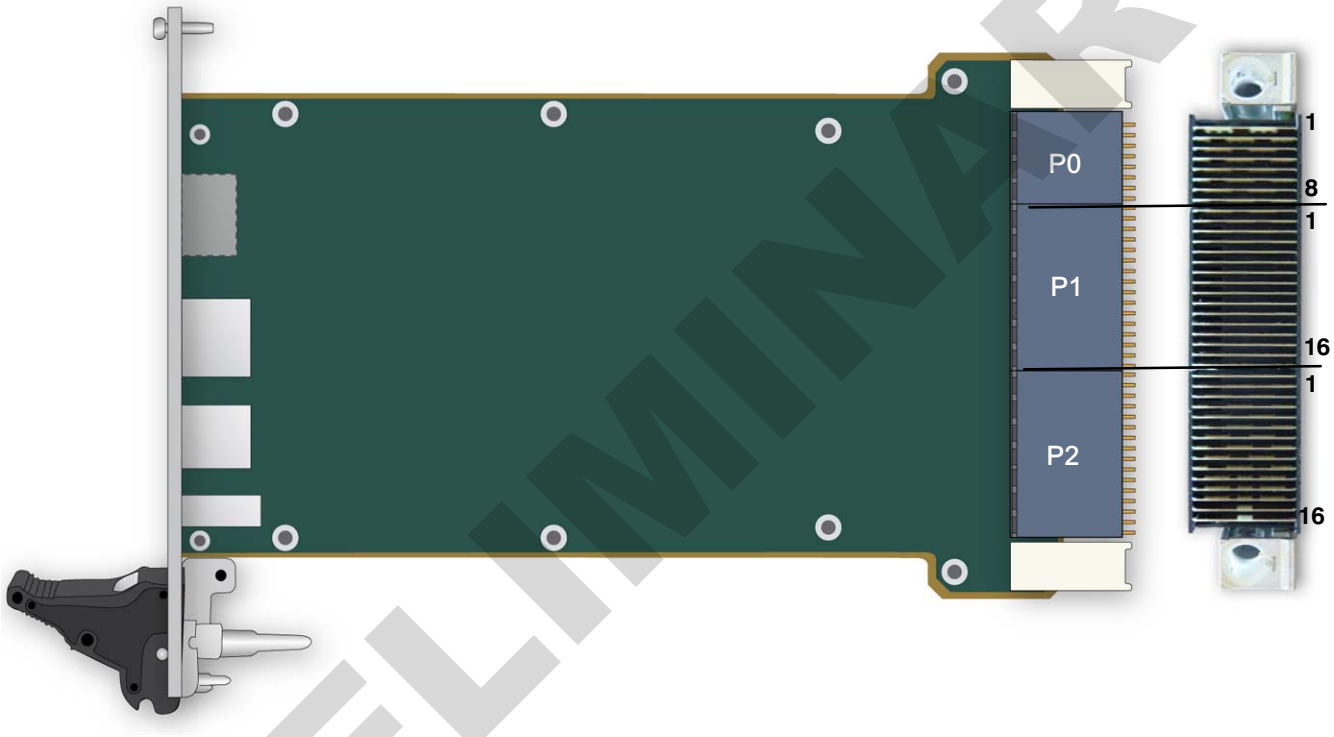


Figure 25: VPX Connectors

4.3.1 P0 Connector

P0 Wafer Assignment

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	+12V	+12V	+12V	NC	NC (VS2)	NC (VS2)	NC (VS2)
2	+12V	+12V	+12V	NC	NC (VS2)	NC (VS2)	NC (VS2)
3	NC (VS3)	NC (VS3)	NC (VS3)	NC	NC (VS3)	NC (VS3)	NC (VS3)
4	I2C1 CLK	I2C1 DAT	GND	-12V_AUX	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3V3_AUX	GND	I2C0 CLK	I2C0 DAT
6	GA3*	GA2*	GND	NC (+12V_AUX)	GND	GA1*	GA0*
7	GPIO5 (TCK)	GND	PCIe_CLK - (TDO)	PCIe_CLK+ (TDI)	GND	GPIO3_10GMCK (TMS)	GPIO4_10GMD (TRST)
8	GND	REF_CLK-	REF_CLK +	GND	AUX_CLK-	AUX_CLK+	GND
CASE	GND						

* signal active when low

Table 31: VPX Connector P0 Wafer Assignment

P0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
+12V	+12 Volts DC power (VS1 VPX supply). NC (+12V) pins are not connected (VS2 VPX supply)
-12V_AUX	-12 Volts auxiliary power. Only used to supply XMC if needed.
NVMRO	Non-Volatile Memory Read Only. When asserted (logical 1), prevents any non-volatile memory from being updated.
GAi	Geographical address pins
GAP	Geographical address parity
GND	Ground
GPIO5*	General purpose I/O 5 (handled by CPLD)
GPIO3_10GMCK*	General purpose I/O 3 (handled by CPLD) or Ethernet 10G I2C clock for rear SFP+
GPIO4_10GMD*	General purpose I/O 4 (handled by CPLD) or Ethernet 10G I2C data for rear SFP+
I2C0	I2C Bus 0
I2C1	I2C Bus 1
REF_CLK+/-	The Reference Clock is a bussed differential pair. Output if the VX305x-SA is plugged in the system controller slot, input otherwise. It enables the entire system to synchronize to a common time reference if desired. Counter/timer in the CPLD can use this clock
AUX_CLK+/-	1 PPS (one pulse per second) clock input. Can be programmed as an output on system controller slot. Can be used to phase the CPLD timer/counter clocked by REF_CLK+/-.
PCIe_CLK+/-	Optional Common Reference PCI Express Clock input.
SYSRESET*	System Reset. Input and open collector output.

* Refer to section 3.7 - GPIOs and GDISCRETE1 - page 41.

Table 32: VPX Connector P0 Signal Definition

4.3.2 P1 Connector

P1 Wafer Assignment

> Legend for Table 33:

P1_VBAT	Battery Voltage	USB0/1 USB3	USB2 links 1 and 13 from PCH USB3 link 2 from PCH
P1_SYS_CON*	System Controller	SATA0/1	SATA links 0 and 1 from PCH
PCIe0 LxRX | LxTX	x8, 2 x4 or 4 x2 PCI-Express	ETHx TX/RX	1000BASE-BX Ethernet controller or 10GbaseKR links 0 and 1 from integrated 10 GbE controller as per VITA 46.7.
		ETH2 DA/DB/DC/DD	1000BASE-T link from I210IT GbE controllers

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	GDISCRETE1	GND	PCIe0 L0-TX-	PCIe0 L0-TX+	GND	PCIe0 L0-RX-	PCIe0 L0-RX+
2	GND	PCIe0 L1-TX-	PCIe0 L1-TX+	GND	PCIe0 L1-RX-	PCIe0 L1-RX+	GND
3	VBAT	GND	PCIe0 L2-TX-	PCIe0 L2-TX+	GND	PCIe0 L2-RX-	PCIe0 L2-RX+
4	GND	PCIe0 L3-TX-	PCIe0 L3-TX+	GND	PCIe0 L3-RX-	PCIe0 L3-RX+	GND
5	SYS_CON*	GND	PCIe0 L4-TX-	PCIe0 L4-TX+	GND	PCIe0 L4-RX-	PCIe0 L4-RX+
6	GND	PCIe0 L5-TX-	PCIe0 L5-TX+	GND	PCIe0 L5-RX-	PCIe0 L5-RX+	GND
7	Reserved	GND	PCIe0 L6-TX-	PCIe0 L6-TX+	GND	PCIe0 L6-RX-	PCIe0 L6-RX+
8	GND	PCIe0 L7-TX-	PCIe0 L7-TX+	GND	PCIe0 L7-RX-	PCIe0 L7-RX-	GND
9	USB PWR	GND	SATA0 TX-	SATA0 TX+	GND	SATA0 RX-	SATA0 RX+
10	GND	SATA1 TX-	SATA1 TX+	GND	SATA1 RX-	SATA1 RX+	GND
11	USB PWR	GND	USB3 TX-	USB3 TX+	GND	USB3 RX-	USB3 RX+
12	GND	USB0 DA-	USB0 DA+	GND	USB1 DA-	USB1 DA+	GND
13	GPIO1	GND	ETH2 DB-	ETH2 DB+	GND	ETH2 DA-	ETH2 DA+
14	GND	ETH2 DD-	ETH2 DD+	GND	ETH2 DC-	ETH2 DC+	GND
15	Maskable Reset* or GPIO2	GND	ETH1 TX-	ETH1 TX+	GND	ETH1 RX-	ETH1 RX+
16	GND	ETH0 TX-	ETH0 TX+	GND	ETH0 RX-	ETH0 RX+	GND
CASE	GND						

* signal active when low

Table 33: VPX Connector P1 Wafer Assignment

P1 Signal Definition

MNEMONIC	SIGNAL DEFINITION
P1-REF_CLK_SE	Reserved
PCIe0 L*x*-RX+/-	x8 PCI Express Link. Receive +/-, gen1, gen2 or gen3 Can also be used as a 2 x4 links or 4 x2 links
PCIe0 Lx-TX+/-	x8 PCI Express Link. Transmit +/-, gen1, gen2 or gen3 Can also be used as a 2 x4 links or 4 x2 links
SATAx RX+/-	Serial ATA. Receive +/- link x
SATAx TX+/-	Serial ATA. Transmit +/- link x
USB PWR	USB Power
USBx D+/-	Differential Data pair of USB link x
USB3 TX+/- RX+/-	Differential Data transmit and receive of USB3 link
ETH2 DA+/-	Ethernet 1000BASE-T: First pair of transmit/receive data.
ETH2 DB+/-	Ethernet 1000BASE-T: Second pair of transmit/receive data
ETH2 DC+/-	Ethernet 1000BASE-T: Third pair of transmit/receive data.
ETH2 DD+/-	Ethernet 1000BASE-T: Fourth pair of transmit/receive data
ETHx RX+/-	1000BASE-BX or 10GbaseKR Ethernet x: Receive data +/-
ETHx TX+/-	1000BASE-BX or 10GbaseKR Ethernet x: Transmit data +/-
GDISCRETE1	Open VPX GDISCRETE1 signal
GPIO1*	General Purpose I/O 1 (handled by the CPLD)
Maskable Reset* or GPIO2	General purpose I/O 2 (handled by CPLD) or Optional reset input (may be left unconnected if not used).
GND	Ground
SYS_CON	System Controller Slot Indication
VBAT	Battery Voltage Input, 3V. Optional alternated source for RTC backup voltage.

* Refer to section 3.7 - GPIOs and GDISCRETE1 - page 41.

Table 34: VPX Connector P1 Signal Definition

4.3.3 P2 Connector

XMC slot option is a nonstandard option because of thermal impacts and product restrictions with XMC slot - on demand only.

P2 Wafer Assignment

> Legend for Table 35:

COM1/2	Simplified asynchronous serial lines	PCIe1_TX/RX	Additionnal PCI express x1 link from PCH
USB2/3	USB links 2 and 12 from PCH	PCIe1_CLK	Additionnal PCI express clock from PCH
SATA2/3	SATA links 2 and 3 from PCH	XMCIO_SE1-4	Single ended XMC IO pins C19,F19,C18,F18 according VITA46.9 X38s
ETH3	ETH3 from PCH	XMCIO_DP1-8	Differential XMC IO pins according VITA46.9 X8d

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	NC	GND	SATA2 TX-	SATA2 TX+	GND	SATA2 RX-	SATA2 RX+
2	GND	SATA3 TX-	SATA3 TX+	GND	SATA3 RX-	SATA3 RX+	GND
3	COM1 TXD/TXD+	GND	USB PWR	USB PWR	GND	USB PWR	USB PWR
4	GND	USB2 DA-	USB2 DA+	GND	NC	NC	GND
5	NC	GND	ETH3 DB--	ETH3 DB+	GND	ETH3 DA-	ETH3 DA+
6	GND	ETH3 DD-	ETH3 DD+	GND	ETH3 DC-	ETH3 DC+	GND
7	COM1 RXD/RXD+	GND	DVI HPD	NC	GND	NC	NC
8	GND	DVI TMDS1-	DVI TMDS1+	GND	DVI TMDS2-	DVI TMDS2+	GND
9	NC	GND	DVI CLK-	DVI CLK+	GND	DVI TMDS0-	DVI TMDS0+
10	GND	PCIe1 CLK-	PCIe1 CLK+	GND	DVI SDA	DVI SCL	GND
11	COM2 TXD/ COM1 TXD-	GND	PCIe1 TX-	PCIe1 TX+	GND	PCIe1 RX-	PCIe1 RX+
12	GND	XMCIO_SE3	XMCIO_SE1	GND	XMCIO_SE4	XMCIO_SE2	GND
13	NC	GND	XMCIO_DP1-	XMCIO_DP1+	GND	XMCIO_DP2-	XMCIO_DP2+
14	GND	XMCIO_DP3-	XMCIO_DP3+	GND	XMCIO_DP4-	XMCIO_DP4+	GND
15	COM2 RXD/ COM1 RXD-	GND	XMCIO_DP5-	XMCIO_DP5+	GND	XMCIO_DP6-	XMCIO_DP6+
16	GND	XMCIO_DP7-	XMCIO_DP7+	GND	XMCIO_DP8-	XMCIO_DP8+	GND
CASE	GND						

* signal active when low

Table 35: VPX Connector P2 Wafer Assignment

P2 Signal Definition

MNEMONIC	SIGNAL DEFINITION
COMx	Serial Lines, EIA-232/EIA-485
USB PWR	USB Power
USBx D+/-	Differential Data pair of USB link x
SATAx RX+/-	Serial ATA. Receive +/- link x
SATAx TX+/-	Serial ATA. Transmit +/- link x
PCIe1 TX/RX	Additional PCI-Express x1 link
PCIe1 CLK	Common Reference Clock Output for PCIe1
GND	Ground
XMCIO_SE1-4	Single ended XMC I/O 1,2,3 and 4 according to VITA 46.9 X38s
XMCIO_DP1-8	Differential pairs XMC I/O 1 to 8 according to VITA 46.8 X8d
DVI	DVI Port

Table 36: VPX Connector P2 Signal Definition

4.4 LEDs

4.4.1 Status LEDs Default Setting

There are five bicolor LEDs (Red/Green) on the front panel of the VX305x-SA 3U VPX board.

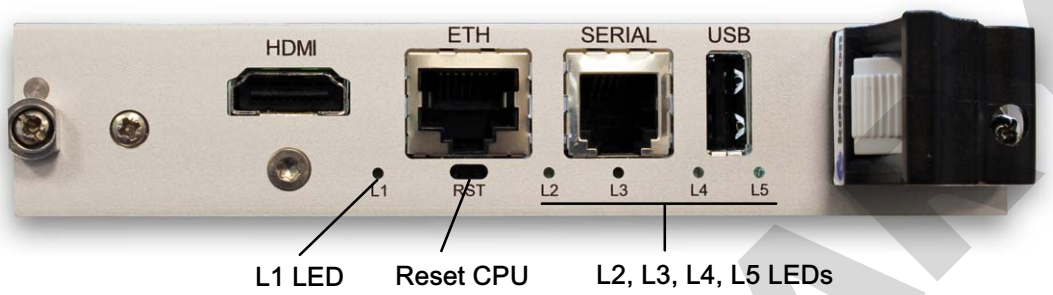


Figure 26: LEDs Front panel

4.4.2 LEDs Activity

CPU LED	DESCRIPTION
○	LED OFF
●	Red LED
●	Green LED
●	Orange LED
✸	Red blinking LED
✸	Green Blinking LED
✸	Orange blinking LED
Not Blink	Indicates that the corresponding LED gives an additional information if any LED is blinking at the same time

Table 37: LEDs Description

The following table describes the informations that the LED can report:

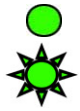
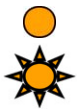
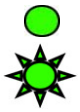
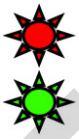
L1	L2	L3	L4	L5	Meaning
	Not Blink	Not Blink	Not Blink	Not Blink	Permanent system error. Internal VX305x-SA power is off. In this state L2, L3, L4 and L5 do not carry the meaning described in this table but an error code detailed in the **POWER ERRORS** table.
					At least one of the LANSW interfaces link up At least one linked at 1000BASE-T Blinking when activity on the links
					At least one of the LANSW interfaces link up. No linked at 1000BASE-T Blinking when activity on the links
					100BASE-TX/1000BASE-T interfaces are down
					PEX FATAL Error detected
					10G Ethernet controller link up. Blinking when activity on the link
					10G Ethernet controller off
					Internal power supplies are ON and board reset is asserted.
					Internal power supplies are ON and board reset de-asserted (normal operation).
					Internal power supplies are ON but PROCPWRGD_PCH not activated
					**Fast** blinking RED (reset asserted) or GREEN (reset de-asserted) when activity to/from backplane I2C/SMBus **Slow** blinking GREEN (1Hz, 50% duty cycle) when internal power supplies are OFF (board in standby)
					Normal operation
					Factory test mode
					CPLD Watchdog expired
					**Off blinking when M2 activity on Slot 2**
					Processor hot event (PROCHOT), supersedes 10G Ethernet routing information
					ETH1 **and** ETH2 LANSW links directed on front connector
					At least one of ETH1 or ETH2 LANSW link directed on VPX connector
					**Off blinking when M2 activity on Slot 1**

Table 38: LEDs Activity

L1	L2	L3	L4	L5	Power Good Errors
●	○	○	○	○	PWRGD_VPX
●	○	○	○	●	VPXPWRGD_UV
●	○	○	●	○	VPXPWRGD_OV
●	○	○	●	●	PWRGD_VR5V0
●	○	●	○	○	PWRGD_VCCSCFUSESUS
●	○	●	○	●	PWRGD_VCCKRHV
●	○	●	●	○	PWRGD_VR1V5_PCH
●	○	●	●	●	PWRGD_VR1V05
●	●	○	○	○	PWRGD_VR2V5_DDR4
●	●	○	○	●	PWRGD_VR1V2
●	●	○	●	○	PWRGD_VTT
●	●	○	●	●	PWRGD_FET1V05
●	●	●	○	○	PWRGD_VRPEX
●	●	●	○	●	PWRGD_VR3V3
●	●	●	●	○	PWRGD_VRVCCIN
●	○	○	◐	◐	WAKE UP ERROR
●	○	○	○	◐	PROCPWRGD ERROR
●	●	●	●	●	More than one Error

L1	L2	L3	L4	L5	LPC CLOCK Errors
●	◐	◐	○	○	LPC Clock 48 MHz (Legacy value is 33 MHz)
●	○	○	◐	◐	LPC Clock 25 MHz

L1	L2	L3	L4	L5	Critical Errors
●	●	●	●	✸	PECI_CRIT#
●	●	●	✸	●	CATERR#
●	●	✸	●	●	VR1V05_VRHOT#
●	✸	●	●	●	VRVCCIN_VRHOT#
✸	●	●	●	●	THERMTRIP#

Chapter 5 - Power and Thermal Specifications

5.1 Power Specifications

All frequency / power data are measured with Intel Performance Tuning Utility tool (PTU) for Xeon-D processors.

Fedora Kontron BSP running TAT 100% all cores, standard glxgears test, and memory, FFT, SATA, LPC, FRAM benchmarks.

Connected peripherals: 2x SATA, USB keyboard/mouse, Front HDMI interface for display, rear 10G/PCIe links, Dual bank DDR4-2133 memory configuration.

5.1.1 VX3052 and VX3058 Thermal Power

The following data show total board consumption for different processor configuration and Thermal Design Power. These data help for thermal power dissipation analysis.

All power values in this table are measured in operational conditions on early field Xeon-D parts.

VX3058 Thermal Power: board power based on current measurements

	Power Mode	CPU Power Measured	Max Total Power Consumption	Test Condition
VX3058 Xeon-D @ 1.6 Ghz	Turbo On Max Processor power, TDP 35W	TBD	TBD	LinuxOS, TAT 100% all cores, maximum junction temperature, DDR, FFT, SATA, LPC, FRAM, glx-gears tests 2x SATA, USB keyboard/mouse, rear links Dual bank DDR4-2133 memory configuration
	Turbo Off Max Processor power, TDP 25W@2.1Ghz	TBD	TBD	
	Linux idle Linux «on demand» mode Processor frequency 1.2 GHz	TBD	TBD	

VX3052 Thermal Power: board power based on current measurements

	Power Mode	CPU Power Measured	Max Total Power Consumption	Test Condition
VX3052 Xeon-D @ TBD				LinuxOS, TAT 100% all cores, 100°C maximum temperature, DDR, FFT, SATA, LPC, FRAM, glx-gears tests 2x SATA, USB keyboard/mouse, Front DisplayPort interface for display, rear links Dual bank DDR4-2133 memory configuration
	Linux idle Linux «on demand» mode Processor frequency 0.8 GHz			

Board	Power Mode	Workload	Total Power Consumption	Current Drawn	Test Condition
VX3052, VX3058			+0.4W	100 mA/ 3V3aux	If 3V3aux is present and main 5V and 12V power supplies not present. Board is in stand-by mode.
Additionnal USB power consumption on 5V USB devices dependant, max 500mA/port			+12.5W	2.5A /5V (12.5W)	**Note**: this thermal power is not dissipated on board
Additionnal XMC(*) daughter card consumption XMC(*) dependant			+7.5W but XMC(*) dependant	7.5W on 3V3 and/or 5V/12V	**Note**: this thermal power is dissipated on XMC(*)

(*) XMC slot option is on demand only

Table 39: VX305x-SA Power Consumption

5.1.2 VX3052, VX3058 Maximum Current

The following data provide maximum current values on VPX VS1(12V) power supplies. These maximum includes 1.25x max TDP reached during turbo boost HFM, VS1 +5% tolerance and 5% margin to guarantee worst case part behavior.

VX3058 Maximum Current: based on maximum current measurements				
	Power Mode	CPU Power Measured	VS1 (12V) max current	Test Condition
VX3058 Xeon-D @ TBDGHz	Turbo On Max Processor power, TDP 35W Including +25% TDP for short duration time	35W (42W during 1.25xTDP)		

VX3052 Maximum Current: based on maximum current measurements				
	Power Mode	CPU Power Measured	VS1 (12V) max current	Test Condition
VX3052 xeon-D @ TBD GHz				

Table 40: VX305x-SA Maximum Current

5.2 Board Thermal Monitoring

To ensure long-term reliability of the VX305x-SA, onboard components must not operate beyond their specified maximum temperature. The most critical component on the VX305x-SA is the processor. Operating the VX305x-SA above the maximum operating limits will result in permanent damage to the board.

The VX305x-SA includes a temperature sensor (NCT7802Y by Nuvoton) managed by the CPLD through I2C. Refer to Figure 17 “I2C Diagram” page 31.

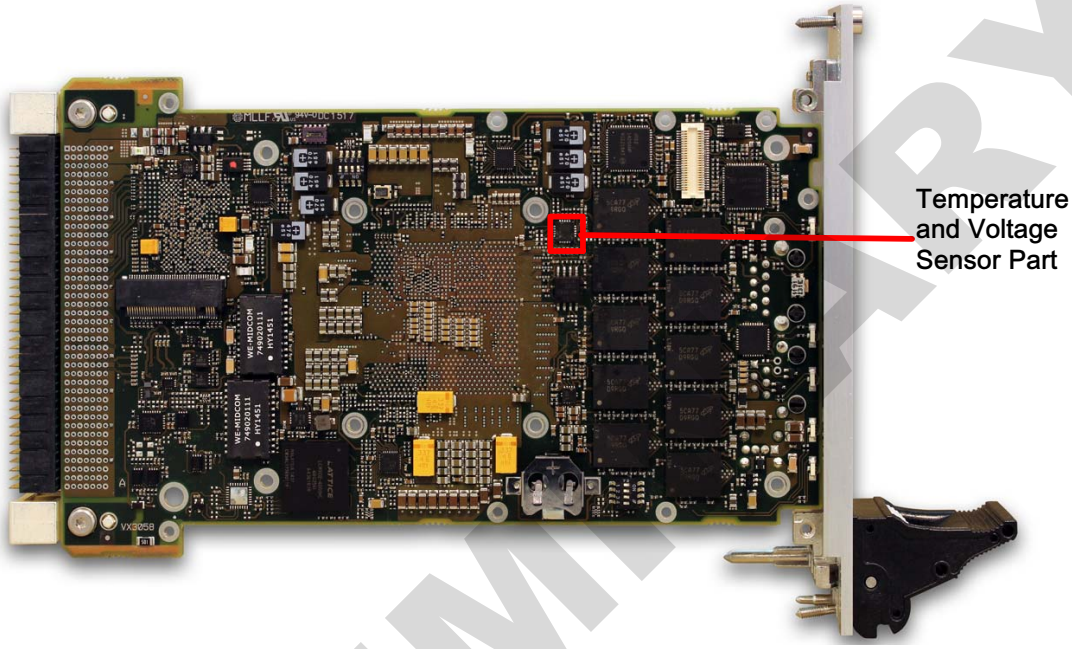


Figure 27: Temperature Sensor Location

In addition to monitoring several internal power supplies, the NCT7802Y supports one on-die temperature sensor and can also get the processor temperature directly via the Intel® PECI3.0 interface. The NCT7802Y temperature and voltages monitoring data may be viewed with the Linux "sensors" command.

The NCT7802Y has 3 alarm outputs connected to the CPLD:

- ALERT#: logged in CPLD to generate a maskable interrupt. The high threshold is set to +85°C by BIOS. The low threshold is set to -45°C but may be modified by the BIOS UEFI command `VX305x-SA> kpld -i2cw 2 36 1 <value>`. The low threshold may also be used as the lower threshold for high temperature hysteresis.
- T_CRIT#: logged in CPLD reg @0x74, leads to fatal error with all internal PSUs power supplies being switched off and the error status is being displayed on the front panel LEDs. The T_CRIT# threshold is set to +95°C by BIOS.
- RESET#: not used by CPLD

NCT7802Y Key specifications:

- Voltage monitoring accuracy +-10mV
- Temperature Sensor Accuracy
  - On-chip Temperature Sensor Accuracy (25~70°C) +- 2°C typ.
  - On-chip Temperature Sensor Resolution 1 °C
- Operating Temperature Range -40°C ~ 85°C

5.3 CPU Thermal Monitoring

All thermal data in the following tables are initial measurements on available Xeon-D processor silicons. These data applies to standard VPX 3U 1" slot profile.

See VX305x-SA Thermal design guide for more information.

CPU Temperature

For a given required air-flow and processor TDP (Thermal Design Power), the following curves show the maximum authorized operating temperature, not to exceed the maximum specified junction temperature of the processor.

For Xeon-D processors, maximum case temperature (TcMAX) depends on processor part number.

These curves help also to choose customer operating points for a given 1 inch slot environment.

The TJMAX temperature is the temperature not to exceed, to avoid entering the throttling mode.

To ease Xeon D temperature measurements and make sure that processor temperature is within Intel specifications, Intel provide maximum Tcase temperatures (measured at the geometric center of the top surface of the intergated heatspreader). Tcase maximum temperature should not exceed 88°C.

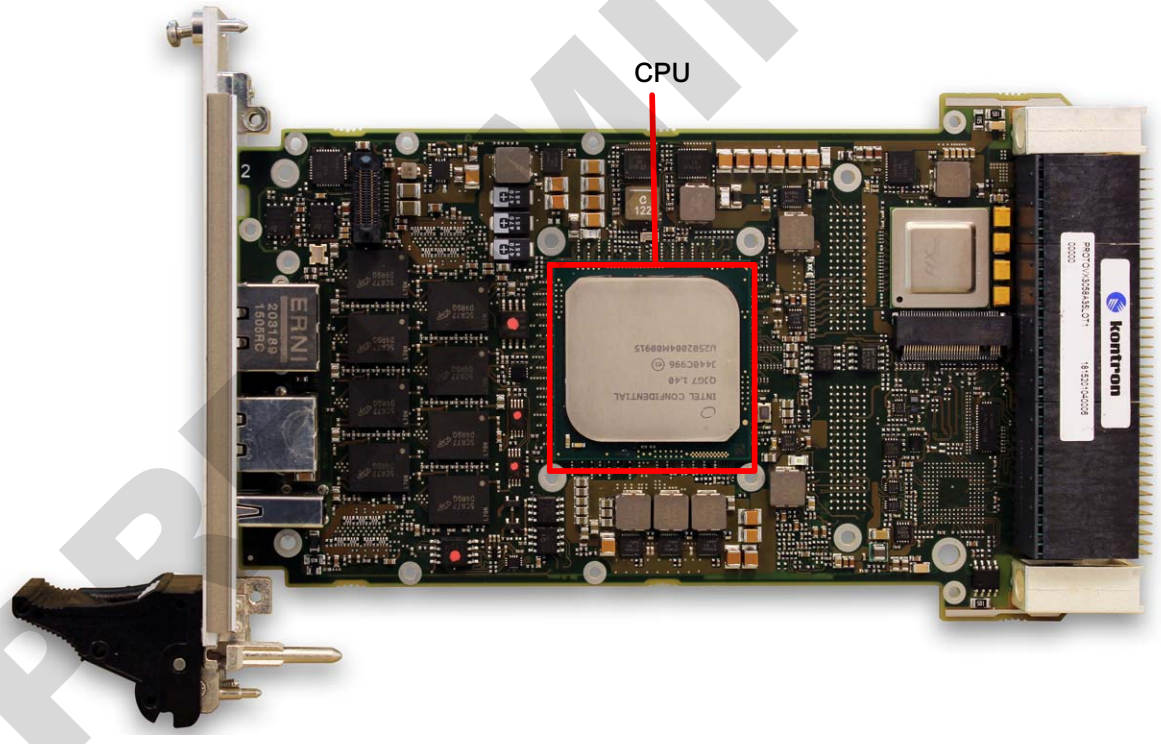


Figure 28: CPU Location

Intel Thermal Analysis Tool (TAT) has been used to force processor TDP or characterization.

All Thermal Design Power (TDP) were measured with Intel Thermal Analysis Tool (TAT) software.

> Standard VX305x-SA heat sink without XMC slot option.

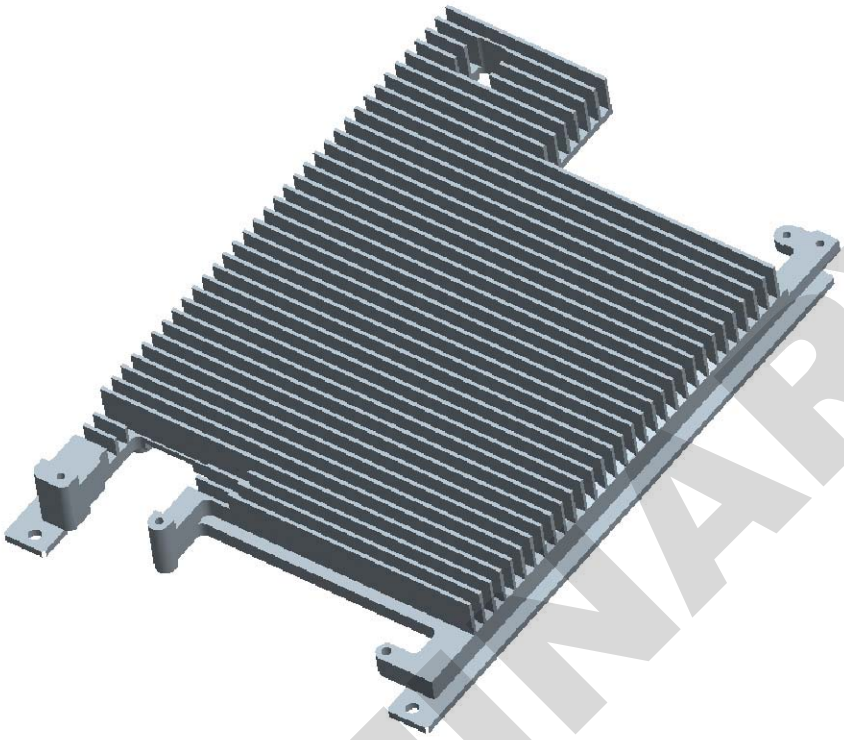


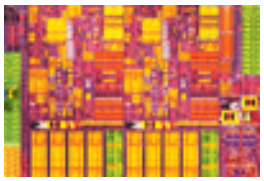
Figure 29: VX305x-SA Heat Sink

VX305x-SA Functional points synthesis (see also curves below):

Heat sink type	Board	Processor TDP	Tjmax All cores	Ambient Tempe-rature	Min Airflow	Calculated Input Air Speed for 1" input section (25.4 mm x 160 mm)	

Table 41: VX305x-SA Functional Points Synthesis

Intel® Turbo Boost Technology



Intel® Turbo Boost Technology is one of the many exciting features that Intel has built into latest-generation Intel® microarchitecture. It automatically allows processor cores to run faster than the base operating frequency if it's operating below power, current, and temperature specification limits.

Dynamically increasing performance

Intel Turbo Boost Technology 2.0 is activated when the Operating System (OS) requests the highest processor performance state (P0).

The maximum frequency of Intel Turbo Boost Technology 2.0 is dependent on the number of active cores. The amount of time the processor spends in the Intel Turbo Boost Technology 2.0 state depends on the workload and operating environment.

Any of the following can set the upper limit of Intel Turbo Boost Technology 2.0 on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency will dynamically increase until the upper limit of frequency is reached. Intel Turbo Boost Technology 2.0 has multiple algorithms operating in parallel to manage current, power, and temperature to maximize performance and energy efficiency.

Intel Turbo Boost Technology 2.0 allows the processor to operate at a power level that is higher than its rated upper power limit (TDP) for short durations to maximize performance.

Learn more about Intel Turbo Boost Technology: http://www.intel.com/technology/turboboost/

- The Intel Turbo Boost is handled by the BIOS through the CPU configuration menu.

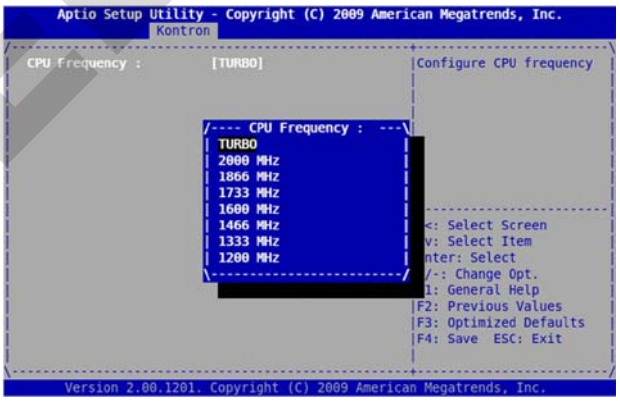


Figure 30: Intel Turbo Boost Technology - CPU Configuration Menu

Refer to the AMI BIOS for VX305x-SA

Chapter 6 - Backplane Suggestions

Kontron can offer for development or deployement of the VX305x-SA the following backplane models:

» Single Star x4, 8 Slots

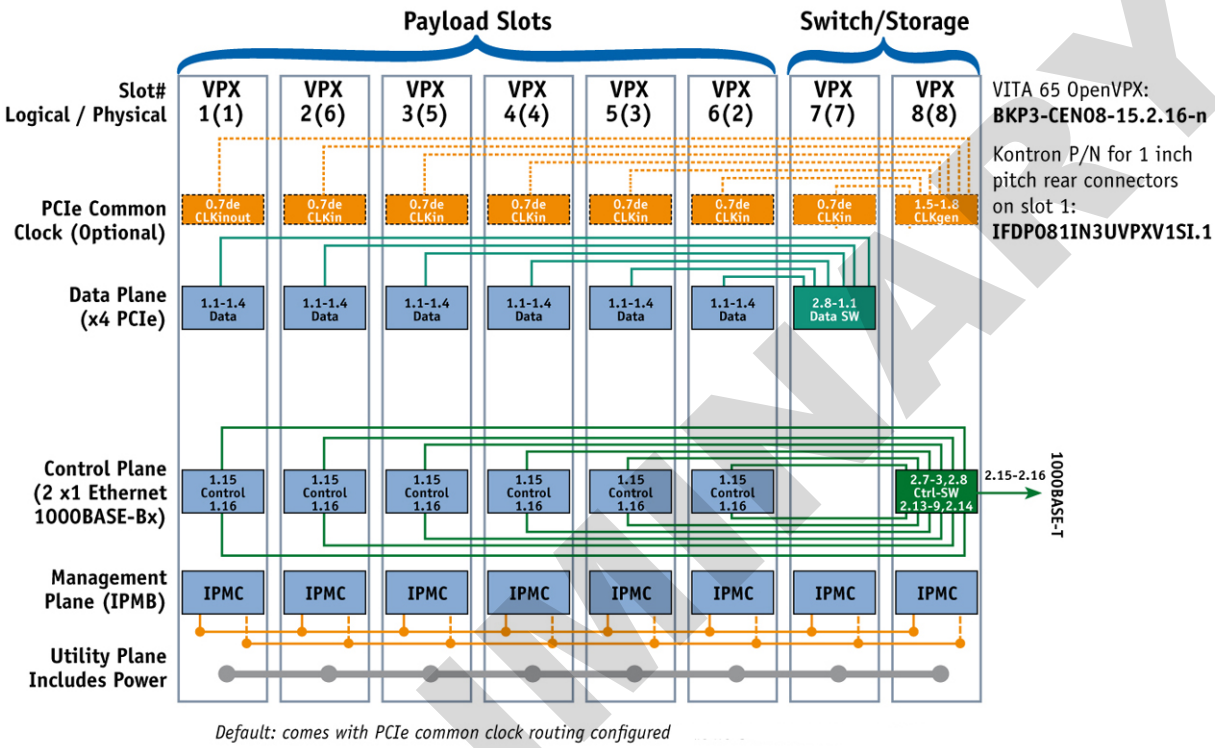


Figure 31: Single Star x4, 8 SlotsTopology

Single Star x4, 5 Slots

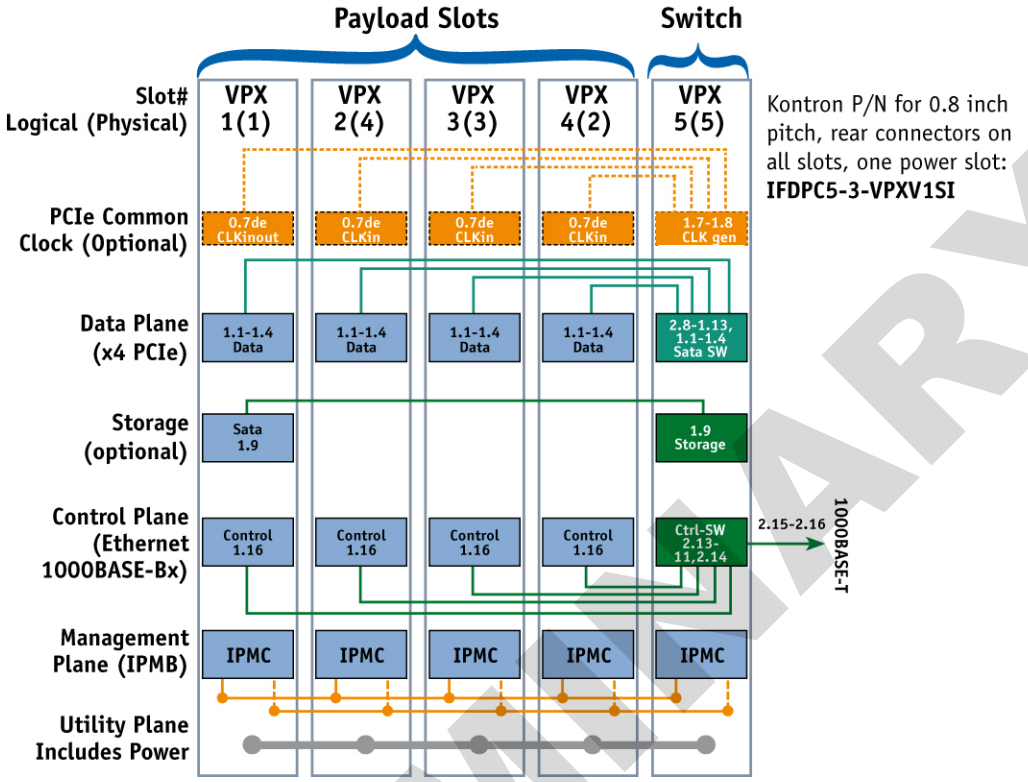


Figure 32: Single Star x4, 5 Slots Topology

Distributed, 2 Slots

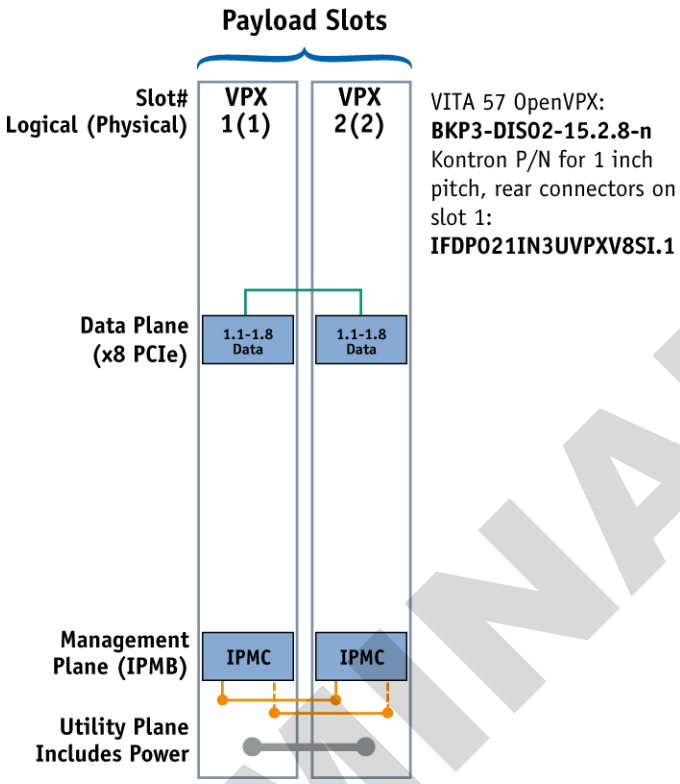


Figure 33: Distributed, 2 Slots Topology

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