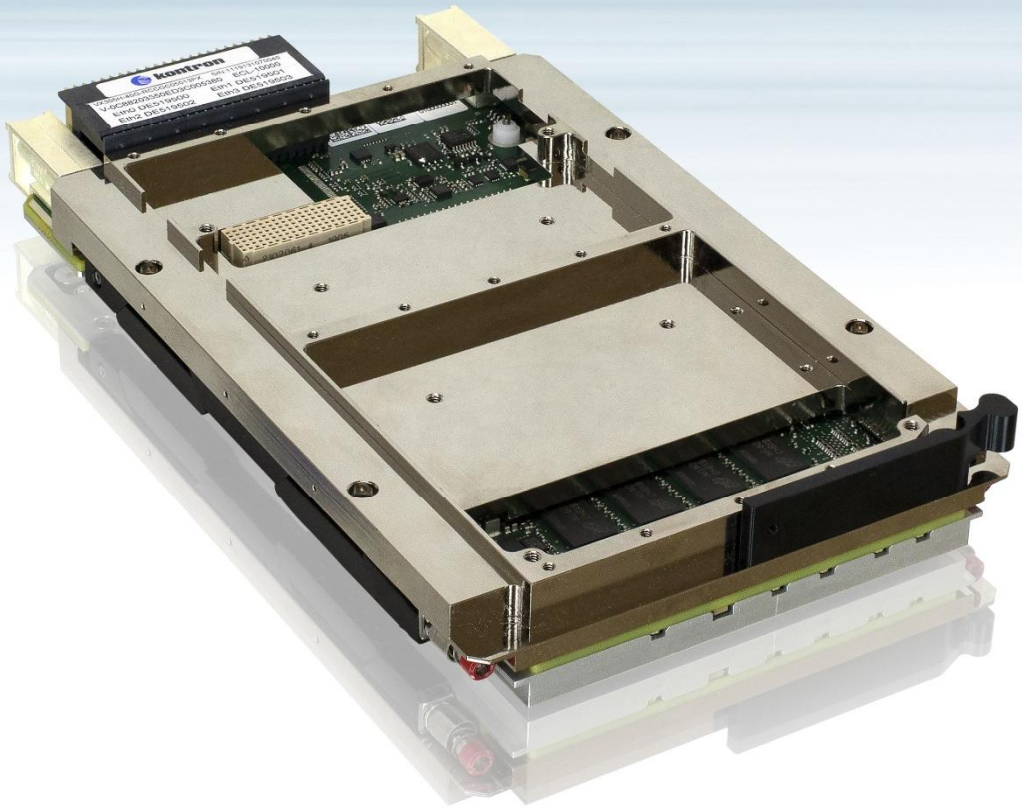
USER'S GUIDE



VX305H-40G

3U VPX Computing Node

D219797-1.0 - July 2019

VX305H-40G - User's Guide

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Revision History

Publication Title:	VX305H-40G User's Guide	
Doc. ID:	D219797	
Revision	Brief Description of Changes	Date of Issue
1.0	Early Field Trial version.	07-2019

Customer Support

Please contact our support team at support.KFR@kontron.com

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Customer Comments

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Symbols

The following symbols may be used in this user guide

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
NOTICE	NOTICE indicates a property damage message.
	**Electric Shock!** This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	**ESD Sensitive Device!** This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	**HOT Surface!** Do NOT touch! Allow to cool before servicing.
	**Laser!** This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol indicates important information which must be read carefully.

This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!

Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed

on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

General Instructions on Usage

In order to maintain Kontron's product warranty and CE compliance, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty and CE compliance.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Environmental protection is a high priority with Kontron.
Kontron follows the WEEE directive
You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

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1/ Introduction

The Kontron VX305H-40G is a 3U VPX computing blade for data and signal processing application focusing on application domains such as Military & Aerospace, Transportation and Energy/Industry.

The Kontron VPX blade VX305H-40G is the ideal building block for intensive parallel computing workloads where a cluster of Kontron VX305H-40G can be used in switched OpenVPX environments.

The VX305H-40G board comes with EFI BIOS and supports Linux. It is covered by Kontron's long term supply program, which guarantees customers multi-year supply of the product beyond its active life.

Featuring the 12 core version of the Intel® Xeon® D processor family (formerly Broadwell-DE) and developed in alignment with the SOSA™ technical standard, the VX305H-40G is a compute intensive SBC compliant with the VITA 65 (OpenVPX) slot profile SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-n.

The VX305H-40G combines server-class processing with a 40 Gigabit Ethernet Data Plane and an extra-wide 8-lane PCI Express® Gen3 Expansion Plane. The VX305H-40G also features an XMC site for non-volatile storage or other expansion options not requiring rear-panel I/O. The result is a powerful, flexible, single board computing platform suitable for a wide range of embedded applications.

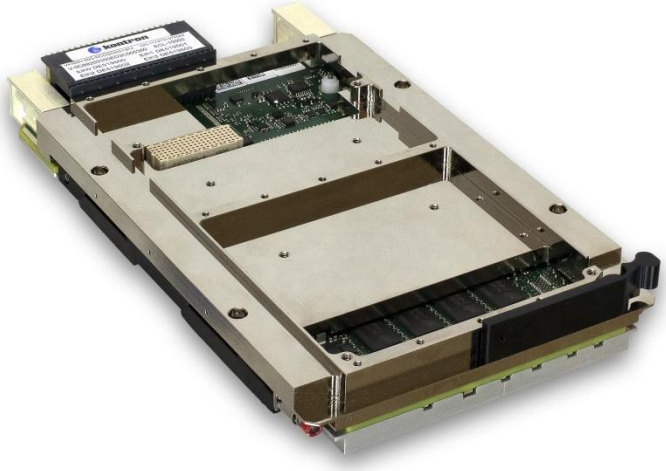
The highly integrated 12-core architecture with Dual 10 Gigabit Ethernet, high bandwidth PCI Express 3.0, high speed DDR4 memory, and versatile mezzanine options, is consequently SWaP-C optimized and simply the best choice for high performance embedded computing platforms.

The M.2 bottom slots can be used for storage modules.

The VX305H-40G features a VITA 46.11 compatible Intelligent Platform Management Controller (IPMC) for centralized system health management.

The high-performance VX305H-40G server blade is available as Conduction-cooled Plug-in units according to VITA 48.2 Type 2, Secondary Side Retainer. The VX305H-40G is also available with the VITA 48.2 Type 1 Ruggedized Enhanced Design Implementation (REDI) Two-Level Maintenance bottom cover option.

Figure 1: VX305H-40G 3U VPX Overview



1.1. Manual Overview

1.1.1. Objective

This guide provides general information, hardware instructions, operating instructions and functional description of the VX305H-40G-RC board. The onboard programming, onboard firmware and other software (e.g. drivers and BSPs) are described in detail in separate guides (see section 1.7 "Related Publications").

This hardware technical documentation reflects the most recent version of the product. The “Release Notes" (see section 1.7"Related Publications") might help to keep track of potential evolutions.

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

1.1.2. Audience

This guide is written to cover, as far as possible the range of people who will handle or use the VX305H-40G-SA, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, system, cabling, grounding and communications.

1.1.3. Scope

This guide describes RC variants of the VX305H-40G series.

1.1.4. Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- Chapter 1 - Introduction (this chapter)
- Chapter 2 - Installation
- Chapter 3 - Additional Board Features
- Chapter 4 - Physical I/O
- Chapter 5 - Power and Thermal Specifications
- Chapter 6 – Optional Board Features
- Chapter 7 – RTM Characteristics
- Chapter 8 – Standard Air-cooled (SA) Characteristics

1.1.5. Terminology, Definitions and Abbreviations

In this document, the term:

- VX305H-40G-yy will be associated to the 3U VPX board family:
  - yy: RC environment class as defined by Kontron standards (see product environmental specifications in this document and product Release Notes)

As an example, VX305C-40G-RC means 12-core product specified for RC environmental class.

Abbreviations

TBD	To Be Defined. Information not available at the time this document was released.
TDP	Thermal Design Power
PTU	Power Thermal Utility

1.2. VPX Overview

VPX (VITA 46) specifications establish a new direction for the next revolution in bus boards. VPX is an ANSI standard which breaks out from the traditional connector scheme of VMEbus to merge the latest in connector and packaging technology with the latest in bus and serial fabric technology. VPX combines best-in-class technologies to assure a very long technology cycle similar to that of the original VMEbus solutions. Traditional parallel VMEbus will continue to be supported by VPX through bridging schemes that assure a solid migration pathway.

For further information regarding this standards and its use, visit the home page of the VITA - Open Standards, Open Markets (http://www.vita.com)

1.3. Board Overview

1.3.1. Main Features

Intel® Xeon® Architecture

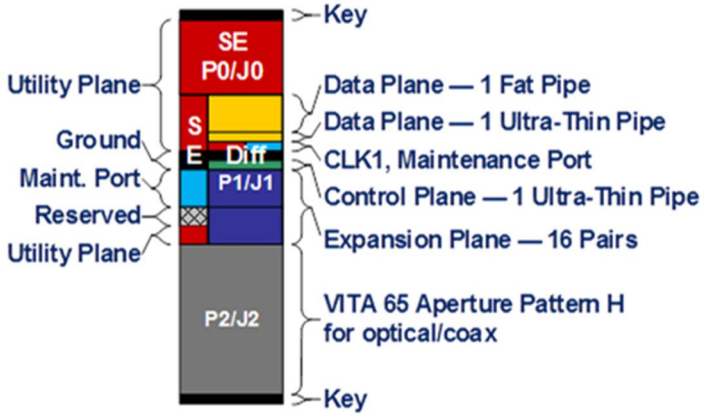
The VX305H-40G computing node is a VPX computing blade for parallel data and signal processing application. The VX305H-40G is the ideal building block for intensive parallel computing workloads where a cluster of VX305H-40Gs is used in full mesh or switched OpenVPX environments. Target applications include radar, sonar, imaging systems, airborne fighters, and unmanned aerial vehicle (UAV) radar, as well as rugged multi-display consoles. It is also well suited for transport applications.

The processing node of the VX305H-40G implements a Xeon® Processor D coupled with dual channel DDR4 memory. The highly integrated Intel® QM77 platform hub provides numerous Ethernet, SATA and PCIe channels. The 3U-format VX305H-40G described in this document is the standard conduction cooled model.

Frequency of the CPU: see Table 1 - Order Codes

However, the Xeon® Processor D is equipped with the Turbo Boost technology, which allows increasing the frequency when the total on chip power allows it.

TECHNICAL SPECIFICATIONS	
Processor	Fifth Generation Intel® Xeon® D-1500 Processor Family, DDR4 dual channel memory with ECC, 2133 MT/s over 144 bits, up to 32 Gbytes Integrated dual 10G Ethernet controller PCIe gen3 to VPX (x8 port) and XMC (x8 port), up to 8 GT/s
Integrated Platform Controller Hub	PCI Express* Base Specification, Revision 2.0 support for up to eight ports with transfers up to 5 GT/s Integrated Serial ATA host controllers with independent DMA operation on up to six ports Two Integrated serial lines

TECHNICAL SPECIFICATIONS	
Onboard Controller	
Gigabit Ethernet	One XL710 40Gbit Ethernet controller connected on VPX backplane for 40GBASE-KR4 operation
Watchdog	PLD-based, timeout ranging from 4 ms to 510s, IRQ, Reset, dual-stages
RTC	Separated low power RTC
System cPLD	Power - on/ off control, Reset control, Local environmental control/monitoring, I2C interfaces to I2C bus IPMB A/B (rear P0), LEDs control, Serial lines multiplexer, Serial VPD and user memories, User and system GPIOs, Internal registers that allow system management
IPMC	FRU subsystem management: Local environmental control/monitoring, IPMB A/B interfaces, FRU memory, system event log
Memory	
System Memory	Up to 32 GB dual channel DDR4 SDRAM running at 2133 MT/s, with ECC, soldered
Flash (uEFI BIOS)	2x16 MB FLASH, with recovery image and uEFI BIOS settings
EEPROM	One serial 256 Kbit EEPROM dedicated to system data One serial 256 Kbit EEPROM dedicated to application data
M.2 SSD option	M.2 SSD module option: Type M, 22 mm x 42 mm
Front Interfaces 5HP (1")	
LEDs	5 LEDs reporting the board CPU health status and activity
Reset	Reset push button
Onboard Interfaces	
M.2 module interface	Bottom M.2 slot for SSD module. Supported module: Type M, 22 mm x 42 mm.
XMC Slot	One x8 PCIe Gen 3 for XMC slot. No XMC IO available;
VPX Interface	
Slot Profiles	SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-n 

TECHNICAL SPECIFICATIONS	
Rear I/O via P1	Data Plane : 40GBASE-KR4 as per IEEE802.3 clause 82 on P1 10GBASE-KR as per IEEE802.3 clause 72 or 1000BASE-KX as per IEEE802.3 clause 70 on VPX P1 (auto negotiation) Expansion plane : x8 PCIe 3.0 on P1. Software configurable as 2 x4 PCIe 3.0. Refer to BIOS IIO configuration submenu in IntelRCSetup menu. Control Plane : 10GBASE-KR as per IEEE802.3 clause 72 or 1000BASE-KX as per IEEE802.3 clause 70 on VPX P1 (auto negotiation) Single-Ended: Maintenance port (Rx,Tx), GPIO (maskable reset),
Supervisory Functions	Non Maskable RESET NVMRO, Master SMBus and Master/Slave SMBus interfaces for system management. Compatible with Kontron CMB (Monitoring Board), temperature and voltage sensors on the board
Power Supplies	On P0: VS1=12V; VS2 not used; VS3=5V not used; 3.3V_AUX, -12V_AUX for XMC slot
OS Support	Linux, ask for: Windows, VxWorks
Mechnical size	3U x 160 mm, Slot pitch: 1.00 inch according VITA 48.1 (air cooled) and VITA 48.2 (conduction cooled)

All the Flash and non volatile memories onboard have a write protect mechanism taking into account the NVMRO (Non Volatile Memory read Only) VPX signal. For further details, see section 3.7 Write Protect Mode

Software

Kontron is one of the few compact PCI, VME and VPX vendors providing in-house support for most of the industry-proven real-time operating systems that are currently available.

Thanks to its close relationship with the software editors, Kontron is able to locally produce and support BIOS, BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology which follow silicon evolution.

Finally, Kontron offers to its customers owners of a maintenance agreement a hotline software support and regular software updates.

A dedicated web site is also available for online updates and release downloads.

The VX305H-40G is delivered with the UEFI BIOS from AMI which supports Secure Boot and TPM. This BIOS supports PBIT Expert mode option from Kontron CMON-Line

The VX305H-40G supports a live Linux distribution for instant evaluation and benchmarking. Based on Fedora Linux, it offers many turn-key features, such as Continuous BIT service (CBIT). Refer to our Kontron VME/VPX Fedora 28 Remix Release Notes for details.

Contact Kontron for further information regarding other operating systems and software support.

Rear Transition Module

The VX305H-40G supports the PB-VX3-40G-H-601, a 3U VPX Rear Transition Module compliant with the definition of the Rear Transition Module on VPX standard - VITA 46.10.

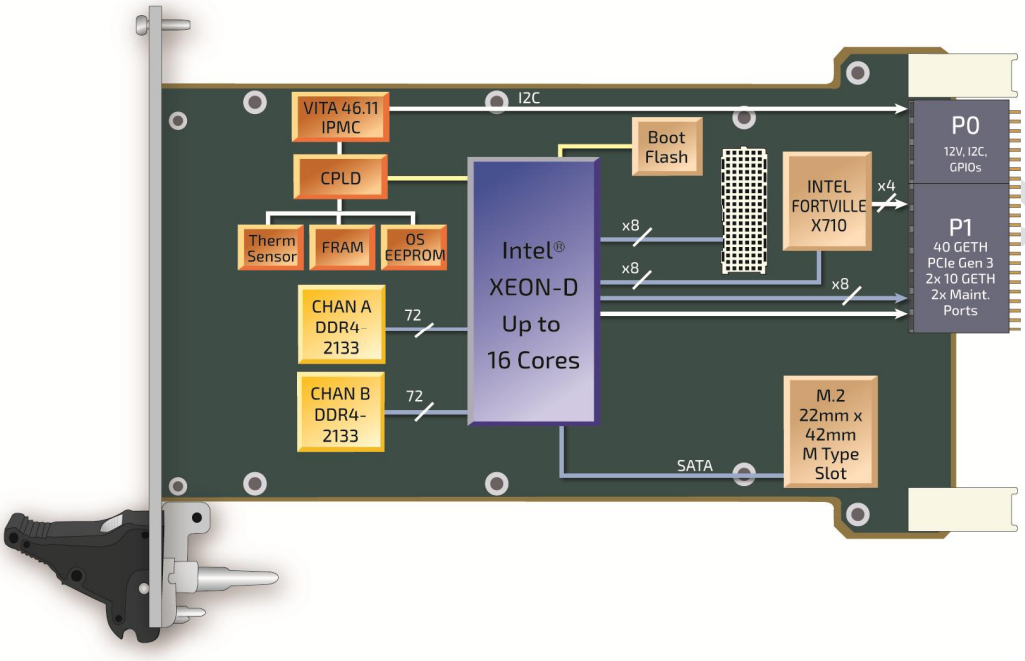
It offers connectivity on the rear for:

- two serial maintenance ports

For further detail about the RTM, refer to section 7/RTM Characteristics, page 79.

1.3.2. Block Diagram

Figure 2: VX305H-40G Block Diagram



1.3.3. Ordering Information

Manufacturing Options

- Processor Type: See Table 1 - Order Codes
- Processor TDP: Up to 45 W
- DDR4 SDRAM Size: 16GB to 32GB
- 22 mmx42 mm M.2 SATA slots: support 2242-S1-M, 2242-S2-M, 2242-S3-M, 2242-D1-M, 2242-D2-M, 2242-D3-M, 2242-D4-M, SATA link up to 6 Gb/s.
- Security Solution: TPM and Approtect
- I/O Features: See Table 1 - Order Codes
- Ruggedization Levels: RC, labs
- Slot pitch: 1 inch

Available Order Codes

Table 1: VX305H-40G Order Codes

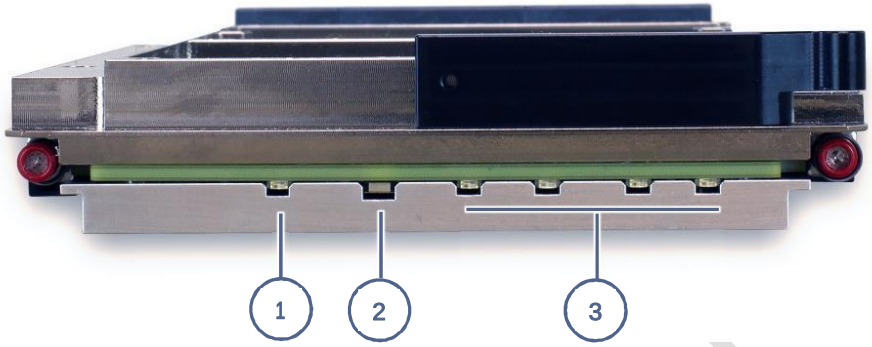
Environ-mental Class	Standard Order Codes	Description
RC	VX305H-40G-RC nmC05y1sz	3U single slot 5 HP (1.0") VPX CPU Blade with Intel® Xeon® D-1500 processor series, conduction cooled, Vita48.2 plug-in type: Type 1, secondary side retainer, 2 Level Maintenance Available options: Processor type: n=8: 8-Core D1539, base frequency 1.6 GHz, TDP 35 W n=C: 12-Core D-1559, frequency 1.5 GHz, TDP 45 W Memory size: m = F: 16 GB dual bank DDR4 m = G: 32 GB dual bank DDR4 I/O feature option: y = 0: Base I/O y = 1: additional P2 VPX connector Security option: s = 0 : no hardware secure element s = 3 : hardware secure element equipped (TPM and Approtect) Other option: z = P : with PBIT z = Q : with PBIT and Eval Linux on SSD
SA	VX305H-40G-SA nmC05y1sz	3U single slot 5 HP (1.0") VPX CPU Blade with Intel® Xeon® D-1500 processor series, Air cooled 10 °C to +30 °C Available options: Processor type: n=8: 8-Core D1539, base frequency 1.6 GHz, TDP 35 W n=C: 12-Core D-1559, frequency 1.5 GHz, TDP 45 W Memory size: m = F: 16 GB dual bank DDR4 m = G: 32 GB dual bank DDR4 I/O feature option: y = 0: Base I/O y = 1: additional P2 VPX connector Security option: s = 0 : no hardware secure element s = 3 : hardware secure element equipped (TPM and Approtect) Other option: z = P : with PBIT z = Q : with PBIT and Eval Linux on SSD

Refer also to the product datasheet for the available order code list.

1.3.4. I/O Interfaces

Front Interfaces

Figure 3: VX305H-40G Front Panel I/O Interfaces



1. L1 LED
2. Reset CPU
3. L2, L3, L4, L5 LEDS

Table 2: Front I/O Interfaces

FUNCTION	DESCRIPTION	SEE ALSO
Reset	Reset push button	Figure 3
LEDs	5 LEDs reporting the board CPU health status and activity	Section 4.3 for LEDs Description

Rear Interfaces

Rear interfaces are compliant with the following slot profiles:

- SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11

Figure 4: VX305H-40G Rear I/O Distribution

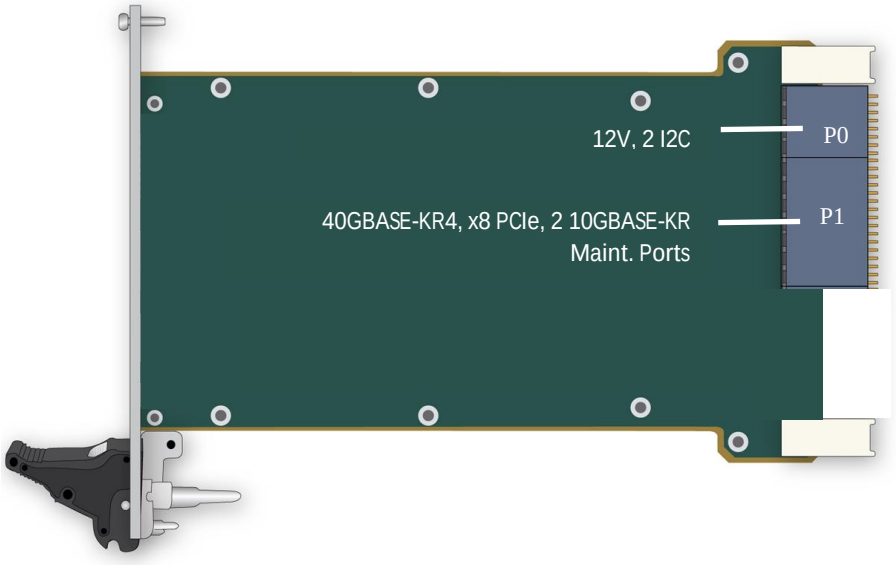
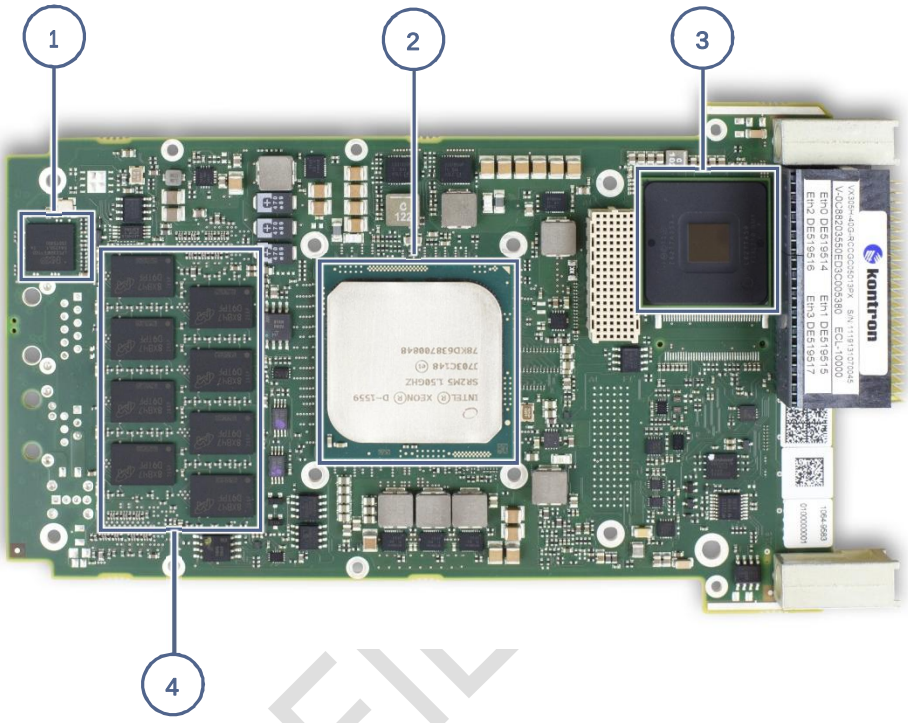


Table 3: Rear I/O Interfaces

FUNCTION	DESCRIPTION	SEE ALSO
PCI Express	1 x8 gen3 PCIe on P1. Can be split into two ports of four lanes, refer to BIOS IIO configuration submenu in IntelRCSetup menu.	Section 4.2 for VPX Connectors Description
Gigabit Ethernet	1 SerDes 40GBASE-KR4 on P1 2 SerDes 10GBASE-KR or 1000BASE-KX on P1 (auto negotiation)	
Serial	2 asynchronous EIA-232 RX/TX maintenance ports, on P1	
GPIOs	1 User GPIOs on P1, including MASKABLE RESET	
Utilities	On P0 and P1: SYSRESET, SYSCON, 6 Geographical Addresses	
I2C	IMPB-A/B I2C busses as per VITA 46.11	
Clocks	On P0: 25 MHz Refclock, 1 PPS Auxclock On P1: 100 MHz radial clock (enable using BIOS configuration menu)	
Power Supplies	VS1=12V; VS2 not used; VS3=5V not used +12V_AUX is optional in VITA 46 and not connected on VX305H-40G. -12V_AUX is optional in VITA 46. It is not used internally on VX305H-40G except for the XMC 3.3V_AUX is mandatory in VITA 46. However, if absent, it will be generated internally.	

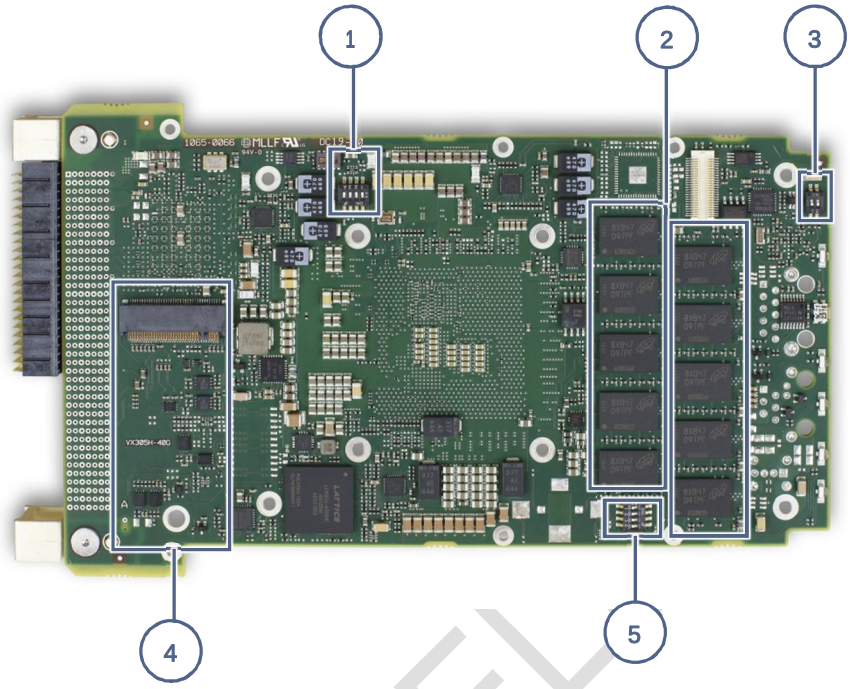
1.3.5. Components Layout

Figure 5: VX305H-40G Components Layout (Top view)



1. IPMC microcontroller
2. Intel Xeon D
3. 40G XL710
4. DDR4-SDRAM

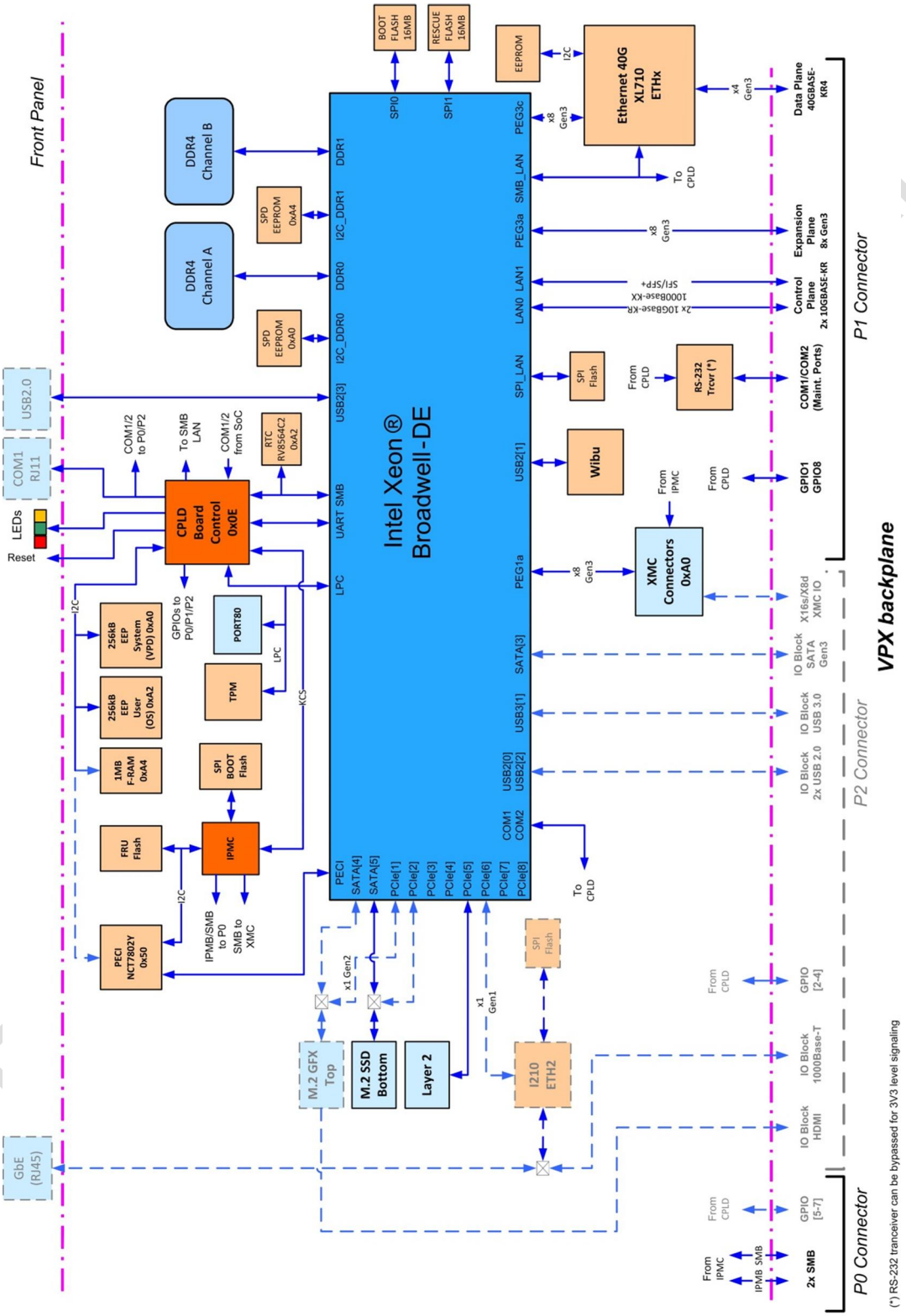
Figure 6: VX305H-40G Components Layout (Bottom view)



1. MicroSwitchSW2
2. DDR4 SDRAM
3. MicroSwitchSW3
4. Bottom M.2 Slot
5. MicroSwitchSW1

1.3.6. Technical Specification

Figure 7: VX305H-40G Functional Block Diagram



1.3.7. M2 Module List

Table 4: Non-exhaustive M.2 module list, tested on VX305H-40G M.2 slots

Module Type	Capacity	Memory Technology	Manufacturer	Part Number
SSD SATA, Type M	60 GB	MLC	Innodisk	DEM24-64GM41BW1DC
SSD SATA, Type M	60 GB	iMLC	Virtium	VSFBM4XI060GB
SSD SATA, Type M	30 GB	iMLC	Virtium	VSFBM4XI030G-F15

1.4. Environmental Specifications

Table 5: VX305H-40G-RC Environmental Specifications

RC - Rugged Conduction (1" single height passive module heat frame)	
Plug-in unit type according VITA48.2	Type 1, secondary side retainers, 2 Level Maintenance
Conformal Coating	Standard
Airflow	NA
Cooling Method	Conduction
Operating	12-core Xeon-D1559 w/o XMC: -40 °C to +70 °C [1] 12-core Xeon-D1559 w/ 7.5-15W XMC: -40 °C to +55 °C[1]
Storage	-50 °C to +100 °C
Vibration (Operating)	Product withstand vibration as defined below, 1 hour per axis: ▸ 5 Hz to 100 Hz PSD increasing at 3 dB/octave ▸ 100 Hz to 1000 Hz PSD = 0.1 g2/Hz ▸ 1000 Hz to 2000 Hz PSD decreasing at 6 dB/octave
Shock (Operating)	40 g / 11 ms peak accel./shock duration half sine
Altitude (Operating)	-1,500 to 60,000 ft
Relative Humidity	95 % non-condensing

[1] Maximum temperature measured at card edge in the following conditions: full processor performance, maximum processor TDP without CPU throttling.

Table 6: VX305H-40G Lab-grade Environmental Specifications

Lab-grade air-cooled version (1" single height passive module heat sink, forced air)	
Conformal Coating	optional
Airflow	Refer to chapter 8.7
Cooling Method	Convection
Operating	10 °C to +30 °C

1.5. Board Weight

Table 7: VX305H-40G Weights

VX305H-40G Weights	
VX305H-40G-RC w/o XMC modules	≈ 800 g
VX305H-40G lab w/o XMC modules	≈ 500 g

1.6. MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

VX305H-40G-RCCGC05013P MTBF Data

Table 8: VX305H-40G-RCCGC05013P MTBF Data

MTBF	MILHDBK217F					
	GB (HOURS)		NS (HOURS)		ARW (HOURS)	AIC (HOURS)
	25 °C	40 °C	25 °C	40 °C	55 °C	40 °C
VX305H-40G-RCCGC05013P	tbd	tbd	tbd	tbd	tbd	tbd

1.7. Related Publications

The following publications contain information relating to this product:

Table 9: Related Publications

PRODUCT	PUBLICATION	
Standard		
ANSI/VITA 46.0	VPX Baseline Standard - ANSI/VITA 46.0-2007 [R2013]	
ANSI/VITA 46.6	Gigabit Ethernet Control Plane on VPX, Feb 2013	
ANSI/VITA 46.9	XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules, Nov 2010	
ANSI/VITA 46.10	Rear Transition Module for VPX - ANSI/VITA 46.10-2009	
ANSI/VITA 46.11	System Management on VPX, June 2015	
ANSI/VITA 65	OpenVPX™ System Specification ANSI/VITA 65-2010 [R2012]	
ANSI/VITA 48.2	Mechanical Specifications for Microcomputers using REDI Conduction Cooling Applied to VITA VPX	
Serial ATA	Serial ATA 1.0a Specification	
Hardware		
VX305H-40G Boards	VX305H-40G Hardware Release Notes	D219738
Firmware		
VX305H-40G Boards	AMI-BIOS User Reference Manual	D213792
VX305x Boards	PBIT User's Guide	SD.DT.G51
Software		
VX305H-40G Boards	Kontron VME/VPX Fedora 28 Remix Release Notes	D215295

2/ Installation

The VX305H-40G has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

2.1. Safety Requirements

The following safety precautions must be observed when installing or operating the VX305H-40G. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Special care shall be taken while handling the board: the heat sink or heat frame can get very hot during operation. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container before the board and heat sink have cooled down to room temperature

This board contains electrostatically sensitive devices. Observe the necessary precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

- Do not touch components, connector pins or traces.
- We strongly recommend our customers to work in an environment equipped with anti-static workbenches with professional discharging equipments

2.2. Board Identification

The VX305H-40G boards are identified by labels fitted to the top side and on the bottom side of the board.

The E.C. Level format is "xxxxxLy" where

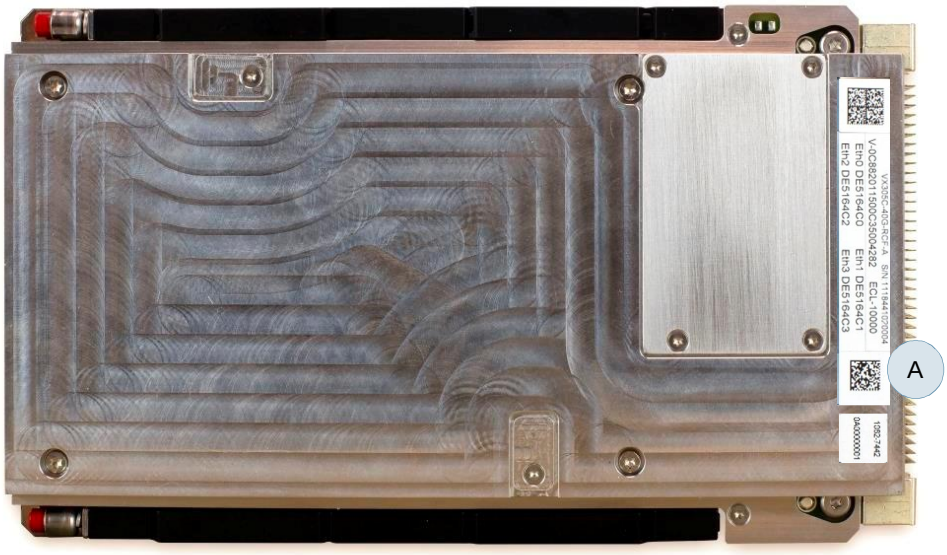
- The five digits "xxxxx" indicate the board E.C. Level (PCB revision included)
- "Ly" indicates the mechanical E.C. Level:
  - letter "L" varies with the environment class ("A" for SA, "B" for WA, "C" for RA and "D" for RC)
  - digit "y" gives the mechanical E.C. Level.

Top Side

A "Identification" label: Order Code, Serial Number, Variant, E.C. Level
Ethernet MAC addresses

Figure 8: VX305H-40G Identification (Top Side)

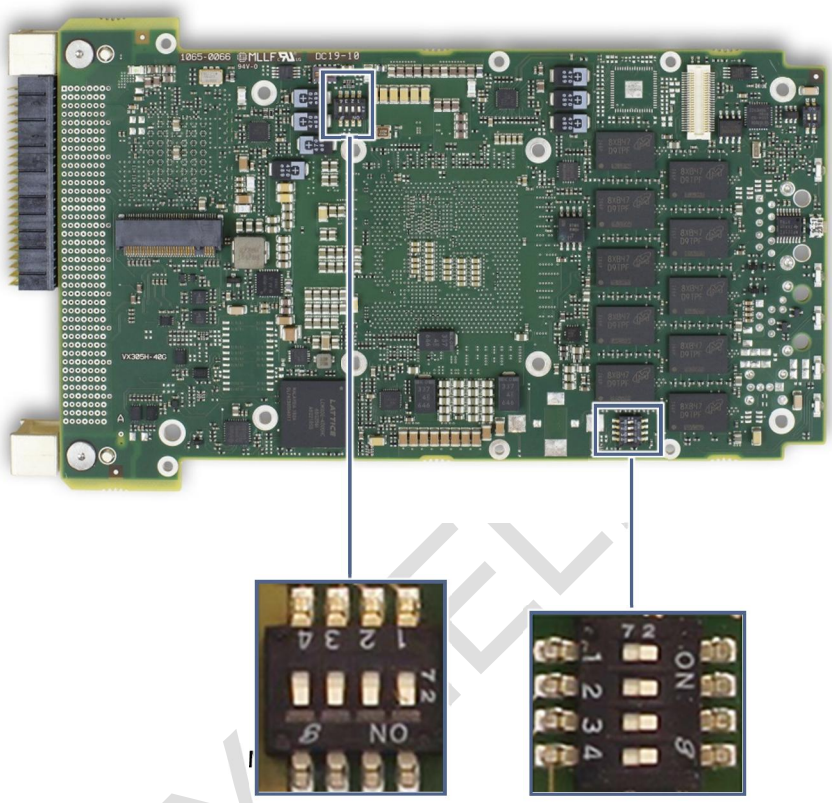
Figure 9: VX305H-40G Identification (Bottom Side)



2.3. Board Configuration

2.3.1. Microswitches

Figure 10: VX305H-40G Board Configuration (Bottom view)



Two microswitches are available on the VX305H-40G: SW1 and SW2.

Microswitch SW3, shown in Figure 6, is not accessible by default, it is used for test and debug purpose only.

2.3.2. SW1 Microswitch Description

Table 10: SW1 Microswitch Description

FUNCTION	DESCRIPTION
1 - Factory Mode	off: Normal Mode on: Factory Mode
2 - Debug Mode	off: Normal Mode on: Debug Mode
3 - VPD level Write Protection	off: Non volatile memory at VPD level Write protected on: Writes are allowed on memory at VPD level
4 - User level Write Protection	off: Writes are allowed on memory at User level on: Non volatile memory at User level write protected

See also section 3.7 "Write Protect Mode", page 47, for write protection level description and for knowing the protected devices.

2.3.3. SW2 Microswitch Description

Table 11: SW2 Microswitch Description

FUNCTION	DESCRIPTION
1 - System Boot Flash	off: Normal Mode on: Rescue Mode
2 - BIOS Failsafe	off: Normal Mode on: BIOS Failsafe Mode
3 - NVMRO	off: Normal Mode (Hi-z state) on: NVMRO signal force to low state (dessasserted)
4 - Force PROCHOT	off: Standard Mode on: Processor PROCHOT force to low state

In rescue mode, the BIOS boot time is significantly increased up to about 1 minute and 40 seconds instead about 20s

2.4. Package Content

The VX305H-40G is packaged with several components. The packing contents of the VX305H-40G Series may vary depending on the ordering code and on the customer requests.

- CPU Module:
  - Order Code: see section 1.3.3 “Order Code Table” :
    - Processor specifications differ depending on Order Code.
    - XMC cover assembled on the board.
    - Bolt accessories for mezzanine mounting (XMC and bottom M2 module).
    - Graphics M2 module.
    - SSD M2 module.
- Rear Transition Module:
  - Order Code: PB-VX3-40G-H-6xx.
- Serial Cable:
  - Order Code: KIT-2X-RJ12DB9 (1057-3995)

Figure 11: Serial Cable

2.5. Initial Installation Procedures

The following procedures are applicable only for the initial installation of the VX305H-40G in a system. Procedures for standard removal operations are found in their respective chapters.

To perform an initial installation of the VX305H-40G in a system proceeds as follows:

1. Ensure that the safety requirements indicated in section 2.1 page 30 are observed.

⚠CAUTION Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the VX305H-40G see section 2.3. For the installation of VX305H-40G, specific peripheral devices and Rear I/O devices refer to the appropriate sections in current Chapter.

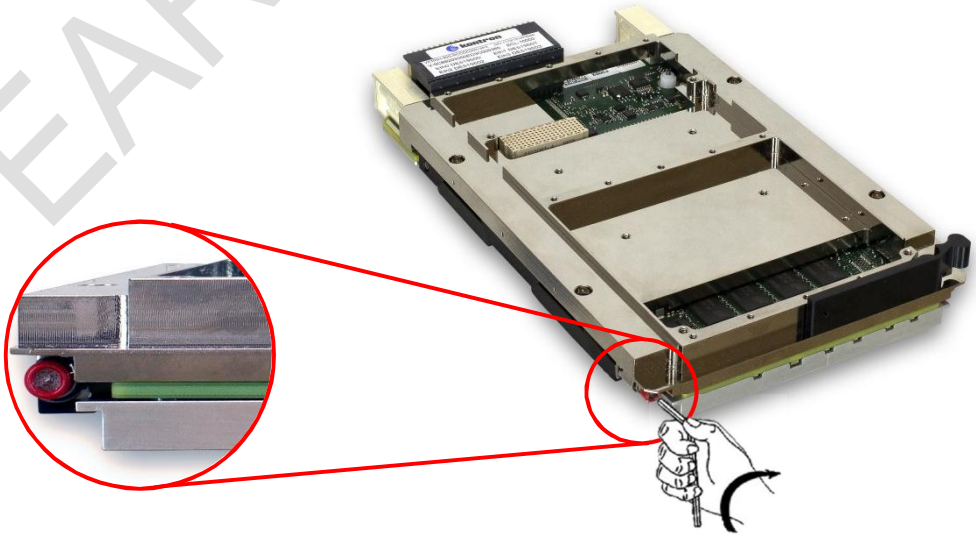
⚠CAUTION Care must be taken when applying the procedures below to ensure that neither the VX305H-40G nor other system boards are physically damaged by the application of these procedures.

3. To install the VX305H-40G-RC, perform the following:
   a. Ensure that no power is applied to the system before proceeding.
   b. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.

i When performing the next step and when the chassis accommodating the board is compliant with VITA48.2, it is recommended to use the ejector handles to seat the board into the backplane connectors. For the other chassis, simply push the board into the backplane connectors.

   c. Engage the board with the backplane using the ejector handle. When the ejector handle is against the heat frame, the board is engaged.
   d. Tight the wedgelocks to the cold plate. A torque of 0.8 N.m must be applied to the wedgelock screw (Calmark serie 265)

Figure 12: VX305H-40G-RC Board Insertion - Wedgelock Screw Location



⚠CAUTION Running the board at high temperature without tightening the wedgelocks to the cold plate may result in permanent damage to the board.

e. Ensure that the board is properly secured.

The VX305H-40G is now ready for operation. For operation of the VX305H-40G, refer to appropriate VX305H-40G specific software, application, and system documentation.

2.6. Standard Removal Procedure

ESD sensitive Device! Precautions are listed in chapter 2.1

To remove the board from the chassis proceeds as follows:

1. Ensure that the safety requirements indicated in Section 2.1 are observed. Particular attention must be paid to the warning regarding the heat frame.

⚠CAUTION Care must be taken when applying the procedures below to ensure that neither the VX305H-40G nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.

3. To remove VX305H-40G-RC, loosen the card locks to the cold plate.

4. Disengage the board from the backplane using the board ejection handle, press the handle until the board is disengaged.

5. After disengaging the board from the backplane, pull the board out of the slot.

Due care should be exercised when handling the board due to the fact that the heat frame can get very hot. Do not touch the heat frame when changing the board.

6. Dispose of the board as required.

2.7. XMC Module Insertion / Removal Instructions

Supported XMC type

The default XMC connectors are VITA 61 XMC 2.0 compliant and support x8 PCI-Express 3.0 interface.
The XMC stack is 12 mm.

XMC installation

ESD sensitive Device! Precautions are listed in chapter 2.1

Apply "Loctite 222e" threadlock on each screw during re-assembling.

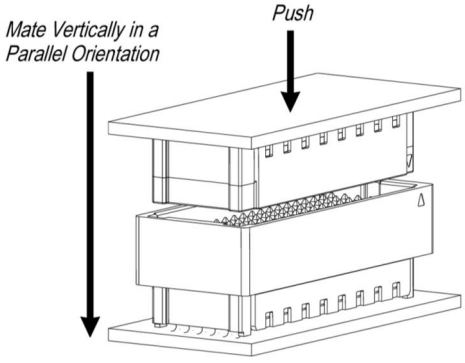
To install a XMC, proceed as follows:

1. Turn off power
2. Remove the XMC cover if it is mounted on the heat frame. Throw nylon washers. For details, see the Figure 14b.
3. Align the XMC connectors. Press to fully engage the XMC.

⚠CAUTION

The XMC connectors should be mated straight: Align the connectors and when the keys start to enter the keyways, push at the approximate center of the connector into the mating connector until the face of the receptacle cover bottoms on the face of the plug. Because of the asymmetric keying, reverse mating is impossible (the key end of the receptacle cannot be inserted into the non-keyway end of the plug). Both connectors have a lead-in around the perimeter that will allow blind mating..

Figure 13: XMC Module Insertion



4. Screw the XMC in place using the height mounting points and screw the XMC cover using nine mounting points. See Figure 14a and Figure 14b for details.

Figure 14: XMC and XMC cover Installation

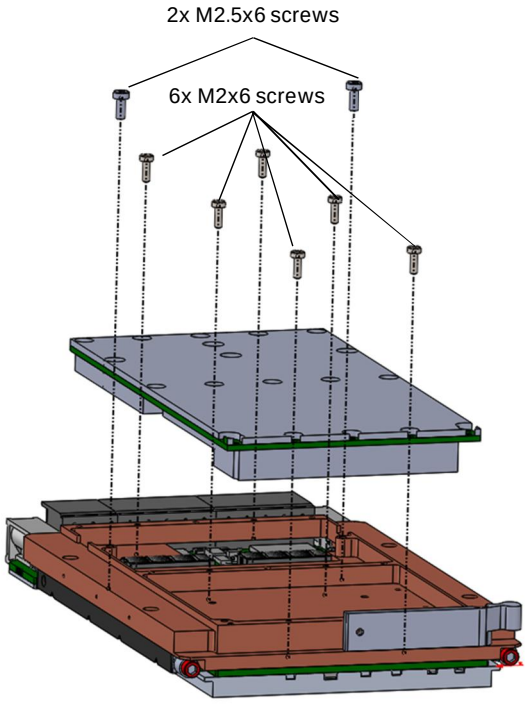


Figure 14a

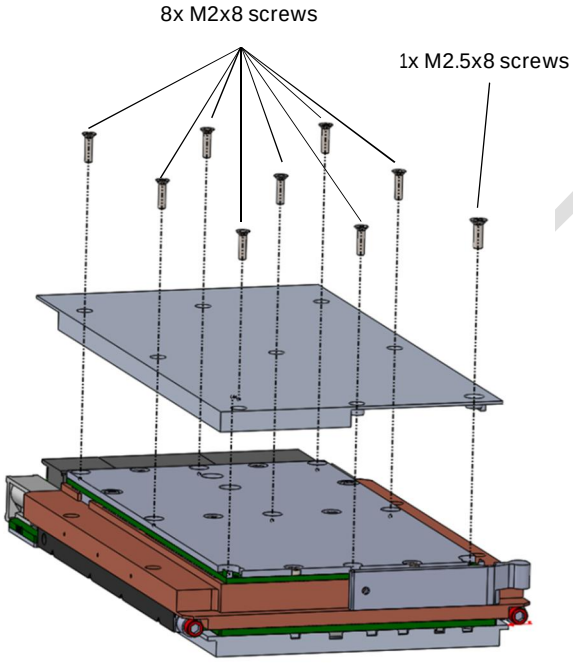
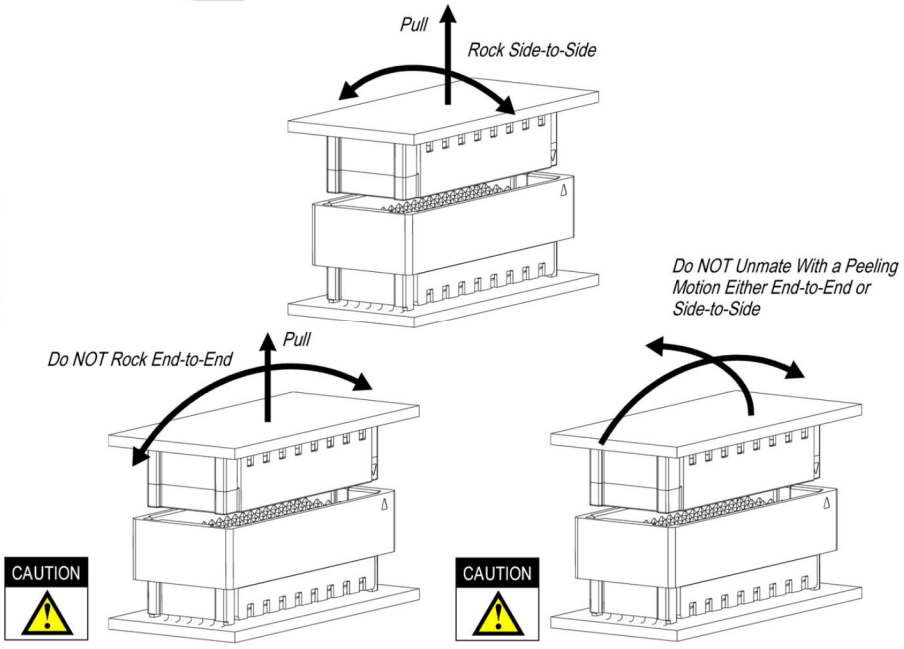


Figure 14b

Unmating

The XMC connectors can be unmated by pulling them straight apart or by “rocking” the connectors from side-to-side while pulling them apart.

Figure 15: XMC Module Removal



2.8. M.2 Module Insertion / Removal Instructions

Supported M.2 Module Type

The M.2 bottom socket is compliant with SATA III interface. The socket can host the following module types: 2242-XX-M with XX = S1, S2, S3, D1, D2, D3, D4.

The M.2 bottom socket is not compliant with D5 form factor.

M.2 Module Insertion Process

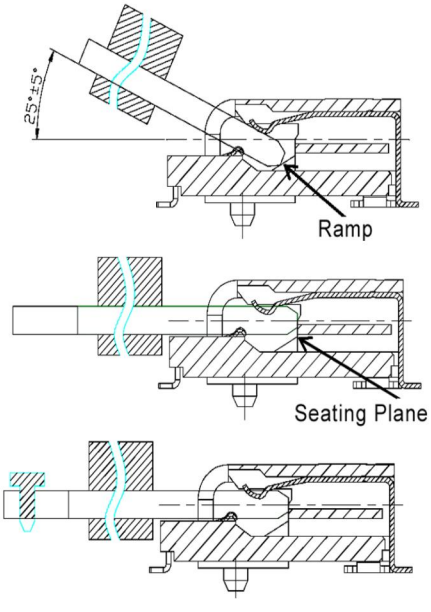
ESD sensitive Device! Precautions are listed in chapter 2.1

Apply "Loctite 222e" threadlock on each screw during re-assembling.

1. Disassemble the bottom M.2 cover by unscrewing 4 screws (M2x4 with Torx). Remove flat washer and hexagon thin nut. See Figure 18.

Figure 16: M.2 Module Insertion Process

2. Insert the module with angle 25°±5° until module touch HSG ramp.



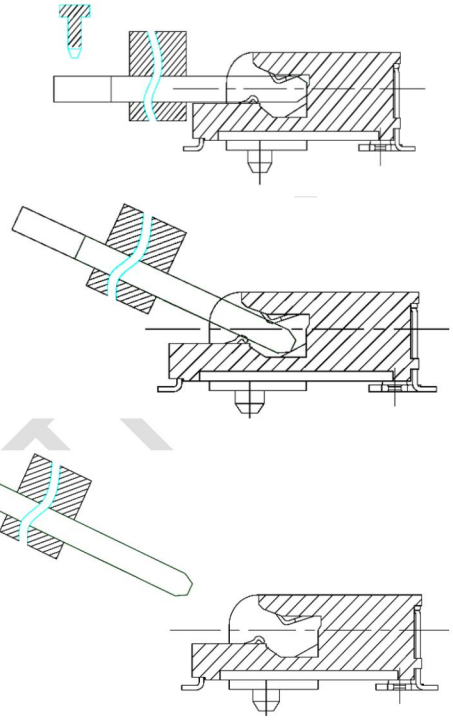
3. Rotate the module to horizon by hand and make sure the card's edge touch HSG seating plane.

4. Fix the module with PCB by nut by hand.

M.2 Module Removal Process

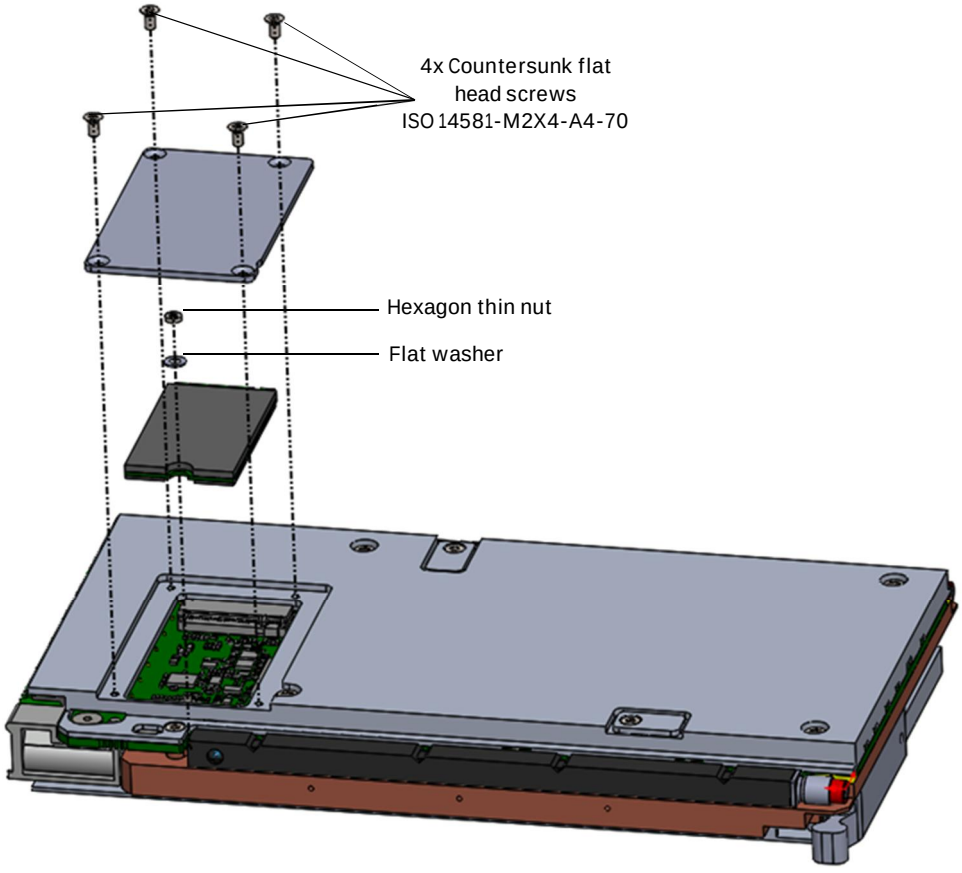
Figure 17: M.2 Module Removal Process

1. Loosen the screw by hand and the module will be rotated automatically due to connector contact's counterforce at the same time.



2. Take away the module by hand.

Figure 18: Bottom M.2 Module Insertion



2.9. Software Installation

The installation of all onboard peripheral drivers is described in detail in the relevant Driver Kit files or Board Support Packages (BSP).

The installation of an operating system is dependent of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.

3/ Additional Board Features

3.1. RTC, Watchdog, Timers

3.1.1. Real-Time Clock (RTC)

Two Real Time Clocks (RTC) are available on the VX305H-40G: one is embedded in the PCH while the other is a standalone, high-precision, low-power component located on the integrated PCH SMBus (RV8564 by Micro Crystal).

Standby power supplied to the RV8564 RTC

When the VX305H-40G is powered off, the RTC is powered through the 3.3V_AUX rail or the VBAT rail on the VPX backplane.

To ensure data retention in the RV8564 RTC, VBAT must be set in the range [2.5V - 5.5V]. The maximum current drawn over the -40 °C/+85 °C temperature range is 500 nA (VBAT= 3 V, no I2C activity) or 550 nA (VBAT=5 V, no I2C activity).

Internal Integrated PCH RTC

The integrated PCH RTC module provides a date and time keeping device with two banks of static RAM with 128 bytes each. The BIOS programs the RTC interrupt on Legacy IRQ8 that is never shared with other interrupts. It is clocked by an external 32.768 KHz oscillator with a parabolic coefficient of 0.4 ppm/°C² and a stability of +/-20 ppm at 25 °C. A 20 ppm stability is equivalent to a 10 mn/year drift.

Standalone low-power RTC RV8564

The RV8564C2/B RTC by Micro Crystal features an internal oscillator, date and time keeping module with programmable alarm, timer and interrupt functions. It has an ultra low-power consumption in time keeping mode: 250 nA, typical and 500 nA, maximum. Its stability is 20 ppm at 25 °C. It is connected to the integrated PCH SMBus

RTC management by BIOS and OS

At each startup, the BIOS retrieves the date and time information from the high-precision RV8564 RTC and copies it into the integrated PCH RTC.

Any update of date and time in the BIOS settings will be done both in integrated PCH RTC and RV8564 RTC.

Regarding the RTC management by the OS, the OS should use the high-precision RV8564 RTC driver. Failing to do so, the updates will be done only in integrated PCH RTC and will not be saved.

If no power is applied on the RV8564 RTC, the BIOS displays the BIOS build date and time instead of the current date and time.

Century flag

For compatibility reasons, the BIOS implements the century flag for the high-precision RTC as follows:

- Century Flag C = 0 for 1900-1999 years
- Century Flag C = 1 for 2000-2099 years.

The user should check that the OS driver implements the same convention.

3.1.2. CPLD Watchdog

In addition to the standard watchdog timer included in the integrated PCH, the cPLD implements a hardware watchdog timer that can be used by the operating software to monitor the normal operation of the system.

It is enabled by software, and once enabled must be restarted at regular intervals. If not, its expiration sets off an interrupt (IRQ) to the local processor, a board reset or a board power-cycle.

The watchdog has the following features:

- timeout programmable from 1 to 511 clock periods, by steps of 2 periods
- clock periods of 1s or 1ms
- lock bit: when set, can only refresh (restart) the watchdog, but not change its settings
- 4 modes: timer, reset, interrupt or power-cycle
- restart counter: can manage the remaining number of resets or power-cycles done by the watchdog before giving-up.

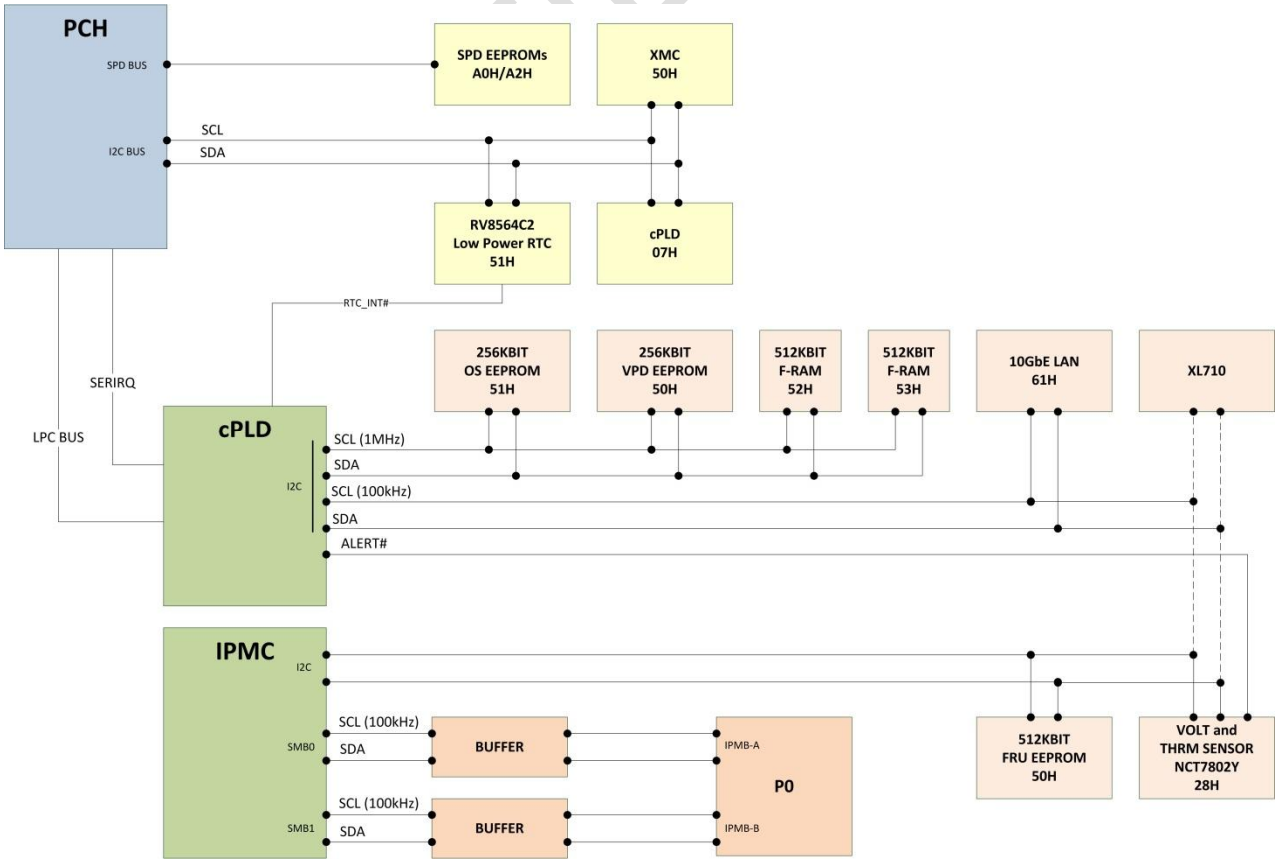
3.2. I2C Structure

The VX305H-40G features several I2C busses.

- Two are attached to the integrated Platform Hub Controller and control the DDR4 SPD EEPROM and the low-power RTC.
- The other are handled by the CPLD device and by the IPMC device according to Figure 19: I2C Diagram.

The I2C addresses shown are 8 bit values which include a read/write bit. Shift one bit to the right to get the 7-bit addresses.

Figure 19: I2C Diagram



PCH SMBus (100 KHz)

SLAVE DEVICES ON SOC SMBUS INTERFACE	SMBUS 7-BIT BASE ADDRESS (8-BIT BASE ADDRESS)	FEATURES
cPLD	07H (0EH)	System cPLD
RV8564C2	51H (A2H)	External RTC Device
XMC Slot	50H (A0H)	To XMC Mezzanine SMBus

cPLD I2C Bus (100 KHz)

SLAVE DEVICES ON CPLD SMBUS INTERFACE	SMBUS 7-BIT BASE ADDRESS (8-BIT BASE ADDRESS)	FEATURES
Integrated LAN to SoC	61H (C2H)	10GbE LAN ports. Note that the low I2C bus is internally disconnected into the cPLD.

cPLD I2C Bus (1 MHz)

SLAVE DEVICES ON CPLD SMBUS INTERFACE	SMBUS 7-BIT BASE ADDRESS (8-BIT BASE ADDRESS)	FEATURES
24FC256-I/SN VPD EEPROM	50H (A0H)	256 Kbits VPD EEPROM
24FC256-I/SN OS EEPROM	51H (A2H)	256 Kbits OS EEPROM
FM24V10-G	52H (A4H) / 54H (A8H) /	1 Mbits User FRAM

IPMC I2C Bus (100 KHz)

SLAVE DEVICES ON IPMC SMBUS INTERFACE	SMBUS 7-BIT BASE ADDRES (8-BIT BASE ADDRESS)S	FEATURES
NCT7802Y sensor	28H (50H)	Nuvoton Voltage / Temperature Sensor
AT24C512C/SN FRU EEPROM	50H (A0H)	512 Kbits FRU EEPROM

3.3. CPLD Features

The CPLD manages the following features:

- Power-on/off control
- Reset control
- LPC interface to processor
- KCS interface to IPMC
- LEDs control
- Serial lines multiplexer
- Serial VPD and user memories
- User and system GPIOs
- Internal registers that allow system management

cPLD Register

cPLD registers are accessible from CPU through LPC bus. See cPLD registers overview in section 11.5 of Linux Kontron VME/VPX Fedora 28 Remix - Release Notes - D215295. Contact Kontron for a detailed description of the CPLD registers.

3.4. Serial Lines Additional Modes

Two EIA-232 serial lines COM1 and COM2 are available on P1 connector. These two serial lines are defined as maintenance ports in VITA65.0 standard.

See section 4.2.2 page 57 - "P1 Connector" for more information on pin assignments.

3.3V LVCMOS signaling

COM1 and COM2 maintenance ports support TIA-232 signal level and 3V3 LVCMOS level signaling. Selection between these two modes is done from BIOS menu, see section 6.1.2 in VX305x-40G AMI BIOS - User Manual D213792.

Maintenance Ports use LVCMOS signaling non-inverted (active high) level with the following characteristics.

Table 12: 3.3V LVCMOS voltage levels

3.3V LVCMOS Voltage levels	
VCC	3.3V +/- 0.3V
Vih	1.7V
Vil	0.7V
Voh	2.0V
Vol	0.4V

3.5. GDISCRETE1

GDISCRETE1 is a bussed open-collector GPIO defined by OpenVPX VITA 65 and available on P1. See section 4.3.2 "P1 Connector" page 57 for detailed pinout.

It is handled by the CPLD and buffered by a SN74LVC1G125 wired as an Open Collector to meet the electrical characteristics defined in VITA 65.

It has a dedicated interrupt in the CPLD.

3.6. Reset

RESET SOURCE	RESET ACTION	RESET CONTROL	RESET STATUS	NOTE
Front panel reset push button	Platform resetreset	Front push button	cPLD I2C_BOARD_STATUS @0x72	Reset propagation options and masks available in cPLD registers
VPX Sysreset	Platform resetreset	VPX P0 / Row B/ Wafer 4	cPLD I2C_BOARD_STATUS @0x72	"See VPX Vita46.0 standard Reset propagation options and masks available in cPLD registers"
VPX maskable reset (GPIO8)	Platform resetreset	VPX P1 / Row G/ Wafer 15	cPLD I2C_BOARD_STATUS @0x72	See VPX Vita46.0 standard
cPLD watchdog reset	Platform resetreset	See Kontron VME/VPX Fedora 28 Remix release notes	cPLD I2C_BOARD_STATUS @0x72	See Kontron VME/VPX Fedora 28 Remix release notes
Processor watchdog reset	Platform resetreset	Intel D-15xx watchdog control registers	Intel D-15xx watchdog status registers	
cPLD software reset	Platform resetreset	cPLD I2C_BOARD_CONTROL @0x73	cPLD I2C_BOARD_STATUS @0x72	See Kontron VME/VPX Fedora 28 Remix release notes

3.7. Write Protect Mode

VX305H-40G non-volatile content is managed in three independent write protection domains.

- SYS: Temporary, run time data
- USR: Settings data , maintenance under user control
- VPD: Kontron driven static data

On top of the domains, two 'top level' settings can override the domains write protection

- NVMRO: force all domains to be Write Protected
- FACTORY: force all domains to be Writeable

SYS_WP

- Description:
  Write protection at system level of run time volatile information (SEL IPMC events and PBIT results)
- Hardware Write Protection:
  NVMRO signal is high and SW1[1] is OFF for full protection
- Write Protect Contol:

NVMRO	sw1[1] Factory mode	CPLD register @09-bit 2	Protection	Mode of Operation
1	OFF	X	YES	Normal
0	X	0	No	Normal
1	ON	1	YES	Factory
1	ON	0	No	Factory
0	X	1	YES	Software forced protection

X = "don't care", CPLD register @09-bit 2 default setting is "0"

- Protected Devices:
  - 256 Kbits OS EEPROM on CPLD I2C bus @0x51
  - XMC EEPROM
  - 512Kbits FRU EEPROM on IPMC local I2C bus @0x50

USER_WP

- Description:
  Write protection at user level for maintenance and user driven information
- Hardware Write Protection:
  MVMRO signal is high and SW1[1] is OFF for full protection
- Write Protect Contol:

NVMRO	sw1[1] Factory mode	sw1[4] User write protection	CPLD register @09-bit 3	Protection	Operation
1	OFF	X	X	YES	Normal
0	X	OFF	0	No	Normal
1	ON	ON	X	YES	Factory
1	ON	OFF	0	No	Factory
1	ON	OFF	1	YES	Factory

NVMRO	sw1[1] Factory mode	sw1[4] User write protection	CPLD register @09-bit 3	Protection	Operation
0	X	ON	X	YES	DIP switch forced protection
0	X	OFF	1	YES	Software forced protection

X = “don’t care”, CPLD register @09-bit 3 default setting is “0”

- Protected Devices:
  - 1 Mbits User FRAM located on CPLD I2C2 bus @0x52/53
  - SPI Boot Flash memories
  - SPI IPMC Boot Flash memory
  - Internal memory Flash of IPMC
  - Internal CPLD configuration flash

VPD_WP

- Description:
  Write protection at VPD level of static information vendor/kontron driven.
- Hardware Write Protection:
  MVMRO signal is high and SW1[3] & SW1[1] are OFF for full protection
- Write Protect Contol:

NVMRO	sw1[1] Factory mode	sw1[3] VPD write protection	CPLD register @09-bit 1	Protection	Protection
X	X	ON	X	No	DIP switch released protection
1	OFF	OFF	X	YES	Normal
1	ON	OFF	0	No	Factory
1	ON	OFF	1	YES	Factory
0	X	OFF	0	No	Software released protection
0	X	OFF	1	YES	Normal

X = “don’t care”, CPLD register @09-bit 1 default setting is “1”

- Protected Devices:
  - 256Kbits VPD EEPROM on CPLD I2C2 bus @0x50
  - DDR4 memory SPD EEPROM devices
  - SPI flash for I210T Ethernet controller
  - SPI flash for 10 Gb integrated Ethernet controller of SoC
  - SPI flash for 40 Gb Ethernet controller

NVMRO

- All non-volatile devices protected.
- NVMRO signal is high and SW1[3] & SW1[1] are OFF for full non-volatile devices protection.
- VX305H-40G offers the capability to drive the NVMRO signal on the backplane by setting SW2[3] OFF.

⚠CAUTION

Set the hardware jumper SW2[3] to OFF force to ground the NVMRO signal on the backplane. Write protection is de-asserted for all the boards in the chassis.

3.8. IPMC

The VX305H-40G embeds an IPMI controller so much so that the VX305H-40G is considered as a FRU as per VITA 46.11. The IMPI controller is accessible through an IPMB bus or through a host Keyboard Controller Style (KCS) interface.

The VX305C-40G is fully compliant with VITA 46.11 specification.

The IPMC manages the following features:

- Local environmental control/monitoring
- I2C interfaces to I2C bus IPMB A/B (rear P0)
- KCS interface to CPLD
- Serial FRU memory
- IPMI watchdog
- System Event Log (SEL)
- Sensor Device functionality

For further detail about IPMI firmware, refer to VX305x-40G IPMI Firmware Release Note D218432.

VX305H-40G VPX IPMB I2C interfaces

VX305H-40G implements two I2C buses connected to P0 VPX connector. See section 4.3.1 “P0 Connector” page 56 for P0 pin assignments:

- IMPB A (I2C0) : CLK signal on pin P0/B5, DATA signal on pin P0/ A5
- IPMB B (I2C1) : CLK signal on pin P0/G4, DATA signal on pin P0/ F4

Supported IPMI commands available

The VX305H-40G IPMI firmware supports all the Mandatory IPMC Tier-1 and Tier-2 commands. See the exhaustive list of IPMI supported commands in the VX305x-40G IPMI Firmware Release Note D218432.

3.9. Kontron Security Solution

The VX305H-40G answers digital security requirements with hardware enforced root of trust (secure elements). The VX305H-40G supports SEC-Line computer security offering:

- **APPROTECT**: Application integrity, confidentiality, only authorized copies
- **TRUSTED BOOT**: Detect system software alteration
- **AUTHENTICATION WITH TPM**: Secure network protocols

If required customers can customize the solution to meet specific needs. For more information contact Kontron Technical Support.

3.9.1. Approtect

The APPROTECT solution, using a security technology from Wibu, a Kontron partner, protects the application from the main security threats with the security of a dedicated hardware secure element located on the VX305H-40G board.

The main security threats at the application level are:

- **Integrity**: the running application might be hacked or patched in binary, on the disk or in memory, to modify its behavior or work around some checks.
- **Confidentiality**: the way the application code is working could be analyzed in details by looking at the execution code, in order to learn or to reproduce its behavior.
- **Unauthorized copies**: the embedded systems (software application or full equipment) suffer the risk of being cloned without authorization.

Technical information

- **Security Hardware**: CodeMeter ASIC 1504-03 based on Infineon SLM-97CUSIFX1M00 smart card chip
- **Encryptions standards**: Used algorithms in Firmware 4.0: 128 bit AES, SHA-256, 2048 bit RSA, 224 bit ECC.

3.9.2. Trusted Platform Module (TPM 2.0)

The VX305H-40G is compliant to TPM 2.0. A Trusted Platform Module (TPM) stores RSA encryption keys specific to the host system for hardware authentication. The term TPM refers to the set of specifications applicable to TPM chips.

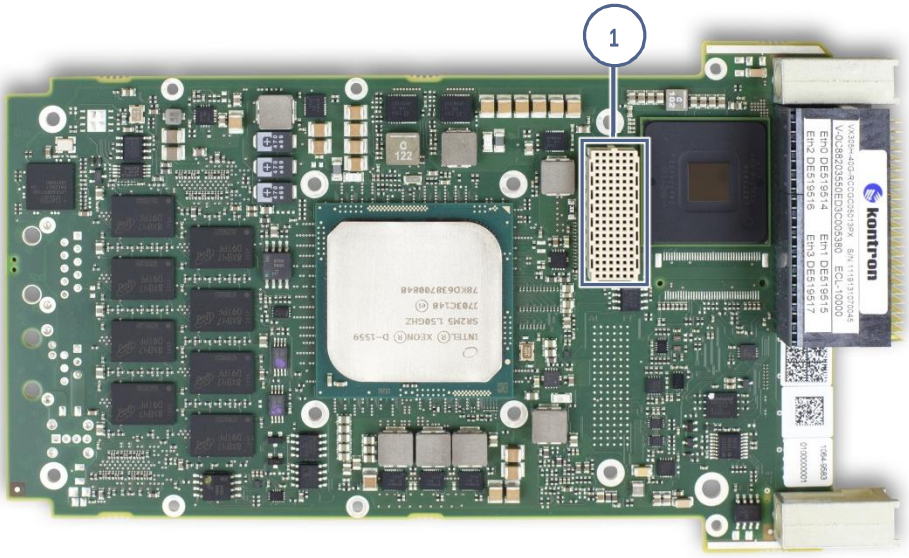
Each TPM chip contains an RSA key pair called the Endorsement Key (EK). The pair is maintained inside the chip and cannot be accessed by software. The Storage Root Key (SRK) is created when a user or administrator takes ownership of the system. This key pair is generated by the TPM based on the Endorsement Key and an owner-specified password.

A second key, called an Attestation Identity Key (AIK) protects the device against unauthorized firmware and software modification by hashing critical sections of firmware and software before they are executed. When the system attempts to connect to the network, the hashes are sent to a server that verifies that they match the expected values. If any of the hashed components have been modified since last started, the match fails, and the system cannot gain entry to the network.

4 / Physical I/O

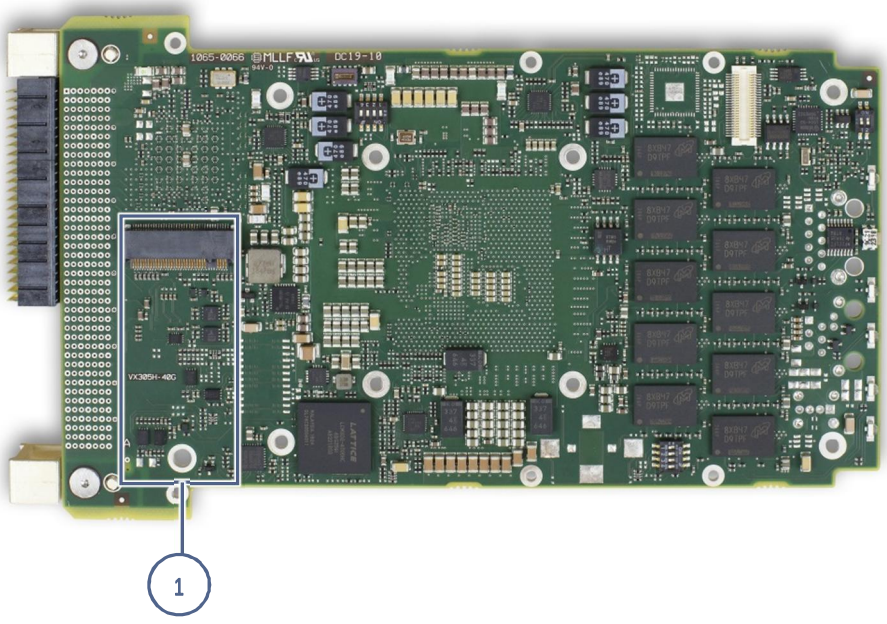
4.1. Onboard Connectors

Figure 20: Onboard Connectors (top)



1. J15

Figure 21: Onboard Connectors (bottom)



1. P2801

4.1.1. XMC J15 Connector Pin Assignments

The pin assignment of the J15 XMC PCI Express connector is compatible with VITA 61.0 pin definition. This interface is a PCI Express with 8 lanes coming from the CPU.

Table 13: XMC J15 Connector Pin Assignments

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR (1)
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR (1)
4	GND	GND	TCK	GND	GND	N.C.
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR (1)
6	GND	GND	TMS	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR (1)
8	GND	GND	TDI	GND	GND	-12V
9	RFU	RFU	N.C.	RFU	RFU	VPWR (1)
10	GND	GND	TDO	GND	GND	GA0
11	PER0p0	PER0n0	N.C.	PER0p1	PER0n1	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PER0p2	PER0n2	3.3V AUX	PER0p3	PER0n3	VPWR (1)
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	N.C.	PER0p5	PER0n5	VPWR (1)
16	GND	GND	NVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	N.C.	PER0p7	PER0n7	N.C.
18	GND	GND	N.C.	GND	GND	N.C.
19	REFCLK+0	REFCLK-0	N.C.	WAKE#	N.C.	N.C.

(1) VPWR is connected to +12V via a fuse.

Signals active when low.

Table 14: XMC J15 Connector Signals Definition

MNEMONIC	DIRECTION	SIGNAL DEFINITION
+12V	O	+12 Volts DC power pin.
-12V	O	-12 Volts DC power pin.
3.3V	O	+3.3 Volts DC power pin.
3.3V AUX	O	Auxiliary +3.3 Volts.
GA[0..2]	O	I2C channel select as per VITA42.0.
GND	-	Ground
MRSTI#*	O	XMC Reset In as per VITA42.0 (10 ms pulse min.) and PCIe PERST# as per VITA42.3.
MSDA	I/O	I2C serial data as per VITA42.0.
MSCL	O	I2C serial clock as per VITA42.0.
MPRESENT#	O	Module present as per VITA42.0.
N.C.	-	Not Connected

MNEMONIC	DIRECTION	SIGNAL DEFINITION
NVMRO	O	XMC Write Prohibit as per VITA42.0.
TCK	O	JTAG Clock as per VITA42.0.
TDI	O	JTAG Data In as per VITA42.0.
TD0	I	JTAG Data Out as per VITA42.0.
TMS	O	JTAG Mode Select as per VITA42.0.
TRST#	O	JTAG Reset as per VITA42.0.
PET0p0/n[0..7]	I	PCIe differential transmit pairs 0 to 7 (as per VITA42.3)
PER0p0/n[0..7]	O	PCIe differential receive pairs 0 to 7 (as per VITA42.3)
REFCLK+/-0	O	100MHz PCIe differential reference clock as per VITA42.3.
RFU	-	Reserved For User
VPWR	O	+12V power pins.
WAKE#	I	Open drain WAKE# signal.

4.1.2. M2 Bottom Socket Pin Assignment

The M.2 bottom socket (P2801 connector) is used to connect a M.2 module, key M for SSD storage. SATA III is the default interface of SSD storage module. PCIe x1 interface may be also available on customer request.

The M.2 socket supports only 2242 form factor. This M.2 slot is compliant with S1, S2, S3, D3, D4 type module component heights as per PCI Express M.2 Specification.

Table 15: P2801 Top Socket Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	3V3
3	GND	4	3V3
5	NC	6	NC
7	NC	8	NC
9	GND	10	DAS/DSS#LED1#
11	NC	12	3V3
13	NC	14	3V3
15	GND	16	3V3
17	NC	18	3V3
19	NC	20	NC
21	GND	22	NC
23	NC	24	NC
25	NC	26	NC
27	GND	28	NC
29	NC	30	NC
31	NC	32	NC
33	GND	34	NC
35	NC	36	NC
37	NC	38	DEVSLP
39	GND	40	NC
41	PER0-/SATA-B+	42	NC
43	PER0+/SATA-B-	44	NC

PIN	SIGNAL	PIN	SIGNAL
45	GND	46	NC
47	PET0-/SATA-A-	48	NC
49	PET0+/SATA-A+	50	PERST#
51	GND	52	CLKREQ#
53	REFCLK_N	54	PEWAKE#
55	REFCLK_P	56	NC
57	GND	58	NC
59	CONNECTOR	60	CONNECTOR_KEY
61	CONNECTOR	62	CONNECTOR_KEY
63	CONNECTOR_KEY	64	CONNECTOR_KEY
65	CONNECTOR_KEY	66	CONNECTOR_KEY
67	NC	68	SUSCLK
69	PEDET	70	3V3
71	GND	72	3V3
73	GND	74	3V3
75	GND		

When PCI Express and SATA functions coexist the following convention applies: PCI Express function / SATA function.

Table 16: M.2 Module Socket Signal Description

MNEMONIC	DIRECTION	SIGNAL DEFINITION
3.3V	O	+3.3V power supply.
GND	-	Logic ground.
LED1# / DAS_DSS#	I	- PCI Express: LED_1# indicator as per PCI Express M.2 specification. - SATA: Device Activity Signal /Disable Staggered Spinup as per SATA 3.2. DAS is not connected to a LED (which is the main purpose of this signal) and DSS is not used since the devices are SSD and not hard drives (no spinup). Signal connected to dedicated CPLD
PEDET	I	PEDET (PCI Express Detect) as per PCI Express M.2 specification is driven low by SATA modules and high-Z by PCI Express modules (seen as a logic 1 due to on-board pull-up resistor). This signal is connected to a dedicated CPLD pin.
PERp/n0 / SATA-B+/-	I	- PCI Express: Receive differential pair as per PCI Express M.2 & PCI Express 3.0 specifications. - SATA: Receive differential pair as per SATA 3.2.
PERST#	O	- PCI Express: PCI Express PERST# as per PCI Express M.2 specification, handled by CPLD. - SATA: NC.
PETp/n0 / SATA-A+/-	O	- PCI Express: Transmit differential pair as per PCI Express M.2 & PCI Express 3.0 specifications. - SATA: Transmit differential pair as per SATA 3.2.
PEWAKE#	I	- PCI Express: Opain drain WAKE# signal as per PCI Express M.2. - SATA: NC..
REFCLKP/N	O	- PCI Express: Opain drain WAKE# signal as per PCI Express M.2. - SATA: NC..
SUSCLK	O	Suspend Clock for low power mode handling as per PCI Express M.2 specification (32.768 kHz, duty cycle between 30% and 70%, 200ppm). Connected to SoC SUSCLK_GPIO62.

When PCI Express and SATA functions coexist the following convention applies: PCI Express function / SATA function.

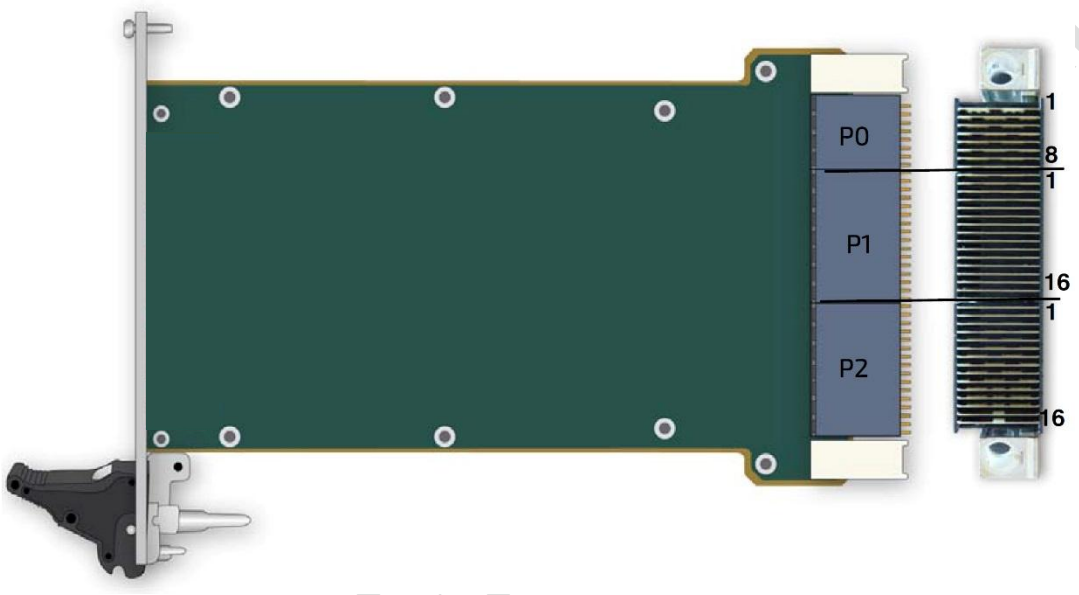
4.2. Rear Connectors

VPX Bus Interface

The complete 3U VPX connectors configuration comprises three connectors named P0 to P2:

- P0: 8-wafer 7-row connector.
- P1 - P2: 16-wafer 7-row differential connectors.

Figure 22: VPX Connectors



P2 connector is not equipped on standard VX305H-40G product to compliant with slot profile SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-n. However, P2 connector can be proposed on customer request offering additional I/O such as USB or 1000Base-T Ethernet. For further details, see section 6.4.1 “P2 Connector” page 76.

4.2.1. P0 Connector

Table 17: VPX Connector P0 Wafer Assignment

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	+12V	+12V	+12V	NC	NC	NC	NC
2	+12V	+12V	+12V	NC	NC	NC	NC
3	NC	NC	NC	NC	NC	NC	NC
4	IPMB_B CLK	IPMB_B DAT	GND	-12V_AUX	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3V3_AUX	GND	IPMB_A CLK	IPMB_A DAT
6	GA3*	GA2*	GND	NC	GND	GA1*	GA0*
7	NC (GPIO7)	GND	NC	NC	GND	NC (GPIO5)	NC (GPIO6)
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND
CASE	GND						

* signal active when low

Table 18: VPX Connector P0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
+12V	+12 Volts DC power (VS1 VPX supply). NC (+12V/+5V) pins are not connected (VS2/VS3 VPX supplies)
3V3_AUX	3.3 Volts auxiliary power. Not required because it generate internally is 3V3_AUX power rail is not present on the backplane.
-12V_AUX	-12 Volts auxiliary power. Only used to supply XMC if needed.
NVMRO	Non-Volatile Memory Read Only. When asserted (logical 1), prevents any non-volatile memory from being updated.
GAi	Geographical address pins
GAP	Geographical address parity
GND	Ground
GPIO5, 6, 7*	General purpose I/O (handled by CPLD). Not connected by default, contact Kontron support for availability.
IPMB A	I2C Bus 0
IPMB B	I2C Bus 1
REF_CLK+/-	The Reference Clock is a bussed differential pair. Output if the VX305H-40G-SA is plugged in the system controller slot, input otherwise. It enables the entire system to synchronize to a common time reference if desired. Counter/timer in the CPLD can use this clock
AUX_CLK+/-	1 PPS (one pulse per second) clock input. Can be programmed as an output on system controller slot. Can be used to phase the CPLD timer/counter clocked by REF_CLK+/-.
SYSRESET*	System Reset. Input and open collector output.

* See section 6.2- “GPIOs” - page 75.

4.2.2. P1 Connector

Table 19: VPX Connector P1 Wafer Assignment

- Legend for Table 19:

P1_VBAT	Battery Voltage	NC (GPIO1)	NC by default. GPIO1 depending on build option
P1_SYS_CON*	System Controller	CLK1-/+	Radial clock
PCIe LxRX | LxTX	x8 PCI-Express	ETHx TX/RX	1000BASE-KX Ethernet controller or 10GBASEKR links 0 and 1 from integrated 10 GbE controller as per VITA 46.7.
COM1/COM2	Maintenance Ports	40GBE_TX/RX	40GBASEKR-4 link from XL710 40GbE controller

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	GDISCRETE1	GND	40GBE_TX0-	40GBE_TX0+	GND	40GBE_RX0-	40GBE_RX0+
2	GND	40GBE_TX1-	40GBE_TX1+	GND	40GBE_RX1-	40GBE_RX1+	GND
3	VBAT	GND	40GBE_TX2-	40GBE_TX2+	GND	40GBE_RX2-	40GBE_RX2+
4	GND	40GBE_TX3-	40GBE_TX3+	GND	40GBE_RX3-	40GBE_RX3+	GND
5	SYS_CON*	GND	ETH0 TX-	ETH0 TX+	GND	ETH0 RX-	ETH0 RX+
6	GND	CLK1-	CLK1+	GND	COM1 TXD	COM1 RXD	GND
7	GND	GND	GND	GND	GND	GND	GND
8	GND	ETH1 TX-	ETH1 TX+	GND	ETH1 RX-	ETH1 RX+	GND
9	COM2 TXD	GND	PCIe L0-TX-	PCIe L0-TX+	GND	PCIe L0-RX-	PCIe L0-RX+
10	GND	PCIe L1-TX-	PCIe L1-TX+	GND	PCIe L1-RX-	PCIe L1-RX+	GND
11	COM2 RXD	GND	PCIe L2-TX-	PCIe L2-TX+	GND	PCIe L2-RX-	PCIe L2-RX+
12	GND	PCIe L3-TX-	PCIe L3-TX+	GND	PCIe L3-RX-	PCIe L3-RX+	GND
13	NC (GPIO1)	GND	PCIe L4-TX-	PCIe L4-TX+	GND	PCIe L4-RX-	PCIe L4-RX+
14	GND	PCIe L5-TX-	PCIe L5-TX+	GND	PCIe L5-RX-	PCIe L5-RX+	GND
15	Maskable Reset*	GND	PCIe L6-TX-	PCIe L6-TX+	GND	PCIe L6-RX-	PCIe L6-RX+
16	GND	PCIe L7-TX-	PCIe L7-TX+	GND	PCIe L7-RX-	PCIe L7-RX+	GND
CASE	GND						

* signal active when low

Table 20: VPX Connector P1 Signal Definition

MNEMONIC	SIGNAL DEFINITION
40GBE-RX[0..3]+/-	40GBASE-KR4 Ethernet link: Receive data +/-
40GBE-TX[0..3]+/-	40GBASE-KR4 Ethernet link: Tranmit data +/-
PCIe Lx-RX+/-	x8 PCI Express Link. Receive +/-, gen1, gen2 or gen3 May also be used as a 2 x4 links using BIOS setting.
PCIe Lx-TX+/-	x8 PCI Express Link. Transmit +/-, gen1, gen2 or gen3 May also be used as a 2 x4 links using BIOS setting.
ETHx RX+/-	10GBASE-KR or 1000BASE-KX Ethernet x: Receive data +/- (auto negotiation)
ETHx TX+/-	10GBASE-KR or 1000BASE-KX Ethernet x: Transmit data +/- (auto negotiation)
GDISCRETE1	Open VPX GDISCRETE1 signal
NC (GPIO1*)	Not connected (General Purpose I/O 1 (handled by the CPLD))
Maskable Reset* or GPIO8	Reset input or Optional general purpose I/O 8 (handled by CPLD) (may be left unconnected if not used).
GND	Ground
SYS_CON	System Controller Slot Indication
VBAT	Battery Voltage Input, 3V. Optional alternated source for RTC backup voltage.
COM1/COM2	Maintenance ports : serial Lines EIA-232 or 3V3 LVCMOS level signaling

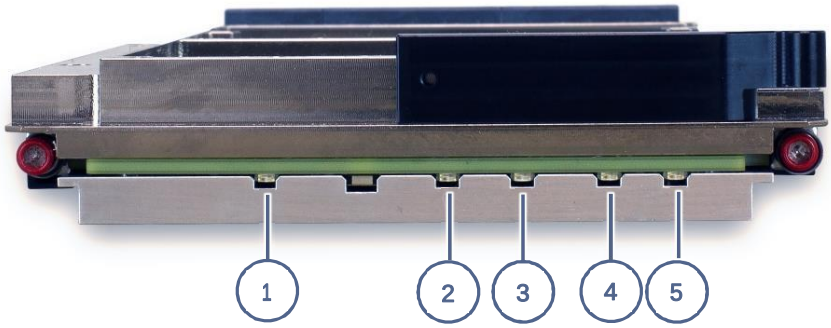
* See section 6.2 - GPIOs- page 75.

4.3. LEDs

4.3.1. Status LEDs Default Setting

There are five bicolor LEDs (Red/Green) on the front panel of the VX305H-40G 3U VPX board.

Figure 23: LEDs Front panel



1. L1 LED
2. L2 LED
3. L3 LED
4. L4 LED
5. L5 LED

4.3.2. LEDs Activity

Table 21: LEDs Description

CPU LED	DESCRIPTION
●	LED OFF
●	Red LED
●	Green LED
●	Orange LED
✳	Red blinking LED
✳	Green Blinking LED
✳	Orange blinking LED
✳	Not blink: Indicates that the corresponding LED gives an additional information if any LED is blinking at the same time

The following table describes the information that the LED can report:

Table 22: LEDs Activity

L1	L2	L3	L4	L5	MEANING
●	Not Blink	Not Blink	Not Blink	Not Blink	Permanent system error. Internal VX305H-40G power is off. In this state L2, L3, L4 and L5 do not carry the meaning described in this table but an error code detailed in the **ERRORS CODES** table.
●					Normal operation
	●				10G Ethernet controller link up. ✳ Blinking when activity on the link
	●				10G Ethernet controller off
		●			Internal power supplies are ON and board reset is asserted.
		●			Internal power supplies are ON and board reset de-asserted (normal operation).
		●			Internal power supplies are ON but PROCPWRGD_PCH not activated
		✳			Blinking (1 Hz, 50% duty cycle) when internal power supplies are OFF (board in standby)
			●		40G Ethernet controller link up. ✳ Blinking when activity on the link
			●		40G Ethernet interfaces: down grade link up or Factory mode (1) ✳ Blinking when activity on the links
			●		CPLD Watchdog expired
			●		40G Ethernet controller off
				●	M2 SSD present on bottom socket ✳ M2 SSD activity
				●	Processor hot event (PROCHOT)
				●	M2 SSD not present

Factory mode supersedes the 40G interface link-up and activity (1)

L1	L2	L3	L4	L5	POWER GOOD ERRORS
●	●	●	●	●	PWRGD_VPX
●	●	●	●	●	VPXPWRGD_UV
●	●	●	●	●	VPXPWRGD_OV
●	●	●	●	●	PWRGD_VR5V0
●	●	●	●	●	PWRGD_VCCSCFUSESUS
●	●	●	●	●	PWRGD_VCCKRHV
●	●	●	●	●	PWRGD_VR1V5_PCH
●	●	●	●	●	PWRGD_VR1V05
●	●	●	●	●	PWRGD_VR2V5_DDR4
●	●	●	●	●	PWRGD_VR1V2
●	●	●	●	●	PWRGD_VTT
●	●	●	●	●	Reserved
●	●	●	●	●	PWRGD_0V85
●	●	●	●	●	PWRGD_VR3V3
●	●	●	●	●	PWRGD_VRVCCIN
●	●	●	●	●	RESERVED
●	●	●	●	●	WAKE UP ERROR (timeout on SLP_S4# deassertion)
●	●	●	●	●	PROCPWRGD ERROR (timeout on PROCPWRGD_PCH assertion)
●	●	●	●	●	PLTRST# ERROR (timeout on deassertion S5 To S0)
●	●	●	●	●	LPC CLOCK is 48 MHz (Legacy value is 33 MHz)
●	●	●	●	●	LPC CLOCK is 25 MHz (Legacy value is 33 MHz)

L1	L2	L3	L4	L5	CRITICAL ERRORS
●	●	●	●	✳	PECI_CRIT#
●	●	●	✳	●	CATERR#
●	●	✳	●	●	VR1V05_VRHOT#
●	✳	●	●	●	VRVCCIN_VRHOT#
✳	●	●	●	●	THERMTRIP#

5/ Power and Thermal Specifications

5.1. Power considerations

The considerations presented in the ensuing sections must be taken into account by system integrators when specifying the VX305H-40G system environment.

5.1.1. Backplane

Backplanes to be used with the VX305H-40G must be adequately specified and comply with VITA 65.0. The backplane must provide optimal power distribution for the VPX VS1, VS2, VS3 and 3V3 AUX power inputs.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided.

5.1.2. Power Supply Units

Power supplies for the VX305H-40G must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires.

An industrial power supply unit should be able to provide at least twice as much power as the entire system requires.

An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for die resistance variations.

Tolerance

The following table provides information regarding the required characteristics for each board input voltage.

POWER RAIL	NOMINAL VALUE	TOLERANCE*	MAX RIPPLE (p-p)	REMARKS
+12V VPX VS1	+12VDC	+/-5%	50mV over a range of 0-20MHz	Main voltage
+3.3V VPX VS2	+3.3VDC	3.25V min 3.45V max	50mV over a range of 0-20MHz	Not used
+5V VPX VS3	+5VDC	+5%/-2.5%	50mV over a range of 0-20MHz	Not used
VPX 3.3V AUX	+3.3VDC	+/-5%	50mV over a range of 0-20MHz	Optional
GND	Ground, not directly connected to potential earth (PE)			

(*)Tolerance values include ripple.

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off

Rise Time

As per VITA 46.0, section 3.2.2, the system power supply ramp-up phase should be between 20 and 150 msec. However, Kontron recommend a ramp-up phase below 25ms.

Regulation

The system power supplies should be monotonic as they ramp to their specified final values during power up conditions as per VITA 46.0, section 3.2.2.

The system power supplies shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it went below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

5.1.3. Power Supplies Monitoring

The VX305H-40G embeds two voltage sensors monitoring power rails and internal power supply voltage.

- NCT7802Y by Nuvoton
- LTC2913 by Linear Technology

The voltage sensor NCT7802Y is programmed by the IPMC to monitor VS1 and internal voltages, it asserts an alert signal whenever either voltages get out of its specified range. This alert is routed to a maskable interrupt in the cPLD. For detailed specification of NCT7802Y, refer to section 5.4, “Board Thermal Monitoring”, page 66.

The voltage sensor LTC2913 monitors VS1 voltage with a 10 % tolerance. The thresholds are set by hardware on the board. Undervoltage and overvoltage conditions on VS1 are reported to the cPLD which in turn shuts down all VX305H-40G internal power supplies. There is no mechanism for masking these alerts.

5.1.4. Output Powers Supplies Protection

On the VX305H-40G, all the output power supplies provided on connectors are protected by fuse or current-limiting devices as described in Table 23.

Table 23: Output Powers Supplies Protection

Port	Function	Location	Voltage	Protection	Rated Current	Trip current	Characteristics
M2. Slots	M2 slot power supply	On board	+3.3 V	Non resettable fuse	2.5 A	-	-
XMC Slot	VPWR XMC slot power supply	On board	+12 V	Non resettable fuse	3 A	-	-
XMC Slot	3.3V XMC slot power supply	On board	+3.3 V	Non resettable fuse	3 A	-	-
VPX P2 Rear DVI power pins	P2 DVI Power	Rear P2	+5 V	Non resettable fuse	1.5 A	2.1 A min @ 85 °C 3.0 A typ @ 23 °C 3.5 A max @ -40 °C	
VPX P2 Rear USB power pins	P2 USB Power	Rear P2	+5 V	Non resettable fuse	1.5 A	2.1 A min @ 85 °C 3.0 A typ @ 23 °C 3.5 A max @ -40 °C -	-

5.2. VPX Input Power Rails Specification

The VX305H-40G board has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

Absolute Maximum Input Voltage

The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the VX305H-40G should be carefully tested to ensure compliance with these ratings.

Table 24: Absolute maximum input voltage

POWER RAIL	ABSOLUTE MAXIMUM INPUT VOLTAGE
VPX 3.3V AUX	3.5V
+12V VPX VS1	13V

⚠WARNING

The maximum permitted voltage indicated in the table above must not be exceeded. Failure to comply with these figures may result in damage to your board.

Recommended Operating Input voltage

The following table specifies the recommended operating conditions of the different input power voltages within the board as per VITA46.0, section 3.2.2. The VX305H-40G is not guaranteed to function if the board is not operating within the prescribed limits.

Table 25: Recommended Operating Input Voltage

POWER RAIL	RECOMMENDED OPERATING INPUT VOLTAGE
VPX 3.3V AUX	3.3V +/-5%
+12V VPX VS1	+12V +/-5% inclusive of ripple

VPX 3.3V AUX shall be used on VX305H-40G boards as per VITA 46.0 and VITA 65.0. However, this power rail input could be optional on VX305H-40G boards because it is internally generated from the +12V VS1 power input when it is not present on the backplane. If both, VBAT and 3.3V AUX are not present on the backplane, the date and time retention is not ensured.

Input Power Supply Protection

The input power rails are protected on the VX305H-40G by fuse as described in Table 26.

To prevent safety hazards, the chassis power supply must not exceed the Voltage Rating and Interrupt Rating of the fuse.

Table 26: Input Powers Supplies Protection

POWER RAIL	VPX VS1	VPX 3.3 V AUX
LOCATION	P0	P0
VOLTAGE	+12 V	+3.3 V
PROTECTION	Non resettable fuse	Non resettable fuse
RATED CURRENT	10 A	1.5 A
TRIP CURRENT	-	2.1 A min @ 85 °C 3.0 A typ @ 23 °C 3.5 A max @ -40 °C
TYPICAL MELT I^2T	2.0	-
VOLTAGE RATING	24 V	32 V
INTERRUPTING RATING	150 A	35 A
MANUFACTURER / PN	3216FF10-R	043501.5KR

5.3. Power Consumption Specification

5.3.1. VX305H-40G Thermal Power

The following data show total board consumption for different processor configuration and Thermal Design Power. These data help for thermal power dissipation analysis.

All power values in this table are measured in operational conditions on Xeon-D parts.

Table 27: Thermal Power: board power based on current measurements

Product	Power Mode	Measured CPU package power/Freq	Max total Power consumption (W)	Test Condition
VX305H-40G D-1559 @ 1.5 GHz	100 % all cores @ 1.5 GHz Max Processor Power package	45 W / 1.5 GHz	60 W	Maximum CPU junction temperature Dual bank DDR4-2133 memory configuration full speed LinuxOS with Power Thermal Utility from Intel running on all cores I/Os configuration: rear panel serial line, no Ethernet links up, no USB devices, one SSD M.2 module, no PCIe x8 link, no LPC/FRAM activity
	80 % all cores	36 W / 1.5 GHz	52 W	
	Linux Idle Linux "On demand" mode	TBD W / 800 MHz	TBD	Maximum CPU junction temperature Dual bank DDR4-2133 memory configuration full speed LinuxOS, no I/Os stress tests

Product	Voltage Rail Name	Max Current	Max Continuous Power Consumption (W)	Test condition
VX305H-40G without VPX VS1 power supply Board in stand-by mode	VPX +3V3_AUX	230 mA continuous (2.5 A peak / 2 ms)	0.76 W	VPX +3V3_AUX power rail is present and VPX VS1 power rail not present. VPX +3V3_AUX power rail must support peak current condition at power-on.

5.3.2. VX305H-40G Maximum and Peak Current

The following data provide maximum continuous and worst case current values on VPX VS1 (12V) power supply. These maximum includes margin to guarantee worst-case part behavior.

Table 28: Maximum VS1 Current

	Max VPX VS1 current	Max VPX VS1 Peak	Test Condition
VX305H-40G D-1559 @ 1.5 GHz	6 A	TDB	Calculated value based on measurements and for CPU @ 1.25*TDP

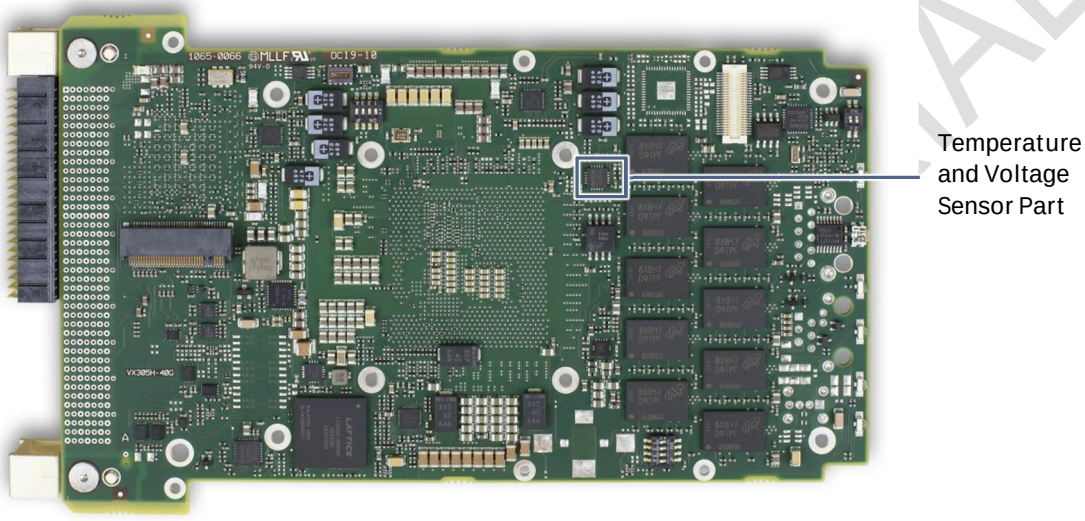
Maximum and peak current draw are intended as without enabled Turbo mode and without XMC mezzanine card or M.2 device plugged on board.

5.4. Board Thermal Monitoring

To ensure long-term reliability of the VX305H-40G, onboard components must not operate beyond their specified maximum temperature. The most critical component on the VX305H-40G is the processor. Operating the VX305H-40G above the maximum operating limits will result in permanent damage to the board.

The VX305H-40G includes a temperature sensor (NCT7802Y by Nuvoton) managed by the IPMC through I2C. See Figure 16 “I2C Diagram” page 44.

Figure 24: Temperature Sensor Location



In addition to monitoring several internal power supplies, the NCT7802Y supports one on-die temperature sensor and can also get the processor temperature directly via the Intel® PECI3.0 interface. The NCT7802Y temperature and voltages monitoring data may be viewed with the Linux "ipmitool" command.

The NCT7802Y has 2 alarm outputs connected to the CPLD:

- ALERT#: logged in CPLD to generate a maskable interrupt. By default, the high threshold is set to +95°C and the low threshold is set to -45 °C.
  Thresholds may be modified by the Shelf Manager using the IPMI command or locally by using Linux “ipmitool” command.
  The low threshold may also be used as the lower threshold for high temperature hysteresis.
- T_CRIT#: logged in CPLD reg @0x74, leads to fatal error with all internal PSUs power supplies being switched off and the error status is being displayed on the front panel LEDs. The T_CRIT# threshold is set by default to +100 °C by IPMC.
  T_CRIT threshold may be modified by the Shelf Manager using the IPMI command or locally by using Linux “ipmitool” command.

NCT7802Y Key specifications:

- Voltage monitoring accuracy +-10 mV
- Temperature Sensor Accuracy
  - On-chip Temperature Sensor Accuracy (25~70 °C) +- 2 °C typ.
  - On-chip Temperature Sensor Resolution 1 °C
- Operating Temperature Range -40 °C ~ 85 °C

5.5. SoC Thermal Monitoring

To allow optimal operation and long-term reliability of the VX305H-40G, the Intel® Xeon-D processor must remain within the maximum junction temperature specifications. The maximum operating temperature for the processor die (TJMAX) is respectively 107°C and 104°Cfor 12-core Xeon-D1559 and 8-core Xeon-D1539 processors. The TJMAX temperature is the temperature not to exceed, to avoid entering the throttling mode with reduced performance.

The Xeon-D processor uses the Adaptive Thermal Monitor feature to protect the processor from overheating and includes the following on-die temperature sensors:

- One Digital Thermal Sensor (DTS) for monitoring each processor core
- Catastrophic Cooling Failure Sensor (THERMTRIP#)

These sensors are integrated in the processor and work without any interoperability of the uEFI BIOS or the software application. Thermal Control Circuit allows the processor to maintain a safe operating temperature without the need for special software drivers or interrupt handling routines.

Digital Thermal Sensor (DTS)

The Intel® Xeon-D processor includes on-die Digital Thermal Sensors (DTS), one per processor cores. They can be read via an internal register of the processor.

The temperature returned by the Digital Thermal Sensor will always be at or below the maximum operating junction temperature .Via the Digital Thermal Sensors, the uEFI BIOS or the application software can measure the processor die temperature.

Catastrophic Cooling Failure Sensor

The Catastrophic Cooling Failure Sensor protects the processor from catastrophic overheating.

The Catastrophic Cooling Failure Sensor threshold is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all executions when the junction temperature exceeds this threshold. Once activated, the event remains latched until the VX305H-40G undergoes a power-on restart (all power off and then on again).

This function cannot be enabled or disabled in the uEFI BIOS. It is always enabled to ensure that the processor is protected in any event.

5.6. Thermal Performance

System Level Thermal Performance

To ensure the best possible basis for operational stability and long-term reliability, the VX305H-40G uses a copper heat frame with secondary side retainers as per VITA 48.2. Coupled together with system chassis, thermal management zone is enlarged and optimize to guarantee an active thermal energy dissipation.

The physical size, shape, and construction of the heat frame ensure the lowest possible thermal resistance.

Figure 25: VX305H-40G Thermal Management Zone

Board Level Thermal Performance

The CPU core maximum junction temperature (TJ MAX) is the maximum temperature allowed before entering into throttling mode. TJMAX value depends on Intel Xeon-D1500 part number. The maximum operating temperature for the processor die (TJMAX) is 107°C for Xeon-D1559 processor.

Due to the actual accuracy of the processor internal sensors, and to secure processor full-on mode, the maximum temperature recommended by Kontron to avoid throttling is not 107°C but 102°C.

This core temperature is accessible through the Linux sensors driver. Refer to the Kontron VME/VPX Fedora 28 Remix Release Notes (D215295) for information about the "sensors" command, RC class specific features, and power management.

To ease Xeon D temperature measurements and make sure that processor temperature is within Intel specifications, Intel provide maximum Tcase temperatures (measured at the geometric center of the top surface of the integrated heatspreader)

The user can modify several parameters to optimize board thermal performance:

- Processor load: Kontron advises to keep some margin for real time behavior and stay within 80% of processor load.
- Turbo boost mode: for a better control of thermal performance, it is advised to disable this mode.

Turbo Boost

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency will dynamically increase until the upper limit of frequency is reached. Intel Turbo Boost Technology 2.0 has multiple algorithms operating in parallel to manage current, power, and temperature to maximize performance and energy efficiency.

Intel Turbo Boost Technology 2.0 allows the processor to operate at a power level that is higher than its rated upper power limit (TDP) for short durations to maximize performance.

Learn more about Intel Turbo Boost Technology: http://www.intel.com/technology/turboboost/

The Intel Turbo Boost is handled by the BIOS through the Advanced Power Management Configuration menu. Refer to the AMI BIOS for VX305H-40G - User Reference Manual, section "IntelRCSetup Menu".

⚠CAUTION Exceeding the limits will lock the board: Enabling the turbo mode is tempting, but the board behavior cannot be guaranteed. Even if the CPU chip may adapt quickly to the situation with frequency reduction, this mode is not recommended and it is disabled by default.

VX305H-40G-RCCmC05y1sz Thermal Performance

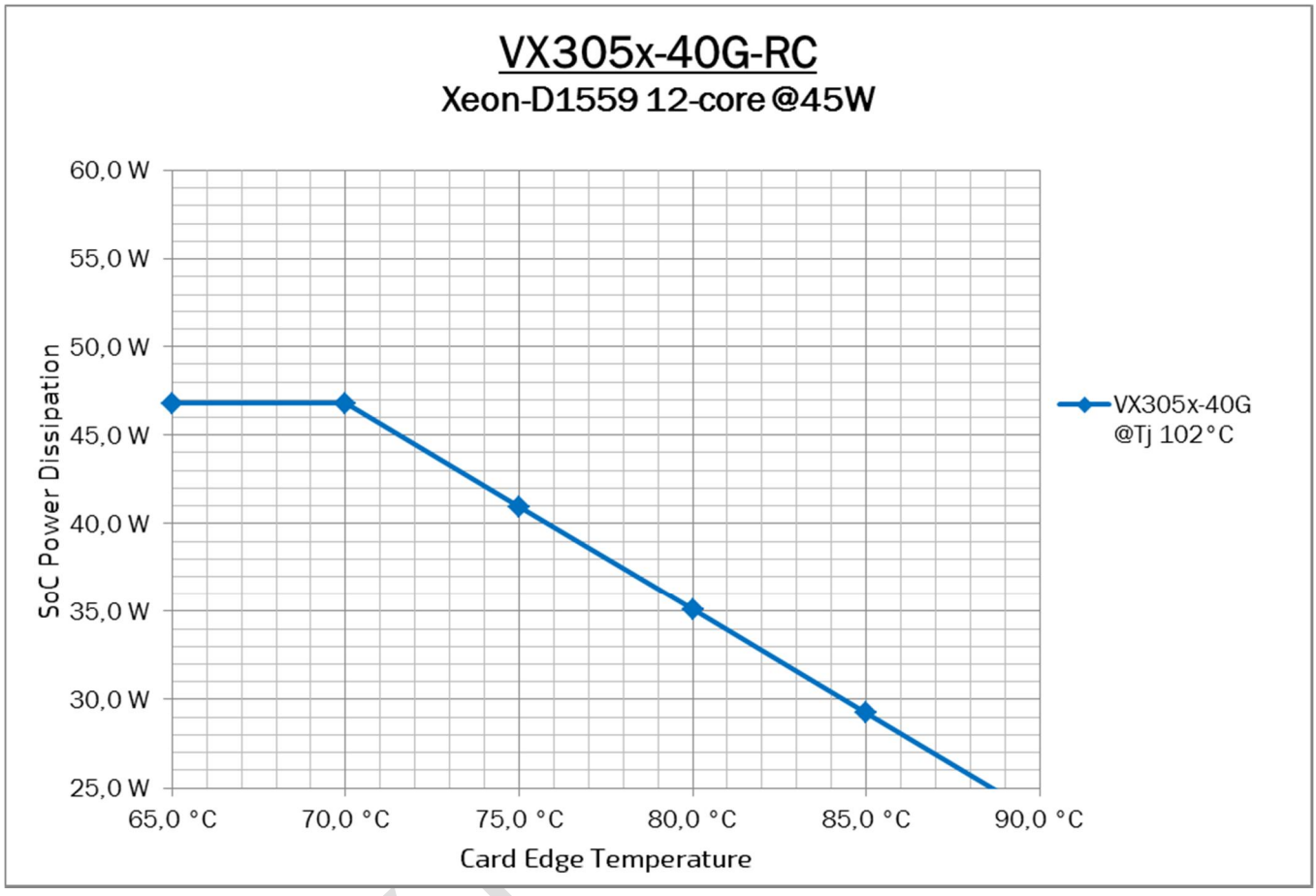
The Figure 26 illustrates the operational limits of the VX305H-40G taking into consideration processor dissipation (TDP) vs. card edge temperature. The core temperature of processor is kept below or equal to 102°C to avoid the processors entering the throttling mode.

The measurements were made based on a 5HP slot (1 inch height) and using Power Thermal Utility (PTU) software from Intel to adjust processor workload.

Table 29: VX305H-40G-RC Functional Points

VX305H-40G-RCCmC05y1sz Product order codes (Processor junction temperature@102°C)		Test conditions
CPU TDP	MEASURED CARD EDGE TEMPERATURE	
35 W	80 °C	PTU test bench. Maximum temperature measured at card edge in the following conditions: full processor performance, maximum processor TDP without CPU throttling. No XMC presence
42 W	74 °C	
45 W	71.5 °C	
47 W	70 °C	

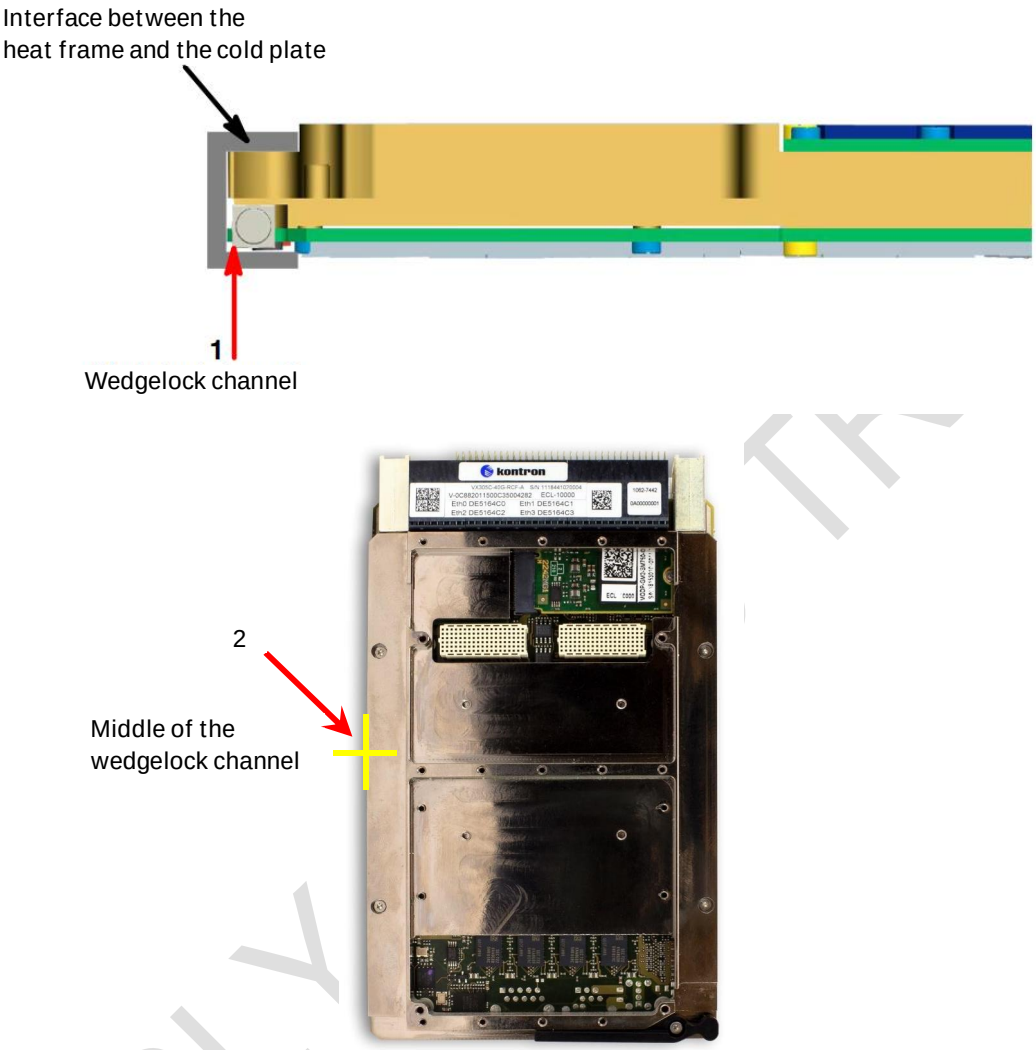
Figure 26: VX305H-40G- RCCmC05y1sz SoC TDP versus Card edge Temperature.



Card Edge Temperature Measurement

The card edge temperature is measured as follows: the middle point in the wedgelock channel on the heat frame. The wedgelock channel is the channel between the edge of the heat frame and the cold wall of the rack. Refer to arrows numbers 1 and 2 in Figure 27.

Figure 27: Measuring the card edge temperature



According to ANSI/VITA 47 standard, the plug-in unit edge surface temperature is measured on the plug-in unit.

6/ Optional Board Features

This section describes the additional features of the VX305H-40G board thanks to optional I/O interfaces. These features are optional and they can be provided on customer demands.

6.1. Overview

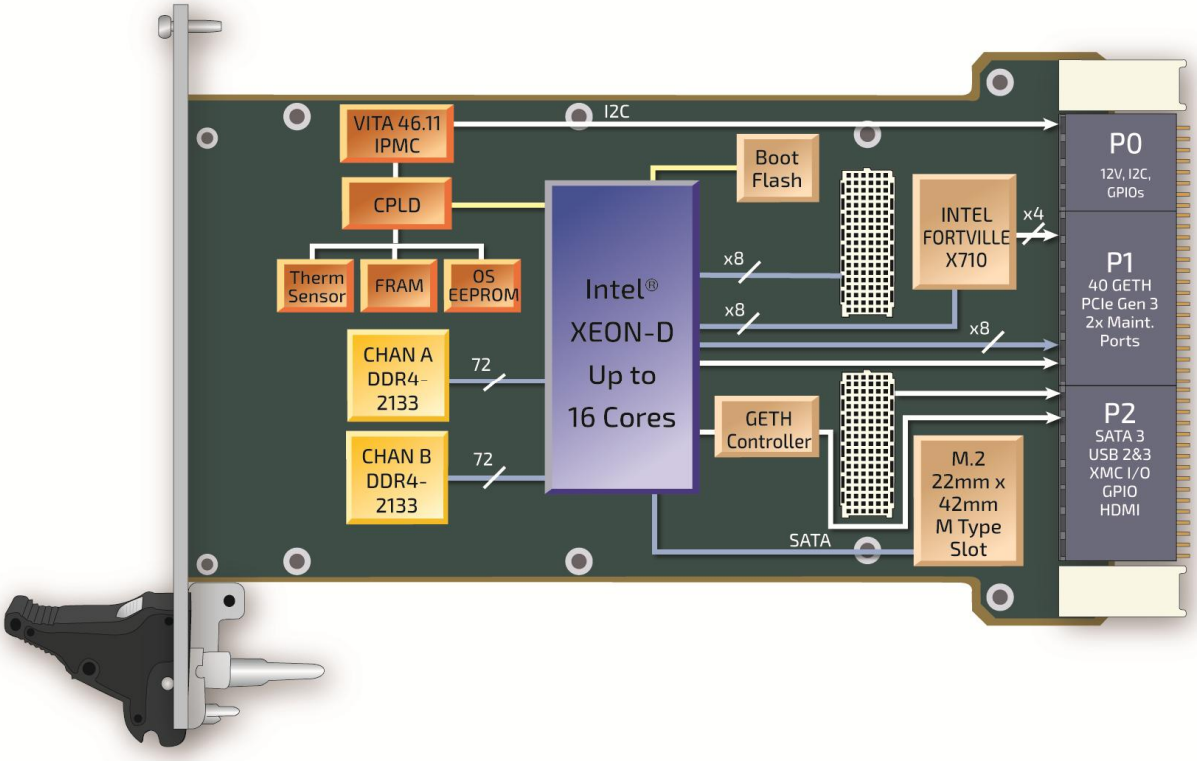
Adding the P2 VPX connector, the VX305H-40G offers additional I/O interfaces such as USB, SATA, XMC IO and 1000Base-T Ethernet on rear. VITA 65 aperture pattern H for optical/coax connectors as per slot profile SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-n is no longer available and it is replaced by VPX P2 connector.

A 2-D graphic M.2 module is also available, based on the Silicon Motion SM750 graphic controller.

Figure 28: VX305H-40G 3U VPX P2 Option Overview

6.1.1. Block Diagram

Figure 29: VX305H-40G Block Diagram with P2 option



6.1.2. Optional Order Codes

Table 30: VX305H-40G Optional Order Codes

Environ-mental Class	Standard Order Codes	Description
RC	VX305H-40G-RC nGC05113z	3U single slot 5 HP (1.0") VPX CPU Blade with Intel® Xeon® D-1500 processor series, conduction cooled, Vita48.2 plug-in type: Type 1, secondary side retainer, P2 VXP connector equipped. Available options: Processor type: n=8: 8-Core D1539, base frequency 1.6 GHz, TDP 35 W n=C: 12-Core D-1559, frequency 1.5 GHz, TDP 45 W Other option: z = P : with PBIT z = Q : with PBIT and Eval Linux on SSD

6.1.3. Optional I/O Interfaces

Additional rear interfaces are compliant with P2 VPX pinout assignment described in the following slot profiles:

- SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16

Adding VPX P2 connector, VX305H-40G is no longer fully compliant with slot profile SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11 as per VITA65.0. VX305H-40G could not be inserted in backplane profile BKP3-TIM12-15.3.6

Table 31: Additional Rear I/O Interfaces

FUNCTION	DESCRIPTION	SEE ALSO
SATA Storage	1 SATA III link	Section 6.4.1 for P2 VPX Connectors Description
USB	2 USB 2.0 and 1 USB 3.0 links (1)	
Gigabit Ethernet	1 1000BASE-T	
XMC IOs	16 single-ended + 8 differential pairs XMC IOs (X16s+X8d)	
GPIOs	3 GPIOs	
Graphics HDMI rear	HDMI/DVI port (depending on ordering code)	

(1) Two USB ports are available on PB-VX3-40G-H-611 RTM, one USB 2.0 port AND one USB 2.0 or USB 3.0 port.

The VS3 VPX backplane power rail (5 Volts) is required when using SATA, HDMI and SFP+ rear I/Os with the PB-VX3-40G-H-611 Rear Transition Module.

HDMI/DVI interface requiring M.2 graphics module is not available by default, it depends on ordering code and on customer request. Contact Kontron support to know availability and ordering information.

6.2. GPIOs

The VX305H-40G features up to 8 GPIOs managed by the CPLD. Refer to the Kontron VME/VPX Fedora 28 Remix Release Notes chapter 11.12 for further details on the GPIO driver.

- 3 GPIOs are available on P2 connector: GPIO2, GPIO3 and GPIO4. See section 6.4.1 “P2 Connector” page 76 for detailed pinout.
- 2 GPIOs are available on P1 connector, GPIO1, GPIO8 (maskable reset). See section 4.3.2 “P1 Connector” page 57 for detailed pinout.
- On customer request, 3 extra GPIOs can be available on P0 connector: GPIO5, GPIO6 and GPIO7. See section 4.3.1 “P0 Connector” page 56 for detailed pinout.

GPIOs availability depends on build option. Please contact Kontron for ordering information and GPIO availability.

GPIO1 and three GPIOs on P0 VPX connector are available on customer request only.

GPIO electrical characteristics: The CPLD features LVCMOS33 cells (0-3V3), drive strength = 8 mA (sink or source), a clamp diode which is not 5V tolerant, an hysteresis of 250mV. The CPLD does not implement any internal pull-up or pull-down.

On the VX305H-40G board, a pull-up of 47 kOhms is connected to GPIO1 to GPIO8.

⚠CAUTION

GPIOs are not 5V tolerant. Maximum voltage on GPIOs is 3.6 V. Absolute maximum voltage is 3.75V and is not suitable for continuous operation. Appropriate voltage reduction (through resistor divider for instance) must be made to avoid permanent damage to the board.

The GPIOs share the same interrupt in the CPLD.

6.3. LED 1 Additional Description

Front panel LEDs description and Activity are respectively defined in Table 21 and Table 22. LED 1 additional meaning, activity and speed of optional 1000Base-T Ethernet interface available adding P2 VPX connector, is described in the following Table 32.

LED1 location is shown in Figure 23: LEDs Front panel

Table 32: LEDs 1 Additional Activity

L1	MEANING
●	1000BASE-T link up
✳	Blinking when activity on the links
●	100M or 10MBASE-T link up
✳	Blinking when activity on the links
●	100BASE-TX/1000BASE-T interface is down

6.4. Connectors

6.4.1. P2 Connector

Table 33: VPX Connector P2 Wafer Assignment

- Legend for Table 33:

SATA	SATA links 3 from PCH	XMCIO_SE1-16	Single ended XMC IO according VITA46.9 X38s
USB port 1 (USB2.0/3.0) USB port 2	USB links from PCH USB link from PCH	XMCIO_DP1-8	Differential XMC IO pins according VITA46.9 X8d
NC	Not connected	ETH2 DA/DB/DC/DD	1000BASE-T link from I210IT GbE controller
GPIOx	General Purpose I/O x	DVI	Graphics HDMI/DVI interface

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	NC	GND	DVI TMDS1-	DVI TMDS1+	GND	DVI TMDS2-	DVI TMDS2+
2	GND	DVI CLK-	DVI CLK+	GND	DVI TMDS0-	DVI TMDS0+	GND
3	NC	GND	DVI PWR	DVI HPD	GND	DVI SDA	DVI SCL
4	GND	USB2 D-	USB2 D+	GND	USB1 D-	USB1 D+	GND
5	NC	GND	USB1 TX-	USB1 TX+	GND	USB1 RX-	USB1 RX+
6	GND	SATA TX-	SATA TX+	GND	SATA RX-	SATA RX+	GND
7	NC	GND	ETH2 DB-	ETH2 DB+	GND	ETH2 DA-	ETH2 DA+
8	GND	ETH2 DD-	ETH2 DD+	GND	ETH2 DC-	ETH2 DC+	GND
9	USB PWR	GND	XMCIO_SE15	XMCIO_SE13	GND	XMCIO_SE16	XMCIO_SE14
10	GND	XMCIO_SE11	XMCIO_SE9	GND	XMCIO_SE12	XMCIO_SE10	GND
11	GPIO2	GND	XMCIO_SE7	XMCIO_SE5	GND	XMCIO_SE8	XMCIO_SE6
12	GND	XMCIO_SE3	XMCIO_SE1	GND	XMCIO_SE4	XMCIO_SE2	GND
13	GPIO3	GND	XMCIO_DP1-	XMCIO_DP1+	GND	XMCIO_DP2-	XMCIO_DP2+
14	GND	XMCIO_DP3-	XMCIO_DP3+	GND	XMCIO_DP4-	XMCIO_DP4+	GND
15	GPIO4	GND	XMCIO_DP11-	XMCIO_DP11+	GND	XMCIO_DP12-	XMCIO_DP12+
16	GND	XMCIO_DP13-	XMCIO_DP13+	GND	XMCIO_DP14-	XMCIO_DP14+	GND
CASE	GND						

* signal active when low

Table 34: VPX Connector P2 Signal Definition

MNEMONIC	SIGNAL DEFINITION
NC	Not connected
ETH2 DA+/-	Ethernet 1000BASE-T: First pair of transmit/receive data.
ETH2 DB+/-	Ethernet 1000BASE-T: Second pair of transmit/receive data
ETH2 DC+/-	Ethernet 1000BASE-T: Third pair of transmit/receive data.
ETH2 DD+/-	Ethernet 1000BASE-T: Fourth pair of transmit/receive data
DVI	DVI/HDMI Port
GND	Ground

MNEMONIC	SIGNAL DEFINITION
GPIOx*	General Purpose I/O x (handled by the CPLD). GPIO3-4 signals are multiplexed with Ethernet LAN1 10G I2C bus signals for rear SFP+ operation. See BIOS User Manuel chapter 6.1.1 for configuration. GPIO is default mode.
SATA RX+/-	Serial ATA. Receive +/-
SATA TX+/-	Serial ATA. Transmit +/-
USB PWR	USB Power limited to 1 Amps
USB1 TX+/- RX+/-	Differential Data transmit and receive of USB1 link
USBx D+/-	Differential Data pair of USB x
XMCIO_SE1-16	Single ended XMC I/O 1 to 16 according to VITA 46.9 X38s
XMCIO_DP1-4/11-14	Differential pairs XMC I/O 1 to 4 and 11 to 14 according to VITA 46.9 X8d

* See section 6.2 - GPIOs -page 75.

6.4.2. XMC J16 Connector Pin Assignment

XMC I/O signals are routed to the VPX P2 connectors according P1w9-X12d+P2w3-X38s+X8d signal assignment defined in VITA 46.9 x12d+x8d for differential pairs (8 pairs) and x38s for single ended (16 last signals).

Table 35: XMC J16 Connector Pin Assignment

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	XMCIO_DP1-	XMCIO_DP1+	NC	XMCIO_DP2-	XMCIO_DP2+	NC
2	GND	GND	NC	GND	GND	NC
3	XMCIO_DP3-	XMCIO_DP3+	NC	XMCIO_DP4-	XMCIO_DP4+	NC
4	GND	GND	NC	GND	GND	NC
5	XMCIO_DP5-	XMCIO_DP5+	NC	XMCIO_DP6-	XMCIO_DP6+	NC
6	GND	GND	NC	GND	GND	NC
7	XMCIO_DP7-	XMCIO_DP7+	NC	XMCIO_DP8-	XMCIO_DP8+	NC
8	GND	GND	NC	GND	GND	NC
9	XMCIO_DP9-	XMCIO_DP9+	NC	XMCIO_DP10-	XMCIO_DP10+	NC
10	GND	GND	NC	GND	GND	NC
11	XMCIO_DP11-	XMCIO_DP11+	NC	XMCIO_DP12-	XMCIO_DP12+	NC
12	GND	GND	XMCIO_SE15	GND	GND	XMCIO_SE16
13	XMCIO_DP13-	XMCIO_DP13+	XMCIO_SE13	XMCIO_DP14-	XMCIO_DP14+	XMCIO_SE14
14	GND	GND	XMCIO_SE11	GND	GND	XMCIO_SE12
15	XMCIO_DP15-	XMCIO_DP15+	XMCIO_SE9	XMCIO_DP16-	XMCIO_DP16+	XMCIO_SE10
16	GND	GND	XMCIO_SE7	GND	GND	XMCIO_SE8
17	XMCIO_DP17-	XMCIO_DP17+	XMCIO_SE5	XMCIO_DP18-	XMCIO_DP18+	XMCIO_SE6
18	GND	GND	XMCIO_SE3	GND	GND	XMCIO_SE4
19	XMCIO_DP19-	XMCIO_DP19+	XMCIO_SE1	XMCIO_DP20-	XMCIO_DP20+	XMCIO_SE2

- XMCIO signals are routed to VPX P2 connectors, see VPX Connector P2 Wafer Assignment - Table 33.
- NC pins are not connected on VX305H-40G board

Table 36: XMC J16 Connector Signals Definition

MNEMONIC	DIRECTION	SIGNAL DEFINITION
XMCIO_DPn+/-	I/O	XMCIO differential pair n
XMCIO_SEn	I/O	XMCIO single-ended signal n

7/ RTM Characteristics

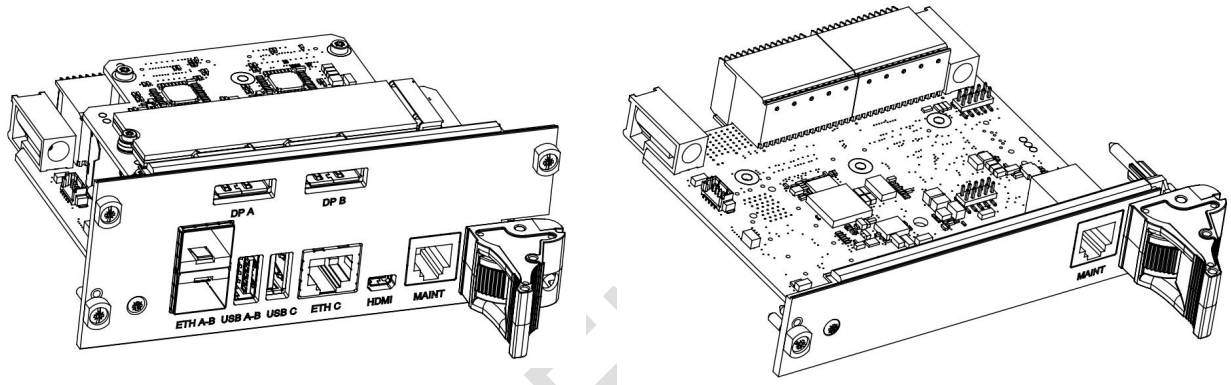
7.1. Introduction

7.1.1. Overview

The Kontron PB-VX3-40G-H-6xx is a 3U VPX Rear Transition Module compliant with the definition of the Rear Transition Module on VPX Standard –VITA 46.10.

It provides rear I/O peripherals connectivity for Kontron VX305H-40G Single Board Computers.

Figure 30: PB-VX3-40G-H-6xx 3U VPX Overview



7.1.2. Ordering information

Table 37: PB-VX3-40G-H-6xx Order Codes

Standard Order Codes	Description
PB-VX3-40G-H-601	3U single slot 5 HP (1.0") VPX Rear Transition Module providing seria lines for standard VX305H-40G boards. Tooling equipment for lab use.
PB-VX3-40G-H-611	3U single slot 10 HP (1.0") VPX Rear Transition Module provides seria lines, USB2.0 and USB3.0, SATA, 1000Base-T Ethernet for VX305H-40G featuring opional P2 VPX connector. Tooling equipment for lab use.

7.1.3. Technical Specification

Table 38: PB-VX3-40G-H-6xx Technical Specification

TECHNICAL SPECIFICATIONS	
Power Specification	
Supply Voltage	5V VS3 VPX, 12V VS1 VPX
Consumption	TDB
USB Ports maximum current	1 A
Mechanical Specification	
Front Panel size	1 slot (5HP) for PB-VX3-40G-H-601 2 slot (10HP) for PB-VX3-40G-H-611
Dimension (mm)	100 x 81.5
Weight (g)	235 (10HP)
Environmental Specification	
Conformal coating	Not available
Operating temperature	10°C/35°C (lab use)

5V VS3 VPX power supply must be provided to PB-VX3-40G-H-611 for full operating. 5V VS3 VPX power supply is not required for PB-VX3-40G-H-601.

7.1.4. Front Panel Interfaces

5HP Front Interfaces

Figure 31: PB-VX3-40G-H-601 Front Panel I/O Interfaces

10HP Front Interfaces

Figure 32: PB-VX3-40G-H-611 Front Panel I/O Interfaces

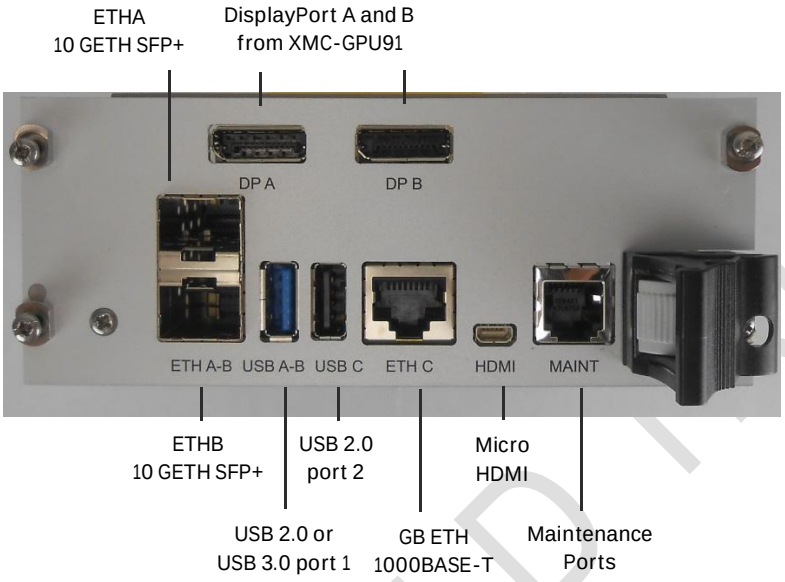


Table 39: PB-VX3-40G-H-6xx Front Panel Technical Specification

Front Panel Name	Description	Comment
USB A-B	USB 3.0 Legacy interface Or USB 2.0 interface (port 1)	
USB C	USB 2.0 interface (port 2)	
ETH A	10 Gigabit Ethernet interface ETH0 implemented on SFP+ cage	Contact Kontron support for availability
ETH B	10 Gigabit Ethernet interface ETH1 implemented on SFP+ cage	Contact Kontron support for availability
ETH C	Gigabit Ethernet interface implemented on RJ-45 connector (1000BASE-T)	
MAINT	COM1/2: maintenance port , EIA-232 or 3.3V LVCMOS level signaling - RJ-12 connector	
HDMI	Graphic: micro HDMI/DVI port	Contact Kontron support for availability
DP A	Graphic: DisplayPort A from XMC-GPU91 (XMCIO)	Contact Kontron support for availability
DP B	Graphic: DisplayPort B from XMC-GPU91 (XMCIO)	Contact Kontron support for availability

⚠CAUTION

Total current of USBs ports (draw simultaneously) must not exceed 1A to avoid RTM damage.

7.2. Installation

The PB-VX3-40G-H-6xx has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

7.2.1. Safety Requirement

The following safety precautions must be observed when installing or operating the PB-VX3-40G-H-6xx. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

This RTM contains electrostatically sensitive devices. Observe the necessary precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

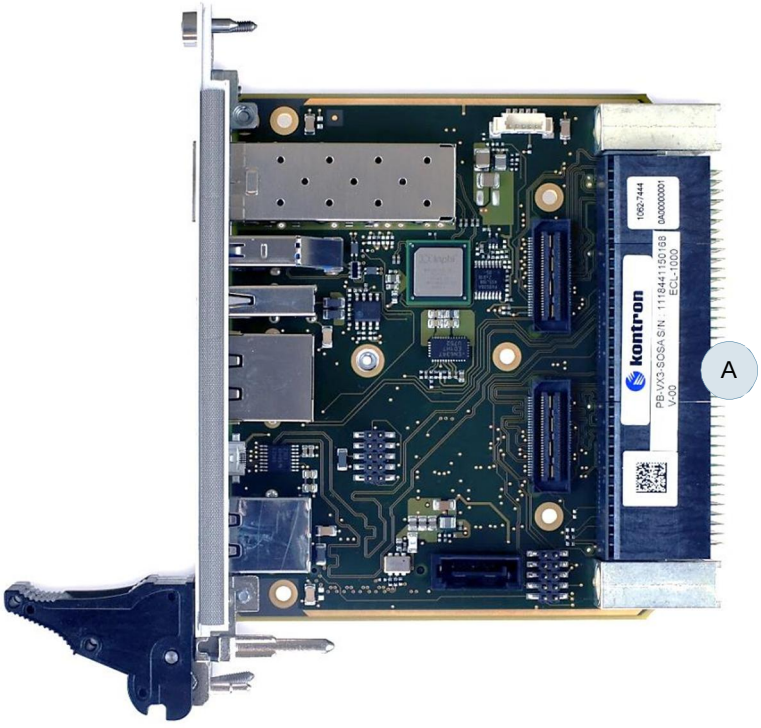
- Do not touch components, connector pins or traces.
- We strongly recommend our customers to work in an environment equipped with anti-static workbenches with professional discharging equipments

7.2.2. Identification

The PB-VX3-40G-H-6xx boards are identified by labels fitted to the VPX connector on the top side of the board.

A "Identification" label: Order Code, Serial Number, Variant, E.C. Level

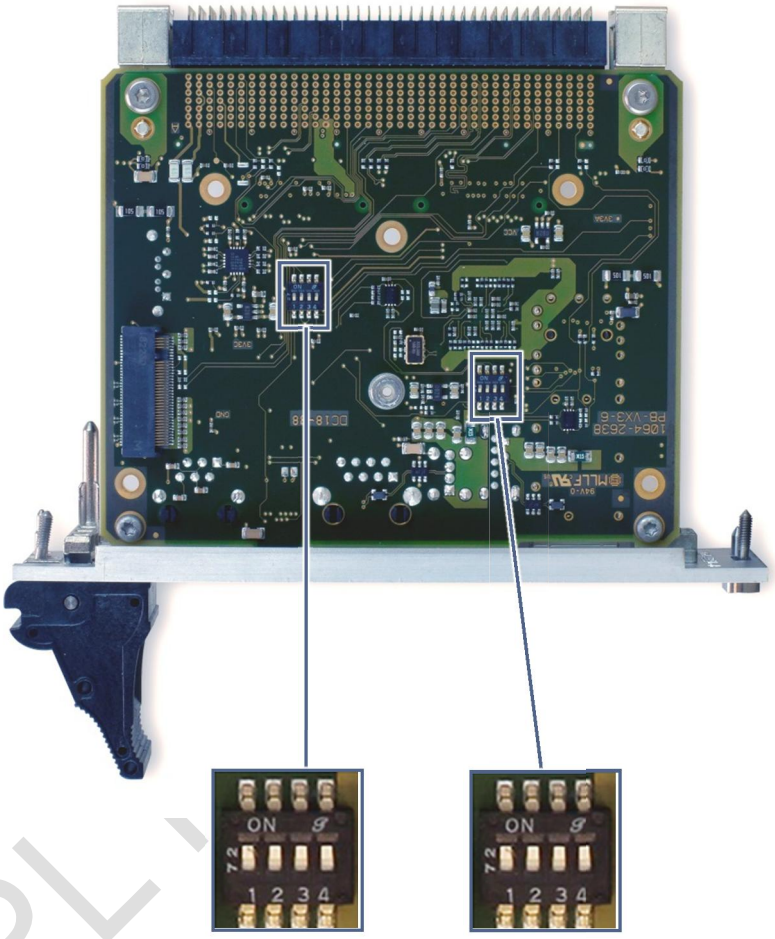
Figure 33: PB-VX3-40G-H-6xx Identification



7.2.3. Microswitches

Two microswitches are available on the PB-VX3-40G-6xx: SW0301 and SW0401

Figure 34: PB-VX3-40G-H-6xx Microswitch Location



SW0401 SW0301

7.2.4. SW0301 Microswitch Description

Table 40: SW0301 Microswitch Description

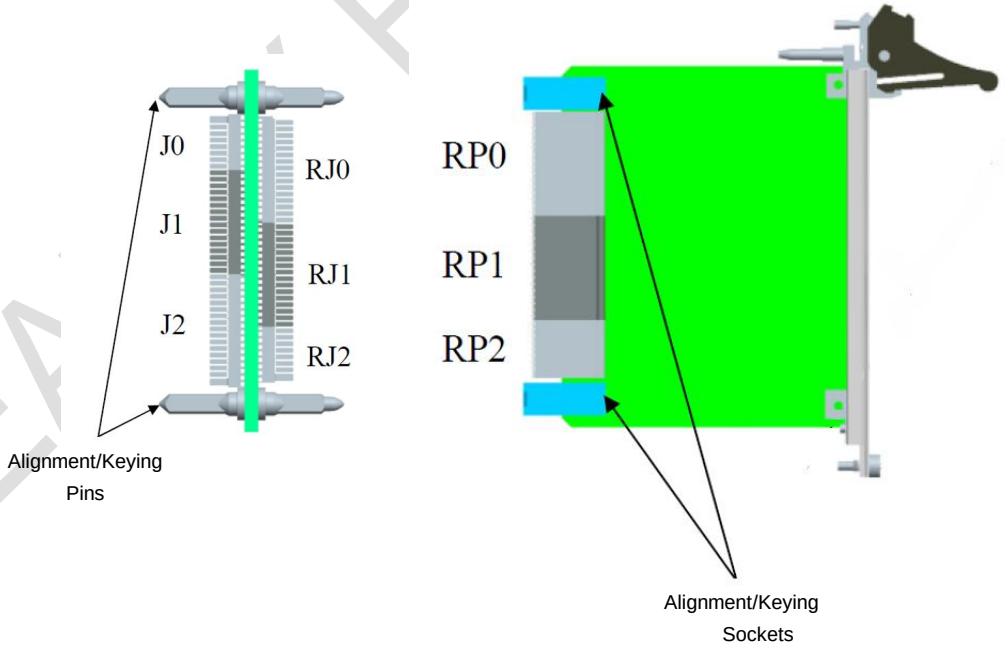
FUNCTION	DESCRIPTION
1 – EEPROM WP	off: The 10Gb Ethernet retimer EEPROM is write protected Default setting on: The EEPROM is not write protected
2 – Reserved	Used for test and debug purpose only. Default setting is OFF
3 – Reserved	Must be OFF
4 – Reserved	Must be OFF

7.2.5. SW0401 Microswitch Description

SW0401 microswitch is used for test and debug purpose only. Default setting is OFF for all switches.

7.2.6. RTM Connectors Identification

Figure 35: Connectors Identification for PB-VX3-40G-H-6xx



7.2.7. Initial Installation Procedure

The following procedures are applicable only for the initial installation of the PB-VX3-40G-H-6xx in a system. Procedures for standard removal operations are found in their respective chapters.

To perform an initial installation of the PB-VX3-40G-H-6xx in a system proceed as follows:

1. Ensure that the safety requirements indicated in section 7.2.1 are observed.

⚠CAUTION Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the RTM is properly configured for operation in accordance with application requirements before installing.

⚠CAUTION Care must be taken when applying the procedures below to ensure that neither the PB-VX3-40G-H-6xx nor other system boards are physically damaged by the application of these procedures.

3. To install the PB-VX3-40G-H-6xx, perform the following:
   a. Ensure that no power is applied to the system before proceeding.
   b. Carefully insert the RTM into the slot designated by the application requirements for the RTM until it makes contact with the backplane connectors.

   When performing the next step DO NOT push the RTM into the backplane connectors. It is recommended to use the ejector handles to seat the RTM into the backplane connectors.

   c. Engage the RTM with the backplane using the ejector handle. When the ejector handle is locked, the RTM is engaged.
   d. Fasten the front panel retaining screws.
   e. Connect all external interfacing cables to the board as required.
   f. Ensure that the RTM and all required interfacing cables are properly secured.

The PB-VX3-40G-H-6xx is now ready for operation.

7.2.8. Standard Removal Procedure

ESD sensitive Device! Precautions are listed in chapter 2.1

To remove the board from the chassis proceeds as follows:

1. Ensure that the safety requirements indicated in section 7.2.1 are observed.

⚠CAUTION

Care must be taken when applying the procedures below to ensure that neither the PB-VX3-40G-H-6xx nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the RTM.
4. Unscrew the front panel retaining screws.
5. Disengage the RTM from the backplane by first unlocking the RTM ejection handles and then by pressing the handles as required until the RTM is disengaged.
6. After disengaging the RTM from the backplane, pull the RTM out of the slot.
7. Dispose of the RTM as required.

7.3. Physical I/O

7.3.1. Front Panel

7.3.1.1. Maintenance Port Connector

The PB-VX3-40G-H-6xx provides two serial maintenance ports, COM1 and COM2 on front panel RJ12 connector. COM1 and COM2 can operate simultaneously in EIA-232 mode only (simplified RX/TX) or in 3.3V LVCMOS level signaling.

Defaults setting are:

- Processor console is redirected on COM1
- Serial mode is simplified serial line mode Rx/Tx only, 115200 bauds

Each serial port is configurable via the BIOS setup menu as EIA-232 or 3.3V LVCMOS level signaling. Each port operates in full duplex mode.

Pin Assignment

Table 41: Serial Connector Pin Assignment

PIN	SIGNAL
1	COM2 TXD
2	Shield
3	COM1 TXD
4	COM1 RXD
5	GND
6	COM2 RXD

Figure 36: Serial Connector

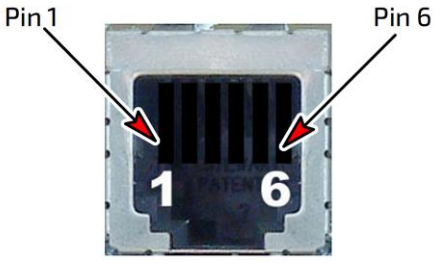


Table 42: Serial Connector Signal Description

MNEMONIC	DESCRIPTION
COM2 RXD	COM2 Receive Data
COM2 TXD	COM2 Transmit data
COM1 RXD	COM1 Receive Data
COM1 TXD	COM1 Transmit Data
GND	Ground
Shell	Chassis Ground

Serial Cable Designation

The Serial cable shall be shielded and shall provide a good shielding continuity between each end.
The Serial cable length should not exceed 10 m.

Serial cable is a RJ-12 (6 pin, 6 conductor). A RJ-12 to DB9/DB25 male or DB9/DB25 female adapter is available from multiple sources, such as:

- Kontron Order Code KIT-2X-RJ12DB9
- Triangle Cable http://www.trianglecables.com/db9m-rj12.html

Table 43: Serial Cable Pin Assignment

DB9 A Pin Connector	DB9 B Pin Connector	Signal	RJ-12 Pin Connector
-	2	TXD1	1
2	-	TXD0	3
3	-	RXD0	4
-	3	RXD1	6
5	5	GND	5

Figure 37: Serial Cable

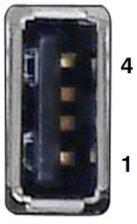
7.3.1.2. USB 2.0 Connector

USB cable shall be compliant to Universal Serial Bus Specification, Revision 2.0.
This USB cable shall have double shielding.
The USB cable length should not exceed 3 m.

Table 44: USB 2.0 Connector Pin Assignment

PIN	SIGNAL	function	I/O
1	VCC (+5V Protected)	VCC	O
2	USB_D-	Differential USB-	I/O
3	USB_D+	Differential USB+	I/O
4	GND	GND	--

Figure 38: USB 2.0 Connector



USB

7.3.1.3. USB 3.0 Connector

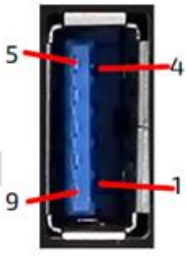
The PB-VX3-40G-H-6xx provides an USB front connector carrying USB 2.0 port and USB 3.0 port USBSS.

USB cable shall be compliant to Universal Serial Bus Specification, Revision 3.0.
This USB cable shall have double shielding.
The USB cable length should not exceed 3 m.

Table 45: USB 3.0 Connector Pin Assignment

PIN	SIGNAL	function	I/O
1	VBUS	+5V Protected by 1.5A fuse	O
2	USB_D-	Differential USB-	I/O
3	USB_D+	Differential USB+	I/O
4	GND	Logic Ground	-
5	STDA_SSRX-	Negative SuperSpeed receiver differential pair	I
6	STDA_SSRX+	Positive SuperSpeed receiver differential pair	I
7	GND_DRAIN	Logic Ground	-
8	STDA_SSTX-	SuperSpeed transmitter differential pair	O
9	STDA_SSTX+	SuperSpeed transmitter differential pair	O

Figure 39: USB 3.0 Connector



7.3.1.4. Gigabit Ethernet Connector

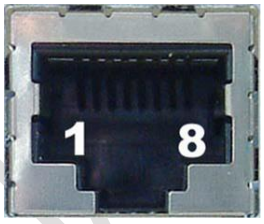
The Ethernet cable shall be CAT6 compliant.
This Ethernet cable shall be S/FTP type at least (Shielded Foiled Twisted Pair), providing shielding continuity between each end.
The Ethernet transmission should operate using a CAT6 cable with a maximum length of 100 m.

The Ethernet connectors are available as RJ-45 connectors with tab down. The interface provides automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

Table 46: Gigabit Ethernet Connector Pin Assignment

pin	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-		I/O	BI_DC+
5	-	-	-		I/O	BI_DC-
6	I	RX-	I	RX-	I/O	BI_DB-
7	-	-	-		I/O	BI_DD+
8	-	-	-		I/O	BI_DD-
Shell	Chassis Ground					

Figure 40: RJ45 Ethernet Connector



7.3.1.5. micro HDMI Connector

Contact Kontron for pin assignment and availability of HDMI feature.

7.3.1.6. Double SPF+ Connector

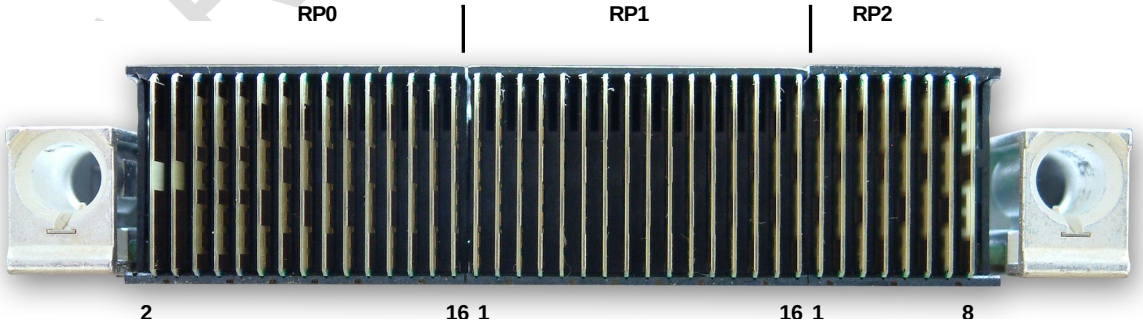
Contact Kontron for pin assignment and availability of double SFP+ cage feature.

7.3.2. Rear I/O Connectors

The PB-VX3-40G-H-6xx Rear Transition Module conducts a wide range of I/O signals through the rear I/O connectors RP0, RP1 and RP2.

- RP0: 15-wafer 7-row mixed connector.
- RP1: 16-wafer 7-row differential connector.
- RP2: 8-wafer 7-row differential connectors.

Figure 41: Rear I/O VPX Connectors



RP0 Wafer Assignment

Table 47: Rear I/O VPX Connector RP0 Wafer Assignment

Legend for Table 47:

IPMB_B/A	IPMB I2C bus	GPIO / SFI	GPIOx and/or SFI I2C management bus
COM1/COM2	Maintenance Ports	ETHx TX/RX	1000BASE-KX Ethernet controller or 10GBASE-KR links 0 and 1 from integrated 10 GbE controller.

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	No wafer						
2	+12V	+12V	+12V	NC	NC	NC	NC
3	+5V	+5V	+5V	NC	+5V	+5V	+5V
4	IPMB_B CLK	IPMB_B DAT	GND	NC	GND	SYSRESET*	NC
5	NC	NC	GND	NC	GND	IPMB_A CLK	IPMB_A DAT
6	NC	NC	GND	NC	GND	NC	NC
7	GPIO7	GND	NC	NC	GND	SFI_SCL (GPIO5)	SFI_SDA (GPIO6)
8	GND	NC	NC	GND	NC	NC	GND
9	NC	GND	NC	NC	GND	NC	NC
10	GND	NC	NC	GND	NC	NC	GND
11	NC	GND	NC	NC	GND	NC	NC
12	GND	NC	NC	GND	NC	NC	GND
13	NC	GND	ETH0 TX-	ETH0 TX+	GND	ETH0 RX-	ETH0 RX+
14	GND	NC	NC	GND	COM1 TXD	COM1 RXD	GND
15	GND	GND	GND	GND	GND	GND	GND
16	GND	ETH1 TX-	ETH1 TX+	GND	ETH1 RX-	ETH1 RX+	GND
CASE	GND						

* signal active when low

Table 48: Rear I/O VPX Connector RP0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
+12V	+12 Volts DC power (VS1 VPX supply). NC (+12V) pins are not connected (VS2 VPX supply)
+5V	+5 Volts DC power (VS3 VPX supply).
GND	Ground
GPIO 5, 6, 7*	General purpose I/O (handled by CPLD). GPIO 5 and 6 not connected by default, and they are multiplexed with Ethernet 10G I2C bus signals for rear SFP+ operation. See BIOS User Manuel chapter 6.1.1 for configuration (GPIO is default mode). Contact Kontron support for availability.
SFI_SCL/SDA	10Gb Ethernet retimer I2C management bus, contact Kontron support for availability.
IPMB A	I2C Bus 0
IPMB B	I2C Bus 1
SYSRESET*	System Reset. Input and open collector output.
COM1	Maintenance port : serial Lines EIA-232 or 3V3 LVCMOS level signaling
ETHx RX+/-	10GBASE-KR or 1000BASE-KX Ethernet x: Receive data +/- (auto negotiation)
ETHx TX+/-	10GBASE-KR or 1000BASE-KX Ethernet x: Transmit data +/- (auto negotiation)
NC	Not connected

RP1 Wafer Assignment

Table 49: Rear I/O VPX Connector RP1 Wafer Assignment

Legend for Table 49:

SATA	SATA link 3 from PCH	GPIOx / Maskable Reset	General Purpose I/O x and maskable reset
PCIe LxRX | LxTX	x8 or 2 x4 PCI-Express	ETH2 DA/DB/DC/DD	1000BASE-T link from I210IT GbE controller
COM2	Maintenance Port	DVI	Graphics HDMI/DVI interface
USB1 USB2	USB 3.0/2.0 link from PCH USB2 2.0 link from PCH		

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	COM2 TXD	GND	PCIe L0-TX-	PCIe L0-TX+	GND	PCIe L0-RX-	PCIe L0-RX+
2	GND	PCIe L1-TX-	PCIe L1-TX+	GND	PCIe L1-RX-	PCIe L1-RX+	GND
3	COM2 RXD	GND	PCIe L2-TX-	PCIe L2-TX+	GND	PCIe L2-RX-	PCIe L2-RX+
4	GND	PCIe L3-TX-	PCIe L3-TX+	GND	PCIe L3-RX-	PCIe L3-RX+	GND
5	GPIO1	GND	PCIe L4-TX-	PCIe L4-TX+	GND	PCIe L4-RX-	PCIe L4-RX+
6	GND	PCIe L5-TX-	PCIe L5-TX+	GND	PCIe L5-RX-	PCIe L5-RX+	GND
7	Maskable Reset*	GND	PCIe L6-TX-	PCIe L6-TX+	GND	PCIe L6-RX-	PCIe L6-RX+
8	GND	PCIe L7-TX-	PCIe L7-TX+	GND	PCIe L7-RX-	PCIe L7-RX+	GND
9	NC	GND	DVI TMDS1-	DVI TMDS1+	GND	DVI TMDS2-	DVI TMDS2+
10	GND	DVI CLK-	DVI CLK+	GND	DVI TMDS0-	DVI TMDS0+	GND
11	NC	GND	DVI PWR	DVI HPD	GND	DVI SDA	DVI SCL
12	GND	USB2 D-	USB2 D+	GND	USB1 D-	USB1 D+	GND
13	NC	GND	USB1 TX-	USB1 TX+	GND	USB1 RX-	USB1 RX+
14	GND	SATA TX-	SATA TX+	GND	SATA RX-	SATA RX+	GND
15	NC	GND	ETH2 DB-	ETH2 DB+	GND	ETH2 DA-	ETH2 DA+
16	GND	ETH2 DD-	ETH2 DD+	GND	ETH2 DC-	ETH2 DC+	GND
CASE	GND						

* signal active when low

For the VX305H-40G boards where the P2 VPX connector is not equipped - standard variant defined in section 1.3.3 – the RP1 wafers 9 to 16 are not connected.

Table 50: Rear I/O VPX Connector RP1 Signal Definition

MNEMONIC	SIGNAL DEFINITION
PCIe Lx-RX+/-	2 x4 PCI Express Link. Receive +/-, gen1, gen2 or gen3 routed to M.2 SSD sockets
PCIe Lx-TX+/-	2 x8 PCI Express Link. Transmit +/-, gen1, gen2 or gen3 routed to M.2 SSD sockets
GPIO1*	Not connected (General Purpose I/O 1 (handled by the CPLD))
Maskable Reset* or GPIO8	Reset input or Optional general purpose I/O 8 (handled by CPLD) (may be left unconnected if not used).
COM2	COM2 Maintenance port : serial Lines EIA-232 or 3V3 LVCMOS level signaling
ETH2 DA+/-	Ethernet 1000BASE-T: First pair of transmit/receive data.
ETH2 DB+/-	Ethernet 1000BASE-T: Second pair of transmit/receive data
ETH2 DC+/-	Ethernet 1000BASE-T: Third pair of transmit/receive data.

MNEMONIC	SIGNAL DEFINITION
ETH2 DD+/-	Ethernet 1000BASE-T: Fourth pair of transmit/receive data
DVI	DVI/HDMI Port
GPIOx*	General Purpose I/O x (handled by the CPLD).
SATA RX+/-	Serial ATA. Receive +/-
SATA TX+/-	Serial ATA. Transmit +/-
USB1 TX+/- RX+/-	Differential Data transmit and receive of USB1 link
USBx D+/-	Differential Data pair of USB x
NC	Not connected
GND	Ground

RP2 Wafer Assignment

Table 51: Rear I/O VPX Connector RP2 Wafer Assignment

Legend for Table 33:

USB PWR	USB 1 and USB 2 power	XMCIO_DP1-8	Differential XMC IO pins according VITA46.9 X8d
GPIOx	General Purpose I/O x	XMCIO_SE1-16	Single ended XMC IO according VITA46.9 X38s

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	USB PWR	GND	XMCIO_SE15	XMCIO_SE13	GND	XMCIO_SE16	XMCIO_SE14
2	GND	XMCIO_SE11	XMCIO_SE9	GND	XMCIO_SE12	XMCIO_SE10	GND
3	GPIO2	GND	XMCIO_SE7	XMCIO_SE5	GND	XMCIO_SE8	XMCIO_SE6
4	GND	XMCIO_SE3	XMCIO_SE1	GND	XMCIO_SE4	XMCIO_SE2	GND
5	GPIO3	GND	XMCIO_DP1-	XMCIO_DP1+	GND	XMCIO_DP2-	XMCIO_DP2+
6	GND	XMCIO_DP3-	XMCIO_DP3+	GND	XMCIO_DP4-	XMCIO_DP4+	GND
7	GPIO4	GND	XMCIO_DP11-	XMCIO_DP11+	GND	XMCIO_DP12-	XMCIO_DP12+
8	GND	XMCIO_DP13-	XMCIO_DP13+	GND	XMCIO_DP14-	XMCIO_DP14+	GND
CASE	GND						

* signal active when low

For the VX305H-40G boards where the P2 VPX connector is not equipped - standard variant defined in section 1.3.3 – the RP2 wafers 1 to 8 are not connected.

Table 52: Rear I/O VPX Connector RP2 Signal Definition

MNEMONIC	SIGNAL DEFINITION
GPIOx*	General Purpose I/O x (handled by the CPLD).
USB PWR	USB Power limited to 1 Amps
XMCIO_SE1-16	Single ended XMC I/O 1 to 16 according to VITA 46.9 X38s
XMCIO_DP1-4/11-14	Differential pairs XMC I/O 1 to 4 and 11 to 14 according to VITA 46.9 X8d
NC	Not connected
GND	Ground

8/ Standard Air-cooled Characteristics

8.1. Overview

The Standard Air-cooled VX305H-40G board is intended to use as be evaluated in lab environment helping the system engineers in the application development before deployment in harsh environment with the ruggedized version.
The VX305H-40G-SA is designed to host XMC in an operational temperature range from +10° C up to +30° C.

Figure 42: VX305H-40G-SA - Overview

VX305H-40G-SA Specificities

The VX305H-40G-SA boards have the same features as the VX305H-40G-RC boards, except for the following items which are fully described in associated sections below:

Table 53: VX305H-40G-SA Specificities

FUNCTION	SEE ALSO
Ordering Information	Section 8.2 page 95
Board Identification	Section 8.3 page 95
Environmental Specifications	Section 8.4 page 95
Mechanical Specifications	Section 8.5 page 95
Peripheral Connectivity	Section 8.6 page 95
Thermal Considerations	Section 8.7 page 96
Installation	Section 8.8 page 97

8.2. Ordering Information

The ordering information of the VX305C-40G-SA boards is detailed in section 1.3.3 - “Ordering Information” – page 20.

8.3. Board Identification

The VX305H-40G-SA boards are identified by labels fitted to the top side to the VPX connector. These labels are at the same location and have the same meaning (except the “Board Identification" label) as the VX305H-40G-RC board labels (refer to the section 2.2 page 31 for more information).

8.4. Environmental Specifications

Table 54: VX305H-40G-SA Environmental Specifications

	VX305C-40G-SA STANDARD AIR-COOLED
Conformal Coating	Optional
Cooling Method	Forced air-cooled
Operating Temperature	10°C to +30°C
Air flow	15 CFM
Storage Temperature	-0° to +55°C

8.5. Mechanical Specifications

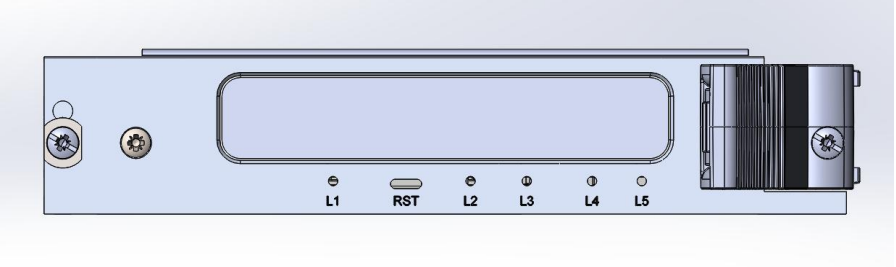
The VX305H-40G-RC boards are built on a multi-layer double Eurocard and conform to the dimensions specified in the IEEE Std 1101.1. The dimensions shown below are in millimeters for general guidance only. For further details about board dimensions, contact Kontron support.

- **Length**: 3U 100 mm max.
- **Depth**: 170.6 mm max.
- **Height**: 1 inch VPX slot compatible

8.6. Peripheral Connectivity

The VX305H-40G-SA board features the same connectors as the VX305H-40G-RC. However, front panel with an ejector handle attaching to the air-cooled board is different from the VX305H-40G-RC, see Figure 43.

Figure 43: VX305H-40G-SA Front Panel



For detailed information about front LEDs and reset, refer to section 1.3.4 page 22.

8.7. Thermal Considerations

The VX305C-40G-SA board is designed for lab environment use. In this environment, the VX305C-40G-SA processing performance is guaranteed across the operating temperature range as defined in Table 54.

The VX305C-40G-SA thermal design is such as, the processor, running in this lab environment does not enter thermal management mode (frequency throttling).

Thermal Regulation

To ensure the best possible basis for operational stability and long-term reliability, the VX305C-40G-SA is equipped with a copper heat sink. Coupled together with system chassis, which provides variable configurations for forced airflow, controlled active thermal energy dissipation is guaranteed.

The physical size, shape, and construction of the heat sink ensure the lowest possible thermal resistance.

The following table illustrates the operational limits of the VX305C-40G-SA taking into consideration processor dissipation vs. ambient air temperature vs. airflow rate.

Table 55: VX305H-40G-SA maximal operating temperature

BOARD	CPU TDP	FREQUENCY	TAMB	MIN AIRFLOW
VX305H-40G Xeon-D1559	45 W	1.5 GHz	30 °C	> 15 CFM
VX305H-40G Xeon-D1539	35 W	1.6 GHz	30 °C	> 12 CFM

⚠CAUTION

Operating the VX30H-40G-SA boards outside its operational limits defined in Table 55 could be result in board damage. Even if the SoC device may adapt quickly to the situation with frequency reduction, the board behavior cannot be guaranteed and this is not recommended.

Turbo Boost

Turbo mode is disabled on VX305H-40G boards by default. This performance mode is not recommended regarding to power dissipation rising. This mode is also disabled by default on VX305H-40G-RC boards.

XMC Hosting

The thermal requirements for a given application, peripherals to be used with the VX305H-40G-SA must also be considered. Devices such as XMC modules which are directly attached to the VX305H-40G-SA must also be capable of being operated at the temperatures foreseen for the application. It may very well be necessary to revise system requirements to comply with operational environment conditions.

In most cases, this will lead to a reduction in the maximum allowable ambient operating temperature or even require active cooling of the operating environment.

⚠CAUTION

As Kontron assumes no responsibility for any damage to the VX305H-40G-SA or other equipment resulting from overheating of the CPU, it is highly recommended that system integrators as well as end users confirm that the operational environment of the VX305H-40G-SA complies with the thermal considerations set forth in this document..

8.8. Installation

8.8.1. Safety Requirement

The following safety precautions must be observed when installing or operating the VX305C-40G-SA. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

This board contains electrostatically sensitive devices. Observe the necessary precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

- Do not touch components, connector pins or traces.
- We strongly recommend our customers to work in an environment equipped with anti-static workbenches with professional discharging equipment

8.8.2. Package Content

The VX305H-40G-SA is packaged with several components, refer to section 2.4 page 35 for the detailed packing contents.

8.8.3. Initial Installation Procedure

The following procedures are applicable only for the initial installation of the VX305H-40G-SA boards in a system. Procedures for standard removal operations are found in their respective chapters.

To perform an initial installation of the VX305H-40G-SA board in a system proceed as follows:

1. Ensure that the safety requirements indicated above are observed.

⚠CAUTION Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing.

⚠CAUTION Care must be taken when applying the procedures below to ensure that neither the VX305H-40G-SA nor other system boards are physically damaged by the application of these procedures.

3. To install the VX305H-40G-SA board, perform the following:
   a. Ensure that no power is applied to the system before proceeding.
   b. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.

When performing the next step DO NOT push the board into the backplane connectors. It is recommended to use the ejector handles to seat the board into the backplane connectors.

   c. Engage the board with the backplane using the ejector handle. When the ejector handle is locked, the board is engaged.
   d. Fasten the front panel retaining screws.
   e. Connect all external interfacing cables to the board as required.
   f. Ensure that the board and all required interfacing cables are properly secured.

The VX305H-40G-SA board is now ready for operation.

8.8.4. Standard Removal Procedure

ESD sensitive Device! Precautions are listed in chapter 2.1

To remove the board from the chassis proceeds as follows:

1. Ensure that the safety requirements indicated in section 8.8.1 are observed.

⚠CAUTION Care must be taken when applying the procedures below to ensure that neither the VX305H--40G nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.
5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.
7. Dispose of the board as required.

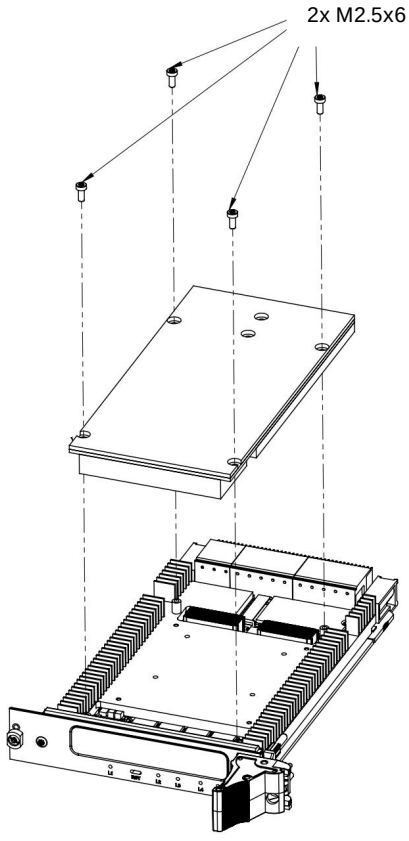
8.8.5. XMC Installation

The XMC installation procedure on a VX305H-40G boards is similar to the VX305H-40G-RC boards. Same caution to plug and to unplug an XMC mezzanine card shall be applied. Refer to section 2.7 page 38.

To install a XMC, proceed as follows:

1. Turn off power
2. Align the XMC connectors. Press to fully engage the XMC.
3. Screw the XMC in place using the four mounting points. See Figure 44 for details.

Figure 44: Air-cooled XMC Installation



⚠CAUTION

The XMC connectors should be mated straight. Align the connectors and when the keys start to enter the keyways, push at the approximate center of the connector into the mating connector until the face of the receptacle cover bottoms on the face of the plug. Because of the asymmetric keying, reverse mating is impossible (the key end of the receptacle cannot be inserted into the non-keyway end of the plug). Both connectors have a lead-in around the perimeter that will allow blind mating.

About Kontron – An S&R Company

Kontron is a global leader in embedded computing technology (ECT). As a part of technology group S&T, Kontron offers a combined portfolio of secure hardware, middleware and services for Internet of Things (IoT) and Industry 4.0 applications. With its standard products and tailor-made solutions based on highly reliable state-of-the-art embedded technologies, Kontron provides secure and innovative applications for a variety of industries. As a result, customers benefit from accelerated time-to-market, reduced total cost of ownership, product longevity and the best fully integrated applications overall.

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