

VX305x

## 3U VPX Computing Node

CA.DT.B25-11e - November 2020

 VX305x - User's Guide

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## Revision History

Publication Title:		VX305x User's Guide
Doc. ID:		CA.DT.B25
Revision	Brief Description of Changes	Date of Issue
11e	Tables 33, 38 and 40 updated. Chap. 2.8 and 2.9: Torque value added for M.2 and XMC screws. Chap. 8 added.	11-2020
10e	Changes between Version 9 and 10 are marked with change bars	08-2019
9e	Changes between Version 8 and 9 are marked with change bars Renumbering of the table and figure references.	03-2019
8e	Updated sections: - 1.1.5 Terminology, Definitions and Abbreviations - 1.3.2 Block Diagram - 1.3.2 Block Diagram - 1.3.3 Ordering Information - Table 1: Order Codes - Table 40: LEDs Activity - Table 45: VX305x-SA Functional Points Synthesis - Table 47: VX305x-RC Environmental Specifications - 7.11 VX305x-RC Covers Removal / Insertion Instructions	07-2018
7e	Updated sections: - 1.3.1 Main Features - 1.3.3 Ordering Information - 1.7 Related Publications New section: - 7 / VX305x-RC Characteristics	06-2017
6e	Updated sections: - 1.3.1 Main Features - Table 3 Rear I/O Interfaces - Table 36 VPX Connector P1 Signal Definition	12-2016
5e	New sections: - 3.8 Reset - 3.9 Write Protect Mode - 3.10 Graphic Option Updated sections: - 2.7 Battery Replacement - 3.3 Battery and Supercap	11-2016
4e	New sections: - 2.9 M2 Module Mechanical Parts References Updated sections: - Table 1: Order Codes - 5.2: Power Specifications - Table 45: VX305x Functional Points Synthesis and associated curves	09-2016
3e	Update of section 2.7 - Battery Replacement	06-2016
2e	Updated sections: - 1.3.1 Main Features / section: Rear Transition Module - 4.2.1 XMC J15 Connector Pin Assignment - 5.2 Power Specifications - 5.3 Board Thermal Monitoring - 5.4 CPU Thermal Monitoring New sections: - 1.3.7 M2 Module List - 5.1 Electrical Specifications	05-2016
1e	Updated sections: - 1.6 - MTBF - 4.4.2 - LEDs Activity	10-2015

0e	Preliminary Version	06-2015
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## Customer Service

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## Symbols

The following symbols may be used in this user guide

<b>⚠ DANGER</b>	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
<b>⚠ WARNING</b>	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
<b>⚠ CAUTION</b>	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
<b>NOTICE</b>	NOTICE indicates a property damage message.
	<p><b>Electric Shock!</b></p> <p>This symbol and title warn of hazards due to electrical shocks (&gt; 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.</p>
	<p><b>ESD Sensitive Device!</b></p> <p>This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.</p>
	<p><b>HOT Surface!</b></p> <p>Do NOT touch! Allow to cool before servicing.</p>
	<p><b>Laser!</b></p> <p>This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.</p>
	<p>This symbol indicates general information about the product and the user guide.</p> <p>This symbol also indicates detail information about the specific product configuration.</p>
	<p>This symbol indicates important information which must be read carefully.</p>
	<p>This symbol precedes helpful hints and tips for daily use.</p>

## For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

### High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

#### **CAUTION**

##### **Warning**

All operations on this product must be carried out by sufficiently skilled personnel only.

#### **CAUTION**



##### **Electric Shock!**

Before installing a non-hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

### Special Handling and Unpacking Instruction

#### **NOTICE**



##### **ESD Sensitive Device!**

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces,

including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

## General Instructions on Usage

In order to maintain Kontron's product warranty and CE compliance, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty and CE compliance.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

## Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.




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Environmental protection is a high priority with Kontron.  
Kontron follows the WEEE directive  
You are encouraged to return our products for proper disposal.

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The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- ▶ Reduce waste arising from electrical and electronic equipment (EEE)
- ▶ Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- ▶ Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- ▶ Improve the environmental performance of all those involved during the lifecycle of EEE

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## 1/Introduction

The Kontron VX305x is a 3U VPX computing blade for data and signal processing application focusing on application domains such as Military & Aerospace, Transportation and Energy/Industry.

The Kontron VPX blade VX305x is the ideal building block for intensive parallel computing workloads where a cluster of Kontron VX305x can be used in switched OpenVPX environments.

The VX305x board comes with EFI BIOS and supports Linux and Windows10. It is covered by Kontron's long term supply program, which guarantees customers multi-year supply of the product beyond its active life.

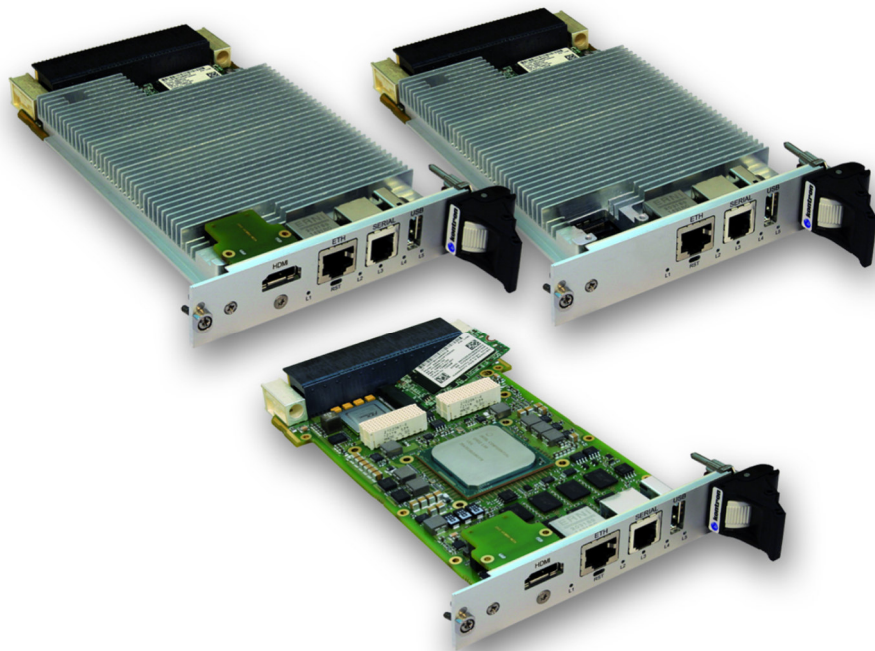
Featuring the Intel® Xeon® processor D1500 Product family, the VX305x is the first 8-core multiprocessing board of the Kontron 3U VPX ecosystem. The highly integrated 8-core architecture with Dual 10 Gigabit Ethernet, high bandwidth PCI Express 3.0, high speed DDR4 memory, and versatile mezzanine options, is consequently SWaP-C optimized and simply the best choice for high performance embedded computing platforms.

VX305x provides two 10GBASE-KR ports and 8 lanes Gen3 PCI Express to the backplane. Kontron VxFabric™ technology provides a TCP/IP protocol over the PCI Express infrastructure towards the application. A 10 Gigabit Ethernet switch and a PCI Express Switch can be complemented with two single star data planes, for 10 GETH and for PCI Express, respectively. A unique API with TCP/IP sockets makes it a powerful, leading edge Multi-CPU computing node architecture.

The M.2 top/bottom slots can be used for storage or for integration of customized personality modules. A 2-D graphic module is available, based on the Silicon Motion SM750 graphic controller.

Front-I/O module options are selectable for DVI/HDMI or Ethernet or other interfaces.

Figure 1: VX305x-SA 3U VPX Overview



## 1.1. Manual Overview

### 1.1.1. Objective

This guide provides general information, hardware instructions, operating instructions and functional description of the VX305x board. The onboard programming, onboard firmware and other software (e.g. drivers and BSPs) are described in detail in separate guides (see section 1.7 "Related Publications").




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This hardware technical documentation reflects the most recent version of the product. The "Release Notes" (see section 1.7 "Related Publications") might help to keep track of potential evolutions.

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Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

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### 1.1.2. Audience

This guide is written to cover, as far as possible the range of people who will handle or use the VX305x-SA, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, system, cabling, grounding and communications.

### 1.1.3. Scope

This guide describes all variants of the VX305x series.

### 1.1.4. Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- ▶ Chapter 1 - Introduction (this chapter)
- ▶ Chapter 2 - Installation
- ▶ Chapter 3 - Additional Board Features
- ▶ Chapter 4 - Physical I/O
- ▶ Chapter 5 - Power and Thermal Specifications
- ▶ Chapter 6 - Backplane Suggestions

### 1.1.5. Terminology, Definitions and Abbreviations

In this document, the term:

- ▶ VX305x -yy will be associated to the 3U VPX board family:
  - ▶ x number of physical processor cores
  - ▶ yy: SA, WA, RA o RC environment class as defined by Kontron standards (see product environmental specifications in this document and product Release Notes)

As an example VX3058-SA means 8-core product specified for SA environmental class.

► **Abbreviations**

TBD	To Be Defined. Information not available at the time this document was released.
TDP	Thermal Design Power
PTU	Power Thermal Utility
PEX	PEX8725 PCIe switch

1.2. VPX Overview

VPX (VITA 46) specifications establish a new direction for the next revolution in bus boards. VPX is an ANSI standard which breaks out from the traditional connector scheme of VMEbus to merge the latest in connector and packaging technology with the latest in bus and serial fabric technology. VPX combines best-in-class technologies to assure a very long technology cycle similar to that of the original VMEbus solutions. Traditional parallel VMEbus will continue to be supported by VPX through bridging schemes that assure a solid migration pathway.

For further information regarding this standards and its use, visit the home page of the VITA - Open Standards, Open Markets (<http://www.vita.com>)

1.3. Board Overview

1.3.1. Main Features

► **Intel<sup>®</sup> Xeon<sup>®</sup> Architecture**

The VX305x-SA computing node is a VPX computing blade for parallel data and signal processing application. The VX305x-SA is the ideal building block for intensive parallel computing workloads where a cluster of VX305x-SAs is used in full mesh or switched OpenVPX environments. Target applications include radar, sonar, imaging systems, airborne fighters, and unmanned aerial vehicle (UAV) radar, as well as rugged multi-display consoles. It is also well suited for transport applications.

The processing node of the VX305x-SA implements a Xeon<sup>®</sup> Processor D coupled with single or dual channel DDR4 memory. The highly integrated Intel<sup>®</sup> QM77 platform hub provides numerous Ethernet, SATA, USB and PCI Express channels. The 3U-format VX305x-SA described in this document is the standard air cooled model.

Frequency of the CPU: see Table 1 - Order Codes

However, the Xeon<sup>®</sup> Processor D is equipped with the Turbo Boost technology, which allows increasing the frequency when the total on chip power allows it.

TECHNICAL SPECIFICATIONS	
Processor	Fifth Generation Intel <sup>®</sup> Xeon <sup>®</sup> D-1500 Processor Family, DDR4 dual channel memory with ECC, 2133 MT/s over 144 bits, up to 32 Gbytes Integrated dual 10G Ethernet controller PCIe x8 ports to VPX and XMC(*), Gen3 capable up to 8 GT/s
Integrated Platform Controller Hub	PCI Express* Base Specification, Revision 2.0 support for up to eight ports with transfers up to 5 GT/s Integrated Serial ATA host controllers with independent DMA operation on up to six ports xHCI USB controller provides support for up to 8 USB ports, of which four can be configured as SuperSpeed USB 3.0 ports Two Integrated serial lines
<b>Onboard Controller</b>	
Gigabit Ethernet	One I210 Ethernet controller connected on front panel or VPX backplane (user selection) for 1000BASE-T operation 2nd I210 Ethernet controller connected on VPX backplane for 1000BASE-T operation, and optionally to the front panel (user selection) if the I/O profile option for "2nd RJ-45 Ethernet 1000BASE-T to the front option" is selected.
Watchdog	PLD-based, timeout ranging from 4 ms to 510s, IRQ, Reset, dual-stages

TECHNICAL SPECIFICATIONS	
RTC	Separated low power RTC with optional onboard battery
System cPLD	Power - on/ off control, Reset control, Local environmental control/monitoring, I2C interfaces to I2C bus IPMB A/B (rear P0), LEDs control, Serial lines multiplexer, Serial VPD and user memories, User and system GPIOs, Internal registers that allow system management
<b>Memory</b>	
System Memory	Up to 16 GB dual channel DDR4 SDRAM running at 2133 MT/s, with ECC, soldered
Flash (uEFI BIOS)	2x16 MB FLASH, with recovery image and uEFI BIOS settings
EEPROM	One serial 256 Kbit EEPROM dedicated to system data One serial 256 Kbit EEPROM dedicated to application data
M.2 SSD option	M.2 SSD module option: Type M, 22 mm x 42 mm
<b>Front Interfaces 5HP (1")</b>	
USB	1x USB 2.0 port
Gigabit Ethernet	1x RJ-45 connector: 10/100/1000BASE-T Ethernet Note: This port is configurable from the BIOS to be routed to the VPX rear connector instead
HDMI (option)	HDMI connector as option. This includes an HDMI front-I/O module and a M.2 mezzanine for 2D graphics. Remark: HDMI front I/O and XMC(*) support are exclusive.
Serial	1x RJ-12 connector: Two EIA-232 interfaces or one EIA-485 interface from CPU, without hardware flow control
LEDs	5 LEDs reporting the board CPU health status and activity
Reset	Reset push button
<b>Onboard Interfaces</b>	
CPU Debug Interface	Bottom Debug connector for Port80, Spare x1 PCIe link with clock
M.2 module interface	Top M.2 slot for a 2D graphic module or a SSD module, compatible with a 12mm stacking height XMC(*) slot. M.2 type M standard pin mapping for SSD module or 2D graphic module option Bottom M.2 slot for SSD module. Supported module: Type M, 22 mm x 42 mm.
XMC(*) Slot option	One x8 PCIe 2 for XMC(*) slot option. X8d+X4s VITA 46.9 XMC(*) I/O routing, 8 differential pairs plus 4 single ended pins For XMC(*) slot option, contact Kontron because of thermal aspects.
<b>VPX Interface</b>	
Slot Profiles	SLT3-PAY-2F2U-14.2.3 SLT3-PAY-1F1F2U-14.2.4 SLT3-PAY-1F1U-14.2.10
Rear I/O via P0/P1/P2	x8 PCIe 3.0, non transparent capability, on P1. Configurable as 1 x8, 2 x4, or 4 x2. 2 SATA 6 Gb/s links on P1, 2 additional SATA 6 Gb/s links on P2 up to 2 USB 2.0 and 1 USB 3.0 port on P1, 1 additional USB 2.0 link on P2 2 serial lines (Rx, Tx only) on P2, for RS-232 or RS-422/485 using dynamic configuration 2 10GBASE-KR as per IEEE802.3 clause 72 or 1000BASE-KX as per IEEE802.3 clause 70 on VPX P1 (auto negotiation) 1 1000BASE-T on P1, 2nd 1000BASE-T on P2 (both front/rear switchable, onboard magnetics) GPIOs on P1: GPIO1, GPIO2/Maskable reset, OpenVPX GDISCRETE1,

TECHNICAL SPECIFICATIONS	
	VBAT, SYSCON. 2x multiplexed GPIO3/4 or SFI I2C on P0 DVI port on P2 as option when a M.2 mezzanine for 2D graphics is present.
Supervisory Functions	Non Maskable RESET NVMRO, Master SMBus and Master/Slave SMBus interfaces for system management. Compatible with Kontron CMB (Monitoring Board), temperature and voltage sensors on the board PCIe optional use of common reference clock feature
Power Supplies	On P0: VS1=12V; VS2 not used; VS3=5V not used; 3.3V_AUX, -12V_AUX for XMC(*) slot option
OS Support	Linux, Windows (ask for VxWorks or other operating systems).
Mechanical size	3U x 160 mm, Slot pitch: 1.00 inch according VITA 48.1 (air cooled) and VITA 48.2 (conduction cooled)

(\*) XMC slot option is on demand only




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All the Flash and non-volatile memories onboard have a write protect mechanism taking into account the NVMRO (Non Volatile Memory read Only) VPX signal.

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### ► Software

Kontron is one of the few compact PCI, VME and VPX vendors providing in-house support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software editors, Kontron is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

Finally, Kontron offers to its customers owners of a maintenance agreement a hotline software support and regular software updates. A dedicated web site is also available for online updates and release downloads.

The VX305x-SA is delivered with the UEFI BIOS from AMI.

The VX305x-SA supports Linux and Windows10 distribution. Refer to BSP Software Release Notes.

Contact Kontron for further information regarding other operating systems and software support.

### ▶ Tooling equipment: PB-VX3-5xx Rear Transition Module

The VX305x-SA supports the PB-VX3-5xx, a 3U VPX Rear Transition Module compliant with the definition of the Rear Transition Module on VPX standard - VITA 46.10.

It offers connectivity on the rear for:

- ▶ 4 HP Version (PB-VX3-501 order code)
  - ▶ one Ethernet SFP+ cage operating at 1 or 10 Gbps.
  - ▶ one Ethernet 1000BASE-T port
  - ▶ one micro HDMI port
  - ▶ two SATA ports up to SATA III (6Gbps)
  - ▶ two serial COM ports
  - ▶ one USB 3.0 / USB 2.0 port
  - ▶ two GPIOs
- ▶ 8 HP Version additional I/O (PB-VX3-511 order code):
  - ▶ 2 additional USB 2.0
  - ▶ 2 additional Sata ports up to SATA III (6Gbps)
  - ▶ 1 additional 1000BASE-T port

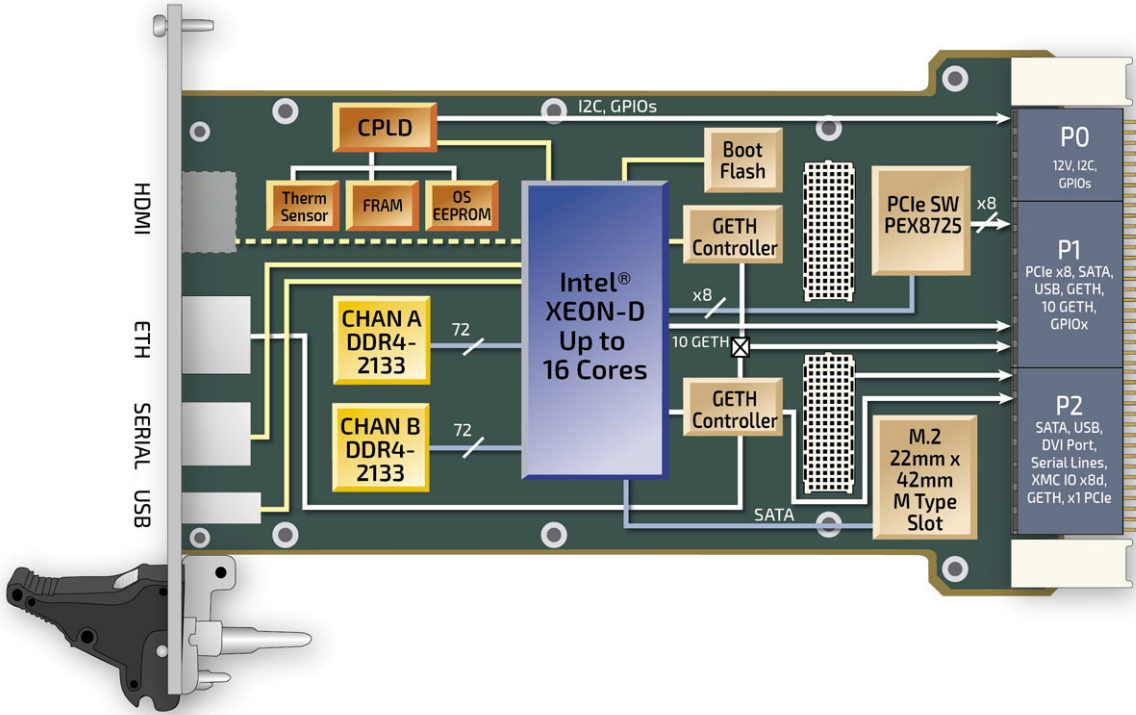
Refer to the PB-VX3-4xx manuals (CA.DT.B03 and CA.DT.B04) applicable to the PB-VX3-5xx except for the front panel I/O differences described. Front and rear connector pin assignments are presented in chapter 8.

Figure 2: PB-VX3-5xx Tooling Equipment



1.3.2. Block Diagram

Figure 3: VX305x-SA Block Diagram



1.3.3. Ordering Information

▶ Manufacturing Options

- ▶ Processor Type: See Table 1 - Order Codes
- ▶ Processor TDP Up to 45 W
- ▶ DDR4 SDRAM Size: 8GB to 32GB
- ▶ BOTTOM 22 mmx42 mm M.2 SATA slots: support 2242-S1-M, 2242-S2-M, 2242-S3-M, 2242-D1-M, 2242-D2-M, 2242-D3-M, 2242-D4-M, SATA link up to 6 Gb/s.
- ▶ TOP 22 mm x 42 mm M.2 slot: 2242-D4-M module with SM750 16 MB graphic controller (MODP-GM2-SM750 module code or idem bottom M.2) Support also same storage modules as define above for the bottom slot.
- ▶ Secure element option: TPM and Approtect.
- ▶ I/O Features: See Table 1 - Order Codes
- ▶ Ruggedization Levels: SA, WA, RA, RC
- ▶ Slot pitch: 1 inch
- ▶ XMC Slot (VITA 61/XMC 2.0 12 mm) XMC slot option is a nonstandard option because of thermal impacts and product restrictions with XMC slot - On demand only

▶ Available Order Codes



Please note that not all order code option combinations are available and released.

Available product order code list can be found in the product datasheet or on the Kontron website.

Table 1: VX305x-SA/WA/RA Order Codes (Air Cooled version)

Environmental Class	Standard Order Codes	Description
SA (0/+55°C)	VX305nSAnmx15y0sz	3U single slot 5 HP (1.0") VPX CPU Blade with Intel® Xeon® D-1500 processor series, fully switched x8 PCIe, Air cooled.
WA (-20/+65°C)	VX305nWAnmx15y0sz	<p><b>Possible Options:</b></p> <p><b>Processor type:</b></p> <p>n=2: 2-Core D-1508, base frequency 2.2 GHz, TDP 25 W                      n=4: 4-Core D-1519, base frequency 1.5 GHz, TDP 25 W                      n=8: 8-Core D1539, base frequency 1.6 GHz, TDP 35 W                      n=A: 8-Core D-1548, frequency 2 GHz, TDP 45 W                      n=C: 12-Core D-1559, frequency 1.5 GHz, TDP 45 W</p>
RA (-40/+70°C)	VX305nRAnmx15y0sz	<p><b>SA/WA/RA Class Heatsink configuration</b></p> <p>x=0: for 25W TDP processors                      x=1: for 35W TDP processors                      x=2: for 45W TDP processors</p> <p><b>Memory size:</b></p> <p>m = 8: 8 GB dual bank DDR4                      m = F: 16 GB dual bank DDR4                      m = G: 32 GB dual bank DDR4</p> <p><b>I/O feature option:</b></p> <p>y = 0: Base I/O                      y = 1: additional front /rear graphics HDMI port                      y = 2: additional front 1000Base-T/RJ45 port</p> <p><b>Security option:</b></p> <p>s = 0 : No hardware secure element and USB port#1 available on VPX P1                      s = 1 : Trusted Platform Module (TPM) equipped (hardware secure element) and USB port#1 available on VPX P1                      s = 2 : TPM and Wibu secure element equipped (Approtect) and USB port#1 not available on VPX P1                      (**)</p> <p><b>Other option:</b></p> <p>z = 0 : standard                      z ≠ 0 : on demand only</p>



(\*\*) Wibu / Approtect feature and USB2.0 port #1 feature (located on P1 wafer B12/C12) are exclusive.

Table 2: VX305x-RC Order Codes (Conduction Cooled version)

Environmental Class	Standard Order Codes	Description
RC	VX305nRCnm <del>x</del> 15y0sz	<p>3U single slot 5 HP (1.0") VPX CPU Blade with Intel® Xeon® D-1500 processor series, fully switched x8 PCIe, conduction cooled, Vita48.                      Plug-in type: Type 2, secondary side retainer.</p> <p><b>Possible Options:</b></p> <p><b>Processor type:</b>                      n=2: 2-Core D-1508, base frequency 2.2 GHz, TDP 25 W                      n=4: 4-Core D-1519, base frequency 1.5 GHz, TDP 25 W                      n=8: 8-Core D1539, base frequency 1.6 GHz, TDP 35 W                      n=A: 8-Core D-1548, frequency 2 GHz, TDP 45 W                      n=C: 12-Core D-1559, frequency 1.5 GHz, TDP 45 W</p> <p><b>RC class Heatsink configuration and performance:</b></p> <p><b>x=0:</b>                      Variants with CPU @25W TDP: -40°C/+85°C @ card edge,                      variants with CPU @35W or @45W TDP : -40°C/+70°C @ card edge</p> <p><b>x=1:</b>                      Variants with D1539: -40°C/+85°C @ card edge, CPU workload below 80% (*)</p> <p><b>Memory size:</b>                      m = 8: 8 GB dual bank DDR4                      m = F: 16 GB dual bank DDR4                      m = G: 32 GB dual bank DDR4</p> <p><b>I/O feature option:</b>                      y = 0: Base I/O                      y = 1: additional front /rear graphics HDMI</p> <p><b>Security option:</b>                      s = 0 : No hardware secure element and USB port#1 available on VPX P1                      s = 1 : Trusted Platform Module (TPM) equipped (hardware secure element) and USB port#1 available on VPX P1                      s = 2 : TPM and Wibu secure element equipped (Approtect) and USB port#1 not available on VPX P1 (**)</p> <p><b>Other option:</b>                      z = 0 : standard                      z ≠ 0 : on demand only</p>



(\*\*) Wibu / Approtect feature and USB2.0 port #1 feature (located on P1 wafer B12/C12) are exclusive.

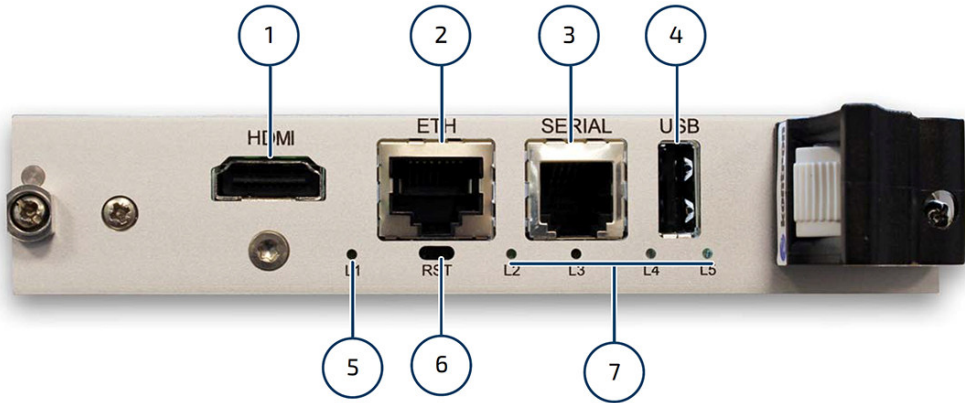


(\*) Ask Kontron for detailed CPU workload and operating conditions. Unless otherwise noted, temperature measurements done with 100% CPU usage.

1.3.4. I/O Interfaces

► Front Interfaces (Models without XMC)

Figure 4: VX305x-SA Front Panel I/O Interfaces



- 1. Optional HDMI
- 2. Gbe ETH
- 3. Serial COM
- 4. USB 2.0
- 5. L1 LED
- 6. Reset CPU
- 7. L2, L3, L4, L5 LEDs

Table 3: Front I/O Interfaces

FUNCTION	DESCRIPTION	SEE ALSO
Serial Ports	COM: 2x EIA-232 or 1x EIA-485 UART interface for CPU on RJ-12 connector.	Section 4.1.1 for Pin Assignment
Gigabit Ethernet	1000BASE-T on RJ-45 connectors: Note: This port is configurable from the BIOS to be routed to the VPX P1 connector instead of the front connector ETH	Section 4.1.2 for Pin Assignment
USB 2.0	USB 2.0 interface	Section 4.1.3 for Pin Assignment
Graphics	HDMI (DVI) option	Section 4.1.4 for Pin Assignment
Reset	Reset push button	Figure 3
LEDs	5 LEDs reporting the board CPU health status and activity	Section 4.4 for LEDs Description

▶ **Rear Interfaces**

Rear interfaces are compliant with the following slot profiles:

- ▶ SLT3-PAY-2F2U-14.2.3
- ▶ SLT3-PAY-1F1F2U-14.2.4
- ▶ SLT3-PAY-1F1U-14.2.10

Figure 5: VX305x-SA Rear I/O Distribution

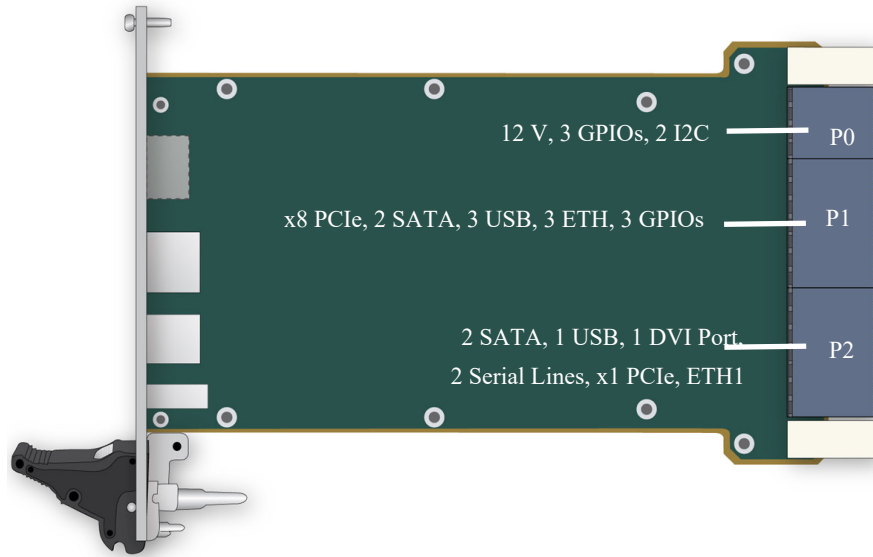


Table 4: Rear I/O Interfaces

FUNCTION	DESCRIPTION	SEE ALSO
PCI Express	<ul style="list-style-type: none"> <li>▶ 1 x8 PCIe, Gen3 capable, non-transparent capability, on P1. Optional use of PCIe common reference clock feature.</li> <li>▶ 1 x1 additional PCIe interface, gen2, on P2</li> </ul>	Section 4.3 for VPX Connectors Description
SATA Storage	<ul style="list-style-type: none"> <li>▶ 2x SATA, Gen III capable, links on P1</li> <li>▶ 2 additional SATA, Gen II capable, links on P2</li> </ul>	
USB	<ul style="list-style-type: none"> <li>▶ Up to 2 USB 2.0 and 1 USB 3.0 links on P1</li> <li>▶ 1 additional USB 2.0 links on P2</li> </ul>	
Gigabit Ethernet	<ul style="list-style-type: none"> <li>▶ 2 SerDes 10GBASE-KR or 1000BASE-KX on P1 (auto negotiation)</li> <li>▶ 1 1000BASE-T on P1</li> <li>▶ 2<sup>nd</sup> 1000BASE-T on P2</li> </ul>	
Serial	<ul style="list-style-type: none"> <li>▶ 2 asynchronous EIA-232/EIA-485 RX/TX serial line, on P2</li> </ul>	
GPIOs	<ul style="list-style-type: none"> <li>▶ 3 User GPIOs on P1, including OpenVPX GDISCRETE1, and MASKABLE RESET</li> <li>▶ 3 additional GPIOs on P0, replacing unused JTAG pins</li> </ul>	
Additional graphics HDMI front/rear	Front HDMI/DVI port and one rear DVI port on P2	
Utilities	On P0 and P1: SYSRESET, SYSCON, 6 Geographical Addresses	Section 4.3 for VPX Connectors Description
Clocks	On P0: 25 MHz Refclock, 1 PPS Auxclock, optional PCIe 100 MHz clock input	
Power Supplies	VS1=12V; VS2 not used; VS3=5V not used; +12V AUX is optional in VITA 46 and not connected on	

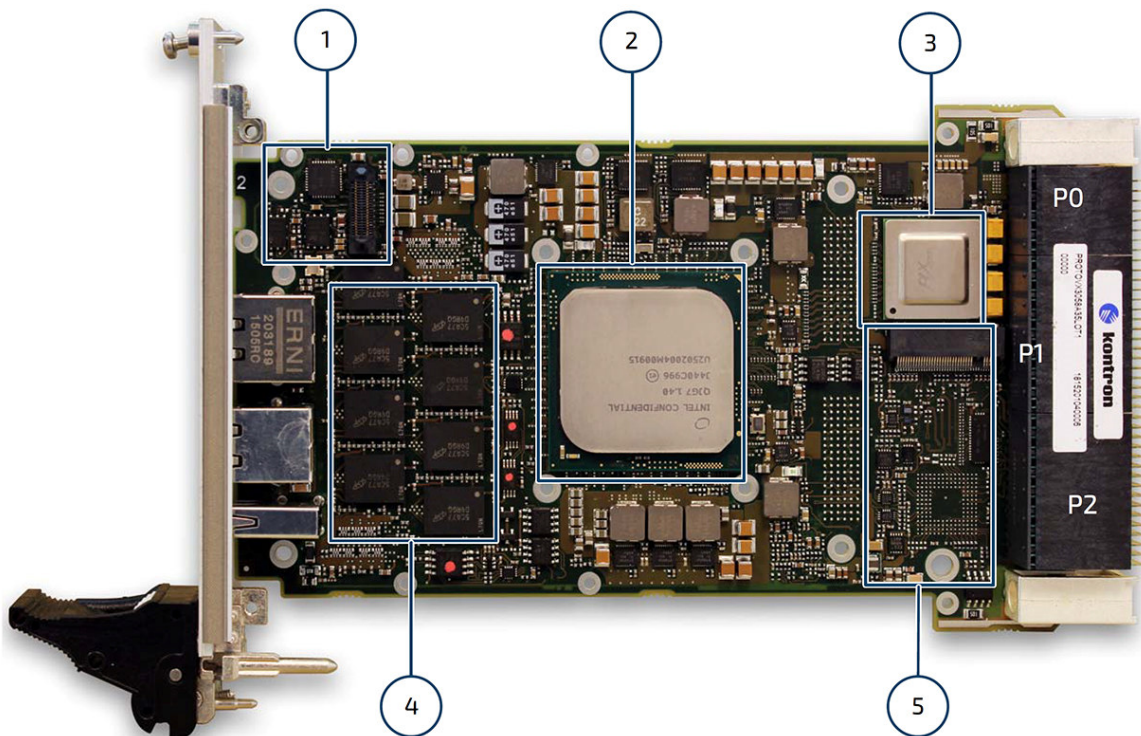
FUNCTION	DESCRIPTION	SEE ALSO
	VX305x-SA. -12V_AUX is optional in VITA 46. It is not used internally on VX305x-SA except for the XMC <sup>(2)</sup> 3.3V_AUX is mandatory in VITA 46. However, if absent, it will be generated internally.	

<sup>(1)</sup> See section 3.1 "The Backplane Power Supplies and their Monitoring" page 43 for tolerance and monitoring.

<sup>(2)</sup> XMC slot option is on demand only - If an XMC mezzanine is to be used on VX305x-SA and needs -12V, -12V\_AUX must be provided on backplane.

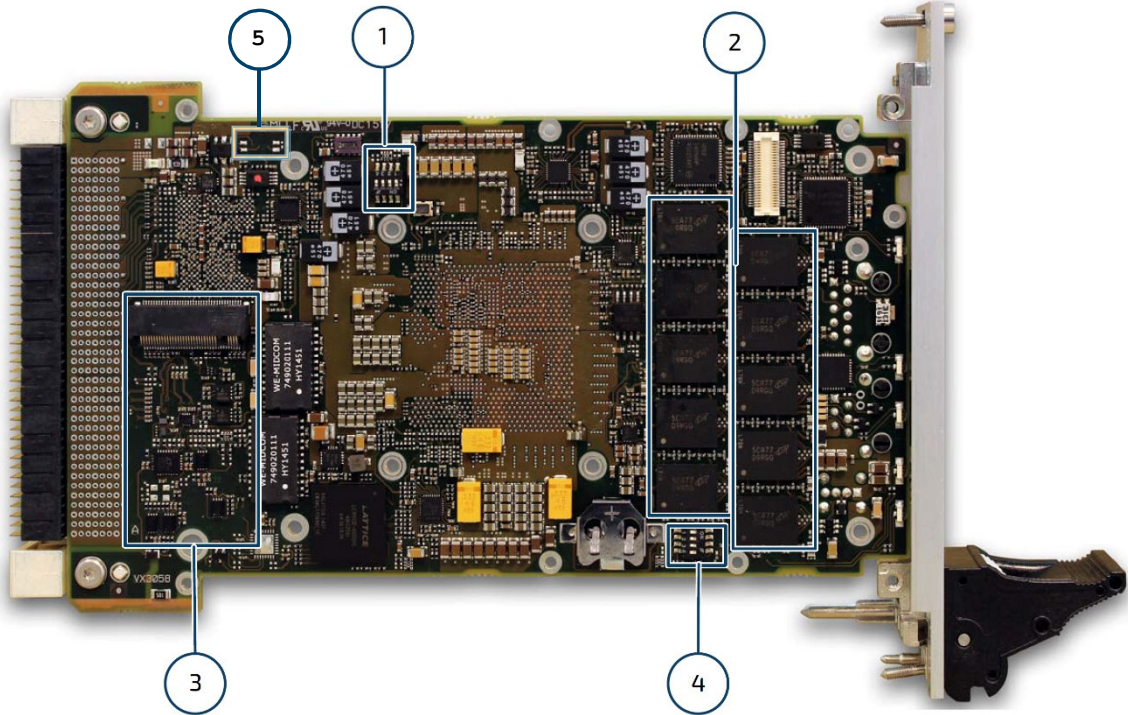
### 1.3.5. Components Layout

Figure 6: VX305x-SA Components Layout (Top view)



- 1. Top I/O Module Slot
- 2. Intel Xeon D
- 3. PCIe SW PEX8725
- 4. DDR4-SDRAM
- 5. Top M.2 Slot

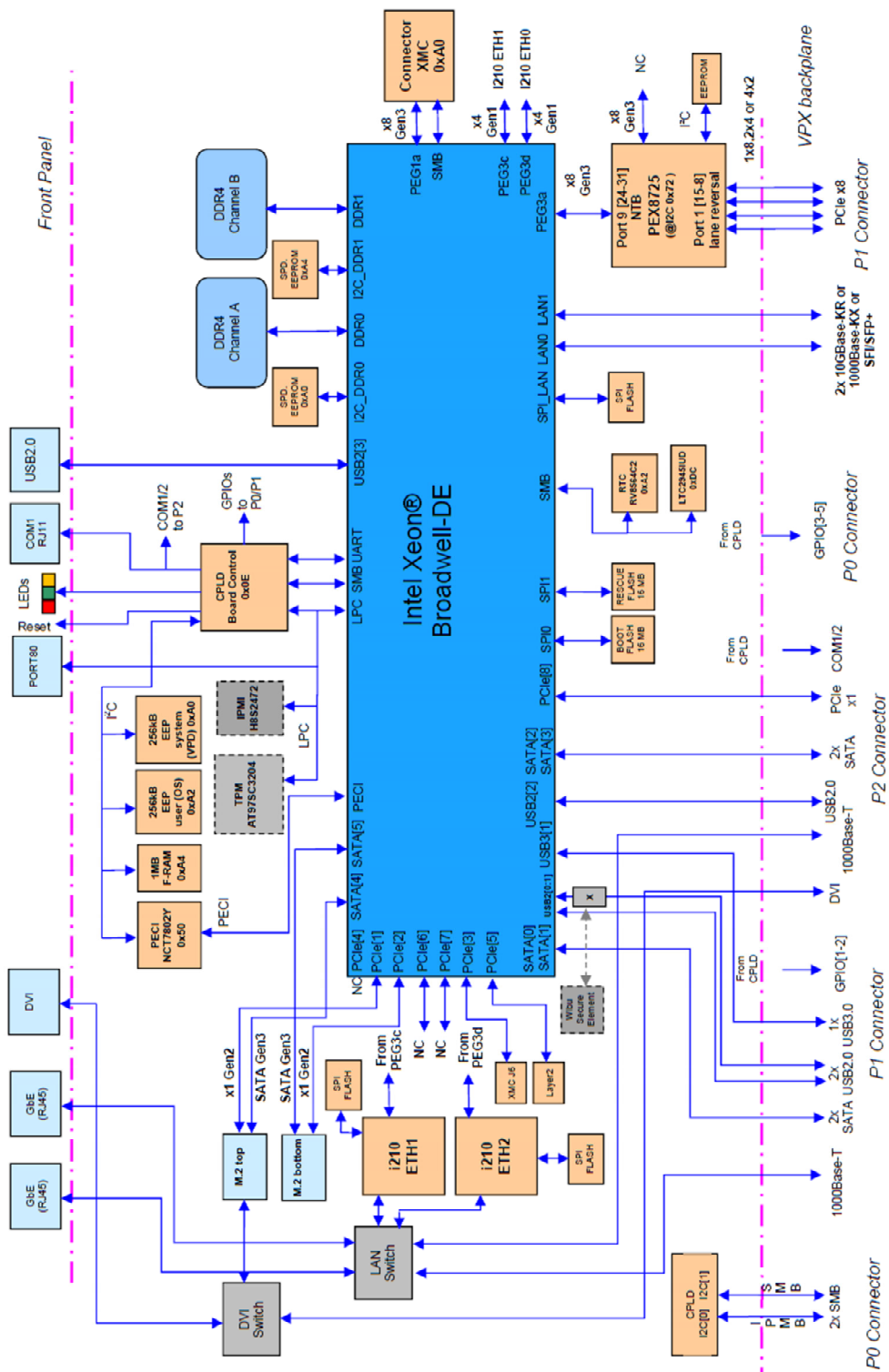
Figure 7: VX305x-SA Components Layout (Bottom view)



- 1. MicroSwitch SW2
- 2. DDR4 SDRAM
- 3. Bottom M.2 Slot
- 4. MicroSwitch SW1
- 5. MicroSwitch SW3

### 1.3.6. Technical Specification

Figure 8: VX305x-SA Functional Block Diagram



### 1.3.7. M2 Module List

Table 5: Non-exhaustive M.2 module list, tested on VX305x M.2 slots

Module Type	Capacity	Memory Technology	Manufacturer	Part Number	Note
SSD SATA, Type M	120 GB	MLC	Intel®	Pro 1500 Series	
SSD SATA, Type M	32 GB	SLC	Unigen	UBM3SMN32H0IS 1-DTC-KF	M2 2242 SATAIII 32GB SLC I-TEMP
SSD SATA, Type M	32 GB	MLC	Transcend	TS32GMTS400	

### 1.4. Environmental Specifications

Table 6: VX305x Air cooled - Environmental Specifications

VX305x 1" single height module heat sink, forced air	SA Standard Commercial	WA Extended Temperature	RA Rugged Air-cooled
Conformal Coating	Optional	Standard	Standard
Airflow	Refer to chapter 5.4	Refer to chapter 5.4	Refer to chapter 5.4
Cooling Method	Convection	Convection	Convection
Operating	0 °C to +55 °C	-20 °C to +65 °C	-40 °C to +70 °C
Storage <sup>(1)</sup>	-40 °C to +85 °C	-45 °C to +100 °C	-50 °C to +100 °C
Vibration Sine (Operating)	1 hour per axis: 5-20 Hz, peak 1.25mm 20-500 Hz, 2g	1 hour per axis: 5-20 Hz, peak 1.25mm 20-500 Hz, 2g	1 hour per axis: 5-19 Hz, peak 2 mm 19 -2000 Hz, 3g
Random (Operating)	1 hour per axis: 5 Hz to 100 Hz, 0.04 g <sup>2</sup> /Hz	1 hour per axis: 5 Hz to 100 Hz, 0.04 g <sup>2</sup> /Hz	1 hour per axis: 5hz to 100Hz, +3dB/octave 100Hz to 1000Hz, 0.04g <sup>2</sup> /Hz 1000Hz to 2000Hz, - 6dB/octave
Shock (Operating)	20 g, 11 ms, half-sine	20 g, 11 ms, half-sine	20 g, 11 ms, half-sine
Altitude (Operating)	-1,500 to 60,000 ft	-1,500 to 60,000 ft	-1,500 to 60,000 ft
Relative Humidity	90 % without condensation (95 % without condensation and with coating option)	95 % without condensation	95 % without condensation

(1) The battery temperature range is -30°C to +70°C.

### 1.5. Board Weight

Table 7: VX305x-SA Weight

SA - Standard Commercial	
VX3058-SA without optional modules	≈ 500 g

## 1.6. MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- ▶ Ground Benign (GB)
- ▶ Air Inhabited Cargo (AIC)
- ▶ Naval Sheltered (NS),
- ▶ Air Rotary Wing (ARW)

### ▶ VX3058-SA881150000 MTBF Data

Table 8: VX3058SA881150000 MTBF Data

MTBF	MILHDBK217F					
	GB (HOURS)		NS (HOURS)		ARW (HOURS)	AIC (HOURS)
	25 °C	40 °C	25 °C	40 °C	55 °C	40 °C
VX3058SA881150000	308 425	209 210	53 545	39 439	6 278	28 356

### ▶ VX3058-SA881151000 MTBF Data

Table 9: VX3058SA881151000 MTBF Data

MTBF	MILHDBK217F					
	GB (HOURS)		NS (HOURS)		ARW (HOURS)	AIC (HOURS)
	25 °C	40 °C	25 °C	40 °C	55 °C	40 °C
VX3058SA881151000	301 934	206 206	53 346	39 331	6 275	28 300

## 1.7. Related Publications

The following publications contain information relating to this product:

Table 10: Related Publications

PRODUCT	PUBLICATION
Standard	
ANSI/VITA 46.0	VPX Baseline Standard - ANSI/VITA 46.0-2007 [R2013]
ANSI/VITA 46.4	PCI Express® on VPX Fabric Connector, Aug 2012
ANSI/VITA 46.6	Gigabit Ethernet Control Plane on VPX, Feb 2013
ANSI/VITA 46.7	Ethernet on VPX Fabric Connector, Mar 2012
ANSI/VITA 46.9	XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules, Nov 2010
ANSI/VITA 46.10	Rear Transition Module for VPX - ANSI/VITA 46.10-2009
ANSI/VITA 65	OpenVPX™ System Specification ANSI/VITA 65-2010 [R2012]
ANSI/VITA 48.1	Mechanical Specification for Microcomputers using REDI Air Cooling
ANSI/VITA 48.2	Mechanical Specifications for Microcomputers using REDI Conduction Cooling Applied to VITA VPX
Serial ATA	Serial ATA 1.0a Specification
Hardware	
VX305x-SA Boards	VX305x-SA Hardware Release Notes CA.DT.B26
Firmware	
VX305x-SA Boards	AMI-BIOS User Reference Manual SD.DT.G50
VX305x-SA Boards	PBIT User's Guide SD.DT.G51
Software	
VX305x-SA Boards	VX305x-SA Software Release Notes SD.DT.G53
Rear Transition Module	
3U-VPX Rear Transition Module	PB-VX3-4xx User's Guide (applicable to PB-VX3-5xx) CA.DT.B03

## 2/Installation

The VX305x-SA has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

### 2.1. Safety Requirements

The following safety precautions must be observed when installing or operating the VX305x-SA. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.



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Special care shall be taken while handling the board: the heat sink can get very hot during operation. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container before the board and heat sink have cooled down to room temperature

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This board contains electrostatically sensitive devices. Observe the necessary precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

- ▶ Do not touch components, connector pins or traces.
  - ▶ We strongly recommend our customers to work in an environment equipped with anti-static workbenches with professional discharging equipment
-

## 2.2. Board Identification

The VX305x-SA boards are identified by labels fitted to the top side of the board. The E.C. Level format is "xxxxxLy" where

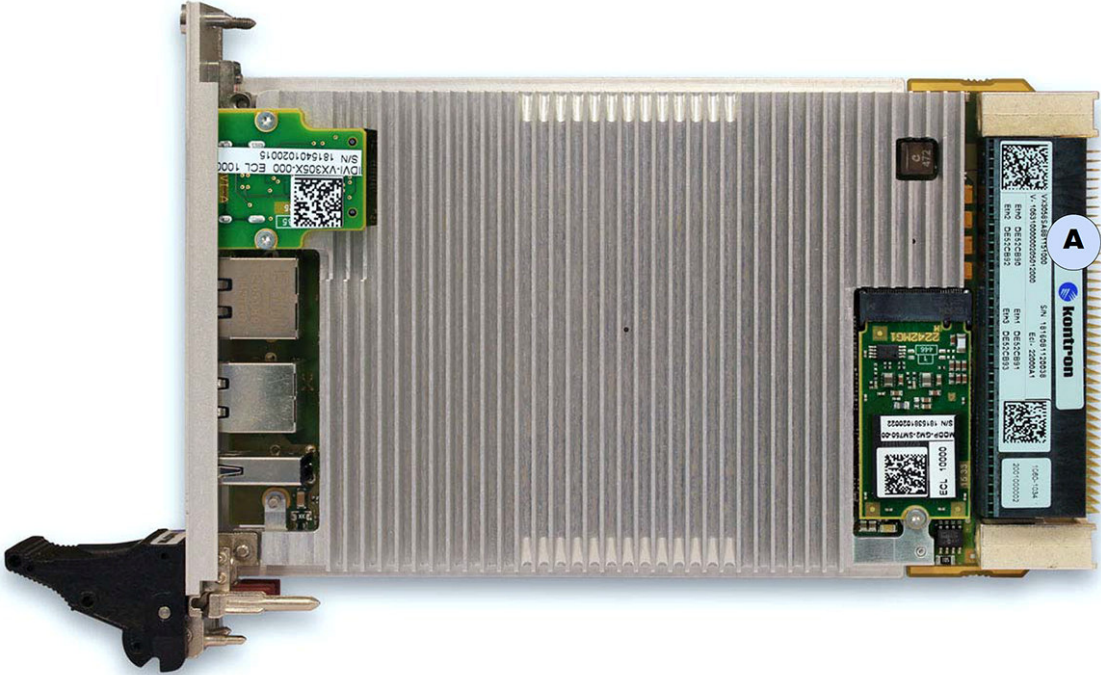
- ▶ The five digits "xxxxx" indicate the board E.C. Level (PCB revision included)
- ▶ "Ly" indicates the mechanical E.C. Level:
  - ▶ letter "L" varies with the environment class ("A" for SA, "B" for WA, "C" for RA and "D" for RC)
  - ▶ digit "y" gives the mechanical E.C. Level.

### ▶ Top Side



"Identification" label: Order Code, Serial Number, Variant, E.C. Level  
Ethernet MAC addresses

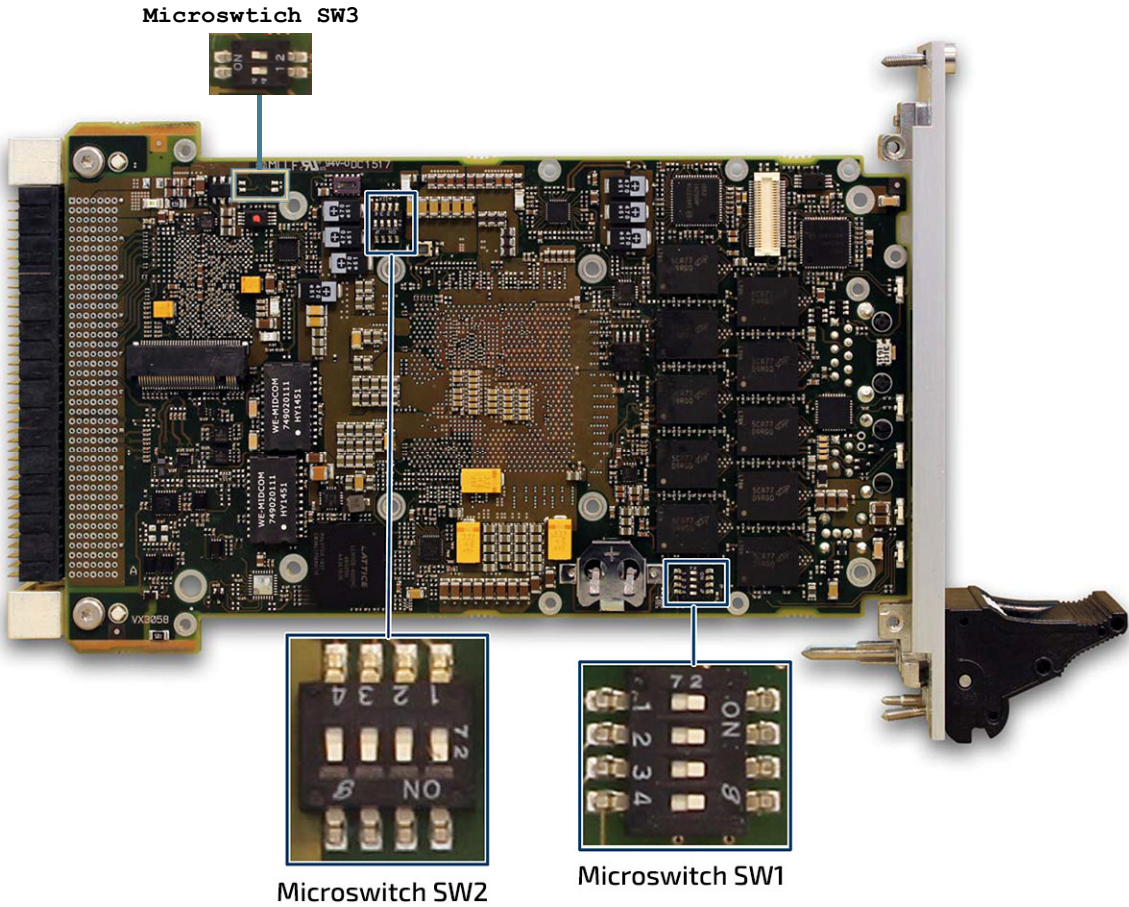
Figure 9: VX305x-SA Identification (Top Side)



### 2.3. Board Configuration

#### 2.3.1. Microswitches

Figure 10: VX305x-SA Board Configuration (Bottom view)



Three microswitches are available on the VX305x-SA: SW1, SW2 and SW3.

#### 2.3.2. SW1 Microswitch Description

Table 11: SW1 Microswitch Description

FUNCTION	DESCRIPTION
1 - Factory Mode	off: Normal Mode on: Factory Mode
2 - Debug Mode	off: Normal Mode on: Debug Mode
3 - VPD Write Protection (VPD and SPD eeprom devices)	off: VPD Write protected on: VPD Writes are allowed
4 - User Write Protection (User FRAM device)	off: User FRAM writes are allowed on: User FRAM write protected

### 2.3.3. SW2 Microswitch Description

Table 12: SW2 Microswitch Description

FUNCTION	DESCRIPTION
1 - System Boot Flash	off: Normal Mode on: Rescue Mode
2 - BIOS Failsafe	off: Normal Mode on: BIOS Failsafe Mode
3 - PCIe Switch Failsafe Mode	off: Normal Mode on: PCIe Switch Failsafe Mode
4 - Force PROCHOT	off: Standard Mode on: Processor PROCHOT force to low state

### 2.3.4. SW3 Microswitch Description

Table 13: SW3 Microswitch Description

FUNCTION	DESCRIPTION
1 - Reserved	off: Normal Position
2 - Reserved	off: Normal Position

## 2.4. Package Content

The VX305x-SA is packaged with several components. The packing contents of the VX305x-SA Series may vary depending on customer requests.

- ▶ CPU Module:
  - ▶ Order Code: see section 1.3.3 "Order Code Table" :
    - ▶ Processor specifications differ depending on Order Code.
    - ▶ Heat sink assembled on the board.
- ▶ Rear Transition Module:
  - ▶ Order Code: see section 1.3.3 "Order Code Table".

## 2.5. Initial Installation Procedures




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ESD sensitive Device! Precautions are listed in chapter 2.1

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The following procedures are applicable only for the initial installation of the VX305x-SA in a system. Procedures for standard removal operations are found in their respective chapters.

To perform an initial installation of the VX305x-SA in a system proceed as follows:

1. Ensure that the safety requirements indicated in section 2.1 page 31 are observed.

### CAUTION

CAUTION: Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the VX305x-SA see Chapter 5. For the installation of VX305x-SA specific peripheral devices and Rear I/O devices refer to the appropriate sections in current Chapter.

### NOTICE

Care must be taken when applying the procedures below to ensure that neither the VX305x-SA nor other system boards are physically damaged by the application of these procedures.

3. To install the VX305x-SA perform the following:
  - a. Ensure that no power is applied to the system before proceeding.

### CAUTION

CAUTION: When performing the next step, DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

- b. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.
- c. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
- d. Fasten the front panel retaining screws.
- e. Connect all external interfacing cables to the board as required.
- f. Ensure that the board and all required interfacing cables are properly secured.

The VX305x-SA is now ready for operation. For operation of the VX305x-SA, refer to appropriate VX305x-SA specific software, application, and system documentation.

## 2.6. Standard Removal Procedure



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ESD sensitive Device! Precautions are listed in chapter 2.1

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To remove the board from the chassis proceed as follows:

1. Ensure that the safety requirements indicated in Section 2.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

---

**CAUTION**

CAUTION: Care must be taken when applying the procedures below to ensure that neither the VX305x-SA nor system boards are physically damaged by the application of these procedures.

---

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.
5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.

---

**CAUTION**

CAUTION: Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

---

7. Dispose of the board as required.

## 2.7. Battery Replacement



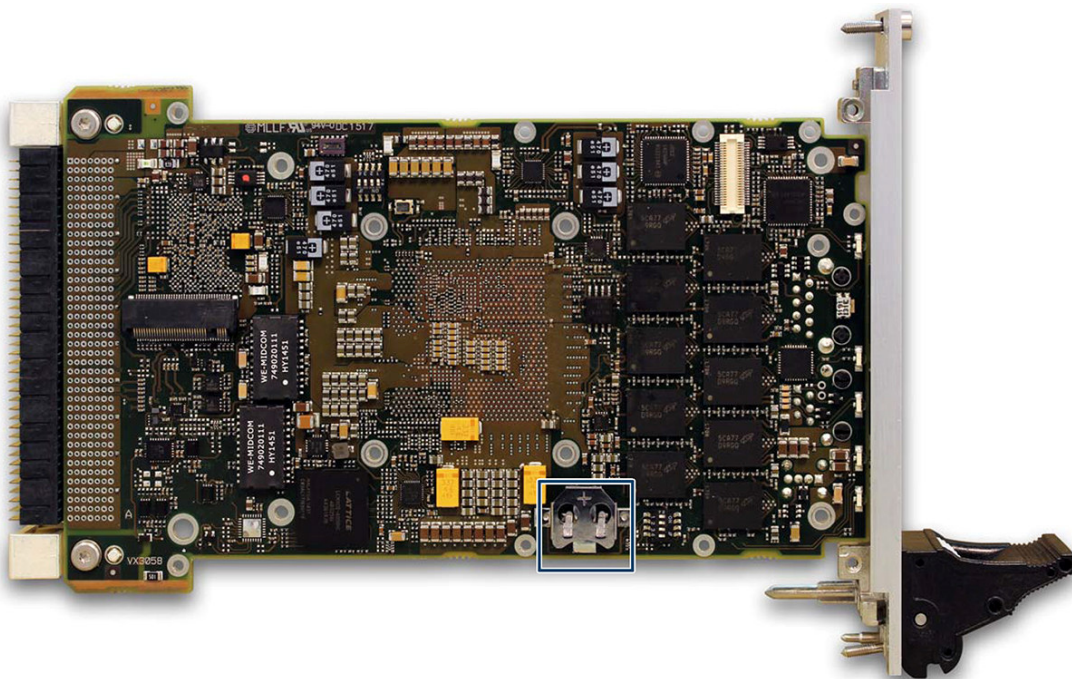
ESD sensitive Device! Precautions are listed in chapter 2.1

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. The battery is used to run a time of day clock during the absence of power. Operation without the battery is possible but the date and time will not be retained in the absence of power. Alternatively, the VPX VBAT signal on P0 can provide a 3.3V voltage from the backplane to retain the date and time.

To replace the battery, proceed as follows:

- ▶ Turn off the power.
- ▶ Remove the board from the chassis.
- ▶ Get the battery outside of its holder:

Figure 11: Battery Replacement on VX305x-SA Board



- ▶ Place the new battery in the socket with the plus pole facing upwards.

### CAUTION

Danger of explosion when replacing with wrong type of battery. Replace only with the same or equivalent type recommended by the manufacturer. The lithium battery type must be UL recognized.



Do not dispose of lithium batteries in general trash collection. Dispose of the battery according to the local regulations dealing with the disposal of these special materials, (e.g. to the collecting points for dispose of batteries).

### NOTICE

Reference of the battery used on the VX305x-SA: RENATA CR1220 MFR  
The design of an electronic circuit powered by a component class battery requires the designer to consider two interacting paths that determine a battery's life: consumption of active electrochemical components and thermal wear-out.

## 2.8. XMC Module Insertion / Removal Instructions



---

XMC slot option is a nonstandard option because of thermal impacts and product restrictions with XMC slot - on demand only.

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### NOTICE

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**Apply "Loctite 222e" threadlock on each screw during re-assembling.**

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ESD sensitive Device! Precautions are listed in chapter 2.1

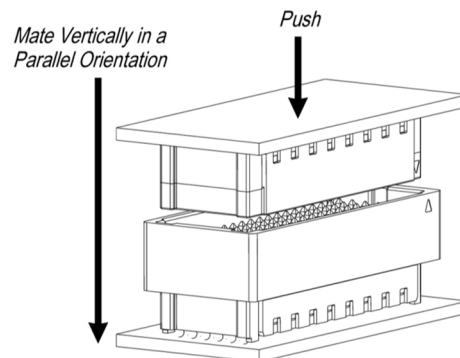
---

### ▶ Mating

These connectors should be mated straight. Align the connectors and when the keys start to enter the keyways, push at the approximate center of the connector into the mating connector until the face of the receptacle cover bottoms on the face of the plug. Because of the asymmetric keying, reverse mating is impossible (the key end of the receptacle cannot be inserted into the non-keyway end of the plug). Both connectors have a lead-in around the perimeter that will allow blind mating.

Torque is 0.25 N.m for M2.5 screws.

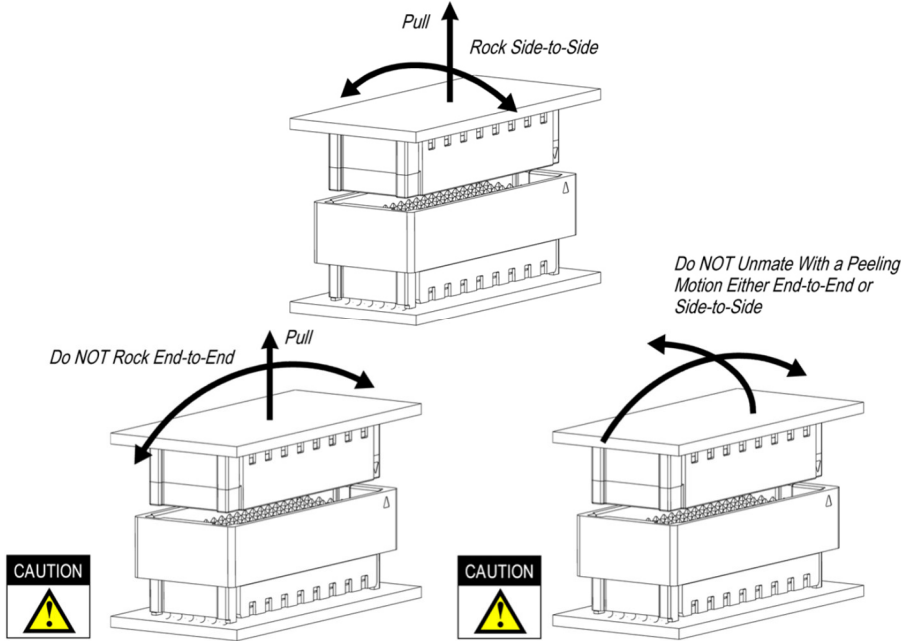
Figure 12: XMC Module Insertion



► **Unmating**

These connectors can be unmated by pulling them straight apart or by “rocking” the connectors from side-to-side while pulling them apart.

Figure 13: XMC Module Removal



## 2.9.M.2 Module Insertion / Removal Instructions



ESD sensitive Device! Precautions are listed in chapter 2.1

### NOTICE

Apply "Loctite 222e" threadlock on each screw during re-assembling.

#### ▶ Top/Bottom supported M.2 Module Type

M.2 sockets can host the following module types: 2242-XX-M with XX = S1, S2, S3, D1, D2, D3, D4.



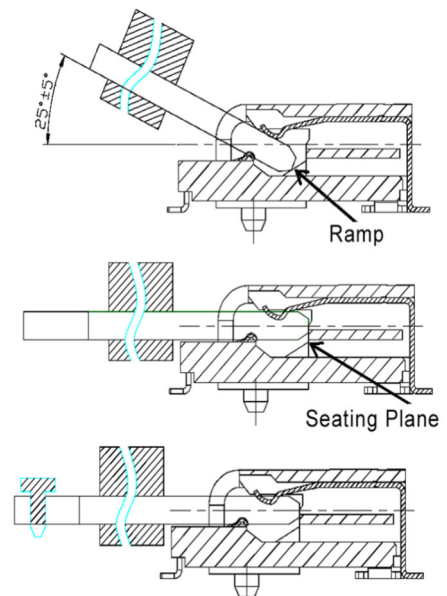
The M.2 bottom socket is not compliant with D5 form factor.

#### ▶ M.2 Module Insertion Process

Process

1. Insert the module with angle  $25^{\circ} \pm 5^{\circ}$  until module touch HSG ramp.
2. Rotate the module to horizon by hand and make sure the card's edge touch HSG seating plane.
3. Fix the module with PCB by screw by hand. Torque is 0.14 N.m for M2 screws.

Figure 14: M.2 Module Insertion



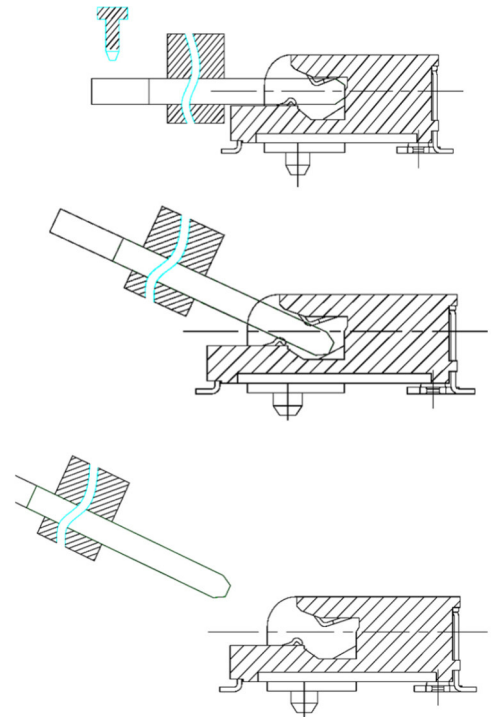
## ▶ M.2 Module Removal Process

Process

1. Loosen the screw by hand and the module will be rotated automatically due to connector contact's counterforce at the same time.

2. Take away the module by hand.

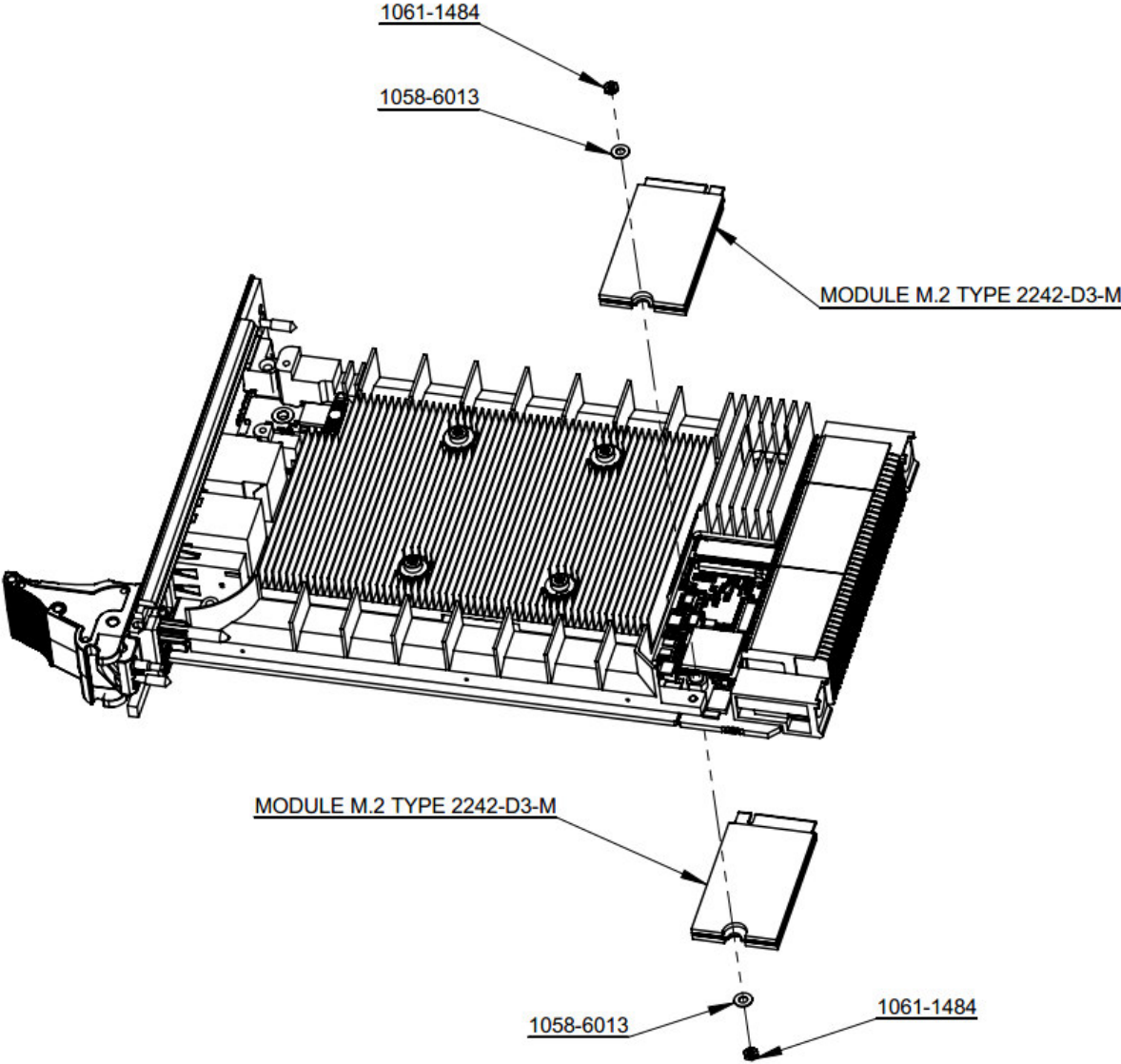
Figure 15: M.2 Module Removal



► **M2 Module Mechanical Parts References**

M.2 module mounting must be done using the following mechanical information.

Figure 16: M2 mechanics



**NOTICE**

Apply "Loctite 222e" threadlock on each nut during re-assembling.

2.10. Software Installation

The installation of all onboard peripheral drivers is described in detail in the relevant Driver Kit files or Board Support Packages (BSP).

The installation of an operating system is dependent of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.

## 3/Additional Board Features

### 3.1. The Backplane Power Supplies and their Monitoring

The VITA46.0 standard specifies the backplane power supplies VS1 as follows:

- ▶ VS1: 12 V +/- 5 % inclusive of ripple ( 11.4 V to 12.6 V).

At Power On, the VPX VS1 system power supply ramp-up phase must be between 20 and 150 msec.

VPX +3.3V\_AUX power supply is optional.

To ensure a valid Power Off, VS1 should remain at 0V for at least one second.

The voltage sensor NCT7802Y by Nuvoton is programmed by BIOS to monitor VS1 and asserts the signal PLD\_PECI\_ALERT\_n whenever either voltage gets out of its VITA 46 specified range. This alert is routed to a maskable interrupt in the cPLD. There is no setup or UEFI command to modify the thresholds value in BIOS.

A second voltage sensor, the LTC2913 by Linear Technology monitors these voltages with a 10 % tolerance. The thresholds are set by hardware on the board. Undervoltage and overvoltage conditions on VS1 are reported to the cPLD which in turn shuts down all VX305x-SA internal power supplies. There is no mechanism for masking these alerts.

### 3.2. RTC, Watchdog, Timers

#### 3.2.1. Real-Time Clock (RTC)

Two Real Time Clocks (RTC) are available on the VX305x-SA: one is embedded in the PCH while the other is a standalone, high-precision, low-power component located on the integrated PCH SMBus (RV8564 by Micro Crystal). The latter is more precise and is powered when the board is off.

#### ▶ Standby power supplied to the RV8564 RTC

When the VX305x-SA is powered off, the RTC is powered either by the onboard battery or through the 3.3V\_AUX rail or the VBAT rail on the VPX backplane.

To ensure data retention in the RV8564 RTC, VBAT must be set in the range [2.5V - 5.5V]. The maximum current drawn over the -40 °C/+85 °C temperature range is 500 nA (VBAT= 3 V, no I2C activity) or 550 nA (VBAT=5 V, no I2C activity).




---

The RTC present in the integrated PCH is never powered by the battery.

---

#### ▶ Internal Integrated PCH RTC

The integrated PCH RTC module provides a date and time keeping device with two banks of static RAM with 128 bytes each. The BIOS programs the RTC interrupt on Legacy IRQ8 that is never shared with other interrupts. It is clocked by an external 32.768 KHz oscillator with a parabolic coefficient of 0.4 ppm/°C<sup>2</sup> and a stability of +/-20 ppm at 25 °C. A 20 ppm stability is equivalent to a 10 mn/year drift.

#### ▶ Standalone low-power RTC RV8564

The RV8564C2/B RTC by Micro Crystal features an internal oscillator, date and time keeping module with programmable alarm, timer and interrupt functions. It has an ultra-low power consumption in time keeping mode: 250 nA, typical and 500 nA, maximum. Its stability is 20 ppm at 25 °C. It is connected to the integrated PCH SMBus

### ▶ RTC management by BIOS and OS

At each startup, the BIOS retrieves the date and time information from the high-precision RV8564 RTC and copies it into the integrated PCH RTC. This is necessary since the integrated PCH RTC is not saved.

Any update of date and time in the BIOS settings will be done both in integrated PCH RTC and RV8564 RTC.

Regarding the RTC management by the OS, the OS should use the high-precision RV8564 RTC driver. Failing to do so, the updates will be done only in integrated PCH RTC and will not be saved.

If no power is applied on the RV8564 RTC, the BIOS displays the BIOS build date and time instead of the current date and time.

### ▶ Century flag

For compatibility reasons, the BIOS implements the century flag for the high-precision RTC as follows:

- ▶ Century Flag C = 0 for 1900-1999 years
- ▶ Century Flag C = 1 for 2000-2099 years.

The user should check that the OS driver implements the same convention.

## 3.2.2. CPLD Watchdog

In addition to the standard watchdog timer included in the integrated PCH, the cPLD implements a hardware watchdog timer that can be used by the operating software to monitor the normal operation of the system.

It is enabled by software, and once enabled must be restarted at regular intervals. If not, its expiration sets off an interrupt (IRQ) to the local processor, a board reset or a board power-cycle.

The watchdog has the following features:

- ▶ timeout programmable from 1 to 511 clock periods, by steps of 2 periods
- ▶ clock periods of 1s or 1ms
- ▶ lock bit: when set, can only refresh (restart) the watchdog, but not change its settings
- ▶ 4 modes: timer, reset, interrupt or power-cycle
- ▶ restart counter: can manage the remaining number of resets or power-cycles done by the watchdog before giving-up.

### 3.3. Battery and Supercap

#### ▶ **Battery, supercap and VPX VBAT.**

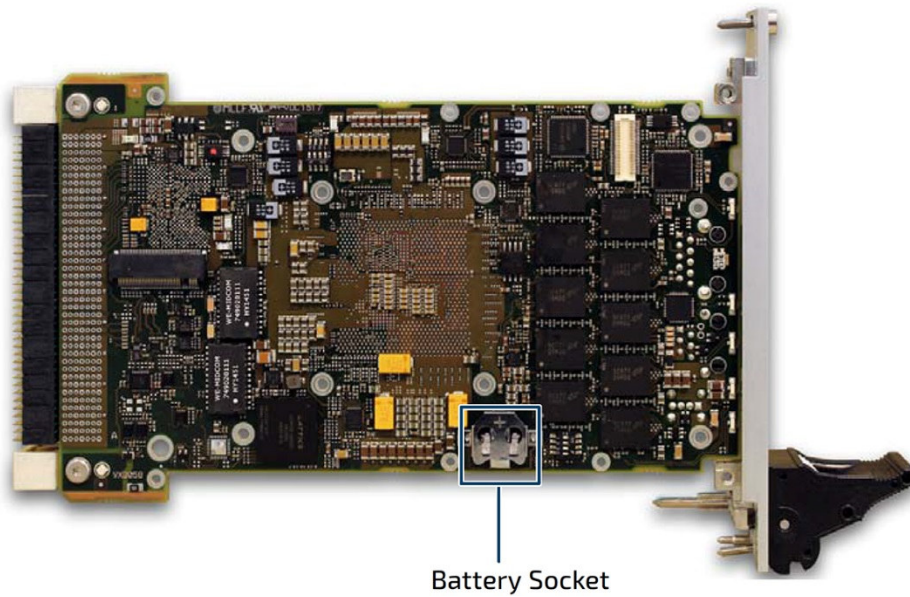
The industrial-grade battery RENATA CR1220 is mounted in a socket located on the board for air-cooled version.

#### ▶ **Battery Life at 25°C**

The RTC consumption is specified at 500nA in nominal conditions. The Battery nominal capacity is specified at 40mAh.

The expected battery duration at 25°C is above 8 years

Figure 17: Battery Socket



#### ▶ **Supercap Option**

On demand.

### 3.4. I2C Structure

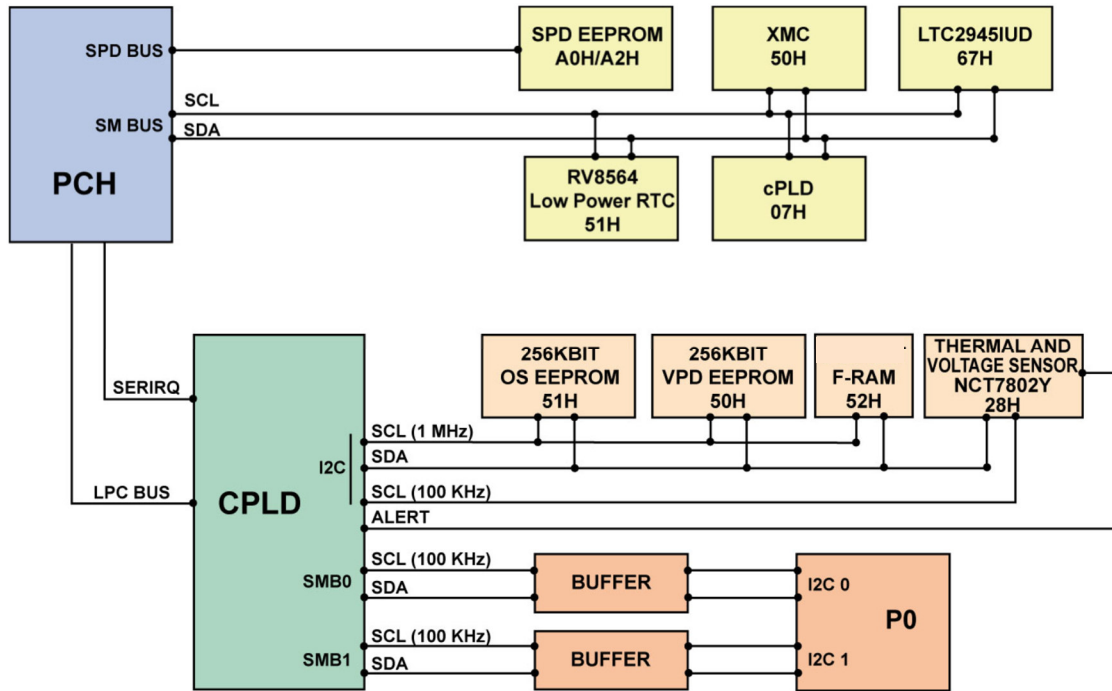
The VX305x-SA features three I2C busses.

- ▶ One is attached to the integrated Platform Hub Controller and controls the DDR4 SPD EEPROM and the low-power RTC.
- ▶ The other two are handled by the CPLD device according to Figure 16 "I2C Diagram".



The I2C addresses shown are 8 bit values which include a read/write bit. Shift one bit to the right to get the 7-bit addresses.

Figure 18: I2C Diagram



▶ **PCH SMBus (100 KHz)**

SLAVE DEVICES ON SOC SMBUS INTERFACE	SMBUS 7-BIT BASE ADDRESS	FEATURES
cPLD	07H (0x07)	System cPLD
LTC2945IUD	67H (0x67)	VS1 Current Monitoring
RV8564C2	51H (0x51)	External RTC Device
XMC Slot	50H (0x50)	To XMC Mezzanine SMBus

▶ **cPLD I2C Bus (100 KHz)**

SLAVE DEVICES ON CPLD SMBUS INTERFACE	SMBUS 7-BIT BASE ADDRESS	FEATURES
NCT7802Y sensor	28H (0x28)	Nuvoton Voltage / Temperature Sensor
24FC256-I/SN VPD EEPROM	50H (0x50)	256 Kbits VPE EEPROM
24FC256-I/SN OS EEPROM	50H (0x51)	256 Kbits OS EEPROM
FM24V10-G	52H (0x52)	1 Mbits User FRAM

### 3.5. CPLD Features

The CPLD manages the following features:

- ▶ Power-on/off control
- ▶ Reset control
- ▶ Local environmental control/monitoring
- ▶ LPC interface to processor
- ▶ I2C interfaces to I2C bus IPMB A/B (rear P0)
- ▶ LEDs control
- ▶ Serial lines multiplexer
- ▶ Serial VPD and user memories
- ▶ User and system GPIOs
- ▶ Internal registers that allow system management

#### 3.5.1. cPLD Registers Definition:

##### 3.5.1.1. Overview

These registers can be accessed from CPU through LPC bus at I/O address 0x800+offset.



Registers 0x72 to 0x78 can also be accessed from I2C bus 0 (register offset 0 to 6) by an external I2C master on the backplane.

Table 14: cPLD Registers Definition - Overview

OFFSET	NAME	PURPOSE	ACCESS
0x72	I2C_BOARD_STATUS	Board state (from I2C)	RW
0x73	I2C_BOARD_CONTROL	Board state and control (from I2C)	RW
0x74	I2C_ERROR_STATUS	Board error state (from I2C)	RW
0x75	I2C_PORT80	PORT80 value (from I2C)	RW
0x76	I2C_FAILCODE	PEX8725 EEPROM CRC error status (from I2C)	RW
0x77	I2C_SCRATCHPAD	Not yet defined	RW
0x78	I2C_MISC	Miscellaneous board information (from I2C)	RW

Contact Kontron for a detailed description of the CPLD registers.

##### 3.5.1.2. Detailed Description

###### ▶ **VX305x-SA VPX I2C interfaces**

VX305x-SA implements two I2C buses connected to P0 VPX connector (see P0 pin assignments):

I2C0 : CLK signal on pin P0/B5, DATA signal on pin P0/ A5

I2C1: CLK signal on pin P0/G4, DATA signal on pin P0/ F4

I2C bus 0 is a master/slave interface.

I2C bus 1 is a master only interface.

I2C bus 0/1 interfaces software tools are described in the Software Release Notes.

▶ VPX I2C bus 0 slave interface:  
 VX305x-SA board I2C bus 0 slave register base address depends on VPX slot ID (slot geographical address):  
 VPX Slot 1 (syscon): VX305x-SA slave I2C base address is 0x18 (I2C 7bits addressing)  
 VPX Slot 2: VX305x-SA slave I2C base address is 0x19 (I2C 7bits addressing)  
 VPX Slot 3: VX305x-SA slave I2C base address is 0x1A (I2C 7bits addressing)  
 And so on....

▶ I2C bus 0 slave registers definition:  
 I2C\_BOARD\_STATUS : This Register can be accessed from I2C0 Slave interface :  
 ▶ I2C\_SLAVE\_ADDR = 7'b0010\_111 + GA  
 ▶ Register offset (1 byte) = 0  
 Bits meaning during read access is controlled by bit 3 of register @73.

Table 15: I2C\_BOARD\_STATUS @0x72

I2C_BOARD_STATUS @0x72				
Can also be accessed from I2C0 slave interface with register offset 0 (or 0x10)				
Bit#	Name	Description	Reset	Type
7	Power Status	Power Status 0: Power Stand By 1: Power ON (S0 State)	0	RO
6-5	Reset Root	Root cause of Last Reset Detected 0x00 Internal PSUs power-on 0x01 Watchdog expired 0x10 SYSRESET (from VPX or VME) 0x11 Local reset : GPIO2 (maskable reset) reset switch reset from I2C (reg 0x73) reset by software asserting PLD PLTRST n	00	RO
4	Reset Status	Reset Status Side A 0: No PWOK or reset asserted 1: PWOK and reset unasserted	0	RO
3-0	Boot Status	Boot Status 0x00: RESET : default hardware value 0x01: BIOS-BOOT : written by BIOS 0x02: BIOS : written by BIOS 0x03: PBIT : written by BIOS 0x04: OS-BOOT : written by BIOS 0x05: OS-RUNNING : to be written by OS at the end of boot 0x06: COMPLETED : to be written by the final application when running 0x07: SHUTDOWN : to be written by OS when issuing a halt/shutdown 0x08: REBOOT : to be written by OS when rebooting 0x09 - 0x0B: Reserved 0x0C - 0x0F: Customer defined Those bits are Read Only through I2C Slave Interface and R/W through LPC Interface. The boot status is also reset at each board reset.	0000	RW

I2C\_BOARD\_CONTROL: This Register can be accessed from I2C0 Slave interface

- ▶ I2C\_SLAVE\_ADDR = 7'b0010\_111 + GA
- ▶ Register offset (1 byte) = 1

Table 16: I2C\_BOARD\_CONTROL @0x73

I2C_BOARD_CONTROL @0x73				
Can also be accessed from I2C0 slave interface with register offset 1 (or 0x11)				
Bit#	Name	Description	Reset	Type
7-4	Board Id	Board Identification 0001 VX6080 0010 VX6070 0011 VX3030 0100 VM6052/VM6054 0101 VM6050 0110 VX6060 0111 VX3035 1000 VX3040 family (VX3042/VX3044) <b>1001 VX305x family (VX3052/VX3058)</b> 1111 Reserved for non-SBC boards (switches, ...)	<b>1001</b>	RO
3	Reserved	This bit must be left at 0. Do not write 1 in this register.	0	RW
2	Reserved	RESERVED	-	-
1	Reset	0: No Reset 1: Reset Assert	0	RW
0	Power_OnOff	Power On/Off Control 0: Power Off (StandBy Mode) 1: Power On  This bit can be used to do a Power OFF or control the Power-On sequence when Standby Power is applied.  The default value is loaded when standby is applied from inverted SYSTEM EEPROM offset 0x100 bit 1, if FACTORY mode is not enabled <b>WARNING:</b> Setting this bit to 0 asserts VPX reset (SYSRESET_OUT#) if register 0x70 bit 0 (LOC2VPX) is set to 0  When this bit is used to do a Power Off (reset to 0), set this bit to 1 is not enough to do a Power-On : VPX PSUs must be switched Off and restarted.	*	RW

Table 17: I2C\_ERROR\_STATUS @0x74

I2C_ERROR_STATUS @0x74				
Can also be accessed from I2C0 slave interface with register offset 2 (or 0x12)				
Bit#	Name	Description	Reset	Type
7	Alert	Alert 0: no alert 1: alert pending from PLD_PECI_ALERT# or PLD_PCHHOT_CPU# See register ALERT_STATUS@5B bit 0 and 3 for current state on these signals See register SERIRQ_CONTROL@0xF bit 6 and 2 for interrupt Mask and Status	0	RO
6	POST_Error	POST Error 0: no error 1: error This bit is set when PBIT has been run with errors (according to reg 0x2) Also set when RTC battery is low (according to reg 0x3 bit 0)	0	RO
5	POST_RTC	POST RTC 0: POST OK 1: POST FAILED (weak or missing battery) This bit is a copy of reg 0x3 bit 0 (POST_RTC), that is set when RTC battery is low	0	RO
4-0	Error_Status	Safety Error status Bit 4: THERMTRIP# Bit 3: VRVCCIN_VRHOT# Bit 2: VR1V05_VRHOT# Bit 1: CATERR# Bit 0: PECI_CRIT# When an unmasked fatal alert occurs, this register is updated, all internal PSUs are switched off and the error status is also reported on the front panel LEDs See also registers @79 @7A	0	RO

Table 18: I2C\_PORT80 @ 0x75

I2C_PORT80 @ 0x75				
Can also be accessed from I2C0 slave interface with register offset 3 (or 0x13)				
Bit#	Name	Description	Reset	Type
7-0	Port_80	Port 80 value The value of this register is automatically updated at each write access to port 0x80 (write snooping). It is cleared at each reset.	0	RW (LPC) RO (I2C)

Table 19: I2C\_FAILCODE @ 0x76

I2C_FAILCODE @ 0x76				
Can also be accessed from I2C0 slave interface with register offset 4 (or 0x14)				
Bit#	Name	Description	Reset	Type
6-0			0	RW (LPC) RO (I2C)
0	PEX_EEPROM_CRC_ERROR	PEX EEPROM CRC error 0: no error 1: error This bit is set by BIOS when a CRC error is detected on the PEX EEPROM	0	RW(LPC) ) RO (I2C)

Table 20: I2C\_SCRATCHPAD @ 0x77

I2C_SCRATCHPAD @ 0x77				
Can also be accessed from I2C0 slave interface with register offset 5 (or 0x15)				
Bit#	Name	Description	Reset	Type
7-0	Scratchpad	Scratchpad register The purpose of this register is not defined	0	RW

Table 21: I2C\_MISC @ 0x78

I2C_MISC @ 0x78				
Can also be accessed from I2C0 slave interface with register offset 6 (or 0x16)				
Bit#	Name	Description	Reset	Type
7	Force_rescue	Force Rescue Mode for System Flash Boot. 0: not forced (default) 1: forced Changing this bit will take effect at next board reset (LPC reset) and override the Switch configuration. Register @09 bit 7 indicates the current Flash selected.	0	RW
6	Force_EFI_Shell	Force stop at EFI shell. 0: not forced (default) 1: forced	0	RW
5-3	Reserved	Reserved	000	RW (LPC) RO (I2C)
2-0	Reserved	Reserved	000	RW

Table 22: POWER ERROR part 1 @ 0x79

POWER ERROR part 1 @ 0x79				
Can also be accessed from I2C0 slave interface with register offset 7 (or 0x17)				
Bit#	Name	Description	Reset	Type
7-0	Power Error Part 1	<p>This register indicates what are the Power rails failed when a power error is detected (see also register @7A)</p> <p>Bit 7: PWRGD_VPX            Bit 6: PWRGD_VR5V0            Bit 5: VPXPWRGD_UV            Bit 4: VPXPWRGD_OV            Bit 3: VCCSCFUSESUS            Bit 2: VCCKRHV            Bit 1: VR1V05            Bit 0: VR2V5_DDR4</p> <p>An error is reported if at least one PSU does not start within the expected delay (timeout) or fails after being OK.</p> <p>This register is cleared by switching the board off (standby) or by removing VPX power.</p>	0	RO

Table 23: POWER ERROR part 2 @ 0x7A

POWER ERROR part 2 @ 0x7A				
Can also be accessed from I2C0 slave interface with register offset 8 (or 0x18)				
Bit#	Name	Description	Reset	Type
7-0	Power Error Part 2	<p>This register indicates what are the Power rails failed when a power error is detected (see also register @79)</p> <p>Bit 7: VR1V2            Bit 6: VTT            Bit 5: Reserved            Bit 4: VR1V5_PCH            Bit 3: VRPEX            Bit 2: VR3V3            Bit 1: VRVCCIN            Bit 0: Safety_Alert (see register @74 for details)</p> <p>An error is reported if at least one PSU does not start within the expected delay (timeout) or fails after being OK.</p> <p>This register is cleared by switching the board off (standby) or by removing VPX power.</p>	0	RO

### 3.6. Serial Lines EIA-422/485 Additional Modes

A total of 2 serial lines are available on VX305x-SA product.

EIA-232 serial lines are available on front panel RJ12 and P2 connectors.

See section 4.1.1 page 58 - "Serial Connector" and section 4.3.3 page 70 - "P2 Connector" for more information on pin assignments.

EIA-232 serial lines mode is the default mode, but EIA-422/485 mode can also be set with the following mode:

Table 24: Serial Lines Additional Modes

MODE	RJ12 FRONT PANEL CONNECTOR	RJ12 FRONT PIN ASSIGNMENT	P2 REAR CONNECTOR	P2 REAR PIN ASSIGNMENT
Default EIA-232	EIA-232: COM1, COM2	COM1 TXD: pin 3 COM1 RXD: pin 4 COM2 TXD: pin 1 COM2 RXD: pin 6	EIA-232: COM1, COM2	COM1 TXD: pin G3 COM1 RXD: pin G7  COM2 TXD: pin G11 COM2 RXD: pin G15
EIA-422/485 on COM1	EIA-422/485: COM1	COM1 TXD+: pin 3 COM1 RXD+: pin 4 COM1 TXD-: pin 1 COM1 RXD-: pin 6	EIA-422/485: COM1	COM1 TXD+: pin G3 COM1 RXD+: pin G7  COM1 TXD-: pin G11 COM1 RXD-: pin G15

The mode EIA-232 or EIA-422/485 is selected in the BIOS by the user. When EIA-422/485 is selected, an optional on board 120 Ohms termination can be activated from the BIOS Menu, as well as a half-duplex mode.

### 3.7. GPIOs and GDISCRETE1

#### 3.7.1. GPIOs

The VX305x-SA features 5 GPIOs managed by the CPLD. Refer to the Software Release Notes chapter 7.7 for further details on the GPIO driver.

- ▶ 3 GPIOs are available on P0 connector: GPIO3, GPIO4 and GPIO5. See section 4.3.1 "P0 Connector" page 68 for detailed pinout.
- ▶ 2 GPIOs are available on P1 connector, GPIO1, GPIO2. See section 4.3.2 "P1 Connector" page 69 for detailed pinout.

GPIO electrical characteristics: The CPLD features LVCMOS33 cells (0-3V3), drive strength = 8 mA (sink or source), a clamp diode which is not 5V tolerant, an hysteresis of 250mV. The CPLD does not implement any internal pull-up or pull-down.

On the VX305x-SA board, a pull-up of 47 kOhms is connected to GPIO1 to GPIO5.



**CAUTION:** GPIOs are not 5V tolerant. Maximum voltage on GPIOs is 3.6 V. Absolute maximum voltage is 3.75V and is not suitable for continuous operation. Appropriate voltage reduction (through resistor divider for instance) must be made to avoid permanent damage to the board.

The GPIOs share the same interrupt in the CPLD.

#### 3.7.2. GDISCRETE1

GDISCRETE1 is a bussed open-collector GPIO defined by OpenVPX VITA 65 and available on P1. See section 4.3.2 "P1 Connector" page 69 for detailed pinout.

It is handled by the CPLD and buffered by a SN74LVC1G125 wired as an Open Collector to meet the electrical characteristics defined in VITA 65.

It has a dedicated interrupt in the CPLD.

### 3.8. Reset

Table 25: Reset sources

RESET SOURCE	RESET ACTION	RESET CONTROL	RESET STATUS	NOTE
Front panel reset push button	Platform resetreset	Front push button	"I2C_BOARD_STATUS @0x72 Or VPX I2C bus 0 slave interface"	Reset propagation options and masks available in cPLD registers
VPX Sysreset	Platform resetreset	VPX P0 / Row B/ Wafer 4	"I2C_BOARD_STATUS @0x72 Or VPX I2C bus 0 slave interface"	"See VPX Vita46.0 standard Reset propagation options and masks available in cPLD registers"
VPX maskable reset (GPIO2)	Platform resetreset	VPX P1 / Row G/ Wafer 15	"I2C_BOARD_STATUS @0x72 Or VPX I2C bus 0 slave interface"	See VPX Vita46.0 standard
cPLD watchdog reset	Platform resetreset	See software release notes	"I2C_BOARD_STATUS @0x72 Or VPX I2C bus 0 slave interface"	See software release notes
Processor watchdog reset	Platform resetreset	Intel D-15xx watchdog control registers	Intel D-15xx watchdog status registers	
cPLD software reset	Platform resetreset	I2C_BOARD_CONTROL @0x73	"I2C_BOARD_STATUS @0x72 Or VPX I2C bus 0 slave interface"	See register definition in this user's guide
VPX SMBus0 slave register	Platform resetreset	See VPX I2C bus 0 slave interface chapter	"I2C_BOARD_STATUS @0x72 Or VPX I2C bus 0 slave interface"	"VPX P0 I2C Bus 0 signals Base address depends on Board slot number (VPX Geographical address)"

### 3.9. Write Protect Mode

VX305x-40G non-volatile content is managed in three independent write protection domains.

- ▶ SYS: Write protection at system level
- ▶ USR: Write protection at user level. Under user control
- ▶ VPD: Kontron Vital Product Data

▶ **SYS\_WP**

- ▶ Description:  
Write protection at system level
- ▶ Write Protect Control table:

SYS_WP Protection	NVMRO	sw1[1] Factory Mode	Note
YES	1	OFF	Normal operation
No	0	X	Normal operation

X = "don't care", CPLD register @09-bit 2 default setting is "0"

- ▶ Protected Devices:  
256 Kbits OS EEPROM, cPLD I2C Bus
  - ▶ OS EEPROM on CPLD I2C bus @0x51
  - ▶ PEX8725 EEPROM
  - ▶ XMC EEPROM

▶ **USER\_WP**

- ▶ Description:  
Write protection at user level
- ▶ Write Protect Control:

USER_WP Protection	NVMRO	sw1[1] Factory mode	sw1[4] User write protection	Note
YES	1	OFF	X	Normal operation
NO	0	X	OFF	Normal operation
YES	0	X	ON	Forced mode

X = "don't care", CPLD register @09-bit 2 default setting is "0"

- ▶ Protected Devices:  
1 Mbits User FRAM, cPLD I2C bus  
SPI Boot Flash  
SPI 10GETH Flash
  - ▶ FRAM located on CPLD I2C2 bus @0x52
  - ▶ SPI Boot Flash memories
  - ▶ SPI 10 Gb ETH Flash

## ▶ VPD\_WP

### ▶ Description:

Write protection at VPD level

### ▶ Hardware Write Protection:

NVRMO signal is high and SW1[3] OFF and SW1[1] is OFF for full protection  
CPLD bit @0x09-Bit1 high.

### ▶ Write Protect Control:

VPD_WP Protection	NVMRO	sw1[1] Factory mode	sw1[3] VPD write protection	Note
YES	1	OFF	OFF	Normal operation
YES	0	X	OFF	Normal operation
NO	X	X	ON	Forced mode

X = "don't care", CPLD register @09-bit 2 default setting is "0"

### ▶ Protected Devices:

VPD EEPROM, CPLD I2C Bus Reserved Factory Mode

Memory SPD EEPROM devices

Ethernet Controller SPI flashes

- ▶ VPD EEROM on CPLD I2C2 bus @0x50
- ▶ DDR4 SPD
- ▶ SPI flash for ETH0 I210T and ETH2 I210T controllers

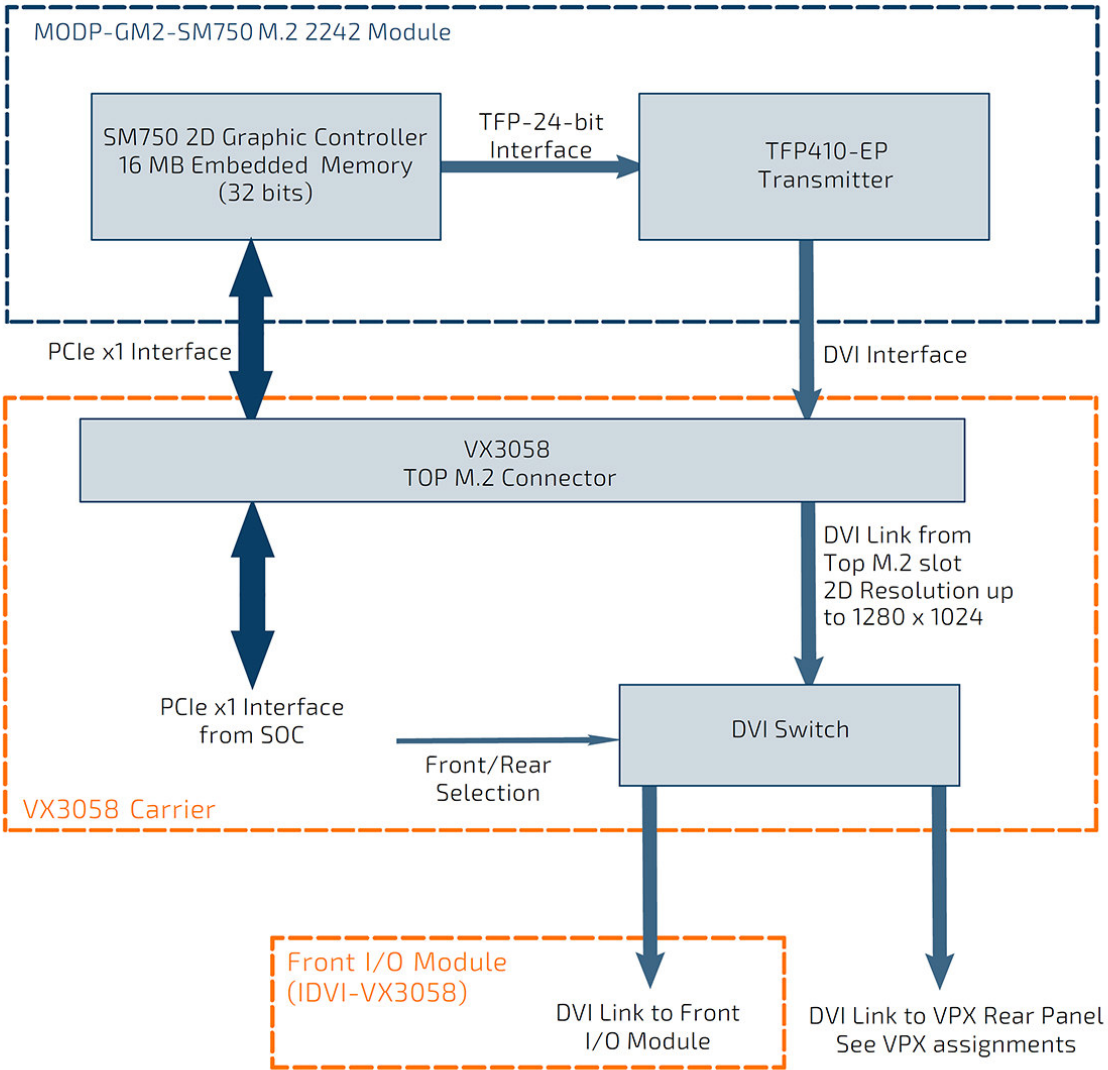
### 3.10. Graphics Option

VX305x can be order with a graphics option offering a single DVI/HDMI interface (maximum resolution of 1280x1024). These video interfaces are available on the front panel or P2 connector.

Please contact Kontron for DisplayPort M2 graphics module availability.

The M2 graphics module implements one 2-D graphic Silicon Motion SM750 controller with 16 MB of embedded DDR memory.

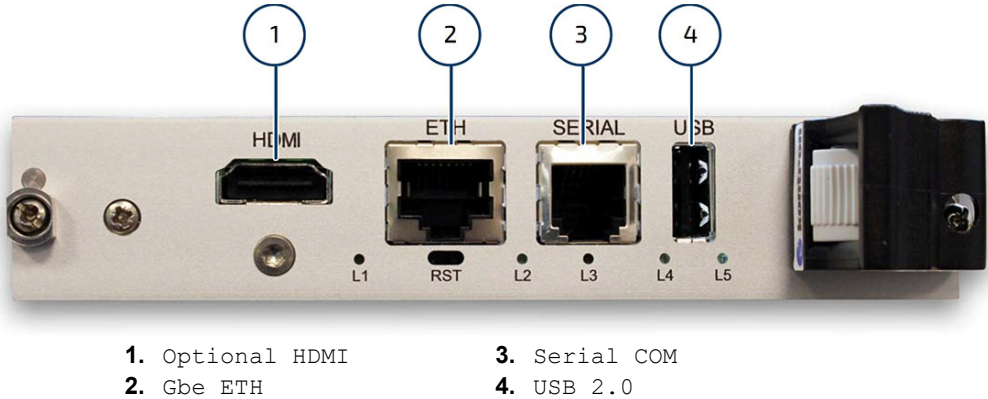
Figure 19: Graphics Option



# 4/Physical I/O

## 4.1. Front Panel Connectors

Figure 20: Location of the Front Panel Connectors



### 4.1.1. Serial Connector - COM

The VX305x-SA integrates two serial communication ports, COM1 and COM2 in PC parlance. COM1 and COM2 are available via the VPX P2 connector.

Default serial mode is simplified serial line mode Rx/Tx only, 115200 bauds.

COM1 is also available via the front panel connector.

- ▶ COM1: EIA-232 or EIA-485 (simplified RX/TX) port on RJ-12 front panel connector or on the rear P2 connector

- ▶ COM2: EIA-232 or EIA-485 (simplified RX/TX) port on the rear P2 connector

Each serial port is configurable via the CPLD as EIA-232 or EIA-485. Each port operates in full duplex mode. Fast slew rate is the default mode in EIA-485 mode.

The signaling level of EIA-485 is compatible with EIA-422, so full duplex EIA-485 may also be used for point-to-point communications with an EIA-422 serial port.

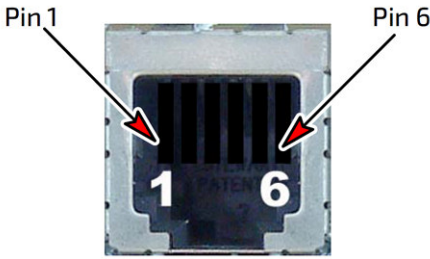
See section 4.3.3 " P2 Connector" page 70 for more information on the serial lines wafer assignment on P2 connector.

#### ▶ Pin Assignment

Table 26: Serial Connector Pin Assignment

PIN	SIGNAL
1	COM2 TXD / COM1TXD-
2	Shell
3	COM1 TXD/TXD+
4	COM1 RXD/RXD+
5	GND
6	COM2 RXD/COM1 RXD-

Figure 21: Serial Connector



A serial line should only be used via one connector at the same time, either the Serial front panel connector or the P2 connector.

Table 27: Serial Connector Signal Description

MNEMONIC	DESCRIPTION
COM2 RXD/COM1 RXD-	COM2 Receive Data (EIA-232) / COM1 Receive Data minus (EIA-485)
COM2 TXD/COM1 TXD-	COM2 Transmit data (EIA-232) / COM1 Transmit Data minus (EIA-485)
COM1 RXD/RXD+	COM1 Receive Data (EIA-232) / Receive Data plus (EIA-485)
COM1 TXD/TXD+	COM1 Transmit Data (EIA-232) / Transmit Data plus (EIA-485)
GND	Ground
Shell	Chassis Ground

Serial Cable Designation



The Serial cable shall be shielded and shall provide a good shielding continuity between each end.

The Serial cable length should not exceed 10 m.

Final EMC qualification is required at system level, after Kontron product integration and customer cable selection.

Serial cable is:

- ▶ RJ-14 (6 pin, 4 conductor) for a simple EIA-232 without handshake support.
- ▶ RJ-12 (6 pin, 6 conductor) for EIA-232 with handshaking.  
A RJ-12 to DB9/DB25 male or DB9/DB25 female adapter are available from multiple sources.
- ▶ Kontron cable: Order Code KIT-2X-RJ12DB9 (not shielded and restricted to lab or maintenance usage)

Table 28: Serial Cable Pin Assignment

DB9 Pin Connector	Signal	RJ-12 Pin Connector
1	RTS	1
2	TXD	3
3	RXD	4
4	CTS	6
5	GND	5

Figure 22: Serial Cable



### 4.1.2. Gigabit Ethernet Connector



The Ethernet cable shall be CAT6 compliant.

This Ethernet cable shall be S/FTP type at least (Shielded Foiled Twisted Pair), providing shielding continuity between each end.

The Ethernet transmission should operate using a CAT6 cable with a maximum length of 100 m.

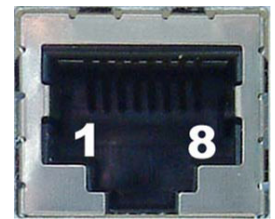
Final EMC qualification is required at system level, after Kontron product integration and customer cable selection.

The Ethernet connectors are available as RJ-45 connectors with tab down. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

Table 29: Gigabit Ethernet Connector Pin Assignment

Figure 23: Ethernet Connector

pin	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-	-	I/O	BI_DC+
5	-	-	-	-	I/O	BI_DC-
6	I	RX-	I	RX-	I/O	BI_DB-
7	-	-	-	-	I/O	BI_DD+
8	-	-	-	-	I/O	BI_DD-
Shell	Chassis Ground					



### 4.1.3. USB Connector



USB cable shall be compliant to Universal Serial Bus Specification, Revision 2.0.

This USB cable shall have double shielding.

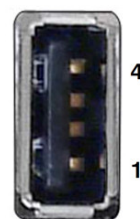
The USB cable length should not exceed 3 m.

Final EMC qualification is required at system level, after Kontron product integration and customer cable selection.

Table 30: USB Connector Pin Assignment

Figure 24: USB Connector

PIN	SIGNAL	function	I/O
1	VCC (+5V Protected)	VCC	--
2	USB_D-	Differential USB-	I/O
3	USB_D+	Differential	I/O



		USB+	
4	GND	GND	--

4.1.4. HDMI Port



The HDMI cable shall provide a good shielding continuity between each end.

This HDMI cable shall have double shielding.

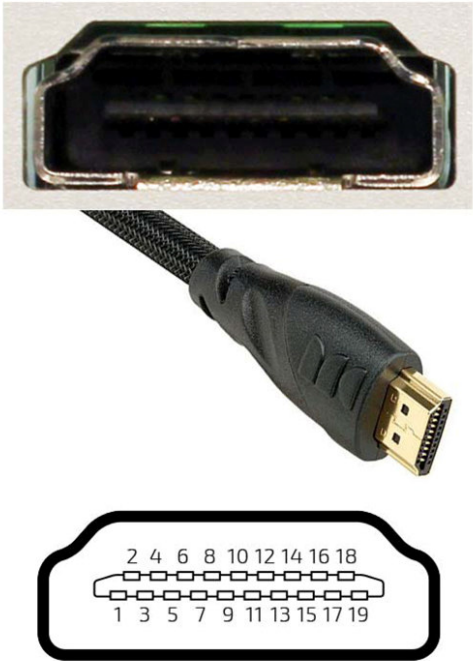
The HDMI cable length should not exceed 3 m.

Final EMC qualification is required at system level, after Kontron product integration and customer cable selection..

Table 31: HDMI Port Pin Assignment

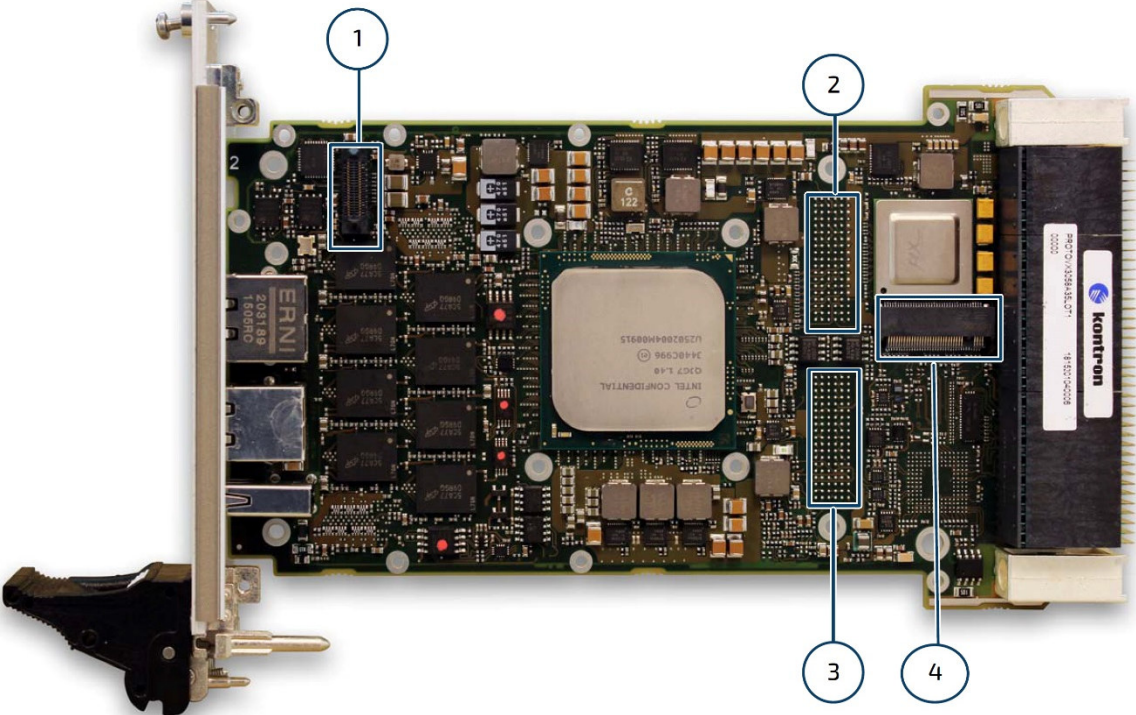
Figure 25: HDMI Port Cable

PIN	SIGNAL
1	TMDS Data2+
2	TMDS Data2 Shield
3	TMDS Data2-
4	TMDS Data1+
5	TMDS Data1 Shield
6	TMDS Data1-
7	TMDS Data0+
8	TMDS Data0 Shield
9	TMDS Data0-
10	TMDS Clock+
11	TMDS Clock Shield
12	TMDS Clock-
13	N.C.
14	N.C.
15	SCL
16	SDA
17	GND
18	+5V
19	Hot Plug Detect



### 4.2. Onboard Connectors

Figure 26: Onboard Connectors



- 1. J4101
- 2. J15
- 3. J16
- 4. P2801

### 4.2.1. XMC J15 Connector Pin Assignments



XMC slot option is a nonstandard option because of thermal impacts and product restrictions with XMC slot - on demand only.

The pin assignment of the J15 XMC PCI Express connector is pin compatible with VITA 42.0 and VITA 42.3. This interface is a PCI Express with 8 lanes coming from the CPU.

Table 32: XMC J15 Connector Pin Assignments

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR <sup>(1)</sup>
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR <sup>(1)</sup>
4	GND	GND	TCK	GND	GND	NC
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR <sup>(1)</sup>
6	GND	GND	TMS	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR <sup>(1)</sup>
8	GND	GND	TDI	GND	GND	-12V
9	RFU	RFU	N.C.	RFU	RFU	VPWR <sup>(1)</sup>
10	GND	GND	TDO	GND	GND	GA0
11	PER0p0	PER0n0	NC	PER0p1	PER0n1	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PER0p2	PER0n2	3.3V AUX	PER0p3	PER0n3	VPWR <sup>(1)</sup>
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	N.C.	PER0p5	PER0n5	VPWR <sup>(1)</sup>
16	GND	GND	NVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	N.C.	PER0p7	PER0n7	N.C.
18	GND	GND	N.C.	GND	GND	N.C.
19	REFCLK+0	REFCLK-0	N.C.	Reserved	N.C.	N.C.

<sup>(1)</sup> VPWR is connected to +12V via a fuse.

# Signals active when low.

## 4.2.2. XMC J16 Connector Pin Assignment



XMC slot option is a nonstandard option because of thermal impacts and product restrictions with XMC slot - on demand only.

XMC I/O signals are routed to the VPX P2 connector according VITA 46.9 x8d for differential pairs (8 pairs) and x38s for single ended (4 last signals).

Table 33: XMC J16 Connector Pin Assignment

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	XMCIO_DP1+	XMCIO_DP1-	NC	XMCIO_DP2+	XMCIO_DP2-	NC
2	GND	GND	NC	GND	GND	NC
3	XMCIO_DP3+	XMCIO_DP3-	NC	XMCIO_DP4+	XMCIO_DP4-	NC
4	GND	GND	NC	GND	GND	NC
5	NC	NC	NC	Reserved	Reserved	NC
6	GND	GND	NC	GND	GND	NC
7	NC	NC	NC	NC	NC	NC
8	GND	GND	NC	GND	GND	NC
9	NC	NC	NC	NC	NC	NC
10	GND	GND	NC	GND	GND	NC
11	XMCIO_DP5+	XMCIO_DP5-	NC	XMCIO_DP6+	XMCIO_DP6-	NC
12	GND	GND	NC	GND	GND	NC
13	XMCIO_DP7+	XMCIO_DP7-	NC	XMCIO_DP8+	XMCIO_DP8-	NC
14	GND	GND	NC	GND	GND	NC
15	Reserved	Reserved	NC	Reserved	Reserved	NC
16	GND	GND	Reserved	GND	GND	Reserved
17	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
18	GND	GND	XMCIO_SE3	GND	GND	XMCIO_SE4
19	Reserved	Reserved	XMCIO_SE1	Reserved	Reserved	XMCIO_SE2



- ▶ XMCIO signals are routed to VPX P2 connector, see VPX P2 pin assignment figure.
- ▶ NC pins are not connected on VX305x-SA board

### 4.2.3. J4101 Connector Pin Assignment

J0401 is dedicated to Front /IO module options.

Table 34: J4101 Connector Pin Assignment

PIN	SIGNAL	FUNCTION
1	GND	
2	GND	
3	DVI_SCL	Optional Front DVI Port
4	ETH2_MDI3 -	Optional 2 <sup>nd</sup> Ethernet MDI Interface
5	DVI_SDA	Optional Front DVI Port
6	ETH2_MDI3 +	Optional 2 <sup>nd</sup> Ethernet MDI Interface
7	GND	
8	GND	
9	DVI_C_CLK +	Optional Front DVI Port
10	ETH2_MDI2 -	Optional 2 <sup>nd</sup> Ethernet MDI Interface
11	DVI_C_CLK -	Optional Front DVI Port
12	ETH2_MDI2 +	Optional 2 <sup>nd</sup> Ethernet MDI Interface
13	GND	
14	GND	
15	DVI_C_TMDS0 +	Optional Front DVI Port
16	ETH2_MDI1 -	Optional 2 <sup>nd</sup> Ethernet MDI Interface
17	DVI_C_TMDS0 -	Optional Front DVI Port
18	ETH2_MDI1 +	Optional 2 <sup>nd</sup> Ethernet MDI Interface
19	GND	
20	GND	
21	DVI_C_TMDS1+	Optional Front DVI Port
22	ETH2_MDI0 -	Optional 2 <sup>nd</sup> Ethernet MDI Interface
23	DVI_C_TMDS1 -	Optional Front DVI Port
24	ETH2_MDI0 +	Optional 2 <sup>nd</sup> Ethernet MDI Interface
25	GND	
26	GND	
27	DVI_C_TMDS2 +	Optional Front DVI Port
28	Reserved	
29	DVI_C_TMDS2 -	Optional Front DVI Port
30	Reserved	
31	GND	
32	GND	
33	DVI_HPD	
34	Reserved	
35	RST#	
36	Reserved	
37	Reserved	
38	GND	
39	Reserved	
40	V_FRONTIO	

#### 4.2.4. P2701/P2801 Connector Pin Assignment

P2701/P2801 are the top/bottom M.2 slot connectors.

Table 35: P2801 Connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	GND_1	2	3V3_2
3	GND_3	4	3V3_4
5	PER3_N	6	Reserved
7	PER3_P	8	Reserved
9	GND_9	10	DAS/DSS#LED1#
11	PET3_N	12	3V3_12
13	PET3_P	14	3V3_14
15	GND_15	16	3V3_16
17	PER2_N	18	3V3_18
19	PER2_P	20	Reserved
21	GND_21	22	Reserved
23	PET2_N	24	Reserved
25	PET2_P	26	Reserved
27	GND_27	28	Reserved
29	PER1_N	30	Reserved
31	PER1_P	32	UART_RXD
33	GND_33	34	Reserved
35	PET1_N	36	Reserved
37	PET1_P	38	DEVSLP
39	GND_39	40	Reserved
41	PER0_N/SATA-B+	42	Reserved
43	PER0_P/SATA-B-	44	Reserved
45	GND_45	46	Reserved
47	PET0_N/SATA-A-	48	Reserved
49	PET0_P/SATA-A+	50	PERST#
51	GND_51	52	CLKREQ#
53	REFCLK_N	54	PEWAKE#
55	REFCLK_P	56	Reserved
57	GND_57	58	Reserved
59	CONNECTOR_KEY_59	60	CONNECTOR_KEY_60
61	CONNECTOR_KEY_61	62	CONNECTOR_KEY_62
63	CONNECTOR_KEY_63	64	CONNECTOR_KEY_64
65	CONNECTOR_KEY_65	66	CONNECTOR_KEY_66
67	NC_67	68	SUSCLK
69	PEDET	70	3V3_70
71	GND_71	72	3V3_72
73	GND_73	74	3V3_74
75	GND_75		

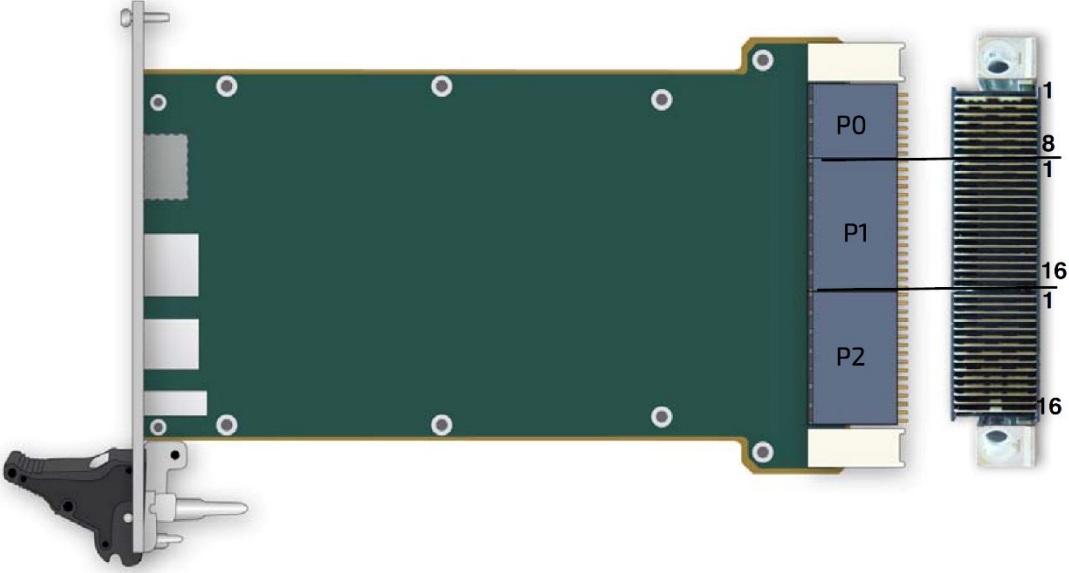
### 4.3. Rear Connectors

#### ▶ VPX Bus Interface

The complete 3U VPX connectors configuration comprises three connectors named P0 to P2:

- ▶ P0: 8-wafer 7-row connector.
- ▶ P1 - P2: 16-wafer 7-row differential connectors.

Figure 27: VPX Connectors



### 4.3.1. P0 Connector

Table 36: VPX Connector P0 Wafer Assignment

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	+12V	+12V	+12V	NC	NC (VS2)	NC (VS2)	NC (VS2)
2	+12V	+12V	+12V	NC	NC (VS2)	NC (VS2)	NC (VS2)
3	NC (VS3)	NC (VS3)	NC (VS3)	NC	NC (VS3)	NC (VS3)	NC (VS3)
4	I2C1 CLK	I2C1 DAT	GND	-12V_AUX	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3V3_AUX	GND	I2C0 CLK	I2C0 DAT
6	GA3*	GA2*	GND	NC (+12V_AUX)	GND	GA1*	GA0*
7	GPIO5 (TCK)	GND	PCIe_CLK- (TDO)	PCIe_CLK+ (TDI)	GND	GPIO3_10GMCK (TMS)	GPIO4_10GMD (TRST)
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND
CASE	GND						

\* signal active when low

Table 37: VPX Connector P0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
+12V	+12 Volts DC power (VS1 VPX supply). NC (+12V) pins are not connected (VS2 VPX supply)
-12V_AUX	-12 Volts auxiliary power. Only used to supply XMC if needed.
NVMRO	Non-Volatile Memory Read Only. When asserted (logical 1), prevents any non-volatile memory from being updated.
GAi	Geographical address pins
GAP	Geographical address parity
GND	Ground
GPIO5*	General purpose I/O 5 (handled by CPLD)
GPIO3_10GMCK*	General purpose I/O 3 (handled by CPLD) or Ethernet 10G I2C clock for rear SFP+
GPIO4_10GMD*	General purpose I/O 4 (handled by CPLD) or Ethernet 10G I2C data for rear SFP+
I2C0	I2C Bus 0
I2C1	I2C Bus 1
REF_CLK+/-	The Reference Clock is a bussed differential pair. Output if the VX305x-SA is plugged in the system controller slot, input otherwise. It enables the entire system to synchronize to a common time reference if desired. Counter/timer in the CPLD can use this clock VPX input REF_CLK is not used on VX305x products.
AUX_CLK+/-	1 PPS (one pulse per second) clock input. Can be programmed as an output on system controller slot. Can be used to phase the CPLD timer/counter clocked by REF_CLK+/-.
PCIe_CLK+/-	Optional Common Reference PCI Express Clock input.
SYSRESET*	System Reset. Input and open collector output.

\* See section 3.7 - GPIOs and GDISCRETE1 - page 53.

### 4.3.2. P1 Connector

Table 38: VPX Connector P1 Wafer Assignment

▶ Legend for Table 35:

P1_VBAT	Battery Voltage	USB0/1	USB2.0 links 0 and 1 (**)
		USB3	USB3 link from PCH
P1_SYS_CON*	System Controller	SATA0/1	SATA links 0 and 1 from PCH
PCIe0 LxRX   LxTX	x8, 2 x4 or 4 x2 PCI-Express	ETHx TX/RX	1000BASE-KX Ethernet controller or 10GBASEKR links 0 and 1 from integrated 10 GbE controller as per VITA 46.7.
		ETH2 DA/DB/DC/DD	1000BASE-T link from I210IT GbE controllers

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	GDISCRETE1	GND	PCIe0 L0-TX-	PCIe0 L0-TX+	GND	PCIe0 L0-RX-	PCIe0 L0-RX+
2	GND	PCIe0 L1-TX-	PCIe0 L1-TX+	GND	PCIe0 L1-RX-	PCIe0 L1-RX+	GND
3	VBAT	GND	PCIe0 L2-TX-	PCIe0 L2-TX+	GND	PCIe0 L2-RX-	PCIe0 L2-RX+
4	GND	PCIe0 L3-TX-	PCIe0 L3-TX+	GND	PCIe0 L3-RX-	PCIe0 L3-RX+	GND
5	SYS_CON*	GND	PCIe0 L4-TX-	PCIe0 L4-TX+	GND	PCIe0 L4-RX-	PCIe0 L4-RX+
6	GND	PCIe0 L5-TX-	PCIe0 L5-TX+	GND	PCIe0 L5-RX-	PCIe0 L5-RX+	GND
7	Reserved	GND	PCIe0 L6-TX-	PCIe0 L6-TX+	GND	PCIe0 L6-RX-	PCIe0 L6-RX+
8	GND	PCIe0 L7-TX-	PCIe0 L7-TX+	GND	PCIe0 L7-RX-	PCIe0 L7-RX-	GND
9	USB PWR	GND	SATA0 TX-	SATA0 TX+	GND	SATA0 RX-	SATA0 RX+
10	GND	SATA1 TX-	SATA1 TX+	GND	SATA1 RX-	SATA1 RX+	GND
11	USB PWR	GND	USB3 TX-	USB3 TX+	GND	USB3 RX-	USB3 RX+
12	GND	USB0 DA-	USB0 DA+	GND	USB1 DA- (**)	USB1 DA+ (**)	GND
13	GPIO1	GND	ETH2 DB-	ETH2 DB+	GND	ETH2 DA-	ETH2 DA+
14	GND	ETH2 DD-	ETH2 DD+	GND	ETH2 DC-	ETH2 DC+	GND
15	Maskable	GND	ETH1 TX-	ETH1 TX+	GND	ETH1 RX-	ETH1 RX+
16	GND	ETH0 TX-	ETH0 TX+	GND	ETH0 RX-	ETH0 RX+	GND
CASE	GND						

\* signal active when low



(\*\*) Wibu / Approtect feature and USB2.0 port #1 feature (located on P1 wafer B12/C12) are exclusive.

Table 39: VPX Connector P1 Signal Definition

MNEMONIC	SIGNAL DEFINITION
P1-REF_CLK_SE	Reserved
PCIe0 Lx-RX+/-	x8 PCI Express Link. Receive +/-, gen1, gen2 or gen3 Can also be used as a 2 x4 links or 4 x2 links
PCIe0 Lx-TX+/-	x8 PCI Express Link. Transmit +/-, gen1, gen2 or gen3 Can also be used as a 2 x4 links or 4 x2 links
SATAx RX+/-	Serial ATA. Receive +/- link x
SATAx TX+/-	Serial ATA. Transmit +/- link x
USB PWR	USB Power
USBx D+/-	Differential Data pair of USB link x
USB3 TX+/- RX+/-	Differential Data transmit and receive of USB3 link
ETH2 DA+/-	Ethernet 1000BASE-T: First pair of transmit/receive data.
ETH2 DB+/-	Ethernet 1000BASE-T: Second pair of transmit/receive data
ETH2 DC+/-	Ethernet 1000BASE-T: Third pair of transmit/receive data.

MNEMONIC	SIGNAL DEFINITION
ETH2 DD+/-	Ethernet 1000BASE-T: Fourth pair of transmit/receive data
ETHx RX+/-	10GBASE-KR or 1000BASE-KX Ethernet x: Receive data +/- (auto)
ETHx TX+/-	10GBASE-KR or 1000BASE-KX Ethernet x: Transmit data +/- (auto)
GDISCRETE1	Open VPX GDISCRETE1 signal
GPIO1*	General Purpose I/O 1 (handled by the CPLD)
Maskable Reset* or GPIO2	General purpose I/O 2 (handled by CPLD) or Optional reset input (may be left unconnected if not used).
GND	Ground
SYS_CON	System Controller Slot Indication
VBAT	Battery Voltage Input, 3V. Optional alternated source for RTC

\* See section 3.7 - GPIOs and GDISCRETE1 - page 53.

### 4.3.3. P2 Connector



XMC slot option is a nonstandard option because of thermal impacts and product restrictions with XMC slot - on demand only.

Table 40: VPX Connector P2 Wafer Assignment

► Legend for Table 37:

COM1/2	Simplified asynchronous serial lines	PCIe1_TX/RX	Additional PCI express x1 link from PCH
USB2	USB2.0 links 2 from PCH	PCIe1_CLK	Additional PCI express clock from PCH
SATA2/3	SATA links 2 and 3 from PCH	XMCIO_SE1-4	Single ended XMC IO pins C19,F19,C18,F18 according VITA46.9 X38s
ETH3	ETH3 from PCH	XMCIO_DP1-8	Differential XMC IO pins according VITA46.9 X8d

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	NC	GND	SATA2 TX-	SATA2 TX+	GND	SATA2 RX-	SATA2 RX+
2	GND	SATA3 TX-	SATA3 TX+	GND	SATA3 RX-	SATA3 RX+	GND
3	COM1 TXD/TXD+	GND	USB PWR	USB PWR	GND	USB PWR	USB PWR
4	GND	USB2 DA-	USB2 DA+	GND	NC	NC	GND
5	NC	GND	ETH3 DB--	ETH3 DB+	GND	ETH3 DA-	ETH3 DA+
6	GND	ETH3 DD-	ETH3 DD+	GND	ETH3 DC-	ETH3 DC+	GND
7	COM1 RXD/RXD+	GND	DVI HPD	NC	GND	NC	NC
8	GND	DVI TMDS1-	DVI TMDS1+	GND	DVI TMDS2-	DVI TMDS2+	GND
9	NC	GND	DVI CLK-	DVI CLK+	GND	DVI TMDS0-	DVI TMDS0+
10	GND	PCIe1 CLK-	PCIe1 CLK+	GND	DVI SDA	DVI SCL	GND
11	COM2 TXD/ COM1 TXD-	GND	PCIe1 TX-	PCIe1 TX+	GND	PCIe1 RX-	PCIe1 RX+
12	GND	XMCIO_SE3	XMCIO_SE1	GND	XMCIO_SE4	XMCIO_SE2	GND
13	NC	GND	XMCIO_DP1+	XMCIO_DP1-	GND	XMCIO_DP2+	XMCIO_DP2-
14	GND	XMCIO_DP3+	XMCIO_DP3-	GND	XMCIO_DP4+	XMCIO_DP4-	GND
15	COM2 RXD/ COM1 RXD-	GND	XMCIO_DP5+	XMCIO_DP5-	GND	XMCIO_DP6+	XMCIO_DP6-
16	GND	XMCIO_DP7+	XMCIO_DP7-	GND	XMCIO_DP8+	XMCIO_DP8-	GND
CASE	GND						

\* signal active when low  
www.kontron.com

Table 41: VPX Connector P2 Signal Definition

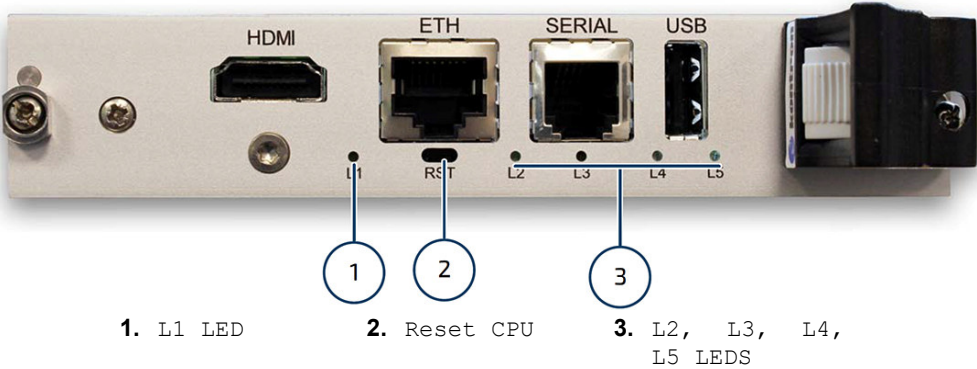
MNEMONIC	SIGNAL DEFINITION
COMx	Serial Lines, EIA-232/EIA-485
USB PWR	USB Power
USBx D+/-	Differential Data pair of USB link x
SATAx RX+/-	Serial ATA. Receive +/- link x
SATAx TX+/-	Serial ATA. Transmit +/- link x
PCIe1 TX/RX	Additional PCI-Express x1 link
PCIe1 CLK	Common Reference Clock Output for PCIe1
GND	Ground
XMCI0_SE1-4	Single ended XMC I/O 1,2,3 and 4 according to VITA 46.9 X38s
XMCI0_DP1-8	Differential pairs XMC I/O 1 to 8 according to VITA 46.8 X8d
DVI	DVI Port

4.4. LEDs

4.4.1. Status LEDs Default Setting

There are five bicolor LEDs (Red/Green) on the front panel of the VX305x-SA 3U VPX board.

Figure 28: LEDs Front panel



### 4.4.2. LEDs Activity

Table 42: LEDs Description

CPU LED	DESCRIPTION
●	LED OFF
●	Red LED
●	Green LED
●	Orange LED
*	Red blinking LED
*	Green Blinking LED
*	Orange blinking LED
*	Not blink: Indicates that the corresponding LED gives an additional information if any LED is blinking at the same time

The following table describes the information that the LED can report:

Table 43: LEDs Activity

L1	L2	L3	L4	L5	MEANING
●	Not Blink	Not Blink	Not Blink	Not Blink	Permanent system error. Internal VX305x-SA power is off. In this state L2, L3, L4 and L5 do not carry the meaning described in this table but an error code detailed in the <b>ERRORS CODES</b> table.
●					1000Base-T interfaces: At least one linked at 1000BASE-T Blinking when activity on the links
●					1000Base-T interfaces: At least one linked at 100M/10MBASE-T Blinking when activity on the links
●					100BASE-TX/1000BASE-T interfaces are down
	●				PEX FATAL Error detected
	●				10G Ethernet controller link up.
	*				Blinking when activity on the link
	●				10G Ethernet controller off
		●			Internal power supplies are ON and board reset is asserted.
		●			Internal power supplies are ON and board reset de-asserted (normal operation).
		●			Internal power supplies are ON but PROCPWRGD_PCH not activated
		*			<b>Fast</b> blinking <b>RED</b> (reset asserted) or <b>GREEN</b> (reset de-asserted) when activity to/from backplane I2C/SMBus
		*			<b>Slow</b> blinking <b>GREEN</b> (1 Hz, 50% duty cycle) when internal power supplies are OFF (board in standby)
			●		Normal operation
			●		Factory test mode
			●		CPLD Watchdog expired
			*		Off blinking when M2 activity on Slot 2
				●	Processor hot event (PROCHOT), supersedes 10G Ethernet routing information
				●	ETH1 <b>and</b> ETH2 links directed on front connector
				●	At least one of ETH1 or ETH2 link directed on VPX connector
				*	Off blinking when M2 activity on Slot 1

L1	L2	L3	L4	L5	POWER GOOD ERRORS
●	●	●	●	●	PWRGD_VPX
●	●	●	●	●	VPXPWRGD_UV
●	●	●	●	●	VPXPWRGD_OV
●	●	●	●	●	PWRGD_VR5V0
●	●	●	●	●	PWRGD_VCCSCFUSESUS
●	●	●	●	●	PWRGD_VCCKRHV
●	●	●	●	●	PWRGD_VR1V5_PCH
●	●	●	●	●	PWRGD_VR1V05
●	●	●	●	●	PWRGD_VR2V5_DDR4
●	●	●	●	●	PWRGD_VR1V2
●	●	●	●	●	PWRGD_VTT
●	●	●	●	●	PWRGD_FET1V05
●	●	●	●	●	PWRGD_VRPEX
●	●	●	●	●	PWRGD_VR3V3
●	●	●	●	●	PWRGD_VRVCCIN
●	●	●	●	●	RESERVED
●	●	●	●	●	WAKE UP ERROR (timeout on SLP_S4# deassertion)
●	●	●	●	●	PROCPWRGD ERROR (timeout on PROCPWRGD_PCH assertion)
●	●	●	●	●	PLTRST# ERROR (timeout on deassertion S5 To S0)
●	●	●	●	●	LPC CLOCK is 48 MHz (Legacy value is 33 MHz)
●	●	●	●	●	LPC CLOCK is 25 MHz (Legacy value is 33 MHz)

L1	L2	L3	L4	L5	CRITICAL ERRORS
●	●	●	●	*	PECI_CRIT#
●	●	●	*	●	CATERR#
●	●	*	●	●	VR1V05_VRHOT#
●	*	●	●	●	VRVCCIN_VRHOT#
*	●	●	●	●	THERMTRIP#

## 5/Power and Thermal Specifications

### 5.1. Electrical Specifications

#### 5.1.1. Input Powers Supplies Protection

The input power rails are protected on the VX305x-SA by fuse as described below.

To prevent safety hazards, the chassis power supply must not exceed the Voltage Rating and Interrupt Rating of the fuse.

Table 44: Input Powers Supplies Protection

POWER RAIL	VPX VS1	VPX 3.3 V AUX
LOCATION	P0	P0
VOLTAGE	+12 V	+3.3 V
PROTECTION	Non resettable fuse	Non resettable fuse
RATED CURRENT	10 A	1.5 A
TRIP CURRENT	-	2.1 A min @ 85 °C 3.0 A typ @ 23 °C 3.5 A max @ -40 °C
TYPICAL MELT I <sup>2</sup> T	2.0	-
VOLTAGE RATING	24 V	32 V
INTERRUPTING RATING	150 A	35 A
MANUFACTURER / PN	3216FF10-R	043501.5KR

#### 5.1.2. Output Powers Supplies Protection

On the VX305x-SA, all the output power supplies provided on connectors are protected by fuse or current-limiting devices as described below.

Table 45: Output Powers Supplies Protection

Port	Function	Location	Voltage	Protection	Worst Case Hold Rated Current (Maximum operation temperature)	Trip current	Characteristics	Note
Front Panel USB	USB 2.0	Front Panel	+5 V	Nano 150F1.5A	1 A	2.2 A @ 60 °C 3 A @ 25 °C 3.54 A @ 0 °C	Time to trip: 0.3s @ 8 A @ 25 °C	
Front HDMI		Front Panel	+5 V	Non resettable fuse	0.8 A	-	-	Graphic option only
VPX P1 Rear USB Power pins	P1 USB power	Rear P1	+5 V	Non resettable fuse	1.25 A	-	-	
VPX P2 Rear USB power pins	P2 USB Power	Rear P2	+5 V	Non resettable fuse	1.25 A	-	-	
M2.	M2	On	+3.3 V	Non	2.5 A	-	-	

Slots	slot power supply	board		resettable fuse				
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## 5.2. Power Specifications

### 5.2.1. VX3052 and VX3058 Thermal Power

The following data show total board consumption for different processor configuration and Thermal Design Power. These data help for thermal power dissipation analysis.

All power values in this table are measured in operational conditions on early field Xeon-D parts.

Table 46: Thermal Power: board power based on current measurements

	Power Mode	Measured CPU package power/Freq	Max total Power consumption (W)	Test Condition
VX3058SA881150000  VX3058 D-1537 @ 1.7 GHz No M.2 module, No GFX option	100 % all cores @ 1.7 GHz Max Processor Power package	35 W / 1.7 GHz	62 W	Maximum CPU junction temperature Dual bank DDR4-2133 memory configuration full speed LinuxOS with full speed and full load stress tests running on all I/Os I/Os configuration: front panel serial line, one front panel lGeth, no USB devices, one external SATA hard drives at full speed on rear panel , PCIe x8 and two 10G-KR rear link full speed, LPC/FRAM activity
	80 % all cores	32 W / 1.7 GHz	58 W	Maximum CPU junction temperature Dual bank DDR4-2133 memory configuration full speed LinuxOS, no I/Os stress tests
	Linux Idle Linux "On demand" mode	10 W / 800 MHz	25 W	Maximum CPU junction temperature Dual bank DDR4-2133 memory configuration full speed LinuxOS, no I/Os stress tests
VX3052SA280150000  VX3058 D-1508* @ 2,2 GHz No M.2 module, No GFX option	Max Processor Power package	25 W / 2.2 GHz	50 W	Maximum CPU junction temperature Dual bank DDR4-2133 memory configuration full speed LinuxOS with full speed and full load stress tests running on all I/Os I/Os configuration: front panel serial line, one front panel lGeth, no USB devices, one external SATA hard drives at full speed on rear panel , PCIe x8 and two 10G-KR rear link full speed, LPC/FRAM activity
	80 % all cores	23 W / 2.2 GHz	46 W	Maximum CPU junction temperature Dual bank DDR4-2133 memory configuration full speed LinuxOS, no I/Os stress tests
	Linux Idle Linux "On demand" mode	10 W / 800 MHz	25 W	Maximum CPU junction temperature Dual bank DDR4-2133 memory configuration full speed LinuxOS, no I/Os stress tests
VX3058SA882150000  VX3058 D-1548 @ 2 GHz No M.2 module, No GFX option	Max Processor Power package	45 W / 2 GHz	75 W	Maximum CPU junction temperature Dual bank DDR4-2133 memory configuration full speed LinuxOS with full speed and full load stress tests running on all I/Os I/Os configuration: front panel serial line, one front panel lGeth, no USB devices, one external SATA hard drives at full speed on rear panel , PCIe x8 and two 10G-KR rear link full speed, LPC/FRAM activity
	80 % all cores @ 2 GHz	41 W / 2 GHz	70 W	Maximum CPU junction temperature Dual bank DDR4-2133 memory configuration full speed LinuxOS, no I/Os stress tests
	Linux Idle Linux "On demand" mode	10 W / 800 MHz	25 W	Maximum CPU junction temperature Dual bank DDR4-2133 memory configuration full speed LinuxOS, no I/Os stress tests

	Voltage Rail Name	Max Current	Max Continuous Power Consumption (W)	Test condition
--	-------------------	-------------	--------------------------------------	----------------

VX3058, VX3052 without VPX VS1 power supply Board in stand-by mode	VPX +3V3_AUX	150 mA continuous (2.5 A peak / 2 ms)	0.5 W	VPX +3V3_AUX power rail is present and VPX VS1 power rail not present. VPX +3V3_AUX power rail must support peak current condition at power-on.
Graphic option module	+3.3 V (generated internaly)	400 mA continuous	1,32 W	Graphic controller at full load. This thermal power is not dissipated on board.

### 5.2.2. VX3052, VX3058 Maximum Current

The following data provide maximum continuous and worst case current values on VPX VS1(12V) power supplies, for SA class. These maximum includes margin to guarantee worst case part behavior.

Table 47: Maximum VS1 Current

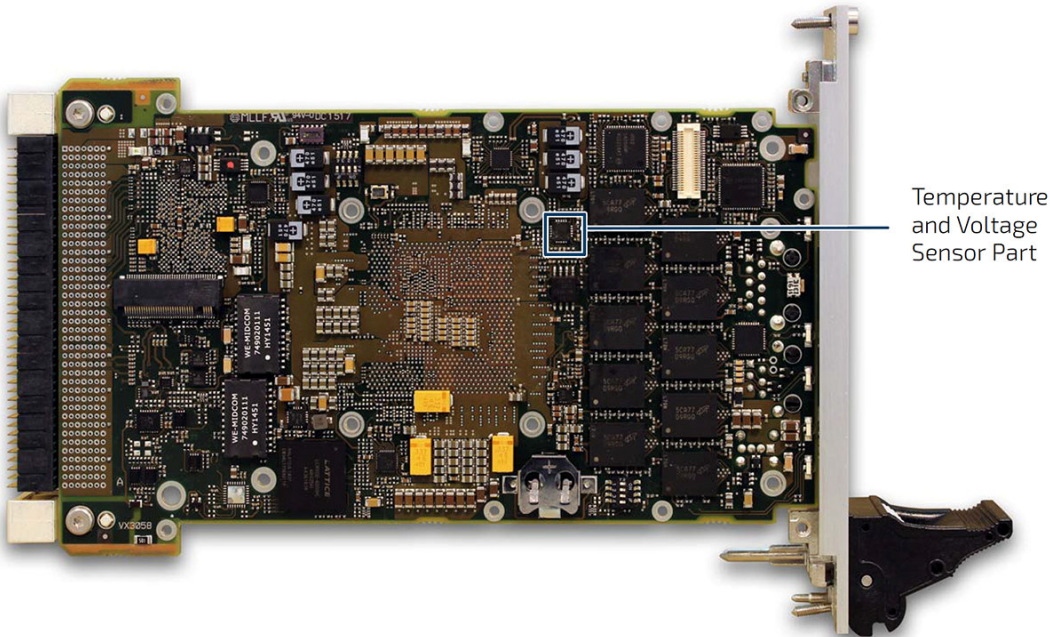
	Max VPX VS1 current	Test Condition
VX3058SA881150000 VX3058 D-1537 @ 1.7 GHz, No M.2 module, No GFX option	6 A	Calculated value based on measurements and for CPU @ 1.25*TDP
VX3052SA280150000 VX3058 D-1508 @ 2.2 GHz, No M.2 module, No GFX option	5 A	Calculated value based on measurements and for CPU @ 1.25*TDP
VX3058SA882150000 VX3058 D-1548 @ 2 GHz, No M.2 module, No GFX option	7 A	Calculated value based on measurements and for CPU @ 1.25*TDP

### 5.3. Board Thermal Monitoring

To ensure long-term reliability of the VX305x-SA, onboard components must not operate beyond their specified maximum temperature. The most critical component on the VX305x-SA is the processor. Operating the VX305x-SA above the maximum operating limits will result in permanent damage to the board.

The VX305x-SA includes a temperature sensor (NCT7802Y by Nuvoton) managed by the CPLD through I2C. See Figure 16 "I2C Diagram" page 46.

Figure 29: Temperature Sensor Location



In addition to monitoring several internal power supplies, the NCT7802Y supports one on-die temperature sensor and can also get the processor temperature directly via the Intel® PECI3.0 interface. The NCT7802Y temperature and voltages monitoring data may be viewed with the Linux "sensors" command.

The NCT7802Y has 3 alarm outputs connected to the CPLD:

- ▶ ALERT#: logged in CPLD to generate a maskable interrupt. The high threshold is set to +85°C by BIOS.  
The low threshold is set to -45 °C.

High threshold may be modified using the BIOS UEFI command

**VX305x-SA> kpld -i2cw 2 50 36 1 <value>**

Low threshold may be modified using the BIOS UEFI command

**VX305x-SA> « kpld -i2cw 2 50 37 1 <value>**

The low threshold may also be used as the lower threshold for high temperature hysteresis.

- ▶ T\_CRIT#: logged in CPLD reg @0x74, leads to fatal error with all internal PSUs power supplies being switched off and the error status is being displayed on the front panel LEDs. The T\_CRIT# threshold is set to +95 °C by BIOS.  
T\_CRIT threshold may be modified using the BIOS UEFI command  
**kpld -i2cw 2 50 3D 1 <value>**
- ▶ RESET#: not used by CPLD

#### ▶ NCT7802Y Key specifications:

- ▶ Voltage monitoring accuracy +-10 mV
- ▶ Temperature Sensor Accuracy
  - ▶ On-chip Temperature Sensor Accuracy (25~70 °C) +- 2 °C typ.
  - ▶ On-chip Temperature Sensor Resolution 1 °C
- ▶ Operating Temperature Range -40 °C ~ 85 °C

## 5.4. CPU Thermal Monitoring

All thermal data in the following tables are initial measurements on available Xeon-D processor silicons. These data applies to standard VPX 3U 1'' slot profile.

See VX305x-SA Thermal design guide for more information.

### ► CPU Temperature

For a given required air-flow and processor TDP (Thermal Design Power), the following curves show the maximum authorized operating temperature, not to exceed the maximum specified junction temperature of the processor.

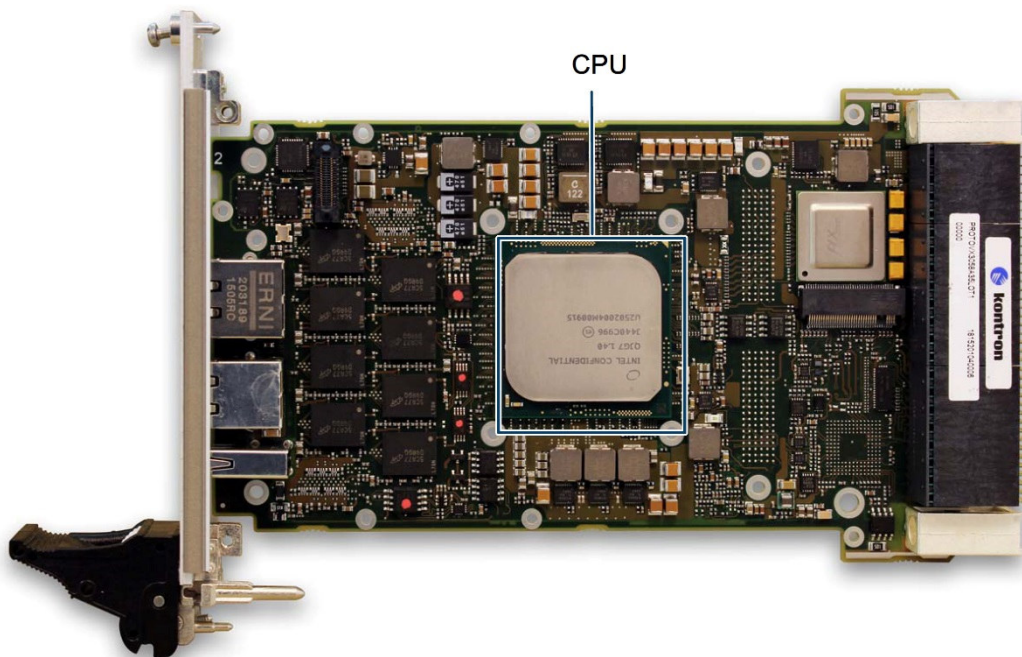
For Xeon-D processors, maximum case temperature ( $T_{cMAX}$ ) depends on processor part number.

These curves help also to choose customer operating points for a given 1 inch slot environment.

The  $T_{JMAX}$  temperature is the temperature not to exceed, to avoid entering the throttling mode.

To ease Xeon D temperature measurements and make sure that processor temperature is within Intel specifications, Intel provide maximum  $T_{case}$  temperatures (measured at the geometric center of the top surface of the intergated heatspreader).

Figure 30: CPU Location



Intel Power Thermal Utility (PTU) software has been used to force processor TDP during thermal characterization.

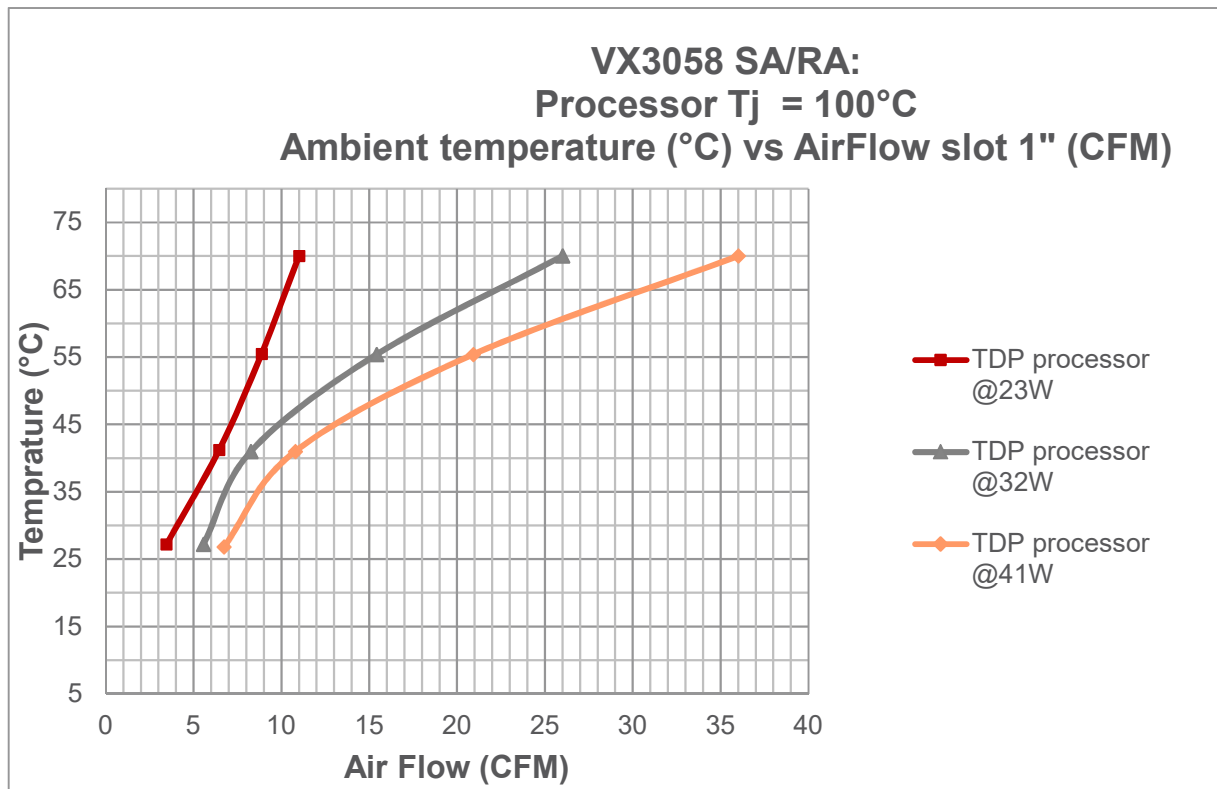
All Thermal Design Power (TDP) were measured with Intel Power Thermal Utility (PTU) software.

Table 48: VX305x-SA Functional Points Synthesis <sup>(1)</sup>

80 % of CPU load is the recommended processor load for normal applications.

		VX3058SA88215000 0 D-1548 CPU (TDP=45W)	VX3058SA88115000 0 D-1537 CPU (TDP=35W)	VX3052SA28015000 0 D-1508 CPU (TDP=25W)	Conditions
Processor Power Dissipation for 80 % CPU load	PW	41 W	32 W	23 W	No throttling, no turbo mode
Processor Junction Temperature all cores	PT	100 °C	100 °C	100 °C	
Inlet Air Temperature	AT	55 °C	55 °C	55 °C	
Minimum Inlet Airflow for 80 % CPU load	ICFM	26 CFM	20 CFM	11 CFM	
Extra Processor power Dissipation to be added in case of 100 % CPU load	EPW	4 W	3 W	2 W	PW CPU @ 100 % = PW + EPW

See also curves below <sup>(1)</sup>:

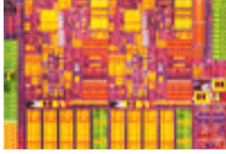


<sup>(1)</sup> Airflow test conditions according to Kontron test bench.



Highest thermal performance solutions for 35W and 45W processors are available on customer request.

## 5.5. Intel® Turbo Boost Technology



Intel® Turbo Boost Technology is one of the many exciting features that Intel has built into latest-generation Intel® microarchitecture. It automatically allows processor cores to run faster than the base operating frequency if it's operating below power, current, and temperature specification limits.

### Dynamically increasing performance

Intel Turbo Boost Technology 2.0 is activated when the Operating System (OS) requests the highest processor performance state (P0).

The maximum frequency of Intel Turbo Boost Technology 2.0 is dependent on the number of active cores. The amount of time the processor spends in the Intel Turbo Boost Technology 2.0 state depends on the workload and operating environment.

Any of the following can set the upper limit of Intel Turbo Boost Technology 2.0 on a given workload:

- ▶ Number of active cores
- ▶ Estimated current consumption
- ▶ Estimated power consumption
- ▶ Processor temperature

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency will dynamically increase until the upper limit of frequency is reached. Intel Turbo Boost Technology 2.0 has multiple algorithms operating in parallel to manage current, power, and temperature to maximize performance and energy efficiency.




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Intel Turbo Boost Technology 2.0 allows the processor to operate at a power level that is higher than its rated upper power limit (TDP) for short durations to maximize performance.

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Learn more about Intel Turbo Boost Technology:

<http://www.intel.com/technology/turboboost/>

The Intel Turbo Boost is handled by the BIOS through the Advanced Power Management Configuration menu.

Refer to the AMI BIOS for VX6090 - User Reference Manual, section "IntelRCSetup Menu".

## 6/Backplane Suggestions

Kontron can offer for development or deployment of the VX305x-SA the following backplane models:

Figure 31: Single Star x4, 8 SlotsTopology

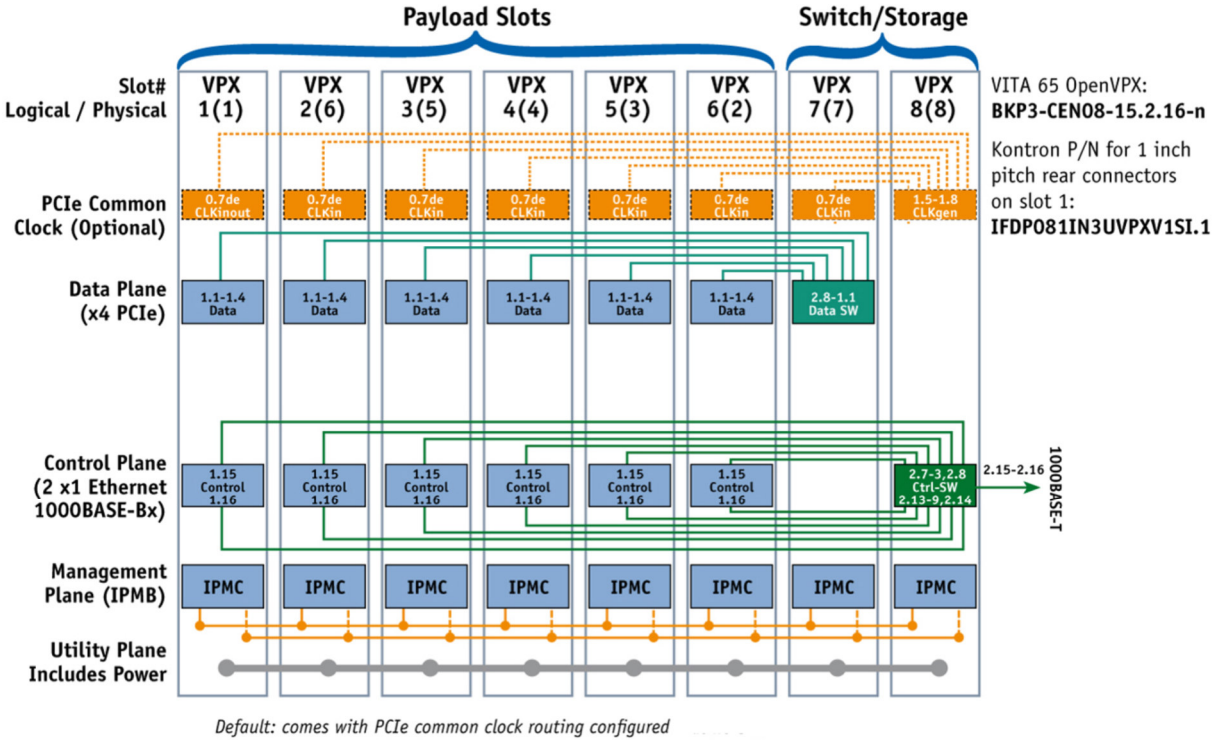
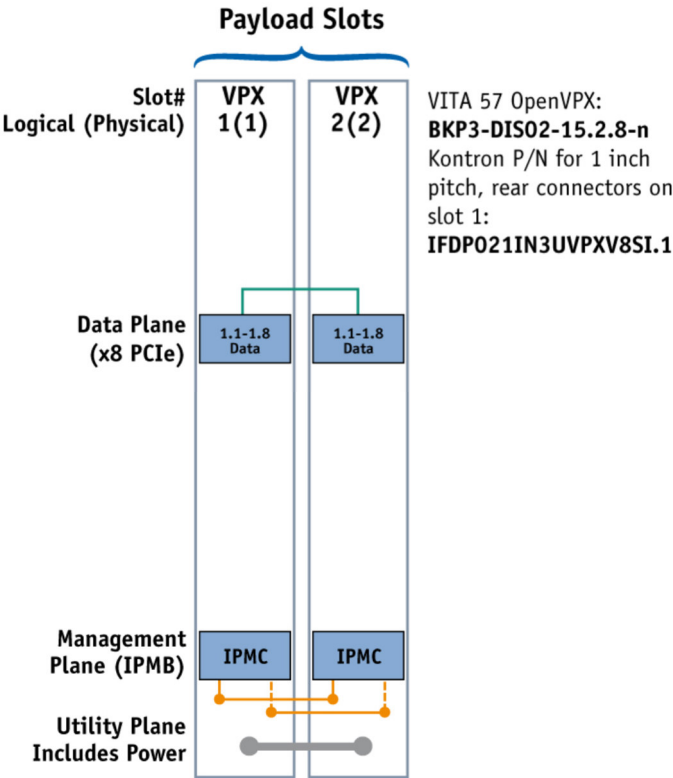


Figure 32: Distributed, 2 Slots Topology



# 7/VX305x-RC Characteristics

Figure 33: VX305x-RC Overview



Available RC order codes are listed in section 1.3.3 - Ordering Information, page 20.

## 7.1. VX305x-RC Specificities

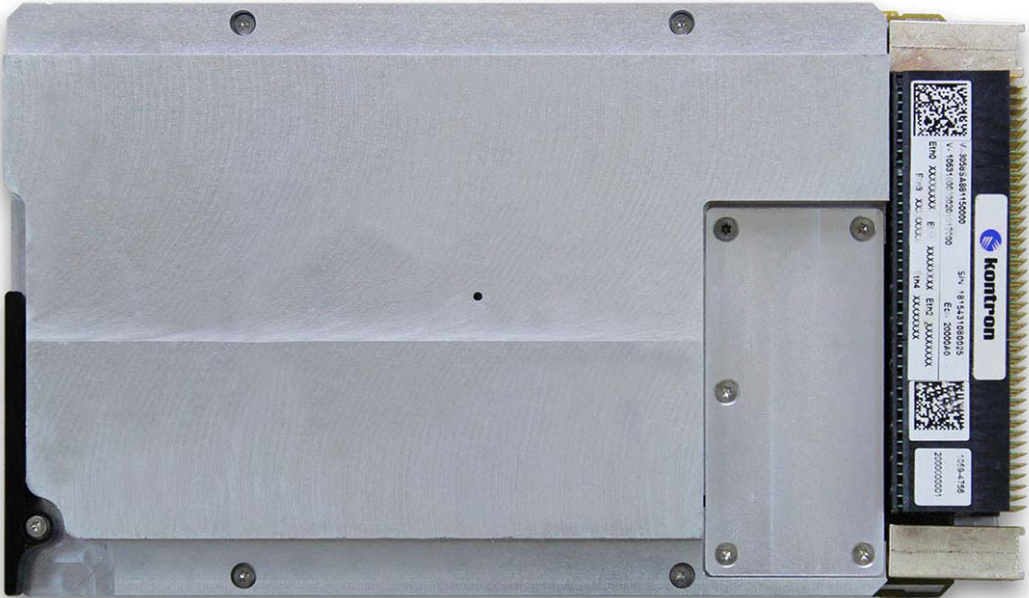
Table 49: VX305x-RC Specificities

FUNCTION	DESCRIPTION	SEE ALSO
Product mass	Mass depends on Mechanical E.C. Level	See section 7.3
Board Identification	Mechanical E.C. Level	See section 7.2
Environmental specifications	Refer to RC environmental specifications	See section 7.3
MTBF	MTBF depends on the environmental class	See section 7.4
Peripheral connectivity	No connector available on the board front panel	See section 7.5
Optional Modules	Module options	See section 7.10

### 7.2. VX305x-RC Board Identification

The VX305x-RC boards are identified by labels fitted on top and bottom sides. These labels are at the same location and have the same meaning as the VX305x-SA boards (See "Board Identification" Section).

Figure 34: VX305x-RC Identification (Top Side)



### 7.3. VX305x-RC Environmental Specifications

Table 50: VX305x-RC Environmental Specifications

ENVIRONMENTAL SPECIFICATIONS	RC
Plug-in unit type according Vita48.2	Type 2, secondary side retainers
Conformal Coating	Standard
Airflow	N.A.
Cooling Method	Conduction
Operating temperature	CPU TDP @25W: -40°C to 85°C <sup>(1)</sup> CPU TDP @35W: -40°C to 70°C <sup>(1) (2)</sup> CPU TDP @45W: -40°C to 70°C <sup>(1)</sup>
Storage Temperature	-50°C to +100°C
Sine vibrations (Operating)	1 hour per axis: 5-22 Hz, 2.5 mm peak 22-2000 Hz, 5 g
Random vibrations (Operating)	Product withstand vibration as defined below, 1 hour per axis: ▶ 5 Hz to 100 Hz PSD increasing at +3 dB/octave ▶ 100 Hz to 1000 Hz PSD = 0.1 g <sup>2</sup> /Hz ▶ 1000 Hz to 2000 Hz PSD decreasing at -6 dB/octave
Mechanical shocks (Operating)	40 g / 11 ms, half sine
Altitude (Operating)	-1,500 to 60,000 ft
Relative Humidity	95% non-condensing
Product mass	620 g

- (1) Maximum temperature measured at card edge in the following conditions: full processor performance, maximum processor TDP without CPU throttling. High thermal performance solutions for 35W and 45W processors are available on customer request.
- (2) Variants with D1539 and Operating Temperature option "-40°C/+85°C @ card edge" can be ordered if CPU workload never exceeds 80%.  
Ask Kontron for detailed CPU workload and operating conditions.

### 7.4. VX305x-RC MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- ▶ Ground Benign (GB)
- ▶ Air Inhabited Cargo (AIC)
- ▶ Naval Sheltered (NS),
- ▶ Air Rotary Wing (ARW)

Table 51: VX305x-RC MTBF Data

MTBF	GB (Hours)		NS (Hours)		ARW (Hours)	AIC (Hours)
	25 °C	40 °C	25 °C	40 °C	55 °C	40 °C
VX3058RC8F1151010	487 293 h	348 937 h	87 334 h	66 736 h	11 150 h	48 315 h

## 7.5. VX305x-RC Peripheral Connectivity

RC product variants do not have front panel I/O connectors. Only LED indicators and rest button are present on RC products front panels. RC variants Rear I/O features are common with SA products.

## 7.6. VX305x-RC Board Insertion

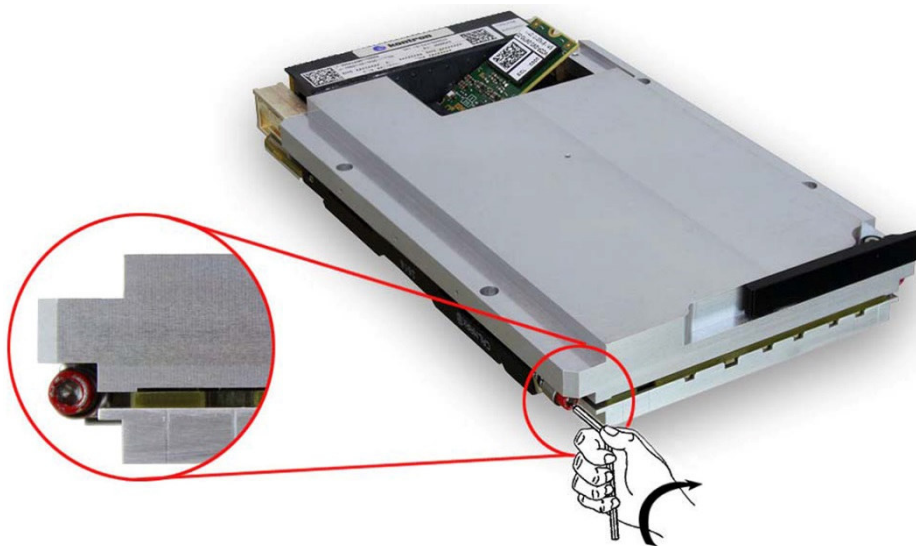
### **CAUTION**

Running the board at high temperature without tightening the wedgelocks to the cold plate may result in permanent damage to the board.

### ▶ **Torque to be applied.**

A torque of 0.9 N.m must be applied to the wedgelock screw (Calmark serie 265 ) when mounting the board into the chassis.

Figure 35: VX305x-RC Board Insertion - Wedgelock Screw Location



## 7.7. VX305x-RC Battery Option

No battery on standard RC product variants. Battery option on demand only.

## 7.8. VX305x-RC Thermal Performance

### ▶ **System Level Thermal Performance: Secondary side retainers to enlarge Thermal Management Zone.**

As per VITA4 8.2, the VX305x-RC features a secondary side attachment to optimize the surface of the Thermal Management Zone between the drain and the cold plate.

Figure 36: VX305x-RCThermal Management Zone



▶ **Board Level Thermal Performance**

The CPU core maximum junction temperature ( $T_j \text{ max}$ ) is the maximum temperature allowed before entering into throttling mode.  $T_j \text{ max}$  is  $104^\circ\text{C}$  for the Intel Xeon-D1500 series processors.

This core temperature is accessible through the Linux sensors driver. Refer to the Release Notes for BSP (SD.DT.G53) for information about the "sensors" command, RC class specific features, and power management.

Due to the actual accuracy of the processor internal sensors, and to secure processor full-on mode, the maximum temperature recommended by Kontron to avoid throttling is not  $104^\circ\text{C}$  but  $100^\circ\text{C}$ .

The user can modify several parameters to optimize thermal performance:

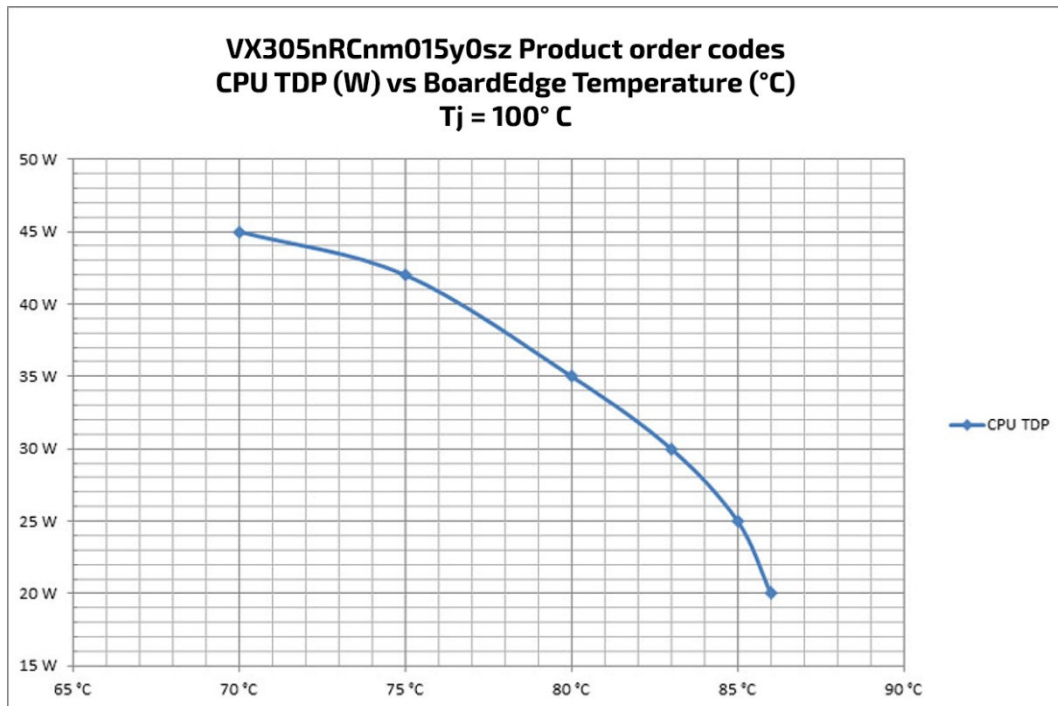
- ▶ Turbo mode: for a better control of thermal performance, it is advised to disable this mode.
- ▶ Processor load: Kontron advises to keep some margin for real time behavior and stay within 80% of processor load.
- ▶ Wedge lock temperature: this temperature depends on the cold plate temperature and on the board power consumption. It can be measured by sensors placed in holes located on the sides of the thermal drain.

The following curves give the relationship between processor dissipation and board edge temperature to keep the core temperature below  $100^\circ\text{C}$ , depending on RC product configuration. Exceeding junction temperature will force the processor to enter the throttling mode with reduced performance.

▶ **VX305nRCnm015y0sz product (Processor junction temperature@ $100^\circ\text{C}$ ) thermal performance versus CPU TDP**

VX305nRCnm015y0sz Product order codes (Processor junction temperature@ $100^\circ\text{C}$ )		Test conditions
CPU TDP	MEASURED CARD EDGE TEMPERATURE	
20 W	$86^\circ\text{C}$	Standard RC Kontron test bench. Maximum temperature measured at card edge in the following conditions: full processor performance, maximum processor TDP without CPU throttling.
25 W	$85^\circ\text{C}$	
30 W	$83^\circ\text{C}$	
35 W	$80^\circ\text{C}$	
42 W	$75^\circ\text{C}$	
45 W	$70^\circ\text{C}$	

Figure 37: VX305nRCnm015y0sz Processor TDP versus Card edge Temperature.




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Highest thermal performance solutions for 35W and 45W processors are available on customer request

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### 7.9. VX305x-RC BIOS Default Configuration for VX305x-RC

The conduction cooled versions of the VX305x come out of production with different BIOS settings than the air cooled versions. The changes are:

- ▶ Processor C-States disabled.
- ▶ Turbo mode disabled.
- ▶ Double refresh rate mode enabled on DDR4 interface (this setting is mandatory at high temperature).
- ▶ ETH1 and ETH2 routed to rear panel.
- ▶ All PCIe buses that are Gen3 capable (8GT/s) are forced in Gen2 mode (5GT/s)
- ▶ All SATA interfaces that are SATA III capable (6Gbps) are forced in SATA II (3Gbps)

### 7.10. VX305x-RC Optional Modules

See section 2.9 page 40 regarding M.2 module insertion / removal instructions.

## 7.11. VX305x-RC Covers Removal / Insertion Instructions.



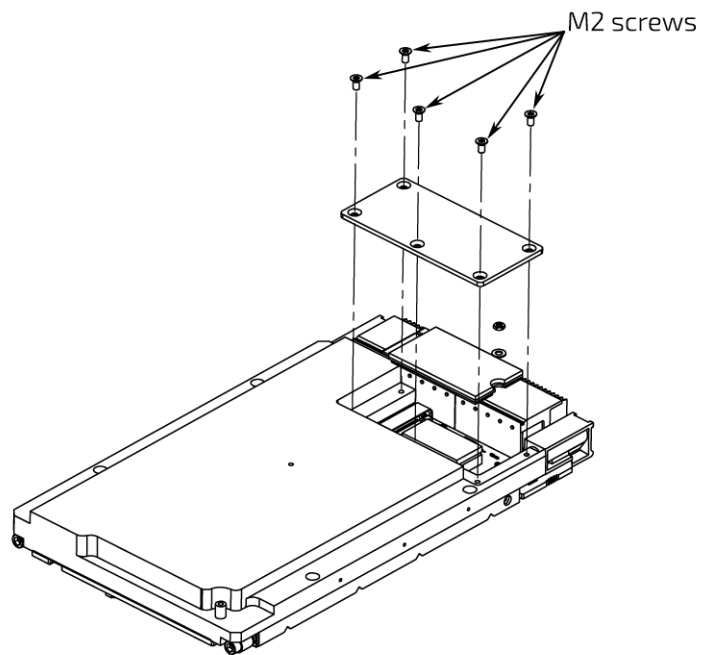
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**Apply "Loctite 222e" threadlock on each screw during re-assembling.**

**M.2 covers equipment depends on the ordered VX305x product oder code.**

---

Disassemble/assemble the top M.2 cover by unscrewing/screwing 5 screws (M2 x 4 with Torx) Refer to section 2.9 regarding M.2 module insertion / removal instructions. Screw with a torque of 0.2 Nm +/- 5%.



## 8/Tooling equipment: PB-VX3-501/511 pin assignments

The VX305x-SA supports the PB-VX3-5xx, a 3U VPX Rear Transition Module compliant with the definition of the Rear Transition Module on VPX standard - VITA 46.10.

### ▶ Tooling equipment: PB-VX3-5xx Rear Transition Module

It offers connectivity for:

- ▶ 4 HP Version (PB-VX3-501 order code)
  - ▶ one Ethernet SFP+ cage operating at 1 or 10 Gbps.
  - ▶ one Ethernet 1000BASE-T port
  - ▶ one micro HDMI port
  - ▶ two SATA ports up to SATA III (6Gbps)
  - ▶ two serial COM ports
  - ▶ one USB 3.0 / USB 2.0 port
  - ▶ two GPIOs
- ▶ 8 HP Version additional I/O (PB-VX3-511 order code):
  - ▶ 2 additional USB 2.0
  - ▶ 2 additional Sata ports up to SATA III (6Gbps)
  - ▶ 1 additional 1000BASE-T port

Refer also to the PB-VX3-4xx manuals (CA.DT.B03 and CA.DT.B04) applicable to the PB-VX3-5xx except for the front panel I/O differences described.

Figure 38: PB-VX3-5xx Tooling Equipment



8.1. ETHA (SFP+) pin assignments

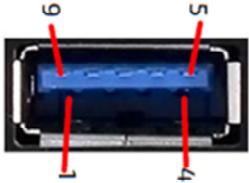
Contact Kontron for pin assignment and availability of SFP+ cage feature.

8.2. USB A-B pin assignments

USB 3.0 Connector Pin Assignment

USB 3.0 Connector

PIN	SIGNAL	function	I/O
1	VBUS	+5V Protected by 1.5A fuse	O
2	USB_D-	Differential USB-	I/O
3	USB_D+	Differential USB+	I/O
4	GND	Logic Ground	-
5	STDA_SSRX-	Negative SuperSpeed receiver differential pair	I
6	STDA_SSRX+	Positive SuperSpeed receiver differential pair	I
7	GND_DRAIN	Logic Ground	-
8	STDA_SSTX-	Negative SuperSpeed transmitter differential pair	O
9	STDA_SSTX+	Positive SuperSpeed transmitter differential pair	O

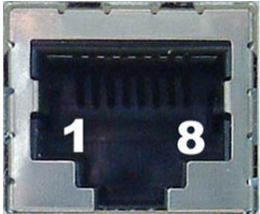


8.3. ETHB/ETHC pin assignments

Gigabit Ethernet Connector Pin Assignment

RJ45 Ethernet Connector

pin	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-	-	I/O	BI_DC+
5	-	-	-	-	I/O	BI_DC-
6	I	RX-	I	RX-	I/O	BI_DB-
7	-	-	-	-	I/O	BI_DD+
8	-	-	-	-	I/O	BI_DD-
Shell	Chassis Ground					

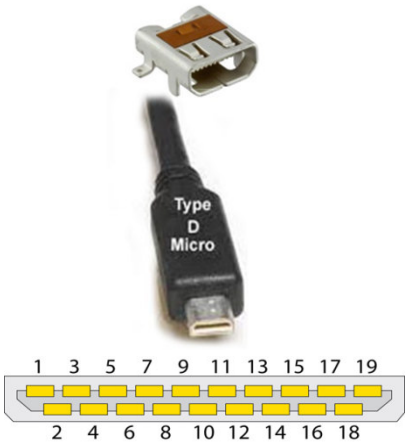


### 8.4. Micro HDMI pin assignments

Micro HDMI Connector Pin Assignment

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	HPD	2	NC
3	TMDS_DATA_2-	4	GND
5	TMDS_DATA_2+	6	TMDS_DATA_1+
7	GND	8	TMDS_DATA_1-
9	TMDS_DATA_0+	10	GND
11	TMDS_DATA_0-	12	TMDS_DATA_CLOCK+
13	GND	14	TMDS_DATA_CLOCK-
15	NC	16	GND
17	SCL	18	SDA
19	HDMI_PWR		

micro HDMI Connector



MNEMONIC	DESCRIPTION
TMDS_DATA_x+/-	HDMI main channel 0 to 2
TMDS_DATA_CLOCK+/-	HDMI clock channel
HPD	Hot Plug detect
SCL	Serial clock for DDC (Display Data Channel)
SDA	Serial data line for DDC (Display Data Channel)
HDMI_PWR	+5V power supply
GND	Ground

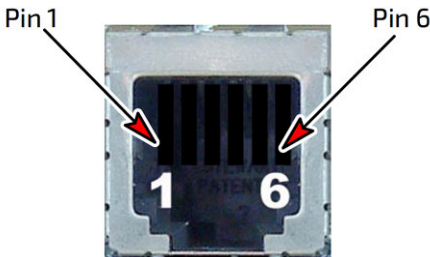
### 8.5. SERIAL pin assignments

► **Pin Assignment**

Serial Connector Pin Assignment

PIN	SIGNAL
1	Reserved
2	Shield
3	COM1 TXD
4	COM1 RXD
5	GND
6	Reserved

Serial Connector



Serial Connector Signal Description

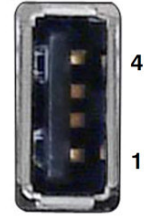
MNEMONIC	DESCRIPTION
COM1 RXD	COM1 Receive Data
COM1 TXD	COM1 Transmit Data
GND	Ground
Shell	Chassis Ground

## 8.6. USB C/D/E pin assignments

USB 2.0 Connector Pin Assignment

PIN	SIGNAL	function	I/O
1	VCC	VCC (+5V Protected)	O
2	USB_D-	Differential USB-	I/O
3	USB_D+	Differential USB+	I/O
4	GND	GND	--

USB 2.0 Connector



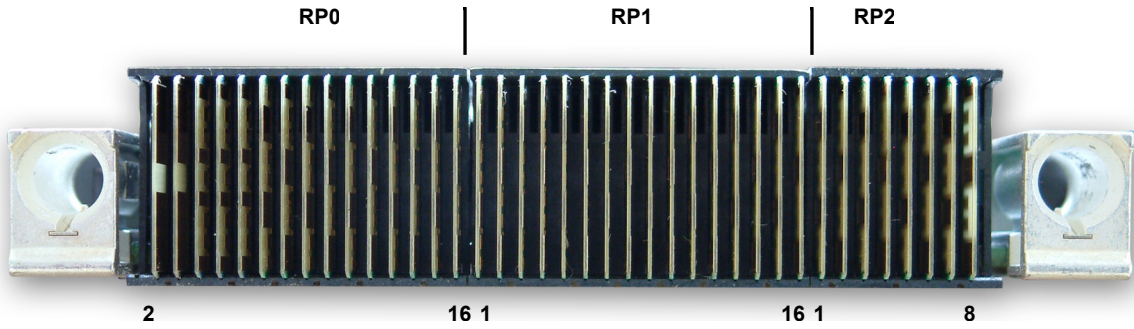
USB

## 8.7. Rear I/O Connectors

The PB-VX3-5xx Rear Transition Module conducts a wide range of I/O signals through the rear I/O connectors RP0, RP1 and RP2.

- ▶ RP0: 15-wafer 7-row mixed connector.
- ▶ RP1: 16-wafer 7-row differential connector.
- ▶ RP2: 8-wafer 7-row differential connectors.

Figure 39: Rear I/O VPX Connectors



### 8.7.1. RP0 pin assignments

#### » RP0 Wafer Assignment

Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A	Board Wafer
1	No Wafer							P0 W1
2	+12V	+12V	+12V	NC	NC (Optional 12V)	NC (Optional 12V)	NC (Optional 12V)	P0 W2
3	+5V	+5V	+5V	GND	+5V	+5V	+5V	P0 W3
4	SMB1 CLK	SMB1 DAT	GND	NC (-12V_AUX)	GND	SYSRESET*	NC (NVMRO)	P0 W4
5	NC (GAP*)	NC (GA4*)	GND	NC (3V3_AUX)	GND	SMB0 CLK	SMB0 DAT	P0 W5
6	NC (GA3*)	NC (GA2*)	GND	NC (+12V_AUX)	GND	NC (GA1*)	NC (GA0*)	P0 W6
7	GPIO5 (TCK)	GND	NC (TDO)	NC (TDI)	GND	GPIO3 (SFI_SCL)	GPIO4 (SFI_SDA)	P0 W7
8	GND	NC (REF_CLK-)	NC (REF_CLK+)	GND	NC (RES_CLK-)	NC (RES_CLK+)	GND	P0 W8
9	NC (GDISCRETE1)	GND	NC	NC	GND	NC	NC	P1 W1
10	GND	NC	NC	GND	NC	NC	GND	P1 W2
11	NC (VBAT)	GND	NC	NC	GND	NC	NC	P1 W3
12	GND	NC	NC	GND	NC	NC	GND	P1 W4
13	NC (SYSCON*)	GND	NC	NC	GND	NC	NC	P1 W5
14	GND	NC	NC	GND	NC	NC	GND	P1 W6
15	NC (P1-REF_CLK_SE)	GND	NC	NC	GND	NC	NC	P1 W7
16	GND	NC	NC	GND	NC	NC	GND	P1 W8
CASE	GND							

\* signal active when low

#### » RP0 Signal Definition

Mnemonic	Signal Definition
+12V	+12 Volts DC power (VS1 VPX supply).
+5V	+5 Volts DC power (VS3 VPX supply)
SFI_SCL	Ethernet 10G I2C clock for SFP+
SFI_SDA	Ethernet 10G I2C data for SFP+
SMB0	System Management Bus 0
SMB1	System Management Bus 1
SYSRESET*	System Reset. Input and open collector output.
GPIOx	General Purpose IO x

8.7.2. RP1 pin assignments

RTM Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A	Board Wafer
1	USB2 PWR	GND	SATA0 TX-	SATA0 TX+	GND	SATA0 RX-	SATA0 RX+	P1 W9
2	GND	SATA3 TX-	SATA3 TX+	GND	SATA3 RX-	SATA3 RX+	GND	P1 W10
3	USB3 PWR	GND	USBSS TX-	USBSS TX+	GND	USBSS RX-	USBSS RX+	P1 W11
4	GND	USB2 DA-	USB2 DA+	GND	USB3 DA-	USB3 DA+	GND	P1 W12
5	GPIO1	GND	ETH DB-	ETH DB+	GND	ETH DA-	ETH DA+	P1 W13
6	GND	ETH DD-	ETH DD+	GND	ETH DC-	ETH DC+	GND	P1 W14
7	Maskable Reset* or GPIO2	GND	SERD1 TX-	SERD1 TX+	GND	SERD1 RX-	SERD1 RX+	P1 W15
8	GND	SERD0 TX-	SERD0 TX+	GND	SERD0 RX-	SERD0 RX+	GND	P1 W16
9	COM1_RTS or COM1 TXD+	GND	SATA1 TX-	SATA1 TX+	GND	SATA1 RX-	SATA1 RX+	P2 W1
10	GND	SATA2 TX-	SATA2 TX+	GND	SATA2 RX-	SATA2 RX+	GND	P2 W2
11	COM1 TXD	GND	USB4 PWR	USB4 PWR	GND	USB5 PWR	USB5 PWR	P2 W3
12	GND	USB4 DA-	USB4 DA+	GND	USB5 DA-	USB5 DA+	GND	P2 W4
13	COM1 CTS or COM1 RXD+	GND	ETHC_MDI1-	ETHC_MDI1+	GND	ETHC_MDI0-	ETHC_MDI0+	P2 W5
14	GND	ETHC_MDI3-	ETHC_MDI3+	GND	ETHC_MDI2-	ETHC_MDI2+	GND	P2 W6
15	COM1 RXD	GND	DVI_HPD	NC	GND	NC	NC	P2 W7
16	GND	DVI_TMDS1-	DVI_TMDS1+	GND	DVI_TMDS2-	DVI_TMDS2+	GND	P2 W8
CASE	GND							

Mnemonic	Signal Definition
DVI xxx	DVI link
ETHC_xx	ETHC 1GbE Ethernet link
COMx	Serial line, EIA-232
USBx_PWR	USB Power link x
USBx_DA +/-	Differential Data pair of USB link x
USBSS_TX +/-	USB SuperSpeed Transmit link (USB 3.0)
USBSS_RX +/-	USB SuperSpeed Receive link (USB 3.0)
SATAx RX+/-	Serial ATA. Receive +/- link port x
SATAx TX+/-	Serial ATA. Transmit +/- link port x
SERD0_TX +/-	Not Connected
SERD0_RX +/-	Not Connected
SERD1_TX +/-	10 G Base KR transmit link
SERD1_RX +/-	10 G Base KR receive link
ETH_DA +/-	Ethernet 1000BASE-T: First pair of transmit/receive data
ETH_DB +/-	Ethernet 1000BASE-T: Second pair of transmit/receive data
ETH_DC +/-	Ethernet 1000BASE-T: Third pair of transmit/receive data
ETH_DD +/-	Ethernet 1000BASE-T: Fourth pair of transmit/receive data
GPIOx	General Purpose IO x
Maskable Reset	Optional reset input
Reserved	Reserved, do not connect

### 8.7.3. RP2 pin assignments

RTM Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A	Board Wafer
1	COM2 TXD+	GND	DVI_CLK-	DVI_CLK+	GND	DVI_TMDS0-	DVI_TMDS0+	P2 W9
2	GND	Reserved	Reserved	GND	DVI_SDA	DVI_SCL	GND	P2 W10
3	COM2 TXD	GND	Reserved	Reserved	GND	Reserved	Reserved	P2 W11
4	GND	Reserved	Reserved	GND	Reserved	Reserved	GND	P2 W12
5	COM2 RXD+	GND	Reserved	Reserved	GND	Reserved	Reserved	P2 W13
6	GND	Reserved	Reserved	GND	Reserved	Reserved	GND	P2 W14
7	COM2 RXD	GND	Reserved	Reserved	GND	Reserved	Reserved	P2 W15
8	GND	Reserved	Reserved	GND	Reserved	Reserved	GND	P2 W16
CASE	GND							

Mnemonic	Signal Definition
COMx	Serial Lines, EIA-232
DVI_xxx	DVI link
GND	Ground
Reserved	Reserved, do not connect



## About Kontron – An S&R Company

Kontron is a global leader in embedded computing technology (ECT). As a part of technology group S&T, Kontron offers a combined portfolio of secure hardware, middleware and services for Internet of Things (IoT) and Industry 4.0 applications. With its standard products and tailor-made solutions based on highly reliable state-of-the-art embedded technologies, Kontron provides secure and innovative applications for a variety of industries. As a result, customers benefit from accelerated time-to-market, reduced total cost of ownership, product longevity and the best fully integrated applications overall.

For more information, please visit: [www.kontron.com](http://www.kontron.com)



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