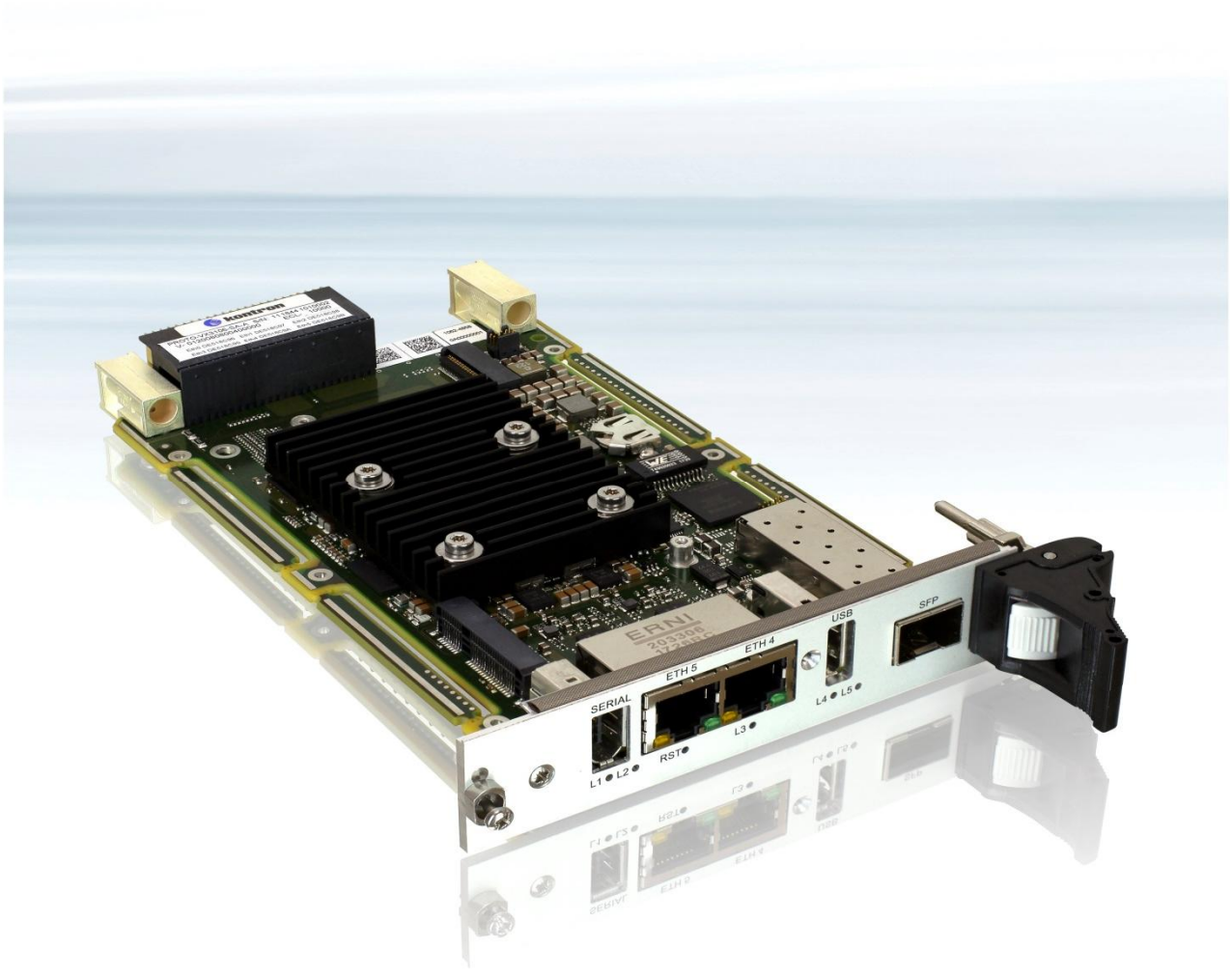
USER'S GUIDE



VX3106

3U VPX Single Board Computer

D218433-1.0 - May 2023

POSSIBILITIES START HERE kontron S&T Group

VX3106 - User's Guide

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Revision	Brief Description of Changes	**Date of Issue**
0.2	Preliminary version.	**04-2019**
1.0	Updated sections: - Section 1/ Introduction - Section 1.3.1 Main Features - Section 1.3.2 Block Diagram - Section 1.3.3 Ordering Information - Section 1.3.6 Technical Specification o Functional block diagram removed (duplicated with section 1.3.2) - Section 2.3 Board Configuration - Section 2.7.1 M.2 Module Insertion / Removal Instructions - Section 3.8 Write Protect Mode - Section 5.3.2 Processor Thermal Monitoring - Section 5.3.3 External Thermal Regulation Updated tables: - Table 1: VX3106 Order Codes - Table 2: Associated Product Order Codes - Table 3: Front I/O Interfaces - Table 4: Rear I/O Interfaces - Table 5: Peripheral Connectivity - Table 6: VX3106 Main Characteristics - Table 11: VX3106 Weights - Table 12: VX3106 MTBF Data - Table 44: VPX Connector P1 Wafer Assignment	**05-2023**

Customer Support

Please contact our support team at support.KFR@kontron.com

Customer Service

As a trusted technology innovator and global solutions provider, Kontron extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly-experienced support enables Kontron to provide exceptional peace of mind to build and maintain successful products.

For more details on Kontron's service offerings such as: enhanced repair services, extended warranty, Kontron training academy, and more visit http://www.kontron.com/support-and-services/services.

Customer Comments

If you have any difficulties using this user guide, discover an error, or just want to provide some feedback, contact Kontron support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user guide on our website.

Symbols

The following symbols may be used in this user guide

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
NOTICE	NOTICE indicates a property damage message.
	**Electric Shock!** This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	**ESD Sensitive Device!** This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	**HOT Surface!** Do NOT touch! Allow to cool before servicing.
	**Laser!** This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol indicates important information which must be read carefully.
	This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!

Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

General Instructions on Usage

In order to maintain Kontron's product warranty and CE compliance, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty and CE compliance.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Environmental protection is a high priority with Kontron.
Kontron follows the WEEE directive
You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

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1/ Introduction

The VX3106 is the first member of a full range of 3U VPX High-Performance, Low Power dissipation Kontron range of products featuring QorIQ 'Layerscape' multicore ARM processors coupled with up to 16GB DDR4 memory.

The VX3106 offers a tailorization of its power consumption and its performance, thanks to the pinout compatibility of NXP Layerscape QorIQ processor and the outstanding flexibility of its design and this makes it well-suited to transportation, industrial and defense applications.

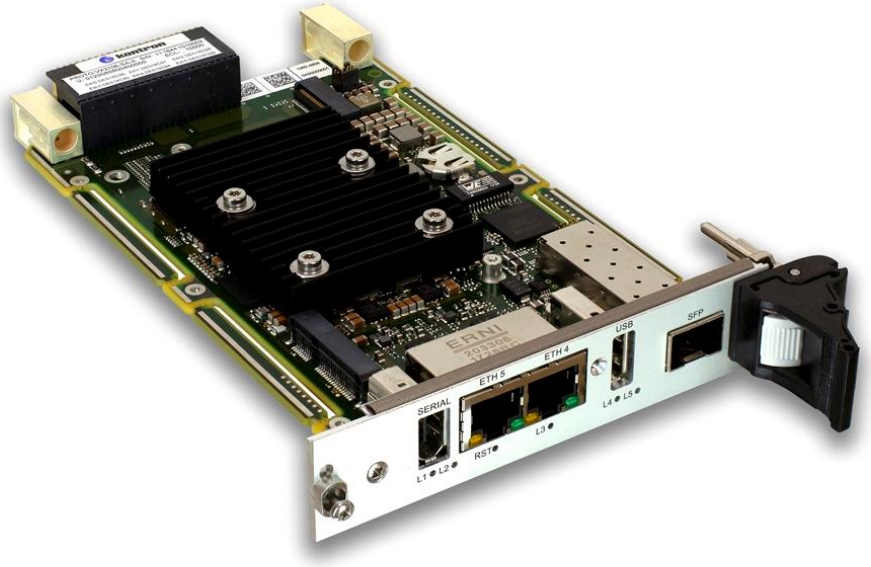
The VX3106 board comes with u-boot firmware and supports Linux. It is covered by Kontron's long term supply program, which guarantees customers multi-year supply of the product beyond its active life.

The Kontron VPX blade VX3106 is the ideal building block for parallel computing workloads where a cluster of Kontron VX3106s can be used in switched OpenVPX environments.

The VX3106 provides one 1000BASE-T port, two 1000BASE-KX ports and 1 lane Gen3 PCI Express to the backplane. Kontron VxFabric™ technology provides a TCP/IP protocol over the PCI Express infrastructure towards the application. A unique API with TCP/IP sockets makes it a powerful, leading edge Multi-CPU computing node architecture.

The VX3106 provides exceptional I/O capabilities onboard and outstanding flexibility by being a 3U VPX board providing support of different form factor mezzanine cards such as miniPCIe, M.2 storage and M.2 PCIe mezzanine cards.

Figure 1: VX3106-SA/WA Overview



1.1. Manual Overview

1.1.1. Objective

This guide provides general information, hardware instructions, operating instructions and functional description of the VX3106-SA/WA board. The onboard programming, onboard firmware and other software (e.g. drivers and BSPs) are described in detail in separate guides (see section 1.7 "Related Publications").

This hardware technical documentation reflects the most recent version of the product. The "Release Notes" (see section 1.7"Related Publications") might help to keep track of potential evolutions.

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

1.1.2. Audience

This guide is written to cover, as far as possible the range of people who will handle or use the VX3106-SA/WA, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, system, cabling, grounding and communications.

1.1.3. Scope

This guide describes SA/WA variants of the VX3106 series.

1.1.4. Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- Chapter 1 - Introduction (this chapter)
- Chapter 2 - Installation
- Chapter 3 - Additional Board Features
- Chapter 4 - Physical I/O
- Chapter 5 - Power and Thermal Specifications

1.1.5. Terminology, Definitions and Abbreviations

In this document, the term:

- VX3106-xx will be associated to the 3U VPX board including VX3106 modules:
  - VX3106-SA will be associated to the standard air-cooled commercial version of the board.
  - VX3106-WA will be associated to the extended air-cooled temperature version of the board.
  - VX3106-RA will be associated to the rugged air-cooled version of the board.
  - VX3106-RC will be associated to the rugged conduction-cooled version of the board
- VX3106-RTM will be associated to the 3U VPX Rear Transition Module (RTM) PB-VX3-401 or PB-VX3-411.

Abbreviations

TBD	To Be Defined. Information not available at the time this document was released.
TDP	Thermal Design Power
PTU	Power Thermal Utility

1.2. VPX Overview

VPX (VITA 46) specifications establish a new direction for the next revolution in bus boards. VPX is an ANSI standard which breaks out from the traditional connector scheme of VMEbus to merge the latest in connector and packaging technology with the latest in bus and serial fabric technology. VPX combines best-in-class technologies to assure a very long technology cycle similar to that of the original VMEbus solutions. Traditional parallel VMEbus will continue to be supported by VPX through bridging schemes that assure a solid migration pathway.

For further information regarding this standards and its use, visit the home page of the VITA - Open Standards, Open Markets (http://www.vita.com)

1.3. Board Overview

1.3.1. Main Features

NXP QorIQ® 'Layerscape®' LS1046A Architecture

The QorIQ LS1046A is a cost-effective, power-efficient, and highly integrated System-on-Chip (SoC) design that extends the reach of the line of QorIQ communications processors, featuring power-efficient quad 64-bit ARM® Cortex®-A72 cores with ECC-protected L1 and L2 cache memories for high reliability, running from 1.2 GHz up to 1.8 GHz. The LS1046A processor coupled with a DDR4-2100 memory includes a Neon SIMD Co-processor and DP FPU.

The VX3106 running the Quad-Core 1.2 GHz LS1046A processor features the outstanding performance of 27.3k DMIPS / 30.1k Coremark in a power dissipation budget which does not exceed 12 W.

Soldered DDR4 Memories with the Support of ECC

The processor accesses one memory-channels (72-bit) having a total size of 4, 8 or 16 GB. The DDR4 memory technology used operates up to 2,100 MT/s. An 8-bit ECC memory is implemented to detect and correct errors.

Numerous Storage Interface and Non Volatile Memories

The following storage features are available :

- An onboard eMMC 4.5 Flash with 32 GB or 64GB capacity (Multiple Levels Cell).
- Redundant 128 Mbits serial NOR flash memories are used to store firmware code.
- Two serial 256 Kbits EEPROMs are dedicated to system and VPD data storage.
- A 1 Mbits ferroelectric, non-volatile random access memory allows the backup of critical data when the board is powered off. This 1 Mbits ferroelectric RAM is a user memory device.

All the Flash and non volatile memories onboard have a write protect mechanism taking into account the NVMRO (Non Volatile Memory read Only) VPX signal. For further details, see section 3.8 "Write Protect Mode".

Backplane Switch

Three Gigabit Ethernet links and up to two 1x PCI express gen 2 link without Non Transparent (NT) capability are available on P1 connector.

Extensive I/O Connectivity

The VX3106 provides:

- Three 10/100/1000BASE-T(X) Ethernet interfaces, two on front and one on rear,
- One Ethernet SFP cage interface,
- Two 1000BASE-KX interfaces on rear P1 connector,
- Up to four EIA-232 serial lines,
- Five general purpose I/Os (GPIO),
- Up to three USB links,
- Two M.2 slots, one for SATA storage and one for PCIe, M.2 PCIe slot is exclusive with second PCIe link on backplane and it depends on build option.
- One miniPCIe slot

Legacy Compatibility

The VX3106 has been design to offer rear legacy I/O compatibility with Kontron's line of x86 and Power VPX SBCs, supporting the same Rear Transition Module. The net effect of this fit form function compatibility is to allow our customers an easy line replacement policy of the SBC in deployed systems.

Software

Kontron is one of the few compact PCI, VME and VPX vendors providing in-house support for most of the industry-proven real-time operating systems that are currently available.

Thanks to its close relationship with the software editors, Kontron is able to locally produce and support BIOS, BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology which follow silicon evolution.

Finally, Kontron offers to its customers owners of a maintenance agreement a hotline software support and regular software updates.

A dedicated web site is also available for online updates and release downloads.

The VX3106 is delivered with the Open Source U-BOOT firmware .

The VX3106 supports the Open Source Yocto framework for creating Linux distribution for embedded applications.

Contact Kontron for further information regarding other operating systems and software support.

Harsh Environments

Designed specifically for harsh environments, the VX3106 is ideal for applications where high reliability and survivability are a must. Available in Kontron air- and conduction-cooled ruggedization levels, the VX3106 also aims Natural Convection cooled applications.

10-year Long Life Cycle

Investing in a new project is always a challenge and risky. Maximizing the lifetime of an application is therefore a critical issue when it comes to saving development investments.

The VX3106 has been designed with long life cycle components. Beyond the use of standard commercially available components, Kontron offers longevity of supply services (LTS) which are designed to make the VX3106 available for over 15 years.

A comprehensive Health Management is optionally available to support easy field maintenance. All this makes the VX3106 the ideal candidate for long term programs.

Rear Transition Module

The VX3106 supports the PB-VX3-411, a 3U VPX Rear Transition Module compliant with the definition of the Rear Transition Module on VPX standard - VITA 46.10. See document ref CA.DT.B03-0e "3U-VPX Rear Transition Module User's guide" .

It offers connectivity on the rear:

- one Ethernet SFP cage operating at 1 Gbits/s (ETH A port).
- one Ethernet 1000BASE-T port (ETH B port)
- one SATA III ports
- two serial COM ports
- one USB3.0 / USB2.0 port (USB A-B port)
- one USB2.0 port (USB-D port)
- three GPIOs

Figure 2: PB-VX3-411 RTM Overview

Security Solution

The key for Kontron with this new VPX board is security. The VX3106 is provisioned with a security chip to enable the support of Kontron's Embedded Security Solution - Approtect.

Kontron Approtect is a combined hardware and software technology ensuring IP and copy protection while avoiding reverse engineering and tampering. Kontron Approtect is a holistic hardware based security solution that provides customers the ability to address security needs at the application layer. Learn more about the security solution

Approtect here: Security Solution - Approtect

Kontron TPM (Trusted Platform Module) secures system software by enabling trusted boot operation on Linux with x86 and by verifying local or remote attestation. It ensures secure SSL/TLS network communication by enabling authentication and by providing associated certificate and private keys

1.3.2. Block Diagram

Figure 3: VX3106 Block Diagram

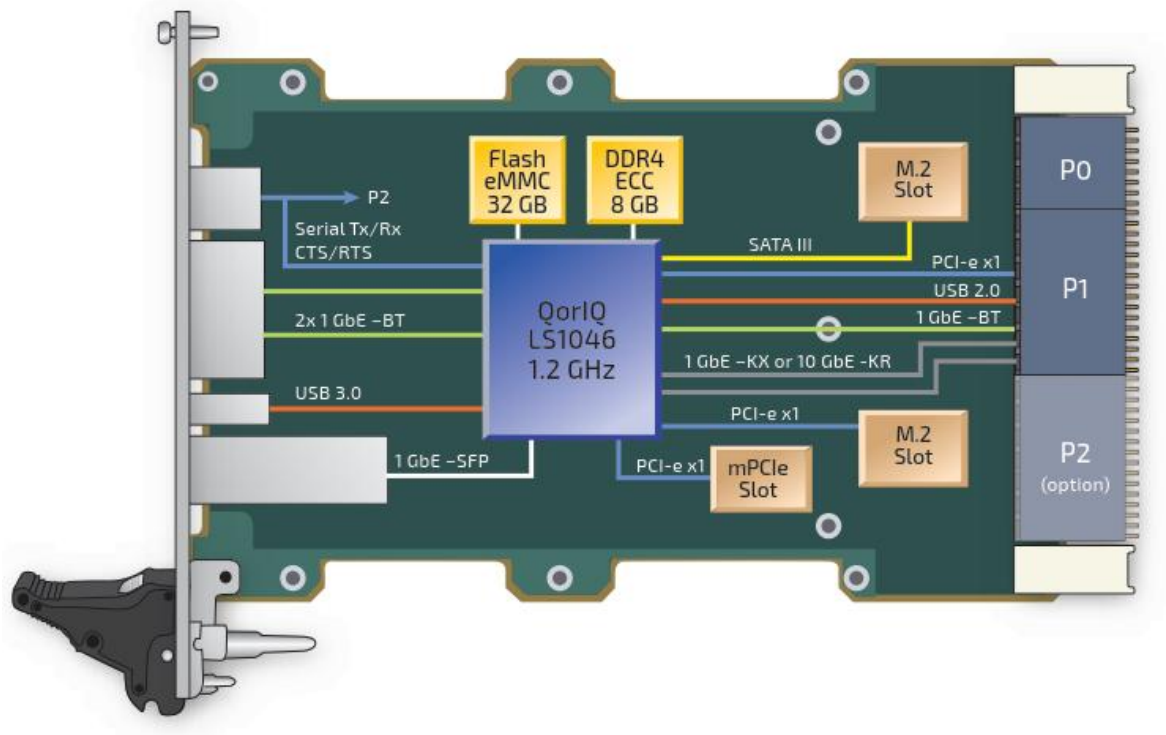
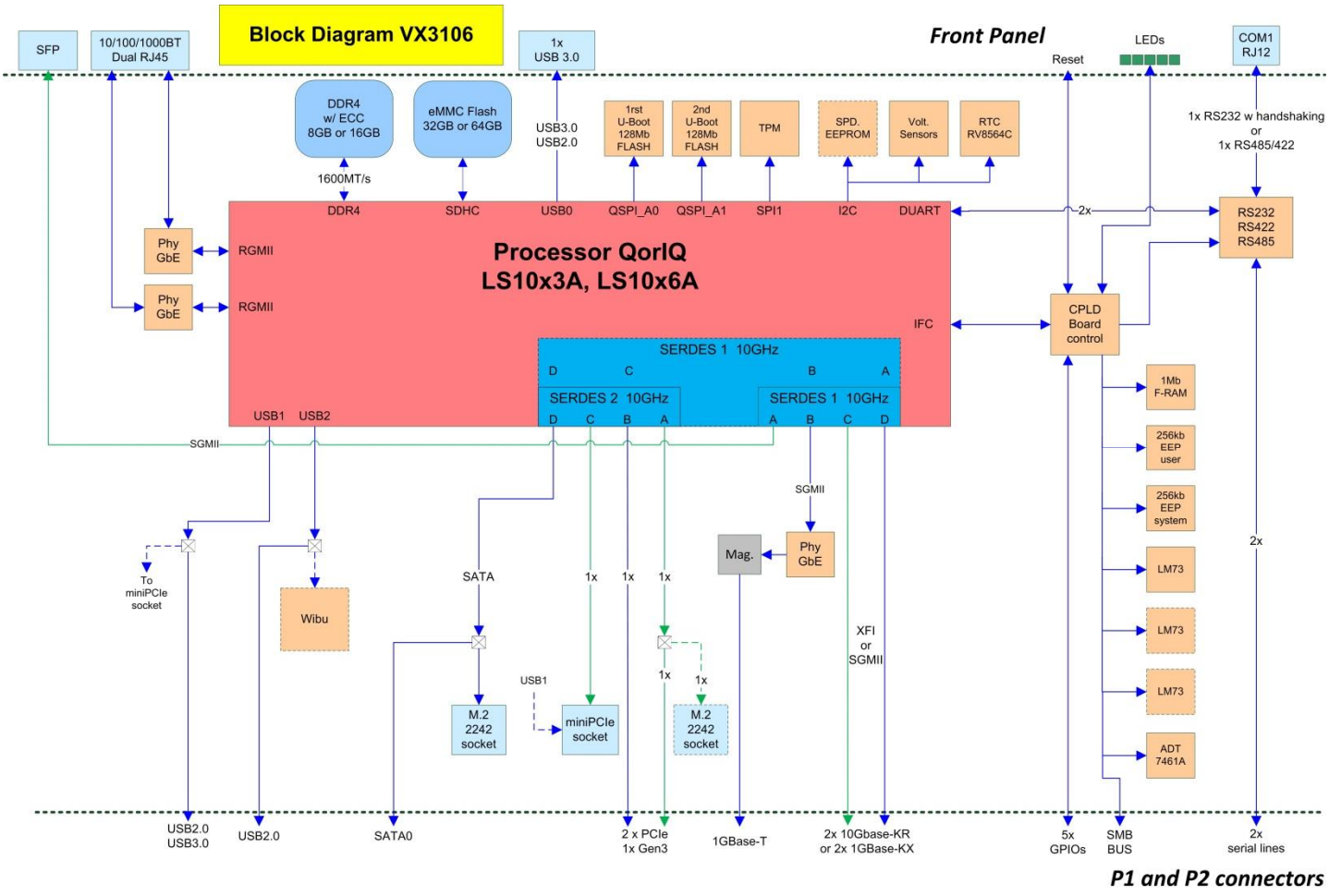


Figure 4: VX3106 Functional Block Diagram



VX3106 offers on rear VPX P1 connector two 1000BASE-KX ports by default. These ports are scalable to 10GBASE-KR under certain conditions. Please contact Kontron support for availability.

1.3.3. Ordering Information

Manufacturing Options

CPU Frequency:	1.2GHz (quad-core)
DDR4 SDRAM Size:	4GB total onboard 8GB total onboard 16GB total onboard *
Ruggedization Levels :	Standard Air-Cooled (SA) Extended Temperature (WA) Natural Air-Cooled (NC) * Rugged Conduction-Cooled (RC) *
eMMC Flash Size :	32GB 64GB
P2 connector :	Present (including two serial lines) Absent
Module socket :	PCIe on M.2 bottom socket Absent
Ethernet:	two 1000BASE-KX on rear P1 connector
Secure Element :	TPM/Wibu TPM 2.0 Wibu (exclusive with USB2.0 port 2 on P0 connector) Not equipped
Battery:	Present Absent (including holder)
Serial line:	two serial line (COM1 and COM2) with handshaking on P2 four null-modem serial line (COM1 to COM4) on P2
Power-on Built-In-Test:	Absent PBIT object run time
Slot pitch:	1 inch
Coating (for SA only)	

Available Order Codes

Table 1: VX3106 Order Codes

Environ-mental Class	Standard Order Codes	Description
SA	VX3106-SAnm-xyzs0tu	3U single slot 5 HP (1.0") VPX SBC, 1.2 GHz QorIQ, Air-Cooled (0°C to +55°C). **Available options:** **Processor type:** **n=2**: Dual core LS1026A processor **n=4**: Quad core LS1046A processor **Memory size:** **m = 4**: 4 GB DDR4-1600 SDRAM with ECC **m = 8**: 8 GB DDR4-1600 SDRAM with ECC **eMMC option:** **x = N**: No soldered Flash **x = 0**: 32 GB eMMC MLC flash **x = 2**: 64 GB eMMC MLC flash **Mezzanine option:** **y = 0**: M2 PCIe bottom slot, M2 SSD top slot, mPCIe slot **y = 1**: M2 SSD top slot, mPCIe slot, no PCIe M.2 Type 2242/2260 **I/O feature option:** **z = 0**: P1 with dual 1000BASE-KX control plane, one x1 PCIe data plane, 5 GPIOs, 1 USB2.0. No P2 connector **z = 1**: P1 with dual 1000BASE-KX control plane, one x1 PCIe data plane, 2 USB2.0, 1 USB3.0, 5 GPIOs. No P2 connector **z = 2**: P1 with dual 1000BASE-KX control plane, two x1 PCIe data plane, 5 GPIOs, 1 USB2.0. No P2 connector **z = 3**: P1 with dual 1000BASE-KX control plane, two x1 PCIe data plane, 2 USB2.0, 1 USB3.0, 5 GPIOs. No P2 connector **z = C**: P1 with dual 1000BASE-KX control plane, x1 PCIe data plane, 5 GPIOs, 1 USB2.0. P2 connector with serial lines **Security option:** **s = 0** : no hardware secure element **s = 1** : hardware secure element equipped (TPM and Approtect , CodeMeter(tm) Secure element for AppProtect. One USB2.0 removed from P1). **Other option:** **t = 0** : standard **t = P** : with PBIT **u = 0** : No coating **u = V** : Conformal Coating option on 'SA' build

Table 2: Associated Product Order Codes

Environ-mental Class	Standard Order Codes	Description
SA	PB-VX3-401	Without SLM (PIM-VX3-410-1) **Main Features :** ▸ VPX Rear I/O ▸ One Ethernet SFP cage operation at 1 Gbits/S ▸ One Ethernet 1000BASE-T port ▸ Up to two SATA III ports ▸ Two serial COM ports ▸ One USB 3.0 / USB 2.0 port ▸ Up to 5 GPIOs ▸ One mini display port (1) ▸ One I2c bus connector
SA	PB-VX3-411	With SLM (PIM-VX3-410-1) **Main Features :** ▸ PB-VX3-401 Features + ▸ Up to two SATA III ports ▸ 3 USB 2.0 ports (2) ▸ One mini DisplayPort (1)
SA	1064-4995	Serial Console Cable Adapter

Refer also to the product datasheet for the available order code list.

Notes:

(1) There is no DisplayPort on the VX3106 board

(2) Only port USB-D is connected to the VX3106. Availability of this USB port depends on VX3106 building option.

1.3.4. I/O Interfaces

Front Interfaces

Not available on RC (Rugged Conduction-Cooled) boards

Figure 5: VX3106-SA Front Panel I/O Interfaces

Table 3: Front I/O Interfaces

FUNCTION	DESCRIPTION	SEE ALSO
Serial Ports	2x EIA-232 w/ flow control or 1x EIA-485 UART interface for CPU on IEEE1394 connector.	Section 4.1.1 for Pin Assignment
Gigabit Ethernet	Two 10/100/1000BASE-T(X) ports on RJ45	Section 4.1.2 for Pin Assignment
USB	USB 2.0 or USB 3.0 interface on USB type A connector	Section 4.1.3 for Pin Assignment
SFP Cage	One single SFP cage supporting 1000BASE-T or 1000BASE-X module	Section 4.1.4 for Pin Assignment
Reset	Reset push button	Figure 4
LEDs	5 LEDs reporting the board CPU health status and activity	Section 4.4 for LEDs Description

Figure 6: Reset Button and LEDs

Rear Interfaces

Rear interfaces are compliant with the following slot profiles:

- SLT3-PAY-2F2U-14.2.3
- SLT3-PAY-1F12U-14.2.4
- SLT3-PAY-1F1U-14.2.10

Figure 7: VX3106-SA Rear I/O Distribution

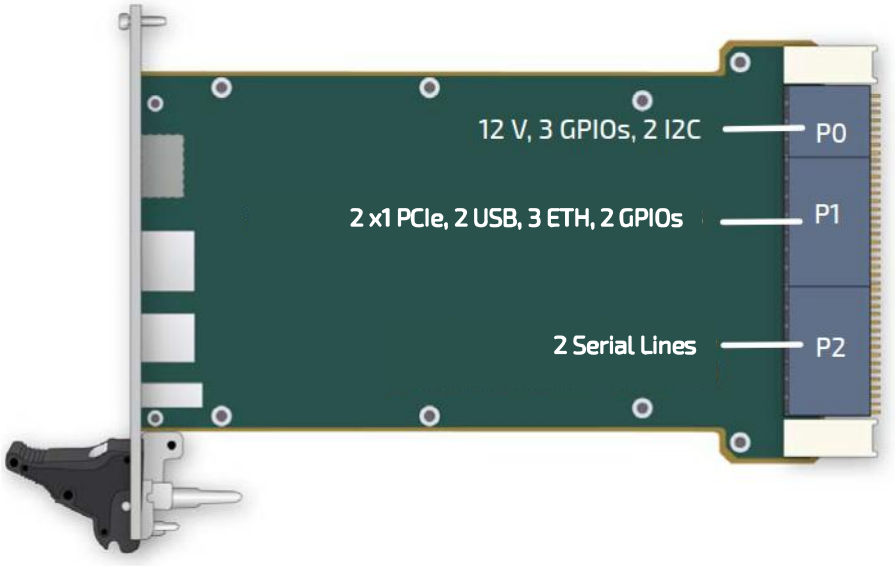


Table 4: Rear I/O Interfaces

FUNCTION	DESCRIPTION	SEE ALSO
PCI Express	▸ 1 x1 gen 2 PCIe w/o non transparent capability on P1. 1 additional x1 gen 2 PCIe on build option.	Section 4.3 for VPX Connectors Description
SATA Storage	▸ 1 SATA III link on P1 (dynamically selectable with M.2 socket)	
USB	▸ 2 USB 2.0 and 1 USB 3.0 links on P2 (depending on build option)	
Gigabit Ethernet	▸ 2 SerDes 1000BASE-KX on P1 ▸ 1 1000BASE-T on P1	
Serial	▸ 2 asynchronous EIA-232 w/ flow control or 2x EIA-485 UART serial line on P2 ▸ 4 asynchronous EIA-232 without flow control, on P2 (depending on build option)	
GPIOs	▸ 2 User GPIOs on P1, including OpenVPX GDISCRETE1, and MASKABLE RESET ▸ 3 additional GPIOs on P0, replacing unused JTAG pins	
Utilities	On P0 and P1: SYSRESET, SYSCON, 6 Geographical Addresses	
I2C	IPMB-A/B I2C busses	
Clocks	Optional in VITA65 and not connected on VX3106	
Power Supplies	VS1=12V; VS2 not used; VS3=5V not used(1) +12V_AUX is optional in VITA 46 and not connected on VX3106. -12V_AUX is optional in VITA 46. It is not used internally on VX3106	

FUNCTION	DESCRIPTION	SEE ALSO
	3.3V_AUX is mandatory in VITA 46. However, if absent, it will be generated internally.	

(1) VS3 VPX backplane power supply (5 Volts) is required when using PB-VX3-4xx Rear Transition Module.

Peripheral Connectivity

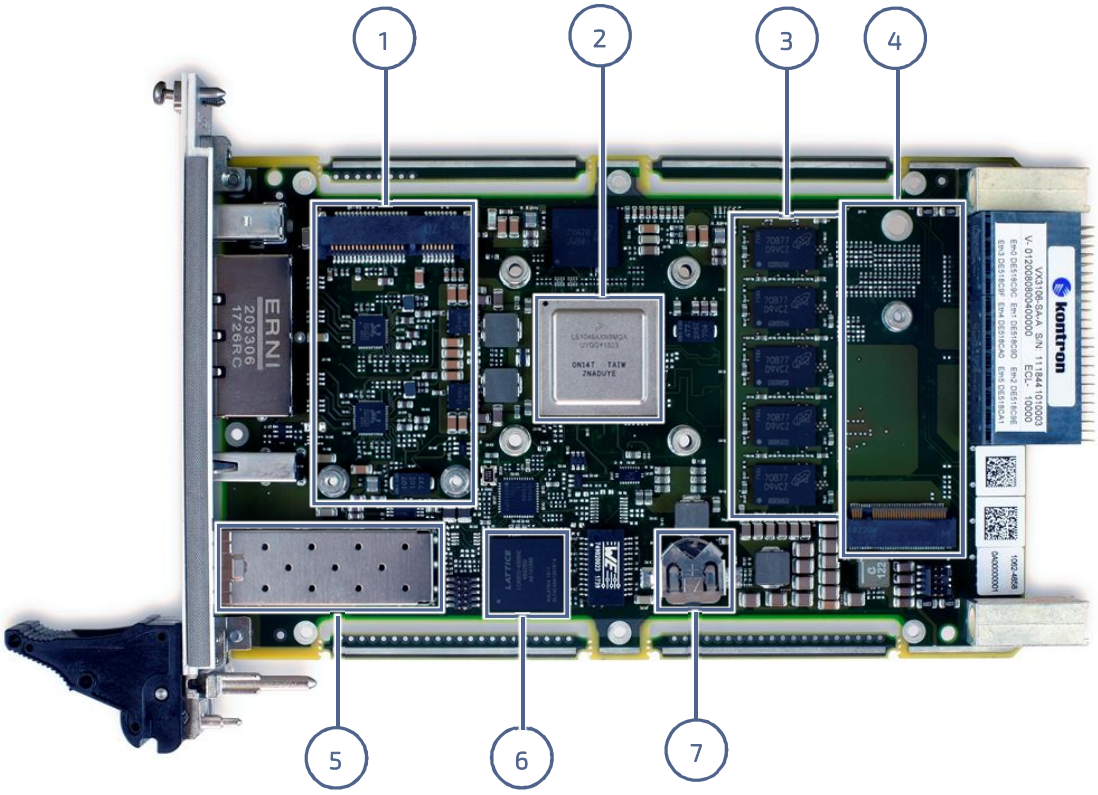
Table 5: Peripheral Connectivity

FUNCTION	VX3106		PB-VX3-411 RTM	
	Front Panel	On-board	Front Panel	On-board
Gigabit Ethernet	Y (x3)	-	Y (x2)	-
USB0	Y	-	-	-
USB1	-	Y (*)	Y (*)	-
USB2	-	-	Y (*)	-
SATA	-	Y (*)	-	Y (*)
COM1	Y	-	Y (*)	-
COM2	-	-	Y (*)	-
COM3	Y (*)	-	Y (*)	-
COM4	-	-	-	-
GPIOs	-	-	-	Y (up to 5)
LED	Y (x5)	-	-	-
Reset Button	Y	-	-	-
SMB	-	-	-	Y
PCIe (miniPCIe and M.2)	-	Y (x2)	-	-

(*) depends on VX3106/PB-VX3-411 building option

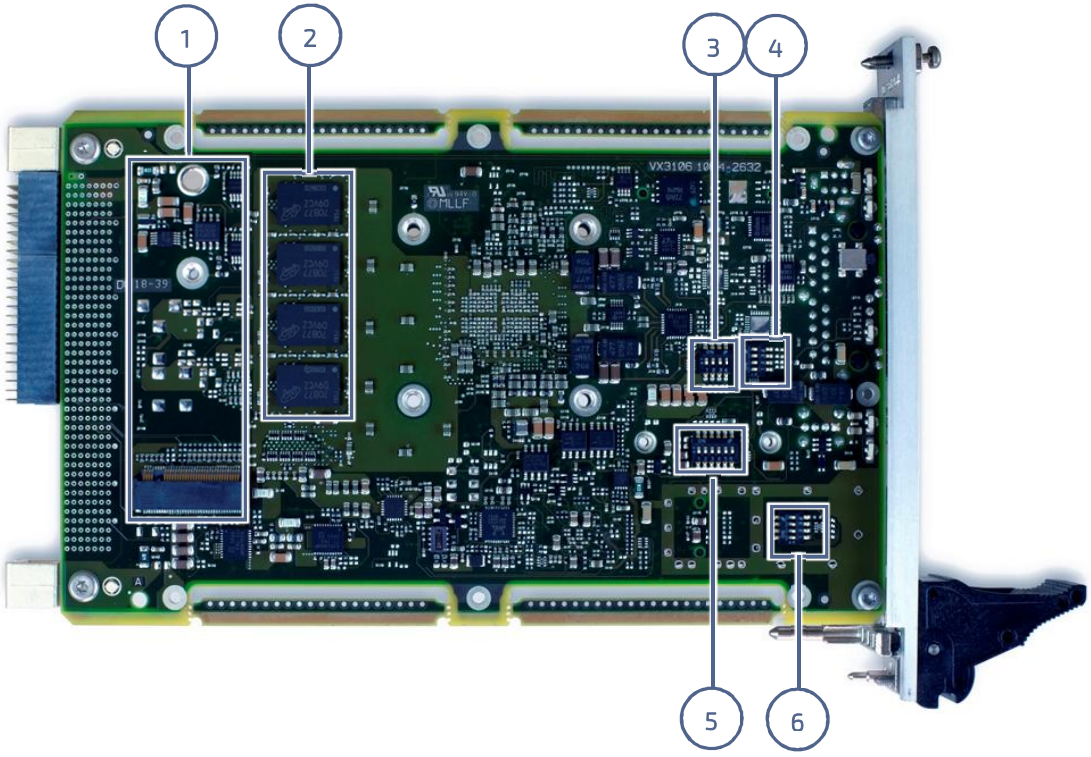
1.3.5. Components Layout

Figure 8: VX3106 Components Layout (Top view)



1. MiniPCIe Slot
2. QorIQ LS10x6
3. DDR4-SDRAM
4. Sata M.2 Slot
5. SFP cage
6. CPLD
7. Battery

Figure 9: VX3106-SA Components Layout (Bottom view)



1. PCIe M.2 Slot
2. DDR4 SDRAM
3. MicroSwitchSW3
4. MicroSwitchSW4
5. MicroSwitchSW1
6. MicroSwitchSW2

1.3.6. Technical Specification

Table 6: VX3106 Main Characteristics

Form Factor	
Form Factor	3U VPX, single slot, 1 inch pitch
SoC : QorIQ Layerscape	
Processor	One NXP QorIQ Layerscape LS1046A quad-core 64-bit ARM® Cortex®-v8 A72 based processor speed up to 1.8GHz. 2 MB L2 cache Neon SIMD Co-processor Power dissipation lower than 12W for 1.2GHz version. 28-nanometer silicon technology.
Memory Controller	Integrated 72 bits DDR4 memory controller with ECC support up to 2100 MT/s. Limited to 1600 MT/s for 1.2GHz version.
PCI Express Interface	1 lane 5 GT/s gen2 PCIe to P1 connector 1 lane 5 GT/s gen2 PCIe to P1 connector (or M.2 slot depending on build option) 1 lane 5 GT/s gen2 PCIe to miniPCIe slot
SATA	Up to 6 Gb/s integrated Serial ATA host controllers 1 SATA port on M.2 socket or P1 (dynamically selectable from firmware)
USB	1 USB 2.0 port on P1 or miniPCIe socket (depending on build option) 1 USB 2.0 port on P1 or on WIBU device (depending on build option) 1 USB 2.0 port on front panel 1 USB 3.0 on P1 connector
Ethernet Controllers	Two Gigabit Ethernet controllers using RGMII Interface Four Gigabit Ethernet controllers using SGMII interface and supporting 1000Base-KX
eMMC Controller	Compatible with the MMC system specification version 4.5
QSPI	Connects to two QSPI flash devices (128 Mbits each)
IFC	16-bit 100 MHz, for CPLD link
DUART	2 DUART interfaces offering 2 Tx/Rx serial lines w/ handshaking or 4 simplified Tx/Rx serial lines (depending on build option)
Package	23 mm X 23 mm, 0.8 mm pitch, 780 pin FC-PBGA Unlidded
Memory / Storage	
System Memory	Up to 16 GB DDR4 SDRAM at 1600 MT/s, one memory channel. 8GB is standard option, 16GB build option available.
SPI Flash	Firmware Boot Device, 2x 128 Mbytes.
eMMC Flash	32GB 4-bit eMMC 4.5 MLC flash, 64GB in option
F-RAM	F-RAM 1 Mbit of non-volatile ferroelectric RAM

EEPROM	One serial 256 Kbit EEPROM dedicated to VPD data One serial 256 Kbit EEPROM dedicated to system data
On-board Controller	
Watchdog	Five watchdog timers with configurable timeout counter with timeout periods from 0.5 to 128 seconds, generates IRQ or reset or IRQ/reset cascaded (cPLD implementation) cPLD watchdog also available.
Ethernet PHY	Three Ethernet PHYs offering Ethernets 10/100/1000 BASE-T(X) port. Two Ethernet PHYs are connected to the SoC through 2x RGMII links and one through SGMII link.
System CPLD	One CPLD Board controller for power sequencing, reset handling, monitoring, failure detection, VPX I2C communication. Provides configuration/status registers on IFC interface
Mezzanines slots	
miniPCIe slot	PCIe x1, Gen2 and USB 2.0 (exclusive with P1 build option) interfaces +1.5V, +3.3V power supplies, 2.3W max on 1.5V Full-mini card 52 pin count
SATA M.2 top slot	SATA Gen3 interface (exclusive with P1 connector) +3.3V ±5% power supply, 2.5A max Type 2242, 2260, including D5, Key M
PCIe M.2 bottom slot	x1 PCIe Gen2 interface (exclusive with P1 connector) +3.3V ±5% power supply, 2.5A max Type 2242, 2260, except D5, Key M
System Rear Interconnection	
VPX slot profiles	SLT3-PAY-2F2U-14.2.3 SLT3-PAY-1F1F2U-14.2.4 SLT3-PAY-1F1U-14.2.10 SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16 (including in new VITA65.0 standard)
Ethernet	2 x 1000BASE-KX on P1 1 x 10/100/1000Base-T(X) on P1
USB Ports	2 x high-speed USB Ports on P1. 1 x super-speed USB Port on P1.
SATA Ports	1x SATA Ports on P1 (dynamically selectable with M.2 socket)
Serial Ports	4 x RS232 Serial Ports on P2 (build option).
GPIO	2 x GPIOs on P1 and 3 x GPIOs on P0 (depending on build option)
VPX SMB buses	Two SMB 100KHz buses from cPLD: one master/slave and one master only available on P0.
Front Interface	
Gigabit Ethernet	2 x 10/100/1000Base-T(X) on dual RJ45 connectors. 1 x 1000BASE-T copper modules or 1000BASE-X optical modules on SFP cage

Serial Port	2 x RS232 UART interfaces w/o handshaking, IEEE1394 connector.
USB Port	1 x USB 2.0 port for storage or keyboard/mouse
Reset	One Reset button and Shelf Manager control (SMB command on VPX)
LEDs	Five Bicolor LEDs on front panel.
Various Interfaces	
CPU debug Interface	JTAG debug connector for CodeWarrior TAP
Board Temperature	TMP on-chip thermal sensor and remote processor thermal diode. One LM73 thermal sensors.
Misc	
Battery	CR1220 on board socket
RTC	External RTC module RV8564C2 with I2C bus
Firmware	U-Boot 2016.092.0+g2735535
Backplane Power Supply	VS1: +12V +5%/-5% only fully protected by fuse. +3.3V +5%/-5% standby optional voltage VS2 and VS3 not used +12V and -12V standby voltage not used
Power Consumption	About 18W without mezzanines, without options, without peripherals/devices. This does not include the power dissipation due to the DC/DC efficiency when mezzanines, options and external peripherals/devices are used.
Operating temperature Range	1.0'' SA : 0°C to +55ºC with 1 slot 1.0" passive module heat sink, forced system airflow (depending on the processor frequency) 1.0'' WA : -20°C to +65ºC with 1 slot 1.0" passive module heat sink, forced system airflow (depending on the processor frequency)..
Humidity	SA class: 90% RH (non condensing) WA class: 95% RH (non condensing)
Options / Companion board	
RTM	PB-VX3-411
CodeWarrior TAP	CPU JTAG emulator probe

1.3.7. M2 and miniPCIe Module List

Table 7: Non-exhaustive miniPCIe module list, tested on VX3106 miniPCIe slots

Module Type	Capacity	Memory Technology	Manufacturer	Part Number	Note
Mini PCIeDOM 1IE3	32GB	iSLC	Innodisk	DHEDM-32GD09BW1DC	

Table 8: Non-exhaustive M.2 module list, tested on VX3106 M.2 slots

Module Type	Capacity	Memory Technology	Manufacturer	Part Number	Note
SSD SATA, type M, 2260	128GB	MLC	Unigen	UBM4SM0128HCM1-ETG-UGN	

1.4. Environmental Specifications

Table 9: VX3106 Environmental Specifications

	SA STANDARD COMMERCIAL			WA EXTENDED TEMPERATURE			RC RUGGED CONDUCTION-COOLED
Conformal Coating	Optional			Standard			Standard
Cooling Method	Convection			Convection			Conduction
Operating Temperature	0° to +55°C			-20° to +65°C			-40° to +85°C
Storage Temperature	-40° to +85°C			-45° to +100°C			-50° to +100°C
Vibration Sine (Operating)	20-500 Hz - 2g Acceleration / Frequency Range			20-500 Hz - 2g Acceleration / Frequency Range			22-2,000 Hz - 5g Acceleration / Frequency Range
Random	f (Hz)	10	40	100	200	2000	5Hz to 100Hz +3dB/octave 100Hz to 1000Hz 0.1g²/Hz 1000Hz to 2000Hz -6dB/octave
	PSD (g2/Hz)	0.01	0.01	0.0007	0.0007	0.00005	
Shock (Operating)	20g/11 ms Peak Accel./ Shock Duration Half Sine			20g/11 ms Peak Accel./ Shock Duration Half Sine			40g/20 ms Peak Accel./ Shock Duration Half Sine
Altitude (Operating)	-1,500 to 60,000 ft			-1,500 to 60,000 ft			-1,500 to 60,000 ft
Relative Humidity	90% non-condensing			95% non-condensing			95% non-condensing

Table 10: VX3106 Lab-grade Environmental Specifications

Lab-grade air-cooled version (1" single height passive module heat sink, forced air)	
Conformal Coating	optional
Airflow	Refer to chapter 5.3.3
Cooling Method	Convection
Operating	10 °C to +30 °C

1.5. Board Weight

Table 11: VX3106 Weights

BOARD WEIGHT	SA STANDARD COMMERCIAL	WA STANDARD COMMERCIAL
VX3106	250g(*)	< 300g

(*) Board without VPX P2 connector option.

1.6. MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

VX3106 MTBF Data

Table 12: VX3106 MTBF Data

MTBF	MILHDBK217F					
	GB		NS		ARW	AIC
	25 °C	40 °C	25 °C	40 °C	55 °C	40 °C
VX3106-SA44-00C0000	310,370 hrs	228,288 hrs	50,847 hrs	36,155 hrs	4,664 hrs	23,319 hrs

1.7. Related Publications

The following publications contain information relating to this product:

Table 13: Related Publications

PRODUCT	PUBLICATION
Standard	
ANSI/VITA 46.0	VPX Baseline Standard - ANSI/VITA 46.0-2007 [R2013]
ANSI/VITA 46.6	Gigabit Ethernet Control Plane on VPX, Feb 2013
ANSI/VITA 46.9	XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules, Nov 2010
ANSI/VITA 46.10	Rear Transition Module for VPX - ANSI/VITA 46.10-2009
ANSI/VITA 46.11	System Management on VPX, June 2015
ANSI/VITA 65	OpenVPX™ System Specification ANSI/VITA 65-2010 [R2012]
ANSI/VITA 48.2	Mechanical Specifications for Microcomputers using REDI Conduction Cooling Applied to VITA VPX
ANSI/VITA 47	Environmental, Design and Construction, Safety, and Quality for Plug-In Unit
Serial ATA	Serial ATA 3.0 Specification, revision 3.0
Mini PCIe	PCI Express Mini Card Electromechanical Specification, Revision 2.0, April 21 2012
M.2	PCI Express M.2 Specification, Revision 1.1
Hardware	
VX3106 Boards	VX3106 Hardware Release Notes D218964
PB-VX3-4xx RTM	3U-VPX Rear Transition Module User's guide CA.DT.B03-0e - November 2012
Firmware	
VX3106 Boards	VX3106 U_Boot User Manual D218963
Software	
VX3106 Boards	VX3106 Yocto Linux Release Notes D218953

2/ Installation

The VX3106 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

2.1. Safety Requirements

The following safety precautions must be observed when installing or operating the VX3106. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Special care shall be taken while handling the board: the heat sink or heat frame can get very hot during operation. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container before the board and heat sink have cooled down to room temperature

This board contains electrostatically sensitive devices. Observe the necessary precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

- Do not touch components, connector pins or traces.
- We strongly recommend our customers to work in an environment equipped with anti-static workbenches with professional discharging equipments

2.2. Board Identification

The VX3106 boards are identified by labels fitted to the top side of the board.

The E.C. Level format is "xxxxxLy" where

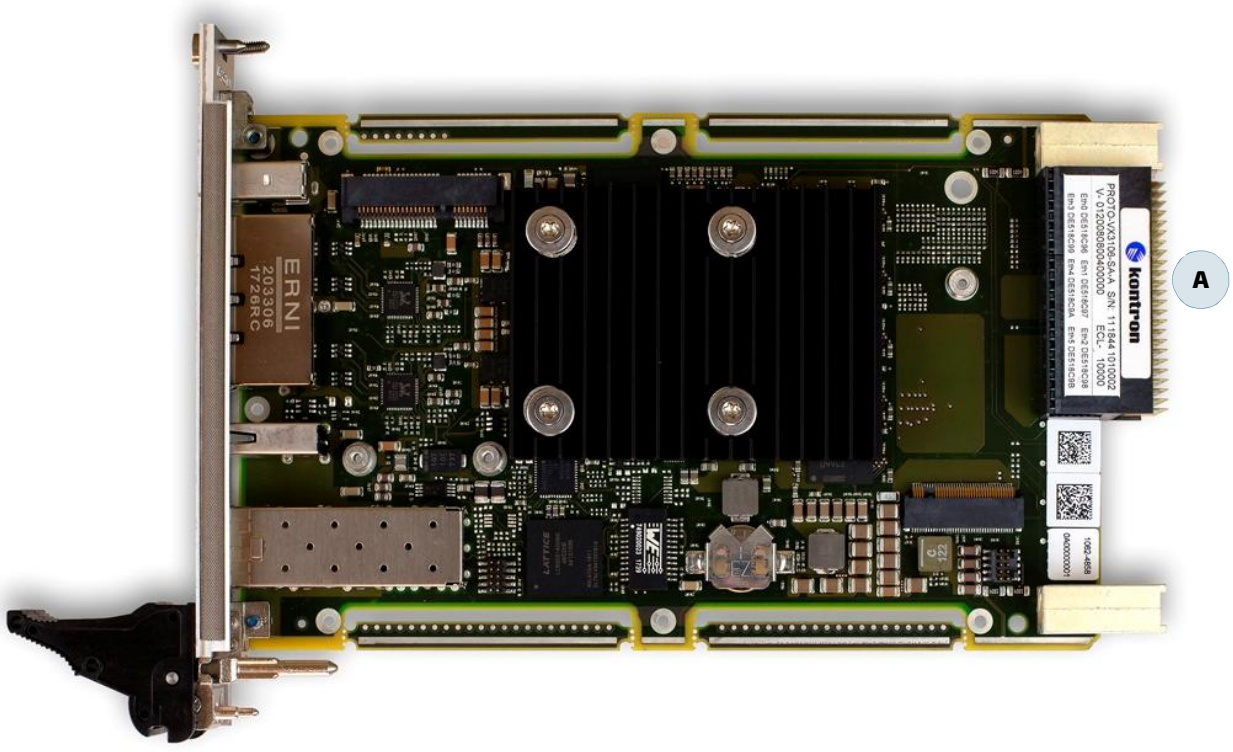
- The five digits "xxxxx" indicate the board E.C. Level (PCB revision included)
- "Ly" indicates the mechanical E.C. Level:
  - letter "L" varies with the environment class ("A" for SA, "B" for WA, "C" for RA and "D" for RC)
  - digit "y" gives the mechanical E.C. Level.

See also section "Vital Product Data" in "VX3106 U-Boot User Manual" – D218953 to display the VPD information stored in VX3106 EEPROM.

Top Side

A "Identification" label: Order Code, Serial Number, Variant, E.C. Level
Ethernet MAC addresses

Figure 10: VX3106 Identification (Top Side)

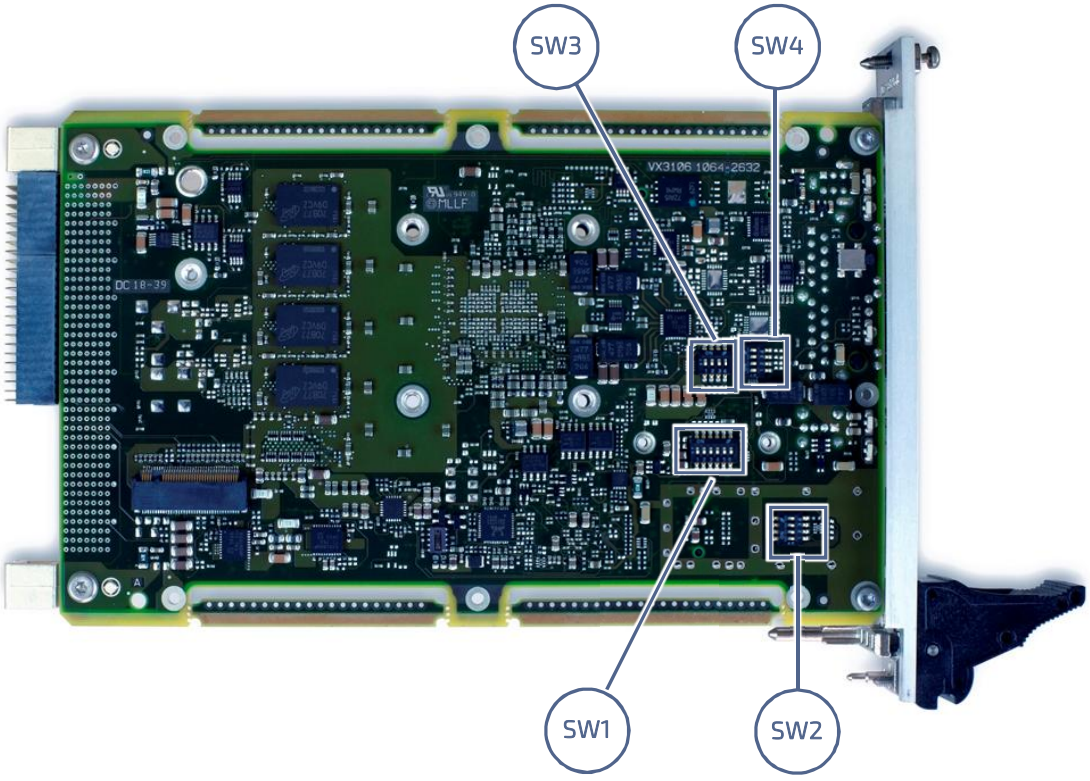


2.3. Board Configuration

2.3.1. Microswitches

Four microswitches are available on the VX3106: SW1, SW2, SW3 and SW4.

Figure 11: VX3106 Board Configuration (Bottom view)



2.3.2. SW1 Microswitch Description

Table 14: SW1 Microswitch Description

FUNCTION	DESCRIPTION
1 - Factory Mode	OFF: Normal Mode ON: Factory Mode (force special config for factory mode
2 - VPD (Vital Product Data) domain write protection	OFF: protected if NVMRO is active, or if CPLD register 0x9 bit 1 is at 1 (default is 1, so protected) ON : unprotected (even if protection is requested by NVMRO or CPLD register) "VPD" domain controls devices storing factory data : VPD EEPROM
3 – SYS domain write protection	OFF : protected if NVMRO is active, or if CPLD register 0x9 bit 2 is at 1 (default is 0, so unprotected) ON : protected "SYS" domain controls devices storing runtime data : System (OS) EEPROM
4 – USER domain write protection	OFF : protected if NVMRO is active, or if CPLD register 0x9 bit 3 is at 1 (default is 0, so unprotected) ON : protected "USER" domain contols devices impacted by a software update : FRAM (Ferroelectric RAM), QSPI boot flashes, CPLD internal flash
5 - Reserved	Always keep this switch OFF
6 - Debug Mode	OFF: Normal Mode ON: Debug Mode (reset from CPU disabled, LEDs reporting power sequencer state)

The System EEPROM contains the PBIT detailed results, so this data may not be updated if protection is active on the "SYS" domain.

The board's configuration (as set by u-boot command "kcfg") is stored in both System EEPROM (CPLD configuration) and QSPI flash (u-boot environment variables), so "SYS" and "USER" domain protections must be disabled to update the configuration settings.

2.3.3. SW2 Microswitch Description

Table 15: SW2 Microswitch Description

FUNCTION	DESCRIPTION
1 - System Boot Flash	OFF : boot on "main" QSPI flash ON : boot on "Rescue" QSPI flash for recovery purpose
2 – Firmware Failsafe Boot	OFF : Normal Mode ON : Start in failsafe mode using default CPLD and firmware configuration
3 - Reserved	Always keep this switch OFF
4 –NVMRO force off	OFF : NVMRO not forced to off (level 0) ON : force NVMRO off on backplane, also forcing it off on local board (useful if backplane does not have a switch to disable NVMRO)

2.3.4. SW3 Microswitch Description

These switches are user defined and their state can be read by software through CPLD register @0xE

Table 16: SW3 Microswitch Description

FUNCTION	DESCRIPTION
1 – User switch 1	Readback in register 0xE bit 4 (1 when ON)
2 – User switch 2	Readback in register 0xE bit 5 (1 when ON)
3 – User switch 3	Readback in register 0xE bit 6 (1 when ON)
4 – User switch 4	Readback in register 0xE bit 7 (1 when ON)

2.3.5. SW4 Microswitch Description

Table 17: SW4 Microswitch Description

FUNCTION	DESCRIPTION
1 – Reserved	Always keep this switch OFF
2 – Reserved	Always keep this switch OFF
3 – Reserved	Always keep this switch OFF
4 – Reserved	Always keep this switch OFF

2.4. Package Content

The VX3106 is packaged with several components. The packing contents of the VX3106 Series may vary depending on customer requests.

- CPU Module:
  - Order Code: see section 1.3.3 "Ordering Information" :
    - Processor specifications differ depending on Order Code.
    - Heat sink assembled on the board.
    - Battery assembled on the board.
  - Serial adaptation cable IEEE1395 <-> DB9 (Order Code: see section 1.3.3 "Ordering Information")

- Rear Transition Module:
  - Order Code: see section 1.3.3 "Ordering Information".
- Serial Cable:
  - Order Code: see section 1.3.3 "Ordering Information".

Figure 12: Serial Cable

2.5. Initial Installation Procedures

The following procedures are applicable only for the initial installation of the VX3106 in a system. Procedures for standard removal operations are found in their respective chapters.

To perform an initial installation of the VX3106 in a system proceeds as follows:

1. Ensure that the safety requirements indicated in section 2.1 are observed.

CAUTION: Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the power and thermal specification of the VX3106 see Chapter 5. For the installation of VX3106, specific peripheral devices and Rear I/O devices refer to the appropriate sections in current Chapter.

CAUTION: Care must be taken when applying the procedures below to ensure that neither the VX3106 nor other system boards are physically damaged by the application of these procedures.

3. To install the VX3106 perform the following:
   a. Ensure that no power is applied to the system before proceeding.
   b. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.

When performing the next step and when the chassis accommodating the board is compliant with VITA48.2, it is recommended to use the ejector handles to seat the board into the backplane connectors. For the other chassis, simply push the board into the backplane connectors.

   c. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.
   d. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
   e. Fasten the front panel retaining screws.
   f. Connect all external interfacing cables to the board as required.
   g. Ensure that the board and all required interfacing cables are properly secured.

The VX3106 is now ready for operation. For operation of the VX3106, refer to appropriate VX3106 specific software, application, and system documentation.

2.6. Standard Removal Procedure

ESD sensitive Device! Precautions are listed in chapter 2.1

To remove the board from the chassis proceeds as follows:

1. Ensure that the safety requirements indicated in Section 2.1 are observed. Particular attention must be paid to the warning regarding the heat frame!

CAUTION: Care must be taken when applying the procedures below to ensure that neither the VX3106 nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws
5. Disengage the board from the backplane by first unlocking the board ejection handle, press the handle until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.

CAUTION: Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

7. Dispose of the board as required.

2.7. Installation of Peripheral Devices

The VX3106 is designed to accommodate a variety of peripheral modules whose installation varies considerably. The following chapters provide information regarding installation aspects and not detailed procedures.

Figure 13: VX3106 Components Layout (Top view)

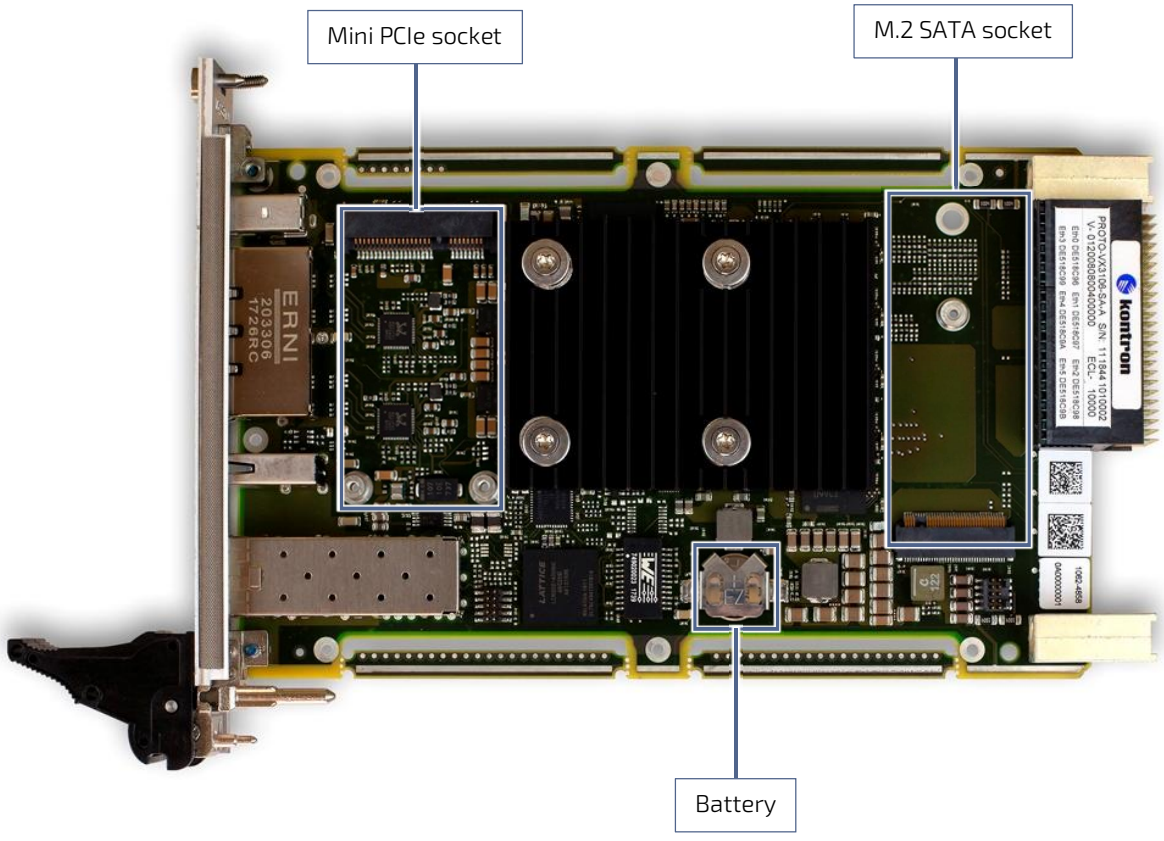
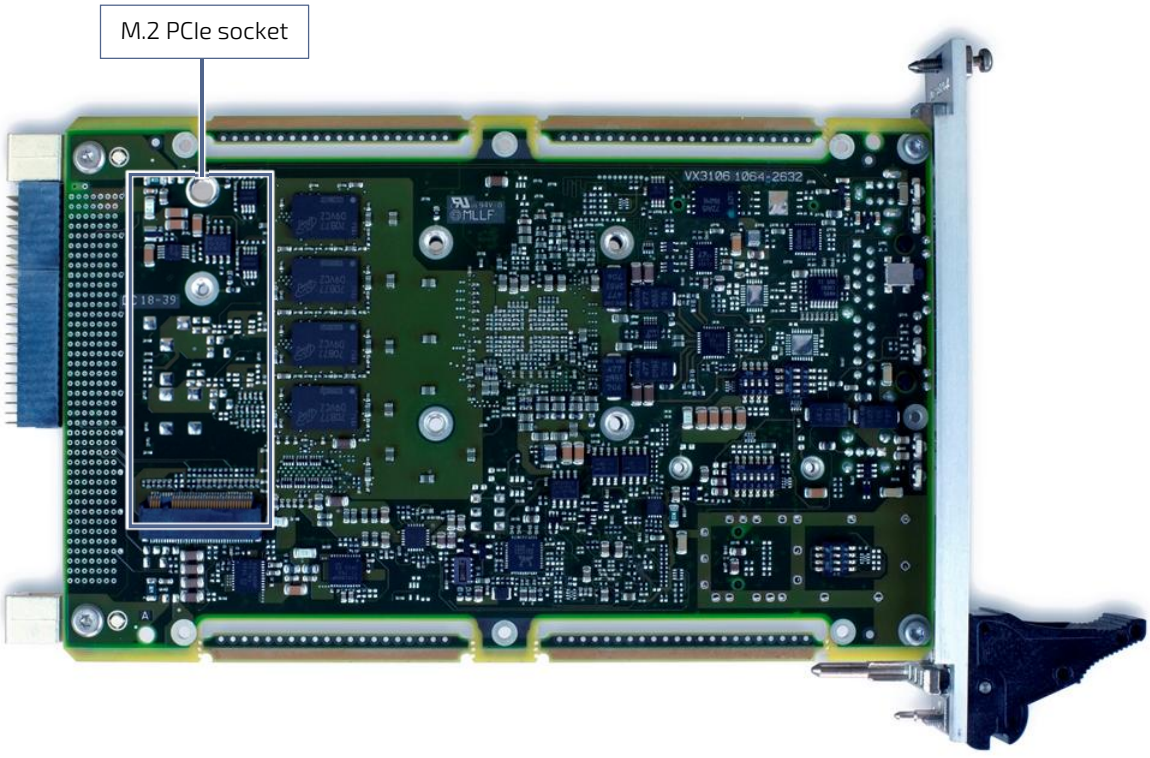


Figure 14: VX3106 Components Layout (Bottom view)



2.7.1. M.2 Module Insertion / Removal Instructions

Supported M.2 Module Type

The M.2 top socket is compliant with SATA III interface. The socket can host the following module types: 2242-XX-M or 2260-XX-M with XX = S1, S2, S3, D1, D2, D3, D4, D5.

The M.2 bottom socket is compliant with PCIe x1 Gen2 interface. The socket can host the following module types: 2242-XX-M or 2260-XX-M with XX = S1, S2, S3, D1, D2, D3, D4.

The M.2 bottom socket is not compliant with D5 form factor.

M.2 Module Insertion Process

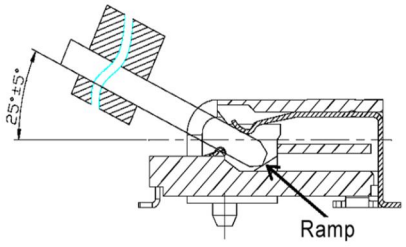
ESD sensitive Device! Precautions are listed in chapter 2.1

Apply "Loctite 222e" threadlock on each screw during re-assembling.

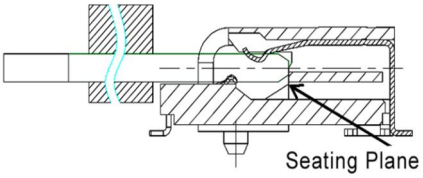
1. Align the notch at the edge of the M.2 card with the key in the connector.

Figure 15: M.2 Module Insertion Process

2. Insert the module with angle 25°±5° until module touch HSG ramp.



3. Rotate the module to horizon by hand and make sure the card's edge touch HSG seating plane.



4. Fix the module with PCB by nut by hand. See Table 18: M.2 Mounting Configuration for details.

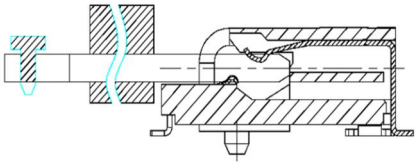


Table 18: M.2 Mounting Configuration

M.2 CONFIGURATION	DETAIL
2260 M2 mounting top side	See Figure 16:2260 M2 mounting top
2242 M2 mounting top side	See Figure 18: 2242 M2 module insertion (top or bottom) and Figure 17: 2242 M2 Mounting Prerequisite
2242 M2 mounting top & bottom side	See Figure 19:M2 2242 module insertion (both) and Figure 17: 2242 M2 Mounting Prerequisite

Refer to Table 19: M2 Fastener Detail for detail about fastener accessories required for M.2 mounting referenced into the Figure 16 to Figure 19.

Figure 16:2260 M2 mounting top

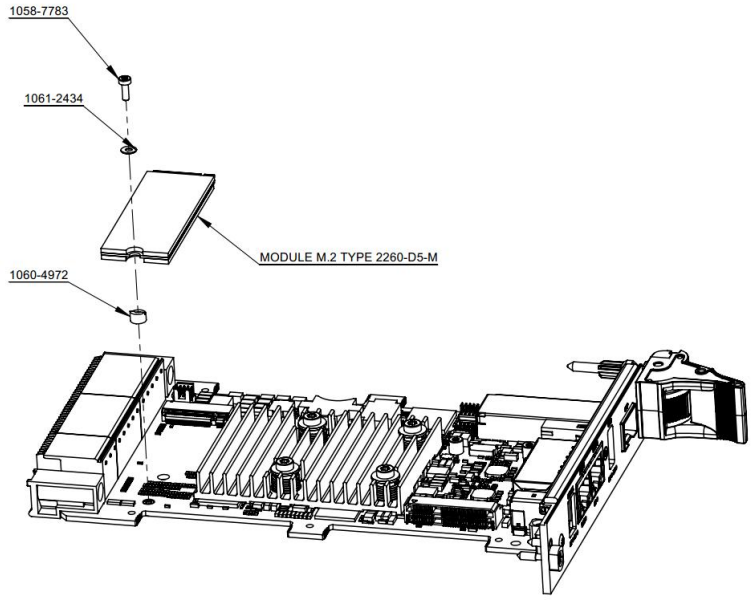


Figure 17: 2242 M2 Mounting Prerequisite

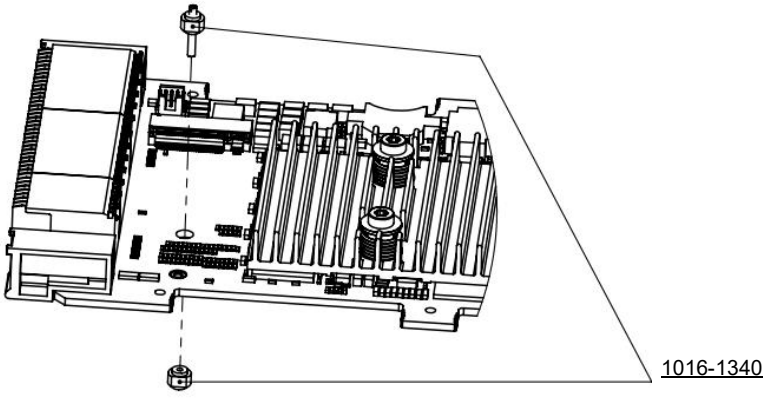


Figure 18: 2242 M2 module insertion (top or bottom)

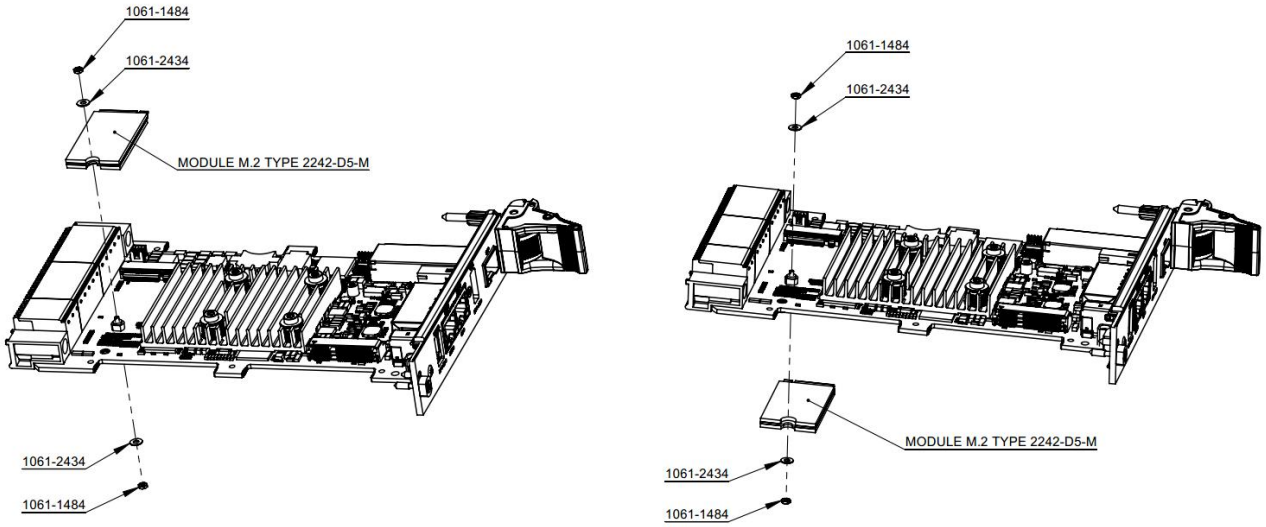


Figure 19:M2 2242 module insertion (both)

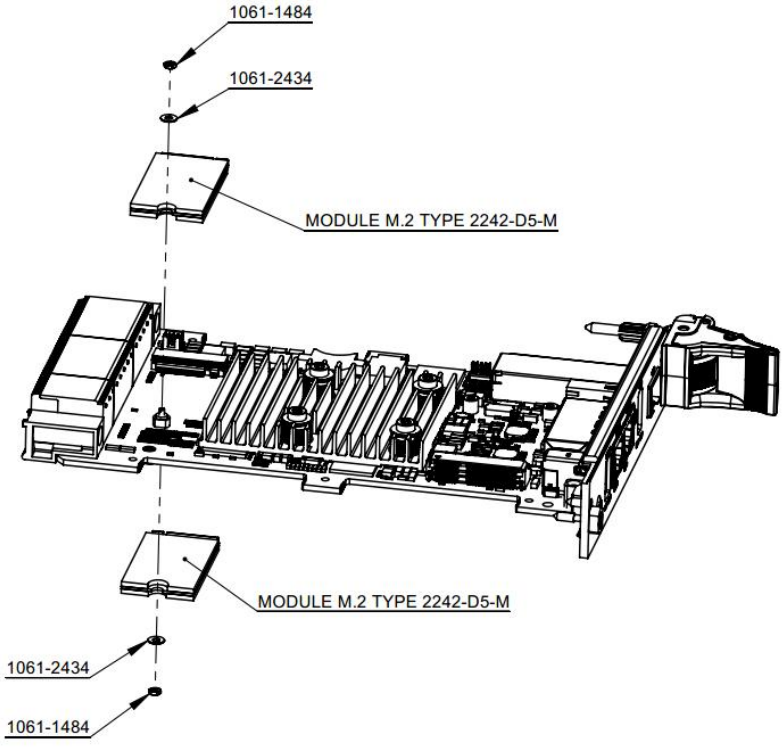
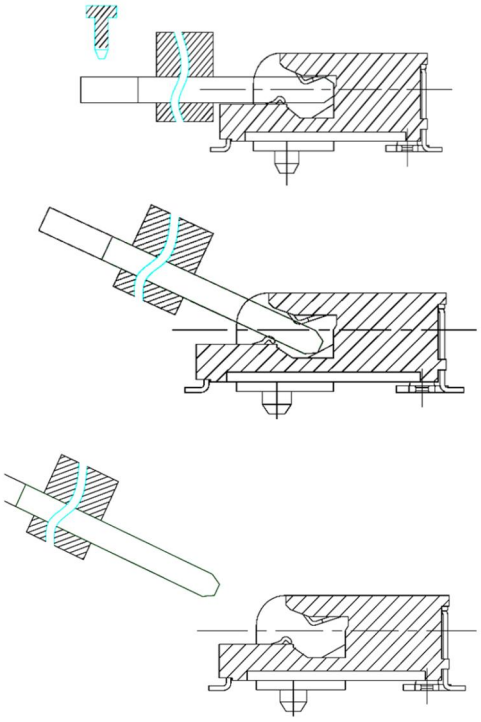


Table 19: M2 Fastener Detail

Kontron P/N	Description
1058-7783	Hexalobular Socket Cheese Head Screw ISO 14580-M2X6-A4-70
1061-2434	Washer ISO 7089-2-200HV-A4
1060-4972	M2 Custom Standoff H4.2
1061-1484	Hexagon Thin Nut ISO 4035-M1.6-A4-70
1061-1340	M.2 Custom Standoff
1061-1482	Slotted Set Screw ISO 4766-M1.6X12-A1

M.2 Module Removal Process

Figure 20: M.2 Module Removal Process



1. Loosen the screw by hand and the module will be rotated automatically due to connector contact's counterforce at the same time.

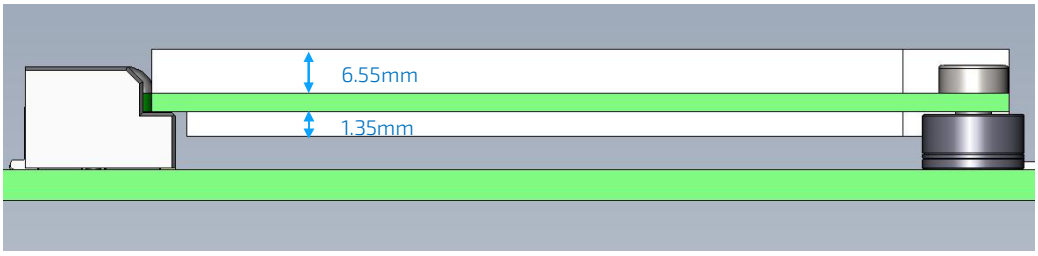
2. Take away the module by hand.

2.7.2. MiniPCIe Module Insertion / Removal Instructions

Supported MiniPCIe Module Type

The system board is equipped with 1 Mini PCIe slot. This slot authorizes the insertion of miniPCIe card compliant with full size F1 and F2 Type.

- miniPCIe slot dimension:



  - Maximum top height of miniPCIe card is limited to 6.55mm in order to satisfy the maximum height requirement (13.71mm) defined in VPX standard.
  - Maximum bottom height of miniPCIe card is limited to 1.35mm by

- Installation procedure:

1. Grasp the Mini PCIe card by its edges and align the notch of the PCIe card with the key in the connector on the system board.

2. Push down on the other end of the Mini PCIe card

The insertion of each module is done obliquely as shown on the figure above. The module should be leaned on the fixing spacer before screwing the mounting screws.

3. Use the provided mounting screws to secure the card on the system board.

Each module is mounted with two M2.5 hexalobular screws of 6 mm length without washers, tighten with a torque of 0.5N.m [+/-0.05N.m]) with help of a T8 screwdriver. Apply “Loctite 222e” threadlock on each screw.

2.7.3. Battery Replacement

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. The battery is used to run a time of day clock during the absence of power. Operation without the battery is possible but the date and time will not be retained in the absence of power. Alternatively the VPX VBAT signal from P1 can provide a 3.3V voltage from the backplane to retain the date and time.

- **Battery Part Number**

Reference of the battery used on the VX3106-SA: RENATA CR1220 MFR (-30/+70°C)

- **Battery Replacement**

To replace the battery, proceed as follows:

1. Turn off power.
2. Use a thin plastic tool to push the battery out of its holder.

NOTICE Do not subject the holder to mechanical stress when inserting the tool to eject battery.

3. Remove the battery.
4. Place the new battery into the socket with positive side (+) upwards and negative side (-) closest to printed circuit board

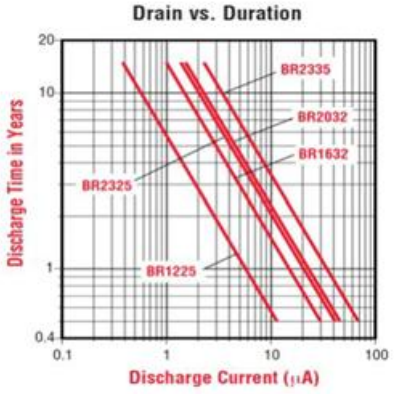
⚠CAUTION **Danger of explosion when replacing with wrong type of battery. Replace only with the same or equivalent type recommended by the manufacturer. The lithium battery type must be UL recognized.**

Do not dispose of lithium batteries in general trash collection. Dispose of the battery according to the local regulations dealing with the disposal of these special materials, (e.g. to the collecting points for dispose of batteries).

- **Battery Life**

Figure 17 gives an estimate of years of service at various discharge currents for BR Lithium coin cells at room temperatures. The RTC circuit power consumption is specified at 500 nA, giving an expected duration of more than 10 years in the absence of external power. In case of storage temperature or operating temperature is higher than 55°C or lower than 0°C, the battery life is reduced to 7 years in worst case.

Figure 21: Battery Life



2.8. Software Installation

The installation of all onboard peripheral drivers is described in detail in the relevant Driver Kit files or Board Support Packages (BSP).

The installation of an operating system is dependent of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.

3/ Additional Board Features

3.1. The Backplane Power Supplies and their Monitoring

The VITA46.0 standard specifies the backplane power supplies VS1 as follows:

- VS1: 12 V +/- 5 % inclusive of ripple (11.4 V to 12.6 V).

At Power On, the VPX VS1 system power supply ramp-up phase must be between 20 and 150 msec. VPX +3.3V_AUX power supply is optional.

To ensure a valid Power Off, VS1 should remain at 0V for at least one second.

A voltage sensor, the LTC2913 by Linear Technology monitors this voltage with a 10 % tolerance. The thresholds are set by hardware on the board. Undervoltage and overvoltage conditions on VS1 are reported to the cPLD which in turn shuts down all VX3106 internal power supplies. There is no mechanism for masking these alerts.

3.2. RTC, Watchdog, Timers

3.2.1. Real-Time Clock (RTC)

The VX3106 offers a standalone, high-precision and low-power Real Time Clocks (RTC) component located on the QorIQ I2C bus (RV8564 by Micro Crystal).

Standby power supplied to the RV8564 RTC

When the VX3106 is powered off, the RTC is powered through the 3.3V_AUX rail or the VBAT rail on the VPX backplane.

To ensure data retention in the RV8564 RTC, VBAT must be set in the range [2.5V - 5.5V]. The maximum current drawn over the -40 °C/+85 °C temperature range is 500 nA (VBAT= 3 V, no I2C activity) or 550 nA (VBAT=5 V, no I2C activity).

Internal Integrated PCH RTC

The integrated PCH RTC module provides a date and time keeping device with two banks of static RAM with 128 bytes each. The BIOS programs the RTC interrupt on Legacy IRQ8 that is never shared with other interrupts. It is clocked by an external 32.768 KHz oscillator with a parabolic coefficient of 0.4 ppm/°C^2 and a stability of +/-20 ppm at 25 °C. A 20 ppm stability is equivalent to a 10 mn/year drift.

Standalone low-power RTC RV8564

The RV8564C2/B RTC by Micro Crystal features an internal oscillator, date and time keeping module with programmable alarm, timer and interrupt functions. It has an ultra low-power consumption in time keeping mode: 250 nA, typical and 500 nA, maximum. Its stability is 20 ppm at 25 °C.

RTC management by Firmware and OS

At each startup, the Firmware retrieves the date and time information from the high-precision RV8564 RTC.

Any update of date and time in the Firmware settings will be done in RV8564 RTC.

Regarding the RTC management by the OS, the OS should use the high-precision RV8564 RTC driver.

Century flag

For compatibility reasons, the Firmware implements the century flag for the high-precision RTC as follows:

- Century Flag C = 0 for 1900-1999 years
- Century Flag C = 1 for 2000-2099 years.

The user should check that the OS driver implements the same convention.

3.2.2. QorIQ Watchdog Timer

The QorIQ processor of VX3106 offers five watchdog timers. The timers are enabled by software. Once enabled it must be restarted at regular intervals. If servicing does not take place, the timer times out. Upon timeout, the watchdog timer asserts the timeout signal as reset request to COP.

There is also a provision for watchdog timer signal assertion by time out counter expiration. There is an option of programmable interrupt generation before the counter actually times out. The time at which the interrupt needs to be generated prior to counter time out is programmable.

All watchdog timer modules use 32 KHz clock, driven at device input RTC pin for their counters.

The watchdog has the following features:

- Configurable timeout counter with timeout periods from 0.5 to 128 seconds,
- Time resolution of 0.5 seconds
- Programmable interrupt generation prior to timeout
- The duration between interrupt and timeout events can be programmed from 0 to 127.5 seconds in steps of 0.5 seconds.

3.2.3. CPLD Watchdog

In addition to the standard watchdog timer included in the inside the QorIQ, the cPLD implements a hardware watchdog timer that can be used by the operating software to monitor the normal operation of the system.

It is enabled by software, and once enabled must be restarted at regular intervals. If not, its expiration sets off an interrupt (IRQ) to the local processor, a board reset or a board power-cycle.

The watchdog has the following features:

- timeout programmable from 1 to 511 clock periods, by steps of 2 periods
- clock periods of 1s or 1ms
- lock bit: when set, can only refresh (restart) the watchdog, but not change its settings
- 4 modes: timer, reset, interrupt or power-cycle
- restart counter: can manage the remaining number of resets or power-cycles done by the watchdog before giving-up.

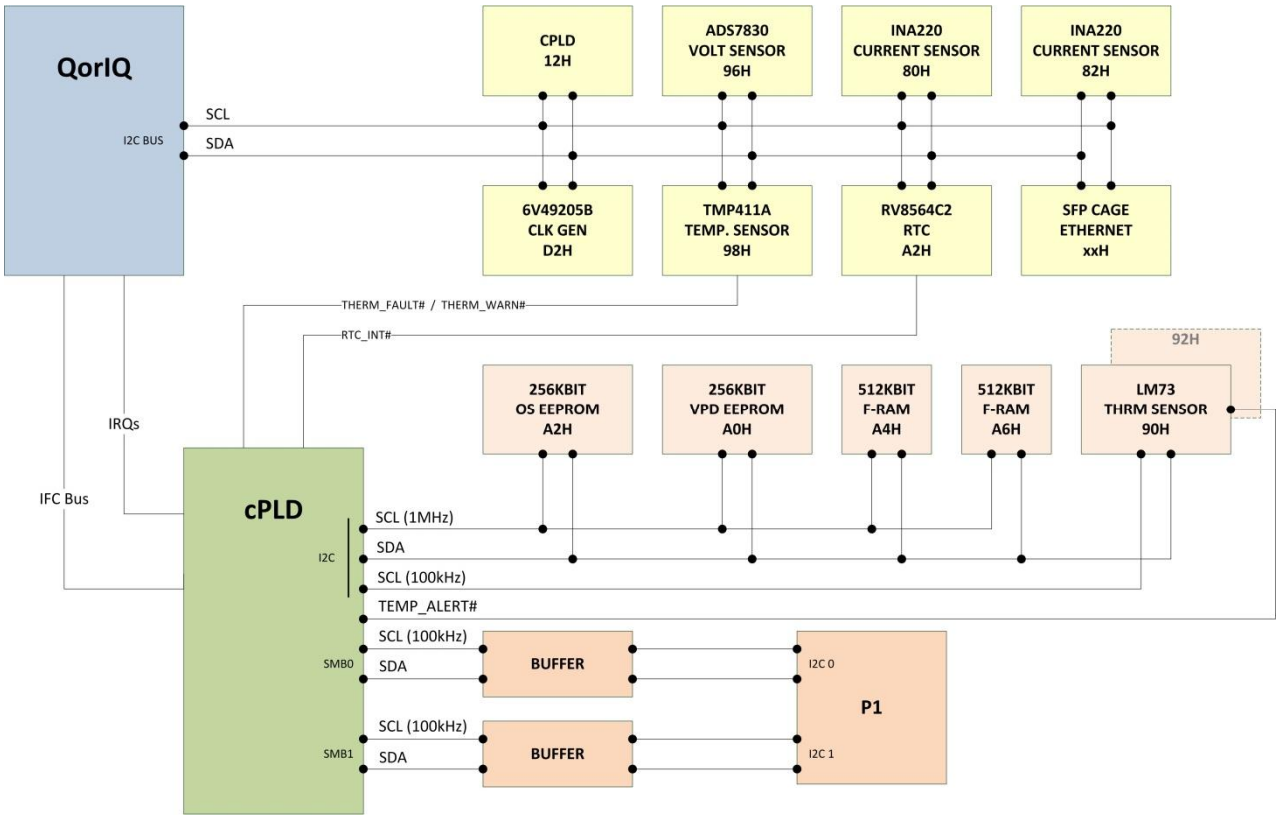
3.3. I2C Structure

The VX3106 features four I2C busses.

- The first one is attached to the QorIQ processor.
- The remaining I2C busses are handled by the CPLD device. The Figure 22: I2C Diagram shows the component attached to the different I2C buses.

The I2C addresses shown are 8 bit values which include a read/write bit. Shift one bit to the right to get the 7-bit addresses.

Figure 22: I2C Diagram



- QorIQ I2C devices (100 KHz)

SLAVE DEVICES ON QorIQ I2C INTERFACE	I2C 7-BIT BASE ADDRESS (8-BIT BASE ADDRESS)	FEATURES
cPLD	09H (12H)	System cPLD
ADS7830	4BH (96H)	Voltage sensor
INA220	40H (80H)	CPU Current monitor
INA220	41H (82H)	VPX 12V CPU Current monitor
6V49205B	69H(D2H)	Clock generator
TMP411A	4CH (98)	CPU temperature sensor
RV8564C2	51H (A2H)	External RTC Device
SFP connector	xxH (xxH)	To SFP I2C bus

- cPLD I2C Bus (1 MHz)

SLAVE DEVICES ON CPLD SMBUS INTERFACE	SMBUS 7-BIT BASE ADDRESS (8-BIT BASE ADDRESS)	FEATURES
24FC256-I/SN VPD EEPROM	50H (A0H)	256 Kbits VPD EEPROM
24FC256-I/SN OS EEPROM	51H (A2H)	256 Kbits OS EEPROM
FM24V10-G	52H (A4H) / 54H (A8H) /	1 Mbits User FRAM

- IPMC I2C Bus (100 KHz)

SLAVE DEVICES ON IPMC SMBUS INTERFACE	SMBUS 7-BIT BASE ADDRES (8-BIT BASE ADDRESS)S	FEATURES
LM73 sensor	48H (90H)	Temperature Sensor

3.4. CPLD Features

The CPLD manages the following features:

- Power-on/off control
- Reset control
- Local environmental control/monitoring
- IFC interface to processor
- I2C interfaces to local I2C bus, and backplane SMB busses (rear VPX P0).
- LEDs control
- Serial lines multiplexer
- Serial VPD and user memories
- User and system GPIOs
- Internal registers that allow system management

3.4.1. cPLD Registers Definition:

3.4.1.1. Overview

These registers can be accessed from CPU through LPC bus at I/O address 0x800+offset.

Table 20: cPLD Registers Definition - Overview

OFFSET	NAME	PURPOSE	ACCESS
0x72	I2C_BOARD_STATUS	Board state (from I2C)	RW
0x73	I2C_BOARD_CONTROL	Board state and control (from I2C)	RW
0x74	I2C_ERROR_STATUS	Board error state (from I2C)	RW
0x75	I2C_CHECKPOINT	CHECKPOINT value (from I2C)	RW
0x76	I2C_FAILCODE	Reserved for future use	RW
0x77	I2C_SCRATCHPAD	Not yet defined	RW
0x78	I2C_MISC	Miscellaneous board information (from I2C)	RW

Contact Kontron for a detailed description of the CPLD registers.

3.4.1.2. Detailed Description

Table 21: I2C_BOARD_STATUS @0x72

I2C_BOARD_STATUS @ 0x72 Can also be accessed from I2C0 slave interface with register offset 0				
Bit#	**Name**	**Description**	**Reset**	**Type**
7	PowerStatus	**Power Status** 0: :Power Stand By 1: :Power ON	0	RO
6-5	Reset Source	**Last Reset Source** 0x00 Internal PSUs power-on 0x01 Watchdog expired 0x10 SYSRESET (from VPX) 0x11 Local reset: reset switch, reset from I2C (reg 0x73), or reset by software	0	RO
4	Reset Status	**Reset Status Side A** 0 Reset asserted 1 Reset unasserted	0	RO
3-0	Boot Status	**Boot Status** 0x00: RESET: default hardware value 0x01: BIOS-BOOT: written by BIOS 0x02: BIOS: written by BIOS 0x03: PBIT: written by BIOS 0x04: OS-BOOT: written by BIOS 0x05: OS-RUNNING: to be written by OS at the end of boot 0x06: COMPLETED: to be written by the final application when running 0x07: SHUTDOWN: to be written by OS when issuing a halt/shutdown 0x08: REBOOT: to be written by OS when rebooting 0x09 - 0x0B: Reserved 0x0C - 0x0F: Customer defined These bits are Read Only through I2C Slave Interface and R/W through LPC Interface The boot status is also reset at each board reset.	0	RW

Table 22: I2C_BOARD_CONTROL @0x73

I2C_BOARD_CONTROL @ 0x73 Can also be accessed from I2C0 slave interface with register offset 1				
Bit #	Name	Description	Reset	Type
7-4	Board Id	**Board Identification** 1110 VX3106	0	RO
3-2	Reserved	Reserved	0	RW
1	Reset	**Reset** 0: No reset 1: Reset asserted	0	RW
0	Power_OnOff	**Power On/Off Control** 0: Power Off (StandBy) 1: Power On This bit can always be used to power on or off, and its default value is loaded when standby is applied from inverted VPD EEPROM offset 0x100 bit 1, if FACTORY mode is not enabled **WARNING** Setting this bit to 0 asserts VPX SYSRESET	*	RW

Table 23: I2C_ERROR_STATUS @0x74

I2C_ERROR_STATUS @ 0x74 Can also be accessed from I2C0 slave interface with register offset 2				
Bit#	Name	Description	Reset	Type
7	Temp Alert	Temperature alert on sensor or CPU 0: no temperature alert 1: temperature alert pending	0	RO
6	POST_Error	POST Error 0: no error 1: error This bit is set when PBIT has been run with errors (according to reg 0x2)	0	RO
5	POST_RTC	POST RTC 0: POST OK 1: POST FAILED (weak or missing battery) This bit is a copy of reg 0x3 bit 0 (POST_RTC), that is set when RTC battery islow	0	RO
4-0	Temp Alert	Reserved	0	RW

Table 24: I2C_CHECKPOINT @ 0x75

I2C_CHECKPOINT @ 0x75 Can also be accessed from I2C0 slave interface with register offset 3				
Bit#	Name	Description	Reset	Type
7-0	Checkpoint	Last checkpoint written to cPLD register	0	RO

Table 25: I2C_FAILCODE @ 0x76

I2C_FAILCODE @ 0x76 Can also be accessed from I2C0 slave interface with register offset 4				
Bit#	Name	Description	Reset	Type
7-0	Reserved	Reserved for future use	0	RO

Table 26: I2C_SCRATCHPAD @ 0x77

I2C_SCRATCHPAD @ 0x77 Can also be accessed from I2C0 slave interface with register offset 5				
Bit#	Name	Description	Reset	Type
7-0	Scratchpad	**Scratchpad register** The purpose of this register is not defined	0	RW

Table 27: I2C_MISC @ 0x78

I2C_MISC @ 0x78 Can also be accessed from I2C0 slave interface with register offset 6				
Bit#	Name	Description	Reset	Type
7	Force_rescue_BIOS	**Force rescue Firm** 0=not forced (default) 1=forced	0	RW
6	Disable_OS_boot	**Disable OS Boot** 0=not disabled (normal boot) 1=disabled	0	RW
5-3	Power_CUR	**Current power profile** This field is updated by the board (Firm/OS) according to its current power profile 000: power profile unsupported other value: see below	000	RO
2-0	Power_REQ	**Requested power profile** This filed is expected to be set by a shelf-manager (such as CMB) or another board, and used by the board (Firm/OS) to set its power profile. 000: uncontrolled : the board uses its onboard switches and/or Firm settings to set a power profile Other: reserved	000	RW

3.5. Serial Lines EIA-422/485 Additional Modes

The VX3106 features up to 4 serial lines in EIA-232 mode and up to 2 serial lines in EIA-422/485.

EIA-232/422/485 serial lines are available on front panel IEEE1394 and P2 connector.

See section 4.1.1 page 67 - "Serial Connector – COM1 & COM" and section 4.3.3 page 82 - "P2 Connector" for more information on pin assignments.

EIA-232 serial line mode is the default mode, but EIA-422/485 mode can also be set for COM1 and COM2 according to the following table:

Table 28: Serial Lines Additional Modes

MODE	IEEE1394 FRONT PANEL CONNECTOR	P2 REAR CONNECTOR	IEEE1394 FRONT PIN ASSIGNMENT	P2 REAR PIN ASSIGNMENT
EIA-232 (default)	EIA-232: COM1, COM3	EIA-232: COM1, COM2, COM3, COM4	COM1 TXD: pin 5 COM1 RXD: pin 3 COM3 TXD: pin 6 COM3 RXD: pin 4	COM1 TXD: pin G3 COM1 RXD: pin G7 COM2 TXD: pin G11 COM2 RXD: pin G15 COM3 TXD: pin G1 COM3 RXD: pin G5 COM4 TXD: pin G9 COM4 RXD: pin G13
EIA-232 with handshaking(1)	EIA-232: COM1	EIA-232: COM1, COM2	COM1 TXD: pin 5 COM1 RXD: pin 3 COM1 RTS: pin 6 COM1 CTS: pin 4	COM1 TXD: pin G3 COM1 RXD: pin G7 COM1 RTS: pin G1 COM1 CTS: pin G5 COM2 TXD: pin G11 COM2 RXD: pin G15 COM2 RTS: pin G9 COM2 CTS: pin G13
EIA-422/485	EIA-422/485: COM1	EIA-422/485: COM1, COM2	COM1 TXD+: pin 6 COM1 TXD-: pin 5 COM1 RXD+: pin 4 COM1 RXD-: pin 3	COM1 TXD+: pin G1 COM1 TXD-: pin G3 COM1 RXD+: pin G5 COM1 RXD-: pin G7 COM2 TXD+: pin G9 COM2 TXD-: pin G11 COM2 RXD+: pin G13 COM2 RXD-: pin G15

(1) This mode requires to modify RCW and to reset the Firmware to be taken into account.

The mode EIA-232 or EIA-422/485 is selected in U-BOOT by the user. When EIA-422/485 is selected, an optional on board 120 Ohms termination can be activated.

3.6. GPIOs and GDISCRETE1

3.6.1. GPIOs

The VX3106 features up to 5 GPIOs managed by the CPLD. Refer to the Software Release Notes D218953 for further details on the GPIO driver.

- 3 GPIOs are available on P0 connector: GPIO3, GPIO4 and GPIO5. See section 4.3.3 "P2 Connector" page 82 for detailed pinout.
- 2 GPIOs are available on P1 connector, GPIO1, GPIO2 (maskable reset). See section 4.3.2 "P1 Connector" page 81 for detailed pinout.

GPIO electrical characteristics:

- The CPLD features LVCMOS33 cells (0-3V3),
- drive strength = 8 mA (sink or source),
- a clamp diode which is not 5V tolerant,
- an hysteresis of 250mV.

The CPLD does not implement any internal pull-up or pull-down.

On the VX3106 board, a pull-up of 47 kOhms is connected to GPIO1 to GPIO5.

CAUTION: GPIOs are not 5V tolerant. Maximum voltage on GPIOs is 3.6 V. Absolute maximum voltage is 3.75V and is not suitable for continuous operation. Appropriate voltage reduction (through resistor divider for instance) must be made to avoid permanent damage to the board.

The GPIOs share the same interrupt in the CPLD.

3.6.2. GDISCRETE1

GDISCRETE1 is a bussed open-collector GPIO defined by OpenVPX VITA 65 and available on P1. See section 4.3.2 "P1 Connector" page 81 for detailed pinout.

It is handled by the CPLD and buffered by a SN74LVC1G125 wired as an Open Collector to meet the electrical characteristics defined in VITA 65.

It has a dedicated interrupt in the CPLD.

3.7. Reset

RESET SOURCE	RESET ACTION	RESET CONTROL	RESET STATUS	NOTE
Front panel reset push button	Board reset Active VPX Sysreset if the board is system controller	Front push button	"I2C_BOARD_STATUS @0x72	Reset propagation options and masks available in cPLD registers
VPX Sysreset	Reset the board if configured in cPLD setting	VPX P0 / Row B/ Wafer 4	"I2C_BOARD_STATUS @0x72	"See VPX Vita46.0 standard Reset propagation options and masks available in cPLD registers"
VPX maskable reset (GPIO2)	Reset the board	VPX P1 / Row G/ Wafer 15	"I2C_BOARD_STATUS @0x72	See VPX Vita46.0 standard
cPLD watchdog reset	Reset the board	See software release notes	"I2C_BOARD_STATUS @0x72	See software release notes
Processor watchdog reset	Reset the board	NXP QrIQ watchdog control registers	NXP QorIQ watchdog status registers	
cPLD software reset	Reset the board	I2C_BOARD_CONTROL @0x73	"I2C_BOARD_STATUS @0x72	See register definition in this user's guide

3.8. Write Protect Mode

VX3106 non-volatile content is managed in three independent write protection domains.

- **SYS:** Temporary, run time data
- **USR:** Settings data , maintenance under user control
- **VPD:** Kontron driven static data

On top of the domains, two 'top level' settings can override the domains write protection

- **NVMRO:** force all domains to be WProtected
- **FACTORY:** force all domains to be Writeable

SYS_WP

- **Description:**
  Write protection at system level of run time volatile information (PBIT results)
- **Hardware Write Protection:**
  NVMRO signal is high and SW1[1] (Factory mode) is OFF for full protection
- **Write Protect Contol:**

NVMRO	sw1[1] Factory mode	sw1[3] System write protection	CPLD register @09-bit 2	Protection	Mode of Operation
1	OFF	X	X	YES	Normal
0	X		0	No	Normal
1	ON		1	YES	Factory
1	ON		0	No	Factory
0	X		1	YES	Software forced protection

X = "don't care", CPLD register @09-bit 2 default setting is "0"

- **Protected Devices:**
  - 256 Kbits OS EEPROM on CPLD I2C bus @0x51

USER_WP

- **Description:**
  Write protection at user level for maintenance and user driven information
- **Hardware Write Protection:**
  MVMRO signal is high and SW1[1] (Factory) is OFF for full protection
- **Write Protect Contol:**

NVMRO	sw1[1] Factory mode	sw1[4] USER write protection	CPLD register @09-bit 3	Protection	Operation
1	OFF	X	X	YES	Normal
0	X	OFF	0	No	Normal
1	ON	ON	X	YES	Factory
1	ON	OFF	0	No	Factory
1	ON	OFF	1	YES	Factory
0	X	ON	X	YES	DIP switch forced protection

NVMRO	sw1[1] Factory mode	sw1[4] USER write protection	CPLD register @09-bit 3	Protection	Operation
0	X	OFF	1	YES	Software forced protection

X = "don't care", CPLD register @09-bit 3 default setting is "0"

- **Protected Devices:**
  - 1 Mbits User FRAM located on CPLD I2C2 bus @0x52/53
  - Internal CPLD configuration flash
  - QSPI Boot Flash memories

VPD_WP

- **Description:**
  Write protection at VPD level of static information vendor/kontron driven.
- **Hardware Write Protection:**
  MVMRO signal is high and SW1[2] & SW1[1] are OFF for full protection
- **Write Protect Contol:**

NVMRO	sw1[1] Factory mode	sw1[2] VPD write protection	CPLD register @09-bit 1	Protection	Protection
X	X	ON	X	No	DIP switch released protection
1	OFF	OFF	X	YES	Normal
1	ON	OFF	0	No	Factory
1	ON	OFF	1	YES	Factory
0	X	OFF	0	No	Software released protection
0	X	OFF	1	YES	Normal

X = "don't care", CPLD register @09-bit 1 default setting is "1"

- **Protected Devices:**
  - 256Kbits VPD EEPROM on CPLD I2C2 bus @0x50

NVMRO

- All non-volatile devices protected.
- NVMRO signal is high and SW1[1], SW1[2] & SW1[3] are OFF for full non-volatile devices protection.
- VX3106 offers the capability to drive the NVMRO signal on the backplane by setting SW2[4] OFF.

CAUTION: Set the hardware jumper SW2[4] to OFF force to ground the NVMRO signal on the backplane. Write protection is de-asserted for all the boards in the chassis.

3.9. Kontron Security Solution

The VX3106 is equipped with the Kontron Security Solution, providing an embedded hardware security solution that enables applications to be secured, even in unsecure environments. The Kontron Security Solution provides features such as:

- **Copy protection**
- **IP protection**
- **License model enforcement**

If required customers can customize the solution to meet specific needs. For more information contact Kontron Technical Support.

3.9.1. Apprtect

The APPROTECT solution, using a security technology from Wibu, a Kontron partner, protects the application from the main security threats with the security of a dedicated hardware secure element located on the VX3106 board.

The main security threats at the application level are:

- **Integrity**: the running application might be hacked or patched in binary, on the disk or in memory, to modify its behavior or work around some checks.
- **Confidentiality**: the way the application code is working could be analyzed in details by looking at the execution code, in order to learn or to reproduce its behavior.
- **Unauthorized copies**: the embedded systems (software application or full equipment) suffer the risk of being cloned without authorization.

- Technical information
  - **Security Hardware**: CodeMeter ASIC 1504-03 based on Infineon SLM-97CUSIFX1M00 smart card chip
  - **Encryptions standards**: Used algorithms in Firmware 4.0: 128 bit AES, SHA-256, 2048 bit RSA, 224 bit ECC.

3.9.2. Trusted Platform Module (TPM 2.0)

The VX3106 is compliant to TPM 2.0. A Trusted Platform Module (TPM) stores RSA encryption keys specific to the host system for hardware authentication. The term TPM refers to the set of specifications applicable to TPM chips.

Each TPM chip contains an RSA key pair called the Endorsement Key (EK). The pair is maintained inside the chip and cannot be accessed by software. The Storage Root Key (SRK) is created when a user or administrator takes ownership of the system. This key pair is generated by the TPM based on the Endorsement Key and an owner-specified password.

A second key, called an Attestation Identity Key (AIK) protects the device against unauthorized firmware and software modification by hashing critical sections of firmware and software before they are executed. When the system attempts to connect to the network, the hashes are sent to a server that verifies that they match the expected values. If any of the hashed components have been modified since last started, the match fails, and the system cannot gain entry to the network.

4/ Physical I/O

4.1. Front Panel Connectors

Figure 23: Onboard Connectors

4.1.1. Serial Connector – COM1 & COM3

The VX3106 integrates up to four serial communications ports, COM1 to COM4 in PC parlance.

COM1 to COM4 are available on rear via the P2 connector. COM1 and COM3 are also available via the front panel connector.

- COM1: EIA-232/485 port on IEEE1394 front panel connector or on the rear P2 connector
- COM2: EIA-232/485 port on the rear P2 connector
- COM3: EIA-232 port on IEEE1394 front panel connector or on the rear P2 connector
- COM4: EIA-232 port on the rear P2 connector

COM1 and COM2 serial ports are configurable via Firmware commands and CPLD as EIA-232 or EIA-422 or EIA-485. Each port operates in full duplex mode or in half duplex mode. Fast slew rate is the default mode in EIA-485 mode.

The signaling level of EIA-485 is compatible with EIA-422, so full duplex EIA-485 may also be used for point-to-point communications with an EIA-422 serial port. When port is operating in EIA-485 mode software may configure the termination for V.35, V11 or unterminated using CPLD.

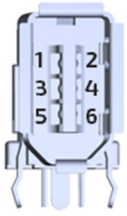
In EIA-232 mode the port is always unterminated register.

Front Serial Connector Description

Table 29: Serial Connector Pin Assignment

Pin	Signal
1	Reserved
2	GND
3	COM1 RXD / COM1 RXD-
4	COM3 RXD / COM1 RXD+
5	COM1 TXD / COM1 TXD-
6	COM3 TXD / COM1 TXD+

Figure 24: Serial Connector (IEEE 1394 Type)



NOTICE

CAUTION: Serial lines are routed to both front panel connector and rear P2. Plugging a serial device to both connectors will lead to electrical contention. Be sure to use only one connector at a time.

Table 30: Serial Connector Signals Definition

Signal	Dir.	Definition
COM1 TXD / COM1 TXD-	O	EIA-232: Transmit Data of port COM1 EIA-485: Transmit Data minus of port COM1
COM1 RXD / COM1 RXD-	I	EIA-232 Receive Data of port COM1 EIA-485: Receive Data minus of port COM1
COM2 TXD / COM1 TXD+	O	EIA-232: Transmit Data of port COM2 EIA-485: Transmit Data plus of port COM1
COM2 RXD / COM1 RXD+	I	EIA-232: Receive Data of port COM2 EIA-485: Receive Data plus of port COM1
Reserved	-	Reserved
GND	-	Logic ground
Shell	-	Chassis ground

Note: EIA-485 protocol requires special configuration. Contact Kontron.

- **Serial Cable Description**

Pin connector DB9	Signal	Pin connector IEE1394
1	NC	1
5	GND	2
3	RXD	3
4	NC	4
2	TXD	5
6	NC	6

4.1.2. Gigabit Ethernet Connectors

The Ethernet transmission should operate using a CAT5e cable with a maximum length of 50m.

The Ethernet connectors are available as RJ-45 connectors with tap down. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negociation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

Table 31: Gigabit Ethernet Connectors Pin Assignment

PIN	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-		I/O	BI_DC+
5	-	-	-		I/O	BI_DC-
6	I	RX-	I	RX-	I/O	BI_DB-
7	-	-	-		I/O	BI_DD+
8	-	-	-		I/O	BI_DD-
Shell			Chassis Ground			

Figure 25: Ethernet Connector

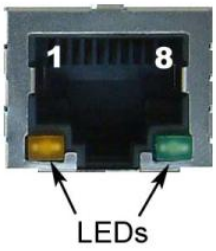


Table 32: Ethernet LEDs Status Definition

STATUS		SPEED LED YELLOW	ACT LED GREEN
Ethernet Link is not established		OFF	OFF
10 Mbps	Ethernet Link Established	OFF	ON
	Ethernet Link Activity	OFF	BLINK
100 Mbps	Ethernet Link Established	OFF	ON
	Ethernet Link Activity	OFF	BLINK
1000 Mbps	Ethernet Link Established	ON	ON
	Ethernet Link Activity	ON	BLINK

- **ACT (green)**

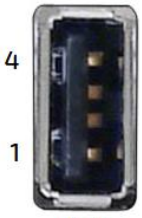
  This LED monitors network connection and activity. The LED lights up when a valid link (cable connection) has been established. The LED goes temporarily off if network packets are being sent or received through the RJ-45 port. When this LED remains off, a valid link has not been established due to a missing or a faulty cable connection.

4.1.3. USB connector

Table 33: USB Connector Pin Assignment

PIN	SIGNAL	FUNCTION	I/O
1	VCC (+5V Protected)	VCC	--
2	USB_D-	Differential USB-	I/O
3	USB_D+	Differential USB+	I/O
4	GND	GND	--

Figure 26: USB Connector

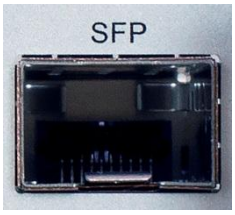


USB

4.1.4. SFP cage

The SFP cage is linked to the QorIQ through a SGMII protocol.

Figure 27: SFP cage Connector



4.2. Onboard Connectors

Figure 28: Onboard Connectors (Top view)

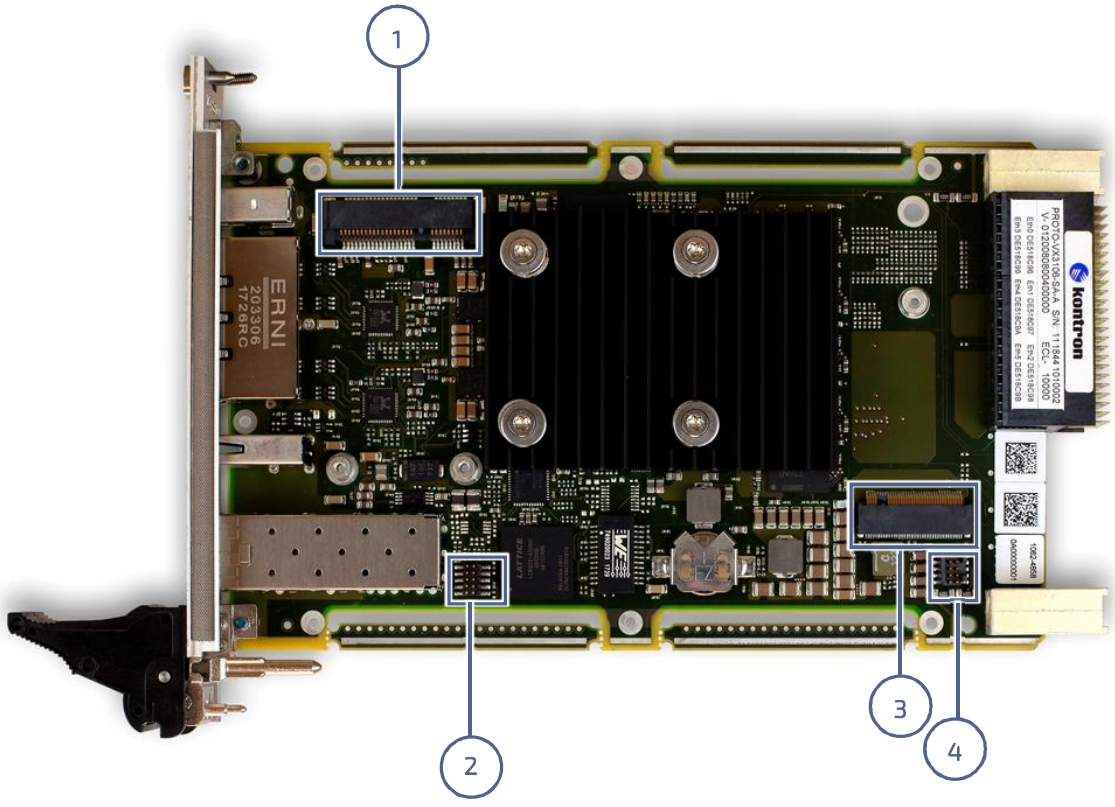
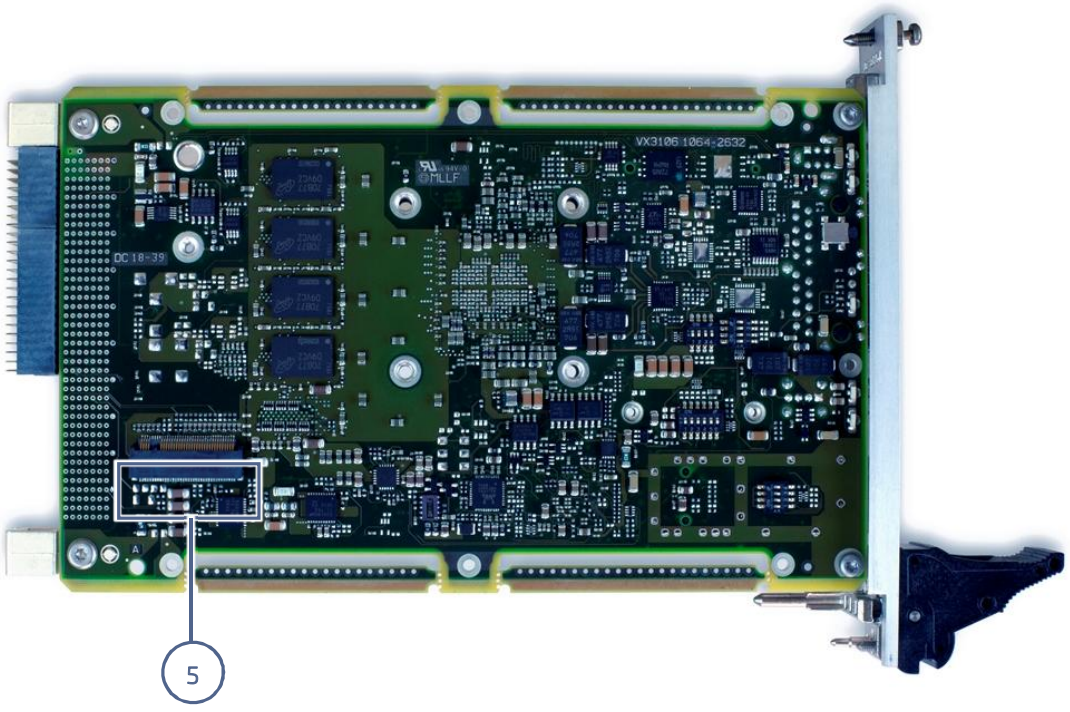


Figure 29: Onboard Connectors (Bottom view)



1. Mini PCIe socket J3202
2. Cortex debug connecor J1001
3. M.2 SATA socket J2301
4. JTAG cPLD connector P3502
5. M.2 PCIe socket J2201

4.2.1. Mini PCIe Connector J3202

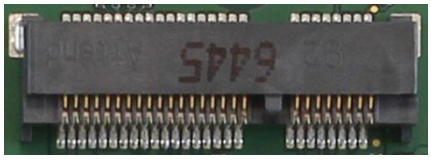
The VX3106 supports mini-PCI Express module F1 and F2 full size type as defined per PCIE Express card Electromechanical Specification through on board connector. This socket offers PCIe x1 Gen2 interface by default and USB2.0 interface depending on build option.

The following figure and table provide pinout information for the MiniPCIe connector:

Table 34: MiniPCIe Socket Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
51	NC	52	+3.3Vaux
49	NC	50	GND
47	NC	48	+1.5V
45	NC	46	NC
43	GND	44	NC
41	+3.3Vaux	42	NC
39	+3.3Vaux	40	GND

Figure 30: MiniPCIe Socket (H3.2)



PIN	SIGNAL	PIN	SIGNAL
37	GND	38	USB_D+
35	GND	36	USB_D-
33	PETp0	34	GND
31	PETn0	32	SMB_DATA
29	GND	30	SMB_CLK
27	GND	28	+1.5V
25	PERp0	26	GND
23	PERn0	24	+3.3Vaux
21	GND	22	PERST#
19	NC	20	NC
17	NC	18	GND
Mechanical Key			
15	GND	16	NC
13	REFCLK+	14	NC
11	REFCLK-	12	NC
9	GND	10	NC
7	CLKREQ#	8	NC
5	NC	6	1.5V
3	NC	4	GND
1	WAKE#	2	3.3Vaux

Table 35: Mini PCIe Module Socket Signal Description

SIGNAL	DIRECTION	DEFINITION
+1.5V	Ouput	+1.5V power supply.
+3.3Vaux	Ouput	+3.3V auxiliary voltage source. Connected to +3.3V internal voltage on VX3106.
GND	-	Ground
NC	-	Not Connected or not used pin.
USB_D+/-	I/O	Differential USB 2.0
PETp0 / PETn0	Ouput	High-speed Differential transmit PCIe pair
PERp0 / PERn0	Input	High-speed Differential receive PCIe pair
SMB_DATA	I/O	SMBus data for optional management feature. Not used on VX3106.
SMB_CLK	Output	SMBus clock for optional management feature. Not used on VX3106.
PERST#	Output	PCI Express PERST# per PCI Express Card Electromechanical Specification. On VX3106 handled by CPLD.
REFCLK+/-	Output	PCIe differential reference clock (100 MHz) per PCI Express Card Electromechanical Specification.
CLKREQ#	Input	Open drain CLKREQ# signal per PCI Express Card Electromechanical Specification. Driven by mini PCIe module to request the platform to activate the PCI Express clock.
WAKE#	Input	Open drain WAKE# signal per PCI Express Card Electromechanical Specification. Driven by miniPCIe module to

SIGNAL	DIRECTION	DEFINITION
		allow the platform to reactivate the link main power rails and reference clock. On VX3106, this signal is wire-ORed with WAKE# signal from XMC connector. It is connected to CPLD.

4.2.2. M.2 SATA Connector J2301

The socket J2301 is compliant with SATA III interface only.
This socket can host the following module types: 2242-XX-M and 2260-XX-M with XX = S1, S2, S3, D1, D2, D3, D4, D5.

Table 36: M.2 J2301 Sockets Pin Assignment

Pin	Signal	Signal	Pin
74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK (32kHz)	PEDET	69
	Connector Key	NC	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	NC	Connector Key	
56	NC	GND	57
54	PEWAKE#	REFCLKP	55
52	NC	REFCLKN	53
50	PERST#	GND	51
48	NC	SATA-A+	49
46	NC	SATA-A-	47
44	NC	GND	45
42	NC	SATA-B-	43
40	NC	SATA-B+	41
38	NC	GND	39
36	NC	NC	37
34	NC	NC	35
32	NC	GND	33
30	NC	NC	31
28	NC	NC	29
26	NC	GND	27
24	NC	NC	25
22	NC	NC	23
20	NC	GND	21
18	3.3V	NC	19
16	3.3V	NC	17
14	3.3V	GND	15
12	3.3V	NC	13
10	DAS_DSS#	NC	11
8	NC	GND	9
6	NC	NC	7
4	3.3V	NC	5
2	3.3V	GND	3
		GND	1

Table 37: M.2 J2301 Socket Signals Definition

Signal SATA	Dir.	Definition
3.3V	O	+3.3V power supply. On VM606x, protected by dedicated 1.5A resettable fuse (one for each M.2 socket).
GND	-	Logic ground.

Signal SATA	Dir.	Definition
DAS_DSS#	I	On VX3106 connected to dedicated CPLD pin. DAS is not connected to a LED (which is the main purpose of this signal) and DSS is not used.
PEDET	I	PEDET (PCI Express Detect) as per PCI Express M.2 specification is driven low by SATA modules and high-Z by PCI Express modules (seen as a logic 1 due to on-board pull-up resistor). On VX3106, this signal is connected to a dedicated CPLD pin.
SATA-B+	I	- SATA: Receive differential signal plus as per SATA 3.2.
SATA-B-	I	- SATA: Receive differential signal minus as per SATA 3.2.
PERST#	O	- SATA: NC.
SATA-A+/-	O	- SATA: Transmit differential pair as per SATA 3.2.
PEWAKE#	I	- SATA: NC.
REFCLKP/N	O	- SATA: NC.
SUSCLK	O	Suspend Clock for low power mode handling as per PCI Express M.2 specification (32.768 kHz, duty cycle between 30% and 70%, 200ppm). On VX3106, connected to cPLD CLK_32K_M2S2.

4.2.3. Cortex Debug Connector

The VX3106 implements legacy 10-pin Cortex-M Debug connector. This connector supports JTAG debug for QorIQ processor by enabling the connection of CodeWarrior TAP target system debugging tool. The CodeWarrior TAP allows you to debug and control of the LS1046A processor using the CodeWarrior IDE.

For further information about CodeWarrior TAP, visit NXP web site: https://www.nxp.com

Table 38: Cortex Debug connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
9	GND Detect	10	RESET#
7	NC	8	TDI
5	GND	6	TDO
3	GND	4	TCK
1	1.8V	2	TMS

Figure 31: Cortex Debug Connector

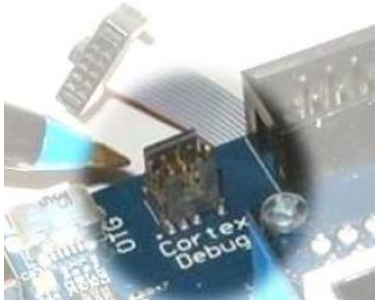


Table 39: Cortex Debug connector Signal Description

SIGNAL	DIRECTION	DEFINITION
1.8V	Ouput	+1.8V power supply.
GND	-	Logic Ground
TDI	Input	JTAG TDI for QorIQ processor
TDO	Output	JTAG TDO for QorIQ processor
TCK	Input	JTAG TCK for QorIQ processor
TMS	Input	JTAG TMS for QorIQ processor
GND Detect	Input	GNDDetect is an optional board feature. Not used on VX3106.
RESET#	Input	Processor reset from CodeWarrior TAP.

4.2.4. M2 PCIe Connector J2201 (Bottom side, Option)

The socket J2201 is compliant with PCIe interface only.
This socket can host the following module types: 2242-XX-M and 2260-XX-M with XX = S1, S2, S3, D1, D2, D3, D4.

The socket J2201 is not compliant with D5 form factor.

Table 40: M.2 J2201 Sockets Pin Assignment

Pin	Signal	Signal	Pin
74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK (32kHz)	PEDET	69
	Connector Key	NC	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	NC	GND	57
56	NC	REFCLKP	55
54	PEWAKE#	REFCLKN	53
52	NC	GND	51
50	PERST#	PETp0	49
48	NC	PETn0	47
46	Reserved	GND	45
44	Reserved	PERp0	43
42	NC	PERn0	41
40	NC	GND	39
38	NC	NC	37
36	NC	NC	35
34	NC	GND	33
32	NC	NC	31
30	NC	NC	29
28	Reserved	GND	27
26	Reserved	NC	25
24	NC	NC	23
22	Reserved	GND	21
20	Reserved	NC	19
18	3.3V	NC	17
16	3.3V	GND	15
14	3.3V	NC	13
12	3.3V	NC	11
10	DAS_DSS#	GND	9
8	NC	NC	7
6	NC	NC	5
4	3.3V	GND	3
2	3.3V	GND	1

Table 41: M.2 J2201 Socket Signals Definition

Signal PCIe	Dir.	Definition
3.3V	O	+3.3V power supply. On VM606x, protected by dedicated 1.5A resettable fuse (one for each M.2 socket).
GND	-	Logic ground.
DAS_DSS#	I	On VX3106 connected to dedicated CPLD pin. DAS is not connected to a LED (which is the main purpose of this signal) and DSS is not used.
PEDET	I	PEDET (PCI Express Detect) as per PCI Express M.2 specification is driven low by SATA modules and high-Z by PCI Express modules (seen as a logic 1 due to on-board pull-up resistor). On VX3106, this signal is connected to a dedicated CPLD pin.
PERn0	I	- PCI Express: Receive differential signal minus as per PCI Express M.2 & PCI Express 3.0 specifications.
PERp0	I	- PCI Express: Receive differential signal plus as per PCI Express M.2 & PCI Express 3.0 specifications.
PERST#	O	- PCI Express: PCI Express PERST# as per PCI Express M.2 specification. On VM606x handled by CPLD.
PETp/n0	O	- PCI Express : Transmit differential pairs as per PCI Express M.2 & PCI Express 3.0 specifications.
PEWAKE#	I	- PCI Express: Open drain WAKE# signal as per PCI Express M.2 specification. Driven by M.2 module to allow the platform to reactivate the link main power rails and reference clock. On VX3106, this signal is wire-ORed with other WAKE# signals from M.2 modules. It is connected to SoC WAKE_# and WAKELAN_# pins.
REFCLKP/N	O	- PCI Express: PCI Express differential reference clock (100 MHz) as per PCI Express M.2 & PCI Express 3.0 specifications.
SUSCLK	O	Suspend Clock for low power mode handling as per PCI Express M.2 specification (32.768 kHz, duty cycle between 30% and 70%, 200ppm). On VX3106, connected to cPLD CLK_32K_M2S1.

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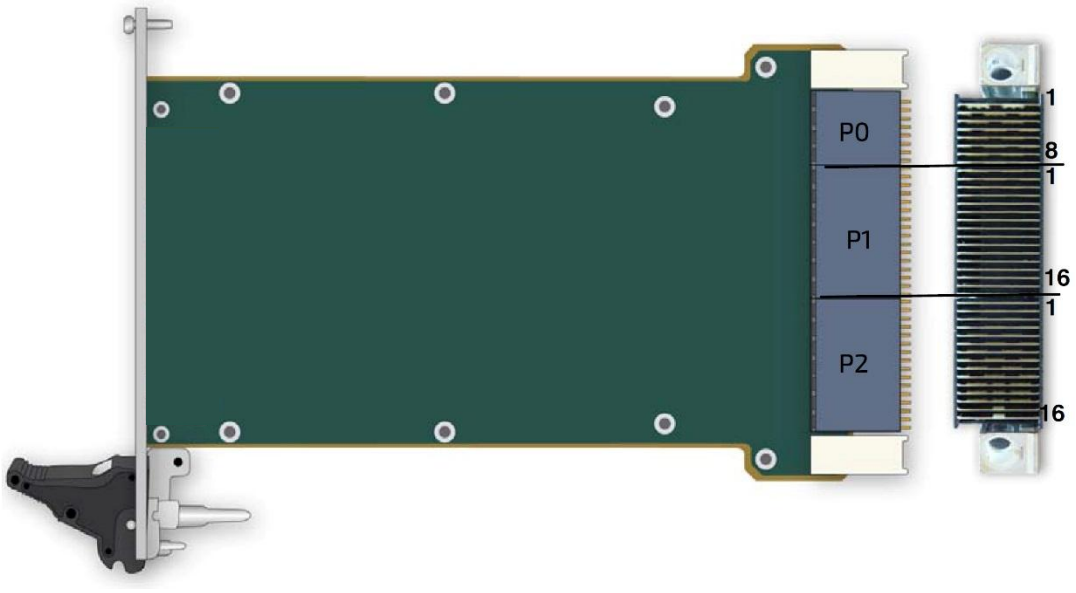
4.3. Rear Connectors

VPX Bus Interface

The complete 3U VPX connectors configuration comprises three connectors named P0 to P2:

- P0: 8-wafer 7-row connector.
- P1 - P2: 16-wafer 7-row differential connectors.

Figure 32: VPX Connectors



4.3.1. P0 Connector

Table 42: VPX Connector P0 Wafer Assignment

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	+12V (VS1)	+12V (VS1)	+12V (VS1)	NC	NC (VS2)	NC (VS2)	NC (VS2)
2	+12V (VS1)	+12V (VS1)	+12V (VS1)	NC	NC (VS2)	NC (VS2)	NC (VS2)
3	NC (VS3)	NC (VS3)	NC (VS3)	NC	NC (VS3)	NC (VS3)	NC (VS3)
4	CMB1 CLK	CMB1 DAT	GND	NC	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3V3_AUX	GND	CMB0 CLK	CMB0 DAT
6	GA3*	GA2*	GND	NC	GND	GA1*	GA0*
7	GPIO5 (TCK)	GND	NC (TDO)	NC (TDI)	GND	GPIO3 (TMS)	GPIO4 (TSRS*)
8	GND	REF_CLK-	REF_CLK+	GND	NC (AUX_CLK-)	NC (AUX_CLK+)	GND
CASE	GND						

* signal active when low

Table 43: VPX Connector P0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
+12V	+12 Volts DC power (VS1 VPX supply). NC (+12V) pins are not connected (VS2 VPX supply)
NVMRO	Non-Volatile Memory Read Only. When asserted (logical 1), prevents any non-volatile memory from being updated.
GAi	Geographical address pins
GAP	Geographical address parity
GND	Ground
GPIO5	General purpose I/O 5 (handled by CPLD).
GPIO4	General purpose I/O 4 (handled by CPLD).
GPIO3	General purpose I/O 3 (handled by CPLD).
CMB0	I2C Bus 0
CMB1	I2C Bus 1
REF_CLK+/-	The Reference Clock is a bussed differential pair. Output if the VX3106 is plugged in the system controller slot, input otherwise. It enables the entire system to synchronize to a common time reference if desired. Counter/timer in the CPLD can use this clock
AUX_CLK+/-	Not Connected on VX3106
SYSRESET*	System Reset. Input and open collector output.

* See section 3.6 - GPIOs and GDISCRETE1 – page 63.

4.3.2. P1 Connector

Table 44: VPX Connector P1 Wafer Assignment

- Legend for Table 42:

P1_VBAT	Battery Voltage	SATA_TX/RX+/-	SATA Port
P1_SYS_CON*	System Controller	ETH2	1000BASE-T Ehernet
PCIe0/1 LxRX | LxTX	x1 PCI-Express Ports	ETHx TX/RX	1000BASE-KX Ethernet controller links 0 and 1 from integrated 10 GbE controller as per VITA 46.7.
USB	USB2.0 and 3.0 Ports		

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	GDISCRETE1	GND	PCIe0 L0-TX-	PCIe0 L0-TX+	GND	PCIe0 L0-RX-	PCIe0 L0-RX+
2	GND	NC	NC	GND	NC	NC	GND
3	VBAT	GND	NC	NC	GND	NC	NC
4	GND	NC	NC	GND	NC	NC	GND
5	SYS_CON*	GND	PCIe1 L0-TX-	PCIe1 L0-TX+	GND	PCIe1 L0-RX-	PCIe1 L0-RX+
6	GND	NC	NC	GND	NC	NC	GND
7	NC	GND	NC	NC	GND	NC	NC
8	GND	NC	NC	GND	NC	NC	NC
9	USB_P3_PWR	GND	SATA_TX-	SATA_TX+	GND	SATA_RX-	SATA_RX+
10	GND	NC	NC	GND	NC	NC	GND
11	USB_P2_PWR	GND	USB3_P2_TX-	USB3_P2_TX+	GND	USB3_P2_RX-	USB3_P2_RX+
12	GND	USB2_P3_D-	USB2_P3_D+	GND	USB2_P2_D-	USB2_P2_D+	GND
13	GPIO1	GND	ETH2_DB-	ETH2_DB+	GND	ETH2_DA-	ETH2_DA+
14	GND	ETH2_DD-	ETH2_DD+	GND	ETH2_DC-	ETH2_DC+	GND
15	Maskable Reset*	GND	ETH1 TX-	ETH1 TX+	GND	ETH1 RX-	ETH1 RX+
16	GND	ETH0 TX-	ETH0 TX+	GND	ETH0 RX-	ETH0 RX+	GND
CASE	GND						

* signal active when low

Table 45: VPX Connector P1 Signal Definition

MNEMONIC	SIGNAL DEFINITION
PCIe0/1 Lx-RX+/-	x1 PCI Express Link. Receive +/-, gen1 or gen2
PCIe0/1 Lx-TX+/-	x1 PCI Express Link. Transmit +/-, gen1 or gen2
SATA_RX+/-	SATA bus Receive +/-, gen1, gen2 or gen3
SATA_TX+/-	SATA bus Transmit +/-, gen1, gen2 or gen3
USB3_P2_RX+/-	USB3.0 port 2 Receive
USB3_P2_TX+/-	USB3.0 port 2 Transmit
USB2_Pz_D+/-	USB2.0 port z (z=2 or z=3)
ETH2_Dy+/-	Ethernet 1000/100/10BASE-T port 2
ETHx RX+/-	10GBASE-KR or 1000BASE-KX Ethernet x: Receive data +/-
ETHx TX+/-	10GBASE-KR or 1000BASE-KX Ethernet x: Transmit data +/-
GDISCRETE1	Open VPX GDISCRETE1 signal
GPIO1	General Purpose I/O 1 (handled by the CPLD)

MNEMONIC	SIGNAL DEFINITION
Maskable Reset(1) or GPIO2	Reset input or Optional general purpose I/O 8 (handled by CPLD) (may be left unconnected if not used).
GND	Ground
SYS_CON*	System Controller Slot Indication
VBAT	Battery Voltage Input, 3V. Optional alternated source for RTC backup voltage.

(1) See section 3.6 - GPIOs and GDISCRETE1 – page 63.

4.3.3. P2 Connector

Table 46: VPX Connector P2 Wafer Assignment

- Legend for Table 44:

COM1	Serial lines 1	DVI	DVI port if M.2 with DVI port is equiped on the bottom side
COM2	Serial lines 2		

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	COM1_RTS or **COM1_TXD+**	GND	DVI TMDS1-	DVI TMDS1+	GND	DVI TMDS2-	DVI TMDS2+
2	GND	DVI CLK-	DVI CLK+	GND	DVI TMDS0-	DVI TMDS0+	GND
3	COM1_TXD or **COM1_TXD-**	GND	DVI PWR	DVI HPD	GND	DVI SCL	DVI SDA
4	GND	**NC**	**NC**	GND	**NC**	**NC**	GND
5	COM1_CTS or **COM1_RXD+**	GND	**NC**	**NC**	GND	**NC**	**NC**
6	GND	**NC**	**NC**	GND	**NC**	**NC**	GND
7	COM1_RXD or **COM1_RXD-**	GND	**NC**	**NC**	GND	**NC**	**NC**
8	GND	**NC**	**NC**	GND	**NC**	**NC**	GND
9	COM2_RTS or **COM2_TXD+**	GND	**NC**	**NC**	GND	**NC**	**NC**
10	GND	**NC**	**NC**	GND	**NC**	**NC**	GND
11	COM2_TXD or **COM2_TXD-**	GND	**NC**	**NC**	GND	**NC**	**NC**
12	GND	**NC**	**NC**	GND	**NC**	**NC**	GND
13	COM2_CTS or **COM2_RXD+**	GND	**NC**	**NC**	GND	**NC**	**NC**
14	GND	**NC**	**NC**	GND	**NC**	**NC**	GND
15	COM2_RXD or **COM2_RXD-**	GND	**NC**	**NC**	GND	**NC**	**NC**
16	GND	**NC**	**NC**	GND	**NC**	**NC**	GND
CASE	GND						

* signal active when low

Table 47: VPX Connector P2 Signal Definition

MNEMONIC	SIGNAL DEFINITION
COM1	Serial Lines, EIA-232/EIA-485
COM2	Serial Lines, EIA-232/EIA-485
DVI	DVI Port
GND	Ground

4.4. LEDs

4.4.1. Status LEDs Normal Operation

There are five bicolor LEDs (Red/Green) on the front panel of the VX3106 3U VPX board.

Figure 33: LEDs Front panel

4.4.2. LEDs Activity

Table 48: LEDs Description

CPU LED	DESCRIPTION
●	LED OFF
●	Red LED
●	Green LED
●	Orange LED
✳	Red blinking LED
✳	Green Blinking LED
✳	Orange blinking LED
✳	Not blink: Indicates that the corresponding LED gives an additional information if any LED is blinking at the same time

The following table describes the information that the LED can report:

Table 49: LEDs Activity

L1	L2	L3	L4	L5	MEANING
●	Not Blink	Not Blink	Not Blink	Not Blink	Permanent system error. Internal VX3106 power is off. In this state L2, L3, L4 and L5 do not carry the meaning described in this table but an error code detailed in the **ERRORS CODES** table.
● ✳					Standby (board's power supplies are off) Flashing green on CPLD activity (IFC bus or I2C)
● ✳					Board reset asserted Blinking orange not used
●					Normal operation (board running)
	●				Watchdog timeout
	● ✳				Normal operation mode Blinking M.2 SATA activity
	●				Factory test mode Same than green, but when PLD_FACTORY_MODE switch is ON
	●				Normal operation (board running)
		●			Temperature alert
		● ✳			Ethernet (EC2) link present and at 1000BaseT. Blinking (EC2) activity
		● ✳			Ethernet (EC2) link present and at not at 1000BaseT. Blinking (EC2) activity
		●			Normal operation (board running)
			●		PBIT reported an error (through reg 0x2)
			● ✳		Not used Not used
			● ✳		Not used Not used
			●		Normal operation (board running)
				●	Not used
				● ✳	Not used Not used
				● ✳	Not used Not used
				●	Normal operation (board running)

L1	L2	L3	L4	L5	POWER GOOD ERRORS
🔴	⚫	⚫	⚫	⚫	Not used
🔴	🔴	⚫	⚫	⚫	ERR_5V0_PWRGD
🔴	⚫	🔴	⚫	⚫	ERR_3V3SB_PWRGD
🔴	🔴	🔴	⚫	⚫	ERR_3V3_PWRGD
🔴	⚫	⚫	🔴	⚫	ERR_3V3SB_SRC
🔴	🔴	⚫	🔴	⚫	ERR_1V5_MPCIE_PWRGD
🔴	⚫	🔴	🔴	⚫	Not used
🔴	🔴	🔴	🔴	⚫	Not used
🔴	⚫	⚫	⚫	🔴	ERR_1V8_PWRGD
🔴	🔴	⚫	⚫	🔴	ERR_1V2_DDR4_PWRGD
🔴	⚫	🔴	⚫	🔴	ERR_VR2V5_DDR4_PWRGD
🔴	🔴	🔴	⚫	🔴	ERR_1V35_PWRGD
🔴	⚫	⚫	🔴	🔴	ERR_CPU_VDD1_PWRGD
🔴	🔴	⚫	🔴	🔴	ERR_CPU_VDD2_PWRGD
🔴	⚫	🔴	🔴	🔴	ERR_THERM_FAULT
🔴	🔴	🔴	🔴	🔴	Not used
🔴	⚫	⚫	⚫	🟠	ERR_BP_UV_PWRGD
🔴	🔴	⚫	⚫	🟠	ERR_BP_OV_PWRGD

5/ Power and Thermal Specifications

5.1. Electrical Specifications

5.1.1. System Power

The considerations presented in the ensuing sections must be taken into account by system integrators when specifying the VX3106 system environment.

5.1.1.1. VX3106 Baseboard

The VX3106 board has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the VX3106 should be carefully tested to ensure compliance with these ratings.

Table 50: Maximum Input Power

SUPPLY VOLTAGE	MAXIMUM PERMIT VOLTAGE
3.3V aux	3.5V
+12V (VPX VS1)	13V

CAUTION: The maximum permitted voltage indicated in the table above must not be exceeded. Failure to comply with these figures may result in damage to your board.

The following table specifies the range of the different input power voltages within the board is functional. The VX3106 is not guaranteed to function if the board is not operating within the prescribed limits.

Table 51: DC Operational Input Voltage Ranges

SUPPLY VOLTAGE	Operational Input Voltage
3.3V aux	3.3V +/- 5% (3.135V min to 3.465V max) inclusive of ripple
+12V (VPX VS1)	12V+/- 5% (11.4V min to 12.6V max) inclusive of ripple

5.1.1.2. Backplane

Backplanes to be used with the VX3106 must be adequately specified. The backplane must provide optimal power distribution for the VS1, VS2, VS3 and 3V3aux power inputs.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided.

5.1.1.3. Power Supply Units

Power supplies for the VX3106 must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires.

An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for die resistance variations.

Tolerance

The following table provides information regarding the required characteristics for each board input voltage.

Table 52: Input Voltage Characteristics

VOLTAGE	Nominal value	Tolerance	Max Ripple (p-P)	Remarks
12V (VS1)	+12.0 VDC	+/-5%	50mV over a range 0-20Mhz	Main voltage
3.3V (VS2)	+3.3 VDC	3.25V min – 3.45V MAX	50mV over a range 0-20Mhz	Not used on the VX3106
5.0V (VS3)	+5.0 VDC	+%5/-2.5%	50mV over a range 0-20Mhz	Not used on the VX3106
3.3Vaux	+3.3 VDC	+/-5%	50mV over a range 0-20Mhz	Not mandatory for the VX3106
GND	Ground not directly connected to potential earth (PE) on the VX3106 board			

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No Voltage of reverse polarity may be present on any output during turn-on or turn-off.

Rise time

On +12V (VS1) power supply, monotonic rise time have to be included between 1 ms and 25 ms at Power on.

Regulation

The power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it went below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

5.1.2. Input Powers Supplies Protection

The input power rails are protected on the VX3106 by fuse as described in Table 53.

To prevent safety hazards, the chassis power supply must not exceed the Voltage Rating and Interrupt Rating of the fuse.

Table 53: Input Powers Supplies Protection

POWER RAIL	VPX VS1	VPX 3.3 V AUX
LOCATION	P0	P0
VOLTAGE	+12 V	+3.3 V
PROTECTION	Non resettable fuse	Non resettable fuse
RATED CURRENT	12 A	1.5 A
TRIP CURRENT	-	2.20 A @ 85 °C 3.00 A @ 25 °C 3.54 A @ -40 °C
TYPICAL MELT I^2T	7.0	-
VOLTAGE RATING	24 V	6 V
INTERRUPTING RATING	150 A	100 A
MANUFACTURER / PN	3216FF12-R	NANOSMDC150F-2

5.1.3. Output Powers Supplies Protection

On the VX3106, all the output power supplies provided on connectors are protected by fuse or current-limiting devices as described in Table 54: Output Powers Supplies Protection.

Table 54: Output Powers Supplies Protection

Port	Function	Location	Voltage	Protection	Worst Case Hold Rated Current (Maximum operation temperature)	Trip current	Characteristics	Note
VPX P1 Rear USB Power pins	P1 USB port 2 power	On board near P1	+5 V	PTC resettable fuse	1.5 A	-	-	
VPX P1 Rear USB Power pins	P1 USB port 3 power	On board near P1	+5 V	PTC resettable fuse	1.5 A	-	-	
mPCIe. Slots	mPCIe slot power supply	On board	+3.3 V	Non resettable fuse	4.5 A	-	-	
M2. Slots	M2 slot power supply	On board	+3.3 V	Non resettable fuse	4.5 A	-	-	

5.2. Power Specifications

5.2.1. VX3106 Thermal Power

The power consumption tables below list the voltage and power specifications for the VX3106 board. The values were measured using an 8-slot passive VPX backplane.

Table 55: VX3106 Thermal Power: board power based on current measurements

	POWER MODE	CPU POWER MEASURED	MAX TOTAL POWER CONSUMP-TION	CURRENT DRAWN	TEST CONDITION
VX3106 QorIQ LS1046A 1.2GHz	Normal mode	6.22W	20.46W	1.54A	Linux, 65°C ambient temperature, 6x Gigabit Ethernet links, 4GB single bank DDR4-1600 memory configuration, several tests (4 FFT tests, 4 memory tests, 1 M.2 SATA, 1 M.2 PCIe, 1 USB)
	Linux idle	3.22W	11.6W	1A	Linux, 65°C ambient temperature, 6x Gigabit Ethernet links, 4GB single bank DDR4-1600 memory configuration.

Table 56: Rail Current Draw

PROCESSOR	0.9V RAIL CURRENT DRAW	
	Typical	MAX
LS1046A @1.2GHz	5.95A	6.81A

Maximum and typical current draw are intended as without mezzanine card or USB device plugged on board.

5.2.2. Maximum Power Consumption of M.2 Module

The M.2 socket 3, key M on VX3106 supports up to 2.5A of current consumption on 3.3V rail per defined in PCI Express M.2 Specification (maximum highest averaged current value over any 100-microsecond period).

The following table resumes the current consumption limit on M.2 module.

Table 57: Current of M.2 module

VOLTAGE	STANDARD LIMIT CURRENT	DESIGN LIMIT CURRENT
3.3V	2.5 A	2.5 A

5.2.3. Maximum Power Consumption of miniPCIe Module

The miniPCIe socket on VX3106 supports respectively up to 2.75 A and 0.5 A of current consumption on 3.3V rail and 1.5V rail per defined in PCI Express Mini card Specification (maximum highest averaged current value over any 100-microsecond period).

The following table resumes the current consumption limit on M.2 module.

Table 58: Current of miniPCIe module

VOLTAGE	STANDARD LIMIT CURRENT	DESIGN LIMIT CURRENT
3.3V	2.75 A	2.75 A
1.5V	0.5 A	0.5 A

5.2.4. Processor Power Monitoring and Management

The VX3106 implements a current sensor on processor core power supply, this device (INA220) accessible from the processor I2C bus gives the current draw by the processor core voltage.

5.3. Thermal Considerations

The following chapters provide system integrators with the necessary information to satisfy thermal and airflow requirements when implementing VX3106 applications.

5.3.1. Board Thermal Monitoring

The following chapters provide system integrators with the necessary information to satisfy thermal and airflow requirements when implementing VX3106 applications.

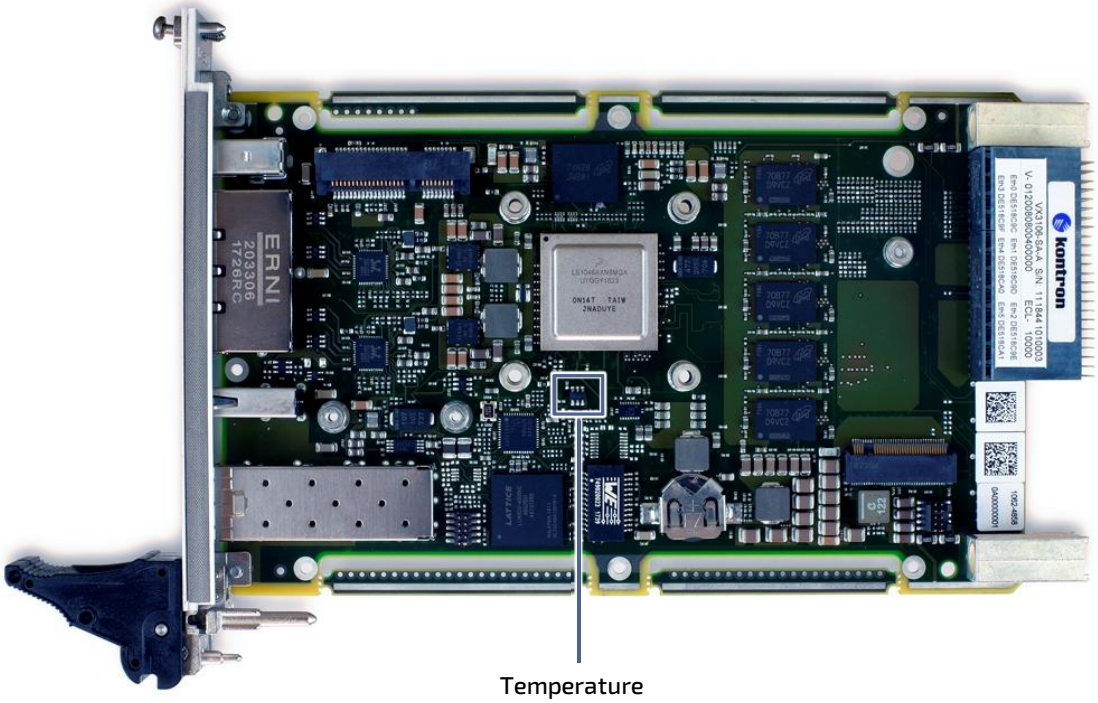
To ensure optimal and long-term reliability of the VX3106, all onboard components must remain within the maximum temperature specifications. The most critical components on the VX3106 are the processor and the memory. Operating the VX3106 above the maximum operating limits will result in permanent damage to the board.

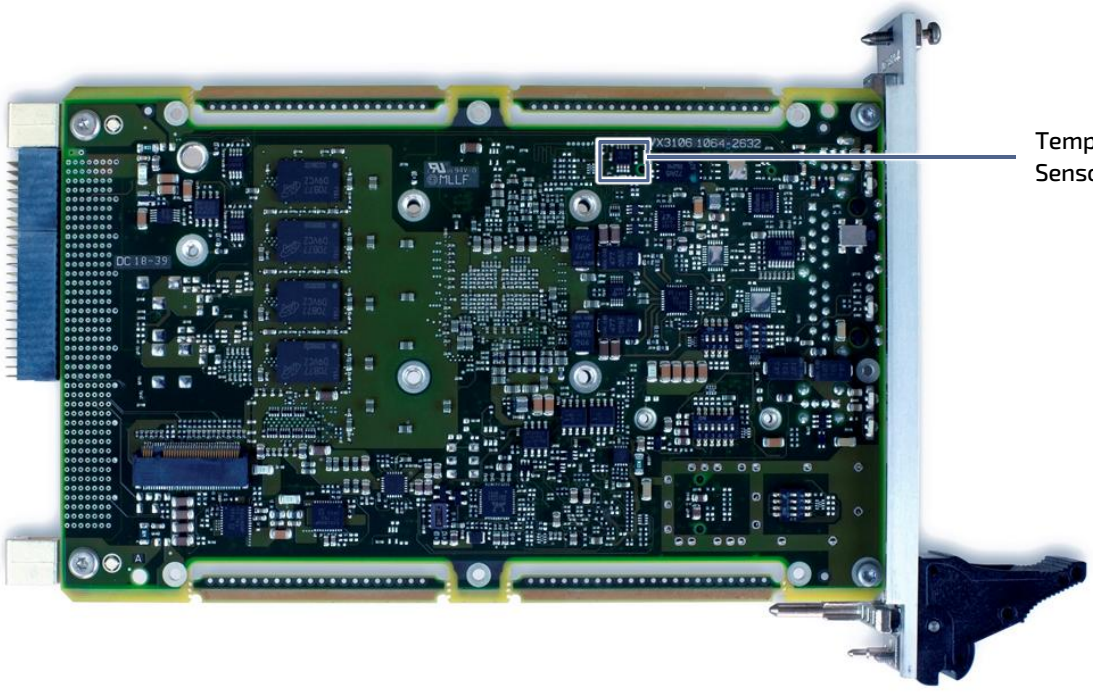
The VX3106 includes several temperature sensors to measure the onboard temperature values:

- Thermal Sensors integrated in the processor
- Two onboard temperature sensors (including processor remote sensor)

One of on-board temperature sensors (National LM73) and one on-board temperature sensors (Texas Instrument TMP411) are located on the I2C bus, and managed by the CPLDs. Refer to Figure 22: I2C Diagram page 56.

Figure 34: Temperature Sensor Location





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TMP411 Key specifications:

TMP411 supports local and remote temperature sensor. TMP411 supports two alarm outputs: ALERT#, THERM# signals to activate system protection, connected to cPLD for event reporting.

- Remote temperature resolution / accuracy : 0.0625°C / ±1.25°C Typ (MAX ±2.5°C)
- Local temperature resolution / accuracy : 0.5°C / ±1°C Typ (MAX ±3°C)
- Operating temperature: –40°C to +125°C
- IC2 address: 0x4C

LM73 Key specifications:

- Local accuracy: / ±2°C
- Operating temperature: -40°C / +150°C
- IC2 address: 0x48

When the LED3 on the front panel is lit red after boot-up, it indicates that one of the processor temperature sites is above this programmed threshold value.

5.3.2. Processor Thermal Monitoring

To allow optimal operation and long-term reliability of the VX3106, the QorIQ Layerscape LS1046A processor must remain within the maximum die temperature specification. The maximum operating temperature for the processor die (TJMAX) is 105°C.

The QorIQ LS1046A processor implements a Thermal Monitoring Unit (TMU) to monitor and report the temperature from one or more remote temperature measurement sites located on processor.

- One Temperature Sensor near DDR controller
- One Temperature Sensor near SerDes
- One Temperature Sensor near Frame manager
- One Temperature Sensor near ARM A72 core
- One Temperature Sensor near SEC

The TMU monitors these sensor sites and signal an alarm if a programmed threshold is ever exceeded. The current and average temperatures are continuously captured for each temperature sites and logged in resister set.

When the LED3 on the front panel is lit red after boot-up, it indicates that one of the processor temperature sites is above this programmed threshold value.

Catastrophic Cooling Failure Sensor

The Catastrophic Cooling Failure Sensor protects the processor from catastrophic overheating.

The Catastrophic Cooling Failure Sensor threshold is set to 110°C. When the junction temperature of processor will exceed this value, the processor will send an interrupt to CPLD for performing a shutdown of the internal power supplies. Once activated, the event remains latched until the VX3106 undergoes a power-on restart (all power off and then on again).

5.3.3. External Thermal Regulation

To ensure the best possible basis for operational stability and long-term reliability, the VX3106 is equipped with a heat sink (SA and WA classes only). Coupled together with system chassis, which provides variable configurations for forced airflow, controlled active thermal energy dissipation is guaranteed.

The physical size, shape, and construction of the heat sink ensures the lowest possible thermal resistance. In addition, the VX3106 has been specifically designed to efficiently support forced airflow as found in modern VPX systems.

Thermal Characteristics Tables

The thermal characteristic table shown in the following sections illustrates the maximum ambient air temperature as a function of the volumetric airflow rate for the processor frequency indicated.

The table is intended to serve as guidance for reconciling board and system with the required computing power/frequency considering the thermal aspect.

There are two values representing the recommended and upper levels working points. These values are based on processor frequency and on processor junction temperature. When operating below the recommended value, the CPU and critical components run steadily without any intervention of thermal supervision. When operated above the maximal junction temperature of 105°C, thermal protection mechanisms take effect resulting in an emergency stop in order to protect the CPU and critical components from thermal destruction.

How to read the Table

Select a board class, a processor frequency and choose a working point just above the recommended. For a given flow rate there is a maximum airflow input temperature (= ambient temperature) provided. Between this operating point and the maximum, thermal supervision will not be activated. Above the maximal operating point, thermal supervision will become active protecting the CPU and the critical components from thermal destruction. The minimum airflow rate provided must be included between the recommended operating point and the maximum specified in the table to guarantee a correct cooling.

Values indicated in this table are issued from Coremark® benchmark with 100% of processor core workload.

Volumetric Flow Rate

The volumetric flow rate refers to an airflow through a fixed cross-sectional area (i.e. slot width x depth). The volumetric flow rate is specified in cfm (cubic-feet-per-minute).

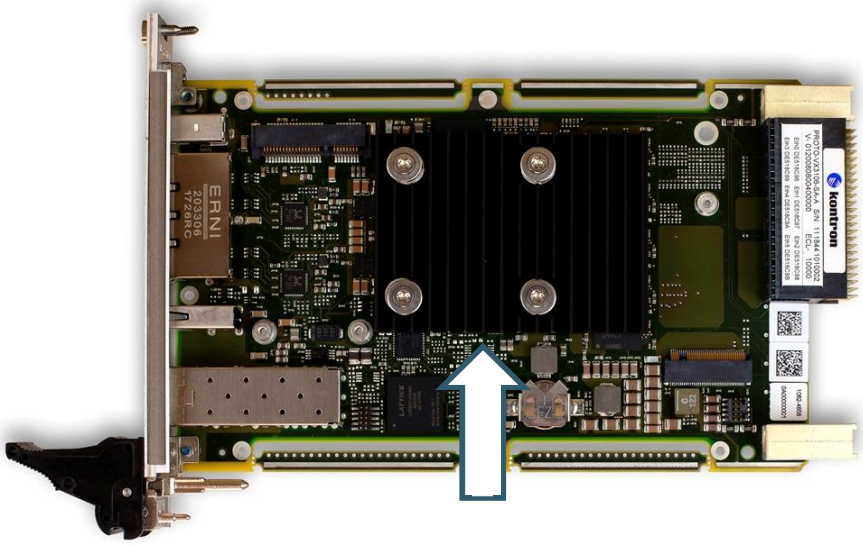
Airflow

At a given cross-sectional area and a required flow rate, an average, homogeneous airflow speed can be calculate using the following formula:

Airflow = Volumetric Flow Rate / Area

The airflow is specified in m/s (meter-per-second).

Figure 35: Airflow Direction



5.3.3.1. Thermal Operating Limits for VX3106

The following table indicates the operational limits of the VX3106 taking into consideration processor frequency vs. ambient air temperature vs. airflow rate. The measurements were made based on a 5HP slot (1 inch height) and using thermal benchmark from Coremark® with 100% of processor workload.

Table 59: VX3106 Thermal operating limits

CLASS	BOARD	TJMAX ALL CORES	TAMB	MIN AIRFLOW
SA Class	VM3106 SA LS1046A @ 1.2 GHz	< 65°C	55°C	5 CFM
		< 105°C	55°C	26 CFM
	VM3106 SA LS1046A @ 1.8 GHz	< 65°C	55°C	TBD
		< 105°C	55°C	TBD

The above table indicates the minimum air flow required for VX3106 cooling. Be careful, these values are intended as without mezzanine board presence (M.2 module or mPCIe module).

5.3.3.2. Peripherals

When determining the thermal requirements for a given application, peripherals to be used with the VX3106 must also be considered. Devices such as M.2 module, miniPCIe module, which are directly attached to the VX3106 must also be capable of being operated at the temperatures foreseen for the application. It may very well be necessary to revise system requirements to comply with operational environment conditions.

In most cases, this will lead to a reduction in the maximum allowable ambient operating temperature or even require active cooling of the operating environment.

CAUTION: As Kontron assumes no responsibility for any damage to the VX3106 or other equipment resulting from overheating of the CPU, it is highly recommended that system integrators as well as end users confirm that the operational environment of the VX3106 complies with the thermal considerations set forth in this document.

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