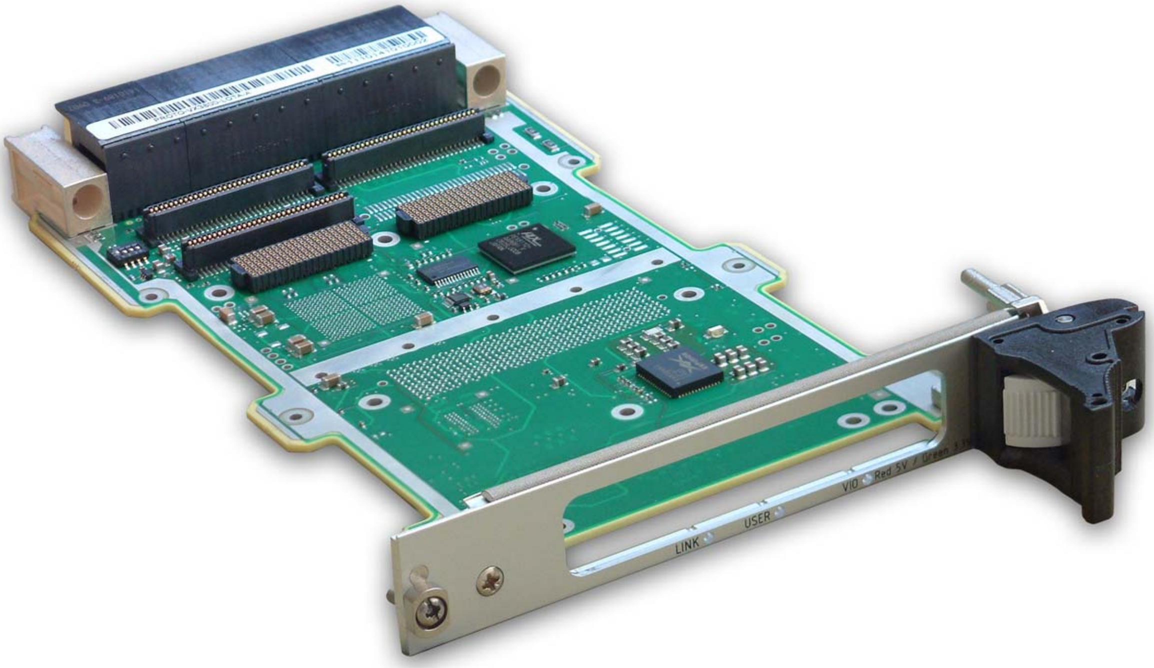
» VX3800 «



3U VPX XMC/PMC Carrier
User's Guide

CA.DT.A78-1e - April 2011

Revision History

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Environmental protection is a high priority with Kontron.

Kontron follows the DEEE/WEEE directive.

You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- reduce waste arising from electrical and electronic equipment (EEE)
- make producers of EEE responsible for the environmental impact of their products, especially when they become waste
- encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- improve the environmental performance of all those involved during the lifecycle of EEE

Conventions

This guide uses several types of notice: Note, Caution, ESD.

Note: this notice calls attention to important features or instructions.

Caution: this notice alert you to system damage, loss of data, or risk of personal injury.

ESD: This banner indicates an Electrostatic Sensitive Device.

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix `0x' shows a hexadecimal number, following the `C' programming language convention.

The multipliers `k', `M' and `G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when `K', `M' and `G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

When describing transfer rates, `k' `M' and `G' mean $*10^3$, $*10^6$ and $*10^9$ *not* $*2^{10}$ $*2^{20}$ *and* $*2^{30}$*.*

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and CompactPCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Signal names ending with an asterisk (*) or a hash (#) denote active low signals; all other signals are active high.

Signal names follow the PICMG 2.0 R3.0 CompactPCI Specification and the PCI Local Bus 2.3 Specification.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.

Caution, Electric Shock!
Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron’s product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron’s Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Chapter 1 - Introduction

The VX3800 is a member of the Kontron's VITA 46 VPX range of products. The VX3800 is designed to operate in a 3U VPX peripheral slot and provides support for any standard mezzanine XMC or PMC.

In this document, the term:

» VX3800 will be associated to the 3U VPX board

- VX3800-SA will be associated to the standard commercial version of the board.
- VX3800-RC will be associated to the rugged conduction-cooled version of the board.

» VX3800-RTM will be associated to the 3U VPX Rear Transition Module (RTM).

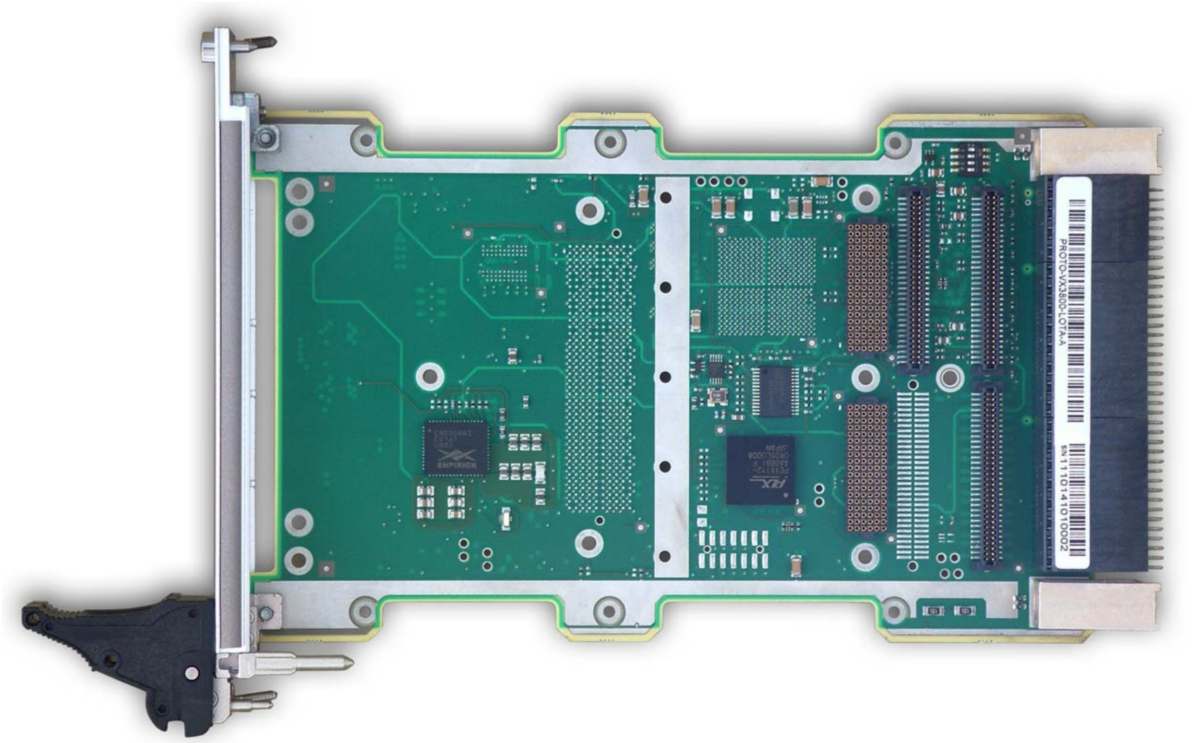


Figure 1: VX3800-SA Overview

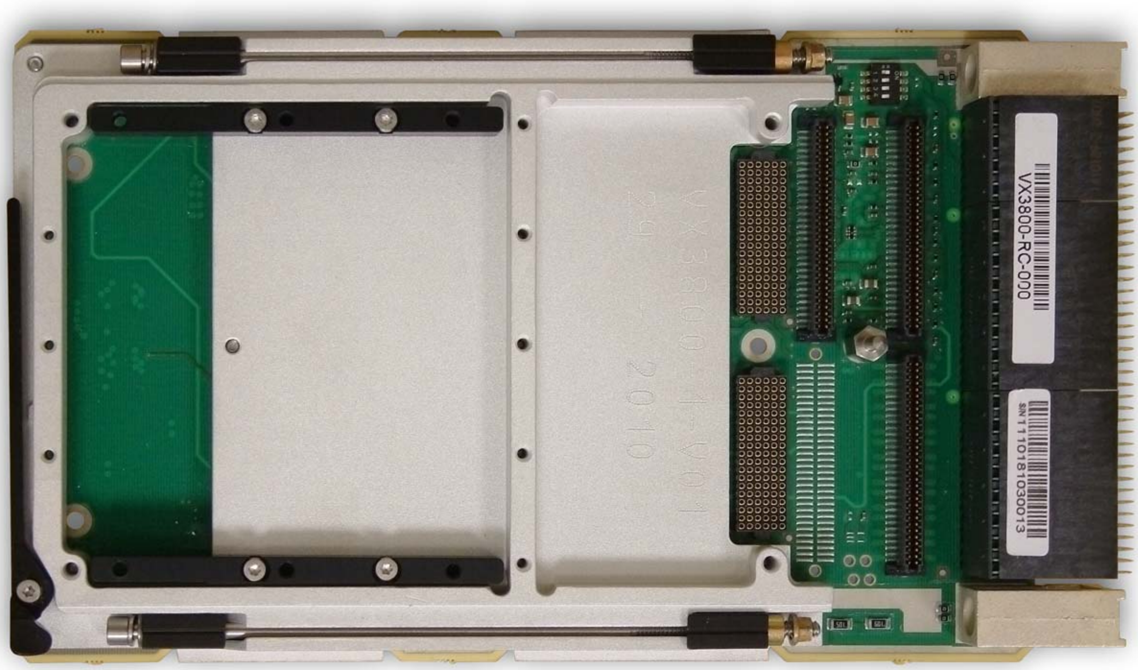


Figure 2: VX3800-RC Overview

1.1 Manual Overview

1.1.1 Objectives

This guide provides general information, hardware preparation and installation instructions, operating instructions and a functional description of the VX3800 board. The onboard programming, onboard firmware andother software (e.g. drivers and BSPs) are described in detail in separate guides (see section 1.8 “Related Publications").

As the standard policy for all the Kontron, hardware technical documentation reflects the most recent version of our products. The “Hardware Release Notes" (see section 1.8 “Related Publications") is to help to keep track of various evolutions that have happened during the early steps of the VX3800 ramp-up or later in its lifetime.

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

1.1.2 Audience

This guide is written to cover, as far as possible, the range of people who will handle or use the VX3800, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, systems, cabling, grounding and communications.

1.1.3 Scope

This guide describes all variants of the VX3800 series. It does not cover any XMC/PMC modules which are described in specific guides (see section 1.8 “Related Publications").

1.1.4 Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with a brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- Chapter 1 - Introduction (this chapter)
- Chapter 2 - Functional Description
- Chapter 3 - Installation
- Chapter 4 - Power Consideration

1.2 VPX Overview

VPX (VITA 46) specifications establish a new direction for the next revolution in bus boards. VPX is a proposed ANSI standard which breaks out from the traditional connector scheme of VMEbus to merge the latest in connector and packaging technology with the latest in bus and serial fabric technology. VPX combines best-in-class technologies to assure a very long technology cycle similar to that of the original VMEbus solutions.

Traditional parallel VMEbus will continue to be supported by VPX through bridging schemes that assure a solid migration pathway.

For further information regarding this standards and its use, visit the home page of the VITA - Open Standards,Open Markets.

1.3 Board Overview

1.3.1 Main Features

The VX3800 is a 3U VPX carrier of a standard XMC/PMC mezzanine. It can be used on 3U VPX backplanes employing PCI-Express on the fabric interface.

» VPX Interface

The VX3800 can be configured to support either a x4-lane and a x1-lane PCI-express link on VPX standard P1 wafers 1 to 4 (Data plane 1)

As a manufacturing build option, the VX3800 can be interfaced to the VPX Data Plane 2 (P1 wafers 5 to 8).

» XMC Interface

The VX3800 features J5, J6 and J4 connectors.

The configured PCI-Express link on the VPX fabric interface is available on the XMC J5 connector.

Depending on the build option, either the I/O pins of J4 or J6 are routed to the VPX P2 connector.

» PMC Interface

The VX3800 supports a 32-bit PCI mezzanine slot. The 64 PMC rear I/O on mezzanine J4 are connected to the VPX P2 connector, depending on the build option.

PCI bus is 5V tolerant. VIO is set at 3.3V by default. A 5V VIO is a manufacturing build option. Please contact Kontron

» Software

The VX3800 does not host any CPU on board and interfaces the PCI-Express bus. It does not require any specific BSP nor Device Driver for use in a system.

» Harsh Environments

The VX3800 has been designed using the same PCB for both air and conduction-cooled boards. Builds variants span a complete range of temperature, shock and vibration requirements as specified in the VITA 47 standards.

1.3.2 Ordering Information

The VX3800 supports the VX3800-RTM, a 3U VPX rear Transition Module compliant to Rear Transition Module on VPX standard - VITA 46.10.

Preferred / Fast Track variant, Air Cooled: VX3800-SA-00000

Preferred / Fast Track variant, Conduction Cooled: VX3800-RC-0N000

VX3800 have several build options covering:

- PMC voltage keying Pin Signaling: 3.3V or 5V I/O : see chapter 2.4 page 23
- VPX P2 I/O Selection: PMC I/O or XMC IO on P2 : see Table 18 page 20
- VPX Data Plane Selection : DP1 or DP2 : see chapter 1.4.1 page 8
- Front panel size : 0.8” (4HP) or 1” (5HP) Front panel: see chapter 1.5 page 9
- Cooling method: Air Cooled (SA) or Rugged Conduction Cooled (RC) board: see chapter 1 page 1

Order Code Table

DESCRIPTION	Code	VX3800- SA	-	0	0	0	0	0
Environment Class : Standard (Air)	SA							
Rugged Conduction Cooled	RC							
Reserved	0							
Front Panel Front Panel (0.8 inch)	0							
Front Panel (1 inch)	1							
No Front Panel	N							
Data Plane Selection VPX DP1 Data Plane Interface	0							
VPX DP2 Data Plane Interface	1							
I/O Routing on VPX P2 PMC J4 I/O routing on VPX P2	0							
XMC J6 I/O routing on VPX P2	1							
PMC Slot VIO 3V3 signaling	0							
5V signaling	1							

Table 1: Order Code Table

1.3.3 I/O Interfaces

» Front Interfaces

FUNCTION	DESCRIPTION
PMC/XMC	PMC/XMC slot, 3.3V signaling, 5V tolerant
LEDs	3 LEDs reporting main interfaces activities

Table 2: Front I/O Interfaces

» Rear Interfaces

FUNCTION	DESCRIPTION
VPX	VPX standard on P0/P1/P2
PMC I/Os	64 bits of I/Os PMC, on P2
Reset	Main reset input available on P0 connector

Table 3: Rear I/O Interfaces

1.4 Board Diagram

The following diagrams provide additional information concerning board functionality and component layout.

1.4.1 Functional Block Diagram

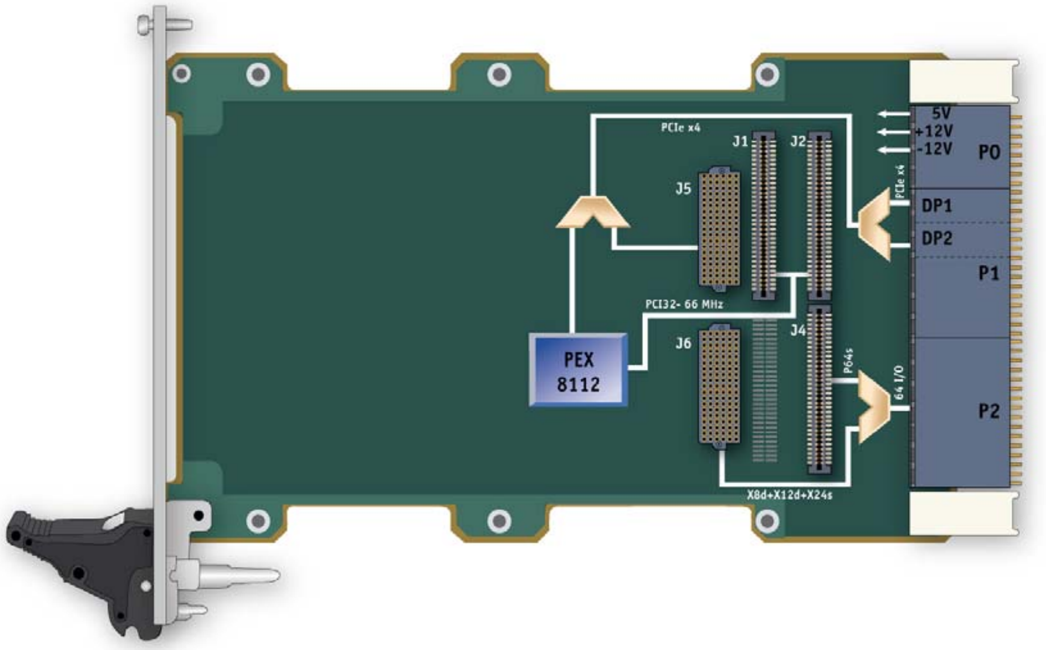


Figure 3: VX3800 Bloc Diagram

Note: VPX Interface to DP2 and XMC J6 rear I/O routing on P2 are modified COTS build options

1.4.2 Front Panel

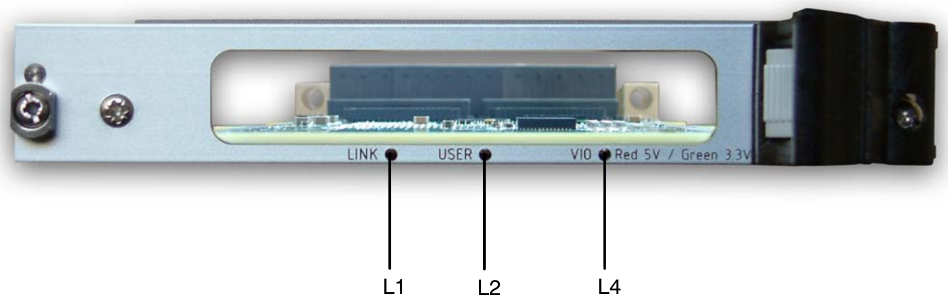


Figure 4: VX3800 Front Panel

Status LEDs Default Settings

Leds	Settings
LINK (L1)	Green: PMC Mode OFF: XMC Mode
USER (L2)	Maintenance
(L3 Layout but not equipped)	
VIO (L4)	Green: VIO=3.3V Red: VIO=5V Note: the function VIO=5V is a build option.

Table 4: LEDs Definition

1.5 Technical Specification

Form Factor	0.8" (4HP) or 1" (5HP) pitch for Standard Air (SA) 0.8" for Rugged Conduction cooled (RC)
Mechanical	3U, VPX compliant form factor
Power Supply	5V, +/-12V if required for mezzanine board
Environmental Specification	Refer to section 1.7.1 “Environmental Specifications"
Dimensions	99.85 mm x 162.54 mm

Table 5: Main Specifications

1.5.1 MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

GB		NS		ARW	AIC
25°C	40°C	25°C	40°C	55°C	40°C
658 515 h	464 837 h	131 885 h	102 664 h	131 885 h	102 664 h

1.6 Software Support

The VX3800 does not host any CPU on board and interfaces the PCI-Express bus. It does not require any specific BSP nor Device Driver for use in a system

1.7 Standard

This Kontron product complies with the requirements of the following standards.

TYPE	ASPECT	DESCRIPTION
CE	Emission	EN55022 EN61000-6-3
	Immission	EN55024 EN61000-6-2
	Electrical Safety	EN60950-1
Mechanical	Mechanical Dimensions	IEEE1101.10
Environmental	WEEE	Waste electrical and electronic equipment
	RoHS	Restriction of the use of certain hazardous substances in electrical and electronic equipment

Table 6: Standards

1.7.1 Environmental Specifications

ENVIRONMENTAL SPECIFICATIONS		
	SA - Standard Commercial	RC - Rugged Conduction-Cooled
Conformal Coating	Optional	Standard
Airflow	1.5 m/s without throttling at 55°C	N.A.
Temperature	VITA 47-Class AC1	VITA 47-Class CC4
Cooling Method	Convection	Conduction
Operating	0°C to +55°C	-40°C to +85°C
Storage	-45°C to +85°C	-45°C to +85°C
Vibration Sine (Operating)	2g / 20-500 Hz acceleration / frequency range	5g / 22-2,000 Hz acceleration / frequency range
Random	VITA 47-Class V1	VITA 47-Class V3
Shock (Operating)	20g / 11ms peak accel. / shock duration half sine	40g / 20ms peak accel. / shock duration half sine
Altitude (Operating)	-1,640 to 15,000 ft	-1,640 to 50,000 ft
Relative Humidity	90% non-condensing	95% non-condensing

Table 7: Environmental Specifications

1.8 Related Publications

The following publications contain information relating to this product:

PRODUCT	PUBLICATION
VITA 46.0	VPX Base Standard - ANSI/VITA 46.0-2007
VITA 46.4	PCI Express on VPX Fabric Connector - VITA draft Standard for Trial use
VITA 46.9	PMC/XMC rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules - VITA Draft Standard
VITA 46.10	Rear Transition Module for VPX - ANSI/VITA 46.10-2009

Table 8: Related Publications

Chapter 2 - Functional Description

2.1 PCI-Express Busses

VPX backplane	Data Plane DP1 (P1 wafer 1-4) Data Plane DP2 (P1 wafer 5-8)	Manufacturing option
XMC/PMC Carrier		Configurable by switch SW1.1 XMC or PMC Carrier
PCI-Express x1-Lane or x4-Lane	In PMC mode, must be set to PCi-Express x1-Lane because the PCI Express-to-PCI Bridge (ExpressLane™ PEX 8112) is a Gen1 component.	Configurable by switch SW1.2

Table 9: PCI-Express Busses Interfaces

VX3800 configured in PMC mode

The basic x1 link has a peak raw bandwidth of 2.5 Gbps (board components compatible PCI-Express Gen1). Because the bus is bidirectional (that is, data can be transferred in both directions simultaneously), the effective raw data transfer rate is 5 Gbps.

VX3800 configured in XMC mode

The basic x1 link has a peak raw bandwidth of 5 Gbps (board components compatible PCI-Express Gen2). Because the bus is bidirectional (that is, data can be transferred in both directions simultaneously), the effective raw data transfer rate is 10 Gbps.

As an example, the effective raw data transfer rate is link is 40 Gbps for an XMC which is PCI-Express Gen2 compatible.

2.2 VX3800 Connectors Layout

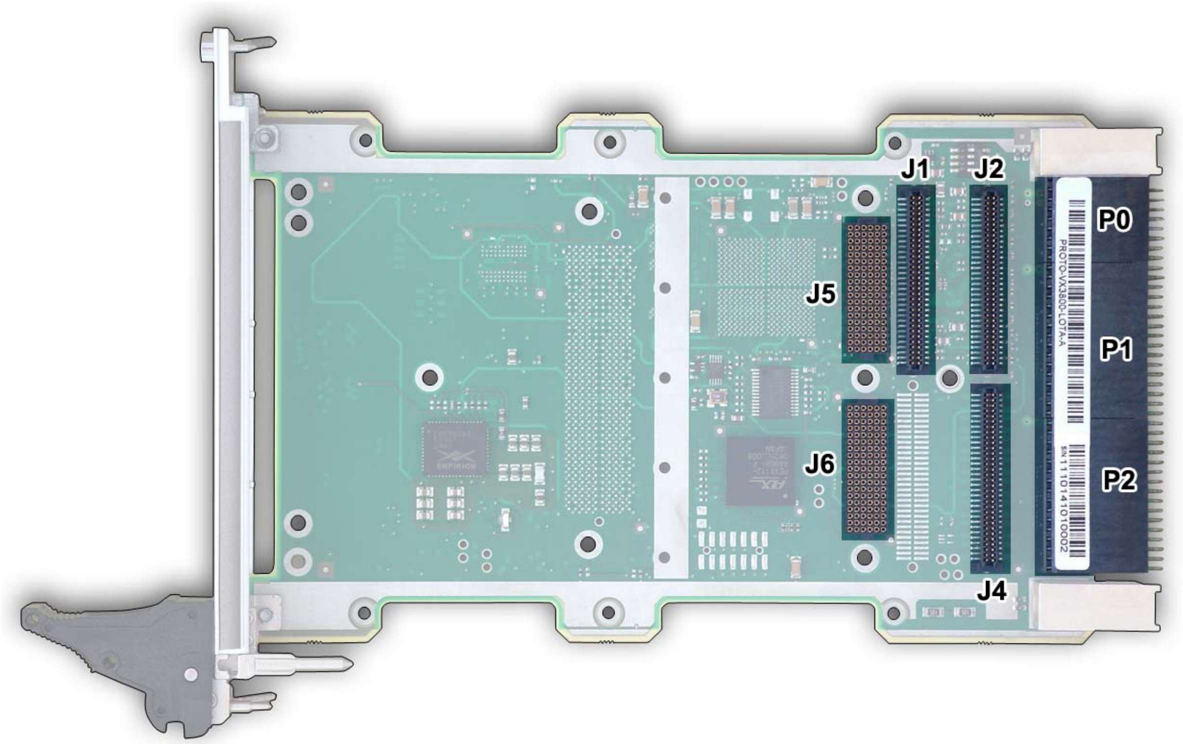


Figure 5: VX3800 Connectors Layout

2.3 Board Interfaces

2.3.1 VPX Bus Interface

The complete VPX connector configuration comprises three connectors named P0, P1 and P2

- P0: one 8-wafer 7-row connector
- P1: one 16-wafer 7-row connector
- P2: one 16-wafer 7-row connector

The VX3800 is not hot-swappable but supports the addition or removal of other boards whilst in a powered-up state.

The VX3800 is designed for a VPX bus architecture.

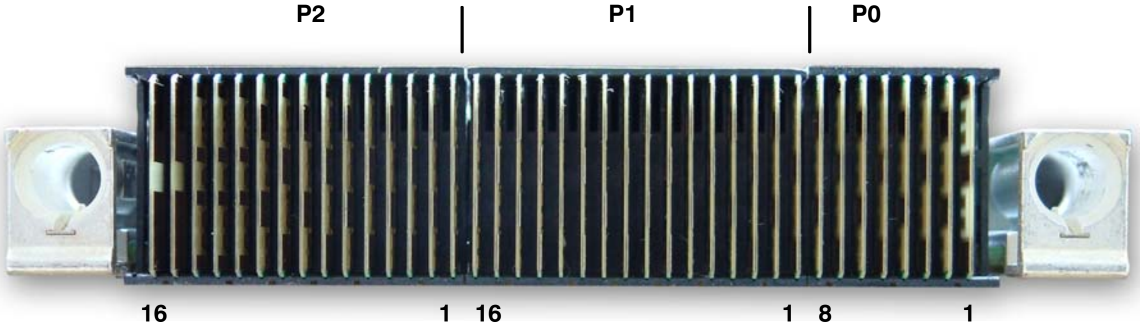


Figure 6: VPX Connectors

2.3.2 Board Connectors Identification

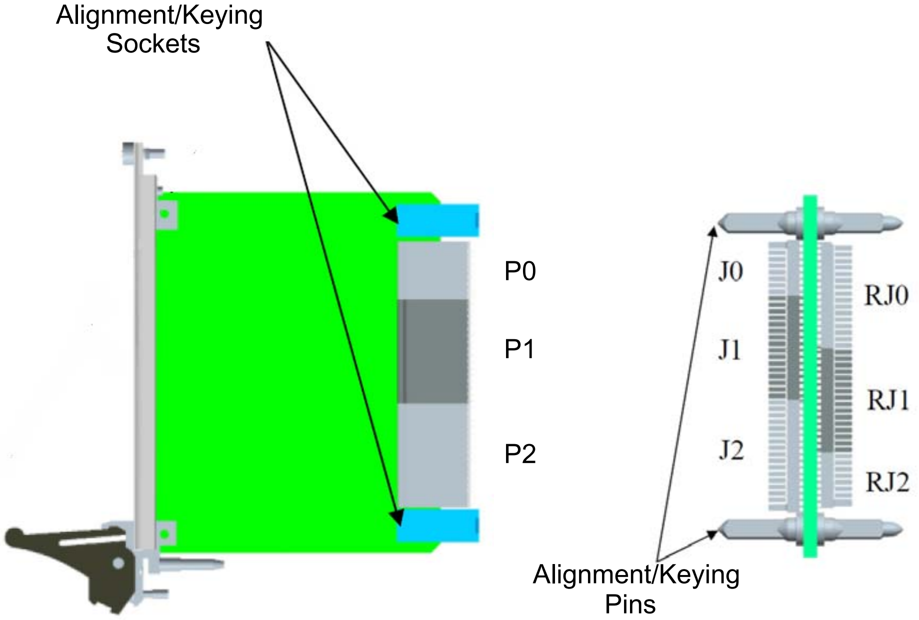


Figure 7: Connector Identification for 3U VPX Board

2.3.3 VPX Connectors Description

The VX3800 is provided with three VPX bus connectors, P0, P1 and P2

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	+12V	+12V	+12V	N.C.			
2	+12V	+12V	+12V	N.C.			
3	+5V	+5V	+5V	N.C.	+5V	+5V	+5V
4			GND	-12V_AUX	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3V3_AUX	GND		
6	GA3*	GA2*	GND		GND	GA1*	GA0*
7		GND	P0_CLK0-	P0_CLK0+	GND		
8	GND	REF_CLK-	REF_CLK+	GND	N.C. (RFU)	N.C. (RFU)	GND
CASE	GND						

* signal active when low

Table 10: VPX Connector P0 Wafer Assignment

» P0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
+12V	+12 Volts DC power
+/-12V_AUX	+/-12 Volts auxiliary DC power
+3V3_AUX	+3.3 Volts auxiliary DC power
+5V	+5 Volts DC power
GA0* to GA4*	Geographical Address Inputs 0-4
GAP	Geographical Address Parity
GND	Ground
N.C.	Not Connected
N.C. (RFU)	Not Connected (Reserved for Future Use)
P0_CLK+/-	Reference Clock, bussed differential pair. It enables the entire system to synchronize to a common clock if desired.
SMB*x*	System Management Bus *x*
SYSRESET*	System Reset

Table 11: VPX Connector P0 Signal Definition

» P1 Wafer Assignment

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A	
1	GPIO0	GND	PCIE0_TX-	PCIE0_TX +	GND	PCIE0_RX-	PCIE0_RX+	port 1Date Plane
2	GND	PCIE1_TX-	PCIE1_TX+	GND	PCIE1_RX-	PCIE1_RX+	GND	
3	N.C.	GND	PCIE2_TX-	PCIE2_TX+	GND	PCIE2_RX-	PCIE2_RX+	
4	GND	PCIE3_TX-	PCIE3_TX+	GND	PCIE3_RX-	PCIE3_RX+	GND	
5	SYS_CON*	GND	(PCIE0_TX)	(PCIE0_TX)	GND	(PCIE0_RX)	(PCIE0_RX)	Date Plane port 2
6	GND	(PCIE1_TX)	(PCIE1_TX)	GND	(PCIE1_RX)	(PCIE1_RX)	GND	
7	N.C.	GND	(PCIE2_TX)	(PCIE2_TX)	GND	(PCIE2_RX)	(PCIE2_RX)	
8	GND	(PCIE3_TX)	(PCIE3_TX)	GND	(PCIE3_RX)	(PCIE3_RX)	GND	
9	N.C.	GND	N.C.	N.C.	GND	N.C.	N.C.	Expan-sion Plane
10	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	
11	N.C.	GND	N.C.	N.C.	GND	N.C.	N.C.	
12	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	
13	GPIO1	GND	N.C.	N.C.	GND	N.C.	N.C.	User Defined
14	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	
15	MASKEABLE_RST#	GND	N.C.	N.C.	GND	N.C.	N.C.	Control Plane
16	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	
CASE	GND							

* signal active when low

Table 12: VPX Connector P1 Wafer Assignment

» P2 Wafer Assignment

> Build option with I/O of J4 routed to P2

Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A	
1		GND	J4-1	J4-3	GND	J4-2	14-4	*P64s*
2	GND	J4-5	J4-7	GND	J4-6	J4-8	GND	
3		GND	J4-9	J4-11	GND	J4-10	J4-12	
4	GND	J4-13	J4-15	GND	J4-14	J4-16	GND	
5		GND	J4-17	J4-19	GND	J4-18	J4-20	
6	GND	J4-21	J4-23	GND	J4-22	J4-24	GND	
7		GND	J4-25	J4-27	GND	J4-26	J4-28	
8	GND	J4-29	J4-31	GND	J4-30	J4-32	GND	
9		GND	J4-33	J4-35	GND	J4-34	J4-36	
10	GND	J4-37	J4-39	GND	J4-38	J4-40	GND	
11		GND	J4-41	J4-43	GND	J4-42	J4-44	
12	GND	J4-45	J4-47	GND	J4-46	J4-48	GND	
13		GND	J4-49	J4-51	GND	J4-50	J4-52	
14	GND	J4-53	J4-55	GND	J4-54	J4-56	GND	
15		GND	J4-57	J4-59	GND	J4-58	J4-60	
16	GND	J4-61	J4-63	GND	J4-62	J4-64	GND	

Table 13: VPX Connector P2 Wafer Assignment for PMC J4 IO

> Build option with I/O of J6 routed to P2

Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A	
1		GND	J6-C8	J6-C9	GND	J6-F8	J16-F9	X24s
2	GND	J6-C10	J6-C11	GND	J6-F10	J6-F11	GND	
3		GND	J6-C12	J6-C13	GND	J6-F12	J6-F13	
4	GND	J6-C14	J6-C15	GND	J6-F14	J6-F15	GND	
5		GND	J6-C16	J6-C17	GND	J6-F16	J6-F17	
6	GND	J6-C18	J6-C19	GND	J6-F18	J6-F19	GND	
7		GND	J6-A1	J6-B1	GND	J6-D1	J6-E1	X8d
8	GND	J6-A3	J6-B3	GND	J6-D3	J6-E3	GND	
9		GND	J6-A11	J6-B11	GND	J6-D11	J6-E11	
10	GND	J6-A13	J6-B13	GND	J6-D13	J6-E13	GND	
11		GND	J6-A5	J6-B5	GND	J6-D5	J6-E5	X12d
12	GND	J6-A7	J6-B7	GND	J6-D7	J6-E7	GND	
13		GND	J6-A9	J6-B9	GND	J6-D9	J6-E9	
14	GND	J6-A15	J6-B15	GND	J6-D15	J6-E15	GND	
15		GND	J6-A17	J6-B17	GND	J6-D17	J6-E17	
16	GND	J6-A19	J6-B19	GND	J6-D19	J6-E19	GND	

Table 14: VPX Connector P2 Wafer Assignment for XMC J6 IO

2.3.4 PMC Connectors

» PMC J1 Connector Pin Assignment

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	N.C.	17	REQ#	33	FRAME#	49	AD[09]
2	-12V	18	+5V	34	GND	50	+5V
3	GND	19	V(I/0) (1)	35	GND	51	GND
4	INTA#	20	AD[31]	36	IRDY#	52	C/BE0#
5	INTB#	21	AD[28]	37	DEVSEL#	53	AD[06]
6	INTC#	22	AD[27]	38	.+5V	54	AD[05]
7	BUSMODE1#	23	AD[25]	39	PCIXCAP	55	AD[04]
8	+5V	24	GND	40	LOCK#	56	GND
9	INTD#	25	GND	41	SDONE#	57	V(I/O) (1)
10	N.C.	26	C/BE3#	42	SBO#	58	AD[03]
11	GND	27	AD[22]	43	PAR	59	AD[02]
12	+3.3V_SUS	28	AD[21]	44	GND	60	AD[01]
13	CLK	29	AD[19]	45	V(I/O) (1)	61	AD[00]
14	GND	30	+5V	46	AD[15]	62	+5V
15	GND	31	V(I/0) (1)	47	AD[12]	63	GND
16	GNT#	32	AD[17]	48	AD[11]	64	REQ64#

(1) V(I/O) is 3.3V only. Neither PMC site provides a 3.3V keying pin

PCI signals active when low.

Table 15: PMC J1 Connector Pin Assignment

» PMC J2 Connector Pin Assignment

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	+12V	17	N.C.	33	GND	49	AD[08]
2	N.C.	18	GND	34	IDSEL B (1)	50	+3.3V
3	Pulled to +3.3V via 10K	19	AD[30]	35	TRDY#	51	AD[07]
4	Pulled to +3.3V via 10K	20	AD[29]	36	+3.3V	52	REQ B# (1)
5	Pulled to +3.3V via 10K	21	GND	37	GND	53	+3.3V
6	Ground	22	AD[26]	38	STOP#	54	GNT B# (1)
7	GND	23	AD[24]	39	PERR#	55	PMC-RSVD
8	N.C.	24	+3.3V	40	GND	56	GND
9	N.C.	25	IDSEL	41	+3.3V	57	PMC-RSVD
10	N.C.	26	AD[23]	42	SERR#	58	EREADY
11	Pulled to +3.3V via 2.7K	27	+3.3V	43	C/BE1#	59	GND
12	+3.3V	28	AD[20]	44	GND	60	N.C.
13	RST#	29	AD[18]	45	AD[14]	61	ACK64#
14	GND	30	GND	46	AD[13]	62	+3.3V
15	+3.3V	31	AD[16]	47	M66EN	63	GND
16	GND	32	C/BE2#	48	AD[10]	64	N.C.

(1) IDSEL B, REQ B# and GNT B# are provided for use by dual-function PMC modules or processor-PMC modules

PCI signals active when low.

Table 16: PMC J2 Connector Pin Assignment

PMC J4 Connector Pin Assignment

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	PMC IO 01	17	PMC IO 17	33	PMC IO 31	49	PMC IO 49
2	PMC IO 02	18	PMC IO 18	34	PMC IO 34	50	PMC IO 50
3	PMC IO 03	19	PMC IO 19	35	PMC IO 35	51	PMC IO 51
4	PMC IO 04	20	PMC IO 20	36	PMC IO 36	52	PMC IO 52
5	PMC IO 05	21	PMC IO 21	37	PMC IO 37	53	PMC IO 53
6	PMC IO 06	22	PMC IO 22	38	PMC IO 38	54	PMC IO 54
7	PMC IO 07	23	PMC IO 23	39	PMC IO 39	55	PMC IO 55
8	PMC IO 08	24	PMC IO 24	40	PMC IO 40	56	PMC IO 56
9	PMC IO 09	25	PMC IO 25	41	PMC IO 41	57	PMC IO 57
10	PMC IO 10	26	PMC IO 26	42	PMC IO 42	58	PMC IO 58
11	PMC IO 11	27	PMC IO 27	43	PMC IO 43	59	PMC IO 59
12	PMC IO 12	28	PMC IO 28	44	PMC IO 44	60	PMC IO 60
13	PMC IO 13	29	PMC IO 29	45	PMC IO 45	61	PMC IO 61
14	PMC IO 14	30	PMC IO 30	46	PMC IO 46	62	PMC IO 62
15	PMC IO 15	31	PMC IO 31	47	PMC IO 47	63	PMC IO 63
16	PMC IO 16	32	PMC IO 32	48	PMC IO 48	64	PMC IO 64

Table 17: PMC J4 Connector Pin Assignment

PMC Signal Description

MNEMONIC	SIGNAL DESCRIPTION
AD[00] to AD[31]	Address/Data bits. Multiplexed address and data bus.
ACK64#	Acknowledge 64-bit Transfer. Driven low by the device to indicate that the target is willing to transfer data using 64 bits.
BUSMODE1#	Bus Mode 1. Driven low by a PMC module to indicate that it supports the current bus mode
C/BE0# to C/BE1#	Command/Byte Enables. During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase the signals are byte enables that specify the active bytes on the bus.
CLK	Clock. Except RST*, the 64-bit PCI bus signals are synchronous to 33 or 66 MHz clock.
DEVSEL#	Device Select. Driven low by a PCI agent to signal that it has decoded its address as the target of the current access.
FRAME#	FRAME. Driven low by the current master to signal the start and duration of an access.
EREADY	EREADY. Output of non-monarch PPMCs that indicates it has completed its onboard initialization and can respond to PCI bus enumeration by the monarch via configuration cycles. Input to the monarch PPMC that indicates all non-monarch PPMCs have completed their onboard initialization and can respond to PCI bus enumeration by the monarch via configuration cycles.
GNT#	Grant. Driven low by the arbiter to grant PCI bus ownership to a PCI agent. GNT B# is provided for use by dual-function PMC modules or processor-PMC modules.
IDSEL	Initialization Device Select. Device chip select during configuration cycles. IDSEL B is provided for use by dual-function PMC modules or processor-PMC modules.
INTA# to INTD#	Interrupt lines. Level-sensitive, active-low interrupt requests.
IRDY#	Initiator Ready. Driven low by the initiator to signal its ability to complete the current data phase.
	Page 1 of 2

MNEMONIC	SIGNAL DESCRIPTION
LOCK#	LOCK. Driven low to indicate an atomic operation that may require multiple transactions to complete.
M66EN	66 MHZ Enable. Indicates to a device if the bus segment is operating at 66 or 33 MHz. If it is high then the bus speed is 66 MHz and if it is low then the bus speed is 33 MHz.
N.C.	This pin is not connected.
PAR	Parity. Parity protection bit for AD0 to AD31 and C/BE0# to C/BE3#.
PERR#	Parity Error. Driven low by a PCI agent to signal a parity error.
PMC IO 01 to PMC IO 64	64-bit PCI bus PMC 64 signals. Used to transmit I/O signals from PCI 64 PMC connector (J4) to P2 connector.
PMC-RSVD	Reserved. Do not connect this pin.
REQ#	Request. Driven low by a PCI agent to request ownership of the PCI bus. REQ B# is provided for use by dual-function PMC modules or processor-PMC modules.
REQ64#	Request 64-bit Transfer. Driven low by the current bus master, indicates that it desires to transfer data using 64 bits.
RST#	Reset. Driven low to reset the PCI bus.
SBO#	Snoop Backoff. Indicates a hit of a modified line asserted.
SDONE#	Snoop Done. Indicates the status of the snoop for the current access.
SERR#	System Error. Driven low by a PCI agent to signal a system error.
STOP#	STOP. Driven low by a PCI target to signal a disconnect or target-abort.
TRDY#	Target Ready. Driven low by the current target to signal its ability to complete the current data phase.
V(I/O)	Power supply delivered by the board. On the PCI 64 PMC slots, +3.3 Volts power is supplied. +5 Volts signaling PMCs are not supported. Contact Kontron for more information.
+3.3V	+3.3 Volts DC power
+5V	+5 Volts DC power
+12V	+12 Volts DC power
-12V	-12 Volts DC power
	Page 2 of 2

Table 18: PMC Signal Description

2.3.5 XMC Connectors

XMC J5 Pin Assignment

One XMC site is provided to allow the installation of VITA 42.3, PCI-Express mezzanine cards. The signals assignments are as shown in the following table.

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR (1)
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR (1)
4	GND	GND	TCK	GND	GND	MRSTO#
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR (1)
6	GND	GND	TMS	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR (1)
8	GND	GND	TDI	GND	GND	-12V
9	RFU	RFU	N.C.	RFU	RFU	VPWR (1)
10	GND	GND	TDO	GND	GND	GA0
11	PER0p0	PER0n0	N.C.	PER0p1	PER0n1	VPWR (1)
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PER0p2	PER0n2	3.3V AUX	PER0p3	PER0n3	VPWR (1)
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	N.C.	PER0p5	PER0n5	VPWR (1)
16	GND	GND	NVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	N.C.	PER0p7	PER0n7	N.C.
18	GND	GND	N.C.	GND	GND	N.C.
19	REFCLK+0	REFCLK-0	N.C.	XMC_WAKE#	XMC_ROOT#	N.C.

(1) VPWR is connected to +5V via a 0 ohm resistor.
The +12V option is available, please contact Kontron for more information on this topic.

Signals active when low.

Table 19: XMC J5 Connector Pin Assignment

XMC J6 Pin Assignment

XMC J6 socket connector is assembled onto the VX3800 but not connected in the boards compliant to the “PMC J4 I/O routed to P2” manufacturing option.

Routing of the I/O J6 to VPX P2 connector is a build option and is defined in Table 14 page 17.

XMC Signal Description

MNEMONIC	SIGNAL DESCRIPTION
GA[0..2]	GA=0
GND	Ground
MPRESENT	Unused
MRSTI#	XMC Reset In. When this signal is asserted low by the carrier, the mezzanine card shall initialize itself into a known state.
MRSTO#	XMC Reset Out. As input to the carrier, this optional signal provides an input to the carrier's reset logic in order to support a reset button or other reset source on the XMC.
MSCL, MSDA	IPMI I2C signals: not connected
NVMRO	XMC Write Prohibit. When this signal is asserted high, the XMC shall disable writes to non-volatile memory on the XMC.
N.C.	Not Connected. Do not Used
PET0p/n[0..7]	PCI-Express Differential Transmit. Depending on link width, signals 0 or [0..4] are used
PER0p/n[0..7]	PCI-Express Differential Receive. Depending on link width, signals 0 or [0..4] are used.
RFU	Reserved for Future Use
TCK,TDI,TDO,TMS,TRST	JTAG signals, not connected
VPWR	Power pins. These are 5V.

Table 20: XMC Signal Description

2.4 XMC/PMC Site

The VX3800 provides one XMC/PMC site.

The XMC/PMC Site can alternately be used as a PCIbus 32/66 or as an XMC site with either a x4 or a x1 PCI-Express link to the VPX backplane.

A XMC card installed in this location uses its P5 (J5 on the VX3800) for the Express Link. The installed XMC should provide either front panel I/O or utilize a P4 (J4 on the VX3800) for I/O.

The following table sums up all information concerning the PCI 32 XMC/PMC Site. It gives information needed for software and hardware configuration.

For EMC protection reasons, when not used, the PMC slots are fitted with a blanking plate.

Electrostatic Discharge (ESD) can damage components. To avoid ESD damage, the board should be kept in its protective antistatic packaging until it is ready to be installed. During installation make sure to wear an antistatic wrist strap to discharge static electricity.

FUNCTION	VALUE	DESCRIPTION
PMC Connectors	J1	Connects the signals for the 32-bit PCI bus.
	J2	Connects the signals for the 32-bit PCI bus.
	J4	Connects the User Defines I/O signals.
XMC Connector	J5	Connects the signals for the switched communications.
V(I/O) Voltage Level	+3.3V	The signaling voltage of the 32-bit PCI bus is +3.3V, 5V tolerant. The VIO is set at 3.3V. A VIO set at 5V is available on demand.
PCI Bus Mode	32 Bits	The 32-bit PCI bus is in 32-bit mode.
PCI Bus Rate	33/66 MHz	Can be set at 33 MHz using switch SW2
PCI Interrupts	INTA INTB INTC INTD	Connected to the Interrupt Controller.
REQ/GNT **IDSEL**	0 AD[18]	For single function PMC's

Table 21: PCI 32 XMC/PMC Site Information

2.4.1 Signaling Voltage Keying Pin (3V VIO)

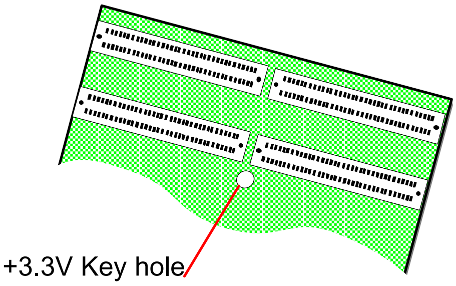
The 32-bit PCI bus of the VX3800 and the PMC plugged on the 32-bit PCI slot have to operate on the same signaling level. The VX3800 sets the signaling level for the 32-bit PCI bus to +3.3V (i.e. V(I/O)=+3.3V). The V(I/O) pins of the PCI 32 PMC are connected to +3.3V.

The distinction between PMC types is the signaling level they use, not the power rails they connect to, nor the component technology they contain.

On the VX3800 PCI 32 XMC/PMC slot, only two XMC/PMC types must be intalled:

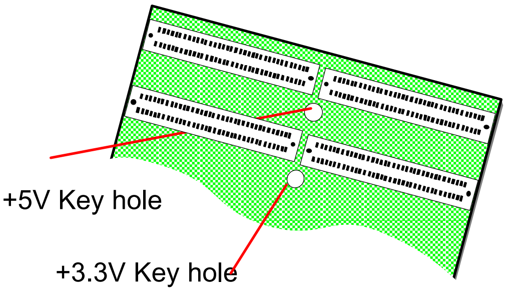
» +3.3V PMC

It is designed to work only in a +3.3V signaling level and will only have a keying hole.

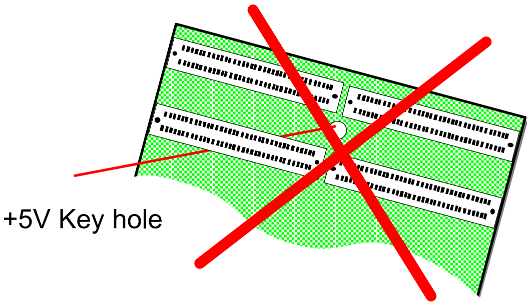


» Universal PMC

It supports both voltages (+5V and +3.3V). This PMC is capable of detecting the signaling level in use and adapting itself to that environment. It has two keying holes (+5V and +3.3.V) and can, therefore, be plugged into either signaling level.



⚠ As no PMC voltage selection key is provided on the board, make sure not to insert a +5V PMC on the board. Failture to observe this restriction may result in damage to the PMC or the VX3800.



2.4.2 Signaling Voltage Keying Pin (5V VIO build option)

When the VIO is set at 5V, both 5V PMC and Universal PMC can be hosted. 3.3V PMC are not supported.

Chapter 3 - Installation

The VX3800 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

3.1 Safety Requirements

The following safety precautions must be observed when installing or operating the VX3800. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.
In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

This board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

3.2 Board Identification

The VX3800 boards are identified by labels fitted to the top and bottom sides.

» Top Side

A "Order Code" label.

B "Serial Number" label.

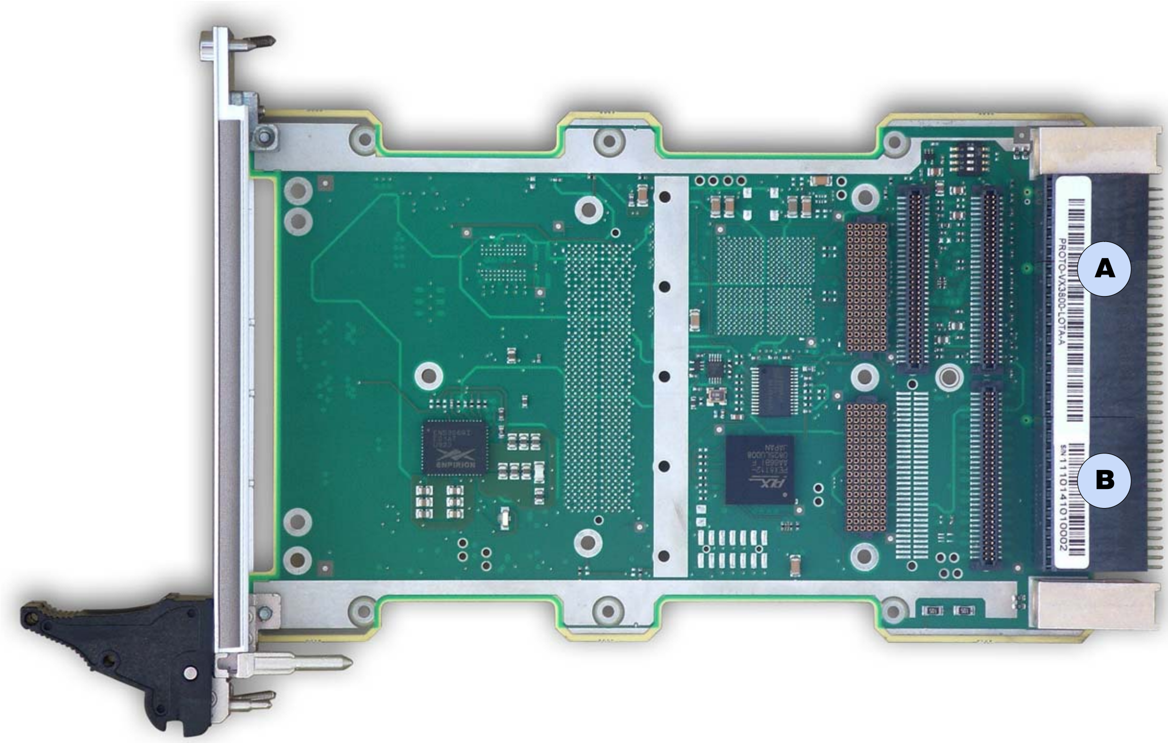


Figure 8: VX3800 Identification (Top Side)

» Bottom Side

C "Functional Identification" label (Variant + E.C. Level)

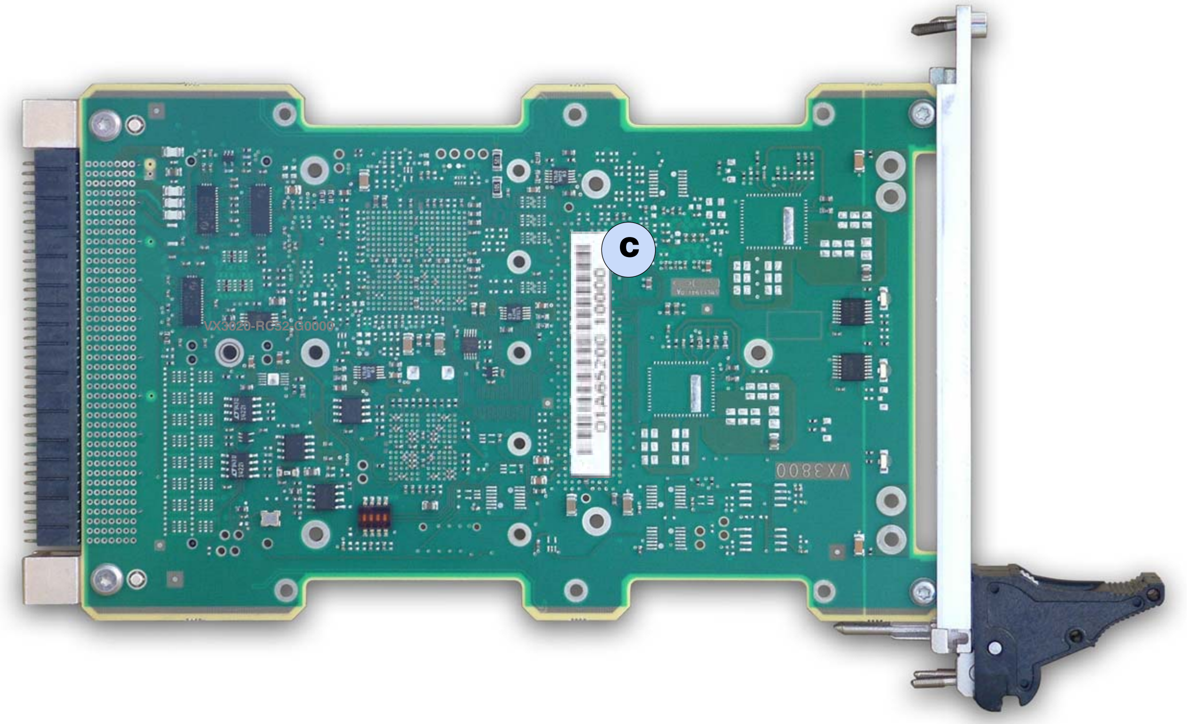


Figure 9: VX3800 Identification (Bottom Side)

3.3 Board Configuration

3.3.1 DIP Switch SW1 Description

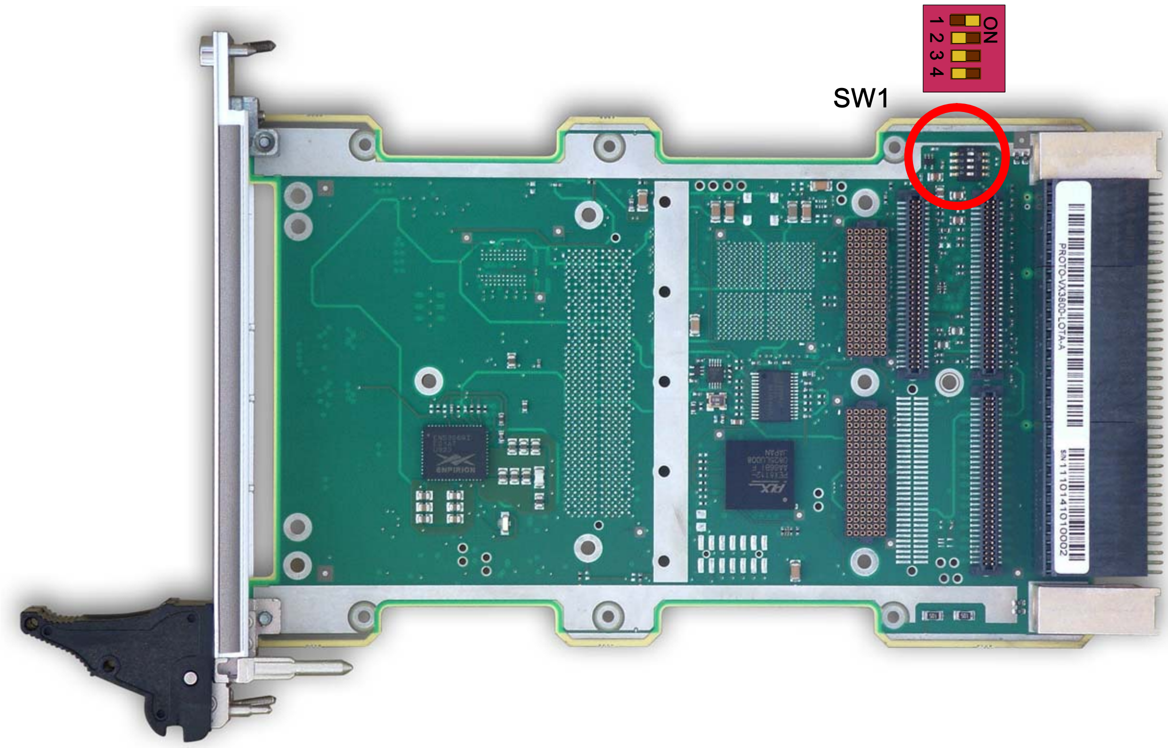


Figure 10: Location of SW1 DIP Switch

Number	OFF function	ON function	Default
1	XMC Carrier (PCI-E on XMC site)	PMC Carrier (PCI-E on PCI bridge)	ON
2	PCI-Express 1x link	PCI-Express 4x link (1)	OFF
3	On Board 100Mhz PCI-E Clock	Backplane common 100Mhz clock	OFF
4	Maskeable reset from the VPX backplane is inactive	Maskeable reset from the VPX backplane is active	OFF

Note: (1) If the Backplane is compatible with 4x link PCI-E

Table 22: Description of SW1 DIP Switch

3.3.2 DIP Switch SW2 Description

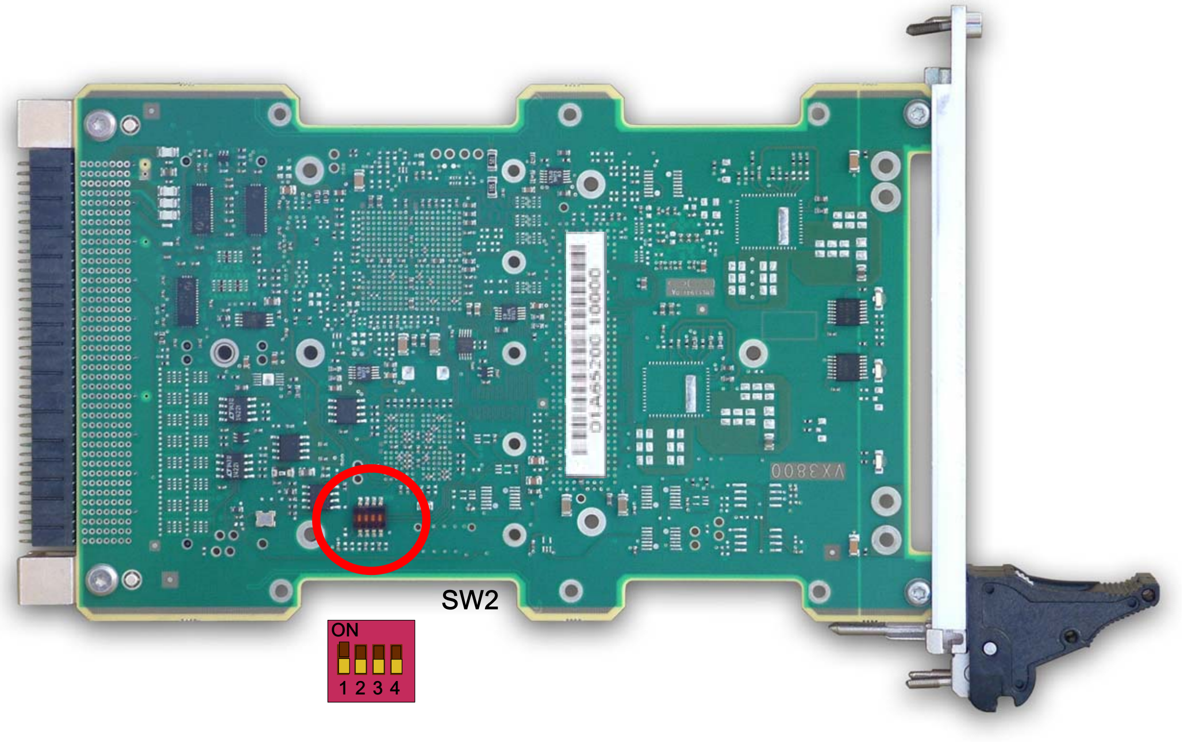


Figure 11: Location of SW2 DIP Switch

Number	OFF function	ON function	Default
1 unused			OFF
2 unused			OFF
3	PCI frequency is either 66 MHz or 33 MHz depending on M66EN level on the PMC board	Force PCI frequency at 33 MHz	OFF
4 unused			OFF

Table 23: Description of SW2 DIP Switch

3.4 PMC Installation

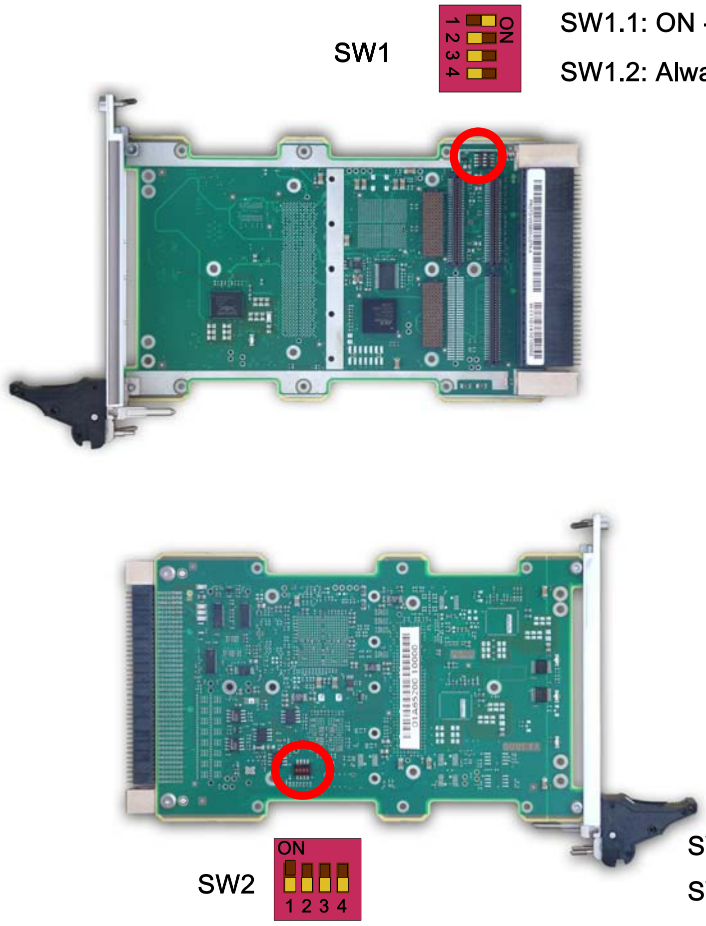
PMC modules are delivered with a full kit of parts for mounting them, and the user guide for the module normally contains instructions on how to fit the module.

The installation of the PMC on the VX3800 conforms to the IEEE P1386.1 standard.

To install the XMC/PMC module, refer to Figure 13 page 32 and follow the steps below:

To avoid ESD damage, wear an antistatic wrist strap to discharge static electricity while performing any part of the installation that involves touching the VX3800 board or the XMC/PMC.
If you can't wear an antistatic wrist strap, touch one hand to the bare metal surface to provide grounding.

1. Place carefully the VX3800 with the backplane connectors facing you on a static dissipative surface connected to a common ground by a low-resistance connection. Do not slide the board over any surface.
2. Check the configuration of the SW1 and SW2 DIP switches.



SW1.1: ON - PMC Carrier

SW1.2: Always OFF as the PLX 8112 is 1x

SW2.3: ON - Force PCI frequency at 33 MHz

SW2.3: OFF - PCI frequency is either 66 or 33 MHz depending on M66EN on the PMC board

Figure 12: DIP Switches Configuration in PMC Mode

3. Remove the blanking plate from the appropriate XMC/PMC slot of the VX3800.
4. Check that the standoffs are attached to the XMC/PMC.

5. Install the XMC/PMC, component-side down, aligning the PCI connectors with their mating connectors on the VX3800 and the XMC connector if available. Press them together so that the friction from the pins holds them together. Insert the standoff plug mounted on the VX3800 into the keyhole. The module's bezel will fill the slot and provide a connection to the module.
6. Screw the XMC/PMC in place using the 4 mounting points, on the bottom side of the VX3800 . You need a Phillips screwdriver for this stage.
7. The XMC/PMC attachment is now complete.
8. Insert the VX3800 into the chassis making sure it is plugged into the backplane.

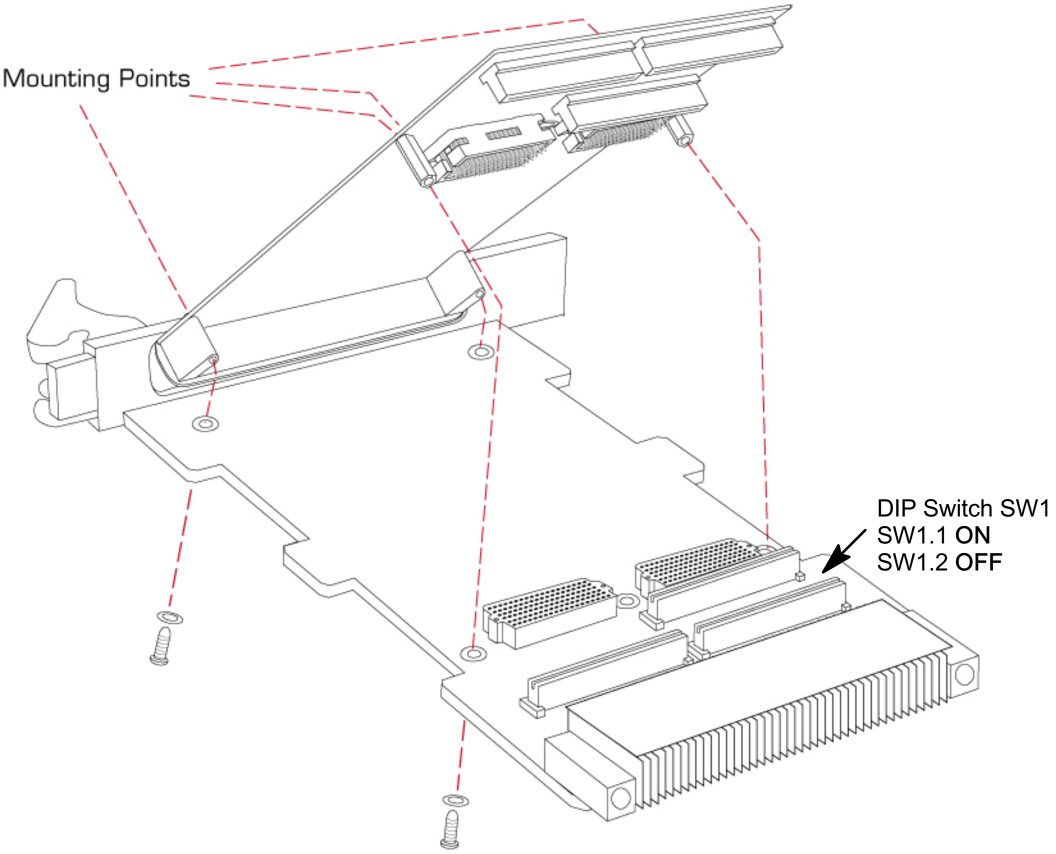


Figure 13: PMC Installation on PMC Site

3.5 XMC Installation

The XMC board standard is based on the PMC mechanical definition, and occupies the same board area.

The XMC board adds one new connector to the connectors already on a PMC. The new connector supports high-speed differential signals for fabric communications.

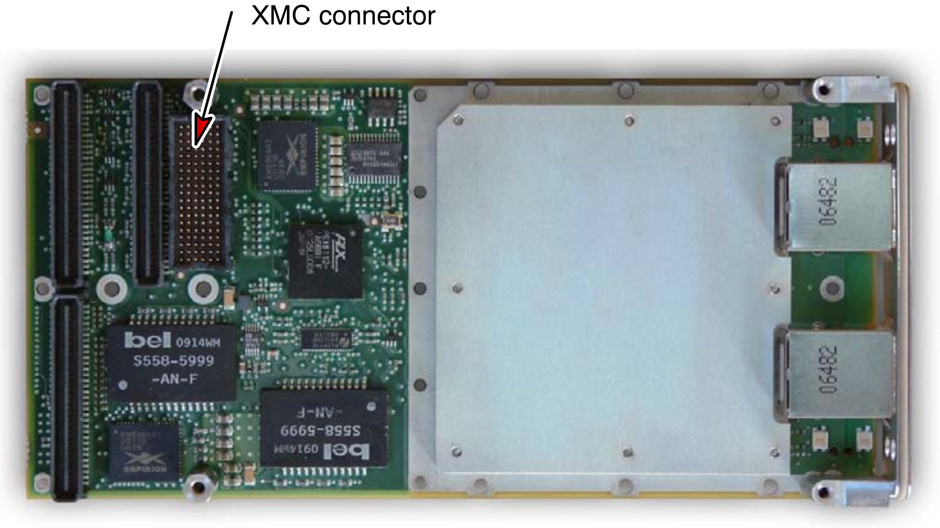
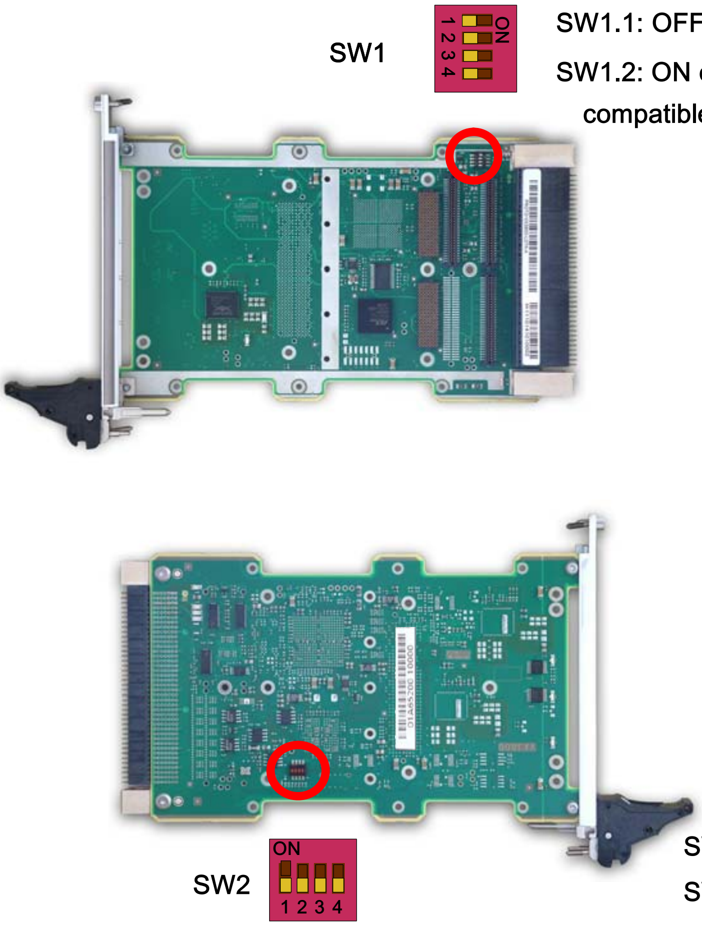


Figure 14: Example of XMC Board

Check the configuration of the SW1 and SW2 DIP switches



SW1.1: OFF - XMC Carrier

SW1.2: ON or OFF depending on the backplane compatible with 4x link PCi-E or 1x link PCI-E

SW2.3: ON - Force PCI frequency at 33 MHz

SW2.3: OFF - PCI frequency is either 66 or 33 MHz depending on M66EN on the PMC board

Figure 15: DIP Switches Configuration in XMC Mode

Figure 16 shows a XMC installation on the PMC/XMC Site.

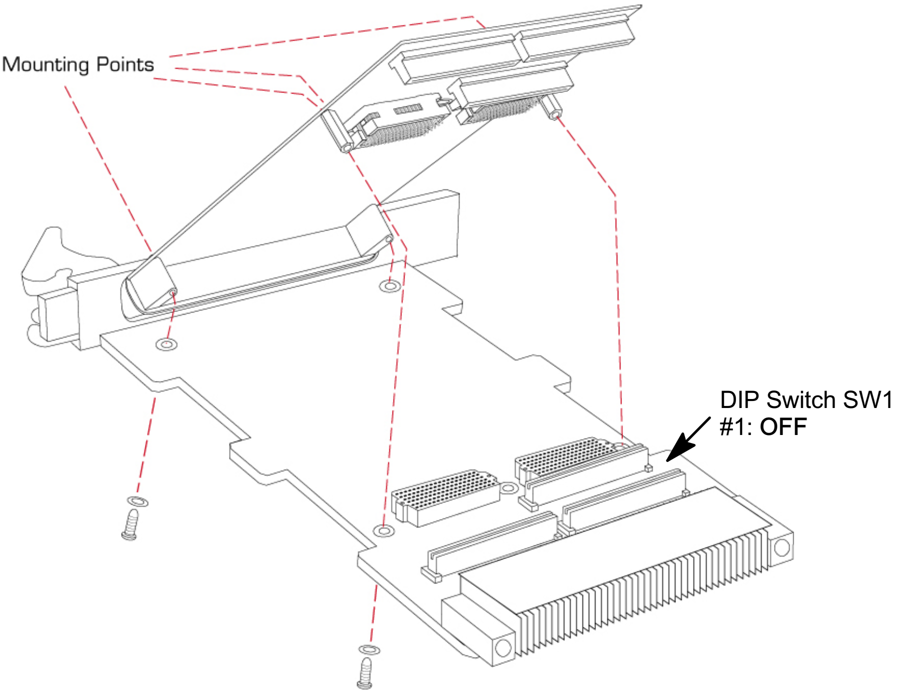


Figure 16: XMC Installation on XMC Site

Chapter 4 - Power Consideration

4.1 System Power

The considerations presented in the ensuing chapters must be taken into account by system integrators when specifying the VX3800 system environment.

4.1.1 VX3800

The VX3800 has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

The following table specifies the ranges for the different input power voltages within which the board is functional.

The VX3800 is not guaranteed to function if the board is not operated within the prescribed limits.

Input supply voltage	Absolute Range
+3.3V	Not used on VX3800
+5V	4.85V min to 5.25V max
+12V	11.4V min to 12,6V max
-12V	-11.4V max to -12,6V min

Table 24: DC Operational Input Voltage Ranges

4.1.2 Backplane

Backplanes to be used with the VX3800 must be adequately specified. The backplane must provide optimal power distribution for the +5 V, -12V and +12 V power inputs. Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided.

4.1.3 Power Supply Units

Power supplies for the VX3800 must be specified with enough reserve for the remaining system consumption.

In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires. As the design of the VX3800 has been optimized for minimal power consumption, the power supply unit shall be stable even without minimum load. Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for die resistance variations. Non-industrial ATX PSUs may require a greater minimum load than a single VX3800 is capable of creating. When a PSU of this type is used, it will not power up correctly and the VX3800 may hangup. The solution is to use an industrial PSU or to add more load to the system. The start-up behavior of VPX power supplies is critical for all new CPU boards. These boards require a defined power of sequence and start-up behavior of the power supply. For information on the required behavior refer to the power supply specifications on the formfactors.org website and to the VPX specification on the VITA web site (http://www.vita.com)

4.1.3.1 Tolerance

The tolerance of the voltage lines is described in the VITA specification (VITA 46.0).The recommended measurement point for the voltage is the VPX connector on the CPU board. The following table provides information regarding the required characteristics for each board input voltage.

Backplane Voltage	Nominal Value Tolerance	Max. Ripple	(P-P)	Notes
+5V	+5V DC	+5% / -2.5%	50 mV	Main voltage
+3V3	Not used			
+12V	+12 VDC	+5% / -5%	50 mV	Required for PMC/-XMC slot
-12V	-12 VDC	+5% / -5%	50 mV	Required for PMC/-XMC slot
GND	Ground, not directly connected to potential earth (PE)			

Table 25: Input Voltage Characteristics

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

4.2 Power Consumption

The goal of this description is to provide a method to calculate the power consumption for the VX3800 and for additional configurations. The processor dissipates the majority of the thermal power. The power consumption tables below list the voltage and power specifications for the VX3800 board. The values were measured using an 5-slot passive VPX backplane. The operating system used was Linux Fedora 9. All measurements were conducted at a temperature of 25°C. The measured values varied, because the power consumption was dependent on processor activity.

4.2.1 Real Applications

The following tables indicate the power consumption, using real applications. The Power Consumption was measured under:

- Linux IDLE Mode(*)
- Linux under PMC test(**)
- Linux under XMC test(***)

POWER	VX3800 in Idle mode (*)	VX3800 under PMC test(**)	VX3800 under XMC test(***)
+5V	2.1W	6.3W	5.3W
+12V	0 (not used)	0 (not used)	0 (not used)
+12V	0 (not used)	0 (not used)	0 (not used)
TOTAL	2.1W	6.3W	5.3W

(*) No PMC/XMC board plugged on the VX3800, no tests are running.

(**) An Ethernet PMC is plugged on the VX3800. A simple test is running to move files over the network

(***) An Ethernet XMC is plugged on the VX3800. A simple test is running to move files over the network

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