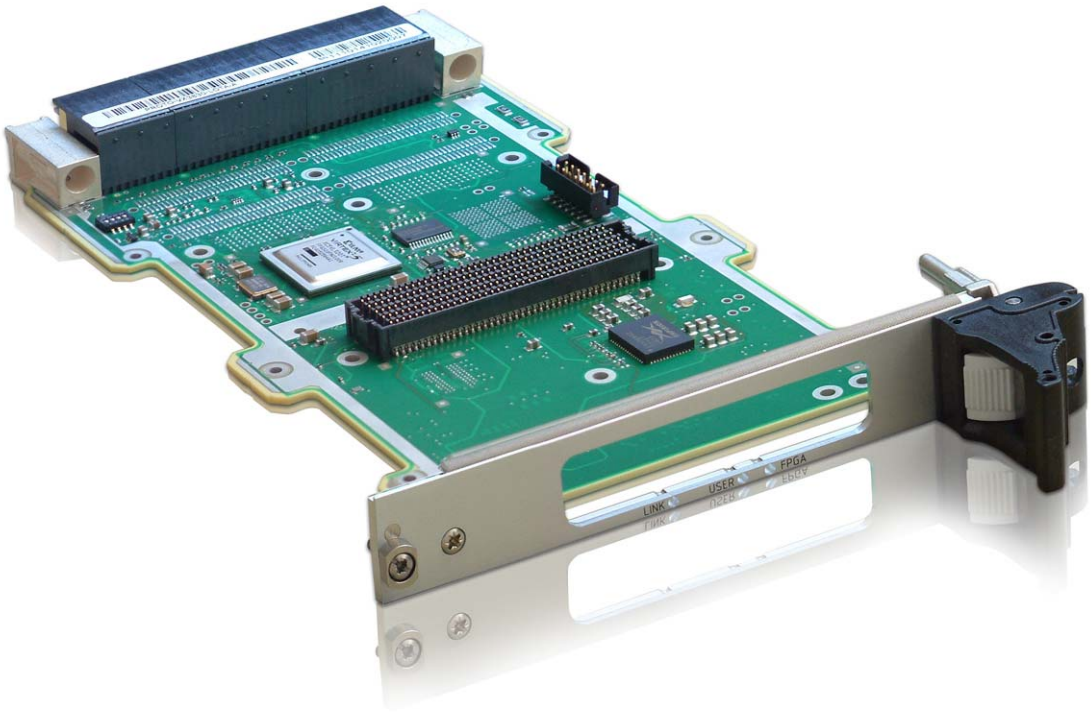
» VX3830 «



3U VPX Xilinx® Virtex®-5 FPGA Processor with FMC Site - User's Guide

CA.DT.A80-4e - January 2012

Revision History

Publication Title:	VX3830 User's Guide
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Rev.	Brief Description of Changes	Date of Issue
4e	Update P0 and P1 Wafer Assignment	01-2012
3e	Chapter 5 added & modif. order code	04-2011
2e	New section 2.3.5 “JTAG/SPI Connector” Error in section 5.2 “Power Consumption”	12-2010
1e	Initial Version	12-2010
0e	Preliminary Version	10-2010

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Environmental protection is a high priority with Kontron.

Kontron follows the DEEE/WEEE directive.

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The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- reduce waste arising from electrical and electronic equipment (EEE)
- make producers of EEE responsible for the environmental impact of their products, especially when they become waste
- encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- improve the environmental performance of all those involved during the lifecycle of EEE

Conventions

This guide uses several types of notice: Note, Caution, ESD.

Note: this notice calls attention to important features or instructions.


Caution: this notice alert you to system damage, loss of data, or risk of personal injury.


ESD: This banner indicates an Electrostatic Sensitive Device.

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix `0x' shows a hexadecimal number, following the `C' programming language convention.

The multipliers `k', `M' and `G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when `K', `M' and `G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

When describing transfer rates, `k' `M' and `G' mean $*10^3$, $*10^6$ and $*10^9$ *not $*2^{10}$ $*2^{20}$ and $*2^{30}$.*

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and CompactPCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Signal names ending with an asterisk (*) or a hash (#) denote active low signals; all other signals are active high.

Signal names follow the PICMG 2.0 R3.0 CompactPCI Specification and the PCI Local Bus 2.3 Specification.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions


Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.


Caution, Electric Shock!
Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Chapter 1 - Introduction

The VX3830 is a member of the Kontron's VITA 46 VPX range of products. The VX3830 is designed to operate in a 3U VPX peripheral slot and provides the resources of a Xilinx® Virtex®-5 FPGA and VITA57 FPGA Mezzanine Card (FMC) slot for designing versatile I/O interface.

In this document, the term:

- VX3830 will be associated to the 3U VPX board
  - VX3830-SA will be associated to the standard commercial version of the board.
  - VX3830-RC will be associated to the rugged conduction-cooled version of the board.
- VX3830-RTM will be associated to the 3U VPX Rear Transition Module (RTM).

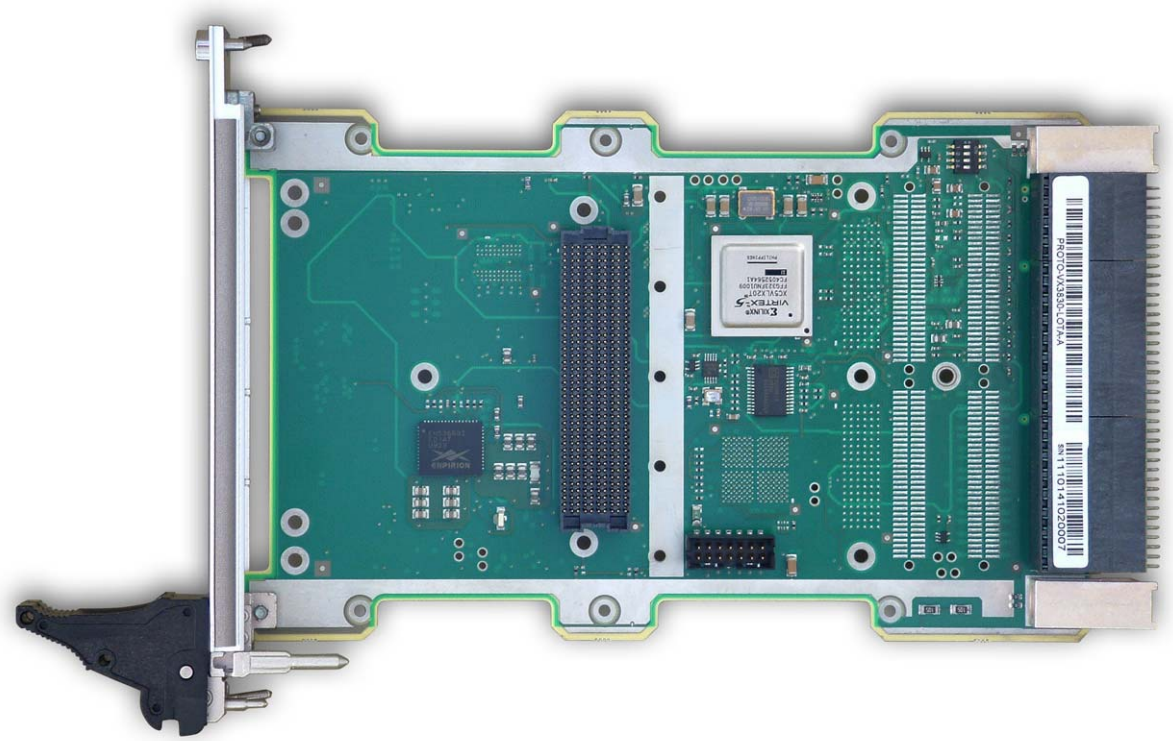


Figure 1: VX3830-SA Overview

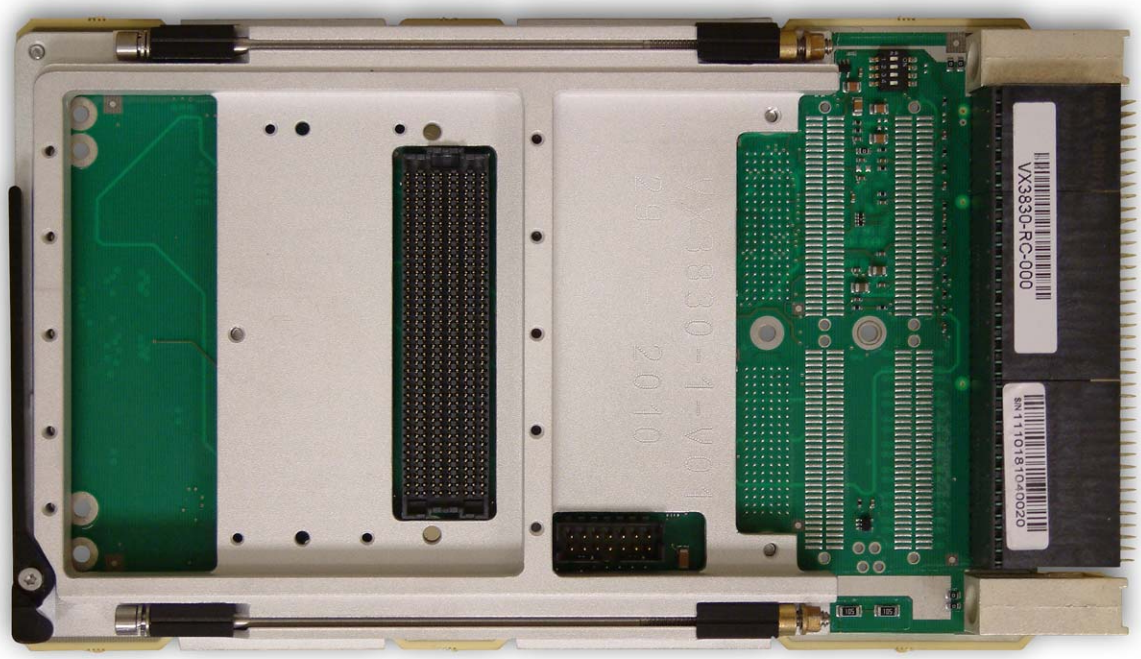


Figure 2: VX3830-RC Overview

1.1 Manual Overview

1.1.1 Objectives

This guide provides general information, hardware preparation and installation instructions, operating instructions and a functional description of the VX3830 board. The onboard programming, onboard firmware and other software (e.g. drivers and BSPs) are described in detail in separate guides (see section 1.8 “Related Publications").

As the standard policy for all the Kontron, hardware technical documentation reflects the most recent version of our products. The “Hardware Release Notes" (see section 1.8 “Related Publications") is to help to keep track of various evolutions that have happened during the early steps of the VX3830 ramp-up or later in its lifetime.

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

1.1.2 Audience

This guide is written to cover, as far as possible, the range of people who will handle or use the VX3830, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, systems, cabling, grounding and communications.

1.1.3 Scope

This guide describes all variants of the VX3830 series. It does not cover any FMC modules which are described in specific guides (see section 1.8 “Related Publications").

1.1.4 Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with a brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- Chapter 1 - Introduction (this chapter)
- Chapter 2 - Functional Description
- Chapter 3 - Installation
- Chapter 4 - Flash Programming
- Chapter 5 - Power Considerations

1.2 VPX Overview

VPX (VITA 46) specifications establish a new direction for the next revolution in bus boards. VPX is a proposed ANSI standard which breaks out from the traditional connector scheme of VMEbus to merge the latest in connector and packaging technology with the latest in bus and serial fabric technology. VPX combines best-in-class technologies to assure a very long technology cycle similar to that of the original VMEbus solutions.

Traditional parallel VMEbus will continue to be supported by VPX through bridging schemes that assure a solid migration pathway.

For further information regarding this standards and its use, visit the home page of the VITA - Open Standards,Open Markets.

1.3 Board Overview

1.3.1 Main Features

The VX3830 is a 3U VPX FMC carrier board based on a Xilinx® Virtex®-5 FPGA.

» VPX Interface

The VX3830 can be configured to support either a x4-lane and a x1-lane PCI-express link on VPX standard P1 wafers 1 to 4 (Data plane 1)

As a manufacturing build option, the VX3830 can be interfaced to the VPX Data Plane 2 (P1 wafers 5 to 8).

» FMC Interface

The VITA57 FMC standard provides an industry standard mezzanine form factor in support of a flexible, modular I/O interface to an FPGA located on a baseboard or carrier card, the VX3830. It allows the physical I/O interface to be physically separated from the FPGA design while maintaining a close coupling between a physical I/O interface and an FPGA through a single connector.

FMC modules are about half the size of PMC or XMC modules (similar width), but provide higher density host I/O.

Key FMC features include:

- Sole high performance connector between carrier and FMC
- Two mechanically compatible types of connectors:
  - 160-pin Low Pin Count (LPC): 40-column 4-row (C,D,G,H)
  - 400-pin High Pin Count (HPC): 40-column 10-row (A to K)
- Flexible interconnect between carrier and FMC:
  - Parallel I/O, single-ended or differential pairs (34 for LPC, 80 for HPC)
  - Up to 10 Multi-Gigabit Transceiver (MGT) (1 for LPC, 10 for HPC)
- Air and conduction-cooled variants
- Module size 69 x 76.5mm

The 34 differential pairs supported by the LPC (rows C,D,G,H) are named LAx_p/n [x=0,33]

The 80 differential pairs supported by the HPC are named:

- LAx_P/N [x=0,33]
- HAx_P/N [x=0,23]
- HBx_P/N [x=0,21]

The VITA 57 identifies by the "_CC" postfix, the signals which should be used as the preferred signals for clocks in source synchronous applications and which are connected to pins on the FPGA which are identified for this purpose.

Exemple: LA01_P_CC and LA01_N_CC

The VX3830 is equipped with a 400-pin High Pin Count (HPC) FMC connector where the I/O signals:

- LAx_p/n [x=0,33] are routed from/to the FPGA
- HAx_p/n [x=14,23] are routed from/to the VPX P2 connector
- HBx_p/n [x=0,21] are routed from/to the VPX P2 connector

FPGA

The VX3830 features a Xilinx® Virtex®-5 Speed grade -1 (industrial grade) FPGA reference: XC5VLX20T-2FFG323I

Device	Configurable Logic Blocks (CLBs)			DSP 48E	Block RAM Blocks			CMTs (4)	PowerPC Processor Blocks	Endpoint blocks for PCI Express	Ethernet MACs (5)	Max Rockett Transceivers (6)		Total I/O Banks (8)	Max User I/O (7)
	Array (Row x Col)	Virtex-5 Slices (1)	Max Distributed RAM (Kb)	Slices (2)	18 Kb (3)	36 Kb	Max (Kb)					GTP	GTX		
XC5VLX20T	60 x 26	3,120	210	24	52	26	936	1	N/A	1	2	4	N/A	7	172

Table 1: VX3830 FPGA resources table (Source Xilinx®)

The VX3830 interfaces the PCI-Express links to the hardened PCI-Express blocs of the Xilinx® Virtex®-5 FPGA in order to minimize design risks and avoid any host dependent minimal FPGA configuration constraint.

Maximum junction temperature: **+125°C**

Software

The VX3830 does not host any CPU on board and interfaces the PCI-Express bus. It does not require any specific BSP nor Device Driver for use in a system.

Harsh Environments

The VX3830 has been designed using the same PCB for both air and conduction-cooled boards. Builds variants span a complete range of temperature, shock and vibration requirements as specified in the VITA 47 standards.

Rear Transition Module

The VX3830 supports the VX3830-RTM, a 3U VPX rear Transition Module compliant to Rear Transition Module on VPX standard - VITA 46.10.

1.3.2 Order Code Table

The VX3830 supports the VX3830-RTM, a 3U VPX rear Transition Module compliant to Rear Transition Module on VPX standard - VITA 46.10.

Preferred / Fast Track variant, Air Cooled: VX3830-SA-00000

Preferred / Fast Track variant, Conduction Cooled: VX3830-RC-0N000

> VPX Data Plane Selection : DP1 or DP2 : see chapter 1.4.1 page 7

DESCRIPTION	Code	VX3830- SA - 0 0 0 0 0
Environment Class : Standard (Air)	SA	
Rugged Conduction Cooled	RC	
Reserved	0	
Front Panel Front Panel (0.8 inch) (SA only)	0	
Front Panel (1 inch) (SA only)	1	
No Front Panel	N	
Data Plane Selection VPX DP1 Data Plane Interface	0	
VPX DP2 Data Plane Interface	1	
Reserved	0	
Reserved	0	
Coating (SA only)	V	Add V suffix only when not default

Table 2: Order Code Table

Manufacturing Build Options

> VPX Interface

- **VPX DP1 Data Plane interface (P1 wafers 1 - 4) . Default**
- VPX DP2 Data Plane interface (P1 wafers 5 - 8)

1.3.3 I/O Interfaces

Front Interfaces

FUNCTION	DESCRIPTION
FMC	FMC slot
LEDs	3 LEDS reporting main interfaces activities

Table 3: Front I/O Interfaces

Rear Interfaces

FUNCTION	DESCRIPTION
VPX	VPX standard on P0/P1/P2
FMC I/Os	64 bits of I/Os of the FMC, on P2
Reset	Main reset input available on P0 connector

Table 4: Rear I/O Interfaces

1.4 Board Diagram

The following diagrams provide additional information concerning board functionality and component layout.

1.4.1 Functional Block Diagram

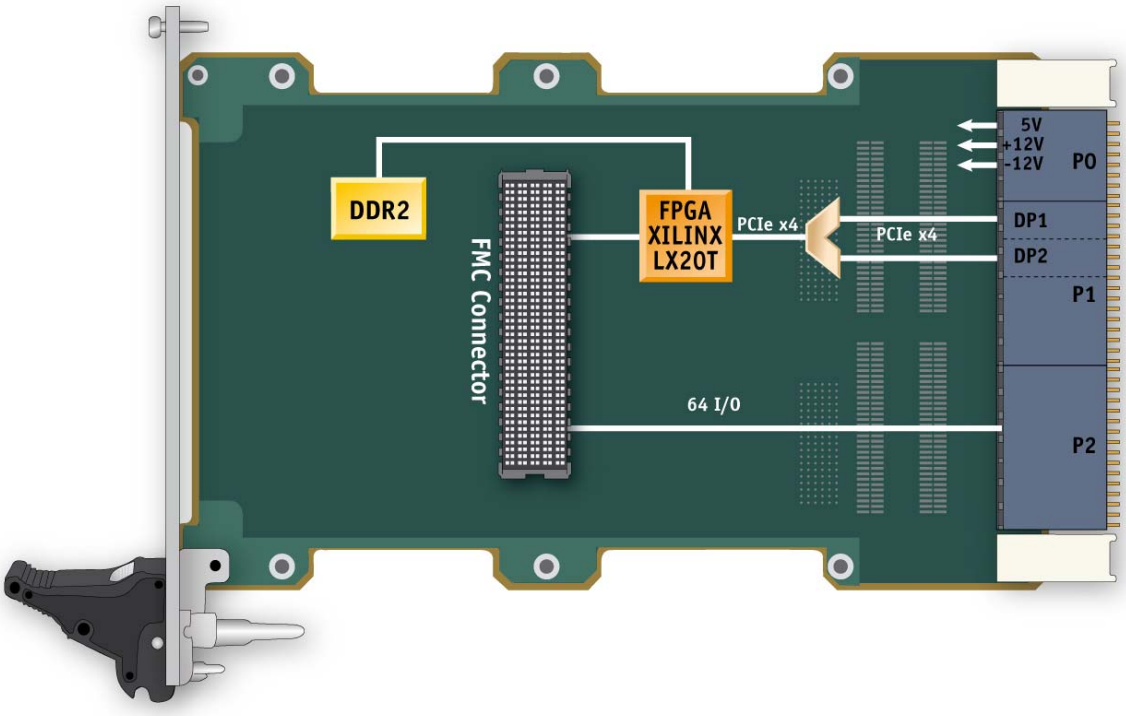


Figure 3: VX3830 Bloc Diagram

Note VPX Interface to DP2 data plane is a manufacturing build option.

1.4.2 Front Panel

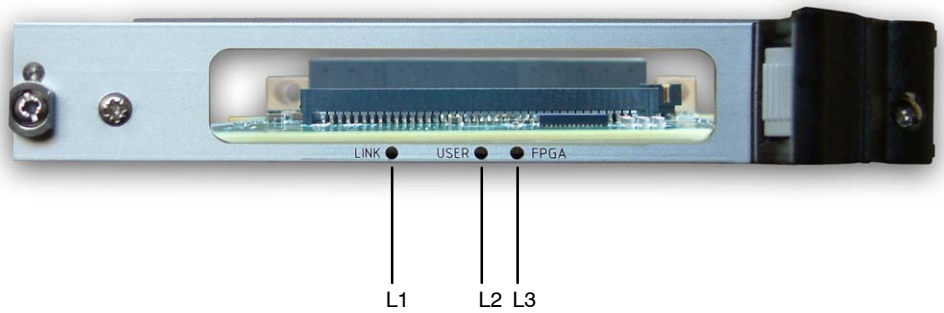


Figure 4: VX3830 Front Panel

Status LEDs Default Settings

Leds	Settings
LINK (L1)	For future Use
USER (L2)	Maintenance
FPGA (L3)	Green: FPGA loaded Red: FPGA not yet loaded
(L4: layout but not equipped)	

Table 5: LEDs Definition

1.5 Technical Specification

Mechanical	3U, VPX compliant form factor
Power Supply	5V, +/-12V if required for mezzanine board
Environmental Specification	Refer to section 1.7.1 “Environmental Specifications"
Dimensions	99.85 mm x 162.54 mm

Table 6: Main Specifications

1.5.1 MTBF Data

GB		NS		ARW	AIC
25°C	40°C	25°C	40°C	55°C	40°C
662 112 h	485 948 h	111 567 h	88 510 h	16 717 h	71 646 h

Table 7: VX3830 FMC Carrier

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

> Ground Benign (GB)

> Air Inhabited Cargo (AIC)

> Naval Sheltered (NS),

> Air Rotary Wing (ARW)

1.6 Software Support

The VX3830 does not host any CPU on board and interfaces the PCI-Express bus. It does not require any specific BSP nor Device Driver for use in a system

1.7 Standard

This Kontron product complies with the requirements of the following standards.

TYPE	ASPECT	DESCRIPTION
CE	Emission	EN55022 EN61000-6-3
	Immission	EN55024 EN61000-6-2
	Electrical Safety	EN60950-1
Mechanical	Mechanical Dimensions	IEEE1101.10
Environmental	WEEE	Waste electrical and electronic equipment
	RoHS	Restriction of the use of certain hazardous substances in electrical and electronic equipment

Table 8: Standards

1.7.1 Environmental Specifications

ENVIRONMENTAL SPECIFICATIONS		
	SA - Standard Commercial	RC - Rugged Conduction-Cooled
Conformal Coating	Optional	Standard
Airflow	1.5 m/s without throttling at 55°C	N.A.
Temperature	VITA 47-Class AC1	VITA 47-Class CC4
Cooling Method	Convection	Conduction
Operating	0°C to +55°C	-40°C to +85°C
Storage	-45°C to +85°C	-45°C to +85°C
Vibration Sine (Operating)	2g / 20-500 Hz acceleration / frequency range	5g / 22-2,000 Hz acceleration / frequency range
Random	VITA 47-Class V1	VITA 47-Class V3
Shock (Operating)	20g / 11 ms peak accel. / shock duration half sine	40g / 20 ms peak accel. / shock duration half sine
Altitude (Operating)	-1,640 to 15,000 ft	-1,640 to 50,000 ft
Relative Humidity	90% non-condensing	95% non-condensing

Table 9: Environmental Specifications

1.8 Related Publications

The following publications contain information relating to this product:

PRODUCT	PUBLICATION
Standard	
ANSI/VITA 46.0	VPX Baseline Standard - ANSI/VITA 46.0-2007
ANIS/VITA 46.4	PCI Express® on VPX Fabric Connector - VITA Draft Standard for Trial Use
ANSI/VITA 46.7	Ethernet on VPX Fabric Connector - VITA Draft Standard for Trial Use
ANSI/VITA 46.9	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules- VITA Draft Standard
ANSI/VITA 46.10	Rear Transition Module for VPX - ANSI/VITA 46.10-2009
ANSI/VITA 47	Environments, Design and Construction, Safety, and Quality for Plug-In Units Standard - ANSI/VITA 47-2005 (R2007)
ANSI/VITA 57	FPGA Mezzanine Card (FMC) Standard - ANSI/VITA 57.1-2008
Hardware	
CA.DT.A76	VX6060 User's Guide
CA.DT.A77	VX6060 Hardware Release Notes

Table 10: Related Publications

Chapter 2 - Functional Description

2.1 PCI-Express Busses

The basic x1 link has a peak raw bandwidth of 2.5 Gbps (board components compatible PCI-Express Gen1). Because the bus is bidirectional (that is, data can be transferred in both directions simultaneously), the effective raw data transfer rate is 5 Gbps.

As an example, the effective raw data transfer rate is link is 20 Gbps for a FPGA connected to a 4x PCI-Express.

VPX backplane	Data Plane DP1 (P1 wafer 1-4) Data Plane DP2 (P1- wafer 5-8)	Manufacturing option
PCI-Express x1-Lane or x4-Lane		Configurable by switch SW1.2

Table 11: PCI-Express Busses Interfaces

2.2 VX3830 Connectors Layout

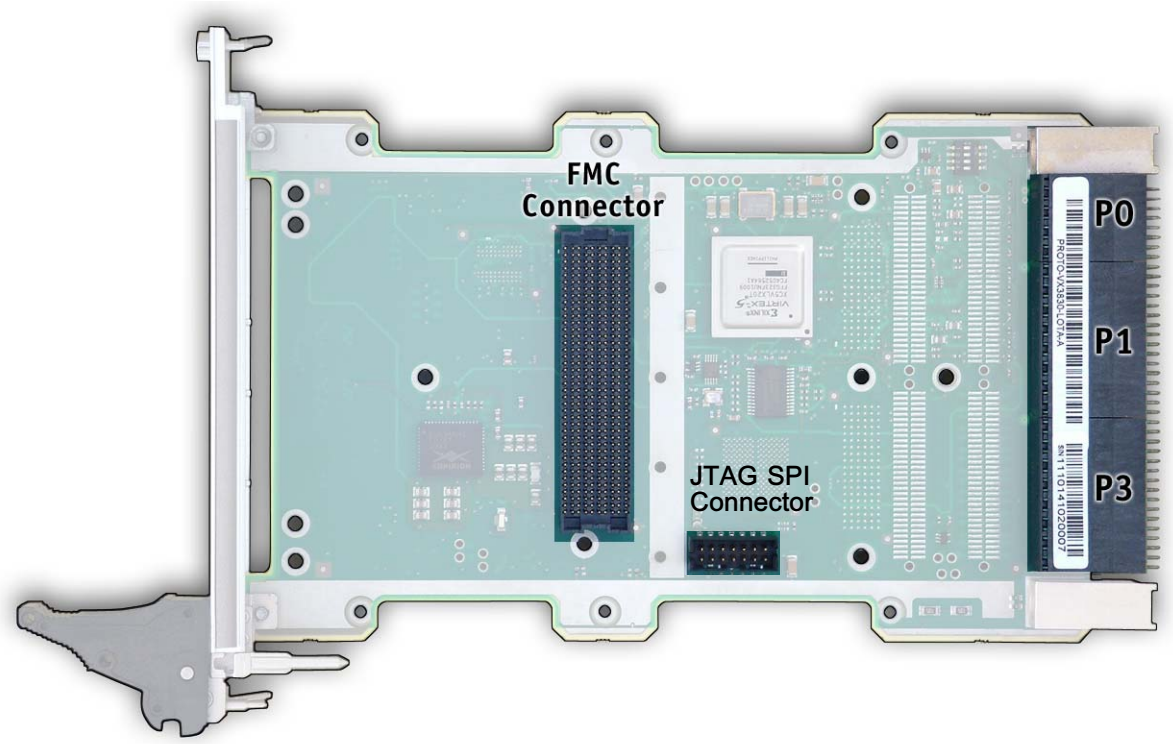


Figure 5: VX3830 Connectors Layout

2.3 Board Interfaces

2.3.1 VPX Bus Interface

The complete VPX connector configuration comprises three connectors named P0, P1 and P2

- P0: one 8-wafer 7-row connector
- P1: one 16-wafer 7-row connector
- P2: one 16-wafer 7-row connector

The VX3830 is not hot-swappable but supports the addition or removal of other boards whilst in a powered-up state.

The VX3830 is designed for a VPX bus architecture.

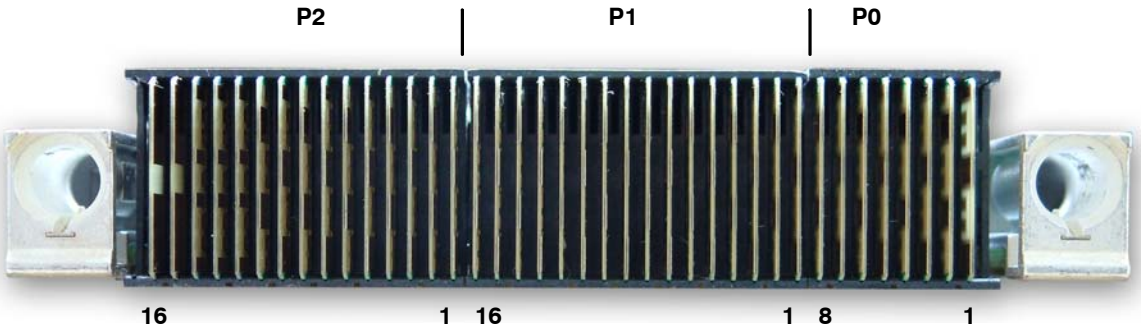


Figure 6: VPX Connectors

2.3.2 VPX Board Connectors Identification

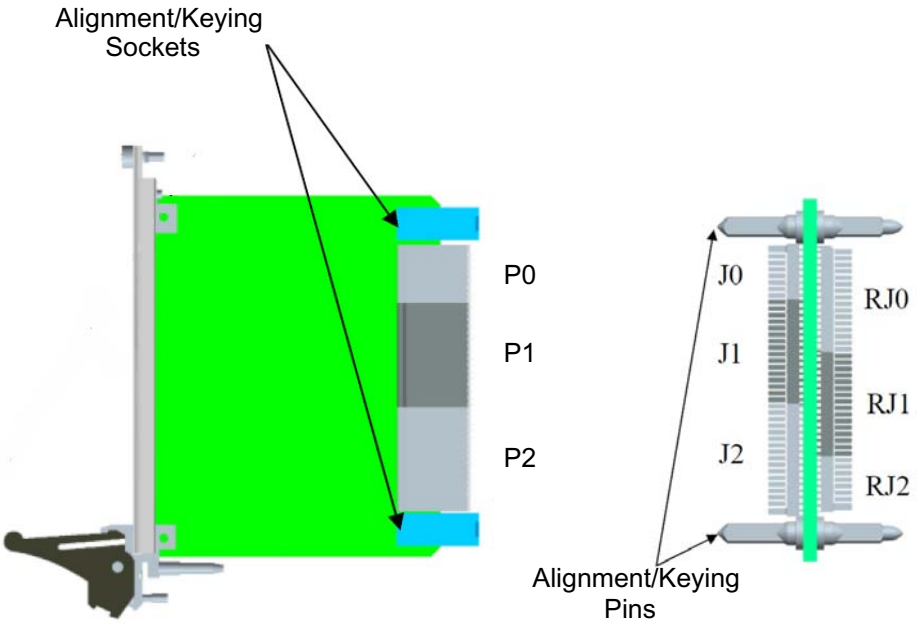


Figure 7: Connector Identification for 3U VPX Board

2.3.3 VPX Connectors Description

The VX3830 is provided with three VPX bus connectors, P0, P1 and P2.

P0 Wafer Assignment

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	+12V	+12V	+12V	N.C.			
2	+12V	+12V	+12V	N.C.			
3	+5V	+5V	+5V	N.C.	+5V	+5V	+5V
4			GND	-12V_AUX	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3V3_AUX	GND		
6	GA3*	GA2*	GND		GND	GA1*	GA0*
7	VPXP0_GPIO5 (1)	GND	P0_CLK0-	P0_CLK0+	GND	VPX_GPIO3 (1)	VPXP0_GPIO4 (1)
8	GND	REF_CLK-	REF_CLK+	GND	N.C. (RFU)	N.C. (RFU)	GND
CASE	GND						

* signal active when low

(1) These GPIO are accessible through a board option, contact Kontron for more details with the default option, this pin is N.C. on the Board.

Table 12: VPX Connector P0 Wafer Assignment

P0 Wafer Assignment

MNEMONIC	SIGNAL DEFINITION
+12V	+12 Volts DC power
+/-12V_AUX	+/-12 Volts auxiliary DC power
+3V3_AUX	+3.3 Volts auxiliary DC power
+5V	+5 Volts DC power
GA0* to GA4*	Geographical Address Inputs 0-4
GAP	Geographical Address Parity
GND	Ground
N.C.	Not Connected
N.C. (RFU)	Not Connected (Reserved for Future Use)
NVMRO	Non-Volatile Memory Read Only. When asserted (logical 1), prevents any non-volatile memory from being updated.
P0_CLK+/-	Reference Clock, bussed differential pair. It enables the entire system to synchronize to a common clock if desired.
SYSRESET*	System Reset

Table 13: VPX Connector P0 Signal Definition

P1 Wafer Assignment

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A	
1	VPXP1_GPIO0 (1)	GND	PCIE0_TX-	PCIE0_TX +	GND	PCIE0_RX-	PCIE0_RX+	port 1Date Plane
2	GND	PCIE1_TX-	PCIE1_TX+	GND	PCIE1_RX-	PCIE1_RX+	GND	
3	NC	GND	PCIE2_TX-	PCIE2_TX+	GND	PCIE2_RX-	PCIE2_RX+	
4	GND	PCIE3_TX-	PCIE3_TX+	GND	PCIE3_RX-	PCIE3_RX+	GND	
5	SYS_CON*	GND	(PCIE0_TX)	(PCIE0_TX)	GND	(PCIE0_RX)	(PCIE0_RX)	Date Plane port 2
6	GND	(PCIE1_TX)	(PCIE1_TX)	GND	(PCIE1_RX)	(PCIE1_RX)	GND	
7	NC	GND	(PCIE2_TX)	(PCIE2_TX)	GND	(PCIE2_RX)	(PCIE2_RX)	
8	GND	(PCIE3_TX)	(PCIE3_TX)	GND	(PCIE3_RX)	(PCIE3_RX)	GND	
9	NC	GND	NC	NC	GND	NC	NC	Expan-sion Plane
10	GND	NC	NC	GND	NC	NC	GND	
11	NC	GND	NC	NC	GND	NC	NC	
12	GND	NC	NC	GND	NC	NC	GND	
13	VPXP1_GPIO1 (1)	GND	NC	NC	GND	NC	NC	User Defined
14	GND	NC	NC	GND	NC	NC	GND	
15	VPXP1_GPIO2 (1)	GND	NC-	NC	GND	NC	NC	Control Plane
16	GND	NC	NC	GND	NC	NC	GND	
CASE	GND							

* signal active when low

(1) These GPIO are accessible through a board option. Contact Kontron for more details. With the default option, this pin is N.C. On the board.

Table 14: VPX Connector P1 Wafer Assignment

P2 Wafer Assignment

Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A	
1		GND	HA14_P	HA14_N	GND	HA16_P	HA16_N	*FMC*
2	GND	HA18_P	HA18_N	GND	HA20_P	HA20_N	GND	
3		GND	HA17_P	HA17_N	GND	HA15_P	HA15_N	
4	GND	HA21_P	HA21_N	GND	HA19_P	HA19_N	GND	
5		GND	HA22_P	HA22_N	GND	HB03_P	HB03_N	
6	GND	HA23_P	HA23_N	GND	HB05_P	HB05_N	GND	
7		GND	HB01_P	HB01_N	GND	HB09_P	HB09_N	
8	GND	HB07_P	HB07_N	GND	HB13_P	HB13_N	GND	
9		GND	HB11_P	HB11_N	GND	HB19_P	HB19_N	
10	GND	HB15_P	HB15_N	GND	HB21_P	HB21_N	GND	
11		GND	HB00_P	HB00_N	GND	HB02_P	HB02_N	
12	GND	HB06_P	HB05_N	GND	HB04_P	HB04_N	GND	
13		GND	HB10_P	HB10_N	GND	HB08_P	HB08_N	
14	GND	HB14_P	HB14_N	GND	HB12_P	HB12_N	GND	
15		GND	HB17_P	HB17_N	GND	HB20_P	HB20_N	
16	GND	HB18_P	HB18_N	GND	HB16_P	HB16_N	GND	

Signal names HA*x*_P/N, HB-*x*/P/N, according to VITA 57 standard routed from J1 FMC connector.

Table 15: VPX Connector P2 Wafer Assignment

2.3.4 FMC Connector

The VX3830 is equipped with a 40-pin High Pin Count (HPC) FMC connector where the I/O signals:

- LAx_P/N [x=0,33] (Rows C, D, G, H) are routed from/to the FPGA
- HAx_P/N [x=14,23] (Rows E, F, J, K) are routed from/to the VPX P2 connector
- HBx_P/N [x=0,21] (Rows E, F, J, K) are routed from/to the VPX P2 connector

	Row H	Row G	Row D	Row C
1	VREF_A_M2C	GND	PG_C2M	GND
2	PRSNT_M2C_L	CLK0_C2M_P	GND	NC
3	GND	CLK0_C2M_N	GND	NC
4	CLK0_M2C_P	GND	NC	GND
5	CLK0_M2C_N	GND	NC	GND
6	GND	LA00_P_CC	GND	NC
7	LA02_P	LA00_N_CC	GND	NC
8	LA02_N	GND	LA01_P_CC	GND
9	GND	LA03_P	LA01_N_CC	GND
10	LA04_P	LA03_N	GND	LA06_P
11	LA04_N	GND	LA05_P	LA06_N
12	GND	LA08_P	LA05_N	GND
13	LA07_P	LA08_N	GND	GND
14	LA07_N	GND	LA09_P	LA10_P
15	GND	LA12_P	LA09_N	LA10_N
16	LA11_P	LA12_N	GND	GND
17	LA11_N	GND	LA13_P	GND
18	GND	LA16_P	LA13_N	LA14_P
19	LA15_P	LA16_N	GND	LA14_N
20	LA15_N	GND	LA17_P_CC	GND
21	GND	LA20_P	LA17_N_CC	GND
22	LA19_P	LA20_N	GND	LA18_P_CC
23	LA19_N	GND	LA23_P	LA18_N_CC
24	GND	LA22_P	LA23_N	GND
25	LA21_P	LA22_N	GND	GND
26	LA21_N	GND	LA26_P	LA27_P
27	GND	LA25_P	LA26_N	LA27_N
28	LA24_P	LA25_N	GND	GND
29	LA24_N	GND	(TCK)	GND
30	GND	LA29_P	(TDI)	SCL
31	LA28_P	LA29_N	(TDO)	SDA
32	LA28_N	GND	3P3VAUX	GND
33	GND	LA31_P	(TMS)	GND
34	LA30_P	LA31_N	(TRST_L)	GA0
35	LA30_N	GND	GA1	12P0V
36	GND	LA33_P	3P3V	GND
37	LA32_P	LA33_N	GND	12P0V
38	LA32_N	GND	3P3V	GND
39	GND	VADJ	GND	3P3V
40	VADJ	GND	3P3V	GND

Table 16: FMC Connector Rows CDGH

	Row K	Row J	Row F	Row E	Row B	Row A
1	NC	GND	PG_M2C	GND	NC	GND
2	GND	CLK1_C2M_P	GND	NC	GND	NC
3	GND	CLK1_C2M_N	GND	NC	GND	NC
4	CLK1_M2C_P	GND	NC	GND	NC	GND
5	CLK1_M2C_N	GND	NC	GND	NC	GND
6	GND	NC	GND	NC	GND	NC
7	NC	NC	NC	NC	GND	NC
8	NC	GND	NC	GND	NC	GND
9	GND	NC	GND	NC	NC	GND
10	NC	NC	NC	NC	GND	NC
11	NC	GND	NC	GND	GND	NC
12	GND	NC	GND	NC	NC	GND
13	NC	NC	NC	NC	NC	GND
14	NC	GND	NC	GND	GND	NC
15	GND	HA14_P	GND	HA16_P	GND	NC
16	HA17_P_CC	HA14_N	HA15_P	HA16_N	NC	GND
17	HA17_N_CC	GND	HA15_N	GND	NC	GND
18	GND	HA18_P	GND	HA20_P	GND	NC
19	HA21_P	HA18_N	HA19_P	HA20_N	GND	NC
20	HA21_N	GND	HA19_N	GND	NC	GND
21	GND	HA22_P	GND	HB03_P	NC	GND
22	HA23_P	HA22_N	HB02_P	HB03_N	GND	NC
23	HA23_N	GND	HB02_N	GND	GND	NC
24	GND	HB01_P	GND	HB05_P	NC	GND
25	HB00_P_CC	HB01_N	HB04_P	HB05_N	NC	GND
26	HB00_N_CC	GND	HB04_N	GND	GND	NC
27	GND	HB07_P	GND	HB09_P	GND	NC
28	HB06_P_CC	HB07_N	HB08_P	HB09_N	NC	GND
29	HB06_N_CC	GND	HB08_N	GND	NC	GND
30	GND	HB11_P	GND	HB13_P	GND	NC
31	HB10_P	HB11_N	HB12_P	HB13_N	GND	NC
32	HB10_N	GND	HB12_N	GND	NC	GND
33	GND	HB15_P	GND	HB19_P	NC	GND
34	HB14_P	HB15_N	HB16_P	HB19_N	GND	NC
35	HB14_N	GND	HB16_N	GND	GND	NC
36	GND	HB18_P	GND	HB21_P	NC	GND
37	HB17_P_CC	HB18_N	HB20_P	HB21_N	NC	GND
38	HB17_N_CC	GND	HB20_N	GND	GND	NC
39	GND	NC	GND	VADJ	GND	NC
40	NC	GND	VADJ	GND	NC	GND

Table 17: FMC Connector Rows ABEFJK

FMC Connector Signal Definition

Mnemonic	Signal Definition
CLK[0,1]_C2M_P, CLK[0,1]_C2M_N	Each differential pair that is assigned for a clock signal, which is driven from the carrier card to the IO Mezzanine Module
CLK[0,1]_M2C_P, CLK[0,1]_M2C_N	Each differential pair that is assigned for a clock signal, which is driven from the IO Mezzanine Module to the carrier card
GA[0..1]	These signals provide geographical addressed of the module and are used for I2C channel select
GND	This is signal ground
HA[00..23]_P HA[00..23]_N	User defined signals on Bank A located on the HPC
HB[00..21]_P HB[00..21]_N	User defined signals on Bank B located on the HPC
LA[00..33]_P LA[00..33]_N	User defined signals on Bank A located on the LPC and HPC
NC	Not Connected
PG_C2M	Power Good Carrier Card. This signal asserts high by the carrier card when power supplies, VADJ, 12P0V, 3P3V, are within tolerance
PG_M2C	Power Good Mezzanine. This signal is routed to an input pin of the FPGA.
PRSNT_M2C_L	Module present signal. This signal allows the carrier to determine whether an IO Mezzanine module is present
SCL, SDA	System Management I2C serial clock and serial data. These signals provide a data line for a two-wire serial management bus
TRST_L, TCK, TMS, TDI, TDO	TAG Reset, Clock, Mode Select, Data In and Data Out signal. The JTAG signals onto the FMC connector of the VX3830 are not activated.
VADJ	These pins carry an adjustable voltage level power from the carrier to the IO Mezzanine module
VREF_A_M2C	This is the reference voltage associated with the signaling standard used by the bank A data pins, LAxx and HAxx. On the VX3830 this signal is routed to the FPGA.
12P0V	These pins carry 12V power from the carrier to the IO Mezzanine module
3P3VAUX	A 3.3V auxiliary power supply.
3P3V	These pins carry 3.3V power from the carrier to the IO Mezzanine module

2.3.5 JTAG/SPI Connector

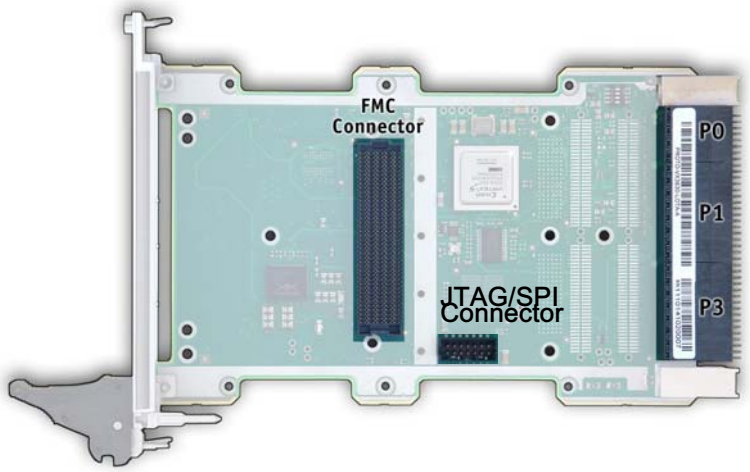


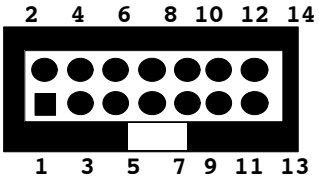
Figure 8: Location of the JTAG/SPI Connector

The JTAG/SPI connector is a 14-pin HE10 connector.

JTAG/SPI Connector Pin Assignment

Pin	Signal	Description
1	N.C.	Not Connected
2	P3V3	+3.3V
3	GND	Ground
4	TMS or $\overline{SS}$	JTAG Test Mode Select Slave Select
5	GND	Ground
6	TCK or SCLK	JTAG Test Clock Serial Clock
7	GND	Ground
8	TDO or MISO	JTAG Test Data Out MASTER IN, SLAVE OUT
9	GND	Ground
10	TDI or MOSI	JTAG Test Data In MASTER OUT, SLAVE IN
11	GND	Ground
12 .. 14	N.C.	Not Connected

Table 18: JTAG/SPI Connector Pin Assigment



JTAG/SPI

Figure 9: Onboard JTAG/SPI Connector

Chapter 3 - Installation

The VX3830 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

3.1 Safety Requirements

The following safety precautions must be observed when installing or operating the VX3830. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.
In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

This board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

3.2 Board Identification

The VX3830 boards are identified by labels fitted to the top and bottom sides.

Top Side

- **A** "Order Code" label.
- **B** "Serial Number" label.

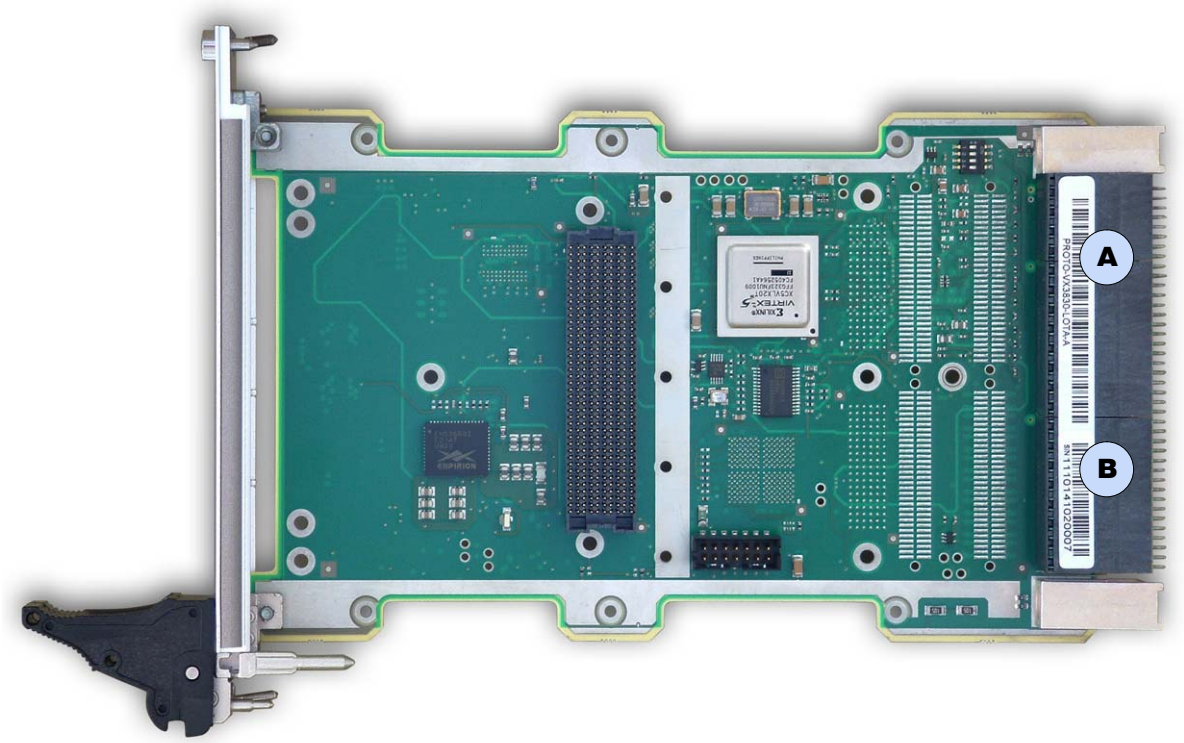


Figure 10: VX3830 Identification (Top Side)

Bottom Side

c "Functional Identification" label (Variant + E.C. Level)

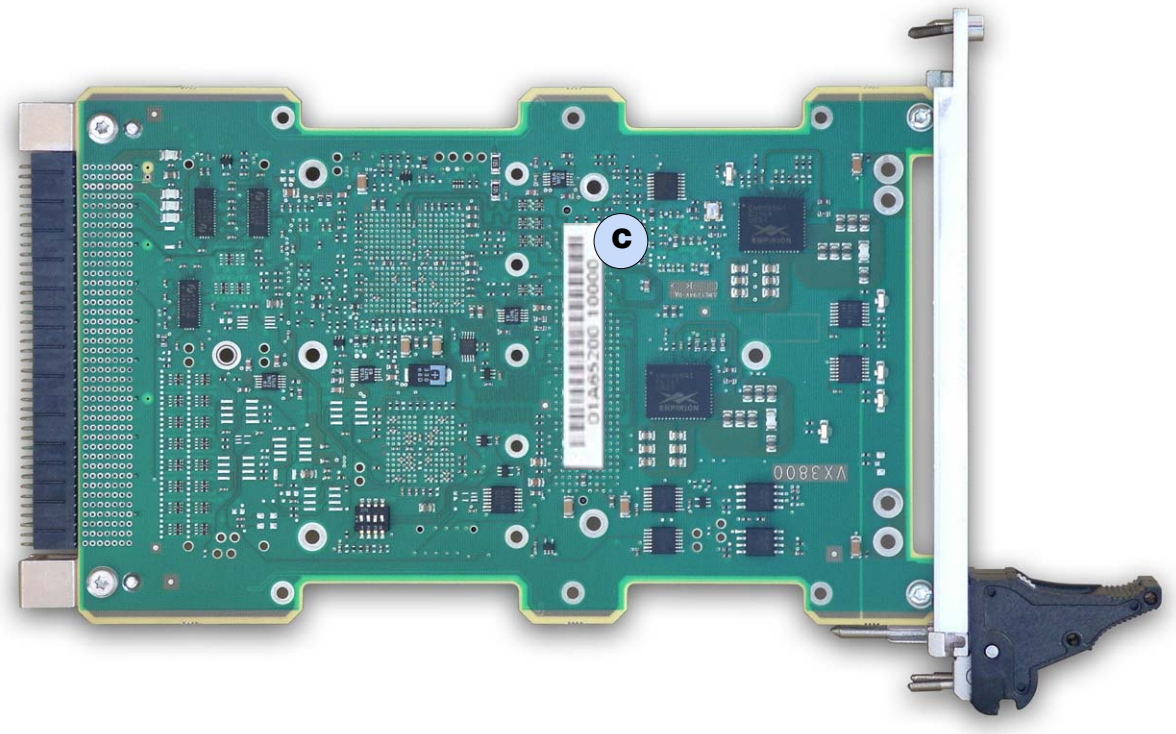
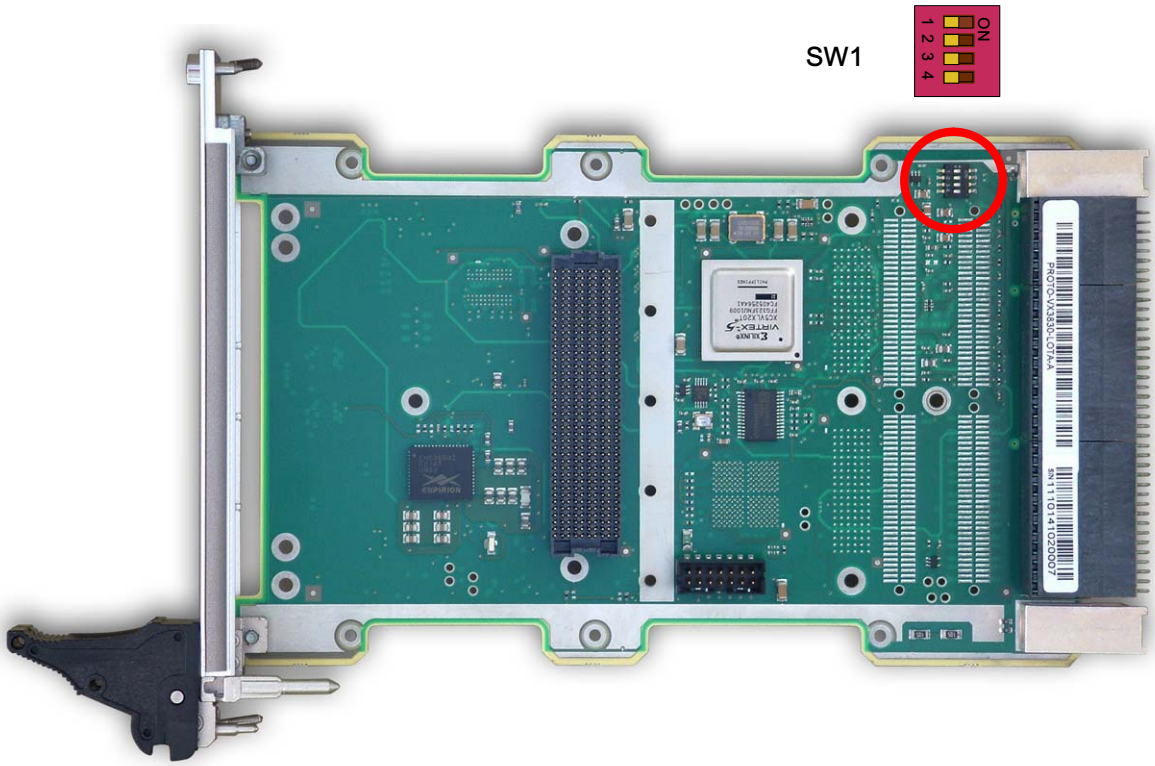


Figure 11: VX3830 Identification (Bottom Side)

3.3 Board Configuration

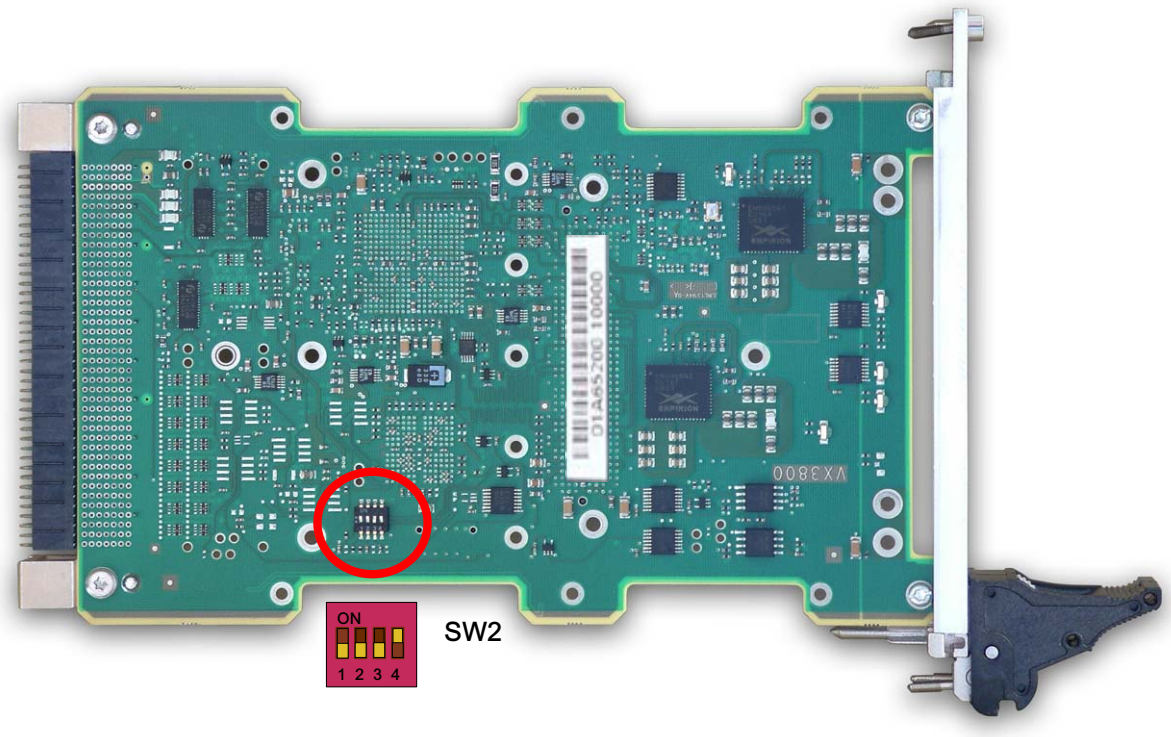
3.3.1 DIP Switch SW1 Description



Number	OFF function	ON function	Default
1	PCI Express on FPGA site	FPGA not connected on PCI Express	OFF
2	PCI Express 1x link	PCI Express 4x link (1)	OFF
3	Onboard 100 MHz PCI-E Clock	Backplane common 100 MHz clock	OFF
4	Maskable reset from the VPX backplane is inactive	Maskable reset from the VPX backplane is active	OFF

Notes: (1) If the Backplane is compatible with 4x link PCI-E

3.3.2 DIP Switch SW2 Description



Number	OFF function	ON function	Default
1	Use of User Flash	Use of Rescue Flash	OFF
2	SPI access from the P0401 connector to flash is enable	JTAG access from the P0401 connector to the FPGA is enable.	OFF
3 unused			OFF
4	Disable automatic FPGA load at power-on	Enable automatic FPGA load at power-on	ON

3.4 FMC Installation

FPGA Mezzanine Card, or FMC, as defined in VITA 57, provides a specification describing an I/O mezzanine module with connection to an FPGA or other device with reconfigurable I/O capability.

The FMC mezzanine module uses a high-pin count 400 pin high-speed array connector, HPC.

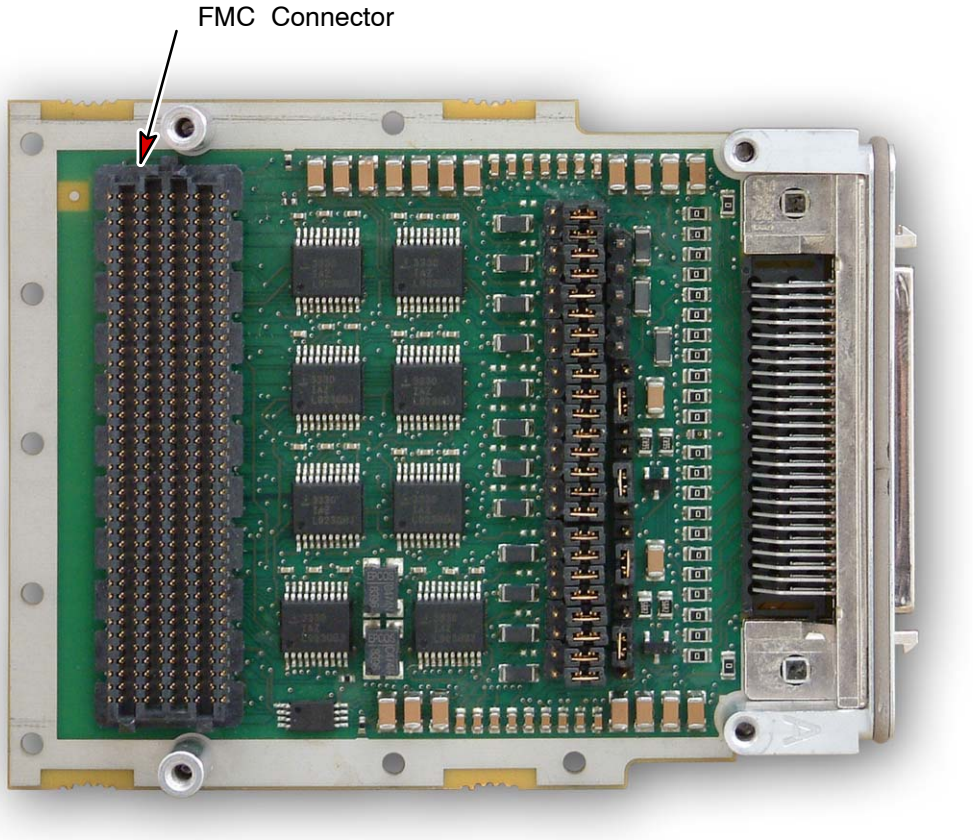


Figure 12: Example of FMC Board

Check the configuration of the SW1 and SW2 DIP switches

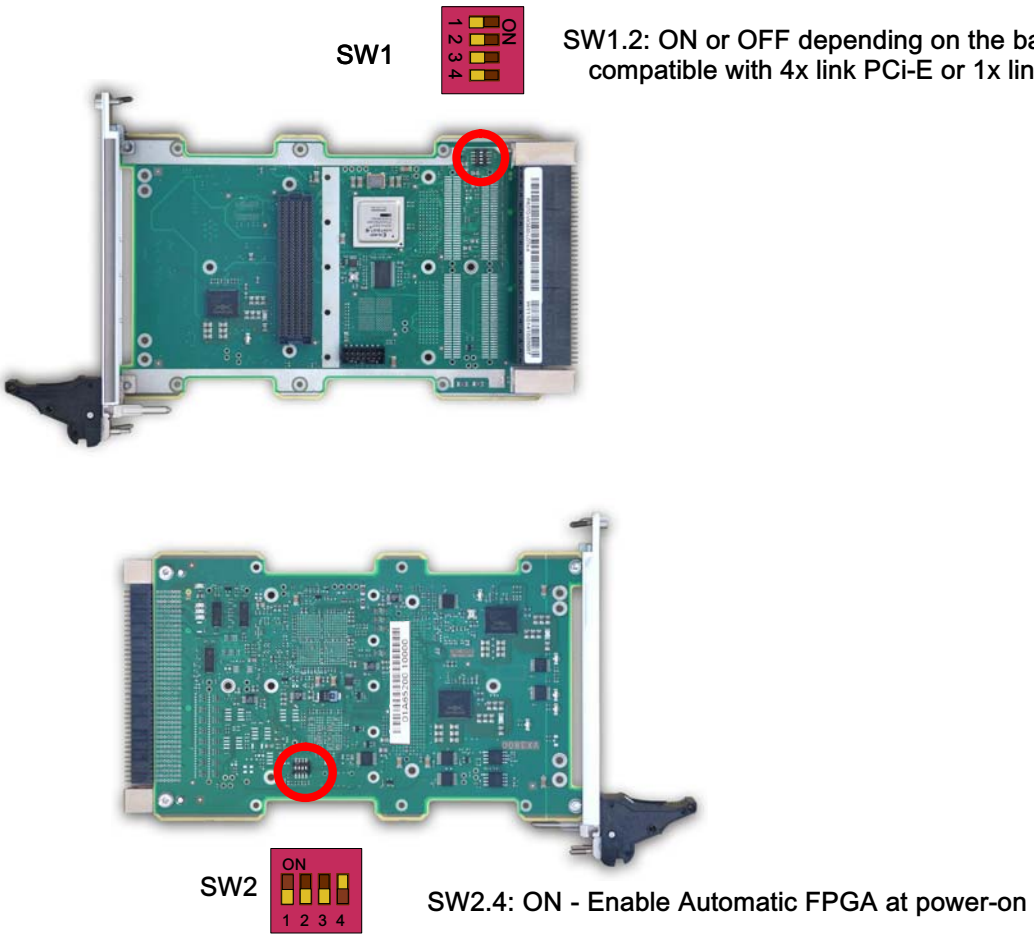


Figure 13: DIP Switches Configuration in FMC Mode

Figure 14 shows a FMC installation on the FMC Site.

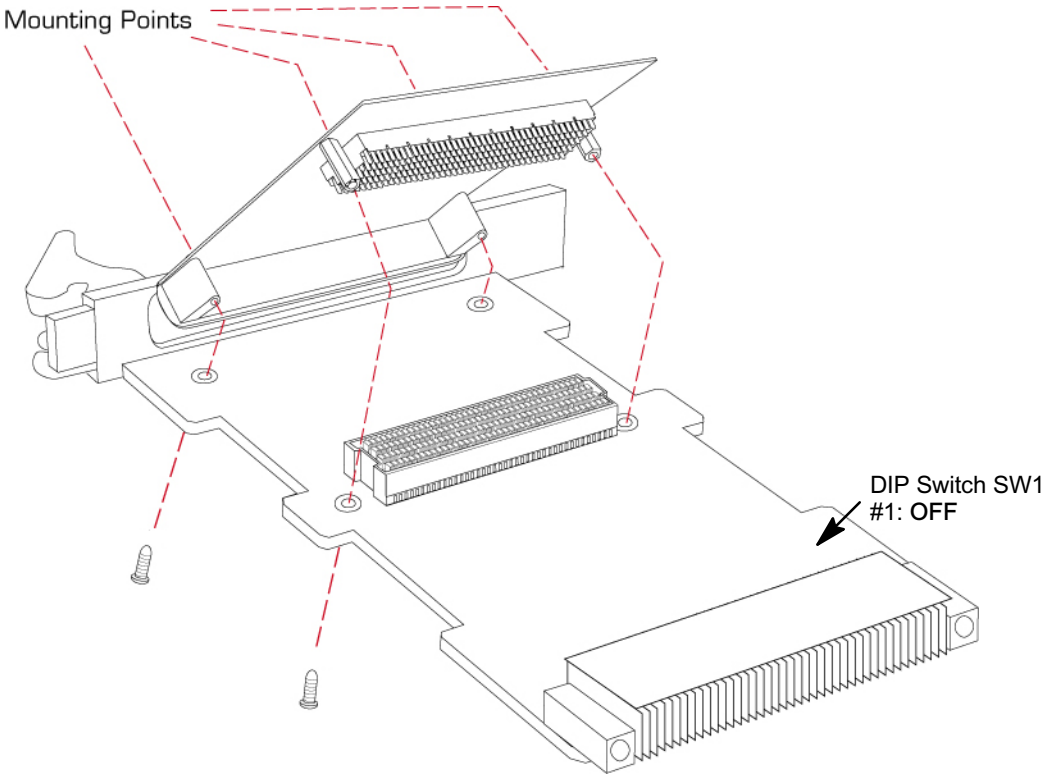


Figure 14: FMC Installation on FMC Site

Chapter 4 - Flash Programming

The flash programming is done in SPI mode , it uses the programming tools provided by Xilinx.

Only the user flash can be programmed by the user. The rescue flash contains a FPGA code compatible with all FMC mezzanines. The rescue code is protected from erasing at the factory.

The flash programming can be done:

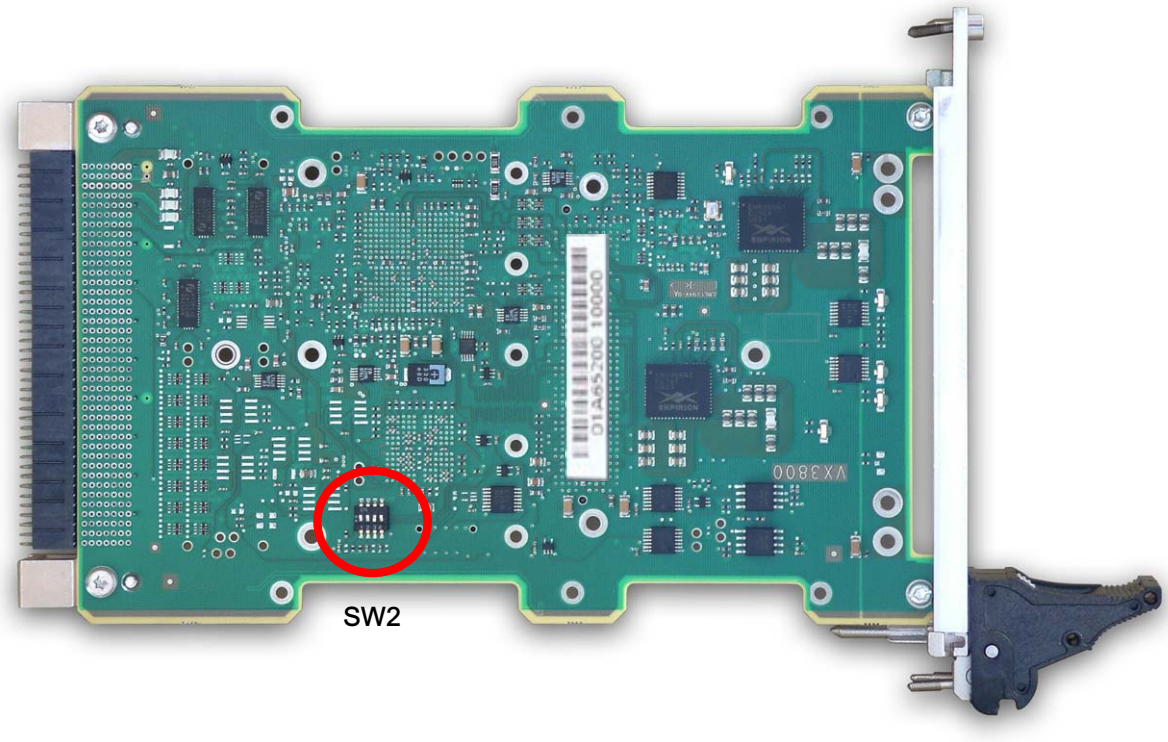
- either remotely using the Kontron's VITA 57 FPGA Configuration

or

- direclty using the JTAG-SPI connector (see below).

Direct SPI Flash Programming

For direct SPI flash programming the switch SW2 must be configured as followed:



Number	OFF function	ON function	SPI Flash programming
1	Use of User Flash	Use of Rescue Flash	OFF
2	SPI access from the P0401 connector to flash is enable	JTAG access from the P0401 connector to the FPGA is enable.	OFF
3			Not used
4	Disable automatic FPGA load at power-on	Enable automatic FPGA load at power-on	ON

The tool used to program the FPGA and the associated flash is named **iMPACT** and is provided by Xilinx.

This tool can be found at the Xilinx web site http://www.xilinx.com/support/download

1 - You need to have a Xilinx account to be able download Xilinx tools (Sign In tab).
2- iMPACT is a standalone programming tool.

Plug the Xilinx programming cable on the VX3830 board:

Plug the USB cable on a PC with the programming tool iMPACT installed.

All the documentation associated with the iMPACT tool can be found at the Xilinx web site http://www.xilinx.com/support/documentation. An application note xapp951.pdf discusses the programmation the flash in SPI mode.

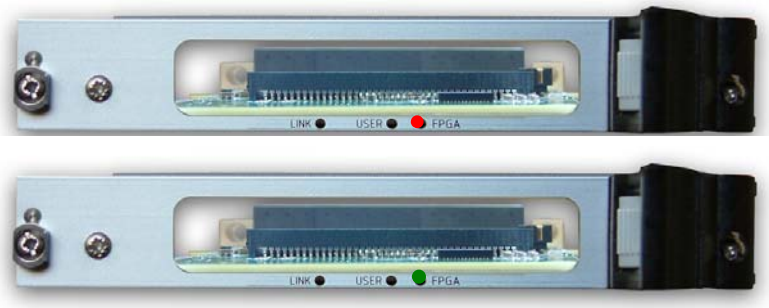
The iMPACT tool needs to know the type of SPI flash used on the board. The VX3830 uses AT45DB161D device for both user and rescue flash. The VX3830 uses a Xilinx XC5VLX20T-2FFG323I FPGA device.

Board order Code	FPGA device	User Flash Device
VX3830-SA-000	Xilinx XC5VLX20T-2FFG323I	Atmel® AT45DB161D
VX3830-RC-000	Xilinx XC5VLX20T-2FFG323I	Atmel® AT45DB161D

When the programming operation has successfully ended, the message: Program Succeeded is displayed in the main window (in blue color). Now the user flash is programmed with the new FPGA code.

To load the FPGA with this new code, turn off the power, remove the programming cable and turn on the power on. At each power on of the VX3830 board, the FPGA code will be downloaded with the new user flash code.

If the FPGA load has successfully completed, the LED FPGA goes from red color to green color.



If the FPGA load fails, the LED FPGA remains red.

To be able to program the SPI user flash of the VX3830, the FPGA needs to be loaded with a valid image (LED FPGA must be green). The rescue flash provides a valid FPGA image. If the user flash image load fails, you need first to load the FPGA with a valid image. To do so:

- Switch off the VX3830
- Set up SW2 switch 1 from OFF position to ON position
- Switch on the VX3830 (the FPGA is loaded with a valid image)
- Without powering-off the VX3830 board, set up SW2 switch 1 from ON position to OFF position
- The VX3830 is ready for user flash programming

Chapter 5 - Power Considerations

5.1 System Power

The information described in following sections must be taken into account by system integrators when specifying the VX3830 system environment.

5.1.1 Input Voltage

The VX3830 has been designed for optimal power input and distribution. Nevertheless, it is necessary to observe certain criteria essential for application stability and reliability.

The following table specifies the ranges for the different input power voltages within which the board is functional.

The VX3830 is not guaranteed to function if the board is not operated within the prescribed limits.

Input Supply Voltage	Absolute Range
+3.3 V	not used on VX3830
+5 V	4.85V min. to 5.25V max.
+12 V	11.4V min. to 12.6V max.

Table 19: DC Operational Input Voltage Ranges

5.1.2 Backplane

Backplanes to be used with the VX3830 must be adequately specified. The backplane must provide optimal power distribution for the +5 V and +12 V power inputs.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided.

5.1.3 Power Supply Units

Power supplies for the VX3830 must be specified with enough reserve for the remaining system consumption.

In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

As the design of the VX3830 has been optimized for minimal power consumption, the power supply unit shall be stable even without minimum load.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for die resistance variations.

Non-industrial ATX PSUs may require a greater minimum load than a single VX3830 is capable of creating. When a PSU of this type is used, it will not power up correctly and the VX3830 may hangup. The solution is to use an industrial PSU or to add more load to the system.

The start-up behavior of VPX power supplies is critical for all new CPU boards. These boards require a defined power of sequence and start-up behavior of the power supply.

For information on the required behavior, refer to the power supply specifications on the Form Factors website (http://www.formfactors.org) and to the VPX specification on the VITA web site (http://www.vita.com).

» Tolerance

The tolerance of the voltage lines is described in the VITA specification (ANSI/VITA 46.0-2007 VPX Baseline Standard).

The recommended measurement point for the voltage is the VPX connector on the CPU board.

The following table provides information regarding the required characteristics for each board input voltage.

Backplane Voltage	Nominal Value Tolerance	Max. Ripple	(P-P)	Notes
+5V	+5V DC	+5% / -2.5%	50 mV	main voltage
+3.3V	Not used			
+12V	+12 VDC	+5% / -5%	50 mV	required for FMC slot
-12V	Not used			
GND	Ground, not directly connected to ptential earth (PE)			

Table 20: Input Voltage Characteristics

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No voltage of reverse polarity may be present on any output during turn-on or turn-off.

5.2 Power Consumption

The goal of this description is to provide a method to calculate the power consumption for the VX3830 and for additional configurations. The processor dissipates the majority of the thermal power.

The power consumption tables below list the voltage and power specifications for the VX3830 board. The values were measured using an 5-slot passive VPX backplane.

The operating system used was Linux Fedora 9. All measurements were conducted at a temperature of 25°C.

The measured values varied, because the power consumption was dependent on processor activity.

Real Applications

The following table indicates the power consumption, using real applications.

The Power Consumption was measured under Linux Operating System in:

- Linux Idle Mode
- Linux Under Test

Power	Linux Idle Mode (1)	Linux Under Test (2)
+5 V	6W	7.1W
+12V	0W (not used)	0W (not used)
Total	6W	7.1W

(1) The FPGA is loaded with an image, no test are running

(2) The FPGA is loaded with a functional GPIO image. A GPIO FMC is plugged on the VX3830. A simple test is running to check the behavior of the GPIO.

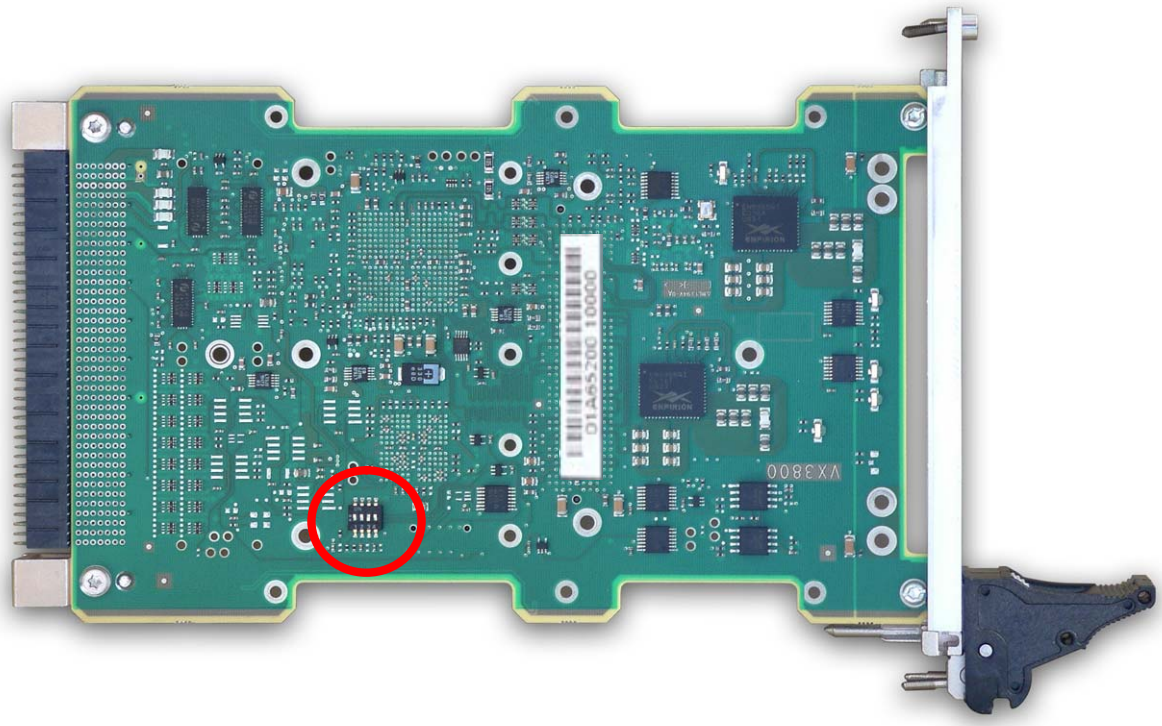
Appendix A - Loading the Image of the Rescue Flash in the FPGA

There are many reasons to load the rescue flash in the FPGA at system power-on:

- No valid image in the user flash (the LED “FPGA” remains red)
- The user flash code does not match the FMC mezzanine set up on the VX3830

To load the rescue flash in the FPGA proceed as decribed below:

- Power-down the board
- Set up the switch SW2



Number	OFF function	ON function	Load Rescue Flash Image
1	Use of User Flash	Use of Rescue Flash	ON
2	SPI access from the P0401 connector to flash is enable	JTAG access from the P0401 connector to the FPGA is enable.	OFF
3 unused			OFF (not used)
4	Disable automatic FPGA load at power-on	Enable automatic FPGA load at power-on	ON

- Power-up the board
- The FPGA is loaded with the rescue flash code

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