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» VX3905 «

3U VPX PCI Express and Ethernet Switch
User's Guide

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Revision History

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Rev.	Brief Description of Changes	Date of Issue
3e	Describe the microcontroller function and the VPX P1/P2 single ended pins evolution. Update the default manufacturing PCIe switch EEPROM content	10-2012
2e	Add of option: Ethernet only	11-2011
1e	Update of sections 1.2 - Ordering Information and 1.4 - Firmware Settings	07-2011
0e	Initial Issue (Preliminary)	07-2011

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- reduce waste arising from electrical and electronic equipment (EEE)
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- encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- improve the environmental performance of all those involved during the lifecycle of EEE

Conventions

This guide uses several types of notice: Note, Caution, ESD.

Note: this notice calls attention to important features or instructions.


Caution: this notice alert you to system damage, loss of data, or risk of personal injury.


ESD: This banner indicates an Electrostatic Sensitive Device.

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix `0x' shows a hexadecimal number, following the `C' programming language convention.

The multipliers `k', `M' and `G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when `K', `M' and `G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

When describing transfer rates, `k' `M' and `G' mean $*10^3$, $*10^6$ and $*10^9$ *not $*2^{10}$ $*2^{20}$ and $*2^{30}$.*

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and CompactPCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Signal names ending with an asterisk (*) or a hash (#) denote active low signals; all other signals are active high.

Signal names follow the PICMG 2.0 R3.0 CompactPCI Specification and the PCI Local Bus 2.3 Specification.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions


Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.


Caution, Electric Shock!
Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Chapter 1 - General Presentation

1.1 Product Overview

The VX3905 is a standard 3U OpenVPX Fabric featuring PCI Express switching and unmanaged Gigabit Ethernet switching. It is compliant with OpenVPX slot profile SLT3-SWH-6F6U-14.4.1 and module profile MOD3-SWH-6F6U-16.4.1-3 while offering additional configuration options.

The module is available in air cooling and conduction cooling environments from 0°C/55°C to -40°C/+85°C. It can be used for switching Ethernet and/or PCIe express protocols in a 3U OpenVPX environment, but is also adequate in an hybrid 6U/3U environment where it can be used to switch PCIe and Ethernet ports of 6U payloads.

The basic product configuration on the VPX connectors is for switching from the backplane 6 PCIe gen2 x4 ports and 6 1000BASE-BX Ethernet 1G serdes ports. The front panel includes 2 1000BASE-T Ethernet RJ45 interfaces connected to the Ethernet switch and one x4 PCIe standard cable connector (downstream port) attached to the PCIe switch. Moreover, one 1000BASE-T Ethernet link is available on the rear on user defined pins of P2 VPX connector.

Additional configuration flexibility accessible by the user includes defining the rear PCIe lanes as x2 ports or x1 ports instead of x4 ports, thereby increasing the number of available ports for a given number of lanes. It is also possible to partition the PCIe switch in multiple smaller independent switches to accommodate multiple root complex controlling their own PCIe adapters on a standard centralized backplane topology.

When needed, some dedicated ordering codes are defined to increase the number of PCIe lanes on the backplane from 24 up to 32, while lowering the number of the Ethernet ports available. In the same philosophy, some PCIe ports on the rear VPX connectors could be replaced by a PCIe common reference clock generator and/or by SATA incoming links when it is desirable to host an onboard Hard Disk Drive on the VPX switch module.

A simplified bloc diagram of the VX3905 architecture in the basic configuration is shown at Figure 1.

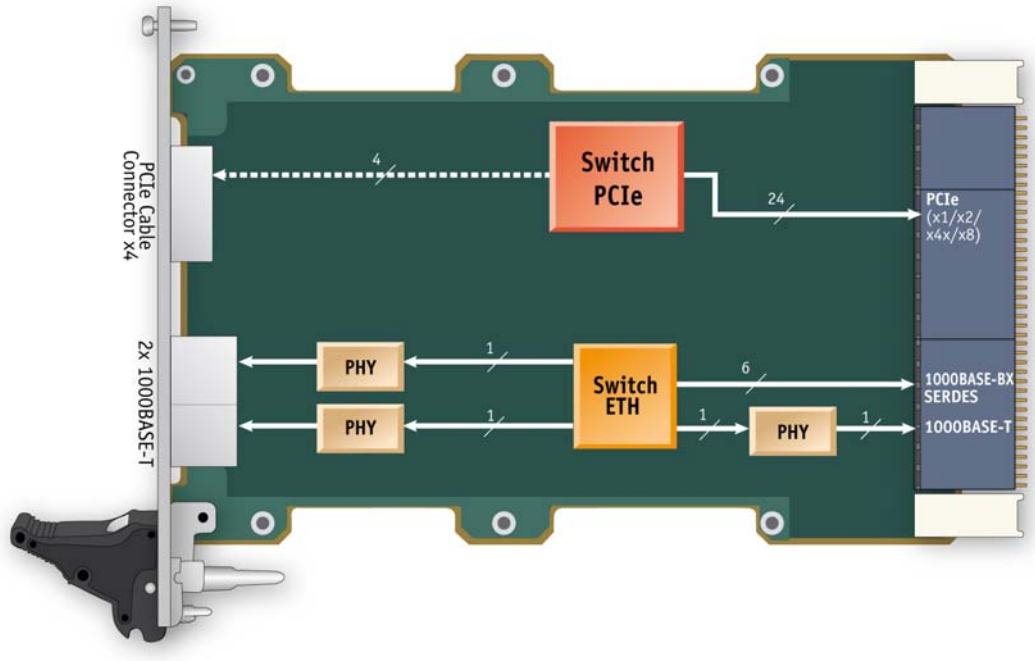

Figure 1: VX3905 Simplified Block Diagram

1.2 Ordering Information

Order code definition

DESCRIPTION					Code	VX3905-	SA	-	0	1	0	0	0	
	SA	WA	RA	RC										
Environment Class :														
Standard (Air)	X				SA									
Extended Temperature		X			WA									
Rugged Convection Cooled			X		RA									
Rugged Conduction Cooled				X	RC									
REDI Covers	X			X	0									
Front Panel														
4HP Front Panel (0.8 inch)	X	X	X		0									
5HP Front Panel (1 inch)	X	X	X		1									
No Front Panel				X	N									
Rear IO Type														
24*PCIe Lanes/6*1000BASE-BX/1*1000BASE-T					0									
28*PCIe Lanes/2*1000BASE-BX/1*1000BASE-T					1									
32*PCIe Lanes/no Ethernet ports					2									
22*PCIe Lanes/2*SATA Links/6 *1000BASE-BX/1*1000BASE-T					S									
20*PCIe Lanes/8*CCLK/6*1000BASE-BX/1 *1000BASE-T					A									
18*PCIe Lanes/8*CCLK/2*SATA Links/6* 1000BASE-BX/1*1000BASE-T					B									
no PCIe lanes/6*1000BASE-BX/1*1000BASE-T					E									
Reserved														
Reserved														
Coating	X	(*)	(*)	(*)	V	Add V suffix only when not default								

(*) Default

Preferred order code: VX3905-SA-01000

Whenever possible, the preferred order code should be used. Otherwise, minimum deviation from the preferred order code should apply, and availability should be checked.

1.3 Technical Specification

1.3.1 Power

Supply voltages:

- 5 Volts only

Power consumption of the VX3905:

- Idle (no links): 11W
- Typical: 14W
- Maximum: 20W

1.3.2 Mechanics

- 3U VPX board occupying 1 slot
- 100 mm (H) x 160 mm (D)
- The SA Air-Cooled board uses standard VPX front panel (0.8 inch or 1 inch depending on order code).
- Weight: SA build 250g, RC build 280g

1.3.3 Environmental Specifications

ENVIRONMENTAL SPECIFICATIONS		
	SA - Standard Commercial	RC - Rugged Conduction-Cooled
Conformal Coating	Optional	Standard
Airflow	1 m/s (2.6 CFM)	N.A.
Temperature	VITA 47-Class AC1	VITA 47-Class CC4
Cooling Method	Convection	Conduction
Operating	0°C to +55°C	-40°C to +85°C
Storage	-45°C to +85°C	-45°C to +85°C
Vibration Sine (Operating)	2g / 20-500 Hz acceleration / frequency range	5g / 20-2,000 Hz acceleration / frequency range
Random	VITA 47-Class V1	VITA 47-Class V3
Shock (Operating)	20g / 11 ms peak accel. / shock duration half sine	40g / 20 ms peak accel. / shock duration half sine
Altitude (Operating)	-1,640 to 60,000 ft	-1,640 to 60,000 ft
Relative Humidity	90% non-condensing 95% non-condensing when coated	95% non-condensing

Table 1: Environmental Specifications

1.3.4 Reliability

The predicted MTBF according MIL-HDBK217F-2 standard are:

GB		NS		ARW	AIC
25°C	40°C	25°C	40°C	55°C	40°C
500 937 h	356 933 h	96 444 h	79 248 h	18 484 h	76 663 h

Table 2: VX3905 MTBF

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

> Ground Benign (GB)

> Naval Sheltered (NS),

> Air Rotary Wing (ARW)

> Air Inhabited Cargo (AIC)

1.4 Firmware Settings

The PCIe switch and the Ethernet switch devices are highly configurable . Both devices come with a power up default configuration that satisfies most of the applications. The PCIe switch includes a number of user settable micro switches to further specify the main operating environments such as PCIe port sizes.

For some applications requiring more precise power up settings, it is possible to program the PCIe switch EEPROM through a software utility provided by Kontron, and running on a Kontron CPU card attached to the upstream PCIe port of the switch.

If you want to proceed to EEPROMs content changes, make sure that during the programmation, the NVMRO (Non Volatile Memory Read Only) signal from the backplane is set to 0. Alternatively, the on board NVMRO micro switch on SW4 can be set to on.

1.4.1 Default Ethernet EEPROM switch setting

The default EEPROM code set at the factory only configures the appropriate Ethernet switch ports as 1000BASE-Bx serdes or 1000BASE-T/SGMII according to the hardware fixed wiring of these ports. The binary content is the following:

```
# set the port 1, 2, 4, 5, 7, 8, 9 in serdes mode
# bit 15:14 to 11 for reg20
# bit 6 to 1 and bit 2:0 to 101 for reg0
# $Id: sweeprom_serdes.xxd,v 1.3 2010/04/28 12:25:34 rod Exp $
0000000: f6d4 c403 f6c0 0045 ffff
```

1.4.2 Default PCIe EEPROM switch setting

The default PCIe EEPROM switch setting alters the micro switch configuration by providing the port LEDs I2C address of GPIO expander, for the PCIe switch to update automatically the status LEDs of the ports. It also turn off the front orange LED as an indication that the PCIe switch has correctly downloaded its EEPROM. Finally, it sets Subsystem ID and vendor ID to Kontron IDs. The binary content is the following:

```
0x0003E000 0x00000008 ;SWCTL register with Register Unlock[3:3] enabled
0x0003F1A8 0x4e404800 ; activate trafic LEDs
0x0003F178 0x00000040 ; set GPIO dir to turn off front orange reset LED
0x0003F174 0x00000040 ; set GPIO value to turn off front orange reset LED
0x000000F4 0x90101059 ; SSID and SSVID values
0x000000C0 0xC803F001 ; Power MGMT capabilities pointing to F0
0x0003E000 0x00000000 ; SWCTL register with Register Unlock[3:3] disabled
```

Kontron can provide a Linux utility named `switch_3905_cfg` to alter the default PCIe switch EEPROM content. This software is provided "as is" with no support on the specific EEPROM configuration results that could be built. The EEPROM binary files must be generated by the IDT utility PCIeBrowser.

Some examples are provided below to operate the `switch_3905_cfg` utility:

```
./switch_3905_cfg --help
.
Usage ./switch_3905_cfg -E OR -e OR -W [-f <Filename> ] [-c] Options are :
[-E   ] : Read the content of the EEPROM into a file
[-e   ] : Displays the EEPROM content into an ASCII format
[-W   ] : WRITE the content of a binary DATA file into the  EEPROM
[-f   ] : Specify the FILE NAME which will contain the DATA of the EEPROM  (
DEFAULT = /tmp/EEPROMBinFile )
[-c   ] : Control the validity of the EEPROM  content
[-d   ] : Enable the debug mode

./switch_3905_cfg  -E
EEPROM data read successfully into file /tmp/EEPROMBinFile

  od -x /tmp/EEPROMBinFile
0000000 6aff 00fc 4048 e04e ffe3 ffff ffff ffff 0000020 ffff ffff ffff ffff ffff ffff ffff ffff

./switch_3905_cfg  -W -c
EEPROM updated from the binary file /tmp/EEPROMBinFile
  Control successful
```

Chapter 2 - Installation

The VX3905 has been designed for easy installation. However, the following standard precautions, installations procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

2.1 Safety Requirements

The following safety precautions must be observed when installing or operating the VX3905. Kontron assumes no responsibility for any damage resulting from

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

ESD Equipment!

This VPX board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- When unpacking a static-sensitive component from its shipping carton, do not remove the component's antistatic packing material until you are ready to install the component in a computer. Just before unwrapping the antistatic packaging, be sure you are at an ESD workstation or grounded. This will discharge any static electricity that may have built up in your body.
- When transporting a sensitive component, first place it in an antistatic container or packaging.
- Handle all sensitive components at an ESD workstation. If possible, use antistatic floor pads and workbench pads.
- Handle components and boards with care. Don't touch the components or contacts on a board. Hold a board by its edges or by its metal mounting bracket. Do not handle or store system boards near strong electrostatic, electromagnetic, magnetic, or radioactive fields.

2.2 VX3905 Identification

The VX3905 boards are identified by labels fitted to the top side.

A "Order Code, Variant, Serial Number and E.C. Level" labels (Text and 2D versions available).

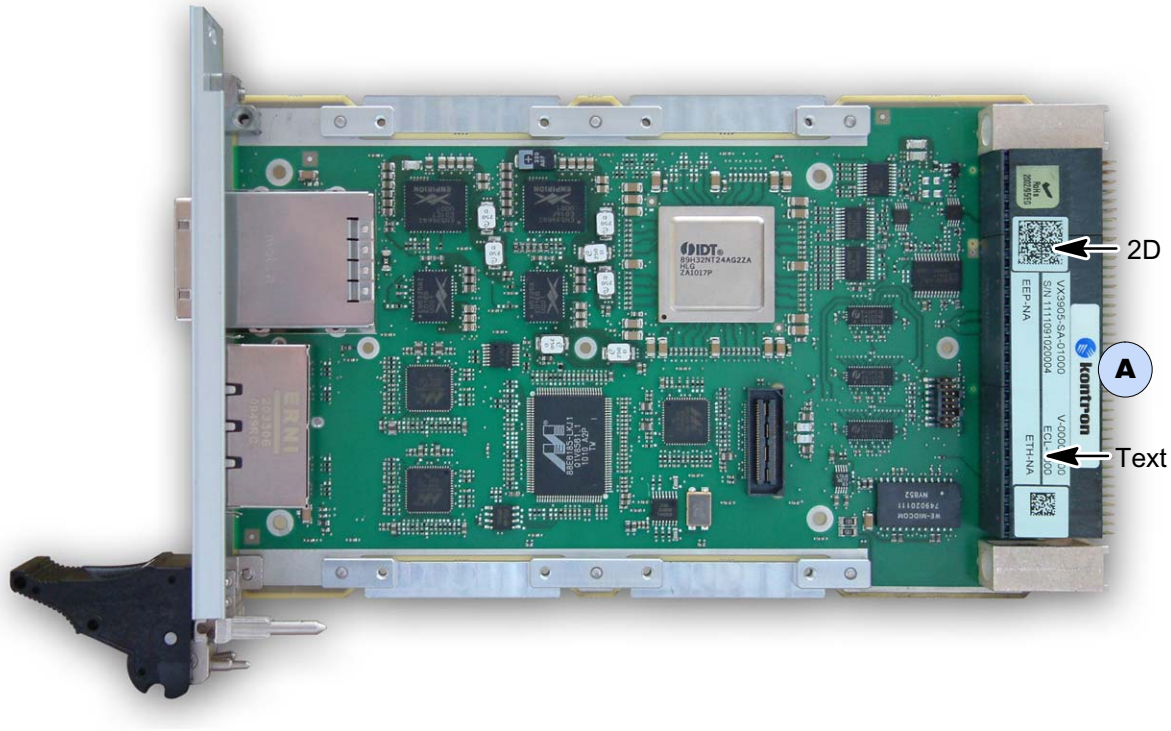

Figure 2: VX3905 Identification (Top Side)

2.3 VX3905 Configuration

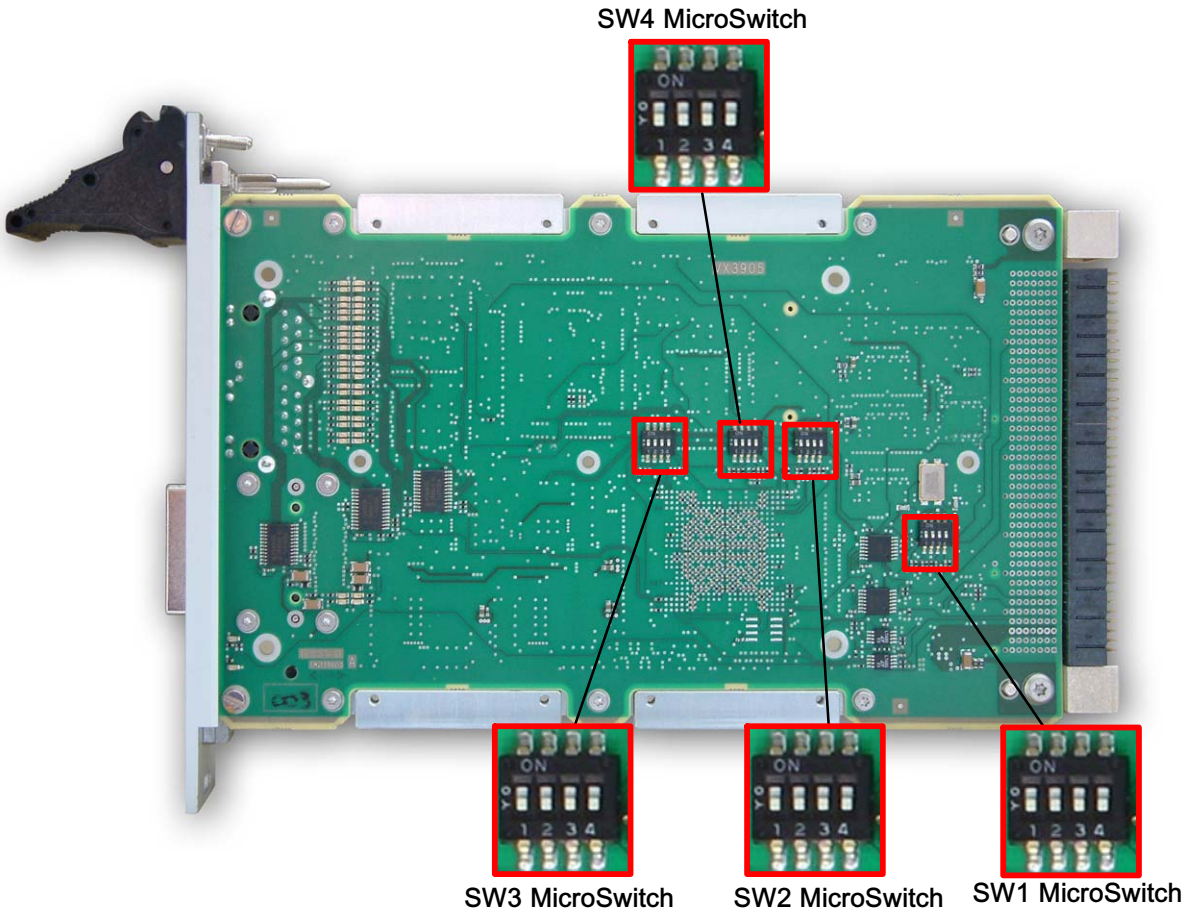

Figure 3: Microswitches Location

Microswitches are not used for the Ethernet only option, except SW4.3.

2.3.1 SW1 Microswitch Description

Function	Description
1 - Reserved	Shall be OFF
2 - Reserved	Shall be OFF
3 - Reserved	Shall be OFF
4 - Reserved	Shall be OFF

Table 3: SW1 Microswitch Description

2.3.2 SW2 Microswitch Description

Function					Description
SW	2.4 OFF	2.3 OFF	2.2 OFF	2.1 OFF	Single PCIe switch partition, ignore EEPROM content. Use this configuration to ignore the EEPROM content or when there is a doubt on the EEPROM content.
	OFF	OFF	OFF	ON	Single PCIe switch partition, use EEPROM content. Factory default configuration.
	OFF	OFF	ON	OFF	Single PCIe switch partition, use EEPROM content at JUMP 0
	OFF	OFF	ON	ON	Single PCIe switch partition, use EEPROM content at JUMP 1
Other combinations					Reserved

Table 4: SW2 Microswitch Description

when the EEPROM content is used, the switch registers are first configured as per the hardware straps SW3, then the EEPROM content may be used to alter these registers to a different configuration before the switch is ready to operate.

2.3.3 SW3 Microswitch Description

Function					Description
SW	3.4 OFF	3.3 OFF	3.2 OFF	3.1 OFF	All PCIe ports of the switch are x4 (total of 8 switch ports)
	OFF	OFF	ON	OFF	All PCIe ports of the switch are x2 (total of 16 switch ports). If used, the PCIe x4 cable port becomes a non standard 2 port x2 cable (with a single set of sideband signals like reset* and common reference clock).
	ON	ON	ON	OFF	16 PCIe ports x1 (P1 wafers 9-16 and P2 wafers 1-8), all other PCIe ports x2.
Other combinations					Reserved; PCIe x8 ports and non uniform port sizes are accessible through programmation of the PCIe EEPROM

Table 5: SW3 Microswitch Description

2.3.4 SW4 Microswitch Description

Function	Description
SW4.1	Reserved, shall be **OFF**
SW4.2	Reserved, shall be **OFF**
SW4.3	**OFF**: write protect of EEPROMs according VPX backplane NVMRO signal **ON**: allow write to EEPROMs
SW4.4	**OFF**: enable PCIe switch slave i2c interface to be visible on the VPX (VPX i2c pins P0-B5 for Clock and P0-A5 for Data) **ON**: PCIe switch slave i2C interface not connected to VPX This setting can be overridden with software or EEPROM by programming GPIO7 and GPIO8 of the PCIe switch.

Table 6: SW4 Microswitch Description

2.4 VX3905 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the VX3905 in a system. Procedures for standard removal operations are found in section 2.5 Standard Removal Procedures

To perform an initial installation of the VX3905 in a system proceed as follows:

1. Ensure that the safety requirements indicated in section 2.1 Safety Requirements are observed.

   
   Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the VX3905 refer to the CLI Reference Manual.

   
   Care must be taken when applying the procedures below to ensure that neither the VX3905 nor other system boards are physically damaged by the application of these procedures.

3. To install the VX3905 perform the following:
   - > Ensure that no power is applied to the system before proceeding.
   - > Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.

     
     DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

   - > Using both ejector handles, engage the board with the backplane. When the ejector handles are locked, the board is engaged.
   - > Fasten the front panel retaining screws.
   - > Connect all external interfacing cables to the board as required.
   - > Ensure that the board and all required interfacing cables are properly secured.

4. The VX3905 is now ready for operation.

2.5 Standard Removal Procedures

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in section 2.1 Safety Requirements are observed.

   
   Care must be taken when applying the procedures below to ensure that neither the VX3905 nor other system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.

   
   Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.
7. Dispose of the board as required.

Chapter 3 - Functional Description

The board is composed of the following building blocks:

- Ethernet Switch
- PCI Express Switch

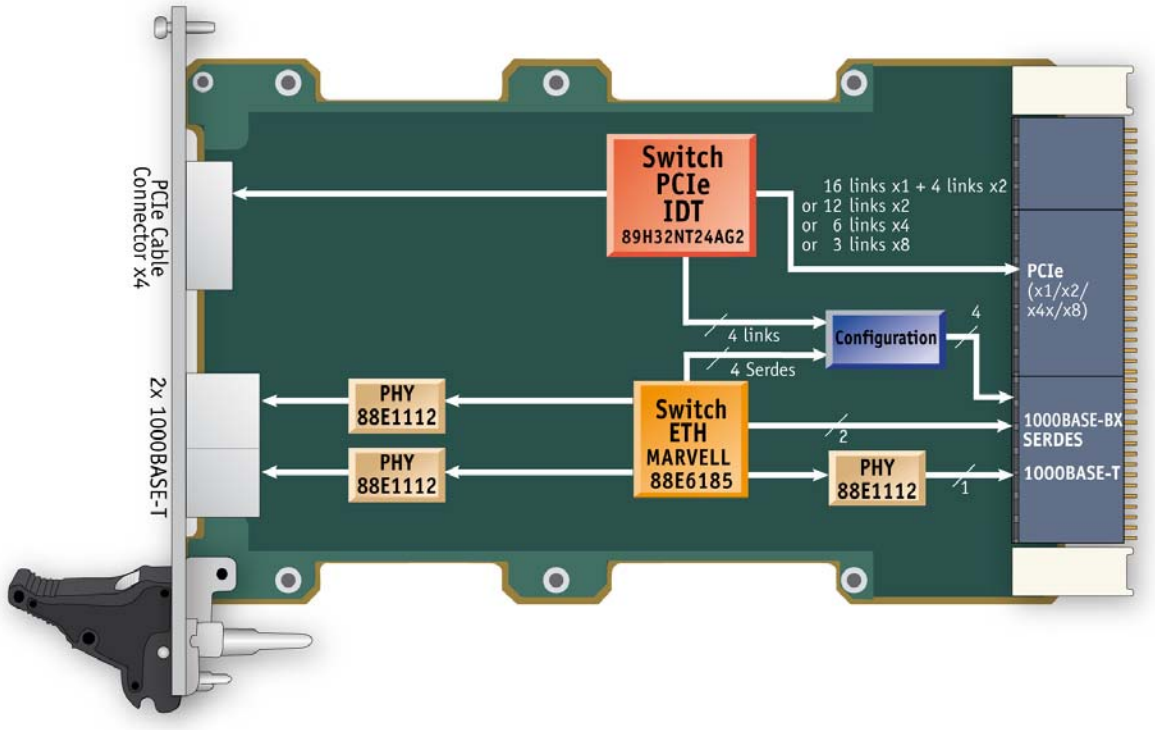

Figure 4: Block Diagram VX3905

For clarity, configurations with 32 PCIe lanes on the backplane (no Ethernet), with incomming SATA links, with no PCIe lanes or with PCIe common reference clock generator on the backplane are not represented on the diagram. Please refer to the VPX connector pin assignment tables for these configurations.

3.1 Ethernet Switch

The Gigabit Ethernet switch device is a Marvell 88E6185. The 88E6185 is a 10 port highly integrated multilayer Ethernet switch with the following Features:

- Up to 10 ports, 1 GbE
- 8K MAC address entries with automatic learning and aging
- 802.1Q VLAN support for full 4096 VLAN IDs

Table 7 describes the Ethernet switch port mapping

Ports	Connectivity	Interface
CH0	Front RJ-45, ETH B	1000BASE-T
CH1	P2 wafer 9	1000BASE-BX
CH2	P2 wafer 10	1000BASE-BX
CH3	Front RJ-45, ETH A	1000BASE-T
CH4	P2 wafer 11	1000BASE-BX
CH5	P2 wafer 12	1000BASE-BX
CH6	P2 wafer 15-16	1000BASE-T
CH7	P2 wafer 13	1000BASE-BX
CH8	P2 wafer 14	1000BASE-BX
CH9	P2 single ended contact 15/13/11/9 (1)	1000BASE-BX

(1) CH9 is available only for VX3905 with minimum EC Level 30000

Table 7: 88E6185 Port Mapping

3.2 PCI Express Switch

The PCI Express switch device is a 89H32NT24AG2 from IDT. It is a 32 lanes 24 ports PCIe gen2 switch device with the following features:

- up to 32 lanes, 24 ports, PCIe gen2 and gen1
- up to 256 Gbits/s switching capacity
- 128 Bytes to 2 KBytes payload size
- low latency cut-through architecture
- port size configurability from x2 to x8 on all lanes, x1 capability on 16 lanes
- supports automatic lane reversal
- automatic per port link width negociation

This section does not apply to the Ethernet only version of VX3905 (rear I/O option E).

Table 8 below describes PCIe switch port mapping.

Switch Device port_lane	OpenVPX Signal Name (1)	VPX Wafer	Front PCIe Connector (1)
PE0_0	PCIE01-0	P1.1	
PE0_1	PCIE01-1	P1.2	
PE1_0	PCIE01-2	P1.3	
PE1_1	PCIE01-3	P1.4	
PE2_0	0/1/2/S: PCIE02-0	P1.5	
PE2_1	0/1/2/S: PCIE02-1	P1.6	
PE3_0	0/1/2/S: PCIE02-2	P1.7	
PE3_1	0/1/2/S: PCIE02-3	P1.8	
PE23_0	0/1/2/A: PCIE03-0	P1.9	
PE22_0	0/1/2/A: PCIE03-1	P1.10	
PE21_0	PCIE03-2	P1.11	
PE20_0	PCIE03-3	P1.12	
PE19_0	PCIE04-0	P1.13	
PE18_0	PCIE04-1	P1.14	
PE17_0	PCIE04-2	P1.15	
PE16_0	PCIE04-3	P1.16	
PE15_0	PCIE05-0	P2.1	
PE14_0	PCIE05-1	P2.2	
PE13_0	PCIE05-2	P2.3	
PE12_0	PCIE05-3	P2.4	
PE11_0	PCIE06-0	P2.5	
PE10_0	PCIE06-1	P2.6	
PE9_0	PCIE06-2	P2.7	
PE8_0	PCIE06-3	P2.8	

Switch Device port_lane	OpenVPX Signal Name (1)	VPX Wafer	Front PCIe Connector (1)
PE7_1	1/2: PCIE07-0	P2.9	
PE7_0	1/2: PCIE07-1	P2.10	
PE6_1	1/2: PCIE07-3	P2.11	
PE6_0	1/2: PCIE07-4	P2.12	
PE5_1	2: PCIE08-0	P2.13	0/1/A/B/S: PCIE08-0
PE5_0	2: PCIE08-1	P2.14	0/1/A/B/S: PCIE08-1
PE4_1	2: PCIE08-2	P2.15	0/1/A/B/S: PCIE08-2
PE4_0	2: PCIE08-3	P2.16	0/1/A/B/S: PCIE08-3

(1): the signal name may be preceded by the rear I/O type order codes when the presence of this signal depends on it.

Table 8: PCIe Switch Port Mapping

The upstream port is always port 0 starting on wafer 1 of VPX connector P1; its width varies depending on the micro-switch settings or the EEPROM content. If the EEPROM content declares more than a single switch partition, there may be multiple upstream ports.

The PCIe switch features 9 General Purpuse Inputs/Outputs (GPIO) accessible from the upstream root complex port. Table 9 below indicates the usage of these GPIOs. By default, all GPIOs are set as high impedance inputs after reset.

GPIO number	Description
GPIO 0/1/2:	Connected to microwire serial interface of Ethernet switch EEPROM, respectively DO/ DI/CK. May be used to reprogram the default Ethernet EEPROM. The Ethernet section of the VX3905 should be kept in reset while reprogramming the EEPROM, see GPIO 5. The Backplane NVMRO signal or the NVMRO microswitch should allow EEPROM writes. The EEPROM is of type M93S66. The software should manually sequence the microwire signals to perform an access.
GPIO 3/4:	Connected respectively to MDIO_CPU/MDC_CPU SMI bus of the ethernet switch. When used, drive actively 0 or keep in high impedance for getting 1 with the external pull up resistors, for voltage compatibility.
GPIO 5:	Ethernet section reset of VX3905. Drive to 0 to activate the reset. Drive 1 or do not drive to release reset. The card reset from the VPX (SYSRESET* or MASKABLE RESET*) also reset the Ethernet section.
GPIO 6:	Input (when not driven): 0 indicates a PCIe cable device is not present; 1 indicates the presence of a PCIe device on the x4 cable interface. Output: drive 0 to activate the PCIe cable reset* output. Otherwise, keep high impedance input mode.
GPIO 7/8:	Output: drive 0 to disable PCIe switch slave SMB/I2C interface from respectively VPX SMB 0 and 1. Microswitch SW4.4 might also be used to disconnect the PCIe switch slave SMB/I2C interface from the VPX SMB 0. Output: drive 1 to connect the PCIe switch slave interface SMB/I2C to respectively VPX SMB 0 or 1. Do not drive both GPIO 7 and 8 to 1. Output high impedance: PCIe switch slave interface SMB/I2C connected to VPX SMB 0 or disconnected according to SW4.4 microswitch. Input: 1 if the PCIe switch slave interface is connected to SMB 0, respectively SMB 1. 0 otherwise. When enabled, the PCIe switch slave SMB/I2C interface will have a seven bit I2C address of 0x76 if the slot geographical address bit GA0 indicates an odd slot number, or 0x77 if the slot geographical address bit GA0 indicates an even slot number.

Table 9: Usage of GPIOs

3.3 Board Interfaces

3.3.1 Status LEDs

Figure 5: Front Panel Status LEDs of the VX3905

Status LEDs

- **RST LED**: orange LED, ON when the board is in reset state, or when the PCIe x4 cable interface is reset by software from GPIO 6.
- **PWR LED**: green LED, ON when the VPX +5V power is present and the internal VX3905 voltages have reached their normal operating states.

3.3.2 Front Panel Ports

Figure 6: Front Panel Ports of the VX3905

- 2x 10/100/1000BASE-T for GbE front panel Interfaces (RJ45 connectors), see section 3.3.2.1 “Copper Uplinks” page 19.
- 1 PCIe x4 cable interface, see section 3.3.2.2 “PCIe x4 cable connector” page 20

3.3.2.1 Copper Uplinks

The Ethernet transmission operates using a CAT5 cable with a maximum length of 100 m.

The VX3905-SA supports two 10/100/1000BASE-T RJ45 fabric switch uplinks to the front panel. The switch is connected to the RJ45 connectors with integrated magnetics and status LEDs on the front panel via external PHYs.

The RJ-45 connectors have the following pin assignment.

PIN	1000BASE-T	
	I/O	SIGNAL
1	I/O	BI_DA+
2	I/O	BI_DA-
3	I/O	BI_DB+
4	I/O	BI_DC+
5	I/O	BI_DC-
6	I/O	BI_DB-
7	I/O	BI_DD+
8	I/O	BI_DD-

Table 10: Cooper Uplinks Connector Pin Assignment

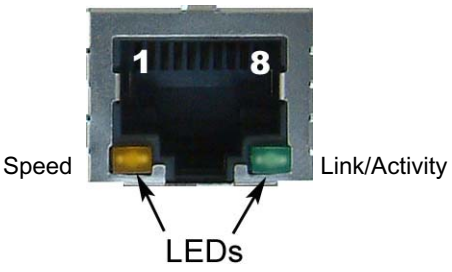

Figure 7: Copper Uplinks Connector

Ethernet LEDs Signification

STATUS		SPEED LED Yellow	ACTIVITY LED Green
Ethernet Link is not established		OFF	OFF
10/100 Mbps	Ethernet Link Established	ON	ON
	Ethernet Link Activity	BLINK	BLINK
1000 Mbps	Ethernet Link Established	OFF	ON
	Ethernet Link Activity	OFF	BLINK

Table 11: Ethernet LEDs Signification

3.3.2.2 PCIe x4 cable connector

The PCIe cable interface is compliant with PCI Express External Cabling Specification Revision 1.0, for x4 width interface. It is a 38 pin connector, the pin assignment is shown in Table 12 below. The function is not available when the rear I/O ordering code is 2. This connector is not present on the Ethernet only version of VX3905.

	A	B
1	GND	GND
2	PCIE08-TD3+	PCIE08-RD3+
3	PCIE08-TD3-	PCIE08-RD3-
4	GND	GND
5	PCIE08-TD2+	PCIE08-RD2+
6	PCIE08-TD2-	PCIE08-RD2-
7	GND	GND
8	PCIE08-TD1+	PCIE08-RD1+
9	PCIE08-TD1-	PCIE08-RD1-
10	GND	GND
11	PCIE08-TD0+	PCIE08-RD0+
12	PCIE08-TD0-	PCIE08-RD0-
13	GND	GND
14	PCIE08-CLK+	PWR
15	PCIE08-CLK-	PWR
16	GND	GND
17	GND	GND
18	CPRSNT*	N.C.
19	CPWRON	CPERST*

Table 12: PCIe Cable Interface Pin Assignment

3.3.3 Backplane Connectors

The complete 3U VPX connector configuration comprises three connectors named P0 to P2.

- P0: 8-wafer 7-row connector.
- P1 to P2: 16-wafer 7-row differential connectors.

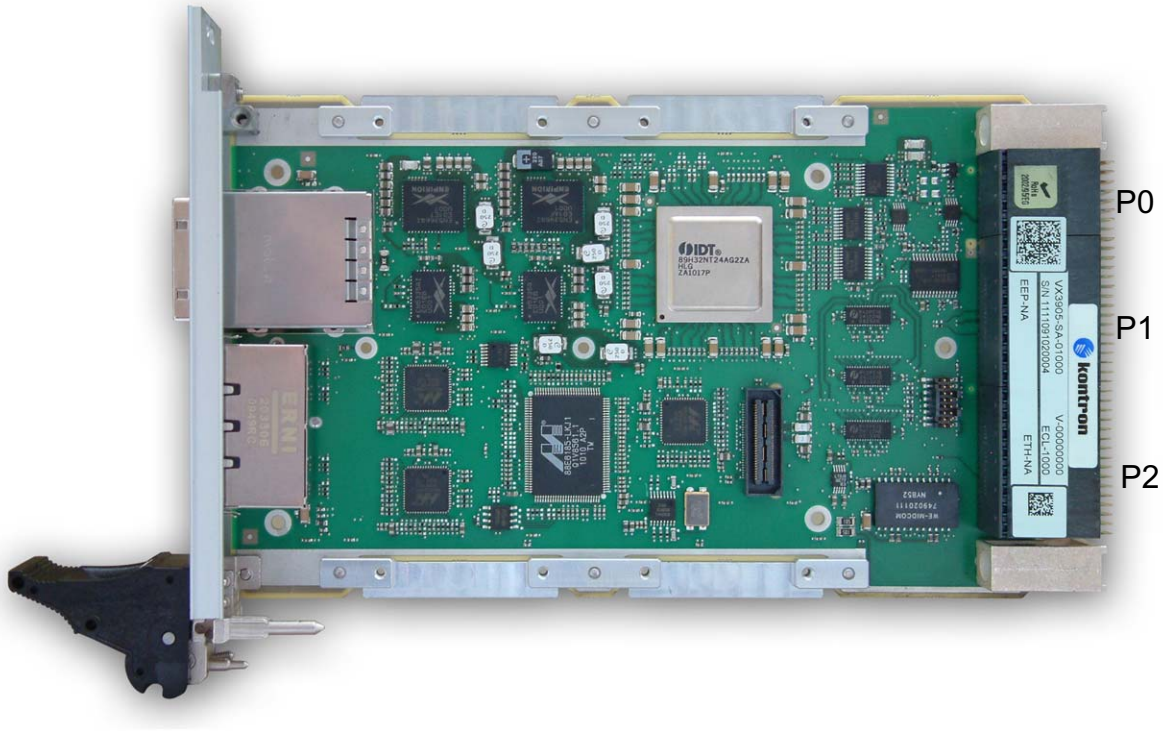

Figure 8: Backplane Connectors

3.3.3.1 P0 Connector

P0 Wafer Assignment

P0 Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	NC (+12V)	NC (+12V)	NC (+12V)	NC	NC (+3V3)	NC (+3V3)	NC (+3V3)
2	NC (+12V)	NC (+12V)	NC (+12V)	NC	NC (+3V3)	NC (+3V3)	NC (+3V3)
3	+5V	+5V	+5V	NC	+5V	+5V	+5V
4	SMB1 CLK	SMB1 DAT	GND	NC (-12V_AUX)	GND	SYSRESET*	NVMRO
5	N.C. (GAP*)	N.C. (GA4*)	GND	N.C. (3V3_AUX)	GND	SMB0 CLK	SMB0 DAT
6	N.C. (GA3*)	N.C. (GA2*)	GND	N.C. (-12V_AUX)	GND	N.C. (GA1*)	GA0*
7	N.C. (TCK)	GND	PCIe_CLK+ (TDO)	PCIe_CLK+ (TDI)	GND	N.C. (TMS)	N.C. (TRST*)
8	GND	N.C. (REF_CLK-)	N.C. (REF_CLK+)	GND	N.C. (AUX_CLK-)	N.C. (AUX_CLK+)	GND
CASE	GND						

* signal active when low

Table 13: VPX Connector P0 Wafer Assignment

P0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
+5V	+5 Volts DC power (VS3 VPX supply)
GA0*	Geographical Address Pin 0, used to determined slave i2c address of PCIe switch
GND	Ground
N.C. (Signal)	Not Connected, (Signal) is the VPX/OpenVPX standard signal on this pin
NVMRO	Non-Volatile Memory Read Only. When asserted (logical 1), prevents any non-volatile memory from being updated.
PCIe_CLK+/-	100 MHz PCIe Common Reference Clock Input, optional
SMB0	System Management Bus 0, I2C protocol
SMB1	System Management Bus 1, I2C protocol
SYSRESET*	System Reset. Input and open collector output.

Table 14: VPX Connector P0 Signal Definition

3.3.3.2 P1 Connector

P1 Wafer Assignment

Depending on the manufacturing option Rear I/O type, the P1 wafer assigment differs.

Table 15 details the P1 wafer assignment Rear I/O type 0 standard OpenVPX default option: VITA65 slot profile SLT3-SWH-6F6U-14.4.1 and module profile MOD3-SWH-6F6U-16.4.1-3.

Table 17 list the P1 pin assignment changes when another configuration is used.

P1 Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	N.C. (GDiscrete1)	GND	PCIE01-TD0-	PCIE01-TD0+	GND	PCIE01-RD0-	PCIE01-RD0+
2	GND	PCIE01-TD1-	PCIE01-TD1+	GND	PCIE01-RD1-	PCIE01-RD1+	GND
3	N.C. (P1-VBAT)	GND	PCIE01-TD2-	PCIE01-TD2+	GND	PCIE01-RD2-	PCIE01-RD2+
4	GND	PCIE01-TD3-	PCIE01-TD3+	GND	PCIE01-RD3-	PCIE01-RD3+	GND
5	N.C. (SYS-CON*)	GND	PCIE02-TD0-	PCIE02-TD0+	GND	PCIE02-RD0-	PCIE02-RD0+
6	GND	PCIE02-TD1-	PCIE02-TD1+	GND	PCIE02-RD1-	PCIE02-RD1+	GND
7	N.C. (Reserved)	GND	PCIE02-TD2-	PCIE02-TD2+	GND	PCIE02-RD2-	PCIE02-RD2+
8	GND	PCIE02-TD3-	PCIE02-TD3+	GND	PCIE02-RD3-	PCIE02-RD3+	GND
9	MSMBCLK (UD)	GND	PCIE03-TD0-	PCIE03-TD0+	GND	PCIE03-RD0-	PCIE03-RD0+
10	GND	PCIE03-TD1-	PCIE03-TD1+	GND	PCIE03-RD1-	PCIE03-RD1+	GND
11	MSMBDAT (UD)	GND	PCIE03-TD2-	PCIE03-TD2+	GND	PCIE03-RD2-	PCIE03-RD2+
12	GND	PCIE03-TD3-	PCIE03-TD3+	GND	PCIE03-RD3-	PCIE03-RD3+	GND
13	Ethreset* (1) (UD)	GND	PCIE04-TD0-	PCIE04-TD0+	GND	PCIE04-RD0-	PCIE04-RD0+
14	GND	PCIE04-TD1-	PCIE04-TD1+	GND	PCIE04-RD1-	PCIE04-RD1+	GND
15	Maskable Reset*	GND	PCIE04-TD2-	PCIE04-TD2+	GND	PCIE04-RD2-	PCIE04-RD2+
16	GND	PCIE04-TD3-	PCIE04-TD3+	GND	PCIE04-RD3-	PCIE04-RD3+	GND
CASE	GND						

* signal active when low

Table 15: VPX Connector P1 Wafer Assignment (Rear I/O type 0)

MNEMONIC	SIGNAL DEFINITION
PCIExx-TDyy+/- PCIExx-RDyy+/-	PCI Express transmit and receive differential pairs as seen from the point of view of the VX3905. These ports are numbered as x4 PCIe ports as described in the OpenVPX standard. When the switch is configured for x2 operation, then each xx port is replaced by two ports made of the first two lanes followed the two last lanes. In a similar principle, the ports can be configured as x8. For x1 operation, only lanes belonging to wafer 9 to 16 have the capabilities to operate as 8 x1 ports, the first 8 lanes remaining in x2 mode at least.
MaskableReset*	Optional reset input for this module. May be left unconnected if not used. Same effect as SYSRESET* P0 input. Unlike SYSRESET*, MaskableReset* is generally not bussed across backplane slots, allowing individual card reset.
EthReset*	Copy of the internal Reset* signal applied to the Ethernet switch and PHYs.
MSMBCLK, MSMBDAT	Copy of VX3905 internal Master I2C bus of the PCIe switch device. May be used to duplicate PCIe activity LEDs on the rear, or to implement other utility fonctions controlled by the PCIe switch on its master I2C interface, such as PCIe hot swap signalling.
N.C. (Signal)	Not Connected, (Signal) is the VPX/OpenVPX standard signal on this pin
(UD)	Pin defined as User Defined by the VPX/OpenVPX standard
GND	Ground
Reserved	Reserved. Do not connect.

Table 16: VPX Connector P1 Signal Definition

The P1 connector is not equipped on the Ethernet only version of VX3905 (rear I/O option E)

Table 17 below describes changes superseding P1 pin assignment of Table 15 for rear I/O type order codes A, B or S only.

P1 Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1							
2							
3							
4							
5			A/B: CCLK0-	A/B: CCLK0+		A/B: CCLK1-	A/B: CCLK1+
6		A/B: CCLK2-	A/B: CCLK2+		A/B: CCLK3-	A/B: CCLK3+	
7			A/B: CCLK4-	A/B: CCLK4+		A/B: CCLK5-	A/B: CCLK5+
8		A/B: CCLK6-	A/B: CCLK6+		A/B: CCLK7-	A/B: CCLK7+	
9			B/S: SATA0T-	B/S: SATA0T+		B/S: SATA0R-	B/S: SATA0R+
10		B/S: SATA1T-	B/S: SATA1T+		B/S: SATA1R-	B/S: SATA1R+	
11							
12							
13							
14							
15							
16							
CASE	GND						

Table 17: VPX Connector P1 pin assignment changes depending on rear I/O type order code

It is recommended to use the SATA link 0 when using the SATA carrier option B or S.

3.3.3.3 P2 Connector

P2 Wafer Assignment

Depending on the manufacturing option Rear I/O type the P2 wafer assignment differs.

Table 18 details the P2 wafer assignment Rear I/O type 0 standard OpenVPX default option: VITA65 slot profile SLT3-SWH-6F6U-14.4.1 and module profile MOD3-SWH-6F6U-16.4.1-3.

Table 20 list the P2 pin assignment changes when another configuration is used

P2 Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	RXD_RS232 (1) (UD)	GND	PCIE05-TD0-	PCIE05-TD0+	GND	PCIE05-RD0-	PCIE05-RD0+
2	GND	PCIE05-TD1-	PCIE05-TD1+	GND	PCIE05-RD1-	PCIE05-RD1+	GND
3	TXD_RS232 (1) (UD)	GND	PCIE05-TD2-	PCIE05-TD2+	GND	PCIE05-RD2-	PCIE05-RD2+
4	GND	PCIE05-TD3-	PCIE05-TD3+	GND	PCIE05-RD3-	PCIE05-RD3+	GND
5	ETH_MDIO (UD)	GND	PCIE06-TD0-	PCIE06-TD0+	GND	PCIE06-RD0-	PCIE06-RD0+
6	GND	PCIE06-TD1-	PCIE06-TD1+	GND	PCIE06-RD1-	PCIE06-RD1+	GND
7	ETH_MDC (UD)	GND	PCIE06-TD2-	PCIE06-TD2+	GND	PCIE06-RD2-	PCIE06-RD2+
8	GND	PCIE06-TD3-	PCIE06-TD3+	GND	PCIE06-RD3-	PCIE06-RD3+	GND
9	ETHBXCH9_RX- (2) (UD)	GND	ETH6-TD-	ETH6-TD+	GND	ETH6-RD-	ETH6-RD1+
10	GND	ETH5-TD-	ETH5-TD+	GND	ETH5-RD-	ETH5-RD+	GND
11	ETHBXCH9_RX+ (2) (UD)	GND	ETH4-TD-	ETH4-TD+	GND	ETH4-RD-	ETH4-RD+
12	GND	ETH3-TD-	ETH3-TD+	GND	ETH3-RD-	ETH3-RD+	GND
13	ETHBXCH9_TX- (2) (UD)	GND	ETH2-TD-	ETH2-TD+	GND	ETH2-RD-	ETH2-RD+
14	GND	ETH1-TD-	ETH1-TD+	GND	ETH1-RD-	ETH1-RD+	GND
15	ETHBXCH9_TX+ (2) (UD)	GND	ETH01-DB- (UD)	ETH01-DB+ (UD)	GND	ETH01-DA- (UD)	ETH01-DA+ (UD)
16	GND	ETH01-DD- (UD)	ETH01-DD+ (UD)	GND	ETH01-DC- (UD)	ETH01-DC+ (UD)	GND
CASE	GND						

* signal active when low

(1) This single ended pin function is available only for vx3905 with minimum EC Level 30000.

(2) ETHBXCH9 1000BaseBX additionnal channel is availabe only for vx3905 with minimum EC Level 30000

Table 18: VPX Connector P2 Wafer Assignment (Rear I/O type 0)

The P2 connector signals related to PCIe are not implemented on the Ethernet only version of VX3905 (rear I/O option E).

MNEMONIC	SIGNAL DEFINITION
PCIExx-TDyy+/- PCIExx-RDyy+/-	PCI Express transmit and receive differential pairs as seen from the point of view of the VX3905. These ports are numbered as x4 PCIe ports as described in the OpenVPX standard. When the switch is configured for x2 operation, then each xx port is replaced by two ports made of the first two lanes followed the two last lanes. In a similar principle, the ports can be configured as x8. For x1 operation, only lanes belonging to wafer 1 to 8 have the capabilities to operate as 8 x1 ports.
ETHx-TD+/- ETHx-RD+/-	Ethernet 1000Base-BX serdes transmit and receive differential pairs as seen from the point of view of the VX3905.
Eth01-DA/DB/ DC/DD+/-	Ethernet 1000Base-T differential pairs
ETH_MDIO / ETH_MDC	Standard SMI bus driven by the Ethernet switch to configure its PHYs
N.C. (Signal)	Not Connected, (Signal) is the VPX/OpenVPX standard signal on this pin
(UD)	Pin defined as User Defined by the VPX/OpenVPX standard
GND	Ground
Reserved	Reserved. Do not connect.

Table 19: VPX Connector P2 Signal Definition

Table 20 below describes changes superseding P2 pin assignment of Table 18 for rear I/O type order codes 1 or 2 only

P2 Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1							
2							
3							
4							
5							
6							
7							
8							
9			1/2:PCIE07-TD0-	1/2:PCIE07-TD0+		1/2:PCIE07-RD0-	1/2:PCIE07-RD0+
10		1/2:PCIE07-TD1-	1/2:PCIE07-TD1+		1/2:PCIE07-RD1-	1/2:PCIE07-RD1+	
11			1/2:PCIE07-TD2-	1/2:PCIE07-TD2+		1/2:PCIE07-RD2-	1/2:PCIE07-RD2+
12		1/2:PCIE07-TD3-	1/2:PCIE07-TD3+		1/2:PCIE07-RD3-	1/2:PCIE07-RD3+	
13			2:PCIE08-TD0-	2:PCIE08-TD0+		2:PCIE08-RD0-	2:PCIE08-RD0+
14		2:PCIE08-TD1-	2:PCIE08-TD1+		2:PCIE08-RD1-	2:PCIE08-RD1+	
15			2:PCIE08-TD2-	2:PCIE08-TD2+		2:PCIE08-RD2-	2:PCIE08-RD2+
16		2:PCIE08-TD3-	2:PCIE08-TD3+		2:PCIE08-RD3-	2:PCIE08-RD3+	
CASE	GND						

* signal active when low

Table 20: VPX Connector P2 pin assignment changes depending on rear I/O type order code

- When using rear I/O type order code of 2, the front panel PCIe express cable is not connected.
- When using rear I/O type 1 or 2, the signal quality of PCIE08 lanes (and to a lesser extent of PCIE07 lanes) on the VPX P2 connector may not be as good as for the remaining lanes of the VPX connector, because of additional rear I/O type multiplexing and trace lengths. Operation at gen1 speed should not be impacted. Operation margin at gen2 speed may depend on the length and routing quality on the backplane.

3.4 Microcontroller Function

For VX3905 with a minimum EC level of 30000, a microcontroller is available to program the port mirroring function of the switch from a simplified EIA-232 RX/TX interface operating at 115200 Bauds. The asynchronous link operates with 8-bit data, 1 start bit and 1 stop bit.

The EIA-232 RX and TX signals are available on the VPX P2 connector. When the card type is E (Ethernet only switch), the serial link is also available on the front panel as an RJ-11 connector with the pin assignment described below.

PIN	SIGNAL
1	NC
2	Shell
3	TXD
4	RXD
5	GND
6	NC

Table 21: Serial Connector Pin Assignment

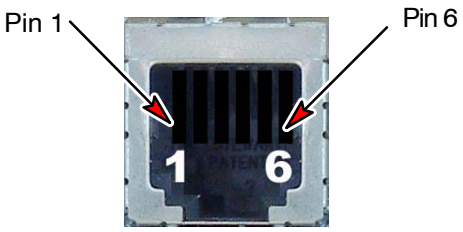

Figure 9: Serial Connector

For more details about the user commands available from the firmware, please refer to document FT.DT.988, "VX3905 Ethernet Switch Firmware User Manual".

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