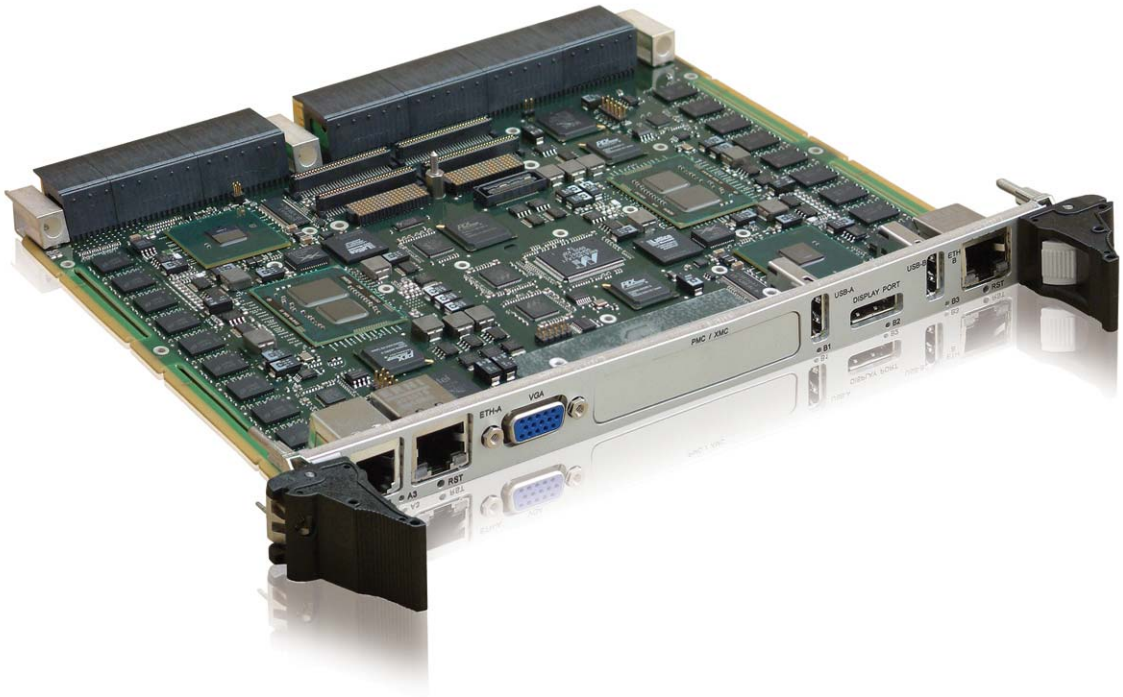
» VX6060 «



6U VPX Computing Node
User's Guide

CA.DT.A76-3e - August 2011

Revision History

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Rev.	Brief Description of Changes	Date of Issue
3e	Update of Ethernet leds Status definition, I2C board control CPLD register definition, and Onboard SATA port number.	08-2011
2e	Additional Features	03-2011
1e	Remove unsupported features	12-2010
0e	Preliminary Version	10-2010

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- reduce waste arising from electrical and electronic equipment (EEE)
- make producers of EEE responsible for the environmental impact of their products, especially when they become waste
- encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- improve the environmental performance of all those involved during the lifecycle of EEE

Conventions

This guide uses several types of notice: Note, Caution, ESD.

Note: this notice calls attention to important features or instructions.


Caution: this notice alert you to system damage, loss of data, or risk of personal injury.


ESD: This banner indicates an Electrostatic Sensitive Device.

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. The prefix `0x' shows a hexadecimal number, following the `C' programming language convention.

The multipliers `k', `M' and `G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when `K', `M' and `G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

When describing transfer rates, `k' `M' and `G' mean $*10^3$, $*10^6$ and $*10^9$ *not $*2^{10}$ $*2^{20}$ and $*2^{30}$.*

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and CompactPCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Signal names ending with an asterisk (*) or a hash (#) denote active low signals; all other signals are active high.

Signal names follow the PICMG 2.0 R3.0 CompactPCI Specification and the PCI Local Bus 2.3 Specification.

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Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions


Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.


Caution, Electric Shock!
Before installing a not hot-swappable Kontron product into a system always ensure that your mains power is switched off. This applies also to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing work.

Special Handling and Unpacking Instructions

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the board is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the board.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the device, which are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This device should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This applies also to the operational temperature range of the specific board version, which must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, please follow only the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the board, please re-pack it as nearly as possible in the manner in which it was delivered.

Special care is necessary when handling or unpacking the product. Please consult the special handling and unpacking instruction on the previous page of this manual.

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Chapter 1 - Introduction

The Kontron VX6060 is an innovative VPX computing blade for parallel data and signal processing applications in the communications, military, aerospace, medical, industrial, and infotainment markets.

With two independently implemented Intel® Core™ i7 processing nodes linked to a powerful Ethernet and PCIe infrastructure, the Kontron VPX blade VX6060 is the ideal building block for intensive parallel computing workloads where a cluster of Kontron VX6060s can be used in full mesh VPX or switched OpenVPX environments.

Each processing node implements Intel's next generation high performance embedded processor with integrated memory controller and Intel® HD graphics - the Intel® Core™ i7 processor - coupled with the highly integrated Intel® Platform Controller Hub (PCH) QM57 with numerous Gigabit Ethernet, SATA, USB 2.0 and PCIe channels.

The VX6060 board comes with EFI BIOS and supports Linux. It is covered by Kontron's long term supply program, which guarantees customers multi-year supply of the product beyond its active life.

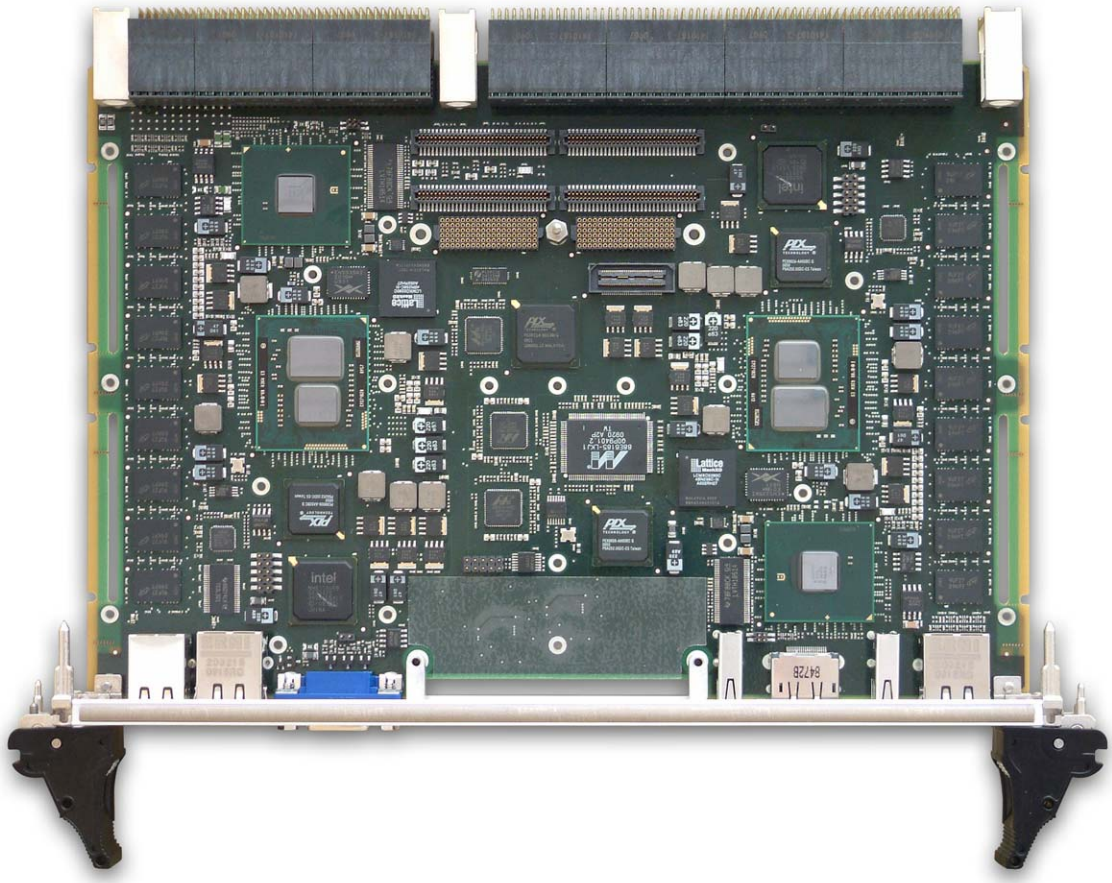


Figure 1: VX6060-SA 6U VPX Overview

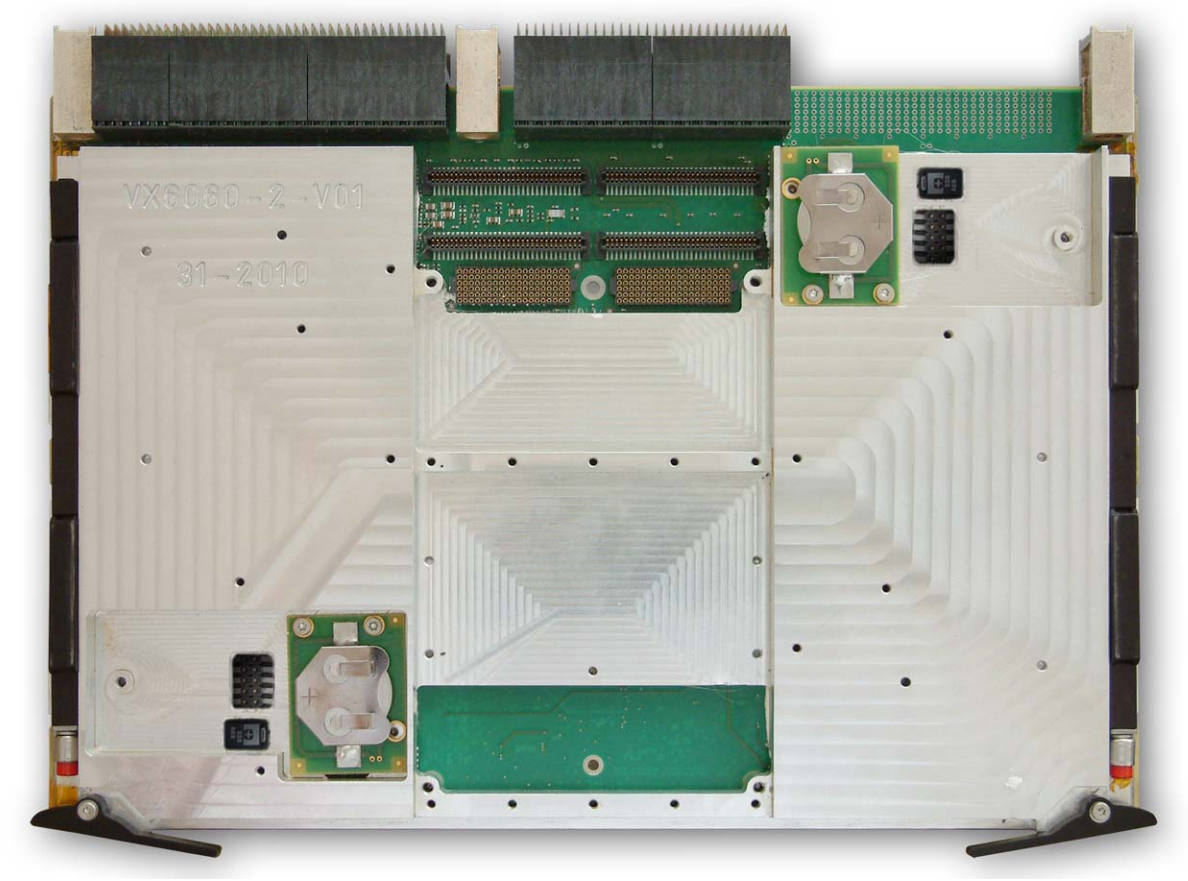


Figure 2: VX6060-RC 6U VPX Overview

1.1 Manual Overview

1.1.1 Objective

This guide provides general information, hardware instructions, operating instructions and functional description of the VX6060 board. The onboard programming, onboard firmware and other software (e.g. drivers and BPS) are described in detail in separate guides (see section 1.x "Related Publications").

This hardware technical documentation reflects the most recent version of the product. The "Hardware release Notes" (see section 1.x "Related Publications") might help to keep track of potential evolutions.

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

1.1.2 Audience

This guide is written to cover, as far as possible the range of people who will handle or use the VX6060, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, system, cabling, grounding and communications.

1.1.3 Scope

This guide describes all variants of the VX6060 series. It does not cover any PMC/XMC modules which are described in specific guides.

1.1.4 Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- Chapter 1 - Introduction (this chapter)
- Chapter 2 - Installation
- Chapter 3 - Additional Board Features
- Chapter 4 - Physical In/Out
- Chapter 5 - Power and Thermal Specifications
- Chapter 6 - Backplane Suggestions

1.1.5 Terminology, Definitions and Abbreviations

In this document, the term:

» VX6060 will be associated to the 6U VPX board

- > VX6060-SA will be associated to the standard air-cooled commercial version of the board.
- > VX6060-RA will be associated to the rugged air-cooled version of the board.
- > VX6060-RC will be associated to the rugged conduction-cooled version of the board.

» VX6060-RTM will be associated to the 3U VPX Rear Transition Module (RTM).

The VX6060 board is implemented as two similar CPU subsystems separated by a central PMC/XMC slot. This implies a common description of CPU subsystems on the board (ex: both parts have same CPU / SATA / USB / DDR3 /… interfaces).

For convenience, the CPU subsystem that faces P0/P1/P2 is called **subsystem A** and the second CPU subsystem on the other side is called **subsystem B**.

In this documentation:

- > CPU in subsystem A is named CPUA,
- > CPU in subsystem B is named CPUB,
- > USB in subsystem A is named USBA,
- > USB in subsystem B is named USBB ,
- > and so on.

1.2 VPX Overview

VPX (VITA 46) specifications establish a new direction for the next revolution in bus boards. VPX is an ANSI standard which breaks out from the traditional connector scheme of VMEbus to merge the latest in connector and packaging technology with the latest in bus and serial fabric technology. VPX combines best-in-class technologies to assure a very long technology cycle similar to that of the original VMEbus solutions. Traditional parallel VMEbus will continue to be supported by VPX through bridging schemes that assure a solid migration pathway.

For further information regarding this standards and its use, visit the home page of the VITA - Open Standards, Open Markets (http://www.vita.com)

1.3 Board Overview

1.3.1 Main Features

» Intel® Core™ i7 Architecture

The VX6060 computing node is a VPX computing blade for parallel data and signal processing application. With two independently implemented Intel® Core™ i7 processing nodes linked to a powerful Ethernet and PCIe infrastructure, the VX6060 is the ideal building block for intensive parallel computing workloads where a cluster of VX6060s is used in full mesh or switched OpenVPX environments. Target applications include radar, sonar, imaging systems, airborne fighters, and unmanned aerial vehicle (UAV) radar, as well as rugged multi-display consoles.

Each processing node of the VX6060 implements an Intel® Core™ i7 processor coupled with dual channel DDR3 memory. The highly integrated Intel® QM57 Express platform hub provides numerous Gigabit Ethernet, SATA, USB 2.0 and PCIe channels. The 6U-format VX6060 is available in standard air-cooled and conduction-cooled versions.

The frequency of each CPU is 2.0 GHz; however, the processor Intel® Core™ i7 is equipped with the Turbo Boost technology, which allows increasing the frequency up to 2.8 GHz when the total on chip power allows (depending on second core and graphics activity).

» Soldered DDR3 Memories with the Support of ECC

Each processor accesses two memory-channels (2 x 72-bit) having a total size of 2, 4 or 8 GB per processor. The DDR3 memory technology used operates at 1067 Gbits/s. An 8 bits ECC memory is implemented to detect and correct errors.

» Numerous Storage Interface and Non Volatile Memories

The following storage features are available for each processor:

- An USB 2.0 Flash drive slot is available onboard supporting low profile USB 2.0 Flash disk modules up to 16 GB.
- Redundant 32 Mbits NOR Flashes are used to store firmware code.
- Two serial 256 Kbits EEPROMs are dedicated to system and application data storage.
- A 512 Kbits Ferro Magnetic, Non-volatile Random Access Memory allows backup of critical data when power is removed.

All the Flash and non volatile memories onboard have a write protect mechanism taking into account the NVMRO (Non Volatile Memory read Only) VPX signal.

Extensive I/O Connectivity

Interface name	Subsystem	Front, Rear or Onboard Connector	Front Panel Connector name	Documentation Name
x4 PCI Express	A	Rear P1		PEX0-A
	B	Rear P1		PEX0-B
x1 PCI Express	A	Rear P2		PEX1-A
Serial EIA-232	A	Front and Rear P2	COM-AB	COM1-A
	B	Front and Rear P2		COM1-B
	A	Rear P2		COM2-A
	B	Rear P2		COM2-B
Ethernet 1000BASE-T	A	Front	ETH-A	ETH-A
	Ethernet Switch	Front or Rear P1 BIOS configuration	ETH-SW	ETH-SW
SerDes Ethernet 1000BASE-BX	Ethernet Switch	Rear P1		ETH-SW7
	Ethernet Switch	Rear P1		ETH-SW8
	Ethernet Switch	Rear P1		ETH-SW9
USB	A	Front	USB-A	USB-A
	A or B BIOS configurable	Front	USB-AB	USB-AB
	A	Onboard Flash Mezzanine		USB1-A
	B	Onboard Flash Mezzanine		USB1-B
	A	Rear P1		USB2-A
	B	Rear P1		USB2-B
	A	Rear P2		USB3-A
	B	Rear P2		USB3-B
Graphics VGA	A	Front	VGA	VGA
Graphics Display Port	A	Front	Display Port	DP2-A
	A	Rear P2		eDP1-A
	B	Rear P2		eDP1-B
Serial ATA	A	Rear P1		SATA0-A
	B	Rear P1		SATA0-B
	A	Rear P2		SATA1-A
	A	Rear P2		SATA2-A
	A	Onboard HDD Mezzanine		SATA3-A

Table 1: I/O Connectivity

Software

Kontron is one of the few compact PCI, VME and VPX vendors providing in-house support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software manufactures, Kontron is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

Finally, customers possessing a maintenance agreement with Kontron can be guaranteed hotline software support and are supplied with regular software updates. A dedicated web site is also provided for online updates and release downloads.

The VX6060 is delivered with the UEFI BIOS from AMI.

The VX6060 supports Linux Fedora 12 distribution.

Please contact Kontron for further information concerning other operating systems and software support.

Harsh Environments

The VX6060 has been designed to use the same PCB for both air and conduction-cooled boards. Build variants span a complete range of temperature, shock and vibration requirements as specified in the VITA 47 standards.

Rear Transition Module

The VX6060 supports the VX6060-RTM (Order Code: PB-VX3-002), a 3U VPX Rear Transition Module compliant to Rear Transition Module on VPX standard - VITA 46.10.

It offers connectivity on the rear for:

- one RJ-45 Ethernet 1000Base-T (when the VX6060 Order Code is compatible with Ethernet on P1)
- two SATA port
- two serial COM ports
- two USB ports
- two GPIOs

1.3.2 Block Diagram

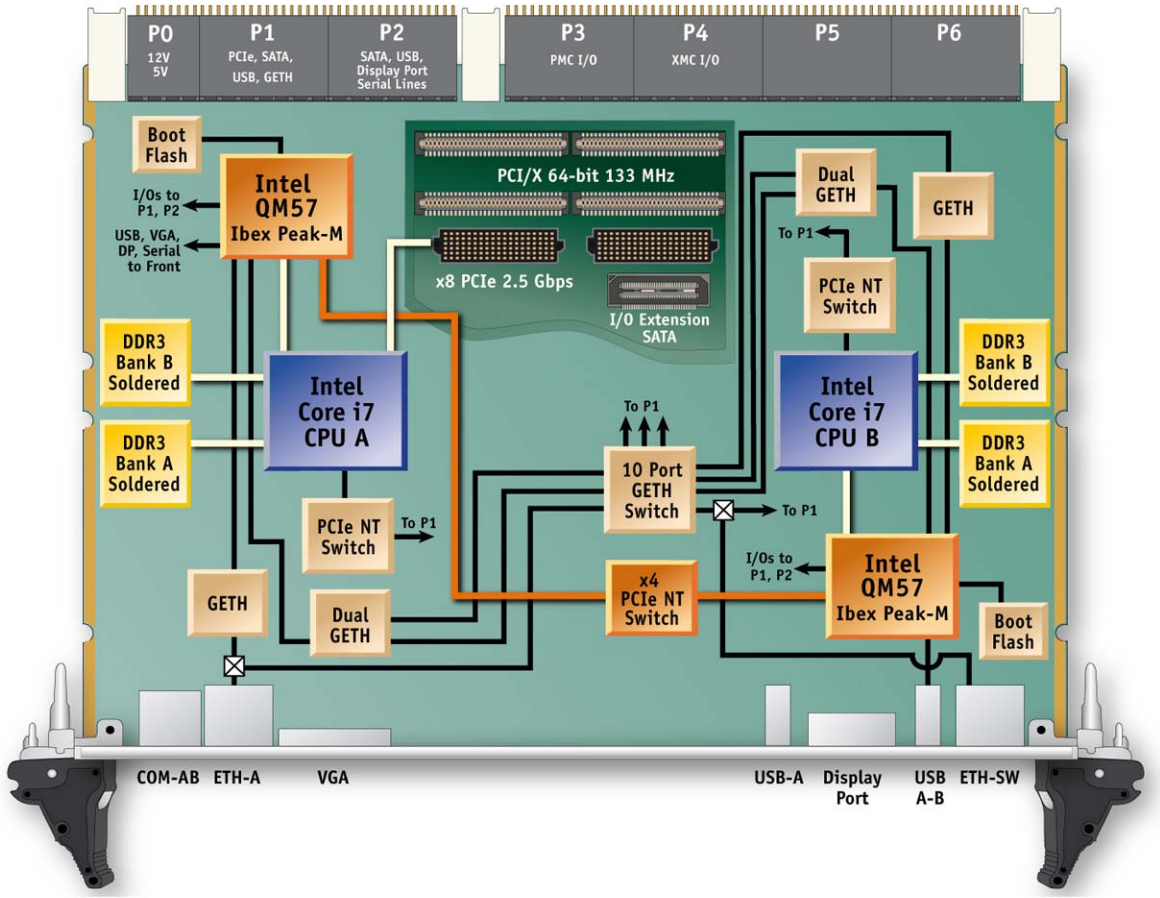


Figure 3: VX6060 Block Diagram

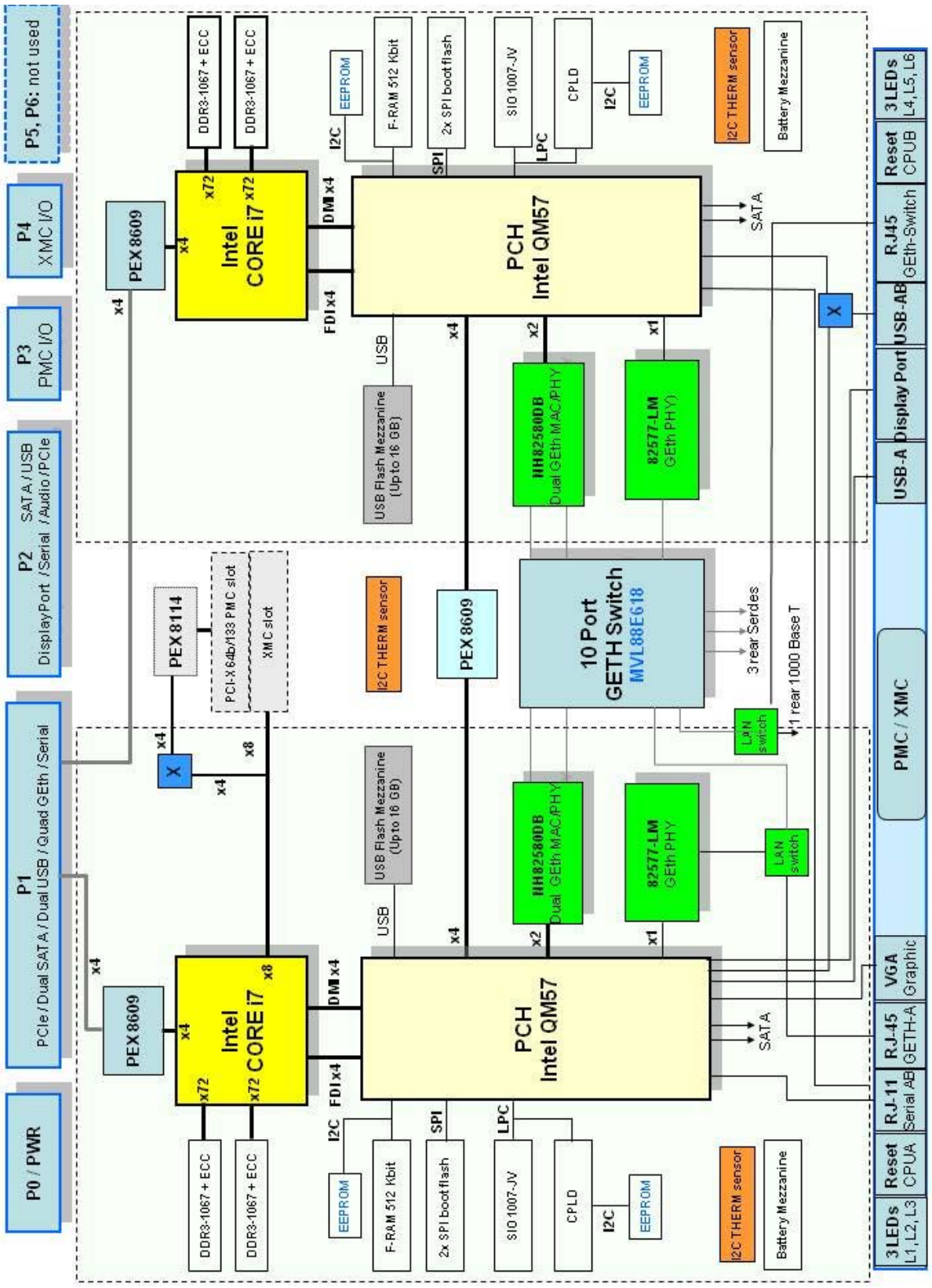


Figure 4: VX6060 Functional Block Diagram

1.3.3 Ordering Information

Manufacturing Options

- **CPU Frequency:** **2 GHz (default)**
- **DDR3 SDRAM Size:** 2 GB per CPU, 4 GB total onboard
  4 GB per CPU, 8 GB total onboard
  8 GB per CPU, 16 GB total onboard
- **Ethernet on VPX Backplane:** **P1 (default)**
  P4
- **Mezzanine Single Ended I/O on P3 VPX Backplane:** **Pn4 PMC P64s (default)**
  Pn6 XMC X38s
- **Ruggedization Levels:** Standard Air-Cooled (SA)
  Rugged Conduction-Cooled (RC)

Order Code Available

Order Code		Description
VX6060-SA	VX6060-SA24-00000	6U VPX Dual Intel® Core™ i7 Computing Node: 2 GHz 4 GB DDR3 SDRAM total onboard Ethernet on P1, P64s on P3 Standard Air-Cooled
VX6060-SA	VX6060-SA25-00000	6U VPX Dual Intel® Core™ i7 Computing Node: 2 GHz 8 GB DDR3 SDRAM total onboard Ethernet on P1, P64s on P3 Standard Air-Cooled
VX6060-SA	VX6060-SA26-00000	6U VPX Dual Intel® Core™ i7 Computing Node: 2 GHz 16 GB DDR3 SDRAM total onboard Ethernet on P1, P64s on P3 Standard Air-Cooled
VX6060-RC	VX6060-RC24-00000	6U VPX Dual Intel® Core™ i7 Computing Node: 2 GHz 4 GB DDR3 SDRAM total onboard Ethernet on P1, P64s on P3 Rugged Conduction-Cooled
VX6060-RTM	PB-VX3-002	3U VPX Rear Transition Module compatible with the VX6060
Flash Module	FDM-USB-*x*GB-2MM-IV	USB Flash Device (*x* GB)
SATA Carrier Module	KIT-DISK25-SATA	2.5" SATA Disk Onboard Mounting Kit
Serial Cable	KIT-2X-RJ12DB9	Serial cable adapter to access CPUA or CPUB.

Table 2: Order Code

1.3.4 I/O Interfaces

Front Interfaces

Not available on RC (Rugged Conduction-Cooled) boardss

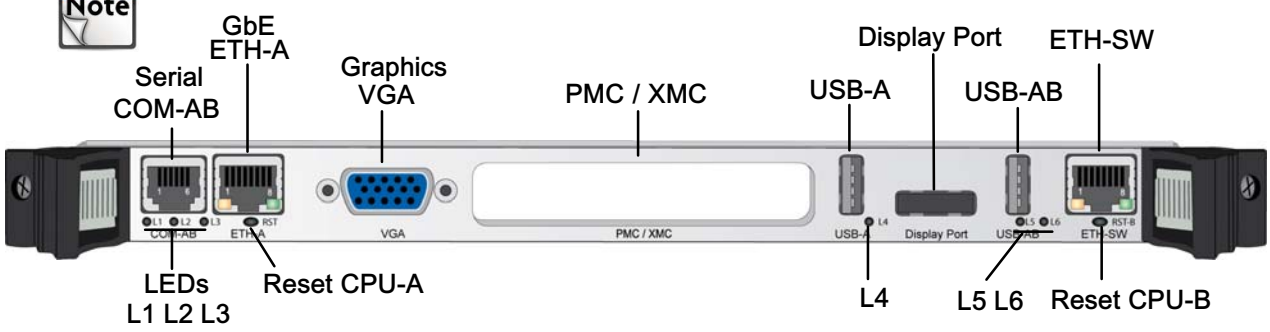


Figure 5: VX6060 Front Panel I/O Interfaces

Function	Description	See also
Serial Ports	**COM-AB**: 1x EIA-232 UART interface for CPUA and CPUB on RJ-11 connector.	Section 4.1.1 for Pin Assignment
Gigabit Ethernet	2x 1000BASE-T on RJ-45 connectors: > **ETH-A**: dedicated to CPUA **Note**: this port is configurable from the BIOS to be routed to the central onboard ethernet switch, instead of the front connector ETH-A > **ETH-SW:** This port is connected to the central onboard ethernet switch **Note**: this port is configurable from the BIOS to be routed to the VPX backplane, P1 connector, instead of the front connector ETH-SW	Section 4.1.2 for Pin Assignment
USB	2x USB 2.0 interfaces > **USB-A**: dedicated to CPUA > **USB-AB**: connector can be setup from the BIOS to be attached to CPUA or CPUB	Section 4.1.3 for Pin Assignment
Graphics	**VGA**: VGA connector, dedicated to CPUA.	Section 4.1.4 for Pin Assignment
Display Port	**Display Port**: Display Port dedicated to CPUA	Section 4.1.5 for Pin Assignment
PMC/XMC	1x PMC/XMC slot	Figure 5
Reset	2 Reset push button (one per processor) > **RST-A:** dedicated to CPUA > **RST-B:** dedicated to CPUB	Figure 5
LEDs	6 LEDs reporting the board CPU health status and activity > **L1, L2, L3** dedicated to CPUA > **L4, L5, L6** dedicated to CPUB	Section 4.6 for LEDs Description

Table 3: Front I/O Interfaces

Rear Interfaces

Compliant with:

- VITA 46.0 (Standard VPX)
- VITA 46.4 (PCI Express on VPX)
- VITA 46.9 (PMC, XMC, I/O and Gigabit Ethernet on VPX)
- VITA 65 (OpenVPX System specification)

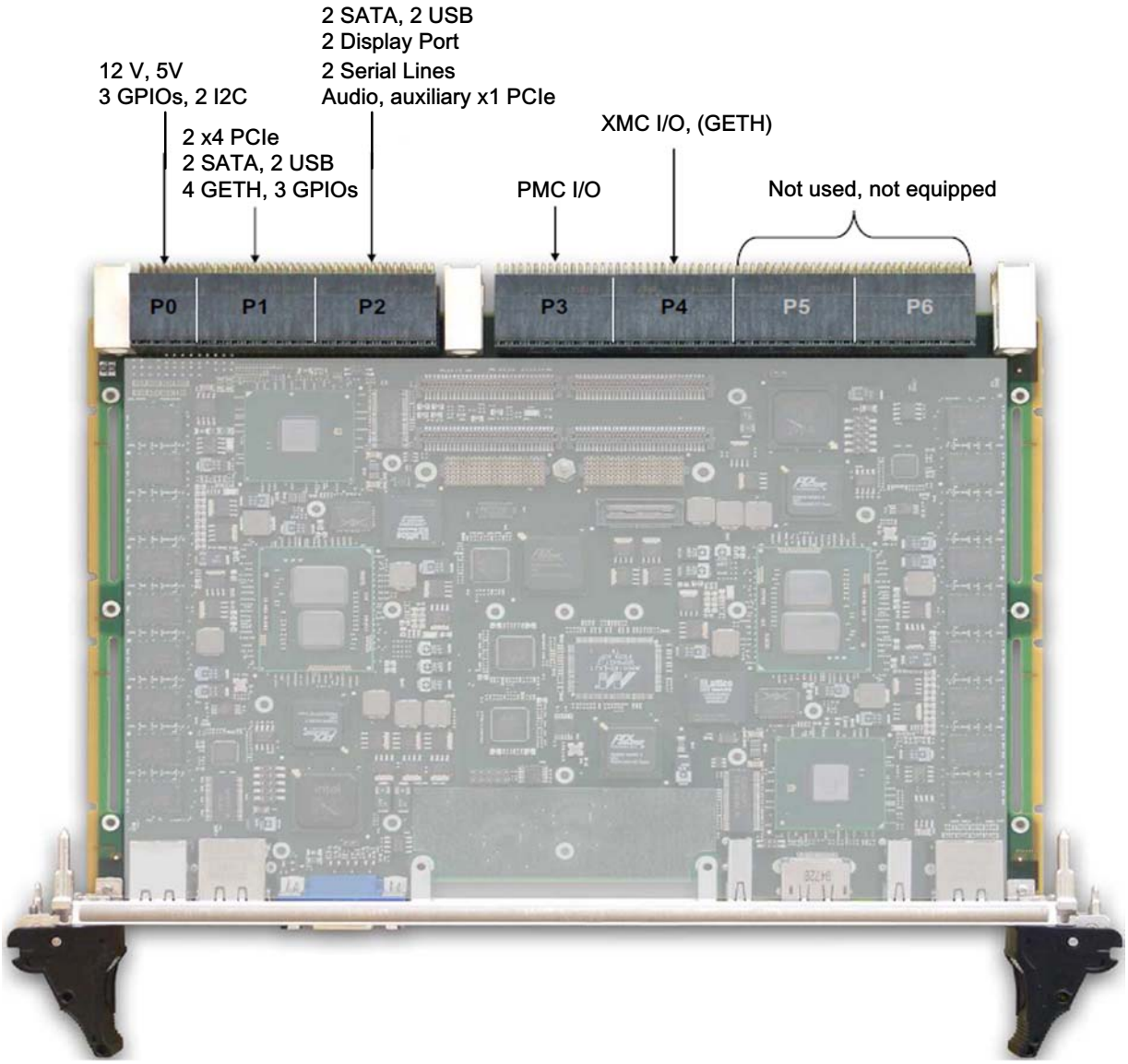


Figure 6: VX6060 Rear I/O Distribution

Function	Description	See also
PCI Express	> 1 x4 gen2 PCIe per CPU, non transparent capability, on P1. Optional use of PCIe common reference clock feature. > 1 x1 additional PCIe interface, gen1, for CPUA on P2	Section 4.3 for VPX Connectors Description
SATA Storage	> 1 SATA II link per CPU on P1 > 2 additional SATA II links on P2 for CPUA	
USB	> 1 USB 2.0 link per CPU on P1 > 1 additional USB 2.0 link per CPU on P2	
Gigabit Ethernet	> 3 SerDes 1000BASE-BX on P1 from onboard central ethernet switch > one 1000Base-T on P1 from the onboard central ethernet switch (exclusive with front panel ETH-SW) > Build option for 2 GETH 1000Base-BX and 1 GETH 1000Base-T on P4, instead of P1, according to VITA 46.9	
Serial	> 1 asynchronous EIA-232 RX/TX serial line per CPU, on P2	
GPIOs	> 3 User GPIOs on P1, including OpenVPX GDISCRETE1, and MASKABLE RESET > 3 additional GPIOs on P0, replacing unused JTAG pins	Section 4.3 for VPX Connectors Description
PMC/XMC I/O	PMC/XMC I/O according to VITA 46.9. Differential I/O from Pn6 on VPX P4: P4-X12d + X8d Single ended I/O on VPX P3; build option for P64s (Pn4 I/O) or X38s (Pn6 I/O)	Section 4.3 for VPX Connectors Description
DisplayPort	1 embedded DisplayPort on P2, per CPU	
Utilities	On P0 and P1: SYSRESET, SYSCON, 6 Geographical Addresses	
Clocks	On P0: 25 MHz Refclock, 1 PPS Auxclock, optional PCIe 100 MHz clock	Section 4.3 for VPX Connectors Description
Power Supplies	On P0: VS1=12V, VS2 not connected, VS3=5V, 3.3V_AUX optional, +12V_AUX not connected, -12V_AUX used for PMC/XMC -12V	Section 4.3 for VPX Connectors Description

Table 4: Rear I/O Interfaces

1.3.5 Components Layout

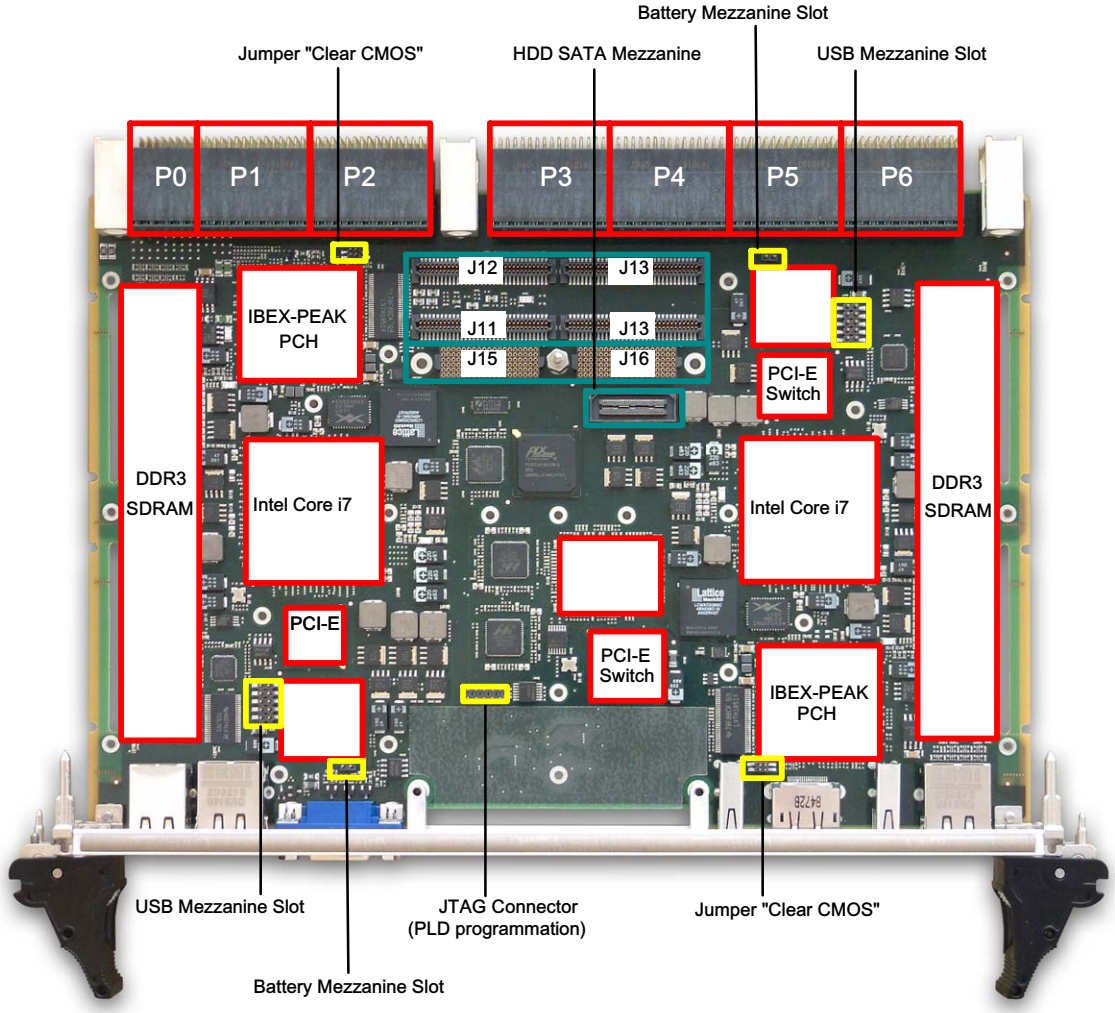


Figure 7: VX6060 Components Layout (Top view)

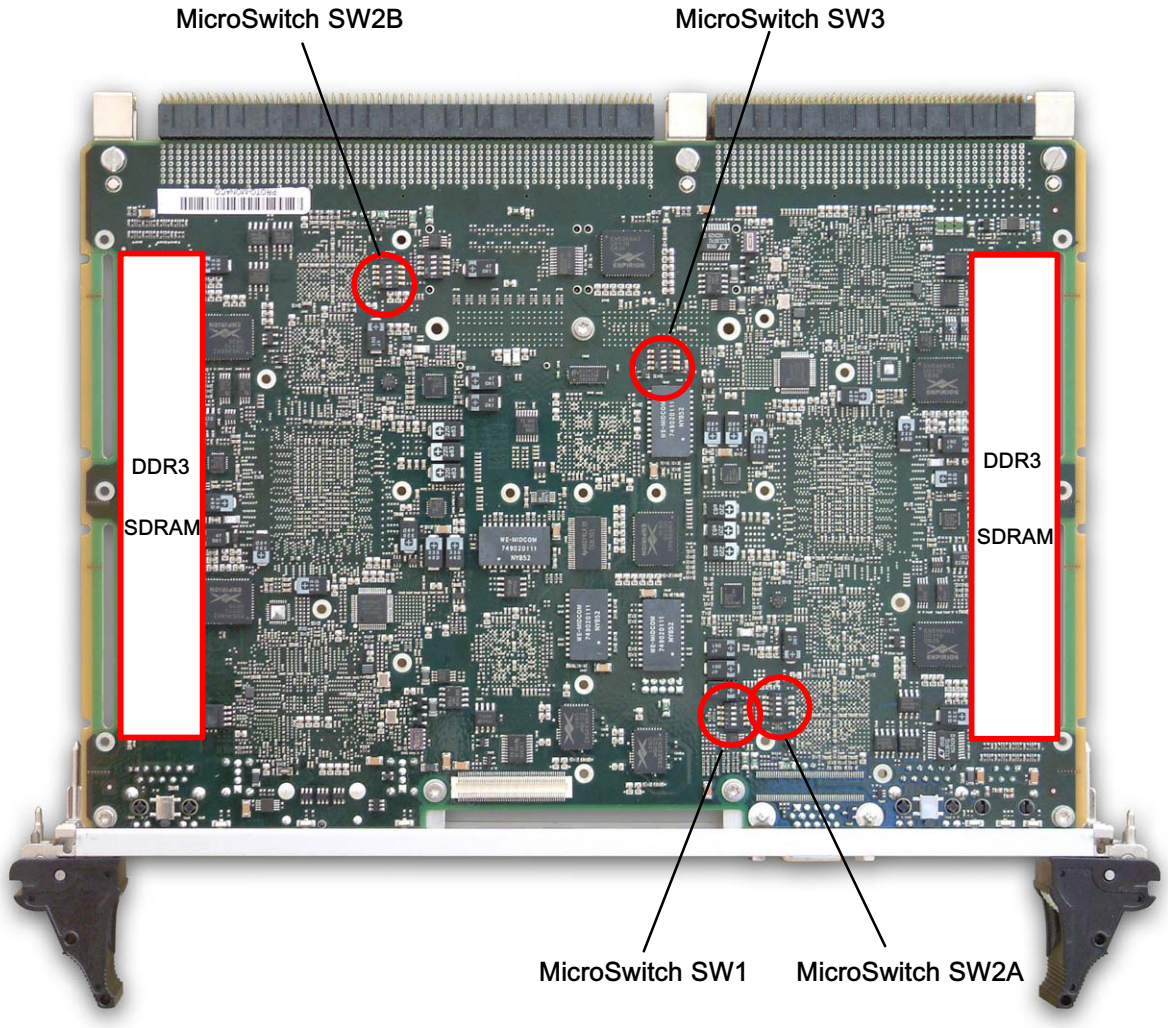


Figure 8: VX6060 Components Layout (Bottom view)

1.3.6 Technical Specification

Form Factor	
Form Factor	6U VPX, single slot, 1 inch pitch for Standard Air (SA), 0.8 inch pitch for Rugged conduction-cooled (RC).
Processor: Intel® Core™ i7	
Processor	Two Intel® Core™ i7-620 at 2 GHz. Each CPU features 4M cache, 2 execution cores, 4 threads. 32-nanometer silicon technology.
Cache Structure	32 KB L1, 256 KB L2 per core, 4 MB L3 shared between cores.
Memory Controller	Integrated DDR3 memory controller with ECC support, 1067 Mbits/s. For each CPU, two memory channels of 72 bits each.
Graphics Core	Integrated Graphics Core
PCI Express Interface	2.5 GT/s gen 1 PCIe. One 8 lane PCIe to XMC slot. One 4 lane PCIe to the backplane through PEX8609 Non Transparent (NT) bridge for PCIe backplane links.
DMI Interface	x4 2.5 GT/s point-to-point DMI interface to Platform Controller Hub (PCH).
FDI Interface	Carries display traffic from the integrated graphics controller to the PCH for generation of external display protocols (VGA, eDP, ...)
PCH: Ibex Peak-M	
PCI Express Interface	4 lane PCIe to PEX8609 Non Transparent (NT) bridge for communication between for CPUA and CPUB 2 lane PCie to 1000BASE-BX dual-ethernet controller for each CPU 1 lane PCIe to VPX backplane for CPUA
SPI Interface	Connects to two SPI flash devices (4 MBytes)
LPC	33 MHz LPC, for SuperIO and CPLD connection
SATA	Up to 3 Gb/s integrated Serial ATA host controllers CPUA: 3 ports on rear VPX connectors, 1 port for onboard HDD carrier connector CPUB: 1 port on rear VPX connectors, 1 port for onboard HDD carrier connector
USB	For each CPU: 2 USB 2.0 ports on the VPX connectors, 1 USB 2.0 port for onboard Flash mezzanine connector One front USB 2.0 for CPUA One front USB 2.0 for CPUA or CPUB
VGA and Display Ports	One VGA front panel interface for CPUA One embedded display port per CPU available on VPX backplane One additional display port on front panel for CPUA

Memory	
System Memory	Up to 8 GB DDR3 SDRAM per CPU at 1067 MHz, two memory channels per CPU
SPI Flash	Firmware Boot Device
NAND Flash	Up to 16 GB USB Nand Flash storage socket (for USB Nand Flash modules). One socket per CPU
F-RAM	512 Kbit of non volatile ferromagnetic RAM per CPU
EEPROM	One serial 256 Kbit EEPROM dedicated to system data per CPU One serial 256 Kbit EEPROM dedicated to application data per CPU
Onboard Controllers	
Gigabit Ethernet Controller	One i82580 Gigabit MAC/PHY connecting two SerDes links per CPU to the onboard central switch
Gigabit Ethernet PHY	One i82577 PHY per CPU connected to the central ethernet switch (or front panel for CPUA)
Gigabit Ethernet Switch	MVL88E6185 10 ports Gigabit Ethernet onboard central switch
System CPLD	One CPLD per CPU Board controller for power sequencing, reset handling, monitoring, failure detection, VPX I2C communication. Provides configuration/status registers on LPC interface
SIO	SIO1007 provides two serial lines One SIO per CPU
Onboard Interfaces	
CPU Debug Interface	XDP port for CPU extended debug port connection (only available on a debug connector and need additional test board for XDP access)

Table 5: VX6060 Main Characteristics

1.3.7 Reset Source Summary

Reset source	Reset Action	Inhibition	Reset status	Force
Front panel Reset CPU-A PLD Watchdog reset CPU-A	CPU-A sub-system, including PMX/XMC slot Geth On-Board switch Bios Controlled : PEX8609 PCIe Switches		CPLD	
	VPX Backplane Reset (250 ms)	REG @70 bit 0 set to 1	PCH	
PCH Watchdog reset CPU-A	CPU-A sub-system			
	Geth On-Board switch			
	PMX/XMC slot			PMC_BUSMODE1# set to 0
	Bios Controlled : PEX8609 PCIe Switches	REG @04 bit 4 set to 1		REG @04 bit 1 set to 0
VPX Soft Reset (REG @70 bit 2)	VPX Backplane Reset (250 ms)	REG @70 bit 0 set to 1		
Maskable Reset (GPIO2)	Global VX6060 reset	REG @70 bit 4 set to 0		
VPX SYSRESET#	Global VX6060 reset	REG @70 bit 1 set to 1		
Front panel Reset CPU-B PLD Watchdog reset CPU-B PCH Watchdog reset CPU-B	CPU-B sub-system		CPLD	
CPLD I2C slave register @Base_addr+1 Bit 1 (Reset_3UA)	CPU-A sub-system, including PMX/XMC slot Geth On-Board switch Bios Controlled : PEX8609 PCIe Switches		CPLD	
CPLD I2C slave register @Base_addr+1 Bit 2 (Reset_3UB)	CPU-B sub-system		CPLD	
CPLD A register @04 Bit 0	CPU-B sub-system			
CPLD B register @04 Bit 0	CPU-A sub-system, including PMX/XMC slot Geth On-Board switch Bios Controlled : PEX8609 PCIe Switches			

PCH= Ibex Peak Platform Controller Hub

1.4 Environmental Specifications

ENVIRONMENTAL SPECIFICATIONS		
	SA - Standard Commercial	RC - Rugged Conduction-Cooled
Conformal Coating	Optional	Standard
Airflow	3 m/s	N.A.
Temperature	VITA 47-Class AC1	VITA 47-Class CC4
Cooling Method	Convection	Conduction
Operating	0°C to +55°C	-40°C to +85°C
Storage	-45°C to +85°C	-45°C to +100°C
Vibration Sine (Operating)	2g / 20-500 Hz acceleration / frequency range	5g / 22-2,000 Hz acceleration / frequency range
Random	VITA 47-Class V1	VITA 47-Class V3
Shock (Operating)	20g / 11 ms peak accel. / shock duration half sine	40g / 20 ms peak accel. / shock duration half sine
Altitude (Operating)	-1,640 to 15,000 ft	-1,640 to 60,000 ft
Relative Humidity	90% non-condensing	95% non-condensing

Table 6: Environmental Specifications

1.5 Technical Specifications

Technical SPECIFICATIONS		
	SA - Standard Commercial	RC - Rugged Conduction-Cooled
Board Weight	630g	990g with ruggedizer

1.6 MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

VX6060-SA24-00000

	GB (Hours)		AIC (Hours)	NS (Hours)		ARW (Hours)
	25°C	40°C	40°C	25°C	40°C	55°C
VX6060 Order Code: VX6060-SA24-00000	143 514 h	104 307 h	17 903 h	26 720 h	21 364 h	4 415 h

Table 7: VX6060-SAA1N-000 MTBF Data

1.7 Related Pubications

The following publications contain information relating to this product:

PRODUCT	PUBLICATION	
Standard		
ANSI/VITA 46.0	VPX Baseline Standard - ANSI/VITA 46.0-2007	
ANIS/VITA 46.4	PCI Express® on VPX Fabric Connector - VITA Draft Standard for Trial Use	
ANSI/VITA 46.6	Gigabit Ethernet Control Plane on VPX - VITA Draft Standard	
ANSI/VITA 46.9	PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules- VITA Draft Standard	
ANSI/VITA 46.10	Rear Transition Module for VPX - ANSI/VITA 46.10-2009	
Serial ATA	Serial ATA 1.0a Specification	
Hardware		
VX6060 Boards	VX6060 Hardware Release Notes	CA.DT.A77
Firmware		
VX6060 Boards	AMI-BIOS User Reference Manual	SD.DT.F69
Software		
VX6060 Boards	Release Note Fedora 12 on VX6060	SD.DT.F72
Systems		
VX6060 Boards	EZ2-VX6060-00-L Quick Start	SD.DT.F64

Table 8: Related Publications

Chapter 2 - Installation

The VX6060 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

2.1 Safety Requirements

The following safety precautions must be observed when installing or operating the VX6060. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot.Do not touch the heat sink when installing or removing the board.
In addition, the board should not be placed on any surface or in any form of storage container until such time as the board and heat sink have cooled down to room temperature.

This board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:
Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector-pins or traces.
- If working at an anti-static workbench with professional discharging equipment, please do not omit to use it.

2.2 Board Identification

The VX6060 boards are identified by labels fitted to the top and bottom sides of the board.

Top Side

- **A** "PLD A reference" label.
- **B** "PLD B reference" label.

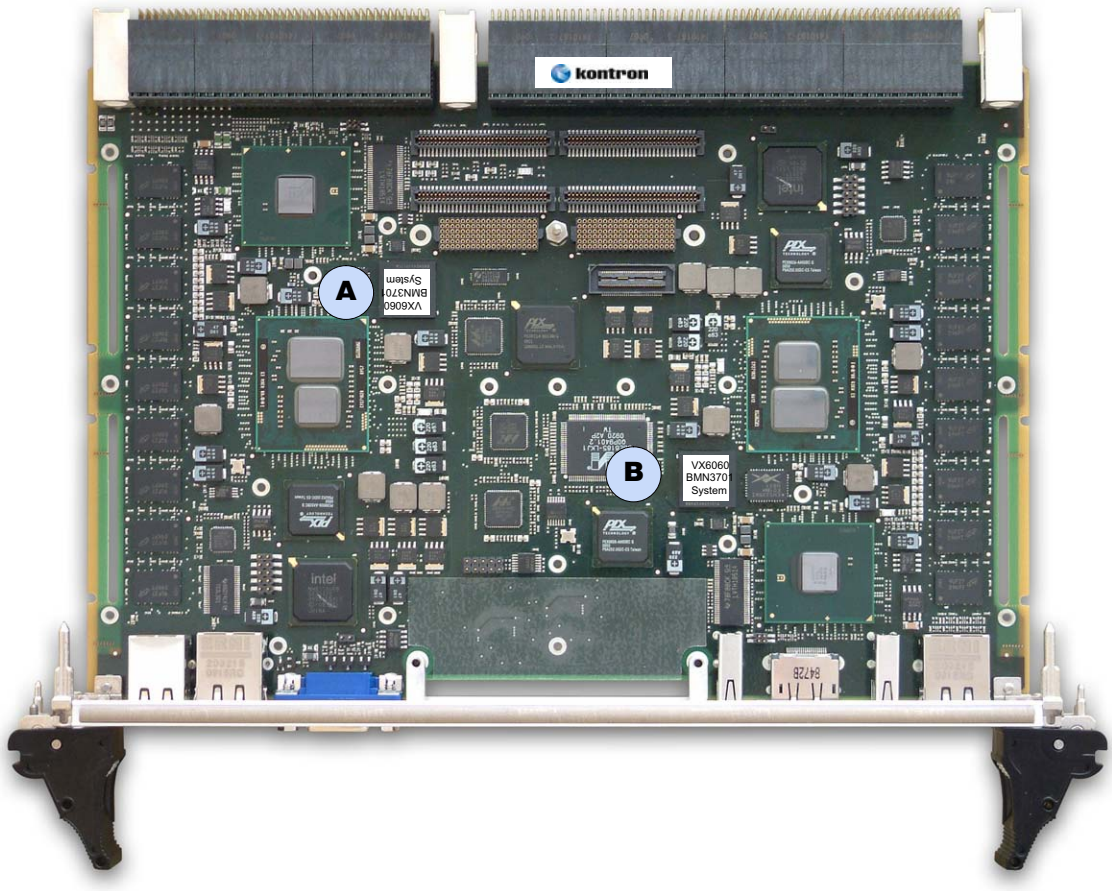


Figure 9: VX6060 Identification (Top Side)

Bottom Side

C "Identification" label: Order Code, Serial Number, Variant, E.C. Level

D "Ethernet MAC addresses" label (Eth0 up to Eth5).

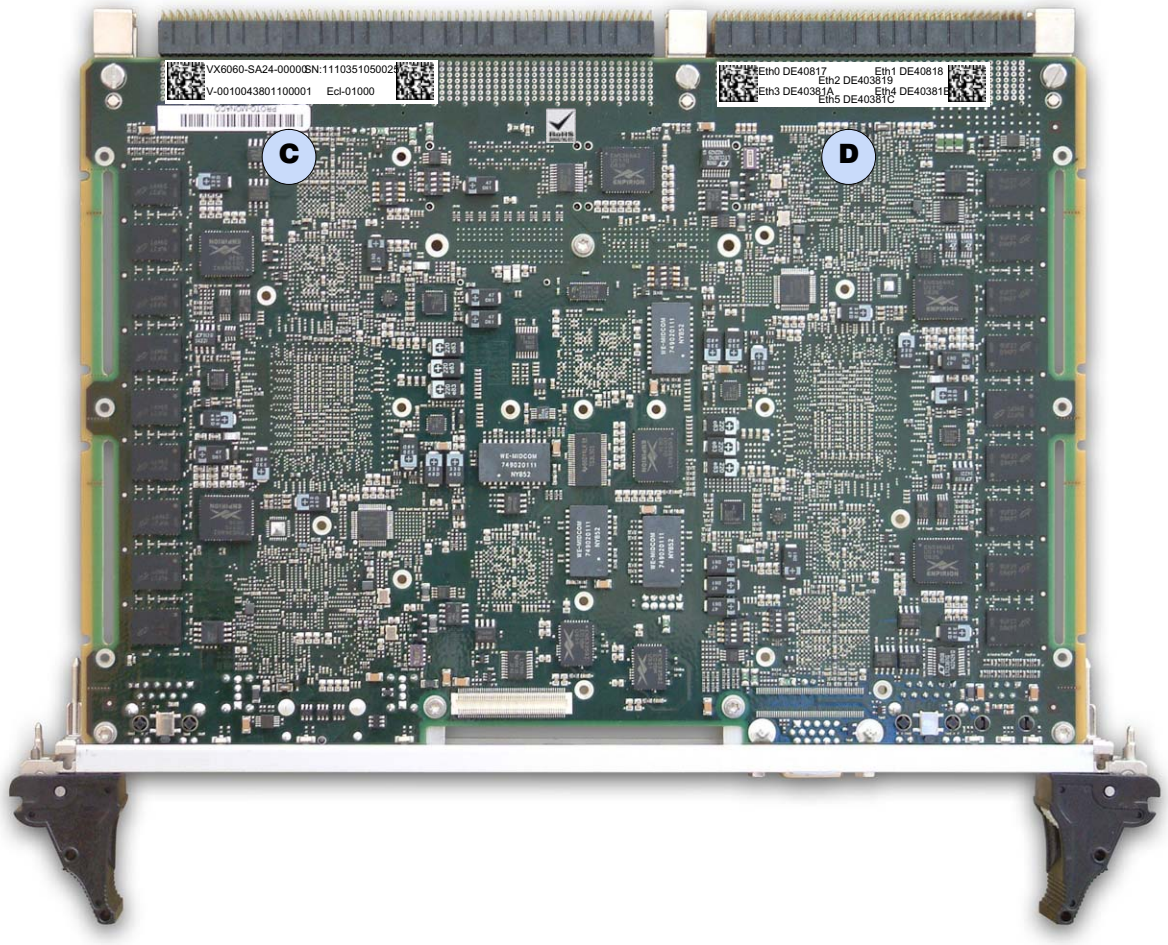


Figure 10: VX6060 Identification (Bottom Side)

2.3 Board Configuration

Jumpers

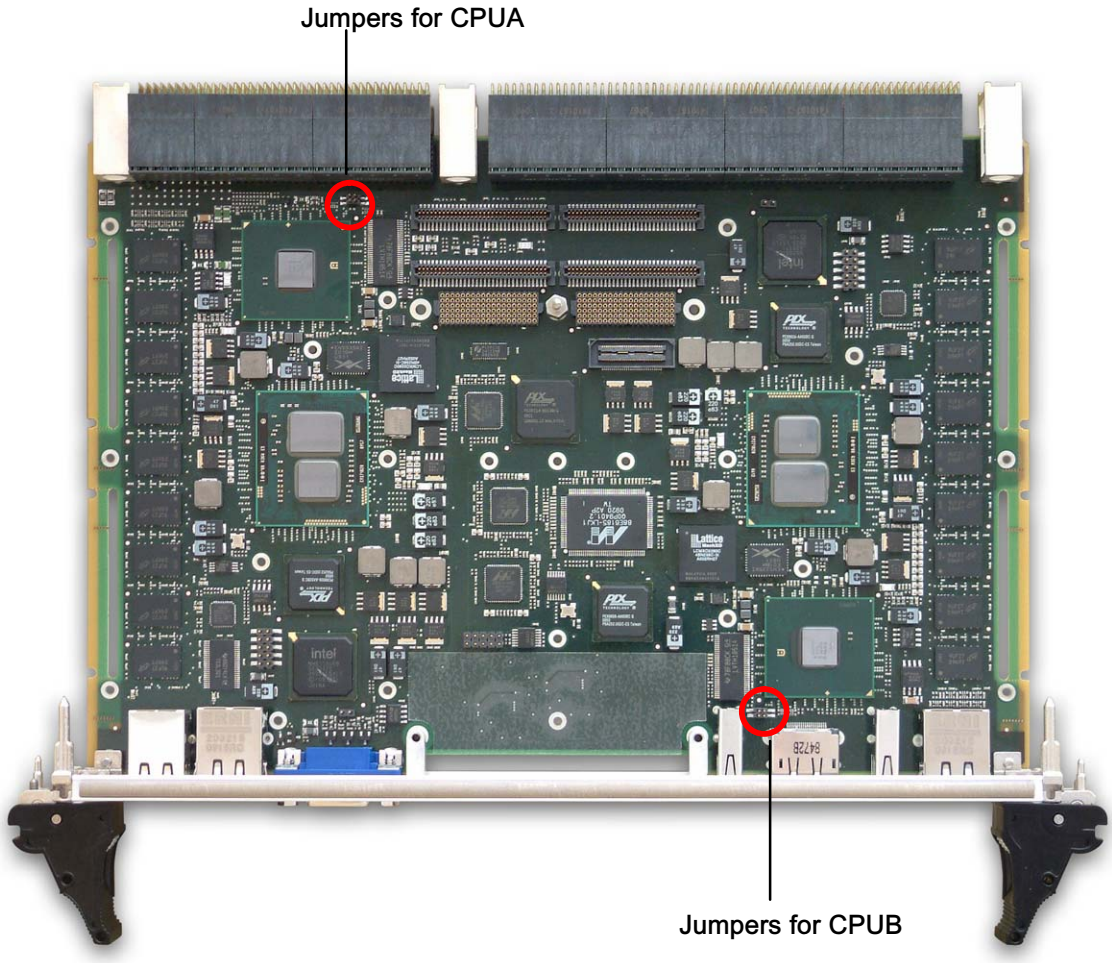


Figure 11: VX6060 Board Configuration (Top view)

Two jumpers are available on the VX6060 for each CPU subsystem:

- Clear CMOS
- Secondary RTC Reset

Microswitches

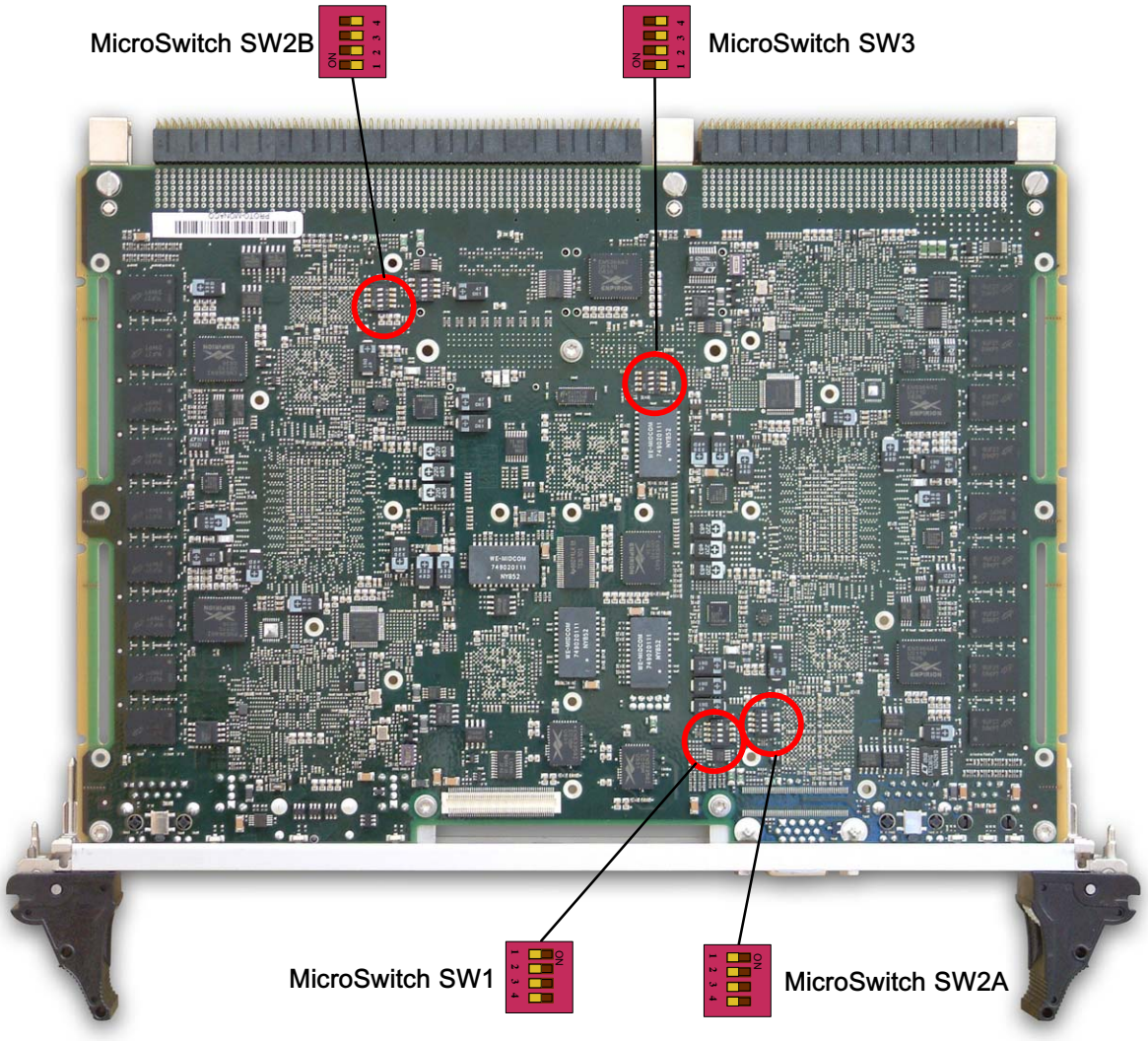


Figure 12: VX6060 Board Configuration (Bottom view)

Four 4-bit microswitches are available on the VX6060: SW1, SW2A, SW2B and SW3

2.3.1 Microswitch SW1 Description

Function	Description
1 - Factory Test Mode	**on**: factory test mode is selected **off**: normal operation
2 - VPD (Vital Product Data) EEPROM write protect	**on**: VPD 32Kx8 EEPROM is write protected **off**: VPD 32Kx8 EEPROM is not write protected unless VPX signal NVMRO is active (logic 1)
3 - System (base software parameters) EEPROM write protect	**on**: System 32Kx8 EEPROM is write protected **off**: System 32Kx8 EEPROM is not write protected unless VPX signal NVMRO is active (logic 1)
4 - FRAM (Ferro Magnetic RAM) write protect	**on**: 64Kx8 User FRAM is write protected **off**: 64Kx8 User FRAM is not write protected whatever the level of the NVMRO VPX signal is

Table 9: Microswitches SW1

2.3.2 Microswitches SW2A and SW2B Description

Function	Description
1 - Rescue Boot Flash	**on**: CPUA (respectively CPUB) boots the BIOS from its rescue flash. **off**: Normal operation. CPUA (respectively CPUB) boots the BIOS from its non rescue flash.
2 - Power on wait (SW2A only)	**on**: VX6060 card waits for an I2C command from the VPX bus to start internal power on. **off**: Normal operation. VX6060 card automatically powers on.
3 - Forced CPU reset	**on**: CPUA (respectively CPUB) is permanently reset. **off**: Normal operation.
4 - Reserved	

Table 10: Microswitches SW2A and SW2B

2.3.3 Microswitch SW3 Description

Function	Description
1 - VPX PCI-E port size	**on**: four x1 ports on VPX PI for each CPU subsystem **off**: one x4 port on VPX P1 for each CPU subsystem
2 - Maximum PCI-E link speed on VPX	**on**: Gen 2 (5 GT/s), will achieve Gen 2 speed transfers if link partner is advertising Gen 2 capability **off**: Gen 1 (2.5 GT/s), to be used with low speed capability backplane
3 - PMC PCI frequency	**on**: 25 / 50 or 100 MHz PCI or PCI-X clocking **off**: 33 / 66 or 133 MHz PCI or PCI-X clocking
4 - SPD debug mode	**on**: DDR3 SPD debug mode **off**: normal operation

Table 11: Microswitches SW3

2.4 Package Content

The VX6060 is packaged with several components. The packing contents of the VX6060 Series may vary depending on customer requests.

- CPU Module:
  - Order Code: refer to section 1.3.3 “Order Code Table” :
    - Processor specifications differ depending on Order Code.
    - Heat sink assembled on the board.
- Rear Transition Module:
  - Order Code: refer to section 1.3.3 “Order Code Table”.
- USB Flash Disk Module:
  - Order Code: refer to section 1.3.3 “Order Code Table”.
- SATA Carrier Module:
  - Order Code: refer to section 1.3.3 “Order Code Table”.
- CD-ROM Technical Documentation.

2.5 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the VX6060 in a system. Procedures for standard removal operations are found in their respective chapters.

To perform an initial installation of the VX6060 in a system proceed as follows:

1. Ensure that the safety requirements indicated in Section 2.1 are observed.

Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the VX6060 refer to Chapter 5. For the installation of VX6060 specific peripheral devices and Rear I/O devices refer to the appropriate sections in current Chapter and Chapter “RTM Characteristics”.

Care must be taken when applying the procedures below to ensure that neither the VX6060 nor other system boards are physically damaged by the application of these procedures.

3. To install the VX6060 perform the following:
    1. Ensure that no power is applied to the system before proceeding.

When performing the next step, DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

    2. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.
    3. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
    4. Fasten the front panel retaining screws.
    5. Connect all external interfacing cables to the board as required.
    6. Ensure that the board and all required interfacing cables are properly secured.

The VX6060 is now ready for operation. For operation of the VX6060, refer to appropriate VX6060 specific software, application, and system documentation.

2.6 Standard Removal Procedure

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Section 2.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

Care must be taken when applying the procedures below to ensure that neither the VX6060 nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.
5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

7. Dispose of the board as required.

2.7 Installation of Peripheral Devices

The VX6060 is designed to accommodate a variety of peripheral devices whose installation varies considerably. The following sections provide information regarding installation aspects and detailed procedures.

- > Section 2.7.1 page 31 USB Device Intallation
- > Section 2.7.2 page 33 Serail ATA Extension Module
- > Section 2.7.3 page 35 Battery Replacement

2.7.1 USB Flash Device Installation

The onboard USB device is used to connect an USB Flash Disk.

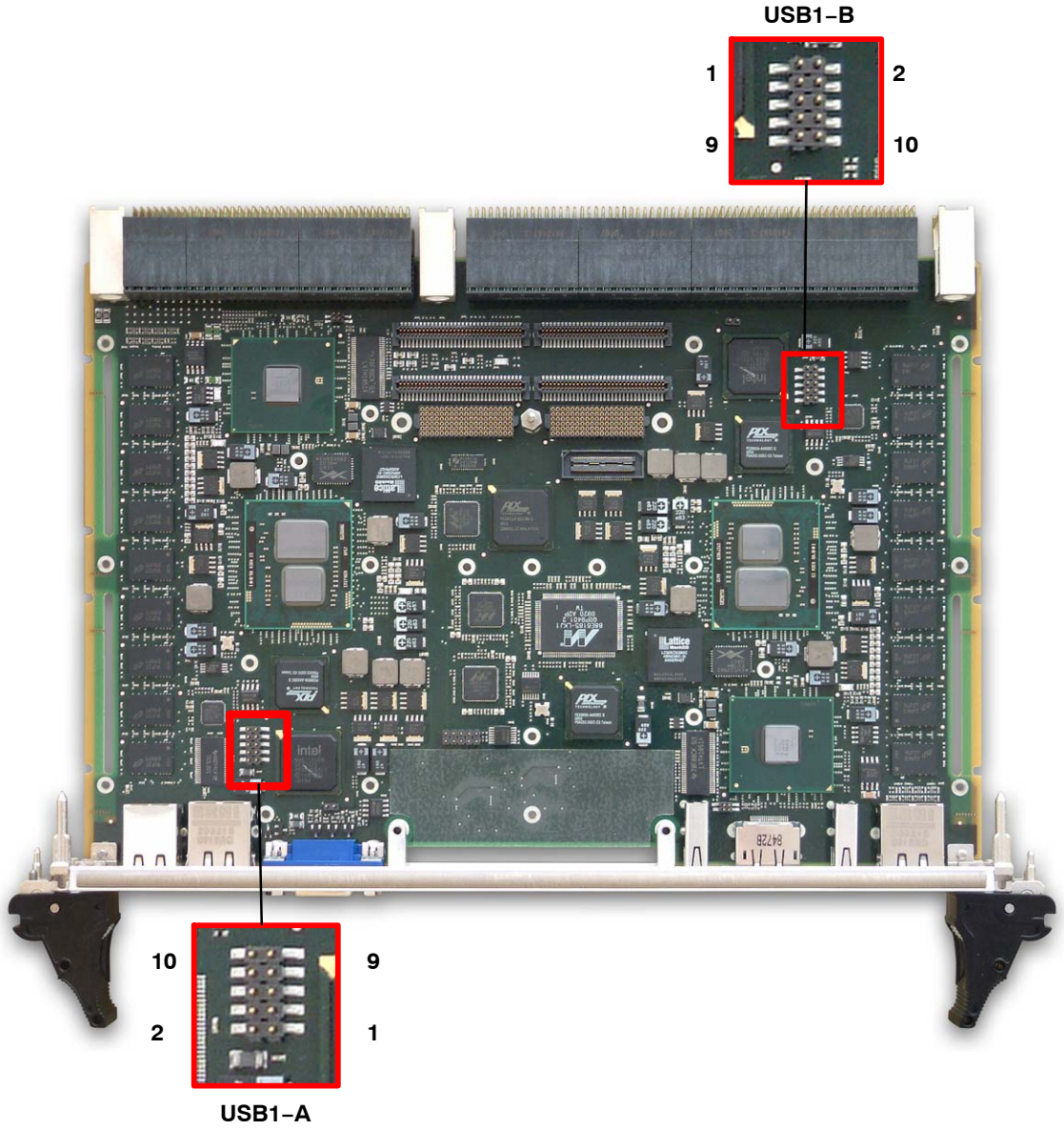


Figure 13: USB Mezzanine Slots Location

The USB Flash module is fixed to the board, by using on one side the USB1-A (USB1-B) connector, and on the other side, a nylon screw mounted on the VX6060 heatsink.

Make sure to use a nylon screwes when installing the USB Flash module, not to damage the VX6060 heatsink. Kontron Order Code: VIS-CLS-M3X6-NYLON. Radiospare Reference: 527-971.

Main Characteristics:
- Cheese head screw
- M3x6mm
- Nylon
- Operating range: -40°C - +158°C

Order Code for the USB flash disk:

FDM-USB-*x*GB-2MM-IV: industrial version with conformal coating for use with rugged versions (*x* = up to 16 GB)

> USB Flash Disk Overview

- Maximum space reserved for USB flash disk is 36.9 mm x 26.6 mm (LxW)
- The distance between connector and screw hole is 27.3 mm~27.9mm
- Maximum allowable connector height is 3.68 mm

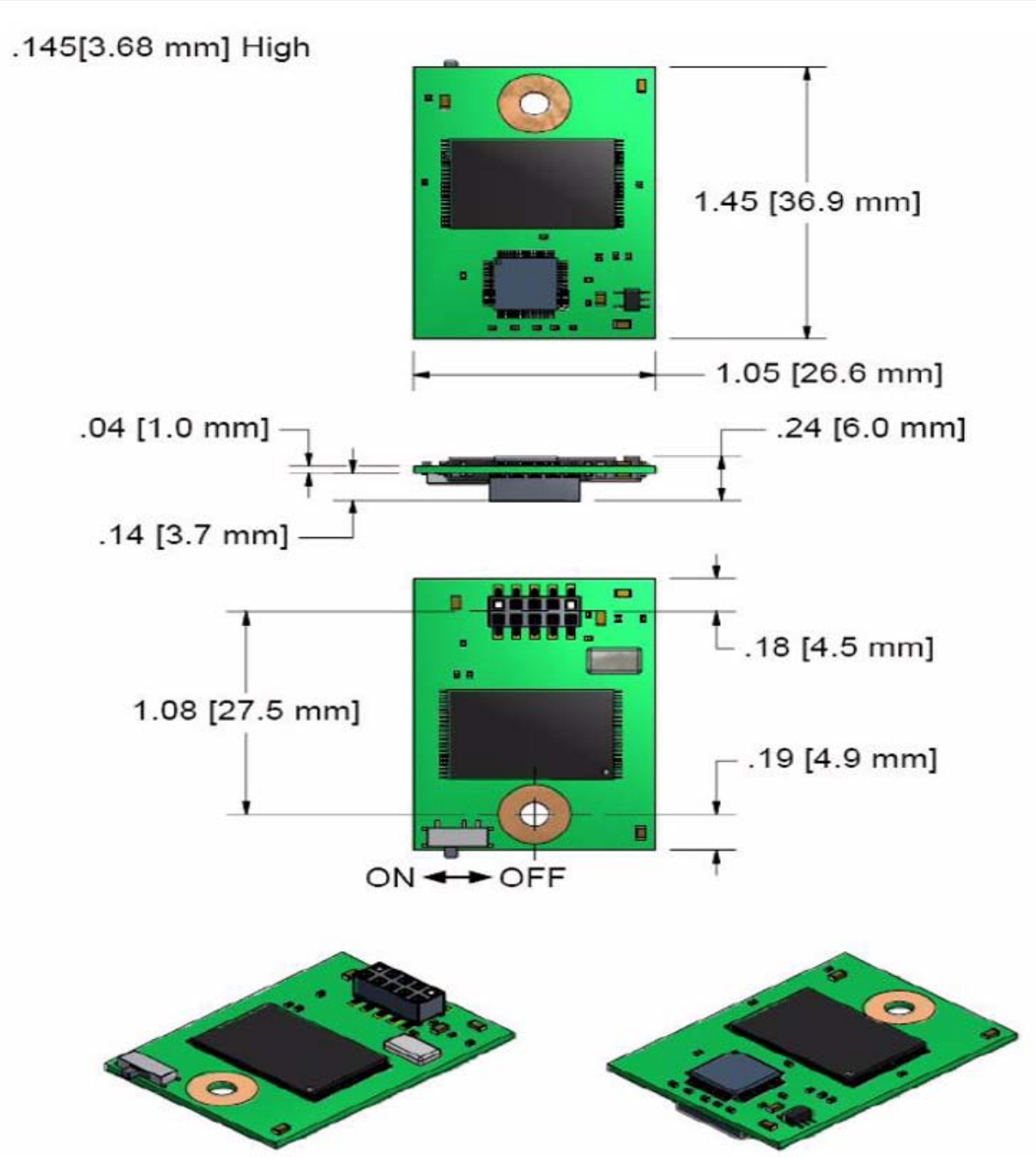


Figure 14: USB Flash Disk Overview

2.7.2 Serial ATA Extension Module

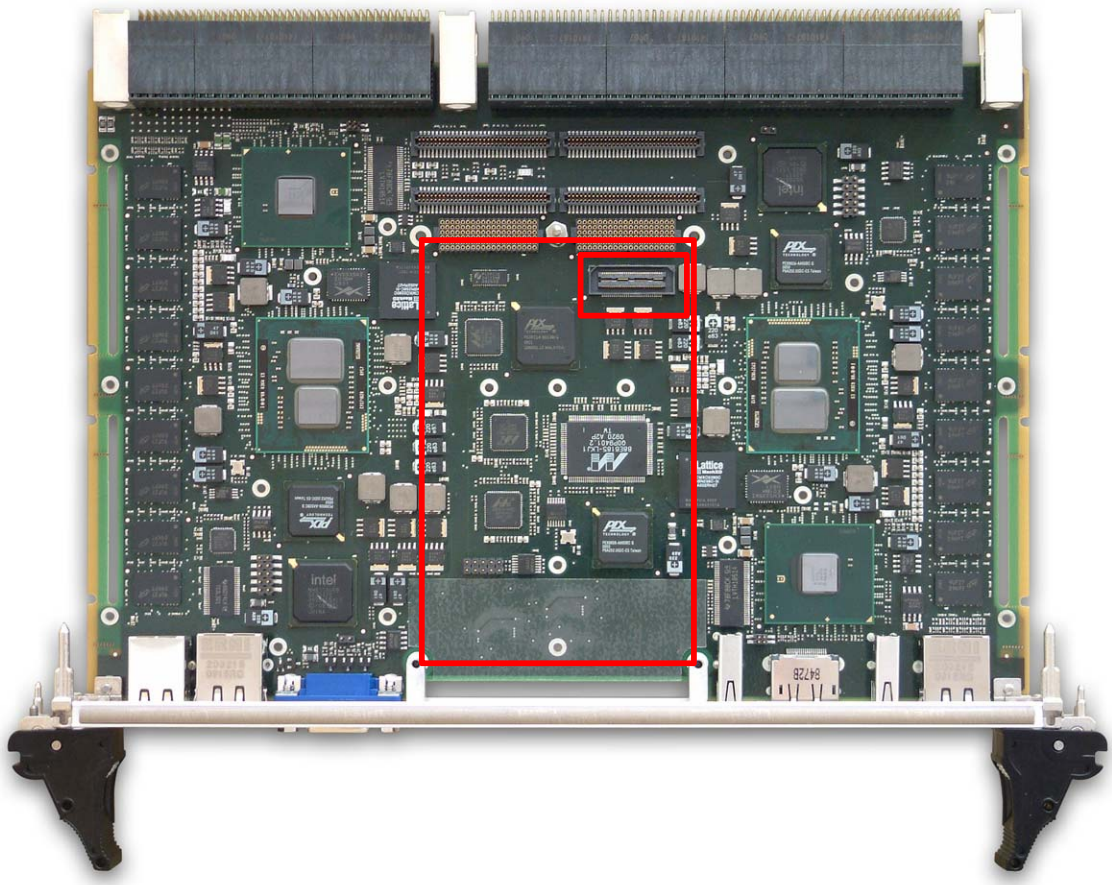


Figure 15: SATA Mezzanine Slot Location

A Serial ATA Extension Module SATA HDD may be connected to the VX6060 via the onboard SATA connector.

- This module must be installed only on the VX6060-SA boards.

If not already done, the SATA extension module must be physically installed on the VX6060 prior to installation of the VX6060 in a system.

During installation it is necessary to ensure that the SATA Flash module is properly seated in the onboard SATA connector, i.e. the pins are aligned correctly and not bent.

Figure 16: SATA Extension Module: Front and Bottom Viewes

The SATA extension module (order code: KIT-DISK25-SATA) is made up of:

- 1 plate fitted with SATA connectors
- 4x screws CZX-M3X5-INOX
- 4x screws CZX-M2.5X5-INOX

Installation process (if not already done):

1. Insert the SATA disk in the SATA connector. Example of SATA disk validated:
   - Manufacturer: Western Digital
   - Part No: SSD-D0015SI-5000
2. Fix the SATA disk to the plate using the four screws CZX-M3X5-INOX. Use medium strengh threadlocker (recommended torque of 0.4 Nm).
3. Plug the kit (plate and disk) on the VX6060 board, SATA connector (P5)
4. Fix the kit to the VX6060 board using the four screws CZX-M2.5X5-INOX. Use medium strengh threadlocker (recommended torque of 0.3 Nm).

Figure 17: Installation the Carrier SATA Board

2.7.3 Battery Replacement

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer.

Make sure not to remove the battery support, this could damage the heatsink.

To replace the battery, proceed as follows:

- Turn off power.
- Use a thin plastic tool to push the battery outside the safety cache. Push from the right or left top side of the safety cache.
- Remove the battery.
- Place the new battery in the socket.
- Make sure that you insert the battery the right way round. The plus pole must be on the top!

Care must be taken to ensure that the battery is correctly replaced.
The battery should be replaced only with an identical or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Reference of the battery used on the VX6060: RAYOVAC BR2032
The design of an electronic circuit powered by a component class battery requires the designer to consider two interacting paths that determine a battery's life: consumption of active electrochemical components and thermal wear-out.

Battery Life

CPUA or CPUB RTC consumption is close to 6 µA at 25°C (PCH specifications). BR2032 battery life on VX6060 at 25°C ambient temperature may reach 195 mAh/6 µA= 32500h= 3.7 years, without stand-by any power.
Figure 18 gives an estimate of years of service at various discharge currents for BR Lithium coin cells at room temperatures.

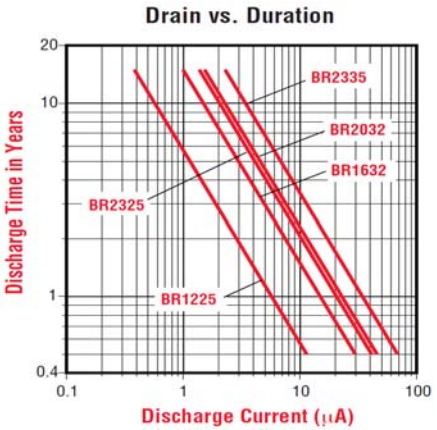


Figure 18: Battery Life

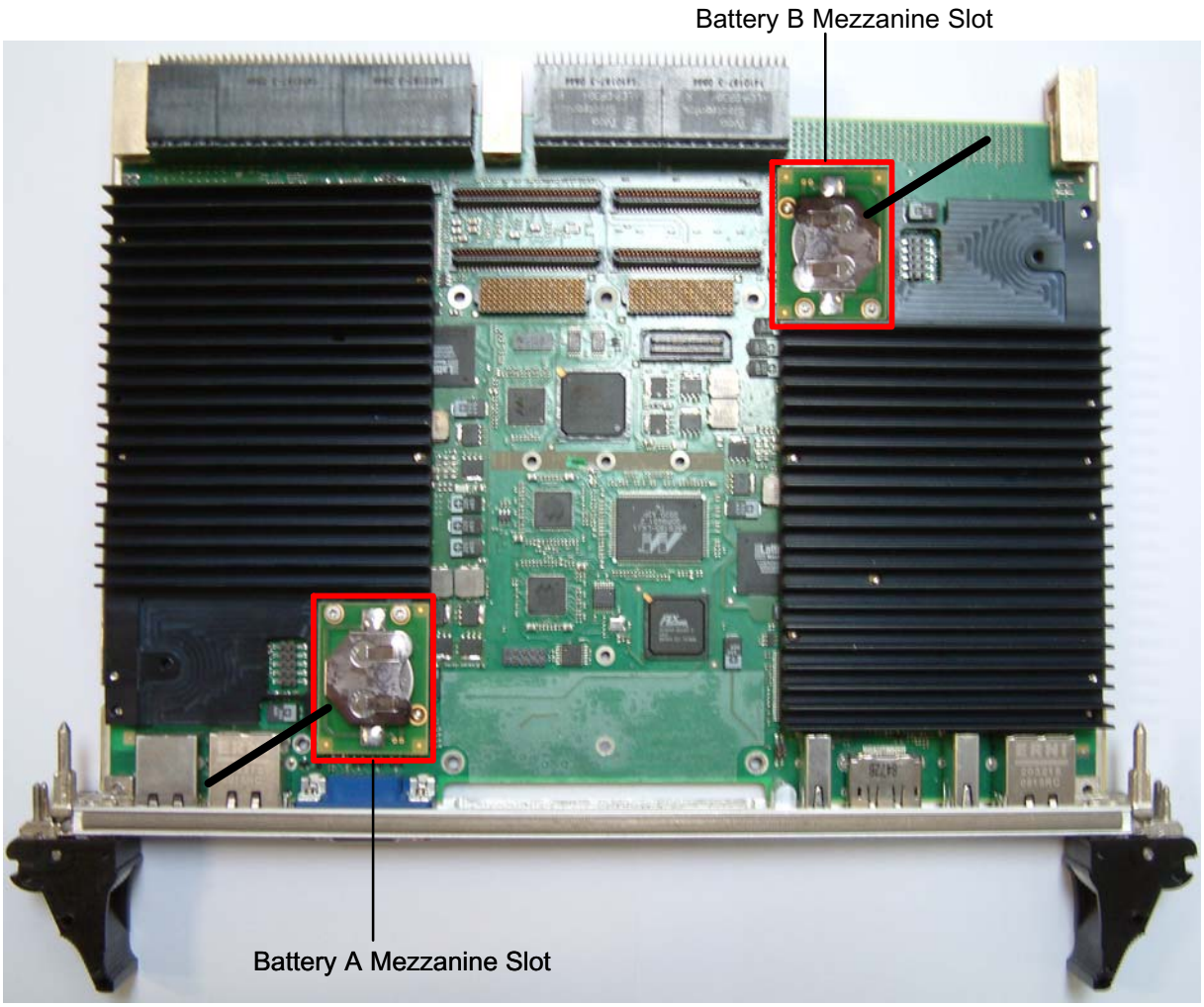


Figure 19: Battery Mezzanine Slots

2.8 PMC/XMC Installation

PMC/XMC modules are delivered with a full kit of parts for mounting them.

The installation of the PMC/XMC on the VX6060 conforms to the IEEE P1386.1 standard.

To install the PMC/XMC module, refer to Figure 20 and follow the steps below:

To avoid ESD damage, wear an antistatic wrist strap to discharge static electricity while performing any part of the installation that involves touching the VX6060 board or the XMC/PMC.
If you can't wear an antistatic wrist strap, touch one hand to the bare metal surface to provide grounding.

1. Place carefully the VX6060 with the backplane connectors facing you on a static dissipative surface connected to a common ground by a low-resistance connection. Do not slide the board over any surface.
2. Remove the blanking plate from the XMC/PMC slot of the VX6060.
3. Check that the standoffs are attached to the XMC/PMC.
4. Install the XMC/PMC, component-side down, aligning the PCI connectors with their mating connectors on the VX6060 and the XMC connector if available. Press them together so that the friction from the pins holds them together. Insert the standoff plug mounted on the VX6060 into the keyhole. The module's bezel will fill the slot and provide a connection to the module.
5. Screw the XMC/PMC in place using the 4 mounting points, on the bottom side of the VX6060 . You need a Phillips screwdriver for this stage.
6. The XMC/PMC attachment is now complete.
7. Insert the VX6060 into the chassis making sure it is plugged into the backplane.

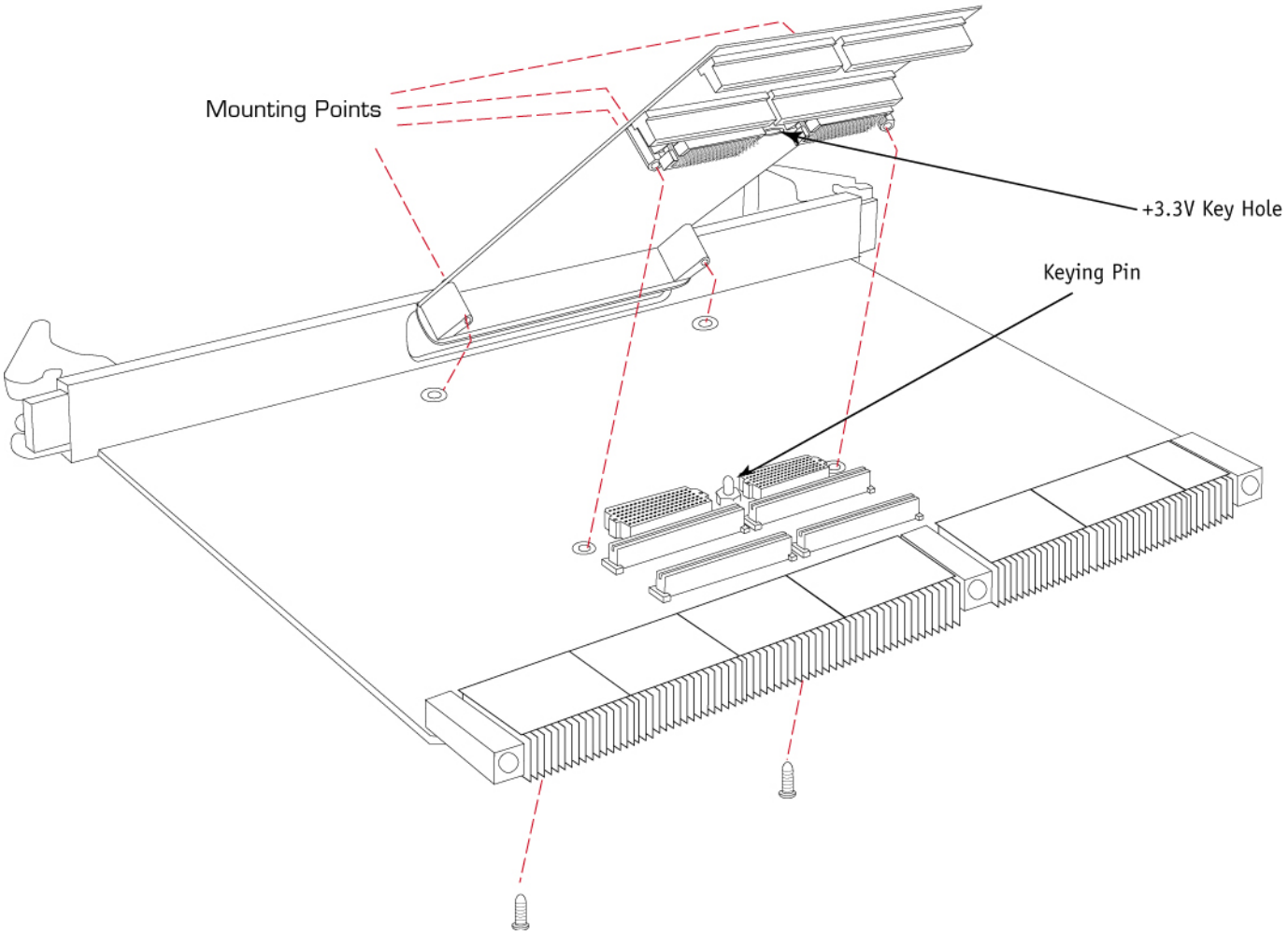


Figure 20: PMC/XMC Installation

XMC

The XMC board standard is based on the PMC mechanical definition, and occupies the same board area.

The XMC board add one or two new connectors to the connectors already on a PMC. The new connectors support high-speed differential signals for fabric communications.

Figure 21 shows a XMC fitted only with one XMC connector.

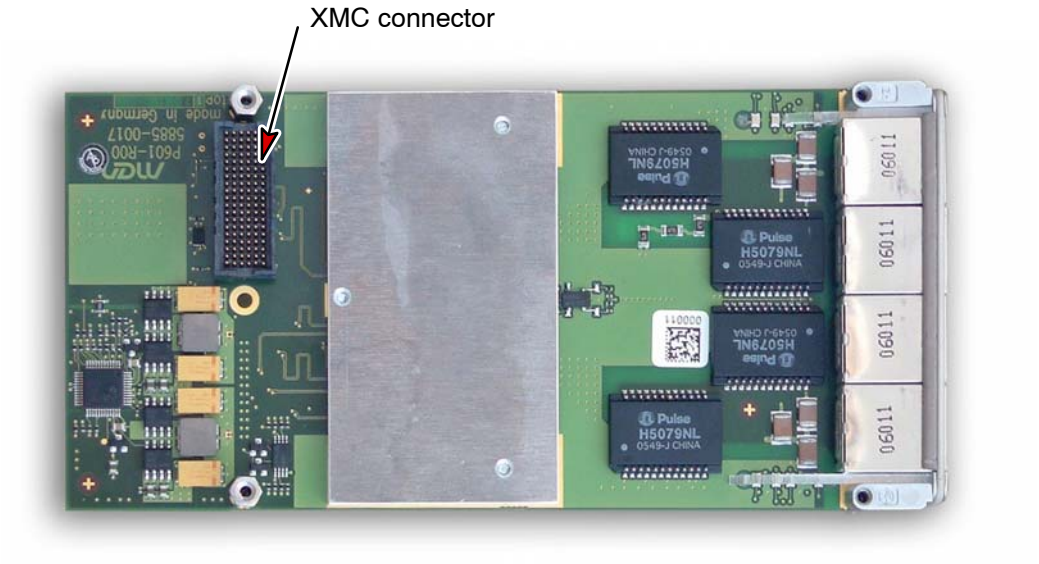


Figure 21: Example of XMC Board

Signaling Voltage Keying Pin

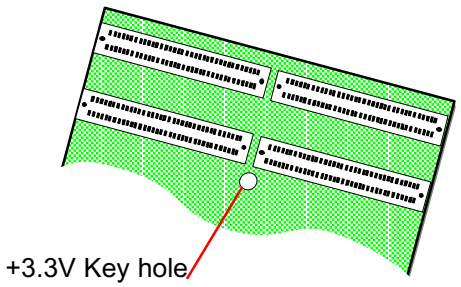
The 64-bit PCI bus of the VX6060 and the PMC plugged on the 64-bit PCI slot have to operate on the same signaling level. The VX6060 sets the signaling level for the 64-bit PCI bus to +3.3V (i.e. V(I/O)=+3.3V). The V(I/O) pins of the PCI PMC are connected to +3.3V.

The distinction between PMC types is the signaling level they use, not the power rails they connect to, nor the component technology they contain.

On the VX6060 PCI XMC/PMC slot, only two XMC/PMC types must be intalled:

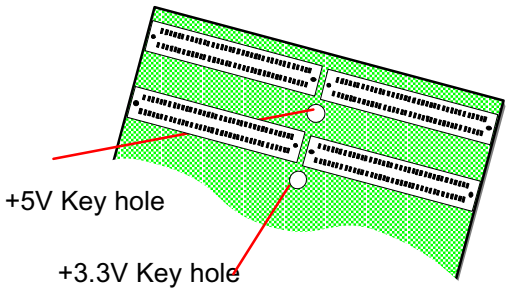
+3.3V PMC

It is designed to work only in a +3.3V signaling level and will only have a keying hole.



Universal PMC

It supports both voltages (+5V and +3.3V). This PMC is capable of detecting the signaling level in use and adapting itself to that environment. It has two keying holes (+5V and +3.3.V) and can, therefore, be plugged into either signaling level.



2.9 Software Installation

The installation of all onboard peripheral drivers is described in detail in the relevant Driver Kit files or Board Support Packages (BSP).

Installation of an operating system is a function of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.

Chapter 3 - Additional Board Features

3.1 Onboard Ethernet Central Switch

VX6060 features a powerful 10 ports Geth SerDes switch that allows flexible Interconnections.

Figure 22 “Onboard Ethernet Central Switch” shows the onboard ethernet network. The lanswitch directions are configured from the BIOS.

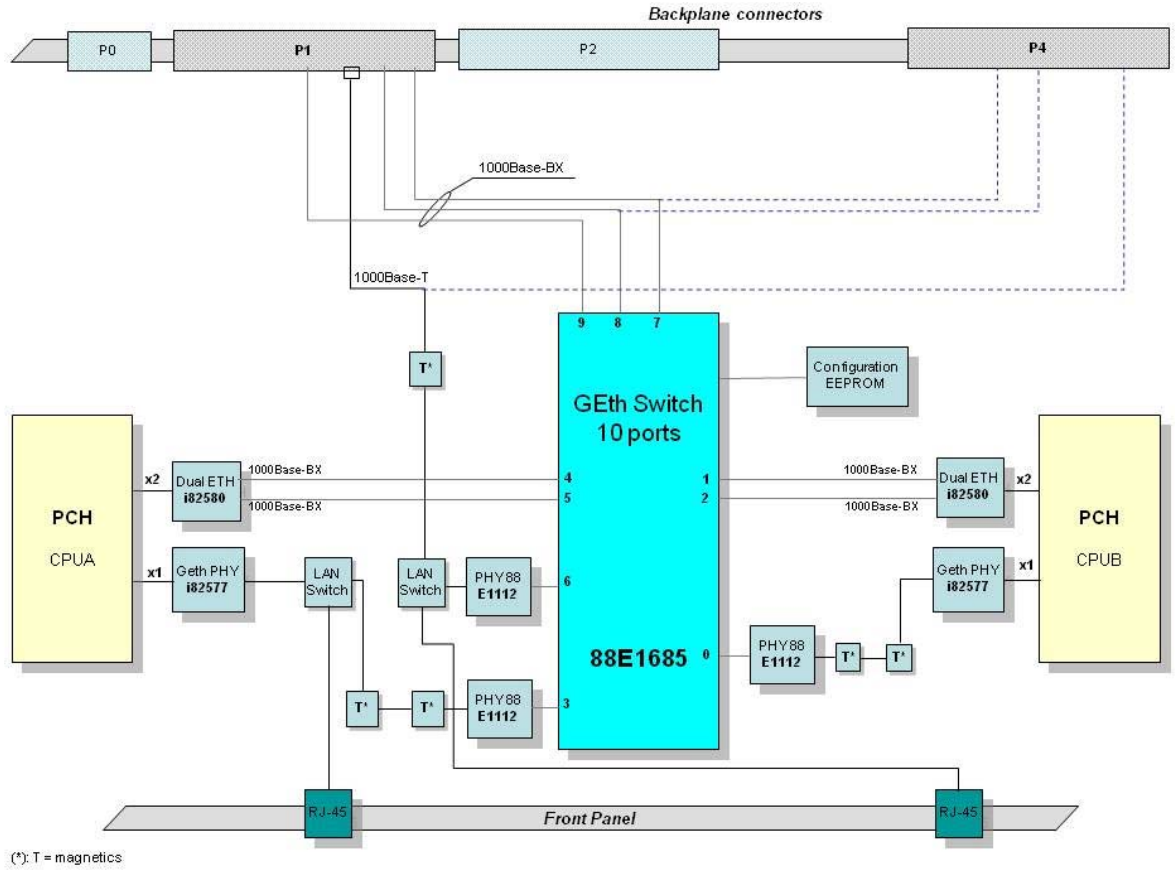


Figure 22: Onboard Ethernet Central Switch

3.2 RTC, Watchdog Timers

3.2.1 Real-Time Clock (RTC)

The following real time clocks are available on the VX6060 board.

- Real-Time Clock (RTC):

  The VX6060 is equipped with an onboard high-precision real-time clock. This real-time clock operates at very low power consumption. The standard equipment of the VX6060 includes a battery. The RTC is powered during the presence of the VPX 3.3V_AUX or 5V power or the battery.

- Hardware delay timer for short reliable delay times

  Internal RTC of the IbexPeak PCH is used for the VX6060.

  IbexPeak Time keeping features two banks of static RAM with 128 bytes each. Three interrupts are available.

  Each CPUA and CPUB RTC can be powered by an optional battery mezzanine, with a minimum 3 years lifetime at 25°C.

  The SBC can operate without the use of mezzanine batteries: CMOS memory and RTC will then not be preserved during the absence of power.

- Real Time Clock (RTC) stability:

  PCH offers internal RTC feature. This RTC stability depends on an external 32.768 KHz oscillator. This external oscillator (FC-135 family) has a parabolic coefficient of 0.4 ppm/°C² and +/-20 ppm stability at 25°C.

  At first order, only considering external oscillator parameters, PCH RTC stability for ambient temperature is 20ppm at 25°C. 20 ppm stability is equivalent to 10 mn/year, worse case.

3.2.2 Watchdog Timer

The timer is enabled by software. Once enabled it must be restarted at regular intervals. If it is not restarted the timer will expire and cause a Non-Maskable Interrupt (NMI) or reset to the local processor. Failure to trigger the Watchdog Timer in time results in an interrupt or a system reset.

3.2.3 CPLD Watchdog

The PLD includes a hardware Watchdog timer that can be used by the operating software to monitor the normal operation of the system.

The timer is enabled by software. Once enabled it must be restarted at regular intervals. If it is not restarted the timer will expire and cause a Non-Maskable Interrupt (NMI) or reset to the local processor.

The Watchdog module uses slow clock at **1 Hz** and it is composed by the following functions:

- Watchdog refresh function
- Clear watchdog register when reset occurs
- Watchdog timeout decoder:

  The timer timeout is programmable ranging from **1s to 510s** by 2s steps in the Watchdog Timer Control register

- Watchdog expiration mode management:

  The expiration mode is chosen in the Watchdog Timer Control register.

  There are 3 expiration modes:

  a. Timer only mode
  b. Reset mode
  c. Interrupt mode

3.3 I2C Structure

Each CPU subsystem features three I2C busses.

- The first one is attached to the PCH Platform Hub Controller and controls the DDR3 SPD EEPROM, the CK505 clock generator and, for CPUA only, the card Voltage monitoring device.
- The remaining i2C busses are handled by the CPLD device according Figure 23 “I2C Diagram”.

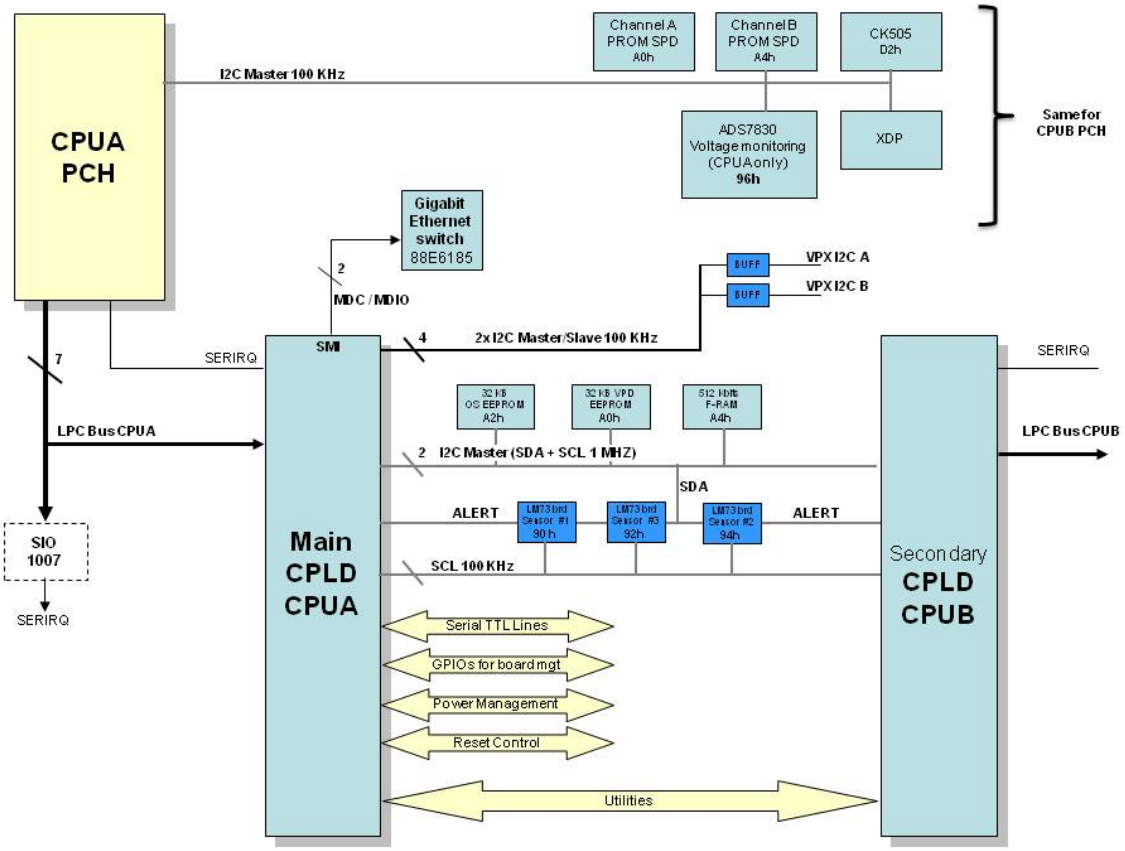


Figure 23: I2C Diagram

3.4 CPLD Features

The CPLD manages following features:

- Power-on/off control
- Reset control
- Local environmental control/monitoring
- LPC interface to processor
- I2C interfaces to P0 VPX real panel
- LEDs control
- Serial lines multiplexer
- Serial VPD and user memories
- User and system GPIOs
- Communication between subsystem A and subsystem B
- Internal registers that allow system management

VX6060 VPX I2C interfaces

VX6060 implements two I2C buses connected to P0 VPX connector (see P0 pin assignments):

I2C0 : CLK signal on pin P0/B5, DATA signal on pin P0/ A5

I2C1: CLK signal on pin P0/G4, DATA signal on pin P0/ F4

I2C bus 0 is a master/slave interface .

I2C bus 1 is a master only interface .

- **VPX I2C bus 0 / 1 master interfaces:**
  I2C bus 0/1 master interfaces software tools are described in Fedora relase note (mettre la bonne ref)
- **VPX I2C bus 0 slave interface:**
  VX6060 board I2C bus 0 slave register base address depends on VPX slot ID (slot geographical address):
  VPX Slot 1 (syscon): VX6060 slave I2C base address is 0x18 (I2C 7bits addressing)
  VPX Slot 2: VX6060 slave I2C base address is 0x19 (I2C 7bits addressing)
  VPX Slot 3: VX6060 slave I2C base address is 0x1A (I2C 7bits addressing)
  And so on…..

➢ I2C bus 0 slave registers definition :

I2C_BOARD_STATUS @(Base_address) – When bit 3 of Register @(Base_address + 1) is set to 0				
Bit#	Name	Description	Reset	Type
7	Power Status	Power Status 0 Power Stand By 1 Power ON	0	RO
6-5	Reset Source	Last Reset Source 0x000 PWRGD_P3V3SB 0x001 Watchdog Expired 0x010 SYSRESET_INb 0x011 Maskable Reset	0	RO
4	Reset Status	Reset Status Side A 0 No PWOK 1 PWOK	0	RO
3-0	Boot Status	Boot Status These bits are Read Only through I2C Slave Interface and R/W through LPC Interface	0	RW

I2C_BOARD_STATUS @(Base_address) – when bit 3 register @(Base_address + 1) is set to 1				
Bit#	Name	Description	Reset	Type
7-0	Power Debug 1	This register indicates State of Powers when a power error occurs (falling of one of the PWRGDG_XX signals). This register is re-initialized only when Stand By power is down. Bit 7 : PWRGD_DDR Bit 6 : PWRGD_GFXCORE Bit 5 : PWRGD_P1V0 Bit 4 : PWRGD_P1V0_6U Bit 3 : PWRGD_P1V05IBEX Bit 2 : PWRGD_P1V05S Bit 1 : PWRGD_P1V2_6U Bit 0 : PWRGD_P1V5_6U	0	RO

I2C_BOARD_CONTROL @(Base_address + 1) – when Bit 3 of this register is set to 0				
Bit#	Name	Description	Reset	Type
7-4	Board Id	**Board Identification** 0x0110 VX6060 0x0011 VX3030	0	RO
3	Check_Errors	**Error Status Selection** 0 Default meaning for register @ 72 and register @73 1 Select Error Status for register @ 72 and register @73	0	RW
2	Reset_3UB	**Reset Side B** 0 No Reset 1 Reset Assert	0	RW
1	Reset_3UA	**Reset Side A** 0 No Reset 1 Reset Assert	0	RW
0	Power_OnOff	**Power On/Off Control** 0 = Power Off (Go to StandBy) 1 = Power On This control bit is valid only if POWER_MODE Dip Switch is on High State (See bit 7 of register @04 for its value)	0	RW

I2C_BOARD_CONTROL @(Base_address + 1) - when Bit 3 of this register is set to 1				
Bit#	Name	Description	Reset	Type
7-4	Error Status	**Error Status** Bit 7 Cross Power Error Bit 6 : Power Error Bit 5 : Fatal Alert Bit 4 : Power Timeout **This register is re-initialized only when Stand By power is down.**	0	RO
3	Check_Errors	**Error Status Selection** 0 Default meaning for register @ 72 and register @73 1 Select Error Status for register @ 72 and register @73	0	RW
2-0	Power Debug 2	**This register indicates State of Powers when a power error occurs (falling of one of the PWRGDG_XX signals).** **This register is re-initialized only when Stand By power is down.** Bit 2 : PWRGD_P1V8S, , } Bit 1: PWRGD_P2V5 Bit 0 : PWRGD_P3V3_6U	0	RW

3.5 Serial Lines EIA-422/485 Additional Modes

A total of 4 simplified lines are available on VX6060 product, two from CPUA and two from CPUB.

EIA-232 serial lines mode are available on front panel RJ11 and VPX P2 connectors.

See section 4.1.1 page 49 - “Serial Connector - COM-AB” and section 4.3.3 page 62 - “P2 Connector” for more information on pin assignments.

EIA-232 serial lines mode is the default mode, but EIA-422/485 mode can also be set with the following mode:

Mode	RJ11 fron panel connector	P2 reap VPX connector	RJ11 front pin assignment	P2 rear pin assignment
Default EIA-232	EIA-232: COM1-A and COM1-B	EIA-232: COM1-A, COM2-A, COM1-B and COM2-B	COM1-A TXD: pin 3 COM1-A RXD: pin 4 COM1-B TXD: pin 1 COM1-B RXD: pin 6	COM2-A TXD: pin G1 COM1-A TXD: pin G3 COM2-A RXD: pin G5 COM1-A RXD: pin G7 COM2-B TXD: pin G9 COM1-B TXD: pin G11 COM2-B RXD: pin G13 COM1-B RXD: pin G15
422/485 on COM1-B rear P2	EIA-232: COM1-A	EIA-232: COM1-A EIA-422/485: COM1-B	COM1-A TXD: pin 3 COM1-A RXD: pin 4	COM1-A TXD: pin G3 COM1-A RXD: pin G7 pin G1 and pin G5 reserved COM1-B TXD-: pin G9 COM1-B TXD+: pin G11 COM1-B RXD+: pin G13 COM1-B RXD-: pin G15
422/485 on rear P2	None	EIA-422/485: COM1-A and COM1-B	Reserved	COM1-A TXD+: pin G1 COM1-A TXD-: pin G3 COM1-A RXD+: pin G5 COM1-A RXD-: pin G7 COM1-B TXD-: pin G9 COM1-B TXD+: pin G11 COM1-B RXD+: pin G13 COM1-B RXD-: pin G15
EIA-232 COM1 cross link	EIA-232: COM1-A and COM1-B	EIA-232: COM1-A, COM1-B COM2-A and COM2-B linked for A/B extended communication	COM1-A TXD: pin 3 COM1-A RXD: pin 4 COM1-B TXD: pin 1 COM1-B RXD: pin 6	COM1-A TXD: pin G3 COM1-A RXD: pin G7 pin G1 and pin G5 reserved COM1-B TXD: pin G11 COM1-B RXD: pin G15 pin G9 and G13 reserved

Chapter 4 - Physical I/O

4.1 Front Panel Connectors

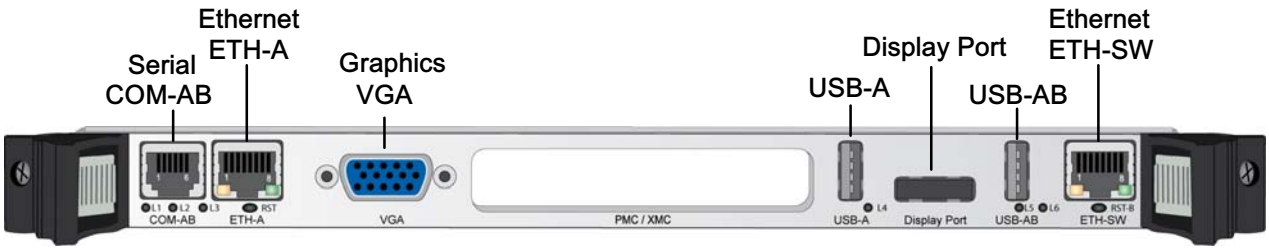


Figure 24: Location of the Front Panel Connectors

4.1.1 Serial Connector - COM-AB

Pin Assignment

Pin	Signal	Description
1	COM1−B TXD	COM1−B EIA−232 Transmit Data
2	Shell	Chassis Ground
3	COM1−A TXD	COM1−A EIA−232 Transmit Data
4	COM1-A RXD	COM1-A EIA-232 ReceiveData
5	GND	Electrical Ground
6	COM1−B RXD	COM1−B EIA−232 Receive Data

Table 12: Serial Connector Pin Assignment

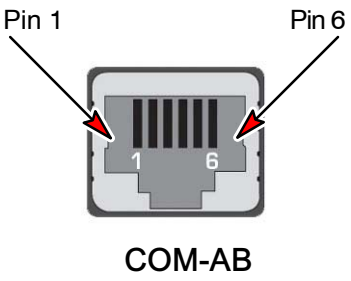


Figure 25: Serial Connector

A serial line should only be used via one connector at the same time, either the Serial front panel connector or the P2 connector.

Kontron provides a specific connection kit Order Code: KIT-2X-RJ12DB9. It includes one RJ-12 cable and two DB9 female adapter tagged CPUA and CPUB. The serial line to CPUA or CPUB will be reachable using the DB9 female adapter tagged CPUA or CPUB.

4.1.2 Gigabit Ethernet Connectors - ETH-A and ETH-SW

The Ethernet transmission should operate using a CAT5 cable with a maximum length of 100 m.

The Ethernet connectors are available as RJ-45 connectors with tab down. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

Pin Assignment

PIN	10BASE-T		100BASE-TX		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_DA+
2	O	TX-	O	TX-	I/O	BI_DA-
3	I	RX+	I	RX+	I/O	BI_DB+
4	-	-	-		I/O	BI_DC+
5	-	-	-		I/O	BI_DC-
6	I	RX-	I	RX-	I/O	BI_DB-
7	-	-	-		I/O	BI_DD+
8	-	-	-		I/O	BI_DD-
Shell	Chassis Ground					

Table 13: Gigabit Ethernet Connectors Pin Assignment

Figure 26: Ethernet Connector

Ethernet ETH-A LEDs Status

> LNK/ACT (green)

This LED monitors network connection and activity. The LED lights up when a valid link (cable connection) has been established. The LED goes temporarily off if network packets are being sent or received through the RJ-45 port. When this LED remains off, a valid link has not been established due to a missing or a faulty cable connection.

> SPEED LED (yellow/green)

This LED indicates the link speed (10, 100, 1000 Mbps).

STATUS		SPEED LED yellow/green	LNK/ACT LED green
Ethernet Link is not established		OFF	OFF
10 Mbps	Ethernet Link Established	OFF	ON
	Ethernet Link Activity	OFF	BLINK
100 Mbps	Ethernet Link Established	ON (green)	ON
	Ethernet Link Activity	ON (green)	BLINK
1000 Mbps	Ethernet Link Established	ON (yellow)	ON
	Ethernet Link Activity	ON (yellow)	BLINK

Table 14: Ethernet ETH-A LEDs Status Definition

Ethernet ETH-SW LEDs Status

- LNK/ACT (green)
  This LED monitors network connection and activity for 100 / 1000 Mbps ethernet links.
- SPEED LED (yellow/green)
  This LED indicates the link speed (10, 100, 1000 Mbps) and network connection / activity for 10 Mbps ethernet links.

STATUS		SPEED LED yellow/green	LNK/ACT LED green
Ethernet Link is not established		OFF	OFF
10 Mbps	Ethernet Link Established	ON (yellow)	OFF
	Ethernet Link Activity	BLINK (yellow)	OFF
100 Mbps	Ethernet Link Established	ON (green)	ON
	Ethernet Link Activity	BLINK (green)	BLINK
1000 Mbps	Ethernet Link Established	OFF	ON
	Ethernet Link Activity	OFF	BLINK

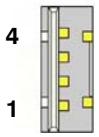
Table 15: Ethernet ETH-SW LEDs Status Definition

4.1.3 USB Connector - USB-A and USB-AB

Pin Assignment

PIN	SIGNAL	FUNCTION	I/O
1	VCC (+5V Protected)	VCC	--
2	USB_D-	Differential USB-	I/O
3	USB_D+	Differential USB+	I/O
4	GND	GND	--

Table 16: USB Connector Pin Assignment



USB-A
USB-AB

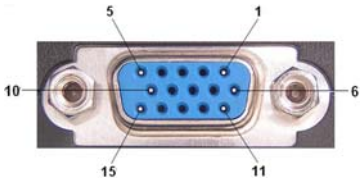
Figure 27: USB Connector

4.1.4 VGA Connector

Pin Assignment

PIN	SIGNAL	FUNCTION	I/O
1	Red	Red Video Signal Output	O
2	Green	Green Video Signal Output	O
3	Blue	Blue Video Signal Output	O
4	N.C.	Not Connected	-
5	GND	Ground Signal	-
6	GND	Ground Signal	-
7	GND	Ground Signal	-
8	GND	Ground Signal	-
9	VCC	Power +5V 1.5 A fuse protection	O
10	GND	Ground Signal	-
11	N.C.	Not Connected	-
12	Sdata	I2C Data	I/O
13	Hsync	Horizontal Sync	TTL Out
14	Vsync	Vertical Sync	TTL Out
15	Sclk	I2C Clock	I/O

Table 17: VGA Connector Pin Assignment



VGA

Figure 28: VGA Connector

4.1.5 DisplayPort Connector

Pin Assignment

PIN	SIGNAL	FUNCTION
1	ML_Lane 0 (p)	Lane 0 (positive)
2	GND	Ground
3	ML_Lane 0 (n)	Lane 0 (negative)
4	ML_Lane 1 (p)	Lane 1 (positive)
5	GND	Ground
6	ML_Lane 1 (n)	Lane 1 (negative)
7	ML_Lane 2 (p)	Lane 2 (positive)
8	GND	Ground
9	ML_Lane 2 (n)	Lane 2 (negative)
10	ML_Lane 3 (p)	Lane 3 (positive)
11	GND	Ground
12	ML_Lane 3 (n)	Lane 3 (negative)
13	GND	Ground
14	GND	Ground
15	AUX CH (p)	Auxiliary Channel (positive)
16	GND	Ground
17	AUX CH (n)	Auxiliary Channel (negative)
18	Hot Plug	Hot Plug Detect
19	Return	Return for power
20	DP_PWR	Power for connector

Table 18: DisplayPort Pin Assignment

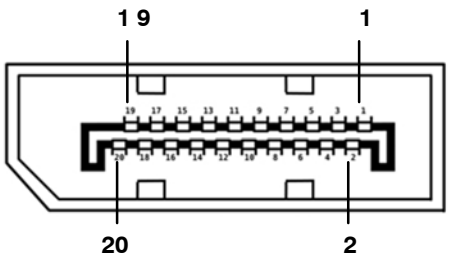


Figure 29: DisplayPort Connector

4.2 Onboard Connectors

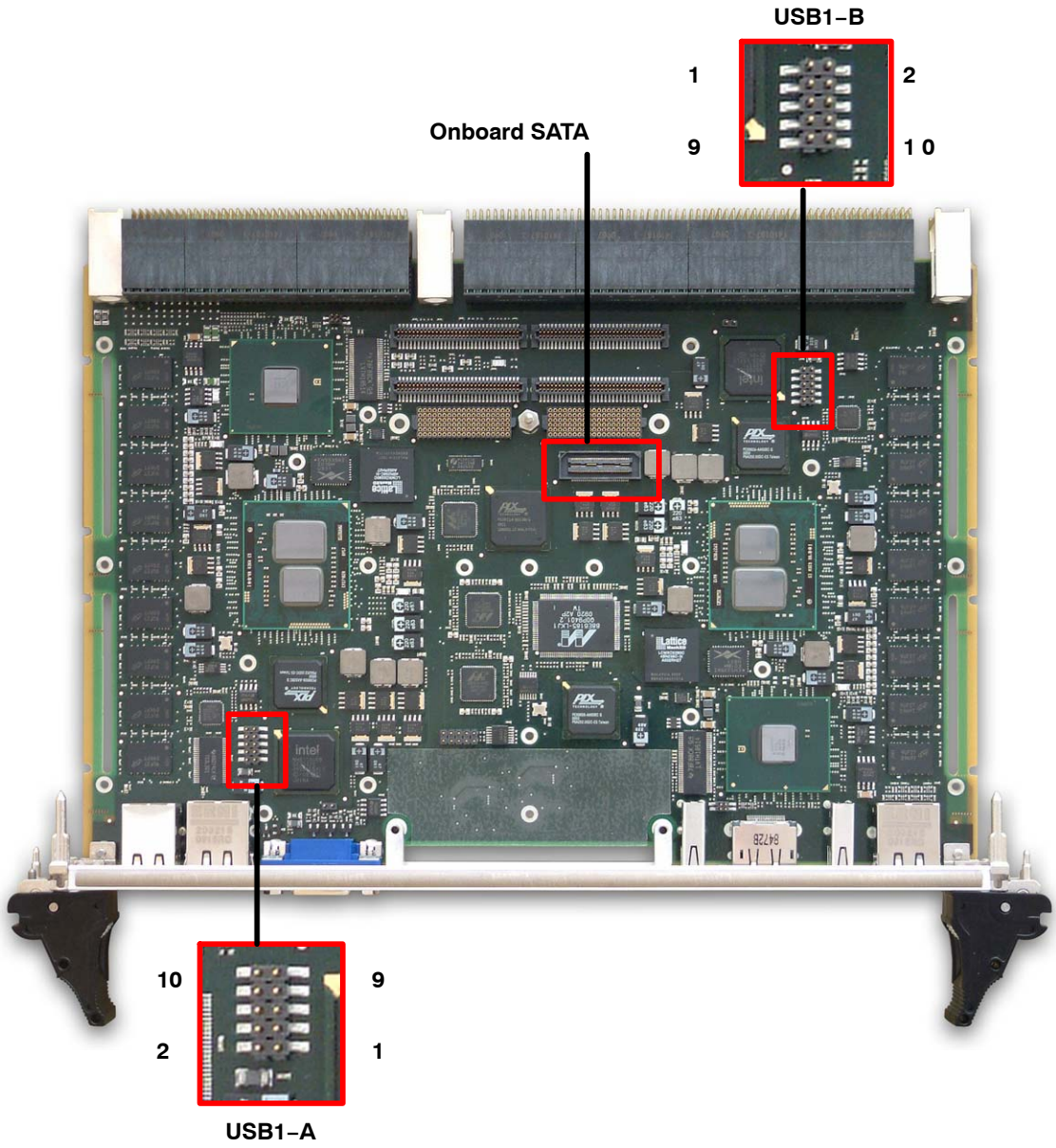


Figure 30: Onboard Connectors

Onboard USB - USB1-A and USB1-B

The onboard USB device is used to connect an USB Flash Disk Module (low profile USB flash mezzanine card, 2 mm connector).

The following table provides pinout information for the onboard USB connector USB1-A (USB1-B) mezzanine slot:

PIN	SIGNAL	FUNCTION	I/O
1	PWR	VCC	-
2	RSV	Reserved	-
3	Data-	Differential USB-	I/O
4	RSV	Reserved	-
5	Data+	Differential USB+	I/O
6	RSV	Reserved	-
7	GND	Ground	-
8	RSV	Reserved	-
9	N.C.	Not Connected	-
10	RSV	Reserved	-

Table 19: Onboard USB Pin Assignment

Onboard SATA - SATA3-A

The VX6060 provides a SATA connector, which is used to connect a HDD carrier.

PIN	SIGNAL	FUNCTION	I/O
1	GND	Ground Signal	-
2 .. 6	N.C.	Not Connected	-
7	GND	Ground Signal	-
8 .. 12	N.C.	Not Connected	-
13	GND	Ground Signal	-
14	N.C.	Not Connected	-
15	SATA3-A RX-	Differential Receive -	I
16	GND	Ground Signal	-
17	SATA3-A RX+	Differential Receive +	I
18	+5V		-
19	GND	Ground Signal	-
20	+5V		-
21	SATA3-A TX+	Differential Transmit +	O
22	+5V		-
23	SATA3-A TX-	Differential Transmit -	O
24 .. 25	GND	Ground Signal	-
26	+3.3V		-
27	N.C.	Not Connected	-
28	+3.3V		-
29 .. 46	N.C.	Not Connected	-
47	GND	Ground Signal	-
48	N.C.	Not Connected	-
49	Reserved	Reserved. Do not connect.	-
50	N.C.	Not Connected	-
51	Reserved	Reserved. Do not connect.	-
52	N.C.	Not Connected	-
53	GND	Ground Signal	-
54	N.C.	Not Connected	-
55	Reserved	Reserved. Do not connect.	-
56	N.C.	Not Connected	-
57	Reserved	Reserved. Do not connect.	-
58	N.C.	Not Connected	-
59	GND	Ground Signal	-
60	N.C.	Not Connected	-

Table 20: Onboard SATA Pin Assignment

4.3 Rear Connectors

VPX Bus Interface

The complete 6U VPX connector configuration comprises seven connectors named P0 to P6:

- P0: 8-wafer 7-row connector.
- P1 to P4: 16-wafer 7-row differential connectors.
- P5 to P6: not used and not equipped.

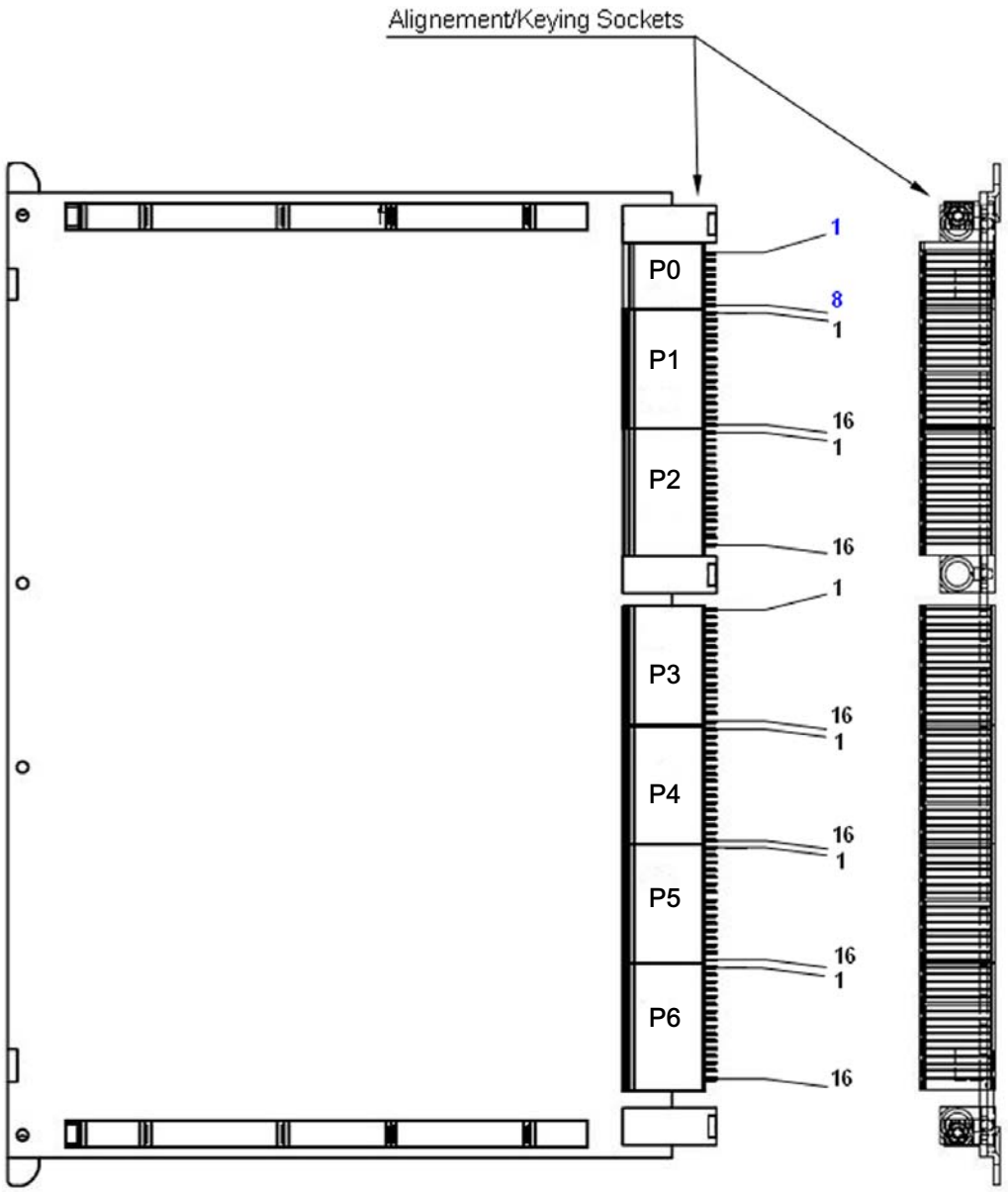


Figure 31: VPX Connectors

4.3.1 P0 Connector

P0 Wafer Assignment

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	+12V	+12V	+12V	NC	NC (+12V)	NC (+12V)	NC (+12V)
2	+12V	+12V	+12V	NC	NC (+12V)	NC (+12V)	NC (+12V)
3	+5V	+5V	+5V	NC	+5V	+5V	+5V
4	I2C1 CLK	I2C1 DAT	GND	-12V_AUX	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3V3_AUX	GND	I2C0 CLK	I2C0 DAT
6	GA3*	GA2*	GND	NC (+12V_AUX)	GND	GA1*	GA0*
7	GPIO5 (TCK)	GND	PCIe_CLK- (TDO)	PCIe_CLK+ (TDI)	GND	GPIO3 (TMS)	GPI04 (TRST)
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND
CASE	GND						

* signal active when low

Table 21: VPX Connector P0 Wafer Assignment

P0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
+12V	+12 Volts DC power (VS1 VPX supply). NC (+12V) pins are not connected (VS2 VPX supply)
-12V_AUX	-12 Volts auxiliary power. Only used on PMC connector.
+5V	+5 Volts DC power (VS3 VPX supply)
NC	Not Connected
NVMRO	Non-Volatile Memory Read Only. When asserted (logical 1), prevents any non-volatile memory from being updated.
GAi	Geographical address pins
GAP	Geographical address parity
GND	Ground
GPIO	General Purpose I/O (handled by the CPLD A). JTAG signals are not used on P0.
I2C0	I2C Bus 0
I2C1	I2C Bus 1
REF_CLK+/-	The Reference Clock is a bussed differential pair. Output if the VX6060 is plugged in the system controller slot, input otherwise. It enables the entire system to synchronize to a common time reference if desired. Counter/timer in the CPLD can use this clock
AUX_CLK+/-	1 PPS (one pulse per second) clock input. Can be programmed as an output on system controller slot. Can be used to phase the CPLD timer/counter clocked by REF_CLK+/-.
PCIe_CLK+/-	Optional Common Reference PCI Express Clock input. Can also be programmed as an output.
SYSRESET*	System Reset. Input and open collector output.

Table 22: VPX Connector P0 Signal Definition

4.3.2 P1 Connector

» P1 Wafer Assignment

> Legend for Table 23:

ETH-SW	Gigabit Ethernet port	ETH-SW*x* TX/RX	1000BASE-BX link *x*
PCIe0-A L*x*RX | L*x*TX	x4 or 4x1 PCI-Express from CPUA	SATA0-A | SATA0-B	Serial ATA link 0 from CPUA | CPUB
PCIe0-B L*x*RX | L*x*TX	x4 or 4x1 PCI-Express from CPUB	USB2-A | USB2-B	USB link 0 from CPUA | CPUB
GPIO*x*	GPIO		

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	GDISCRETE1	GND	PCIe0-A L0-TX-	PCIe0-A L0-TX+	GND	PCIe0-A L0-RX-	PCIe0-A L0-RX+
2	GND	PCIe0-A L1-TX-	PCIe0-A L1-TX+	GND	PCIe0-A L1-RX-	PCIe0-A L1-RX+	GND
3	VBAT	GND	PCIe0-A L2-TX-	PCIe0-A L2-TX+	GND	PCIe0-A L2-RX-	PCIe0-A L2-RX+
4	GND	PCIe0-A L3-TX-	PCIe0-A L3-TX+	GND	PCIe0-A L3-RX-	PCIe0-A L3-RX+	GND
5	SYS_CON*	GND	PCIe0-B L0-TX-	PCIe0-B L0-TX+	GND	PCIe0-B L0-RX-	PCIe0-B L0-RX+
6	GND	PCIe0-B L1-TX-	PCIe0-B L1-TX+	GND	PCIe0-B L1-RX-	PCIe0-B L1-RX+	GND
7	Reserved	GND	PCIe0-B L2-TX-	PCIe0-B L2-TX+	GND	PCIe0-B L2-RX-	PCIe0-B L2-RX+
8	GND	PCIe0-B L3-TX-	PCIe0-B L3-TX+	GND	PCIe0-B L3-RX-	PCIe0-B L3-RX+	GND
9	USB2-A PWR	GND	SATA0-A TX-	SATA0-A TX+	GND	SATA0-A RX-	SATA0-A RX+
10	GND	SATA0-B TX-	SATA0-B TX+	GND	SATA0-B RX-	SATA0-B RX+	GND
11	USB2-B PWR	GND	ETH-SW2 TX-	ETH-SW2 TX+	GND	ETH-SW2 RX-	ETH-SW2 RX+
12	GND	USB2-A D-	USB2-A D+	GND	USB2-B D-	USB2-B D+	GND
13	Reserved	GND	ETH-SW DB- (1)	ETH-SW DB+ (1)	GND	ETH-SW DA- (1)	ETH-SW DA+ (1)
14	GND	ETH-SW DD- (1)	ETH-SW DD+ (1)	GND	ETH-SW DC- (1)	ETH-SW DC+ (1)	GND
15	Maskable Reset* or GPIO2	GND	ETH-SW1 TX- (1)	ETH-SW1 TX+ (1)	GND	ETH-SW1 RX- (1)	ETH-SW1 RX+ (1)
16	GND	ETH-SW0 TX- (1)	ETH-SW0 TX+ (1)	GND	ETH-SW0 RX- (1)	ETH-SW0 RX+ (1)	GND
CASE	GND						

* signal active when low

(1) Only present for ethernet on P1 order option, otherwise not connected.

Table 23: VPX Connector P1 Wafer Assignment

P1 Signal Definition

MNEMONIC	SIGNAL DEFINITION
PCIe0-A | PCIe0-B L*x*-RX+/-	x4 PCI Express Link on CPUA or CPUB . Receive +/- Can also be used as a 4 x1 links.
PCIe0-A | PCIe0-B L*x*-TX+/-	x4 PCI Express Link on CPUA or CPUB . Transmit +/- Can also be used as a 4 x1 links.
SATA0-A | SATA0-B - RX+/-	Serial ATA on CPUA or CPUB. Receive +/-
SATA0-A | SATA0-B - TX+/-	Serial ATA on CPUA or CPUB. Transmit +/-
USB2-A | USB2-B - PWR	USB Power on CPUA or CPUB
USB2-A | USB2-B - D+/-	Differential Data pair of USB on CPUA or CPUB
ETH-SW*x* RX+/-	1000BASE-BX Links x from onboard central ethernet switch. Receive +/- ETH-SW0 and ETH-SW1 only present for ethernet on P1 order option, otherwise not connected.
ETH-SW*x* TX+/-	1000BASE-BX Links x from onboard central ethernet switch. Transmit +/- ETH-SW0 and ETH-SW1 only present for ethernet on P1 order option, otherwise not connected.
ETH-SW - DA+/-	Ethernet 1000BASE-T: First pair of transmit/receive data. Only present for ethernet on P1 order option, otherwise not connected.
ETH-SW - DB+/-	Ethernet 1000BASE-T: Second pair of transmit/receive data. Only present for ethernet on P1 order option, otherwise not connected.
ETH-SW - DC+/-	Ethernet 1000BASE-T: Third pair of transmit/receive data. Only present for ethernet on P1 order option, otherwise not connected.
ETH-SW - DD+/-	Ethernet 1000BASE-T: Fourth pair of transmit/receive data Only present for ethernet on P1 order option, otherwise not connected.
GPIOx	General Purpose I/Ox (handled by the CPLD A)
Maskable Reset*	Optional reset input for this module. May be left unconnected if not used.
GND	Ground
SYS_CON*	System Controller Slot Indication
VBAT	Battery Voltage Input, 3V. Optional alternated source for RTC backup voltage.

Table 24: VPX Connector P1 Signal Definition

4.3.3 P2 Connector

P2 Wafer Assignment

> Legend for Table 25:

COM*x*-A | COM*x*-B RXD	Simplified EIA-232 port *x* from CPUA | CPUB Receive Data	SATA*x*-A	Serial ATA link *x* from CPUA
COM*x*-A | COM*x*-B TXD	Simplified EIA-232 port *x* from CPUA | CPUB Transmit Data	USB3-A | USB3-B	USB link 3 from CPUA | CPUB
eDP1-A | eDP1-B	embedded Display Port from CPUA | CPUB		

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	COM2-A TXD	GND	SATA1-A TX-	SATA1-A TX+	GND	SATA1-A RX-	SATA1-A RX+
2	GND	SATA2-A TX-	SATA2-A TX+	GND	SATA2-A RX-	SATA2-A RX+	GND
3	COM1-A TXD	GND	USB3-A PWR	USB3-A PWR	GND	USB3-B PWR	USB3-B PWR
4	GND	USB3-A D-	USB3-A D+	GND	USB3-B D-	USB3-B D+	GND
5	COM2-A RXD	GND	eDP1-A 1-	eDP1-A 1+	GND	eDP1-A 0-	eDP1-A 0+
6	GND	eDP1-A 3-	eDP1-A 3+	GND	eDP1-A 2-	eDP1-A 2+	GND
7	COM1-A RXD	GND	eDP1-B HPD	eDP1-A HPD	GND	eDP1-A AUX-	eDP1-A AUX+
8	GND	eDP1-B 1-	eDP1-B 1+	GND	eDP1-B 0-	eDP1-B 0+	GND
9	COM2-B TXD	GND	eDP1-B 3-	eDP1-B 3+	GND	eDP1-B 2-	eDP1-B 2+
10	GND	Reserved	Reserved	GND	eDP1-B AUX-	eDP1-B AUX+	GND
11	COM1-B TXD	GND	Reserved	Reserved	GND	Reserved	Reserved
12	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
13	COM2-B RXD	GND	Reserved	Reserved	GND	Reserved	Reserved
14	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
15	COM1-B RXD	GND	Reserved	Reserved	GND	Reserved	Reserved
16	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
CASE	GND						

* signal active when low

Table 25: VPX Connector P2 Wafer Assignment

P2 Signal Definition

MNEMONIC	SIGNAL DEFINITION
COM*x*-A / COM*x*-B	CPUA and CPUB RX/TX Serial Lines, EIA-232
USB3-A / USB3-B	USB Link 3 on CPUA / CPUB
SATA*x*-A	SATA Link *x* on CPUA
eDP1-A / eDP1-B	embedded Display Port on CPUA / CPUB
PCIe1-A CLK	Common Reference Clock Output for PCIe1-A
Reserved	Reserved, do not connect
GND	Ground

Table 26: VPX Connector P2 Signal Definition

4.3.4 P3 Connector

P3 Wafer Assignment

> **Manufacturing option:** Mezzanine I/O on P3 VPX Backplane: Pn4 PMC P64s single-ended I/O

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A	
1	5V	GND	Jn4-1	Jn4-3	GND	Jn4-2	Jn4-4	P64s
2	GND	Jn4-5	Jn4-7	GND	Jn4-6	Jn4-8	GND	
3	Reserved	GND	Jn4-9	Jn4-11	GND	Jn4-10	Jn4-12	
4	GND	Jn4-13	Jn4-15	GND	Jn4-14	Jn4-16	GND	
5	Reserved	GND	Jn4-17	Jn4-19	GND	Jn4-18	Jn4-20	
6	GND	Jn4-21	Jn4-23	GND	Jn4-22	Jn4-24	GND	
7	Reserved	GND	Jn4-25	Jn4-27	GND	Jn4-26	Jn4-28	
8	GND	Jn4-29	Jn4-31	GND	Jn4-30	Jn4-32	GND	
9	Reserved	GND	Jn4-33	Jn4-35	GND	Jn4-34	Jn4-36	
10	GND	Jn4-37	Jn4-39	GND	Jn4-38	Jn4-40	GND	
11	Reserved	GND	Jn4-41	Jn4-43	GND	Jn4-42	Jn4-44	
12	GND	Jn4-45	Jn4-47	GND	Jn4-46	Jn4-48	GND	
13	Reserved	GND	Jn4-49	Jn4-51	GND	Jn4-50	Jn4-52	
14	GND	Jn4-53	Jn4-55	GND	Jn4-54	Jn4-56	GND	
15	Reserved	GND	Jn4-57	Jn4-59	GND	Jn4-58	Jn4-60	
16	GND	Jn4-61	Jn4-63	GND	Jn4-62	Jn4-64	GND	
CASE	GND							

Table 27: P64s Mapping Pn4 PMC I/Os on P3 Connector

> **Signal Definition**

MNEMONIC	SIGNAL DEFINITION
Reserved	Reserved. Do not connect
5V	5V output, 1 A protection
Jn4-x	Connected to onboard PMC Jn4 connector pin x. Impedance: 50 Ohms single ended. 100 Ohms differential pairs formed by Jn4-x, Jn4-x+2 with x = 4*n+1 or x=4*n+2

> **Manufacturing option:** Mezzanine I/O on P3 VPX Backplane: Pn6 XMC X38s single-ended

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A	
1	5V	GND	Jn4-1	Jn4-3	GND	Jn4-2	Jn4-4	
2	GND	Jn4-5	Jn4-7	GND	Jn4-6	Jn4-8	GND	
3	Reserved	GND	Jn4-9	Jn4-11	GND	Jn6-C1	Jn6-F1	X38s
4	GND	Jn6-C2	Jn6-C3	GND	Jn6-F2	Jn6-F3	GND	
5	Reserved	GND	Jn6-C4	Jn6-C5	GND	Jn6-F4	Jn6-F5	
6	GND	Jn6-C6	Jn6-C7	GND	Jn6-F6	Jn6-F7	GND	
7	Reserved	GND	Jn6-C8	Jn6-C9	GND	Jn6-F8	Jn6-F9	
8	GND	Jn6-C10	Jn6-C11	GND	Jn6-F10	Jn6-F11	GND	
9	Reserved	GND	Jn6-C12	Jn6-C13	GND	Jn6-F12	Jn6-F13	
10	GND	Jn6-C14	Jn6-C15	GND	Jn6-F14	Jn6-F15	GND	
11	Reserved	GND	Jn6-C16	Jn6-C17	GND	Jn6-F16	Jn6-F17	
12	GND	Jn6-C18	Jn6-C19	GND	Jn6-F18	Jn6-F19	GND	
13	Reserved	GND	Jn4-49	Jn4-51	GND	Jn4-50	Jn4-52	
14	GND	Jn4-53	Jn4-55	GND	Jn4-54	Jn4-56	GND	
15	Reserved	GND	Jn4-57	Jn4-59	GND	Jn4-58	Jn4-60	
16	GND	Jn4-61	Jn4-63	GND	Jn4-62	Jn4-64	GND	
CASE	GND							

Table 28: X38s Mapping Pn6 XMC I/Os on P3 Connector

> **Signal Definition**

MNEMONIC	SIGNAL DEFINITION
Reserved	Reserved. Do not connect
5V	5V output, 1 A protection
Jn4-x	Connected to onboard PMC Jn4 connector pin x. Impedance: 50 Ohms single ended. 100 Ohms differential pairs formed by Jn4-x, Jn4-x+2 with x = 4*n+1 or x=4*n+2
Jn6-y	Connected to onboard XMC Jn6 connector pin y. Impedance: 50 Ohms single ended.

4.3.5 P4 Connector

P4 Wafer Assignment

> X12d+X8d Mapping for XMC I/Os on VPX P4 connector

> Legend for Table 29:

ETH-SW	Gigabit Ethernet port	ETH-SW*x* TX/RX	1000BASE-BX link *x*

Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A	
1	5V	GND	Jn6-A5	Jn6-B5	GND	Jn6-D5	Jn6-E5	X12d
2	GND	Jn6-A7	Jn6-B7	GND	Jn6-D7	Jn6-E7	GND	
3	Reserved	GND	Jn6-A9	Jn6-B9	GND	Jn6-D9	Jn6-E9	
4	GND	Jn6--A15	Jn6-B15	GND	Jn6-D15	Jn6-E15	GND	
5	Reserved	GND	Jn6--A17	Jn6-B17	GND	Jn6-D17	Jn6-E17	
6	GND	Jn6-A19	Jn6-B19	GND	Jn6-D19	Jn6-E19	GND	
7	Reserved	GND	Jn6-A1	Jn6-B1	GND	Jn6-D1	Jn6-E1	X8d
8	GND	Jn6-A3	Jn6-B3	GND	Jn6-D3	Jn6-E3	GND	
9	Reserved	GND	Jn6-A11	Jn6-B11	GND	Jn6-D11	Jn6-E11	
10	GND	Jn6-A13	Jn6-B13	GND	Jn6-D13	Jn6-E13	GND	
11	Reserved	GND	ETH-SW1 TX- (1)	ETH-SW1 TX+ (1)	GND	ETH-SW1 RX- (1)	ETH-SW1 RX+ (1)	
12	GND	ETH-SW0 TX- (1)	ETH-SW0 TX+ (1)	GND	ETH-SW0 RX- (1)	ETH-SW0 RX+ (1)	GND	
13	Reserved	GND	NC	NC	GND	NC	NC	
14	GND	NC	NC	GND	NC	NC	GND	
15	Reserved	GND	ETH-SW DB- (1)	ETH-SW DB+ (1)	GND	ETH-SW DA- (1)	ETH-SW DA+ (1)	
16	GND	ETH-SW DD- (1)	ETH-SW DD+ (1)	GND	ETH-SW DC- (1)	ETH-SW DC+ (1)	GND	
CASE	GND							

(1) Only present for ethernet on P4 order option, otherwise not connected.

Table 29: X12d+X8d Mapping Pn6 XMC I/Os on P4 Connector

P4 Signal Definition

MNEMONIC	SIGNAL DEFINITION
Reserved	Reserved. Do not connect
5V	5V output, 1 A protection
GND	Ground
Jn6-x	Connected to onboard XMC Jn6 connector pin x. Impedance: 100 Ohms differential pairs formed by 2 consecutive Jn6-x on the same row.
ETH-SW*x* RX+/-	1000BASE-BX Links x from onboard central ethernet switch. Receive +/- ETH-SW0 and ETH-SW1 only present for ethernet on P4 order option, otherwise not connected.
ETH-SW*x* TX+/-	1000BASE-BX Links x from onboard central ethernet switch. Transmit +/- ETH-SW0 and ETH-SW1 only present for ethernet on P4 order option, otherwise not connected.
ETH-SW - DA+/-	Ethernet 1000BASE-T: First pair of transmit/receive data. Only present for ethernet on P4 order option, otherwise not connected.
ETH-SW - DB+/-	Ethernet 1000BASE-T: Second pair of transmit/receive data. Only present for ethernet on P4 order option, otherwise not connected.
ETH-SW - DC+/-	Ethernet 1000BASE-T: Third pair of transmit/receive data. Only present for ethernet on P4 order option, otherwise not connected.
ETH-SW - DD+/-	Ethernet 1000BASE-T: Thourth pair of transmit/receive data Only present for ethernet on P4 order option, otherwise not connected.

4.3.6 P5 and P6 Connectors

P5 and P6 connectors are unused on the VX6060 and are not equipped.

4.3.7 XDP

Standard XDP debug connector for CPUA and CPUB can be made available through a dedicated adapter board.

4.4 PMC Connectors

- PMC Slot: 4-lane PCI Express from CPUA on PCIe/PCI-X bridge to PMC PCI connectors.
- PCI-X 64 bits 100 MHz 3.3V signalling only.
- All 64 I/Os routed to P3 with controlled impedance and controlled length pairs.
- Compliance to: IEEE P1386-2001 and IEEE P1386-2001.1.

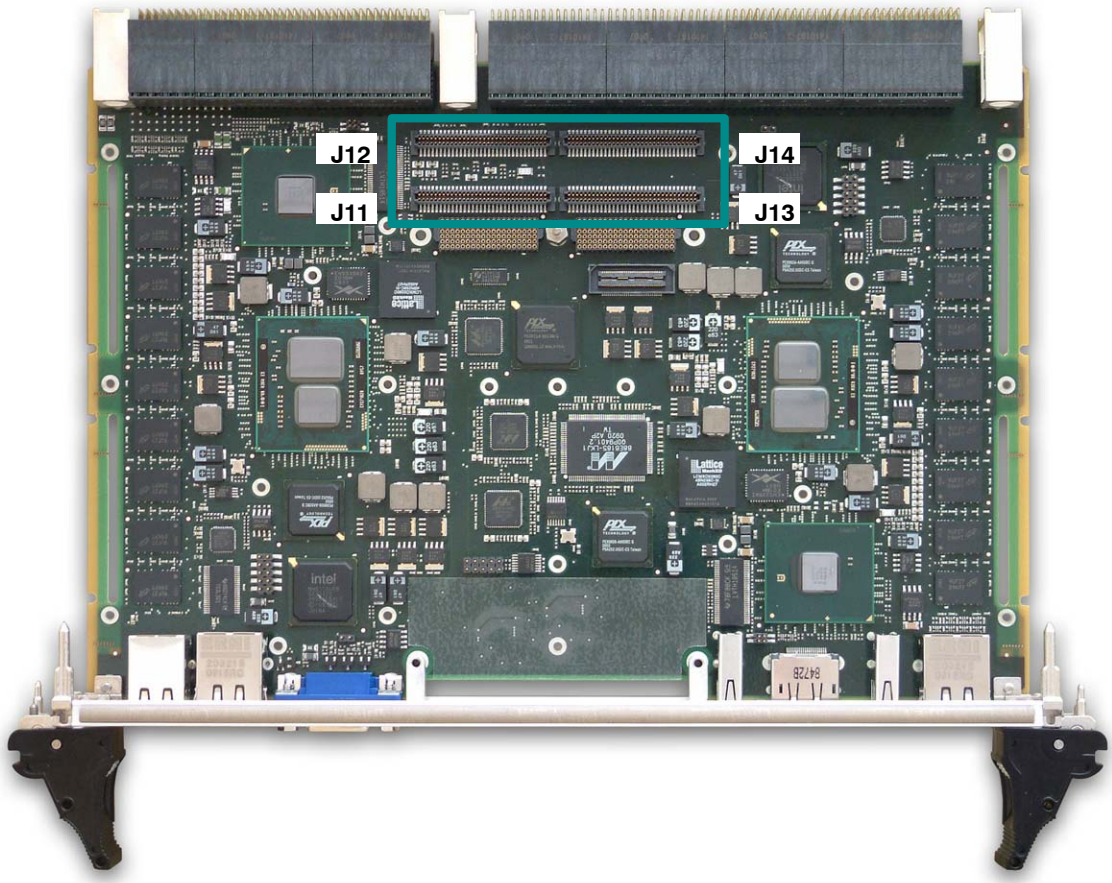


Figure 32: Location of the PMC Connectors

4.4.1 PMC J11 Connector Pin Assignment

Pin	Signal	Signal	Pin
1	TCK	–12V	2
3	GND	INTA#	4
5	INTB#	INTC#	6
7	BUSMODE1#	+5V	8
9	INTD#	N.C.	10
11	GND	+3.3V_SUS	12
13	CLK	GND	14
15	GND	GNT#	16
17	REQ#	+5V	18
19	V(I/O) (1)	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	GND	24
25	GND	C/BE3#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	V(I/O) (1)	AD[17]	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	DEVSEL#	+5V	38
39	PCIXCAP	LOCK#	40
41	SDONE	SBO#	42
43	PAR	GND	44
45	V(I/O) (1)	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	GND	C/BE0#	52
53	AD[06]	AD[05]	54
55	AD[04]	GND	56
57	V(I/O) (1)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	GND	REQ64#	64

(1) V(I/O) is 3.3V only.

PCI signals active when low.

Table 30: PMC J11 Connector Pin Assignment

4.4.2 PMC J12 Connector Pin Assignment

Pin	Signal	Signal	Pin
1	+12V	TRST#	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	N.C.	8
9	N.C.	N.C.	10
11	BUSMODE2#	+3.3V	12
13	RST#	BUSMODE3#	14
15	+3.3V	BUSMODE4#	16
17	PME#	GND	18
19	AD[30]	AD[29]	20
21	GND	AD[26]	22
23	AD[24]	+3.3V	24
25	IDSEL1	AD[23]	26
27	+3.3V	AD[20]	28
29	AD[18]	GND	30
31	AD[16]	C/BE2#	32
33	GND	IDSEL B (1)	34
35	TRDY#	+3.3V	36
37	GND	STOP#	38
39	PERR#	GND	40
41	+3.3V	SERR#	42
43	C/BE1#	GND	44
45	AD[14]	AD[13]	46
47	M66EN	AD[10]	48
49	AD[08]	+3.3V	50
51	AD[07]	REQ B# (1)	52
53	+3.3V	GNT B# (1)	54
55	PMC−RSVD	GND	56
57	PMC−RSVD	EREADY	58
59	GND	N.C.	60
61	ACK64#	+3.3V	62
63	GND	N.C.	64

(1) IDSEL B, REQB# and GNTB# are provided for use by dual-function PMC modules or processor-PMC modules

PCI signals active when low.

Table 31: PMC J12 Connector Pin Assignment

4.4.3 PMC J13 Connector Pin Assignment

Pin	Signal	Signal	Pin
1	N.C.	GND	2
3	GND	C/BE7#	4
5	C/BE6#	C/BE5#	6
7	C/BE4#	GND	8
9	V(I/O) (1)	PAR64	10
11	AD[63]	AD[62]	12
13	AD[61]	GND	14
15	GND	AD[60]	16
17	AD[59]	AD[58]	18
19	AD[57]	GND	20
21	V(I/O) (1)	AD[56]	22
23	AD[55]	AD[54]	24
25	AD[53]	GND	26
27	GND	AD[52]	28
29	AD[51]	AD[50]	30
31	AD[49]	GND	32
33	GND	AD[48]	34
35	AD[47]	AD[46]	36
37	AD[45]	GND	38
39	V(I/O) (1)	AD[44]	40
41	AD[43]	AD[42]	42
43	AD[41]	GND	44
45	GND	AD[40]	46
47	AD[39]	AD[38]	48
49	AD[37]	GND	50
51	GND	AD[36]	52
53	AD[35]	AD[34]	54
55	AD[33]	GND	56
57	V(I/O) (1)	AD[32]	58
59	RSVD	RSVD	60
61	RSVD	GND	62
63	GND	RSVD	64

(1) V(I/O) is 3.3V only.

PCI signals active when low.

Table 32: PMC J13 Connector Pin Assignment

4.4.4 PMC J14 Connector Pin Assignment

Pin	Signal	Signal	Pin
1	PMC IO 01	PMC IO 02	2
3	PMC IO 03	PMC IO 04	4
5	PMC IO 05	PMC IO 06	6
7	PMC IO 07	PMC IO 08	8
9	PMC IO 09	PMC IO 10	10
11	PMC IO 11	PMC IO 12	12
13	PMC IO 13	PMC IO 14	14
15	PMC IO 15	PMC IO 16	16
17	PMC IO 17	PMC IO 18	18
19	PMC IO 19	PMC IO 20	20
21	PMC IO 21	PMC IO 22	22
23	PMC IO 23	PMC IO 24	24
25	PMC IO 25	PMC IO 26	26
27	PMC IO 27	PMC IO 28	28
29	PMC IO 29	PMC IO 30	30
31	PMC IO 31	PMC IO 32	32
33	PMC IO 33	PMC IO 34	34
35	PMC IO 35	PMC IO 36	36
37	PMC IO 37	PMC IO 38	38
39	PMC IO 39	PMC IO 40	40
41	PMC IO 41	PMC IO 42	42
43	PMC IO 43	PMC IO 44	44
45	PMC IO 45	PMC IO 46	46
47	PMC IO 47	PMC IO 48	48
49	PMC IO 49	PMC IO 50	50
51	PMC IO 51	PMC IO 52	52
53	PMC IO 53	PMC IO 54	54
55	PMC IO 55	PMC IO 56	56
57	PMC IO 57	PMC IO 58	58
59	PMC IO 59	PMC IO 60	60
61	PMC IO 61	PMC IO 62	62
63	PMC IO 63	PMC IO 64	64

Table 33: PMC J14 Connector Pin Assignment

Refer to Table 27 page 64 and Table 28 page 65 for J14 pin assignment on VPX P3 connector.

4.4.5 PMC Signal Description

MNEMONIC	SIGNAL DESCRIPTION
AD[00] to AD[31]	Address/Data bits. Multiplexed address and data bus.
ACK64#	Acknowledge 64-bit Transfer. Driven low by the device to indicate that the target is willing to transfer data using 64 bits.
BUSMODE1#	Bus Mode 1. Driven low by a PMC module to indicate that it supports the current bus mode
C/BE0# to C/BE1#	Command/Byte Enables. During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase the signals are byte enables that specify the active bytes on the bus.
CLK	Clock. The 64-bit PCI bus signals are synchronous to 33 or 66 MHz clock.
DEVSEL#	Device Select. Driven low by a PCI agent to signal that it has decoded its address as the target of the current access.
FRAME#	FRAME. Driven low by the current master to signal the start and duration of an access.
EREADY	EREADY. Output of non-monarch PPMCs that indicates it has completed its onboard initialization and can respond to PCI bus enumeration by the monarch via configuration cycles. Input to the monarch PPMC that indicates all non-monarch PPMCs have completed their onboard initialization and can respond to PCI bus enumeration by the monarch via configuration cycles.
GNT#	Grant. Driven low by the arbiter to grant PCI bus ownership to a PCI agent. GNT B# is provided for use by dual-function PMC modules or processor-PMC modules.
IDSEL	Initialization Device Select. Device chip select during configuration cycles. IDSEL B is provided for use by dual-function PMC modules or processor-PMC modules.
INTA# to INTD#	Interrupt lines. Level-sensitive, active-low interrupt requests.
IRDY#	Initiator Ready. Driven low by the initiator to signal its ability to complete the current data phase.
LOCK#	LOCK. Driven low to indicate an atomic operation that may require multiple transactions to complete.
M66EN	66 MHZ Enable. Indicates to a device if the bus segment is operating at 66 or 33 MHz. If it is high then the bus speed is 66 MHz and if it is low then the bus speed is 33 MHz.
N.C.	This pin is not connected.
PAR	Parity. Parity protection bit for AD0 to AD31 and C/BE0# to C/BE3#.
PERR#	Parity Error. Driven low by a PCI agent to signal a parity error.
PMC IO 01 to PMC IO 64	64-bit PCI bus PMC 64 signals. Used to transmit I/O signals from PCI 64 PMC connector (J14) to VPX P3 connector.
PMC-RSVD	Reserved. Do not connect this pin.
REQ#	Request. Driven low by a PCI agent to request ownership of the PCI bus. REQ B# is provided for use by dual-function PMC modules or processor-PMC modules.
REQ64#	Request 64-bit Transfer. Driven low by the current bus master, indicates that it desires to transfer data using 64 bits.
RST#	Reset. Driven low to reset the PCI bus.
SBO#	Snoop Backoff. Indicates a hit of a modified line asserted. Not used.
SDONE#	Snoop Done. Indicates the status of the snoop for the current access. Nor used.
SERR#	System Error. Driven low by a PCI agent to signal a system error.
STOP#	STOP. Driven low by a PCI target to signal a disconnect or target-abort.
TRDY#	Target Ready. Driven low by the current target to signal its ability to complete the current data phase.
V(I/O)	Power supply delivered by the board. On the PCI 64 PMC slots, +3.3 Volts power is supplied. +5 Volts signaling PMCs are not supported.

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MNEMONIC	SIGNAL DESCRIPTION
+3.3V	+3.3 Volts DC power derived from VPX +5V power
+5V	+5 Volts DC power
+12V	+12 Volts DC power
-12V	-12 Volts DC power from VPX -12V_AUX
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Table 34: PMC Signal Description

4.5 XMC Connectors

One XMC site is provided to allow the installation of VITA 42.3, PCI-Express mezzanine cards.

- XMC Slot (same mechanical slot than PMC slot) : 8-lane PCI Express XMC from CPUA.
- Supports x8 PCI Express XMC slot with 10W power budget and Rear I/O to P3/P4 as per VITA 46.9.
- The signal assignments are as shown in the following tables.

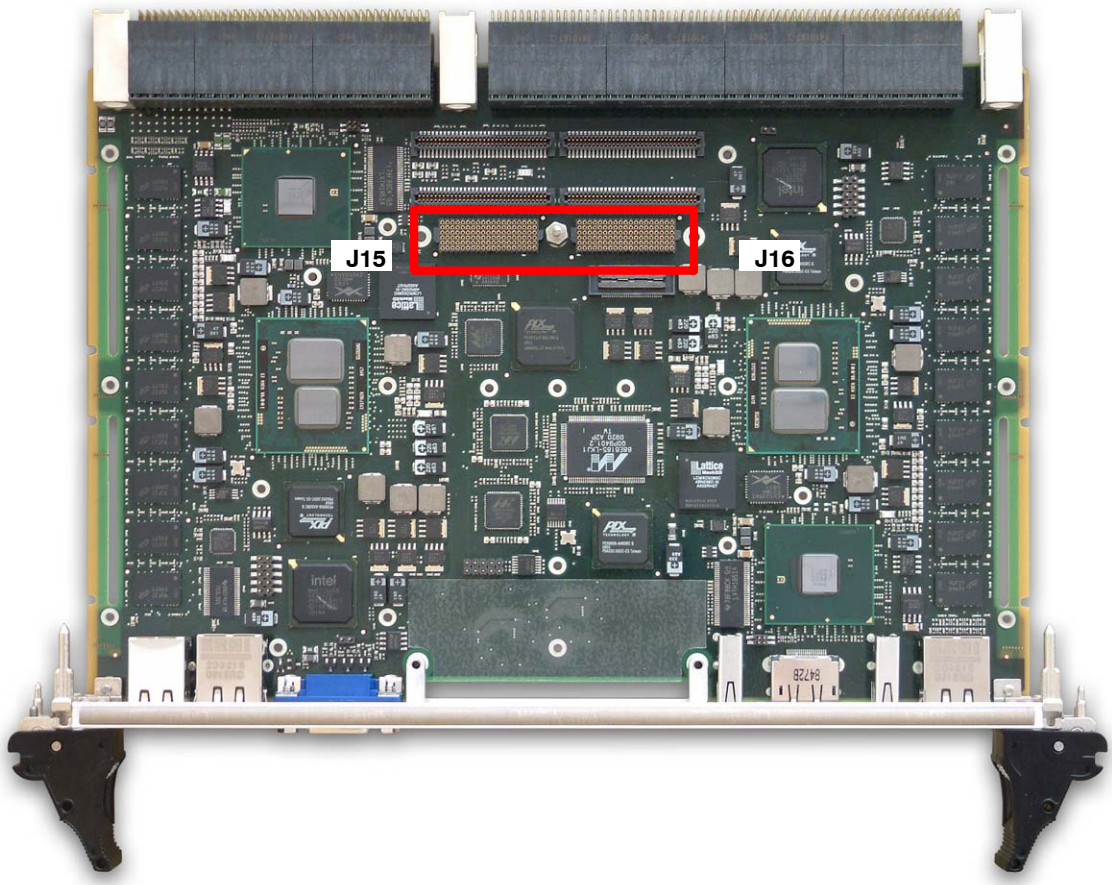


Figure 33: Location of the XMC Connectors

4.5.1 XMC J15 Connector Pin Assignment

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR (1)
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR (1)
4	GND	GND	TCK	GND	GND	MRSTO#
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR (1)
6	GND	GND	TMS	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR (1)
8	GND	GND	TDI	GND	GND	–12V
9	RFU	RFU	N.C.	RFU	RFU	VPWR (1)
10	GND	GND	TDO	GND	GND	GA0
11	PER0p0	PER0n0	N.C.	PER0p1	PER0n1	VPWR (1)
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PER0p2	PER0n2	3.3V AUX	PER0p3	PER0n3	VPWR (1)
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	N.C.	PER0p5	PER0n5	VPWR (1)
16	GND	GND	NVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	N.C.	PER0p7	PER0n7	N.C.
18	GND	GND	N.C.	GND	GND	N.C.
19	REFCLK+0	REFCLK–0	N.C.	WAKE#	N.C.	N.C.

(1) VPWR is set at the factory to +5V.

Signals active when low.

Table 35: XMC J15 Connector Pin Assignment

4.5.2 XMC Signal Decription

MNEMONIC	LEGEND	SIGNAL DESCRIPTION
GA[2..0]		I2C channel select. These signals allow to address the XMC slot . Set to 100.
GND		Ground
MPRESENT#		Module present. Not used, pulled up.
MRSTI#		XMC Reset In. When this signal is asserted low, the mezzanine card shall initialize itself into a known state.
MRSTO#		XMC Reset Out. Not used.
MSCL		IPMI I2C serial clock. Connected to PCH A I2C.
MSDA		IPMI I2C serial data. Connected to PCH A I2C.
NVMRO		XMC Write Prohibit. When this signal is asserted high, the XMC shall disable writes to non-volatile memory on the XMC.
N.C.		Not Connected.
PET0p/n[0..7]		Link 0 Differential Transmit. These signals are used by the XMC to transmit high-speed protocol-specific data TO the CPUA over the PCI Express interface at gen1 speed.
PER0p/n[0..7]		Link 0 Differential Receive. These signals are used by the XMC to receive high-speed protocol-specific data FROM the CPUA over the PCI Express interface at gen1 speed.
REFCLK+/-0		Differential reference clock for Link 0 PCI Express interface.
RFU		Reserved for Future Use
TCK		JTAG Clock.
TDI		JTAG Data In
TDO		JTAG Data Out
TMS		JTAG Mode Select
TRST#		JTAG Reset.
VPWR		Power pins. These signals carry either +12V or +5V power from the carrier to the XMC. Set at factory to +5V.
3.3V		+3.3 Volts DC power derived from VPX +5V power
3.3V AUX		3.3V auxiliairy power present when VPX 5V or VPX 3.3V_AUX power are present
+/-12V		-12V is connected to VPX -12V_AUX power.

Table 36: XMC Signal Description

4.5.3 XMC J16 Connector Pin Assignment

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	XMCIO X8d+ 01	XMCIO X8d– 01	XMCIO X38s 37	XMCIO X8d+ 02	XMCIO X8d– 02	XMCIO X38s 38
2	GND	GND	XMCIO X38s 35	GND	GND	XMCIO X38s 36
3	XMCIO X8d+ 03	XMCIO X8d– 03	XMCIO X38s 33	XMCIO X8d+ 04	XMCIO X8d– 04	XMCIO X38s 34
4	GND	GND	XMCIO X38s 31	GND	GND	XMCIO X38s 32
5	XMCIO X12d+ 01	XMCIO X12d– 01	XMCIO X38s 29	XMCIO X12d+ 02	XMCIO X12d– 02	XMCIO X38s 30
6	GND	GND	XMCIO X38s 27	GND	GND	XMCIO X38s 28
7	XMCIO X12d+ 03	XMCIO X12d– 03	XMCIO X38s 25	XMCIO X12d+ 04	XMCIO X12d– 04	XMCIO X38s 26
8	GND	GND	XMCIO X38s 23	GND	GND	XMCIO X38s 24
9	XMCIO X12d+ 05	XMCIO X12d– 05	XMCIO X38s 21	XMCIO X12d+ 06	XMCIO X12d– 06	XMCIO X38s 22
10	GND	GND	XMCIO X38s 19	GND	GND	XMCIO X38s 20
11	XMCIO X8d+ 05	XMCIO X8d– 05	XMCIO X38s 17	XMCIO X8d+ 06	XMCIO X8d– 06	XMCIO X38s 18
12	GND	GND	XMCIO X38s 15	GND	GND	XMCIO X38s 16
13	XMCIO X8d+ 07	XMCIO X8d– 07	XMCIO X38s 13	XMCIO X8d+ 08	XMCIO X8d– 08	XMCIO X38s 14
14	GND	GND	XMCIO X38s 11	GND	GND	XMCIO X38s 12
15	XMCIO X12d+ 07	XMCIO X12d– 07	XMCIO X38s 09	XMCIO X12d+ 08	XMCIO X12d– 08	XMCIO X38s 10
16	GND	GND	XMCIO X38s 07	GND	GND	XMCIO X38s 08
17	XMCIO X12d+ 09	XMCIO X12d– 09	XMCIO X38s 05	XMCIO X12d+ 10	XMCIO X12d– 10	XMCIO X38s 06
18	GND	GND	XMCIO X38s 03	GND	GND	XMCIO X38s 04
19	XMCIO X12d+ 11	XMCIO X12d– 11	XMCIO X38s 01	XMCIO X12d+ 12	XMCIO X12d– 12	XMCIO X38s 02

Table 37: XMC J16 Connector Pin Assignment

Refer to Table 28 page 65 and Table 29 page 66 for the mapping of XMC J16 connector on VPX P3 and P4 connectors.

4.6 LEDs

Status LEDs Default Setting

There are six bicolor LEDs (Red/Green) on the front panel of the VX6060 6U VPX board, three dedicated to CPUA and three dedicated to CPUB.

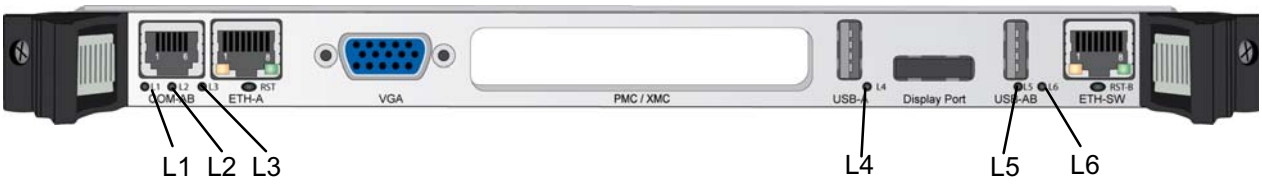


Figure 34: LEDs Front panel

CPUA LED	COLOR	DESCRIPTION
L1	RED	Permanent error on CPUA subsystem
	GREEN	Internal power OK for CPUA subsystem
	ORANGE	Reset state on CPUA subsystem
	OFF	Blinking during CPLDA LPC activity
L2 (1)	RED	CPLDA watchdog reset timer has expired
	GREEN	Normal operation mode
	ORANGE	Factory test mode
	OFF	Blinking during SATA activity in CPUA subsystem
L3 (1)	RED	Processor hot, may trigger processor performance limitations on CPUA
	GREEN	Ethernet ETH-A connector valid on front panel
	ORANGE	Ethernet ETH-A link directed to central onboard ethernet switch
	OFF	Blinking during ETH-A link activity in CPUA subsystem

(1) The color of these LEDs may also be fixed by software through CPLD registers

Table 38: CPUA LEDs Description

CPUB LED	COLOR	DESCRIPTION
L4	RED	Permanent error on CPUB subsystem
	GREEN	Internal power OK for CPUB subsystem
	ORANGE	Reset state on CPUB subsystem
	OFF	Blinking during CPLDB LPC activity
L5 (1)	RED	CPLDB watchdog reset timer has expired
	GREEN	USB-AB front connector selection: USB attached to CPUB subsystem
	ORANGE	USB-AB front connector selection: USB attached to CPUA subsystem
	OFF	Blinking during SATA activity in CPUB subsystem
L6 (1)	RED	Processor hot, may trigger processor performance limitations on CPUB
	GREEN	Ethernet ETH-SW connector valid on front panel
	ORANGE	Ethernet ETH-SW link directed to VPX rear connector
	OFF	Blinking during ETH-SW link activity

(1) The color of these LEDs may also be fixed by software through CPLD registers

Table 39: CPUB LEDs Description

Chapter 5 - Power and Thermal Specifications

5.1 Power Specifications

Board Load	Power Consumption VX6060-SA24-00000	Current Drawn (1)
Typical	85W	5A 12V 5A 5V
Maximum	100W	5.8A 12V 6.1A 5V

Table 40: VX6060 Power Consumption

(1) Does not include current eventually supplied to PMC/XMC or external periphals like USB.

PMC/XMC Power

Maximum cumulative currents supplied to PMC/XMC mezzanine connectors: 3A 5V, 4A 3.3V. For XMC, VPOWER is set to 5V as the standard configuration (VPOWER can be reconfigured to 2A 12V instead of 5V at the factory).

For standard thermal operating environnements defined in this manual, the VX6060 is qualified for a maximum of 10W thermal power dissipation of the PMC/XMC.

5.2 Board Thermal Monitoring

To ensure optimal and long-term reliability of the VX6060, all onboard components must remain within the maximum temperature specifications. The most critical components on the VX6060are the processor and the memory. Operating the VX6060 above the maximum operating limits will result in permanent damage to the board.

The VX6060 includes three temperature sensors, located on the I^2C bus, and managed by the CPLDs. Refer to Figure 23 “I2C Diagram” page 44.

Key Features of the Temperature Sensors

- Local temperature accuracy: +/- 2°C.
- Operating temperature: -40 °C / +150°C.

Location of the Temperature Sensors

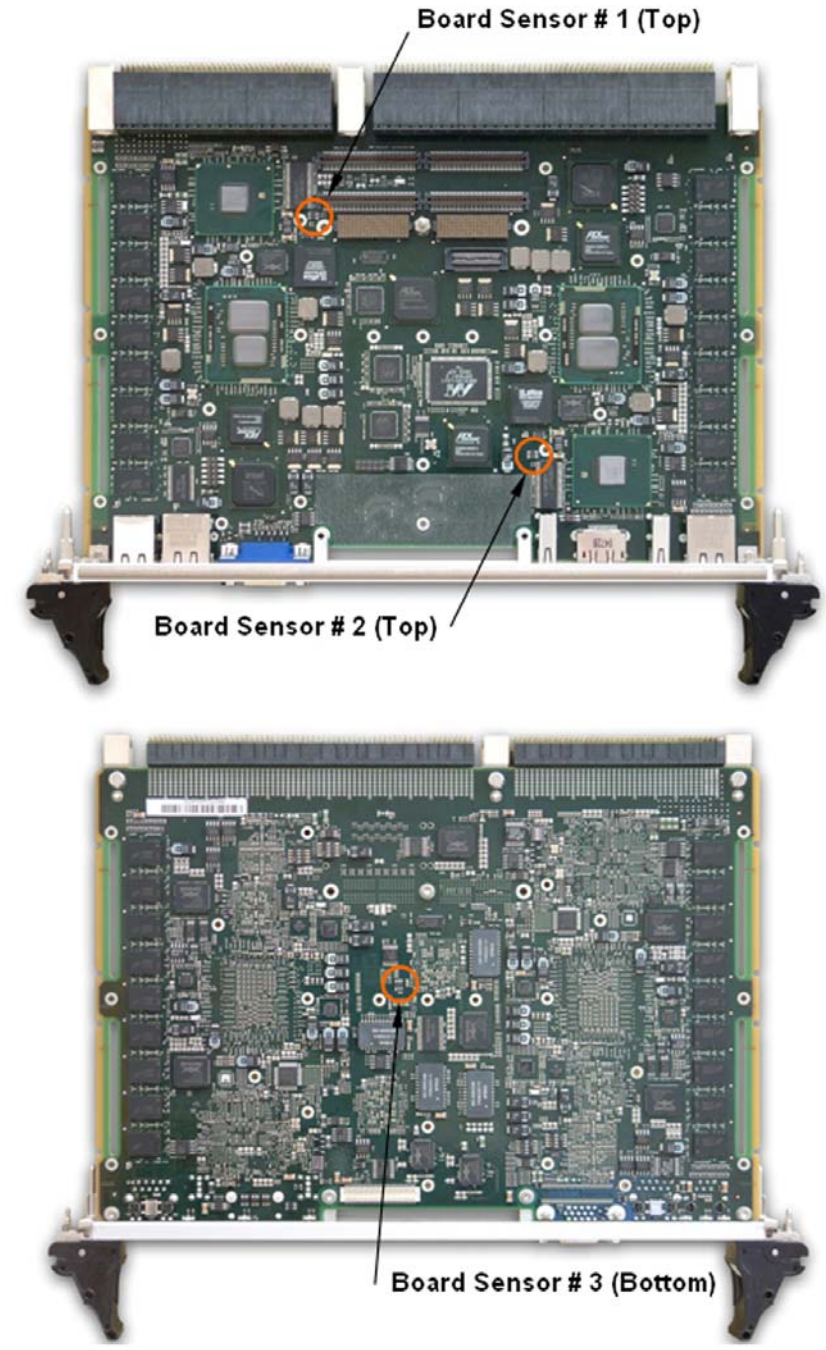


Figure 35: Board Temperature Sensors Location

5.3 CPU Thermal Monitoring

CPU Temperature

For a given minimum required air-flow, following curves (Figure 36 page 84) show the maximum **authorized** operating temperature, not to exceed the maximum specified junction temperature of the processor.

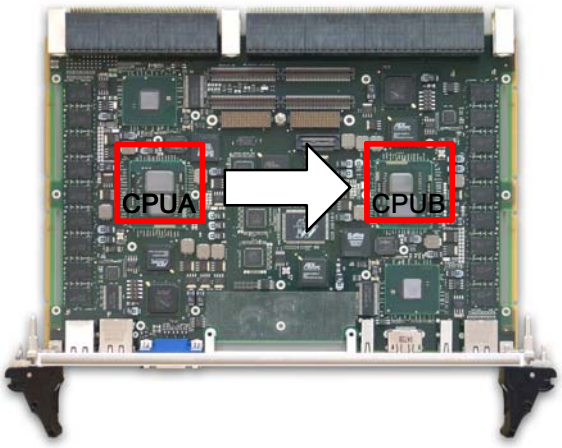
T_{JMAX} CPU cores: 105°C

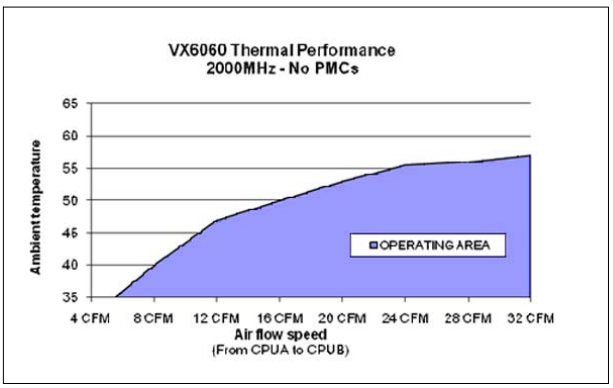
T_{JMAX} GFX cores: 100°C

The T_{JMAX} temperature is the temperature not to exceed, to avoid entering the throttling mode.

For instance, for:

- VX6060-SA board (Order Code: VX6060-SA2X-00000), maximum operating CPUA and CPUB cores frequencies (2 GHz), without PMC on board: at +55°C ambient temperature, the minimum air flow (from CPUA to CPUB) needed to cool enough the processor die is about **24 CFM** (either **3.1 m/s)** in a 1 inch slot.
- VX6060-SA board (Order Code: VX6060-SA2X-00000), maximum operating CPUA and CPUB cores frequencies (2 GHz), with PMC on board: at +55°C ambient temperature, the minimum air flow (from CPUA to CPUB) needed to cool enough the processor die is about **28 CFM** (either **3.6 m/s)** in a 1 inch slot.





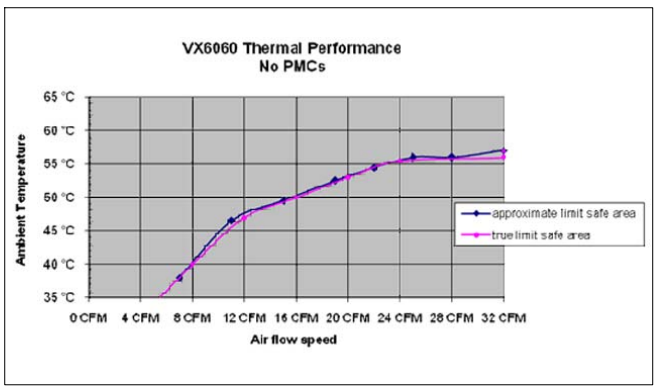
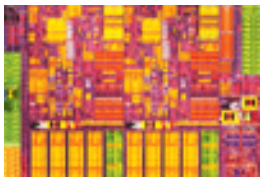


Figure 36: VX6060 Thermal Performance

The CPU temperature is also accessible through the Linux sensors driver. Refer to the Release Notes for BSP Fedora 12 (SD.DT.F72), section “BSP Specific Features - Sensors” for more information on this topic.

Intel® Turbo Boost Technology



Intel® Turbo Boost Technology is one of the many exciting features that Intel has built into latest-generation Intel® microarchitecture. It automatically allows processor cores to run faster than the base operating frequency if it's operating below power, current, and temperature specification limits.

Dynamically increasing performance

Intel Turbo Boost Technology is activated when the Operating System (OS) requests the highest processor performance state (P0).

The maximum frequency of Intel Turbo Boost Technology is dependent on the number of active cores. The amount of time the processor spends in the Intel Turbo Boost Technology state depends on the workload and operating environment.

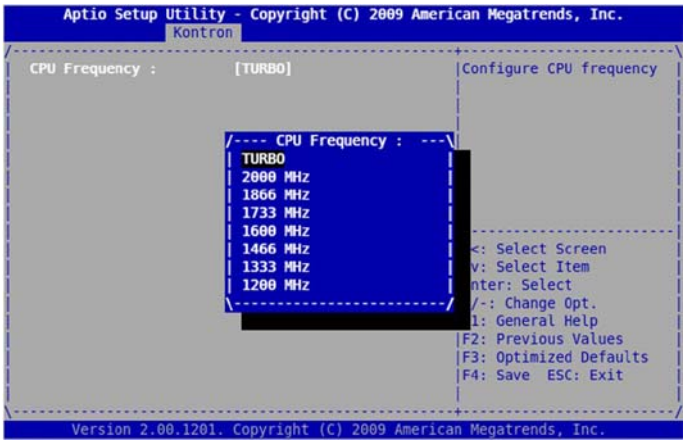
Any of the following can set the upper limit of Intel Turbo Boost Technology on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency will dynamically increase by 133 MHz on short and regular intervals until the upper limit is met or the maximum possible upside for the number of active cores is reached.

Learn more about Intel Turbo Boost Technology: http://www.intel.com/technology/turboboost/

> The Intel Turbo Boost is handled by the BIOS through the CPU configuration menu.



Refer to the AMI BIOS for VX6060 - User Reference Manual (SD.DT.F69), section “CPU Configuration”.

Chapter 6 - Backplane Suggestions

Kontron can offer for development or deployement of the VX6060 the following backplane models:

Single Star x4

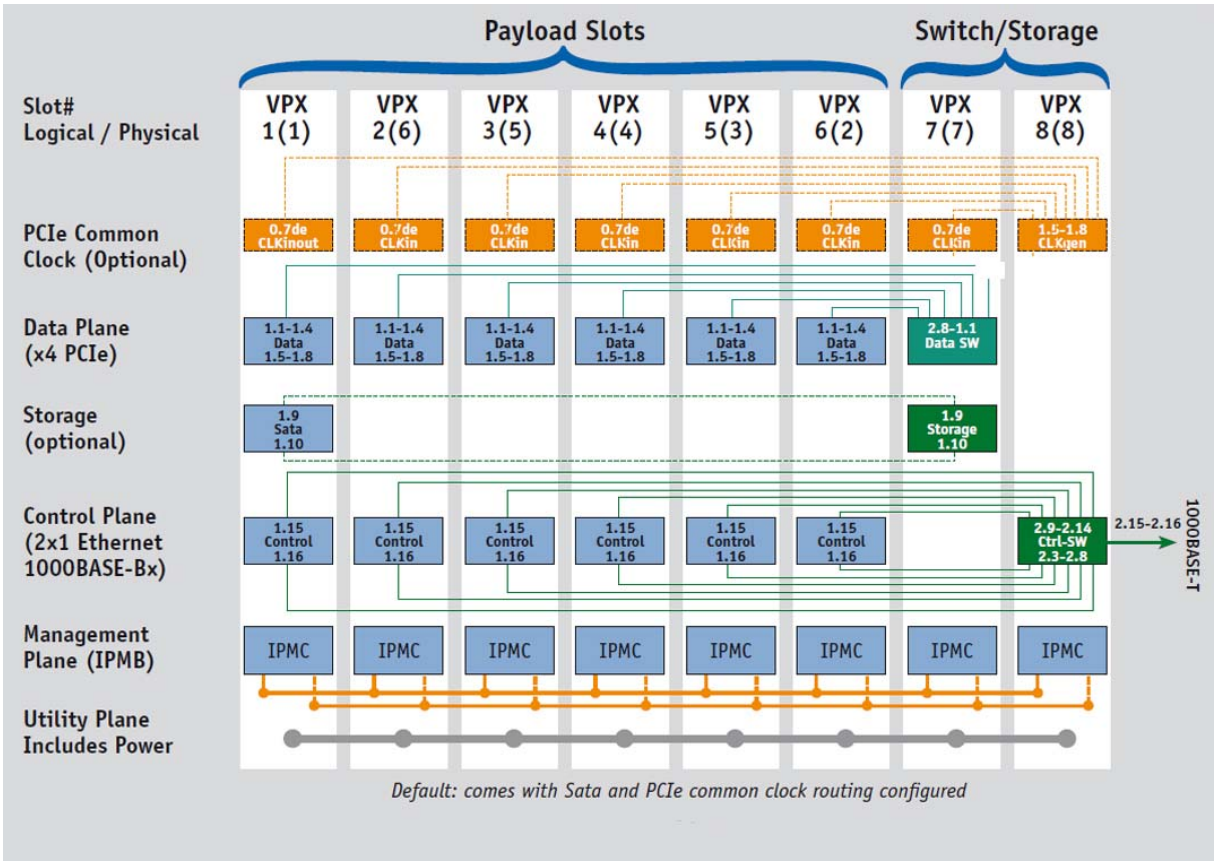


Figure 37: Single Star x4 Topology

Dual Star x4

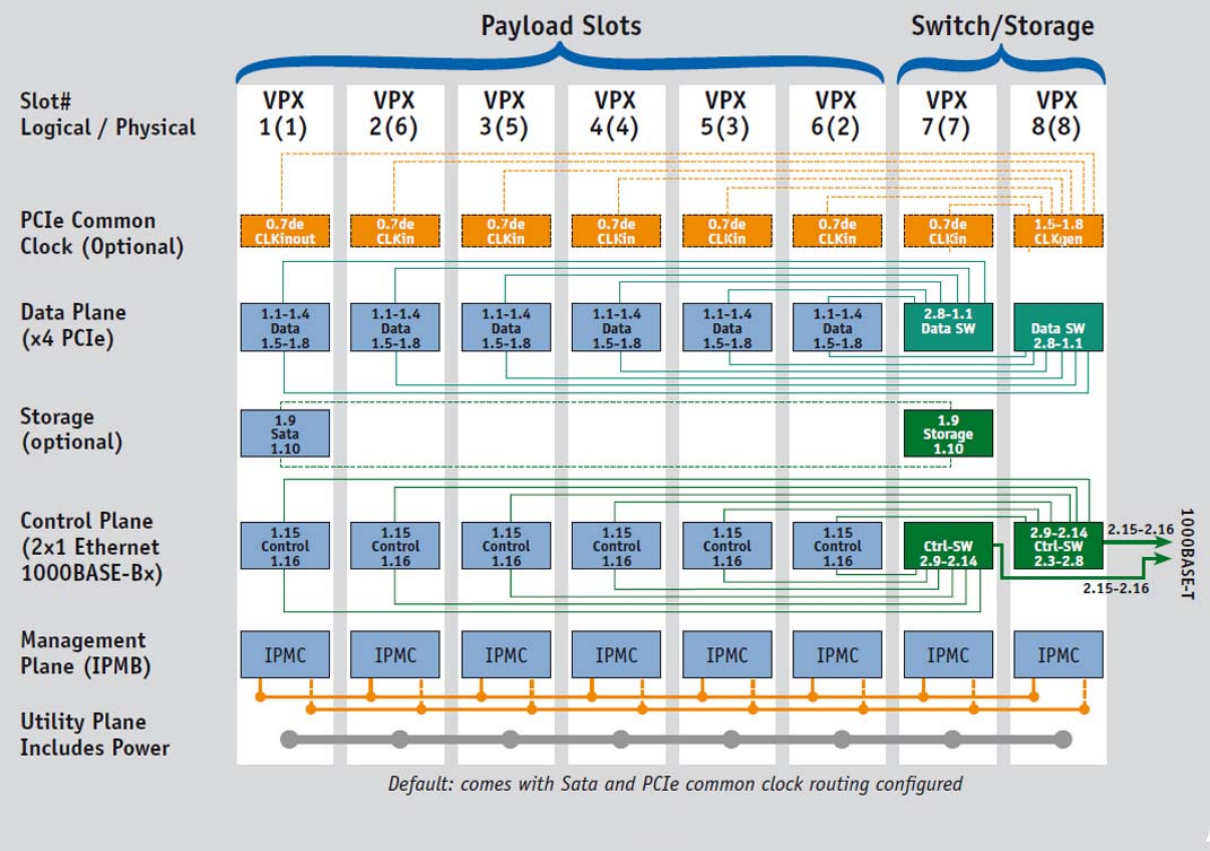


Figure 38: Dual Star x4 Topology

Single Star x2

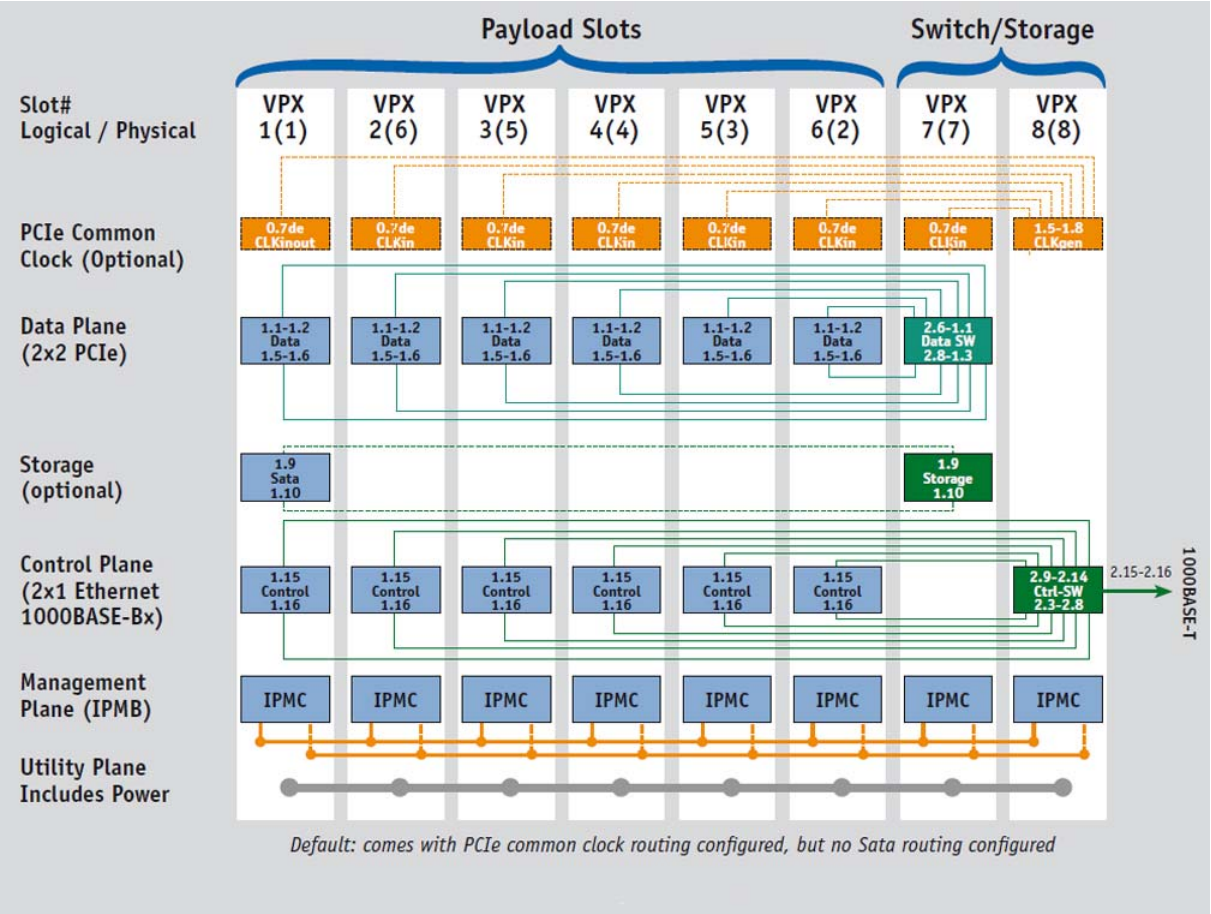


Figure 39: Single Star x2 Topology

Chapter 7 - VX6060-RTM Characteristics

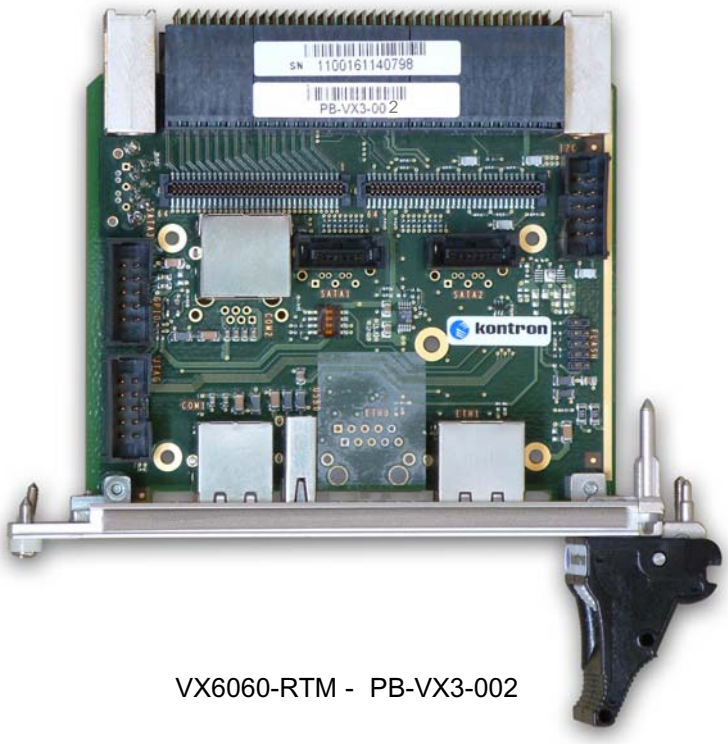
7.1 Overview

The VX6060 provides optional Rear I/O connectivity for peripherals, a feature which may be particularly useful in specialized CompactPCI systems. Some standard PC interfaces are implemented and assigned to the front panel and to the Rear I/O connector J2 on the VX6060.

When the VX6060-RTM is used, the signals of some of the main board/front panel connectors are routed to the module interface. Thus, the VX6060 Rear Transition Module makes it much easier to remove the CPU in the rack as there is practically no cabling on the CPU board.

The VX6060-RTM provides the following functions:

- VPX Rear I/O
- Two USB 2.0 ports
- One Gigabit Ethernet ports without LED signals
- Two COM (Serial) ports
- Two SATA ports
- Two GPIOs
- One Reset Button
- One I2C Bus connector
- One JTAG connector



VX6060-RTM - PB-VX3-002

Figure 40: VX6060-RTM Overview

7.2 Technical Specifications

VX6060-RTM		SPECIFICATIONS
Front Panel Interfaces	USB	One USB 2.0 interface: 4-pin connector
	Ethernet	One Gigabit Ethernet interfaces implemented as dual RJ-45 connector without LEDs
	COM	One serial port (COM1), RS-232 simplified, RJ-11 connector
	Reset	One Push Button
Onboard Interfaces	SATA	Two SATA interfaces; SATA1 and SATA2
	VPX	VPX connector for connecting Rear I/O to the backplane
	COM	One serial port (COM2) implemented as a RJ-11 onboard connector, RS-232 simplified
	GPIOs	Two General Purpose I/Os
	USB	One USB interface used to connect a Flash disk
	I2C Bus	
	JTAG	
General	Temperature Range	Operational: 0°C to +55°C Storage: -55°C to +85°C
	Climatic Humidity	99% non-condensing
	Dimensions	Dimensions: 99.85 mm x 82.54 mm
	Board Weight	120g

Table 41: VX6060-RTM Main Specifications

7.3 RTM Configuration

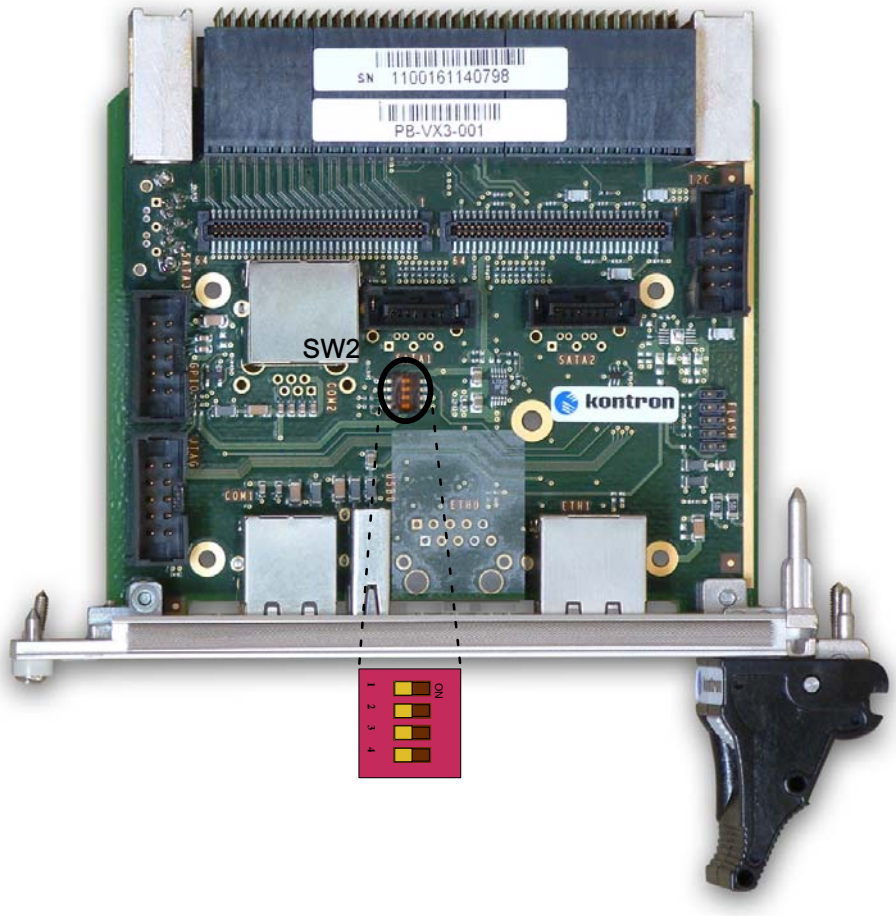


Figure 41: VX6060-RTM MicroSwitch Location

MicroSwitch SW2	Function	Description
1	NVMRO Non-Volatile Memory Read Only	ON (0) Set NVMRO VPX signal to Ground OFF (1) No action on NVMRO VPX signal **Default setting**
2	Reserved	Reserved
3	COM1 Differential Termination	ON (0) Connect a 100 Ohms parallel termination between RXD+ and RXD- OFF (1) No differential termination/mode **Default setting**
4	COM2 Differential Termination	ON (0) Connect a 100 Ohms parallel termination between RXD+ and RXD- OFF (1) No differential termination/ mode **Default setting**

7.4 Connectors

7.4.1 RTM Connectors Identification

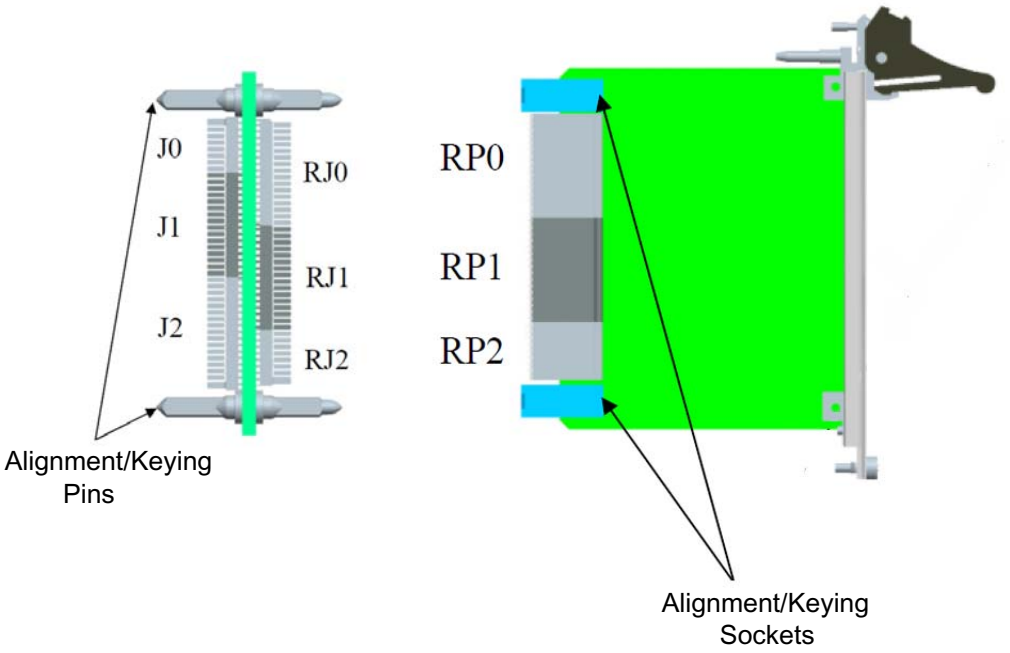


Figure 42: Connector Identification for 3U RTM

7.4.2 Front Panel Connectors

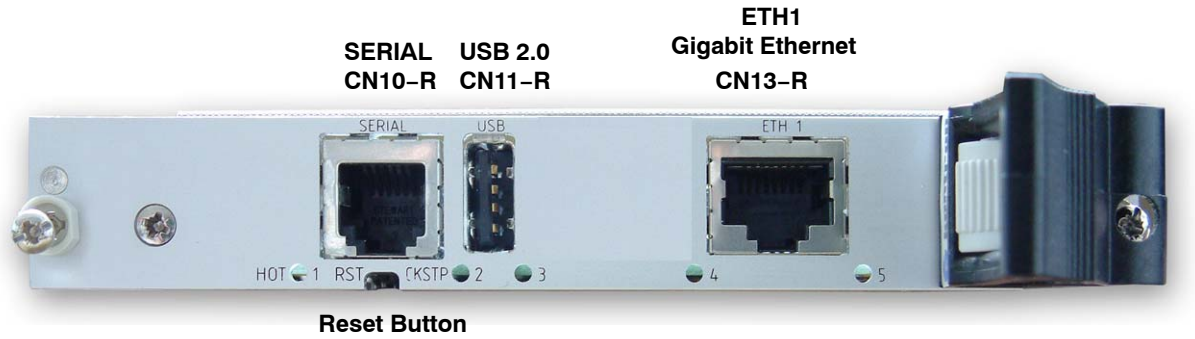


Figure 43: VX6060-RTM Front Panel Connectors

LED 1 to LED 5 are not connected.

7.4.3 Onboard Connectors

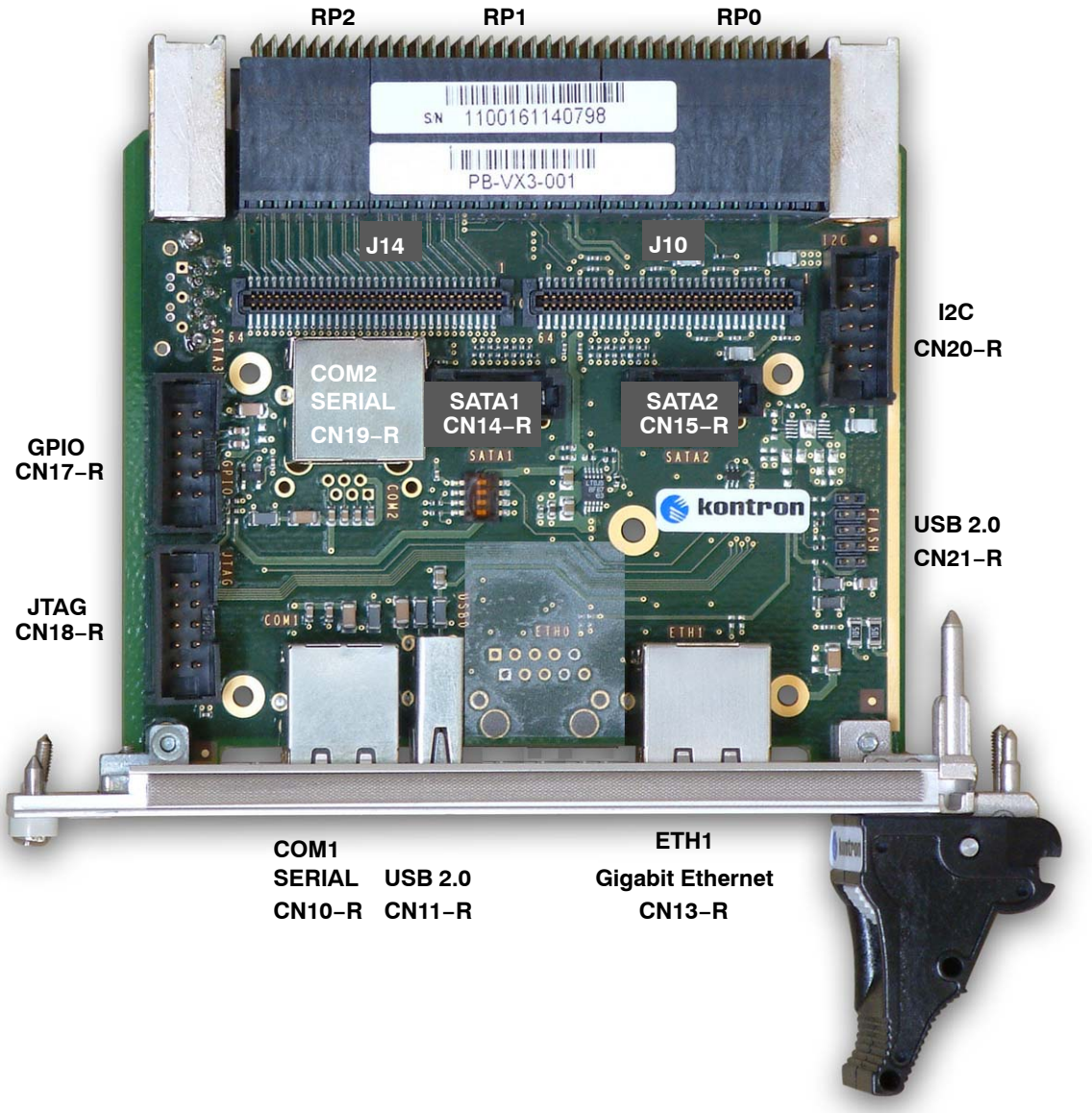


Figure 44: VX6060-RTM Onboard Connectors

7.5 Modules Interfaces

7.5.1 COM Interfaces

The VX6060-RTM provides two COM (COM1-A and COM1-B) ports for connecting devices to the VX6060-RTM.

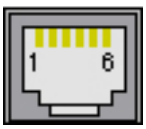
- COM1-A serial port RJ-11 connector is located on the front panel of the RTM.
- COM1-B serial port RJ-11 connector is located onboard.

COM1-A - EIA-232 Simplified

The following figure and table provide pinout information for the 6-pin RJ-11 COM1-A connector CN10-R located on the front panel.

PIN	SIGNAL	DESCRIPTION	I/O
1	--	Not used	--
2	Shell		-
3	TXD	Transmit data	O
4	RXD	Receive data	I
5	GND	Signal ground	--
6	--	Not used	--

Table 42: Front Panel Serial Port Connector Pinout



CN10–R

Figure 45: Front Panel Serial Port Connector

- Serial Cable Designation

  RJ-14 (6 pin, 4 conductor) for a simple EIA-232 without handshake support. A RJ-12 to DB9/DB25 male or DB9/DB25 female adapter is available from multiple sources, such as:

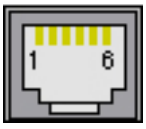
  - Kontron Order Code KIT-RJ12DB9
  - Triangle Cable http://www.trianglecables.com/db9m-rj12.html

COM1-B - EIA-232 Simplified

The following figure and table provide pinout information for the 6-pin RJ-11 COM1-B connector CN19-R located onboard.

PIN	SIGNAL	DESCRIPTION	I/O
1	--	Not used	--
2	Shell		-
3	TXD	Transmit data	O
4	RXD	Receive data	I
5	GND	Signal ground	--
6	--	Not used	--

Table 43: Onboard Serial Port Connector Pinout



CN19–R

Figure 46: Onboard Serial Port Connector

7.5.2 USB Interfaces

There are two USB 2.0 ports available on the VX6060-RTM, each with a maximum transfer rate of 480 Mb/s provided for connecting USB devices.

- One interface is available on the VX6060-RTM front panel. One USB peripheral may be connected to this port. To connect more USB devices, an external hub is required.
- The second USB interface is onboard and used to connect a Flash disk.

USB Front Panel

The following figure and table provide pinout information for the CN11-R connector located on the front panel.

PIN	SIGNAL	FUNCTION	I/O
1	VCC	VCC	--
2	UV0-	Differential USB-	I/O
3	UV0+	Differential USB+	I/O
4	GND	GND	--

Table 44: Front Panel USB Connector Pinout

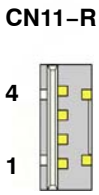


Figure 47: Front Panel USB Connector

The USB host interfaces on the VX6060-RTM can be used with maximum 500 mA continuous load current as specified in the Universal Serial Bus Specification, Revision 2.0. Short-circuit protection is provided. All the signal lines are EMI-filtered.

The Rear I/O interface supports the USB 1.1 and USB 2.0 standards. For USB 2.0 it is strongly recommended to use a cable length not exceeding 3 meters.

USB Onboard

The onboard USB device (CN21-R connector) is used to connect an USB flash disk module. The following figure and table provide pinout information for the onboard USB connector.

PIN	SIGNAL	FUNCTION	I/O
1	USB_PWR	VCC	--
2	N.C.	Not Connected	--
3	USB_D-	Differential USB-	I/O
4	N.C.	Not Connected	--
5	USB_D+	Differential USB+	I/O
6	N.C.	Not Connected	--
7	GND	GND	--
8	N.C.	Not Connected	--
9	N.C.	Not Connected	--
10	N.C.	Not Connected	--

Table 45: Onboard USB Connector Pinout

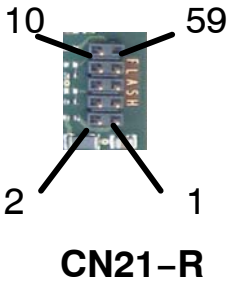


Figure 48: Onboard USB Connector

The USB Flash module is fixed to the board, by using on one side the CN21-R connector, and on the other side, a standoff screwed to the VX6060-RTM board and to the USB Flash module.

Figure 49: USB Flash Disk Overview

Order Code for the USB flash disk:

FDM-USB-*x*GB-2MM-IV: industrial version with conformal coating for use with rugged versions (*x* = up to 16 GB)

USB Flash Disk Layout:

- Maximum space reserved for USB flash disk is 36.9 mm x 26.6 mm (LxW)
- The distance between connector and screw hole is 27.3 mm~27.9mm
- Maximum allowable connector height is 3.68 mm

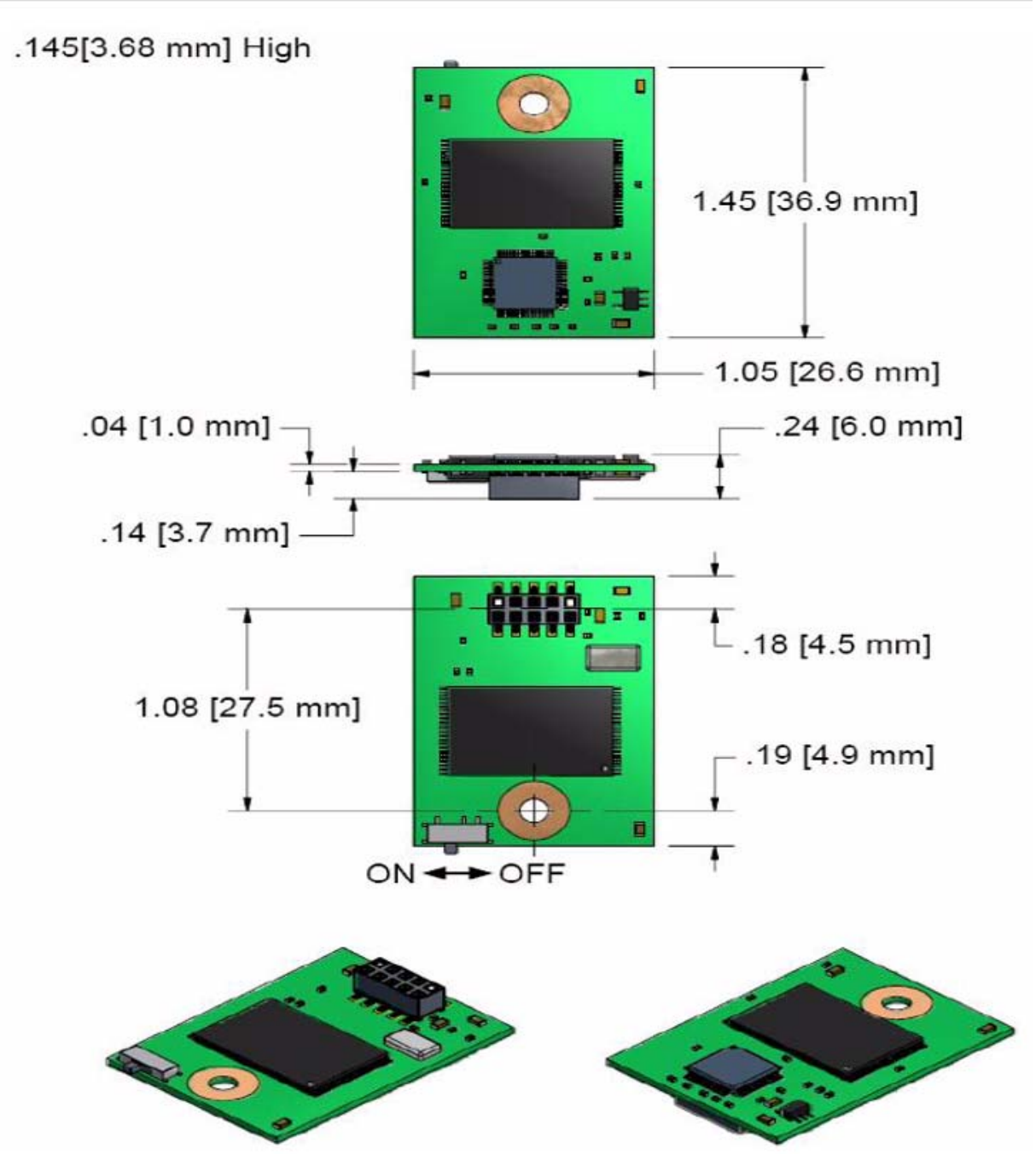


Figure 50: USB Flash Disk Layout

7.5.3 Gigabit Ethernet Interfaces

The Ethernet connector is realized as RJ-45 connectors. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

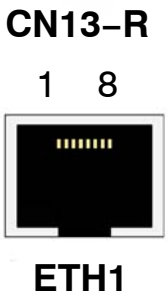


Figure 51: Gigabit Ethernet Connector

The RJ-45 ethernet port signal assigment is described below.

MDI/STANDARD ETHERNET CABLE						PIN	MDIX/CROSSED ETHERNET CABLE					
10BASE-T		100BASE-TX		1000BASE-T			10BASE-T		100BASE-TX		1000BASE-T	
I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL		I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
O	TX+	O	TX+	I/O	BI_DA+	1	I	RX+	I	RX+	I/O	BI_DB+
O	TX-	O	TX-	I/O	BI_DA-	2	I	RX-	I	RX-	I/O	BI_DB-
I	RX+	I	RX+	I/O	BI_DB+	3	O	TX+	O	TX+	I/O	BI_DA+
-	-	-	-	I/O	BI_DC+	4	-	-	-	-	I/O	BI_DD+
-	-	-	-	I/O	BI_DC-	5	-	-	-	-	I/O	BI_DD-
I	TX-	I	RX-	I/O	BI_DB-	6	O	TX-	O	TX-	I/O	BI_DA-
-	-	-	-	I/O	BI_DD+	7	-	-	-	-	I/O	BI_DC+
-	-	-	-	I/O	BI_DD-	8	-	-	-	-	I/O	BI_DC-

Table 46: Gigabit Ethernet Connector Pin Assignment

The Ethernet transmission can operate effectively using a CAT5 cable or higher specifications.

7.5.4 Serial ATA Interfaces

The onboard Serial ATA connectors CN14-R and CN15-R allow the connection of standard HDDs and other Serial ATA devices to the VX6060 Rear Transition Module.

The following figure and table provide pinout information for the SATA connectors CN14-R and CN15-R.

PIN	SIGNAL	DESCRIPTION	I/O
1	GND	Ground signal	--
2	SATA_TX+	Differential Transmit +	O
3	SATA_TX-	Differential Transmit -	O
4	GND	Ground signal	--
5	SATA_RX-	Differential Receive -	I
6	SATA_RX+	Differential Receive +	I
7	GND	Groudn Signal	--

Table 47: Onboard SATA Connectors Pinout

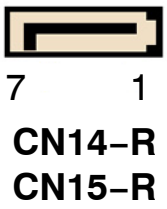


Figure 52: Onboard SATA Connectors

When using a Serial ATA cable, it is recommended to use a special right-angled Serial ATA cable due to possible space limitations within the system. For further information, contact Kontron's Technical Support.

7.5.5 GPIO Connector

Routed from RP1 to CN17-R connector (right angle HE10 10-pin connector male).

PIN	SIGNAL	DESCRIPTION
1	Reserved	
2	Reserved	
3	GND	Ground
4	GND	Ground
5	Reserved	
6	Reserved	
7	GPIO1(*)	General Purpose IO
8	GND	Ground
9	GPIO2/MRST (*)	General Purpose IO
10	GND	Ground

(*) Signals available when RTM is connected to VX6060 product

Table 48: Onboard GPIO Connector Pinout

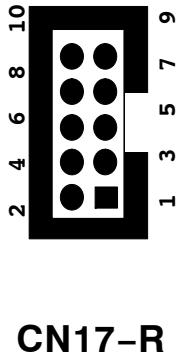


Figure 53: Onboard GPIO Connector

7.5.6 JTAG Connector

Routed from RP0 to CN18-R connector (right angle HE10 10-pin connector male).

PIN	SIGNAL	DESCRIPTION
1	GPIO5 (*)	General Purpose IO
2	GND	Ground
3	Reserved	
4	3.3V sense	
5	GPIO3 (*)	General Purpose IO
6	N.C.	Not Connected
7	N.C.	Not Connected
8	GPIO4 (*)	General Purpose IO
9	Reserved	
10	GND	Ground

(*) Signals available when RTM is connected to VX6060 product

Table 49: Onboard JTAG Connector Pinout

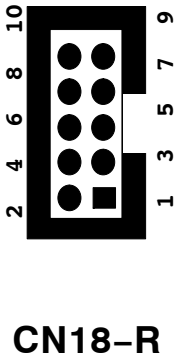


Figure 54: Onboard JTAG Connector

7.5.7 I2C System Management Connector

Routed from RP0 to CN20-R connector (right angle HE10 10-pin connector male).

PIN	SIGNAL	DESCRIPTION
1	Reserved	
2	Reserved	
3	GND	Ground
4	GND	Ground
5	Reserved	
6	Reserved	
7	+3V3_AUX	+3.3V auxiliary power supply
8	+3V3_AUX	+3.3V auxiliary power supply
9	N.C.	Not Connected
10	Reserved	

Table 50: Onboard I2C Connector Pinout

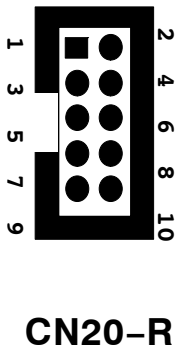
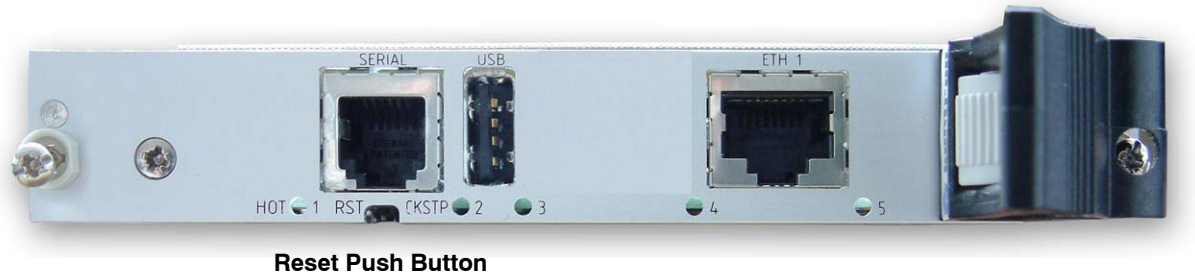


Figure 55: Onboard JTAG Connector

7.6 Reset



Reset Push Button

Figure 56: VX6060-RTM Reset Push Button

Reset and SW1 Reset Switch

The VX6060-RTM generates a system reset signal on the VPX bus at each +5V power-on for a duration of 140 ms to 560 ms.

In addition, the front panel reset push button of the VX6060-RTM is used to generate a VPX bus reset with the same minimum duration.

LEDs

The five LEDs are not connected, and unsued.

7.7 Power Consideration

Only the 5V main power from the VPX is used.

The 3.3V and +12V VPX main power are not used in order to accomodate 6U VPX backplane.

Auxiliary VPX voltages 3.3V (I2C connector), +/- 12V (PIM J10 connector) are used.

The 3.3V on the J10 connector is regulated from the 5V input through a 1.5A max linear regulators.

7.8 Rear I/O Interfaces

The VX6060 Rear Transition Module conducts a wide range of I/O signals through the Rear I/O connectors RP0, RP1 and RP2.

- RP0: one 15-wafer 7-row connector
- RP1: one 16-wafer 7-row connector
- RP2: one 8-wafer 7-row connector

To support the Rear I/O feature a special backplane is necessary. Do not plug a Rear I/O configured board in a non-system slot Rear I/O backplane. Failure to comply with the above may result in damage to your board.

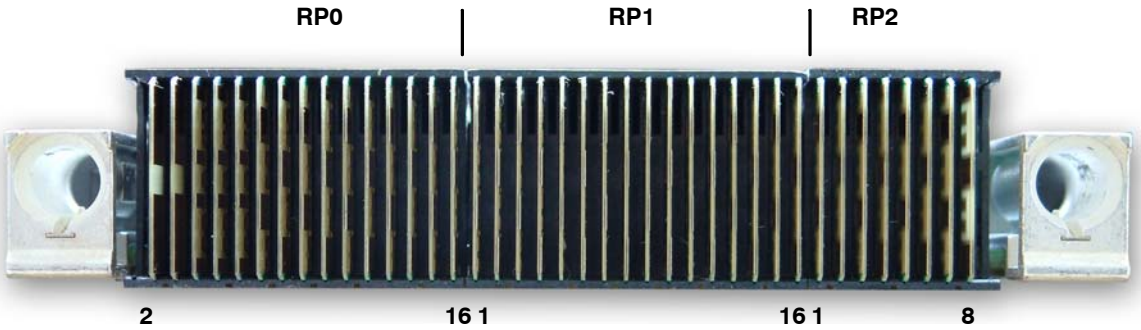


Figure 57: Rear I/O VPX Connectors

The VX6060-RTM provides the following interfaces:

- Two USB 2.0 ports (USB2-A and USB2-B via RP1 connector)
- One Gigabit Ethernet ports without LED signals (ETH0 and ETH1 via RP1 connector)
- Two SATA ports (SATA0 and SATA1 via RP1 connector)
- Two EIA-232 COM ports (COM1-A via RP1 connector, COM1-B via RP2 connector)

7.8.1 RP2 Connector

> Legend for Table 51

COM1-A | COM1-B	Simplified EIA-232 port from	PMCIO 01..32	

RP2 Wafer Assignment

RPM Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A	Board Wafer
1	Reserved	GND	PMCIO 33	PMCIO 35	GND	PMCIO 34	PMCIO 36	P2 w09
2	GND	PMCIO 37	PMCIO 39	GND	PMCIO 38	PMCIO 40	GND	P2 w10
3	COM1-B TXD	GND	PMCIO 41	PMCIO 43	GND	PMCIO 42	PMCIO 44	P2 w11
4	GND	PMCIO 45	PMCIO 47	GND	PMCIO 46	PMCIO 48	GND	P2 w12
5	Reserved	GND	PMCIO 49	PMCIO 51	GND	PMCIO 50	PMCIO 52	P2 w13
6	GND	PMCIO 53	PMCIO 55	GND	PMCIO 54	PMCIO 56	GND	P2 w14
7	COM1-B RXD	GND	PMCIO 57	PMCIO 59	GND	PMCIO 58	PMCIO 60	P2 w15
8	GND	PMCIO 61	PMCIO 63	GND	PMCIO 62	PMCIO 64	GND	P2 w16
CASE	GND							

Table 51: Rear I/O VPX Connector RP2 Wafer Assignment

RP2 Signal Definition

Mnemonic	Signal Definition
COM1-B RXD	Channel EIA-232 Receive Data
COM1-B TXD	Channel EIA-232 Transmit Data
GND	Ground
PMCIO [33..64]	PCI PMC signals - I/Os signals from PMC connector (J14) to RP2 connector.

Table 52: Rear I/O VPX Connector RP2 Signal Definition

7.8.2 RP1 Connector

RP1 Wafer Assignment

> Legend for Table 53

ETH-SW	Gigabit Ethernet port	USB2-A | USb2-B	USB link 0 fromCPUA | CPUB
COM1-A | COM1-B	Simplified EIA-232 port from	SATA0-A | SATA0-B	Serial ATA link from CPUA | CPUB
PMCIO 01..32			

RPM Wafer	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A	Board Wafer
1	USB2-A PWR	GND	SATA0-A TX-	SATA0-A TX+	GND	SATA0-A RX-	SATA0-A RX+	P1 w09
2	GND	SATA0-B TX-	SATA0-B TX+	GND	SATA0-B RX-	SATA0-B RX+	GND	P1 w10
3	USB2-B PWR	GND	Reserved	Reserved	GND	Reserved	Reserved	P1 w11
4	GND	USB2-A DA-	USB2-A DA+	GND	USB2-B DA-	USB2-B DA+	GND	P1 w12
5	Reserved	GND	ETH-SW DB-	ETH-SW DB+	GND	ETH-SW DA-	ETH-SW DA+	P1 w13
6	GND	ETH-SW DD-	ETH-SW DD+	GND	ETH-SW DC-	ETH-SW DC+	GND	P1 w14
7	Reserved	GND	Reserved	Reserved	GND	Reserved	Reserved	P1 w15
8	GND	Reserved	Reserved	GND	Reserved	Reserved	GND	P1 w16
9	Reserved	GND	PMCIO 01	PMCIO 03	GND	PMCIO 02	PMCIO 04	P2 w01
10	GND	PMCIO 05	PMCIO 07	GND	PMCIO 06	PMCIO 08	GND	P2 w02
11	COM1-A TXD	GND	PMCIO 09	PMCIO 11	GND	PMCIO 10	PMCIO 12	P2 w03
12	GND	PMCIO 13	PMCIO 15	GND	PMCIO 14	PMCIO 16	GND	P2 w04
13	Reserved	GND	PMCIO 17	PMCIO 19	GND	PMCIO 18	PMCIO 20	P2 w05
14	GND	PMCIO 21	PMCIO 23	GND	PMCIO 22	PMCIO 24	GND	P2 w06
15	COM1-A RXD	GND	PMCIO 25	PMCIO 27	GND	PMCIO 26	PMCIO 28	P2 w07
16	GND	PMCIO 29	PMCIO 31	GND	PMCIO 30	PMCIO 32	GND	P2 w08
CASE	GND							

Table 53: Rear I/O VPX Connector RP1 Wafer Assignment

RP1 Signal Definition

Mnemonic	Signal Definition
ETH-SW D[A..D]+/-	Ethernet *x:* First to Fourth pair of Transmit/receive data.
GND	Ground
PMCIO [01..32]	PCI PMC signals - I/Os signals from PMC connector (J14) to RP1 connector.
SATA*x* RX/TX+/-	Serial ATA *x* Receive/Transmit +/-
USB*x* DA+/-	Differential Data Pair of USB Line *x*
USB*x* PWR	USB Line *x*

Table 54: Rear I/O VPX Connector RP1 Signal Definition

7.8.3 RP0 Connector

RP0 Wafer Assignment

RPM Wafer	Row G	Row F	Row E	Row D	Row C	Row B	Row A	Board Wafer
2	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	P0 w02
3	+5V	+5V	+5V	+5V	+5V	+5V	+5V	P0 w03
4	Reserved	Reserved	GND	-12V_AUX	GND	SYSRESET*	NVMRO	P0 w04
5	N.C.	N.C.	GND	3V3_AUX	GND	Reserved	Reserved	P0 w05
6	N.C.	N.C.	GND	N.C.	GND	N.C.	N.C.	P0 w06
7	TCK	GND	Reserved	Reserved	GND	Reserved	Reserved	P0 w07
8	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	P0 w08
9	Reserved	GND	N.C.	N.C.	GND	N.C.	N.C.	P1 w01
10	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	P1 w02
11	N.C.	GND	N.C.	N.C.	GND	N.C.	N.C.	P1 w03
12	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	P1 w04
13	N.C.	GND	N.C.	N.C.	GND	N.C.	N.C.	P1 w05
14	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	P1 w06
15	N.C.	GND	N.C.	N.C.	GND	N.C.	N.C.	P1 w07
16	GND	N.C.	N.C.	GND	N.C.	N.C.	GND	P1 w08
CASE	GND							

* signal active when low

Table 55: Rear I/O VPX Connector RP0 Wafer Assignment

RP0 Signal Definition

Mnemonic	Signal Definition
+/-12V_AUX	Auxiliary Power Supplies
3V3_AUX	3.3V Auxiliary Power, System Management
+5V	+5V Power Input
GND	Ground
NVMRO	Non-Volatile Memory Read Only
N.C.	Not Connected
SYSRESET*	System Reset

Table 56: Rear I/O VPX Connector RP0 Signal Definition

7.9 PCI 64 PIM Connector

7.9.1 J14 Connector

J14 Connector Pin Assignment

Pin	Signal
01	PMC64 IO 01
...	...
64	PMC64 IO 64

Signal Description

Mnemonic	Description
PMC64 IO xx	I/O 01 through 64 of the motherboard

7.9.2 J10 Connector

J10 Connector Pin Assignment

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
01	N.C.	02	+12V_AUX	03	N.C.	04	N.C.
05	+5V	06	N.C.	07	N.C.	08	N.C.
09	N.C.	10	+3.3V	11	N.C.	12	N.C.
13	GND	14	N.C.	15	N.C.	16	N.C.
17	N.C.	18	GND	19	N.C.	20	N.C.
21	+5V	22	N.C.	23	N.C.	24	N.C.
25	N.C.	26	+3.3V	27	N.C.	28	N.C.
29	GND	30	N.C.	31	N.C.	32	N.C.
33	N.C.	34	GND	35	N.C.	36	N.C.
37	+5V	38	N.C.	39	N.C.	40	N.C.
41	N.C.	42	+3.3V	43	N.C.	44	N.C.
45	GND	46	N.C.	47	N.C.	48	N.C.
49	N.C.	50	GND	51	N.C.	52	N.C.
53	+5V	54	N.C.	55	N.C.	56	N.C.
57	N.C.	58	+3.3V	59	N.C.	60	N.C.
61	-12V_AUX	62	N.C.	63	N.C.	64	N.C.

Signal Description

Mnemonic	Description
+/-12V-AUX	Auxiliary Power Supplies
+3.3V	+3.3V Power Input
+5V	+5V Power Input
GND	Ground
N.C.	Not Connected

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