USER'S GUIDE

VX6090

CA.DT.B20-5e - April 2017

POSSIBILITIES START HERE kontron

VX6090 User's Guide

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1e	Preliminary Version 1	02-2016
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Customer Support

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Customer Service

As a trusted technology innovator and global solutions provider, Kontron extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly-experienced support enables Kontron to provide exceptional peace of mind to build and maintain successful products.

For more details on Kontron's service offerings such as: enhanced repair services, extended warranty, Kontron training academy, and more visit http://www.kontron.com/support-and-services/services.

Customer Comments

If you have any difficulties using this manual, discover an error, or just want to provide some feedback, contact Kontron support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised manual on our website.

SYMBOLS

The following symbols may be used in this manual:

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
NOTICE	NOTICE indicates a property damage message.
	**Electric Shock!** This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	**ESD Sensitive Device!** This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	**HOT Surface!** Do NOT touch! Allow to cool before servicing.
	**Laser!** This symbol inform of the risk of exposure to laser beam from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user manual. This symbol also indicates detail information about the specific product configuration.
	This symbol precedes helpful hints and tips for daily use.

FOR YOUR SAFETY

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning!
All operations on this device must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Caution, Electric Shock!
Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.
Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instructions

ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

GENERAL INSTRUCTIONS ON USAGE

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this manual or received from Kontron's Technical Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version, that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present manual.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

ENVIRONMENTAL PROTECTION STATEMENT

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Environmental protection is a high priority with Kontron.
Kontron follows the DEEE/WEEE directive.
You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when they become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE

Improve the environmental performance of all those involved during the lifecycle of EEE

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1 / Introduction

Based on the Intel® Xeon® D processor, the VX6090 is a high-performance, SWaP-C optimized, 6U VPX computing blade well suited for intensive data and signal processing in domains such as Military, Aerospace and Transportation.

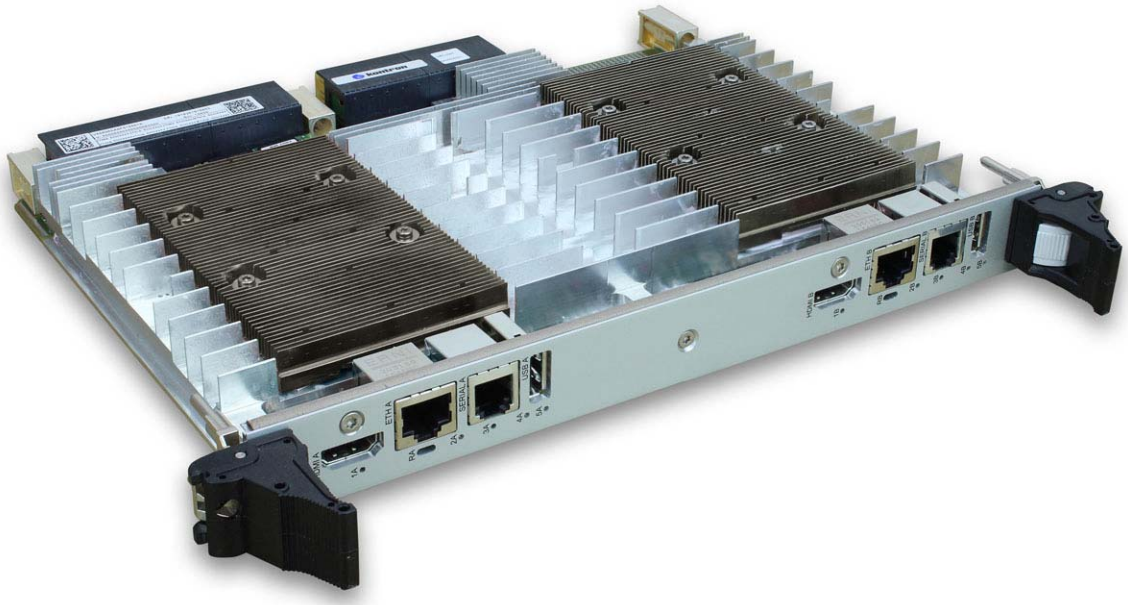
The board is structured as two symmetrical computing blocks referred to as side A and side B. Each side is built around the Xeon® D system-on-chip (SoC) and features eight 64-bit cores, up to 16 GBytes of DDR4-2400 memory, a dual 10 Gigabit Ethernet, a high bandwidth PCI Express 3.0 link, a 2-D SM750 graphic controller, two 1 GbE Ethernet controllers and a M.2 socket for SSD M.2 modules. In addition, several I/Os ports are available on front panel and rear backplane as well: SATA, USB 3.0, USB 2.0, serials and GPIOs.

Seated between these two sides, an optional high-performance XMC slot provides further storage, computing or I/O possibilities.

To interconnect VX6090 boards in switched OpenVPX environments, Kontron has developped the VX3920, a 10 Gigabit Ethernet switch and the VX3905, a PCI Express switch.

The VX6090 comes with EFI BIOS. It is covered by Kontron's long term supply program, which guarantees customers multi-year supply of the product beyond its active life.

Figure 1: VX6090-SA 6U VPX Overview



1.1 Manual Overview

1.1.1 Objective

This guide provides general information, hardware instructions, operating instructions and functional description of the VX6090 board. The onboard programming, onboard firmware and other software (e.g. drivers and BSPs) are described in detail in separate guides (see section 1.3 "Related Publications").

This hardware technical documentation reflects the most recent version of the product. The "Hardware release Notes" (see section 1.3 "Related Publications") might help to keep track of potential evolutions.

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

1.1.2 Audience

This guide is written to cover, as far as possible the range of people who will handle or use the VX6090, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, system, cabling, grounding and communications.

1.1.3 Scope

This guide describes all variants of the VX6090 series.

1.1.4 Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- Chapter 1 - Introduction (this chapter)
- Chapter 2 - Board Overview
- Chapter 3 - Installation
- Chapter 4 - Additional Board Features
- Chapter 5 - Physical I/O
- Chapter 6 - Electrical Specifications
- Chapter 7 - Power and Thermal Management
- Chapter 8 - Backplane Suggestions

1.1.5 Terminology, Definitions and Abbreviations

- In this document, the term VX6090 designates the whole VX6090 6U VPX board family (air-cooled, either commercial or extended temperature range).

- Sides A and B identification

The two symmetrical computing blocks are referred to as Side A and Side B. Their parts are identified by the corresponding A and B suffixes: SoCA vs SoCB, CPLDA vs CPLDB etc. The different ports are labelled in the same way: ETH0A vs ETH0B etc.

Terms and acronyms

TERM OR ACRONYM	DEFINITION
1 GbE, 10 GbE	Abbreviation for 1-Gbit Ethernet interfaces (1000BASE-T or 1000BASE-KX) and 10-Gbit Ethernet interfaces (10GBASE-KR).
AVX2 (Intel®)	Intel Advanced Vector Extensions 2.0. A set of advanced instructions including 256-bit integer instructions, floating-point fused multiply add (FMA) instructions and gather operations meant to improve performance in math and digital signal processing, vector calculations and general purpose high performance computing.
Core	A processing unit including instruction cache, data cache, and often L2 cache.
COTS	Commercial Off The Shelf.
LPC	Low Pin Count bus interface.
MTBF	Mean Time Between Failure.
Option	A feature which requires a specific order code.
PCB	Printed Circuit Board.
PCH	Platform Controller Hub. In Xeon® D architecture, the PCH is integrated in the SoC.
Processor	According to Intel terminology, the processor - synonymous with SoC - includes the 64-bit cores, uncore, I/Os, Integrated PCH Logic, Integrated 10Gb, and package.
Provision	A feature not yet available.
PTU (Intel®)	Intel® Performance Test Utility.
SBC	Single Board Computer (the term defaults to VX6090).
SKU	Stock Keeping Unit: A catalog's product and service identification code.
SMBus	System Management Bus.
SoC (Intel®)	System-on-a-chip. According to Intel terminology, the SoC - synonymous with processor - includes the 64-bit cores, uncore, I/Os, Integrated PCH Logic, Integrated 10Gb, and package. In this document, SoCA and SoCB terms are used to identify SoC on side A or B of the VX6090.
SWaP, SWaP-C	Seize, Weight and Power - Cost: an acronym to summarize the capabilities of an embedded system in Military or Aerospace.
TDP	Thermal Design Power: the target power level of the processor. It represents the maximum sustained power expected from realistic applications. It is an input to the thermal design of the board.
TPM	Trusted Platform Module: An international standard for a secure cryptoprocessor based on a dedicated hardware device and integrating cryptographic keys. Promoted by consortium TCG (Trusted Computing Group).
Turbo Boost Technology (Intel®)	A feature that opportunistically enables the processor to run a faster frequency. This results in increased performance of both single and multi-threaded applications.
Uncore	In Xeon® D architecture, a unit of the SoC which includes the Ring, the Caching Agent Cbo, the Last Level Cache (LLC), the Home Agent (HA), the Integrated Memory Controller (IMC), the Integrated I/O Module (IIO), the Power Control Unit (PCU).

1.2 VPX Overview

For many years, VITA VME has been the de-facto bus standard for COTS Circuit Card Assemblies. Although it did well to enhance transfer rates and accomodate new technologies (namely VME320 and PCI mezzanines cards), there came a time when a technology break was necessary to address new needs in high-speed serial switch fabric interconnects and power delivery. To this purpose, VITA 46 VPX was introduced with newly designed high-speed connectors and back-planes compatible with former VME systems form factors.

VPX is now a well established standard, giving to the large existing base of VMEbus users access to the latest switched fabrics technologies.

For further information regarding VPX and its use, visit VITA home page "Open Standards, Open Markets" (http://www.vita.com)

1.3 Related Publications

The following publications contain information relating to this product:

Table 1: Related Publications

TOPIC	PUBLICATION
Standard	
ANSI/VITA 42.0	XMC Switched Mezzanine Card Auxiliary Standard - ANSI/VITA 42.0-2008 (R2014)
ANSI/VITA 42.3	XMC PCI Express Protocol Layer Standard - ANSI/ VITA 42.3-2006
ANSI/VITA 46.0	VPX Baseline Standard - ANSI/VITA 46.0-2007 (R2013)
ANIS/VITA 46.4	PCI Express® on VPX Fabric Connector - ANSI/VITA 46.4-2012
ANSI/VITA 46.6	Gigabit Ethernet Control Plane on VPX - ANSI/VITA 46.6-2013
ANSI/VITA 46.9	XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules- VITA
ANSI/VITA 46.10	Rear Transition Module for VPX - ANSI/VITA 46.10-2009
ANSI/VITA 47	Environments, Design and Construction, Safety, and Quality for Plug-In Units Standard ANSI/VITA 47-2005 (R2007)
ANSI/VITA 48.1	Mechanical Specification for Microcomputers Using REDI Air Cooling - ANSI/VITA 48.1 - 2010.
ANSI/VITA 61.0	XMC 2.0 - ANSI/VITA 61.0-2011 (R2014)
ANSI/VITA 65	OpenVPX™ System Specification - ANSI/VITA 65-2010 (R2012)
IEC62380	Reliability data handbook – Universal model for reliability prediction of electronics components, PCBs and equipment - IEC IEC62380-2004
IEEE 802.3	- Clause 40 and other clauses related to 1000BASE-T: IEEE 802.3 Physical Layer specification for a 1000 Mb/s CSMA/CD LAN using four pairs of Category 5 balanced copper cabling. - Clause 70 and other clauses related to 1000BASE-KX: IEEE 802.3 Physical Layer specification for 1 Gb/s using 1000BASE-X encoding over an electrical backplane. - Clause 72 and other clauses related to 10GBASE-KR: IEEE 802.3 Physical Layer specification for 10 Gb/s using 10GBASE-R encoding over an electrical backplane. IEEE 802.3-2012
MIL-HDBK-217	Military Handbook - Reliabiliity Prediction of Electronic Equipment - Department Of Defense MIL-HDBK-217-1991
MIL-STD-810-G	Environmental Engineering Considerations and Laboratory Tests - Department Of Defense MIL-STD-810-G w/ Change 1 - 2014
PCI Express M.2	PCI Express M.2 Specification - PCI SIG-2013
Serial ATA	Serial ATA Revision 3.2 - SATA IO-2013
Trusted Platform Module	TPM Main Specification Level 2 Version 1.2, Revision 116 Part 1 – Design Principles Part 2 – Structures of the TPM Part 3 – Commands
Hardware	
VX6090	VX6090 Hardware Release Notes TBD
Firmware	
VX6090	AMI-BIOS User Reference Manual TBD

2 / Board Overview

2.1 Main Features

2.1.1 A Harsh Environment Computing Node

The VX6090 computing node is designed to meet the requirements of harsh environment market segments. It allows intensive parallel data or signal processing in full meshed or switched OpenVPX environments. Target applications include radar, sonar, imaging systems, airborne fighters, and unmanned aerial vehicle (UAV), as well as rugged multi-display consoles and transportation applications.

2.1.2 A Symmetrical Architecture featuring two Multi-Core SoC

The VX6090 is structured as two symmetrical computing blocks also referred to as Side A and Side B. Each side implements a Xeon® D SoC coupled to a dual channel DDR4 memory and several additional features listed below. The two sides are fully independent; and the power supplies sequencing and monitoring, the reset and alerts handling are performed separately by each CPLD. Nevertheless, both sides share most of the VPX ressources: VS1 power supply, PCI Express gen3 x8 port, two different SMBus, GPIOs and various control and supervisory signals such as GEOID, SYSRESET#, NVMRO, clocks…

2.1.3 The Xeon® D System on Chip

The Xeon® D SoC is a 64-bit, multi-core SoC built on 14-nanometer process technology. It implements:

- Eight cores running at a rated frequency of 2.0 GHz in the 45 W TDP version. This frequency can be either decreased in order to make appropriate power/performance trade-offs or opportunistically increased via "Turbo Boost" to enhance performance. Each core includes two levels of cache: Instruction and Data Cache (ICU and DCU, corresponding to a L1 cache) and Mid-Level Cache (MLC, corresponding to a L2 cache). The cores support Intel Hyper-Threading Technology (two threads per core).
- A unit called "uncore module" which implements the "Ring", a bi-directionnal topology to interconnect core and uncore modules, the "Caching Agent" (Cbo), the Last Level Cache (LLC, corresponding to a L3 cache), the "Home Agent" (HA) which handles the DRAM requests, the Integrated Memory Controller (IMC), the "Integrated I/O Module" (IIO) which is the PCI Express interface and the "Power Control Unit" (PCU).
- An integrated 10 GbE controller with two 10 GbE MACs supporting XGMII interfaces to KR physical device interfaces (10GBASE-KR as per IEEE802.3 clause 72 or 1000BASE-KX as per IEEE802.3 clause 70).
- An integrated PCH implementing several PCI Express gen3 and gen2 interfaces, SATA III ports, USB 3.0 and USB 2.0 ports, a SMBus, a LPC interface, two UARTs.

2.1.4 Soldered DDR4 Memories with the Support of ECC

The two banks of DDR4-2400 memory include ECC and are soldered directly on the PCB. They totalize a capacity of 16 GB for each SoC.

2.1.5 Additional Features

Each computing side implements the following additionnal features:

- One 1000BASE-T Intel i210IT controller routed either to the front or to the rear.
- One 1000BASE-KX Intel i210IS controller routed to the rear but which can also be used for bridging SoCA and SoCB.

- One 2-D graphic Silicon Motion SM750 controller connected to the front: 16 MB embedded DDR memory (32 bits mode), no RGB interface, single TFP 24-bit interface used with Texas Instruments TFP410-EP transmitter, maximum resolution of 1280x1024
- One M.2 socket to host SSD M.2 modules.
- One RTC and a watchdog/timer.
- A CPLD which handles the I2C interfaces, resets, internal power-supplies and their monitoring

2.1.6 Optional XMC Slot

Seated between the two computing blocks, an optional VITA 61 XMC slot provides further storage, computing or I/O possibilities.

2.1.7 Numerous Storage Interface and Non Volatile Memories

- The M.2 socket can host SATA III SSD modules with various form factors and capacities: 2242-D5-M on sides A and B, and 2260-D5-M or 2280-D5-M on side A. This allows the equipment of large SLC SSD (up to 256 GBytes).
- Redundant 64-Mbit SPI NOR Flash memories are used to store firmware code.
- Two serial 256-Kbit I2C EEPROMs per side are dedicated to VPD and data storage.
- One 1-Mbit non-volatile, ferroelectric RAM per side allows the backup of critical data when the board is powered off. This F-RAM is a user memory device.
- Lastly, several SPI Flash and EEPROMs store the set-up information for the local controllers: PCI Express switch PEX8725, Ethernet controllers (10GBASE-KR LAN, 1000BASE-T, 1000BASE-KX), graphic controller SM750, XMC, DDR4 SPD.

All on board Flash devices and non volatile memories have a write protect mechanism implementing the VPX NVMRO signal. See section 4.8 page 38 for detailed information.

2.1.8 Form Factor and Temperature Grade

The VX6090 form factor is VPX 6U, 5 HP (233.35 x 160 x 25.4 mm).

It is available in two versions: standard air-cooled 0 to 55°C (SA) and ruggedized air-cooled -25°C to +55°C. For more information on power and thermal specifications, see chapter 6 page 68.

2.1.9 Software

Kontron is one of the few compact PCI, VME and VPX vendors providing in-house support for most of the industry-proven real-time operating systems that are currently available. Due to its close relationship with the software editors, Kontron is able to produce and support BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology.

The VX6090 is delivered with the UEFI BIOS from AMI.

For information regarding operating systems and software support, please contact Kontron.

2.2 Block Diagram

Figure 2: VX6090 Simplified Block Diagram

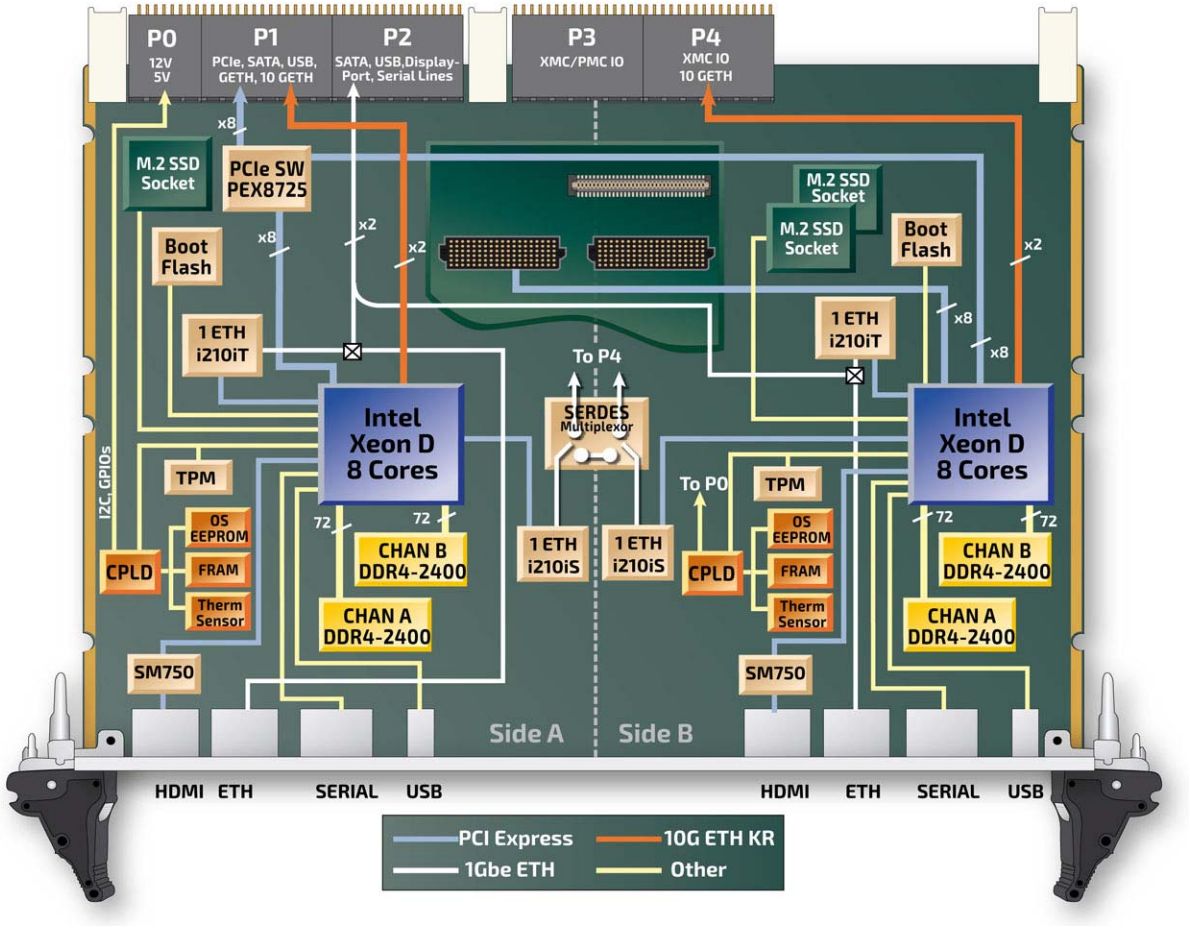
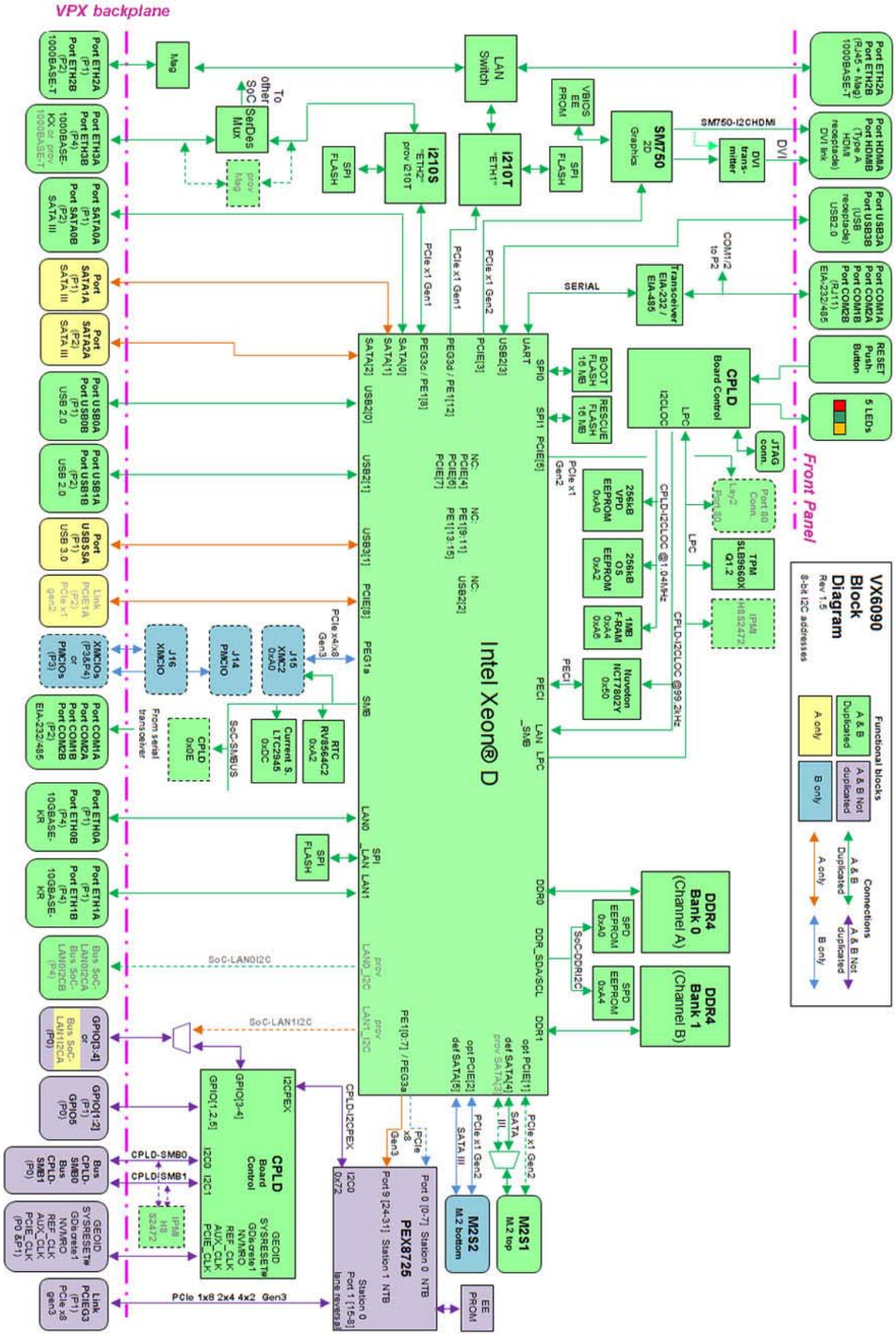


Figure 3: VX6090 Detailed Block Diagram



2.3 Ordering Information

2.3.1 Manufacturing Options

- Core Frequency: 2.0 GHz (other frequencies on demand)
- Processor TDP: 45W (other TDP on demand)
- DDR4 SDRAM Size: 16 GB per side, 32 GB total (other capacities on demand)
- VPX PCI Express interface: Optional
- XMC Slot (VITA 61 / XMC 2.0 12 mm): Optional.
- Supercap: On demand
- Ruggedization Levels: Standard Air-Cooled (SA), Rugged Air-Cooled
- Conformal Coating Optional in SA class, Standard in Rugged Air Cooled.
- Mounted M.2 module: On demand, M.2 module may be mounted before delivery

2.3.2 Available Order Codes

Table 2: VX6090 Order Codes

ORDER CODE		DESCRIPTION
VX6090	VX6090SA8G0050010	6U VPX Single Board Computer Two 8-core Intel® Xeon® D processors D-1548, 2.0 GHz, TDP 45 W 16-GB dualbank DDR4 per processor (32 GB total) Standard air cooled (SA) 0°C to +55°C No Switched PCI Express interface No XMC slot
VX6090	VX6090RA8G0050010	6U VPX Single Board Computer Two 8-core Intel® Xeon® D processors D-1548, 2.0 GHz, TDP 45 W 16-GB dualbank DDR4 per processor (32 GB total) Rugged air cooled -25°C to +55°C No Switched PCI Express interface No XMC slot

2.4 I/O Interfaces

2.4.1 Front Interfaces

Figure 4: VX6090 Front Panel I/O Interfaces

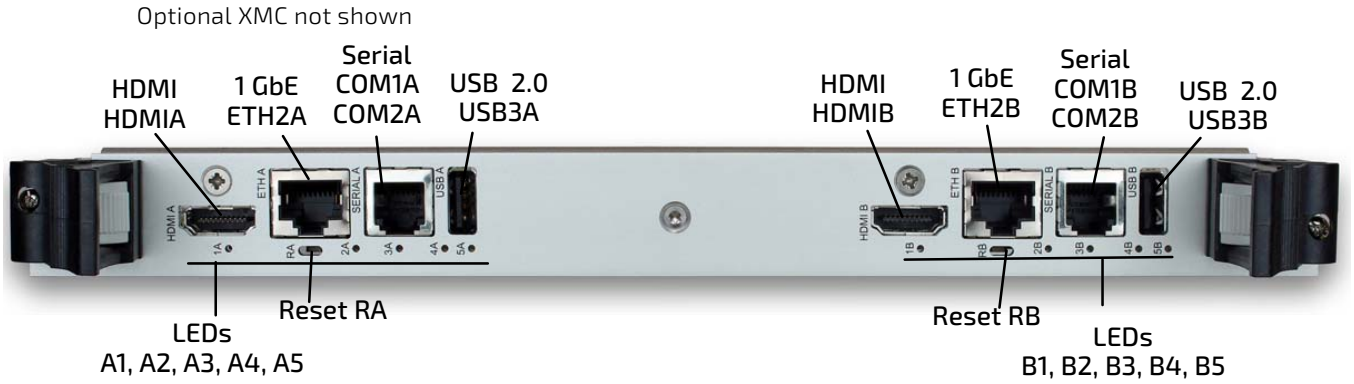


Table 3: Front I/O Interfaces

PORT ID	FUNCTION	DESCRIPTION	SEE ALSO
COM1A, COM2A COM1B, COM2B	Serial Ports	2x EIA-232 ports (COM1x and COM2x) or 1x EIA-485 (COM1x) port. Note: These ports are also routed to rear P2.	Section 5.1.1 for Pin Assignment
ETH2A ETH2B	Gigabit Ethernet	1000BASE-T port on RJ45 connectors. Note: This port may be routed to rear P1 through specific BIOS setting.	Section 5.1.2 for Pin Assignment
USB3A USB3B	USB 2.0	USB 2.0 ports	Section 5.1.3 for Pin Assignment
HDMIA HDMIB	HDMI Graphics	HDMI interface (without audio)	Section 5.1.4 for Pin Assignment
RA RB	Reset	Reset push button.	Figure 4
A1 to A5 B1 to B5	LEDs	5 LEDs reporting the board processor health status and activity	Section 5.4 for LEDs Description

2.4.2 Rear Interfaces

Compliant with:

- VITA 46.0 (Standard VPX)
- VITA 46.4 (PCI Express on VPX)
- VITA 46.9 (XMC and I/O on VPX)
- VITA 65 (OpenVPX System specification): VX6090 rear I/Os mapping is fully compliant with OpenVPX system Specification (VITA 65), Payload Slot Profile SLT6-PAY-2F2U2T-10.2.5.

Figure 5: VX6090 Rear I/O Distribution

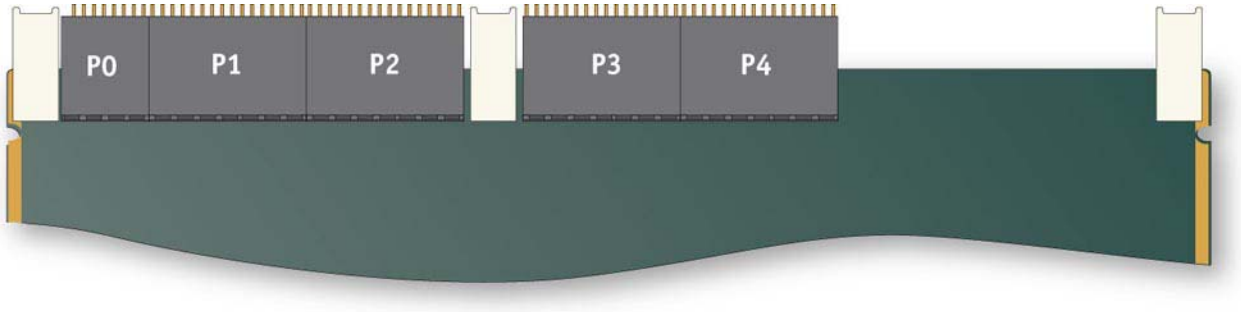


Table 4: Rear I/O Interfaces

	VPX P0	VPX P1	VPX P2	VPX P3	VPX P4
PCIE		Link PCIEG3: x8 gen3 PCI Express	Provision: Link PCIE1A: 1x gen2 PCI Express		
SATA		Ports SATA0A & SATA1A: SATA III	Ports SATA0B & SATA2A: SATA III		
USB		Ports USB0A & USB0B: USB 2.0 Port USBSSA: USB 3.0	Port USB1A & USB1B: USB 2.0		
ETH		Port ETH2A: 1000BASE-T Port ETH0A & ETH1A: 10GBASE-KR	Port ETH2B: 1000BASE-T		Ports ETH3A & ETH3B: 1000BASE-KX or opt 1000BASE-T Port ETH0B & ETH1B: 10GBASE-KR
SER			Ports COM1A, COM2A, COM1B, COM2B: EIA-232 or EIA422/485		
GPIOs	GPIO[3:4], GPIO5	GDISCRETE1, GPIO1, GPIO2/Mask. Reset*			
I2C	CPLD-SMB0 CPLD-SMB1				
XMC I/Os				XMCIOs: X38s or PMCIOs: P64s	XMCIOs: X8d + X12d
CLK	REF_CLK, AUX_CLK PCIE_CLK				
MISC	12V (VS1), -12V_AUX, 3.3V_AUX SYSRESET*, NVMRO, GEOID	P1_VBAT, SYS_CON*			

2.5 Components Layout

Figure 6: VX6090 Components Layout (Top view)

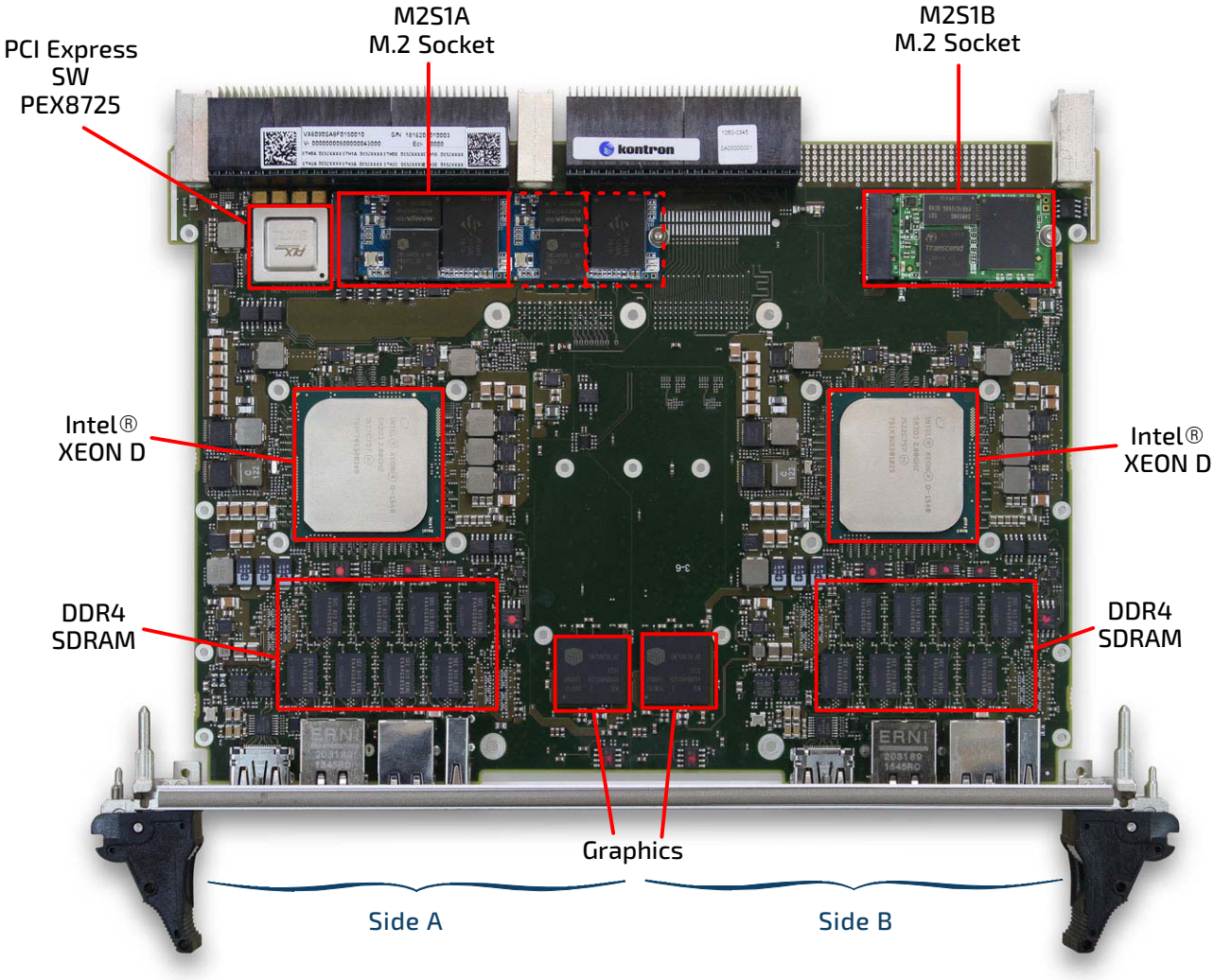
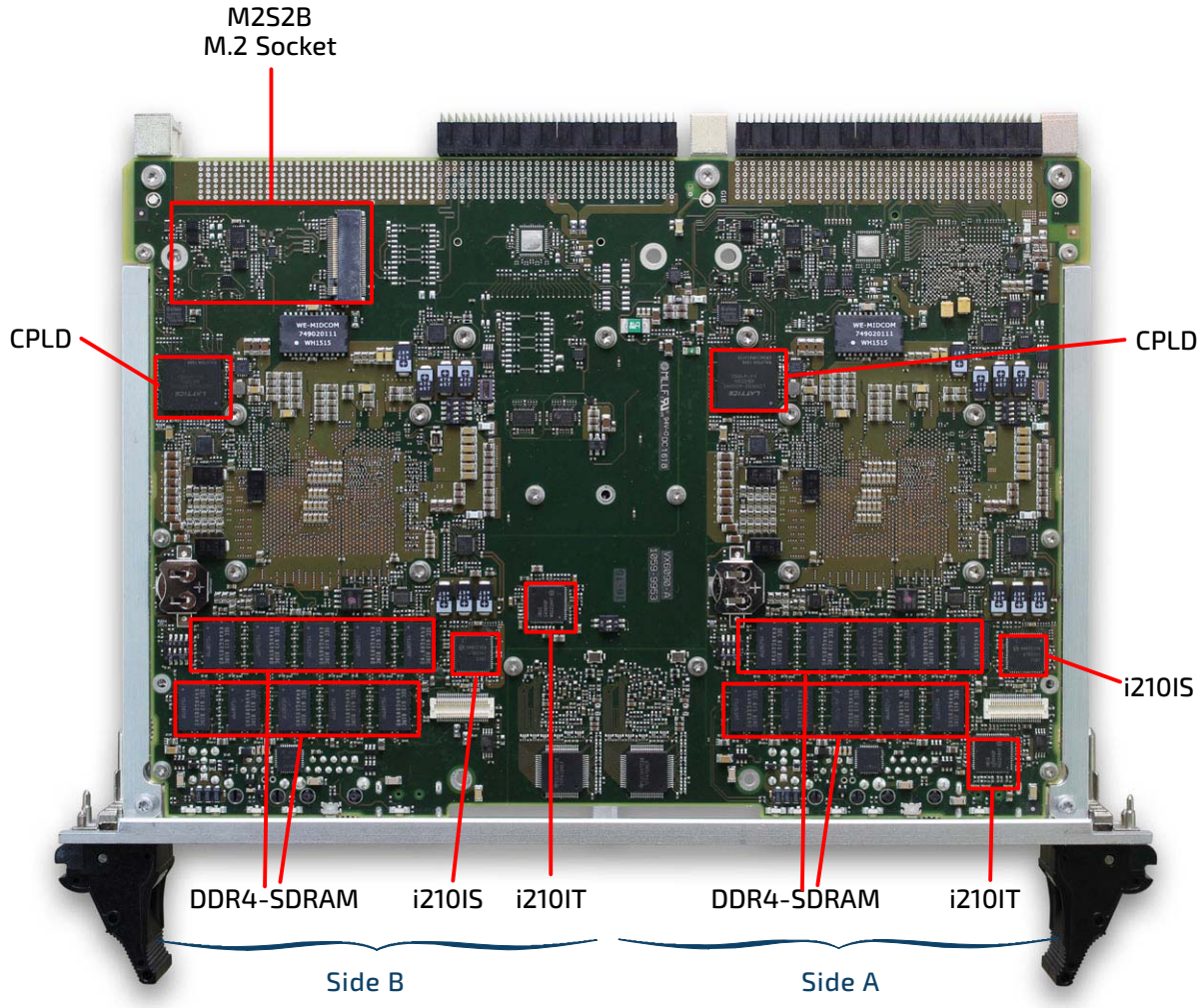


Figure 7: VX6090 Components Layout (Bottom view)



2.6 Technical Specifications

Table 5: VX6090 Main Characteristics

DEVICE OR FUNCTION	DESCRIPTION	SIDE A	SIDE B
ONBOARD FUNCTIONS			
Processor	Intel® Xeon® D Octo Core™, 45 W, 2.0 GHz (8 execution cores, 16 threads, 12 MB)	X	X
System DDR4 memory	DDR4 dual channel memory with ECC, 2400 MT/s over 144 bits.	16 Gbytes	16 Gbytes
RTC, Watchdog, Timer	- RTC: RV8564C2 device powered by onboard battery or backplane VBAT. Connected to SoC-SMBus. - Watchdog and Timer (integrated in CPLD): timeout ranging from 2 µs to 510s, IRQ, Reset, dual-stage	X	X
F-RAM, boot and rescue Flash Devices, VPD and OS EEPROM	- F-RAM: 1-Mbit serial I2C device. Connected to CPLD-I2CLOC bus. - Boot and rescue Flash Devices: 16-MByte devices. Connected to SoC SPI0 and SPI1 interfaces. - VPD and OS EEPROM: 256k-Byte devices. Connected to CPLD-I2CLOC bus.	X	X
System CPLD	The CPLD handles the I2C interfaces, poweron/poweroff controls and board resets, internal power-supplies sequencing and their monitoring, alerts, LEDs, GPIOs, onboard Ethernet multiplexors control, serial lines configuration. Configuration/status registers can be accessed from SoC LPC interface.	X	X
TPM	TPM device, version 1.2, revision 116. Component SLB9660XQ1.2 FW 4.40 by Infineon. Connected to SoC LPC interface.	X	X
ONBOARD INTERFACES			
Top M.2 socket	One M.2 socket 2242-D5-M H4.2 on side A and side B. On side A the socket M2S1A can also host 2260-D5-M or 2280-D5-M modules. Connected to SoC interface SATA[4]. For a connection to the SoC PCI Express interface PCIE[1], contact Kontron.	M2S1A	M2S1B
Bottom M.2 socket	One M.2 socket 2242-D4-M H4.2 is available on bottom side of side B. Connected to SoC interface SATA[5]. For a connection to the SoC PCI Express interface PCIE[1], please contact Kontron.	-	M2S2B
Port 80	Provisional Port 80 on bottom side of the board. Connected to SoC LPC interface.	X	X
PCI Express gen2 port on Port 80 connector	Provisional PCI Express 2.0 link, fixed x1 configuration. Connected to SoC PCI Express interface PCIE[5].	X	X
XMC slot	Optional VITA 46.9 XMC2 slot . Connected to SoCB PCI Express x8 gen3 interface PE2[7:0]. Stack 12 mm achieved by motherboard connectors. XMC mezzanine: 10 mm stack form factor. XMC I/Os: VITA 46.9 X12d+X8d+X38s from J16 to P3/P4. PMC I/Os: P64s from J14 to P3.	-	Routed to SoCB rear I/Os P3/P4. Access from front panel
FRONT PANEL			
1000BASE-T port	Intel i210IT controller. 10/100/1000BASE-T protocol with Auto-Negotiation. Auto-wire switching for crossed cables (Auto-MDI/X). Connection: from SoC PCI Express interface PE1[12] (a PCI Express gen3 interface but used as PCI Express gen1 x1) to LAN switch and front RJ45 connector.	ETH2A	ETH2B
USB2.0 port	USB2.0 port. Connection: from SoC USB interface USB[3] to front panel.	USB3A	USB3B
Serial port	Two full duplex EIA-232 interfaces (default) or one full duplex EIA-485. EIA-232 interface: simplified (TXD, RXD, GND), 115.200baud max, EIA-485 interface: Fast slew rate (default). Connection: from SoC UARTs, without hardware flow control, to transceivers and then to front RJ11 connector and rear P2.	COM1A COM2A	COM1B COM2B
HDMI port	HDMI (DVI) interface without audio. Connection: from SoC PCI Express gen2 interface PCIE[3] to SM750 graphic controller and front HDMI connector.	HDMIA	HDMIB

DEVICE OR FUNCTION	DESCRIPTION	SIDE A	SIDE B
LEDs	5 LEDs (Red/Green/Orange) reporting the board health status and activity. Handled by CPLD.	LEDs A1 to A5	LEDs B1 to B5
Reset	Reset push button. Handled by CPLD.	RA	RB
VPX BACKPLANE			
Slot profile	VITA 65 Payload Slot Profile SLT6-PAY-2F2U2T-10.2.5	-	-
PCI Express gen3 port	Optional PCI Express 3.0 link, configurable as 1 x8, 2 x4, or 4 x2. Non-transparent capability. Connection: from SoC PCI Express gen3 interface PE1[7:0] to PCI Express switch PEX8725 and P1.	PCIEG3 / P1 Shared by both SoCA and SoCB	
PCI Express gen2 port	Provisional PCI Express 2.0 link, fixed x1 configuration. Connection: from SoCA PCI Express gen2 interface PCIE[8] to P2.	PCIE1A / P2	-
10 GbE ports	Dual 10G Ethernet controller integrated in SoC. Protocol: 10GBASE-KR or 1000BASE-KX. Connection: from SoC interface LAN0 and LAN1 to P1 and P4.	ETH0A / P1 ETH1A / P1	ETH0B / P4 ETH1B / P4
SATA ports	SATA III, 6 Gb/s links. Connection: from SoC SATA interfaces SATA[0], SATA[1], SATA[2] to P1 and P2.	SATA0A / P1 SATA1A / P1 SATA2A / P2	SATA0B / P2
1000BASE-T port	Intel i210IT controller. 10/100/1000BASE-T protocol with Auto-Negotiation. Auto-wire switching for crossed cables (Auto-MDI/X). Connection: from SoC PCI Express gen3 interface PE1[12] (a PCI Express gen3 interface but used as PCI Express gen1 x1) to i210 controller, to LAN switch, magnetics and P1 or P2.	ETH2A / P1	ETH2B / P2
1000BASE-KX port	Intel i210IS controller. 1000BASE-KX protocol. Connection: from SoC PCI Express gen3 interface PE1[8] (a PCI Express gen3 interface but used as PCI Express gen1 x1) to i210 controller, to SerDes switch. From SerDes switch, routed either to P4 or to the other SoC. Provision: ports ETH3A, ETH3B may be converted to 1000BASE-T.	ETH3A / P4 or SoCB	ETH3B / P4 or SoCA
USB3.0 port	One USB Super Speed 3.0. Connection: from SoCA USB 3.0 interface USB3[1] to P1.	USBSSA / P1	-
USB 2.0 ports	Two USB 2.0 ports for each SoC. Connection: from SoC USB 2.0 interface USB2[0] and USB2[1] to P1 and P2.	USB0A / P1 USB1A / P2	USB0B / P1 USB1B / P2
GPIOs and GDISCRETE1	Five GPIOs shared by CPLDA/B : GPIO1, GPIO2/MaskableReset*, GPIO3, GPIO4, GPIO5. OpenVPX GDISCRETE1.	Shared by both CPLDA and CPLDB	
Serial	Two EIA-232 or one EIA-485 interfaces. Connection: from SoC UARTs, without hardware flow control, to transceiver, front RJ11 connector and rear P2.	COM1A / P2 COM2A / P2	COM1B / P2 COM2B / P2
XMC I/O	If optional XMC is equiped: - XMC I/Os: VITA 46.9 X12d+X8d+X38s from J16 to P3/P4. - or PMC I/Os: P64s from J14 to P3.	X12d+X8d+X38s on P3/P4 or P64s on P3	
Supervisory functions	- Open VPX MaskableReset* - Non maskable RESET. - NVMRO. - Master/Slave SMBus interfaces for system management. - Compatible with Kontron CMB (Monitoring Board), temperature and voltage sensors on the board. - For PCI Express common reference clock feature, please contact Kontron.	Shared by both sides A and B	
Power Supplies	On P0: VS1=12V; VS2 not used; VS3=5V not used; 3.3V_AUX optional, -12V_AUX for XMC slot option only.	Shared by both sides A and B.	
SOFTWARE			
UEFI	UEFI BIOS from AMI		
PBIT	Kontron PBIT test suite.		
OS support	Please contact Kontron.		

DEVICE OR FUNCTION	DESCRIPTION	SIDE A	SIDE B
FORM FACTOR			
VITA 48.1 type	Type 2.		
Board outline	As per IEEE 1101.1 6U outline: Dimensions: 233.35 mm max x 170.60 mm max.		
Front panel	5HP - 1 inch.		
Overall envelope dimensions	As per VITA 48.1 / 1-inch plug-in units: Plug-in unit thickness: 24.94 mm max. Primary side of PCB to outside of heatsink: 16.76 mm max. Primary side of PCB to outside of bottom cover: 7.87 mm max.		

2.7 Environmental Specifications

Table 6: Environmental Specifications

	SA - STANDARD COMMERCIAL	RUGGED AIR-COOLED
Conformal Coating	Optional	Standard
Airflow (1)	25 CFM @41W per SoC 30 CFM @45W per SoC	25 CFM @41W per SoC 30 CFM @45W per SoC
Cooling Method	Convection	Convection
Operating	0°C to +55°C	-25°C to +55°C
Storage (2)	-40°C to 85°C	-40°C to 85°C
Vibration Sine (Operating)	5 Hz to 500 Hz: 2 g	4 Hz: 6 m/s^2 8 Hz: 25 m/s^2 12-33 Hz: 10 m/s^2
Random (Operating)	5 Hz to 500 Hz: 0.04 g^2/Hz	5 Hz to 30 Hz: 10 g^2/Hz 30 Hz to 100 Hz: 1 g^2/Hz 100 Hz to 500 Hz: 0.01 g^2/Hz
Shock (Operating)	20 g, 11 ms, half-sine	20 g, 18 ms, half-sine
Altitude (Operating)	-1 500 ft to 60 000 ft	-1 500 ft to 60 000 ft
Relative Humidity	90% non-condensing (95% with coating option)	95% non-condensing

(1) These figures apply to VX6090 at E.C. Level xxxxxE1 minimum.

(2) The battery temperature range is -30°C to +70°C.

2.8 Board Weight

Table 7: Board Weight

	SA - STANDARD COMMERCIAL	RUGGED AIR-COOLED	NOTE
Weight	1300g	1300g	No Mezzanine

2.9 MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

Table 8: VX6090 MTBF Data

MTBF	MILHDBK217F						IEC62380
	GB (HOURS)		NS (HOURS)		ARW (HOURS)	AIC (HOURS)	Typical Railway Mission Profile
	25°C	40°C	25°C	40°C	55°C	40°C	
VX6090	126 365	107 377	68 352	61 647	17 619	61 647	TBD

3 / Installation

The VX6090 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

3.1 Safety Requirements

The following safety precautions must be observed when installing or operating the VX6090. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Special care shall be taken while handling the board: the heat sink can get very hot during operation. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container before the board and heat sink have cooled down to room temperature.

This board contains electrostatically sensitive devices. Please observe the necessary precautions to avoid damage to your board:

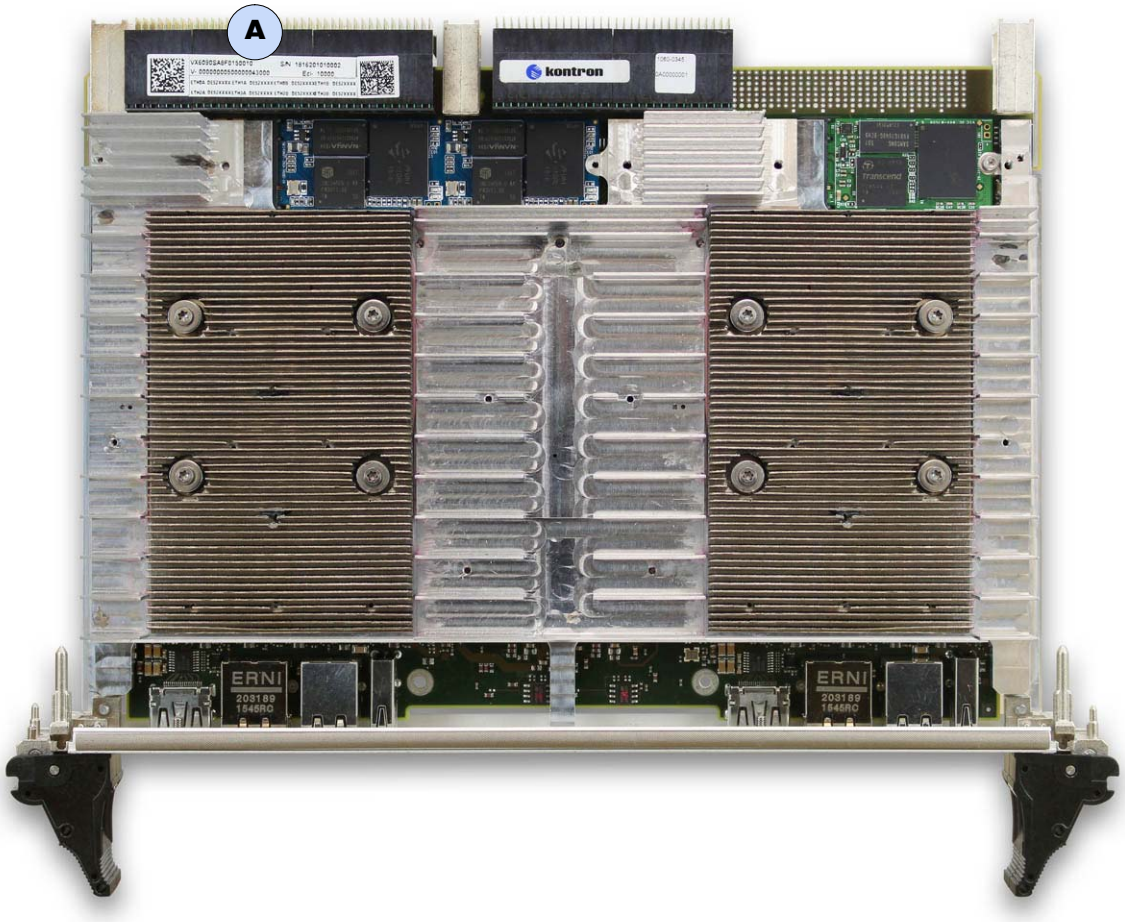
- Discharge your clothing before touching the assembly. Tools must be discharged before use.
- Do not touch components, connector pins or traces.
- We strongly recommend our customers to work in an environment equipped with anti-static workbenches with professional discharging equipments.

3.2 Board Identification

The VX6090 boards are identified by labels fitted to the top side of the board.

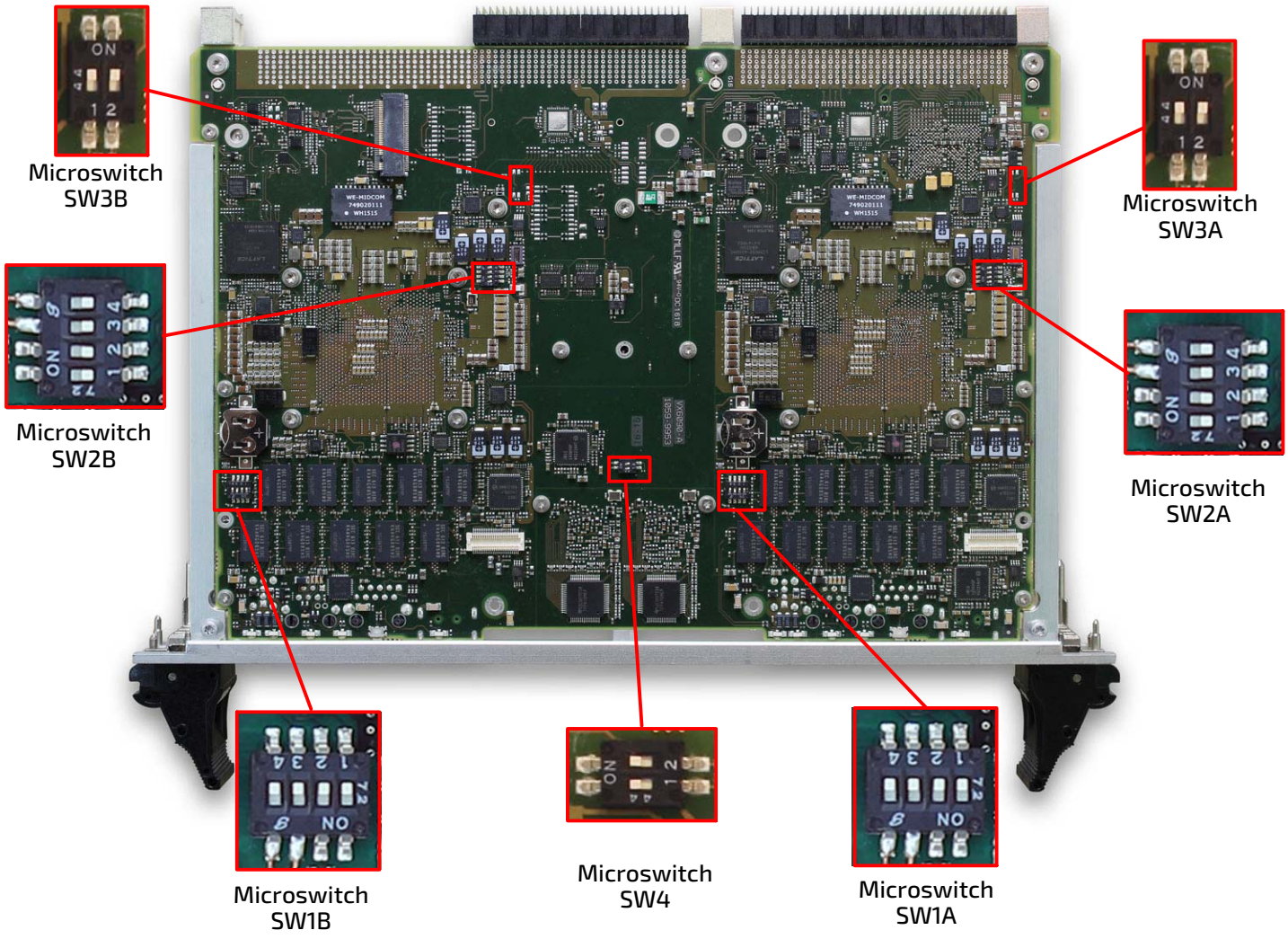
Figure 8: VX6090 Identification (Top Side)

A "Identification" label: Order Code, Serial Number, Variant, E.C. Level, Ethernet MAC addresses



3.3 Board Configuration

Figure 9: VX6090 Board Configuration - Microswitches (Bottom view)



Seven microswitches are available on the VX6090:

- Side A: SW1A, SW2A, SW3A,
- Side B: SW1B, SW2B, SW3B,
- SW4 shared by sides A and B.

3.3.1 Microswitches SW1A and SW1B Description

SW1A and SW1B are located on the bottom side of the board and associated to sides A and B respectively.

Table 9: Microswitches SW1A and SW1B

FUNCTION	DESCRIPTION
1 - Factory Test Mode	off: Normal mode on: Factory mode
2 - Debug Mode	off: Normal mode on: Debug mode
3 - Write Protection of EEPROMs: DDR4 SPD, VPD, i210IS, i210IT	off Write-protected. on: Writes allowed
4 - Write Protection of EEPROMs: BIOS SPI Flash (Main), BIOS SPI Flash (Rescue), FRAM, 10GbE EEPROM	off: Writes allowed on: Write-protected

See section 4.8 page 38 for a detailed description of the EEPROM and Flash devices protection.

3.3.2 Microswitches SW2A and SW2B Description

SW2A and SW2B are located on the bottom side of the board and associated to sides A and B respectively.

Table 10: Microswitches SW2A and SW2B

FUNCTION	DESCRIPTION
1 - System Boot Flash	off: Normal mode on: Rescue mode
2 - BIOS Failsafe	off: Normal mode on: BIOS FAILSAFE mode
3 - PCI Express Switch FAILSAFE Mode (1)	off: Normal mode on: PCI Express Switch allowed
4 - Force PROCHOT	off: Normal mode on: SoC PROCHOT forced to low state; the processor core frequency is set to its lowest value.

(1) Available in side A only. In side B, this microswitch is a spare.

3.3.3 Microswitches SW3A and SW3B Description

SW3A and SW3B are located on the bottom side of the board and associated to sides A and B respectively.

Table 11: Microswitches SW3A and SW3B

FUNCTION	DESCRIPTION
1 - Reserved	Reserved
2 - Reserved	Reserved

3.3.4 Microswitch SW4 Description

SW4 is located on the bottom side of the board and shared by sides A and B.

Table 12: Microswitch SW4

FUNCTION	DESCRIPTION
1- VBIOS Write Protection (SM750 EEPROM device), side A	off: Write-protected on: Writes allowed
2 - VBIOS Write Protection (SM750 EEPROM device), side B	off: Write-protected on: Writes allowed

3.4 Package Content

The packing contents of the VX6090 Series may vary with the ordered board version. See section 2.3 - Ordering Information page 9.

3.5 Initial Installation Procedures

The following procedures are applicable only for the initial installation of the VX6090 in a system. Procedures for standard removal operations are found in their respective chapters.

To perform an initial installation of the VX6090 in a system proceed as follows:

1. Ensure that the safety requirements indicated in Section 3.1 are observed.

CAUTION: Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the configuration of the VX6090 refer to Chapter 5. For the installation of VX6090 specific peripheral devices and Rear I/O devices refer to the appropriate sections in current Chapter.

CAUTION: Care must be taken when applying the procedures below to ensure that neither the VX6090 nor other system boards are physically damaged by the application of these procedures.

3. To install the VX6090 perform the following:
    1. Ensure that no power is applied to the system before proceeding.

CAUTION: When performing the next step, DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors.

    2. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.
    3. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
    4. Fasten the front panel retaining screws.
    5. Connect all external interfacing cables to the board as required.
    6. Ensure that the board and all required interfacing cables are properly secured.

The VX6090 is now ready for operation. For operation of the VX6090, refer to appropriate VX6090 specific software, application, and system documentation.

3.6 Standard Removal Procedure

To remove the board proceed as follows:

1. Ensure that the safety requirements indicated in Section 2.1 are observed. Particular attention must be paid to the warning regarding the heat sink!

CAUTION: Care must be taken when applying the procedures below to ensure that neither the VX6090 nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws.
5. Disengage the board from the backplane by first unlocking the board ejection handles and then by pressing the handles as required until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.

Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

7. Dispose of the board as required.

3.7 Installation of Peripheral Devices

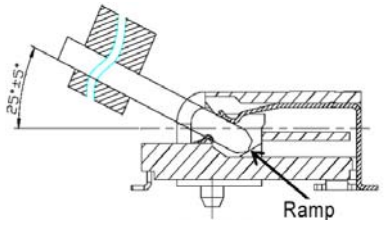
The VX6090 is designed to accommodate a variety of peripheral devices whose installation varies considerably. The following sections provide information regarding installation aspects and detailed procedures.

- Section 3.7.1 page 24 M.2 Module Insertion / Removal Instructions
- Section 3.7.2 page 25 Battery Replacement

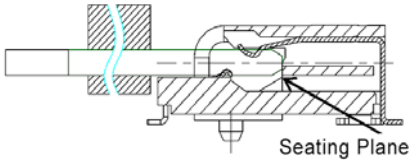
3.7.1 M.2 Module Insertion / Removal Instructions

M.2 Module Insertion Process

Figure 10: M.2 Module Insertion Process



1. Insert the module with angle 25°±5° until module touch HSG ramp.

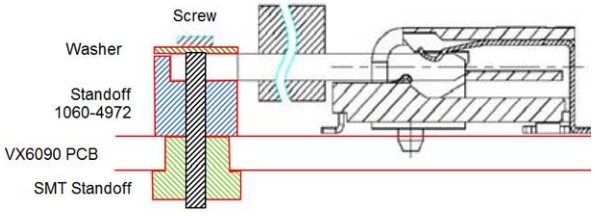


2. Rotate the module to horizon by hand and make sure the card's edge touch HSG seating plane.

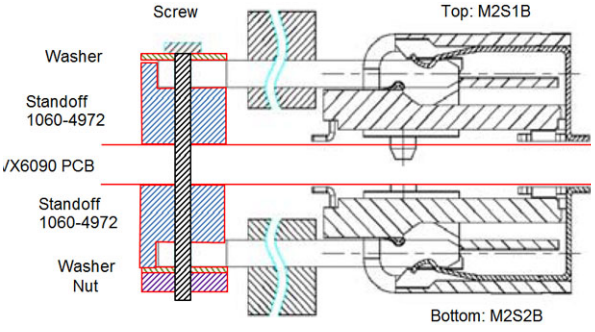
3. Assembly of M.2 module

3.1. Assembly of M.2 module on side A (socket M2S1A, form factors 2242 and 2260): Place stand-off 1060-4972 between module and VX6090 PCB. Add Washer. Add screw.

For form factor 2280 contact Kontron.

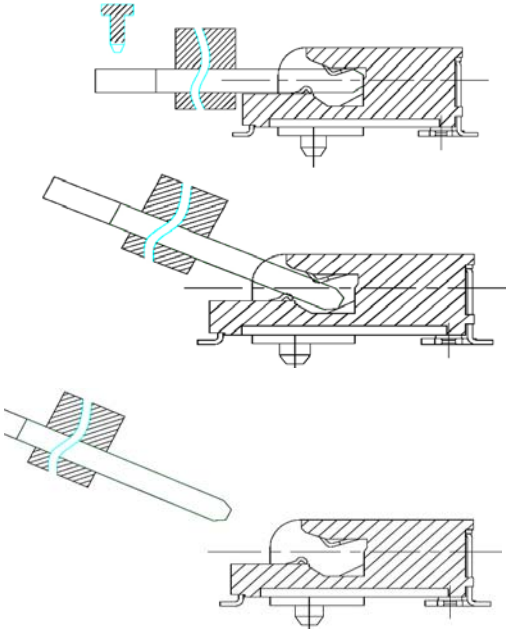


3.2. Assembly of M.2 module on side B (sockets M2S1B and M2S2B): Place stand-offs 1060-4972 between module and VX6090 PCB. Add washers. Add screw and nut.



M.2 Module Removal Process

Figure 11: M.2 Module Removal Process

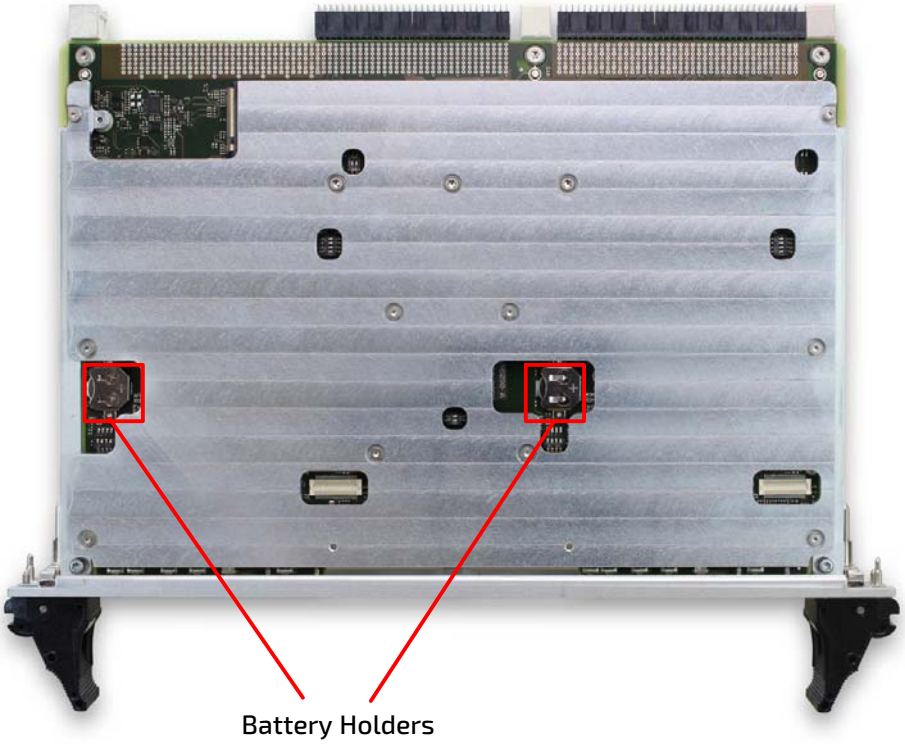


1. Loose the screw by hand and the module will be rotated automatically due to connector contact's counterforce at the same time.

2. Take away the module by hand.

3.7.2 Battery Replacement

Figure 12: Battery Holders Location



To replace the battery, proceed as follows:

- Turn off power.
- Use a thin plastic tool to push the battery out of its holder.

- Remove the battery.
- Place the new battery into the socket.
- Be sure to insert the battery with positive side (+) upwards and negative side (-) closest to printed circuit board.

⚠CAUTION

Danger of explosion when replacing with wrong type of battery. Replace only with the same or equivalent type recommended by the manufacturer. The lithium battery type must be UL recognized.

Do not dispose of lithium batteries in general trash collection. Dispose of the battery according to the local regulations dealing with the disposal of these special materials, (e.g. to the collecting points for dispose of batteries).

Reference of the battery used on the VX6090: RENATA CR1220 MFR (-30/+70°C)

The design of an electronic circuit powered by a component class battery requires the designer to consider two interacting paths that determine a battery's life: consumption of active electrochemical components and thermal wear-out

3.8 Software Installation

The installation of all onboard peripheral drivers is described in detail in the relevant Driver Kit files or Board Support Packages (BSP).

The installation of an operating system is dependent of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.

4 / Additional Board Features

4.1 RTC, Watchdog

4.1.1 Real-Time Clock (RTC)

Two Real Time Clocks (RTC) are available on the VX6090: one is embedded in the PCH of the SoC while the other is a standalone, high-precision, low-power component located on the SoC-SMBus (RV8564 by Micro Crystal). The latter is more precise and is the only one powered when the board is off.

Standby power supplied to the RV8564 RTC

When the VX6090 is powered off, the RTC is powered through Schottky diodes either by the onboard battery or the VPX 3.3V_AUX rail or the VPX VBAT rail.

The maximum current drawn over the -40°C/+85°C temperature range is 500 nA (VBAT= 3 V, no I2C activity) or 550 nA (VBAT=5 V, no I2C activity).

The RTC present in the PCH of the SoC is never powered by the battery.

Internal PCH RTC

The RTC module inside the SoC PCH provides a date and time keeping device with two banks of static RAM with 128 bytes each. The BIOS programs the RTC interrupt on Legacy IRQ8 that is never shared with other interrupts. It is clocked by an external 32.768 kHz oscillator with a parabolic coefficient of 0.4 ppm/°C^2 and a stability of +/-20 ppm at 25°C. A 20 ppm stability is equivalent to a 10 mn/year drift.

Standalone low-power RTC RV8564

The RV8564C2/B RTC by Micro Crystal features an internal oscillator, date and time keeping module with programmable alarm, timer and interrupt functions. It has an ultra low-power consumption in time keeping mode: 250 nA, typical and 500 nA, maximum. Its stability is 20 ppm at 25°C. It is connected to the SoC-SMBus.

RTC management by BIOS and OS

At each startup, the BIOS retrieves the date and time information from the high-precision RV8564 RTC and copies it into the PCH RTC inside the SoC. This is necessary since the PCH RTC is not saved.

Any update of date and time in the BIOS settings will be done both in PCH RTC and RV8564 RTC.

Regarding the RTC management by the OS, the OS should use the high-precision RV8564 RTC driver. Failing to do so, the updates will be done only in PCH RTC and will not be saved.

If no power is applied on the RV8564 RTC, the BIOS displays the BIOS build date and time instead of the current date and time.

Century flag

For compatibility reasons, the BIOS implements the century flag for the high-precision RTC as follows:

- Century Flag C = 0 for 1900-1999 years
- Century Flag C = 1 for 2000-2099 years.

The user should check that the OS driver implements the same convention.

4.1.2 CPLD Watchdog

In addition to the standard watchdog timer included in the integrated PCH, the cPLD implements a hardware watchdog timer that can be used by the operating software to monitor the normal operation of the system.

It is enabled by software, and once enabled must be restarted at regular intervals. If not, its expiration sets off an interrupt (IRQ) to the local processor, a board reset or a board power-cycle.

The watchdog has the following features:

- Timeout programmable from 1 to 511 clock periods, by steps of 2 periods
- Clock periods of 1s or 1ms
- Lock bit: when set, can only refresh (restart) the watchdog, but not change its settings
- Four modes: timer, reset, interrupt or power-cycle
- Restart counter: can manage the remaining number of resets or power-cycles done by the watchdog before giving-up.

4.2 I2C Structure

The I2C structure is detailed in Table 13. See also Figure 3 - Block Diagram page 8.

Table 13: I2C Structure

I2C & SMBUS BUS	VX6090 SIDE A	VX6090 SIDE B
I2C bus SoC-DDRI2: - SPD EEPROM access from SoC	Bus SoC-DDRI2CA (8-bit add.): - Master: SoC (DDR_SDA/SCL) - SPD EEPROM - DDR0 @0xA0 - SPD EEPROM - DDR1 @0xA4	Bus SoC-DDRI2CB (8-bit add.): - Master: SoC (DDR_SDA/SCL) - SPD EEPROM - DDR0 @0xA0 - SPD EEPROM - DDR1 @0xA4
SMBus SoC-SMBUS - Access to various local devices from the SoC. - Three possible speeds: 100 kHz (Standard mode), 357 kHz (Fast mode), 750 kHz (Fast mode plus)	Bus SoC-SMBUSA (8-bit add.): - Master: SoC (SMBDATA/CLK) - Current monitor LTC2945 @0xDC - RTC RV8564CV @0xA2 - no XMC - Retimer @0x30 - Opt: CPLD @0x0E - Opt: Nuvoton NCT7802Y @0x50	Bus SoC-SMBUSB (8-bit add.): - Master: SoC (SMBDATA/CLK) - Current monitor LTC2945 @0xDC - RTC RV8564CV @0xA2 - Opt: XMC @0xA0 - Retimer @0x30 - Opt: CPLD @0x0E - Opt: Nuvoton NCT7802Y @0x50
I2C bus CPLD-I2CLOC - Access to various local devices from the CPLD. - One data but two different clocks: 99.2kHz or 1.04Mhz	Bus CPLD-I2CLOCA @99.2KHz (8-bit add.): - Master: CPLD (I2CLOC_DAT_A / I2CLOC_LS_CLK_A) - VPD EEPROM @0xA0 - OS EEPROM @0xA2 - FRAM @0xA4 0xA6 Bus CPLD-I2CLOCA @1.04MHz (8-bit add.): - Master: CPLD (I2CLOC_DAT_A / I2CLOCHS_CLK_A) - Nuvoton NCT7802Y @0x50 - Debug: SoC LAN_SMBUS	Bus CPLD-I2CLOCB @99.2KHz (8-bit add.): - Master: CPLD (I2CLOC_DAT_B / I2CLOC_LS_CLK_B) - VPD EEPROM @0xA0 - OS EEPROM @0xA2 - FRAM @0xA4 0xA6 Bus CPLD-I2CLOCB @1.04MHz (8-bit add.): - Master: CPLD (I2CLOC_DAT_B / I2CLOCHS_CLK_B) - Nuvoton NCT7802Y @0x50 - Debug: SoC LAN_SMBUS
I2C bus CPLD- I2CPEX - Configuration of PEX8725	Bus CPLD-I2CPEX (8-bit add.) - Master: CPLDA (PLD_PEX_SDA0/SCL0_A) - PEX8725 (I2C_SDA0/SCL0) @0x72	Not available.

I2C & SMBUS BUS	VX6090 SIDE A	VX6090 SIDE B
SMBus CPLD-SMB0 (also called I2C0 or IPMBus) ▸ SMBus on VPX backplane	Bus CPLD-SMB0 (8-bit add.): ▸ Multi-Master: CPLDA & CPLDB (PLDAB_SMB0_DAT/CLK) ▸ P0.w5	
SMBus CPLD-SMB1 (also called I2C1 or SMBus) ▸ SMBus on VPX backplane	Bus CPLD-SMB1 (8-bit add.): ▸ Multi-Master: CPLDA & CPLDB (PLDAB_SMB1_DAT/CLK) ▸ P0.w4	
I2C bus SM750-I2CHDMI ▸ Routed from SM750 to HDMI receptacle for display management.	Bus SM750-I2CHDMIA ▸ Master: SM750 ▸ HDMI receptacle (front panel)	Bus SM750-I2CHDMIB ▸ Master: SM750 ▸ HDMI receptacle (front panel)

4.3 Battery and Supercap

Battery location and replacement

See section 3.7.2 - Battery Replacement page 25.

Battery Life

Since the capacity of CR1220 MFR by Renata is 40 mAh, and the current drawn by RTC RV8564C2 is 500 nA, the expected battery life is 8 years in the absence of external power.

Supercap

Supercap and battery are mutually exclusive.

For supercap solutions, contact Kontron.

4.4 cPLD Features

4.4.1 Overview

The CPLD handles:

- Power-on/off management
- Onboard voltage regulators sequencing and monitoring
- Reset management
- LPC interface to processor
- I2C interface to rear SMBus (CPLD-SMB0 and CPLD-SMB1 on VPX P0)
- I2C interface to serial VPD EEPROM, OS EEPROM and F-RAM device (PLD-I2CLOC @ 1.04 MHz)
- I2C interface to Nuvoton monitor device NCT7802Y (CPLD-I2CLOC @ 99.2 KHz)
- Front LEDs for board status display
- Serial lines configuration (EIA-232 vs EIA-422/585)
- SerDes switch (Etherne ETH3 routed to P4 or to other SoC)
- GPIOs and GDISCRETE1
- Internal registers, board configuration (switches) and system management

The CPLD registers can be accessed by the processor on the LPC bus at I/O address 0x800+offset. The I2C registers 0x72 to 0x78 in the CPLD - which are described in the next section - can also be accessed from any master of the I2C bus CPLD-SMB0 with register offset 0 to 6.

For a detailed description of other CPLD registers, please contact Kontron.

4.4.2 CPLD I2C Registers

I2C0 and I2C1 interfaces:

The two CPLD I2C interfaces I2C0 and I2C1 are connected to VPX SMBus CPLD-SMB0 (P0 wafer 5) and CPLD-SMB1 (P0 wafer 4). See detailed Block Diagram (Figure 3 page 8).

I2C0 is a master/slave interface while I2C1 is a master-only interface.

I2C0 and I2C1 master interface:

For information about how to handle the master interface of I2C0 and I2C1 in the BSP, contact Kontron.

I2C0 slave interface:

The I2C0 slave register base address depends on the VPX slot ID (geographical address of the slot):

VPX Slot 1 (SYSCON): slave I2C0 base address is 0x18 (I2C 7-bit addressing)

VPX Slot 2: slave I2C0 base address is 0x19 (I2C 7-bit addressing)

VPX Slot 3: slave I2C0 base address is 0x1A (I2C 7-bit addressing)

etc.

On VX6090, both CPLDs share the same slave I2C0 base address. To avoid erroneous addressing and bus contention, CPLDA will respond to address range 0x00 to 0x0F and CPLDB to 0x10 to 0x1F. Outside the correct address range, writes are discarded and reads are responded to with 0xFF data (which has no electrical effect on an open-collector I2C data).

I2C Registers Overview

Table 14: I2C Registers of CPLD

OFFSET	NAME	PURPOSE	ACCESS
0x72	I2C_BOARD_STATUS	Board state (from I2C)	RW
0x73	I2C_BOARD_CONTROL	Board state and control (from I2C)	RW
0x74	I2C_ERROR_STATUS	Board error state (from I2C)	RW
0x75	I2C_PORT80	PORT80 value (from I2C)	RW
0x76	I2C_FAILCODE	PEX8725 EEPROM CRC error status (from I2C)	RW
0x77	I2C_SCRATCHPAD	Not yet defined	RW
0x78	I2C_MISC	Miscellaneous board information (from I2C)	RW

I2C_BOARD_STATUS : This Register can be accessed from I2C0 Slave interface :

- I2C_SLAVE_ADDR = 7'b0010_111 + GA
- Register offset (1 byte) = 0

Bits meaning during read access is controlled by bit 3 of register @73.

Table 15: I2C_BOARD_STATUS @0x72

I2C_BOARD_STATUS @0x72 Can also be accessed from I2C0 slave interface with register offset 0 (or 0x10)				
BIT#	**NAME**	**DESCRIPTION**	**RESET**	**TYPE**
7	Power Status	Power Status (used by CMB board to read power status) 0: Power Stand By 1: Power ON (PWROK_STATE State just before S0	0	RO
6-5	Reset Origin	Origin of Last Reset Detected 00 Internal PSUs power-on 01 CPLD Watchdog expired 10 SYSRESET# (from VPX) 11 Other Reset sources : - Front Reset Push Button - MaskableReset*/GPIO2* - Soft Reset (bit 1 register @73) - Cross Reset from the other CPLD - SoC Soft Reset (through register CF9h)	0	RO
4	Reset Status	Reset Status Side A 0: PCH_PWROK not asserted OR Reset (* see below) asserted 1: PCH_PWROK asserted AND Reset not asserted *Sources of Reset are : - Front Reset Push Button - MaskableReset*/GPIO2 - Soft Reset (bit 1 register @73) - Cross Reset from the other CPLD - CPLD Watchdog	0	RO
3-0	Boot Status	Boot Status 0x00: RESET : default hardware value 0x01: BIOS-BOOT : written by BIOS 0x02: BIOS : written by BIOS 0x03: PBIT : written by BIOS 0x04: OS-BOOT : written by BIOS 0x05: OS-RUNNING : to be written by OS at the end of boot 0x06: COMPLETED: to be written by the final application when running 0x07: SHUTDOWN: to be written by OS when issuing a halt/shutdown 0x08: REBOOT: to be written by OS when rebooting 0x09 - 0x0B: Reserved 0x0C - 0x0F: Customer defined These bits are Read Only through I2C Slave Interface and R/W through LPC Interface. The boot status is also reset at each board reset.	0	RW

I2C_BOARD_CONTROL: This Register can be accessed from I2C0 Slave interface

- I2C_SLAVE_ADDR = 7'b0010_111 + GA
- Register offset (1 byte) = 1

Table 16: I2C_BOARD_CONTROL @0x73

I2C_BOARD_CONTROL @0x73 Can also be accessed from I2C0 slave interface with register offset 0x01 (CPLD A), 0x11 (CPLD B)				
BIT#	**NAME**	**DESCRIPTION**	**RESET**	**TYPE**
7-4	Board Id	Board Identification 0001 VX6080 0010 VX6070 0011 VX3030 0100 VM6052/VM6054 0101 VM6050 0110 VX6060 0111 VX3035 1000 VX3040 family (VX3042/VX3044) 1001 VX305x family (VX3052/VX3058) 1010 VX6090 family 1111 Reserved for non-SBC boards (switches, ...)	N.A.	RO
3	Reserved	RESERVED	0	RW
2	Cross_Reset	Cross Reset between Side A and Side B– (Only for VX6090) 0: No reset 1: Reset asserted on the other side	0	RW
1	Reset	0: No Reset 1: Reset Assert (side A forVX6090)	0	RW
0	Power_OnOff	Power On/Off Control 0: Power Off (StandBy Mode) 1: Power On This bit can be used to do a Power OFF or control the Power-On sequence when Standby Power is applied. The default value is loaded when standby is applied from inverted SYSTEM EEPROM offset 0x100 bit 1, if FACTORY mode is not enabled WARNING: Setting this bit to 0 asserts VPX reset (SYSRESET_OUT#) if register 0x70 bit 0 (LOC2VPX) is set to 0.	*.	RW

Table 17: I2C_ERROR_STATUS @0x74

I2C_ERROR_STATUS @0x74 Can also be accessed from I2C0 slave interface with register offset 0x02 (CPLD A), 0x12 (CPLD B)				
BIT#	NAME	DESCRIPTION	RESET	TYPE
7	Alert	Alert 0: no alert 1: alert pending from PLD_PECI_ALERT# or PLD_PCHHOT_CPU# See register ALERT_STATUS@5B bit 0 and 3 for current state on these signals See register SERIRQ_CONTROL@0xF bit 6 and 2 for interrupt Mask and Status	0	RO
6	POST_Error	POST Error 0: no error 1: error This bit is set when PBIT has been run with errors (according to reg 0x2) Also set when RTC battery is low (according to reg 0x3 bit 0)	0	RO
5	POST RTC	POST RTC 0: POST OK 1: POST FAILED (weak or missing battery) This bit is a copy of reg 0x3 bit 0 (POST_RTC), that is set when RTC battery is low	0	RO
4-0	Error_Code	Error Code (CMB Compatibility Mode) 0x10 VPXPWRGD_UV 0x11 VPXPWRGD_OV 0x0C PECI_CRIT# 0x0D VRVCCIN_VRHOT# Or VR1V05_VRHOT 0x0E THERMTRIP# 0x0F CATERR# 0x1F "Onboard PSUs Error" Other: Reserved When an unmasked fatal alert occurs, this register is updated, all internal PSUs are switched off and the error status is also reported on the front panel LEDs. See Also registers @7A and @7B	0	RO

Table 18: I2C_PORT80 @ 0x75

I2C_PORT80 @ 0x75 Can also be accessed from I2C0 slave interface with register offset 0x03 (CPLD A), 0x13 (CPLD B)				
BIT#	NAME	DESCRIPTION	RESET	TYPE
7-0	Port_80	Port 80 value The value of this register is automatically updated at each write access to port 0x80 (write snooping). It is cleared at each reset.	0	RW (LPC) RO (I2C)

Table 19: I2C_FAILCODE @ 0x76

I2C_FAILCODE @ 0x76 Can also be accessed from I2C0 slave interface with register offset 0x04 (CPLD A), 0x14 (CPLD B)				
BIT#	NAME	DESCRIPTION	RESET	TYPE
7-1	Reserved	RESERVED	0	RW (LPC) RO (I2C)
0	PEX_EEPROM_ CRC_ERROR	PEX EEPROM CRC error 0: no error 1: error This bit is set by BIOS when a CRC error is detected on the PEX EEPROM	0	RW(LPC) RO (I2C)

Table 20: I2C_SCRATCHPAD @ 0x77

I2C_SCRATCHPAD @ 0x77 Can also be accessed from I2C0 slave interface with register offset 0x05 (CPLD A), 0x15 (CPLD B)				
BIT#	NAME	DESCRIPTION	RESET	TYPE
7-0	Scratchpad	Scratchpad register The purpose of this register is not defined	0	RW

Table 21: I2C_MISC @ 0x78

I2C_MISC @ 0x78 Can also be accessed from I2C0 slave interface with register offset 0x06 (CPLD A), 0x16 (CPLD B)				
BIT#	NAME	DESCRIPTION	RESET	TYPE
7	Force_rescue	Force Rescue Mode for System Flash Boot. 0: not forced (default) 1: forced Changing this bit will take effect at next board reset (LPC reset) and override the Switch configuration. Register @09 bit 7 indicates the current Flash selected.	0	RW
6	Force_EFI_Shell	Force stop at EFI shell. 0: not forced (default) 1: forced	0	RW
5-3	Power_CUR	Current power profile. This field is updated by the board (BIOS/OS) according to its current power profile (power/TDP budget) 000: power profile unsupported other value: see below	000	RW (LPC) RO (I2C)
2-0	Power_REQ	Requested power profile. This filed is expected to be set by a shelf-manager (such as CMB) or another board, and used by the board (BIOS/OS) to set its power profile: 000: uncontrolled : the board uses its onboard switches and/or BIOS settings to set a power profile 001: low TDP 010: normal TDP 011: high TDP	000	RW

Table 22: POWER ERROR part 1 @ 0x79

POWER ERROR part 1 @ 0x79 (1) Can also be accessed from I2C0 slave interface with register offset 7 (or 0x17)				
BIT#	NAME	DESCRIPTION	RESET	TYPE
7-0	Power Error Part 1	This register indicates what are the Power rails failed when a power error is detected (see also register @07A) Bit 7: VPXPWRGD_UV_n or VPXPWRGD_OV_ Bit 6: VR5V0 Bit 5: VCCSCFUSESUS Bit 4: VCCKRHV Bit 3: VR1V05 Bit 2: VR2V5_DDR4 Bit 1: VR1V2 Bit 0: VTT An error is reported if at least one PSU does not start within the expected delay (timeout) or fails after being OK. This register is cleared by switching the board off (standby) or by removing VPX power	0	RO

(1) This power error mapping applies to VX6090 at E.C. Level 2xxxxxx minimum.

Table 23: POWER ERROR part 2 @ 0x7A

POWER ERROR part 2 @ 0x7A (1) Can also be accessed from I2C0 slave interface with register offset 8 (or 0x18)				
BIT#	NAME	DESCRIPTION	RESET	TYPE
7-0	Power Error Part 2	This register indicates what are the Power rails failed when a power error is detected (see also register @079) Bit 7: VR1V5_PCH Bit 6: VRPEX or VR1V8 Bit 5: VR3V3 Bit 4: VRVCCIN Bit 3: VR1V8_SERDES Bit 2: VR3V3SUS Bit 1: WAKEUP Error Bit 0: Critical_Alert An error is reported if at least one PSU does not start within the expected delay (timeout) or fails after being OK. This register is cleared by switching the board off (standby) or by removing VPX power	0	RO

(1) This power error mapping applies to VX6090 at E.C. Level 2xxxxxx minimum.

4.5 Serial Lines EIA-422/485 Additional Modes

The EIA-232 mode is the default mode for all serial simplified lines. EIA-422/485 mode can be selected through BIOS settings along with an optional onboard 120 Ohm termination and a half-duplex option.

Since the EIA-422/485 protocol is based on diffential pairs, the EIA-422/485 mode can be set for COM1 only as shown in Table 24 (COM2 is no longer available in this mode).

Table 24: Availability of EIA-232 and EIA-422/485 modes on COM serial ports.

MODE	RJ12 FRONT PANEL CONNECTOR	P2 REAR CONNECTOR
EIA-232 (default)	RJ12 side A: COM1A, COM2A RJ12 side B: COM1B, COM2B	P2: COM1A, COM2A, COM1B, COM2B
EIA-422/485 (BIOS setting)	RJ12 side A: COM1A RJ12 side B: COM1B	P2: COM1A, COM1B

For detailed pin assignment of front and rear connectors, please refer to 5.1 (Front Panel Connectors) page 43 and 5.3 (Rear Connectors) page 56.

4.6 GPIOs and GDISCRETE1

4.6.1 GPIOs

The VX6090 features five GPIOs managed by the CPLD. For information about the GPIO driver, contact Kontron.

- Three GPIOs are available on P0 connector: GPIO3, GPIO4 and GPIO5. See section 5.3.1 page 56 for detailed pinout.
- Two GPIOs are available on P1 connector: GPIO1 and GPIO2. GPIO2 shares its VPX P1 pin with the OpenVPX MaskableReset* signal. See section 5.3.2 page 58 for detailed pinout.

The GPIOs share the same interrupt in the CPLD.

4.6.2 GDISCRETE1

GDISCRETE1 is a bussed open-collector GPIO defined by OpenVPX VITA 65 and available on P1. See section 5.3.2 page 58 for detailed pinout.

It is handled by the CPLD and buffered by a SN74LVC1G125 wired as an Open Collector to meet the electrical characteristics defined in VITA 65.

It has a dedicated interrupt in the CPLD.

4.7 Reset

In addition to the initial Reset generated during the power-up sequence, several Reset sources are defined and shown in Table 25. Except for the last two sources (Processor Watchdog Reset and SoC Soft Reset) all these sources are managed by the CPLD. To generate a reset, the CPLD activates the SoC input SYS_RESET_N. This leads to the activation by the SoC of the platform reset signal PLTRST_N.

Table 25: Reset Sources Description

RESET SOURCE	TYPE OF RESET	SIDE INVOLVED (MASK)	RESET STATUS	NOTE
Front panel reset push button	Platform Reset	1 side (A or B) (not maskable)	CPLD register @0x72 accessed from local LPC bus or from rear SMBus CPLD-SMB0	See reset propagation options and masks in CPLD registers.
Activation of VPX SYSRESET* (P0-B4)	Platform Reset	2 sides simultaneously (unless masked)		See VPX VITA 46.0 standard. Reset propagation options and masks available in CPLD registers.
Activation of VPX MaskableReset* (P1-G15)	Platform Reset	2 sides simultaneously (unless masked)		See Open VPX standard VITA 65. MaskableReset* shares pin P1-G15 with GPIO2.
Rear SMBus soft reset (write to CPLD register @0x73 bit 1 from rear SMBus CPLD-SMB0)	Platform Reset	1 side (A or B)		Base address on rear SMBus depends on Board slot number (VPX Geographical Address)
CPLD soft reset (write to CPLD registrer @0x73 bit 1 from local processor via LPC bus)	Platform Reset	1 side (A or B)		See register definition in this user's guide
CPLD watchdog reset	Platform Reset	1 side (A or B) (unless masked)		See software release notes
CPLD cross reset	Platform Reset	1 side (A or B) (unless masked)		
Processor watchdog reset	Platform Reset	1 side (A or B)	Intel Xeon D-15xx watchdog status registers	See Intel Xeon D-15xx watchdog control registers
SoC soft reset (write to SoC Reset Control register CF9h)	Platform Reset	1 side (A or B)	Intel Xeon D-15xx watchdog status registers	

4.8 EEPROMs and Flash Devices Write Protection

4.8.1 EEPROMs and Flash Devices Summary

There are four types of write-protection which define four groups of EEPROMs: SYS, USER, VPD and SM750.

These groups are detailed in Table 26.

Table 26: EEPROM and Flash Devices Summary

GROUP	NAME AND SIDE	DESCRIPTION	FUNCTION	ACCESS	DEVICE WP PIN DEFINITIONCE	WP SIGNAL READ BACK IN CPLD	RELATED SWITCH
SYS	OS EEPROM Sides A & B	I2C 256Kbit EEPROM	EEPROM used by PBITs	I2C bus CPLD-I2CLOC	0: W enabled 1: W disabled	CPLD 0x7E[1]	-
	PEX8725 SideA	256Kbit SPI Flash	PEX8725 EEPROM	I2C bus CPLD-I2CPEX	0: W disabled 1: W enabled	CPLD 0x7D[6]	-
	XMC Side B	XMC EEPROM	XMC EEPROM	SMBus Soc-SMBUS	0: W enabled 1: W disabled	CPLD 0x7D[7]	-
USER	Boot Main Sides A & B	128Mbit SPI Flash	BIOS Boot Flash (Main)	SoC SPI0 interface	0: W disabled 1: W enabled	CPLD 0x7D[1]	SW1A[4] SW1B[4]
	Boot Rescue Sides A & B	128Mbit SPI Flash	BIOS Boot Flash (Rescue)	SoC SPI1 interface	0: W disabled 1: W enabled	CPLD 0x7E[0]	SW1A[4] SW1B[4]
	FRAM Sides A & B	1Mbit FRAM	FRAM	I2C bus CPLD-I2CLOC	0: W enabled 1: W disabled	CPLD 0x7D[2]	SW1A[4] SW1B[4]
	10GbE Sides A & B	32Mbit SPI Flash	10GBASE-KR LAN 0/1	SoC SPI_LAN interface	0: W disabled 1: W enabled	CPLD 0x7D[0]	SW1A[4] SW1B[4]
VPD	SPDs Sides A & B	I2C 4Kbit EEPROM	DDR Bank 0 SPD DDR Bank 1 SPD	I2C bus SoC-DDRI2C	0: W enabled 1: W disabled	CPLD 0x7D[4]	SW1A[3] SW1B[3]
	VPD Sides A & B	I2C 256Kbit EEPROM	System (VPD) EEPROM	I2C bus CPLD-I2CLOC	0: W enabled 1: W disabled	CPLD 0x7D[5]	SW1A[3] SW1B[3]
	i210IT Sides A & B	8Mbit SPI Flash	i210IT 1000BASE-T	Through i210 device	0: W disabled 1: W enabled	CPLD 0x7D[3]	SW1A[3] SW1B[3]
	i210IS Sides A & B	8Mbit SPI Flash	i210IS 1000BASE-KX	Through i210 device	0: W disabled 1: W enabled	CPLD 0x7D[3]	SW1A[3] SW1B[3]
SM750	SM750 Side A	256Kbit SPI Flash	VBIOS of SM750 A	Through SM750 device	0: W disabled 1: W enabled	CPLD 0x7E[2] (1)	SW4[1]
	SM750 Side B	256Kbit SPI Flash	VBIOS of SM750 B	Through SM750 device	0: W disabled 1: W enabled	CPLD 0x7E[3] (1)	SW4[2]

(1) Switches SW4[1] & SW4[2] are not routed to CPLD and the state of the WP signal read back from CPLD reflects only NVMRO.

4.8.2 Write Protection SYS_WP

- **Description:**
  This type of protection applies to the SYS group of EEPROMs and SPI Flash devices.

  The priority defined from highest to lowest is:

  - NVMRO high (provided that the factory mode switch SW1[1] is OFF),
  - CPLD bit @0x09-Bit2 high.

- **Equation:**
  Device protected when:
  (NVMRO=1 & SW1[1]=OFF) | (NVMRO=0 & @0x09-Bit2=1)
- **Truth table:**

NVMRO	SW1[1]	CPLD @0X09-BIT2	PROTECTION
1	OFF	X	YES
1	ON	0	NO
1	ON	1	YES
0	X	0	NO
0	X	1	YES

X ="don't care"

4.8.3 Write Protection USER_WP

- **Description:**
  This type of protection applies to the USER group of SPI Flash and FRAM devices. The priority defined from highest to lowest is:
  - NVMRO high (provided that the factory mode switch SW1[1] is OFF),
  - switch SW1[4] ON, CPLD bit @0x09-Bit3 high.
- **Equation:**
  Device protected when:
  (NVMRO=1 & SW1[1]=OFF) | (NVMRO=0 & SW1[4]=ON) | (NVMRO=0 & SW1[4]=OFF & @0x09-Bit3=1)
- **Truth table:**

NVMRO	SW1[1]	SW1[4]	CPLD @0X09-BIT3	PROTECTION
1	OFF	X	X	YES
1	ON	ON	X	YES
1	ON	OFF	0	NO
1	ON	OFF	1	YES
0	X	ON	X	YES
0	X	OFF	0	NO
0	X	OFF	1	YES

X ="don't care"

4.8.4 Write Protection VPD_WP

- **Description:**
  This type of protection applies to the VPD group of EEPROMs and SPI Flash devices. The protection is disabled when SW1[3] is ON. When SW1[3] is OFF, the priority defined from highest to lowest is:
  - NVMRO high (provided that the factory mode switch SW1[1] is OFF),
  - CPLD bit @0x09-Bit1 high.

- **Equation:**
  Device protected when:

SW1[3]=OFF & ((NVMRO=1 & SW1[1]=OFF) | (NVMRO=0 & @0x09-Bit1=1))

- **Truth table:**

SW1[3]	NVMRO	SW1[1]	CPLD @0X09-BIT1	PROTECTION
ON	X	X	X	NO
OFF	1	OFF	X	YES
OFF	1	ON	0	NO
OFF	1	ON	1	YES
OFF	0	X	0	NO
OFF	0	X	1	YES

X="don't care"

4.8.5 Write Protection SM750_WP

- **Description:**

  This type of protection applies to the SM750 group of SPI Flash devices.

  SW4[1] is dedicated to SM750 side A and SW4[2] is dedicated to SM750 side B.

  The priority defined from highest to lowest is:

  - SW4[1] or SW4[2] low,
  - NVMRO high (provided that the factory mode switch SW1[1] is OFF).
- **Equation:**

  Device protected when

  SW1[3]=OFF & ((NVMRO=1 & SW1[1]=OFF) | (NVMRO=0 & @0x09-Bit1=1))
- **Truth table:**

SW4[1]	NVMRO	SW1[1]	CPLD @0X09-BIT1	PROTECTION
ON	X	X	X	NO
OFF	1	OFF	X	YES
OFF	1	ON	0	NO
OFF	1	ON	1	YES
OFF	0	X	0	NO
OFF	0	X	1	YES

X="don't care"

4.9 M.2 Modules

4.9.1 Write-protect of SSD M.2 Modules

All the Flash and non volatile memories onboard have a write protect mechanism taking into account the NVMRO (Non Volatile Memory Read Only) VPX signal. See section 4.8 page 38 for detailed information.

4.9.2 M.2 Modules on Top Side (M2S1A, M2S1B)

Form factors

The M2S1A socket on side A can host the following form factors: 2242-D5-M, 2260-D5-M, 2280-D5-M.

The M2S1B socket on side B can host 2242-D5-M modules.

The default protocol is SATA III, for PCI Express interface contact Kontron.

Stacking Height of Top Side M.2 Sockets

The PCI Express M.2 specification defines H4.2-D5 modules with a 1.5 mm maximum bottom-side component height.

The stacking height of the M.2 connector soldered on VX6090 is 2.48 +/- 0.20 mm.

The maximum component height on VX6090 is 0.5 mm.

The clearance between components of the VX6090 and M.2 module is 0.28 mm minimum.

For a safe assembly of the module, make sure that:

- The selected M.2 module complies to the 1.5 mm maximum bottom-side component height.
- The standoff provided by Kontron is used for the M.2 module assembly.

Failing to respect these requirements could lead to permanent damage to the board and/or the M.2 card.

M.2 Module List for M2S1A and M2S1B

Table 27 lists some of the SATA SSD M.2 modules tested on VX6090.

Table 27: Non-exhaustive M.2 module list, tested on VX6090 M.2 slots

MODULE	CAPACITY	MODULE TYPE	MEMORY TECHNOLOGY	TEMPERATURE GRADE	FITS ON SLOT
Virtium VSFBM4XI030G-150	30 GB	2242	iMLC	-40/+85°C	M2S1A M2S1B
Transcend TS32GMTS400	32 GB	2242	MLC	0/+70°C	M2S1A M2S1B
Swissbit SFSA030GM1AA1TO-I-LB216-STD	30 GB	2242	MLC	-40/+85°C	M2S1A M2S1B

4.9.3 M.2 Module on Bottom Side (M2S2B)

Form factors

The M2S2B socket on side B hosts 2242-D4-M modules.

There is no bottom M.2 socket on side A.

Stacking Height of Bottom Side M.2 Socket

The PCI Express M.2 specification defines H4.2-D4 modules with a 0.7 mm maximum bottom-side component height.

The stacking height of the M.2 connector soldered on VX6090 is 2.48 +/- 0.20 mm.

The maximum component height on VX6090 is 1.1 mm.

The clearance between components of the VX6090 and M.2 module is 0.48 mm minimum.

For a safe assembly of the module, make sure that:

- The selected M.2 module complies to the 0.7 mm maximum bottom-side component height.
- The standoff provided by Kontron is used for the M.2 assembly.

Failing to respect these requirements could lead to permanent damage to the board and/or the M.2 card.

5 / Physical I/O

5.1 Front Panel Connectors

Figure 13: Front Panel Connectors Location

5.1.1 Serial Connector - COM

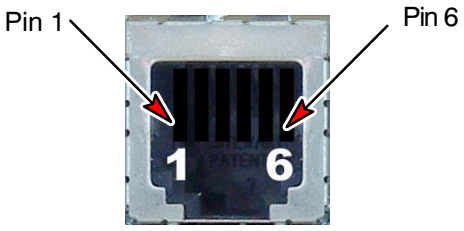
This section describes the two RJ12 front connectors carrying serial ports COM1A, COM2A, COM1B, COM2B.

Front Serial Connector Description

Table 28: Serial Connector Pin Assignment

PIN	SIGNAL
1	COM2 TXD / COM1 TXD-
2	Shell
3	COM1 TXD / COM1 TXD+
4	COM1 RXD / COM1 RXD+
5	GND
6	COM2 RXD / COM1 RXD-

Figure 14: Serial Connector



CAUTION: Serial lines are routed to both front pannel RJ12 connector and rear P2. Plugging a serial device to both connectors will lead to electrical contention. Be sure to use only one connector at a time.

Table 29: Serial Connector Signals Definition

SIGNAL	DIRECTION	DEFINITION
COM1 TXD / COM1 TXD+	Output	EIA-232: Transmit Data of port COM1A/B EIA-485: Transmit Data Plus of port COM1A/B
COM1 RXD / COM1 RXD+	Input	EIA-232: Receive Data of port COM1A/B EIA-485: Receive Data Plus of port COM1A/B
COM2 TXD / COM1 TXD-	Output	EIA-232: COM2 Transmit Data of port COM2A/B EIA-485: Transmit Data Minus of port COM1A/B
COM2 RXD / COM1 RXD-	Input	EIA-232: Receive Data of port COM2A/B EIA-485: Receive Data Minus of port COM1A/B
GND	-	Logic Ground
Shell	-	Chassis Ground

Serial Cable Description

RJ12 to DB9/DB25, male or female adapters are available from multiple sources, such as:

- Kontron (Order Code KIT-2X-RJ12DB9)
- Triangle Cable

Table 30: Serial Cable Mapping

DB9 CONNECTOR PIN	SIGNAL	RJ12 CONNECTOR PIN
1	-	1
2	TXD	3
3	RXD	4
4	-	6
5	GND	5

Figure 15: RJ12 / Female DB9 Cable

5.1.2 Gigabit Ethernet Connector

This section describes the two RJ45 front connectors carrying 1000BASE-T Ethernet ports ETH2A and ETH2B.

Front Gigabit Ethernet Connector Description

Table 31: Gigabit Ethernet Connector Pin Assignment

PIN	SIGNAL
1	TX+ / BI_DA+
2	TX- / BI_DA-
3	RX+ / BI_DB+
4	BI_DC+
5	BI_DC-
6	RX- / BI_DB-
7	BI_DD+
8	BI_DD-
Shell	Chassis Ground

Figure 16: RJ45 Tabdown Ethernet Connector

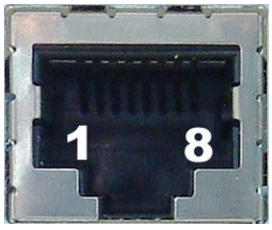


Table 32: Gigabit Ethernet Connector Signals Definition

SIGNAL	DIRECTION	DEFINITION
TX+/- / BI_DA+/-	Output / Bidir	10BASE-T & 100BASE-T: Transmit differential pair 1000BASE-T: BI_DA differential pair
RX+/- / BI_DB+/-	Input / Bidir	10BASE-T & 100BASE-T: Receive differential pair 1000BASE-T: BI_DB differential pair
BI_DC+/-	Bidir	10BASE-T & 100BASE-T: NC 1000BASE-T: BI_DC differential pair
BI_DD+/-	Bidir	10BASE-T & 100BASE-T: NC 1000BASE-T: BI_DD differential pair
Shell	-	Chassis ground

Ethernet Cable Description

The Ethernet cable should be a CAT5e with a maximum length of 100 meters.

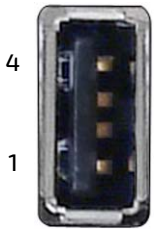
5.1.3 USB Connector

This section describes the two USB front connectors carrying USB 2.0 ports USB3A and USB3B.

Table 33: USB Connector Pin Assignment

PIN	SIGNAL
1	VCC
2	D-
3	D+
4	GND

Figure 17: USB Series A Receptacle



USB

Table 34: Gigabit Ethernet Connector Signals Definition

SIGNAL	DIRECTION	DEFINITION
D+/-	Bidir	USB differential pair
VCC	Output	+5V output rail. Protected by two dedicated power switches (rated current: 1A, limit current: minimum 1.3A, typical 1.55A, maximum 1.8A).
GND	-	Logic ground.

5.1.4 HDMI Connector

Front HDMI Connector Description

This section describes the two HDMI front connectors carrying the ports HDMIA and HDMIB.

Table 35: Mini DisplayPort Pin Assignment

PIN	SIGNAL
1	TMDS Data2+
2	GND
3	TMDS Data2-
4	TMDS Data1+
5	GND
6	TMDS Data1-
7	TMDS Data0+
8	GND
9	TMDS Data0-
10	TMDS Clock+
11	GND
12	TMDS Clock-
13	NC
14	NC
15	SCL
16	SDA
17	GND
18	+5V
19	Hot plug detect

Figure 18: Type A 19-position HDMI Receptacle

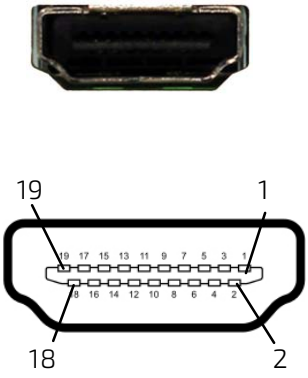


Table 36: HDMI Connector Signals Definition

SIGNAL	DIRECTION	DEFINITION
TMDS Data0+/-	Bidir	TMDS 0 differential pair
TMDS Data1+/-	Bidir	TMDS 1 differential pair
TMDS Data2+/-	Bidir	TMDS 2 differential pair
TMDS Clock+/-	Bidir	Clock differential pair
+5V	Output	+5V output rail. Protected by 1A resettable fuse.
Hot plug detect	-	Hot plug detection.

5.2 Onboard Connectors

Figure 19: Onboard Connectors (top side)

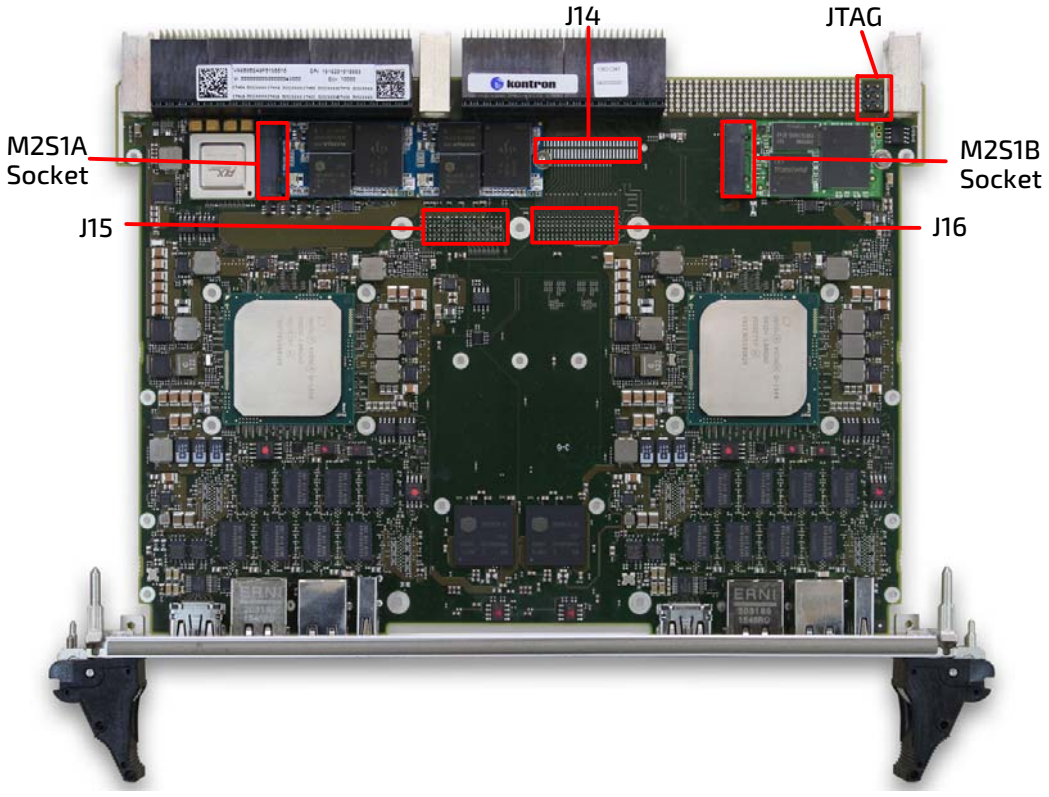
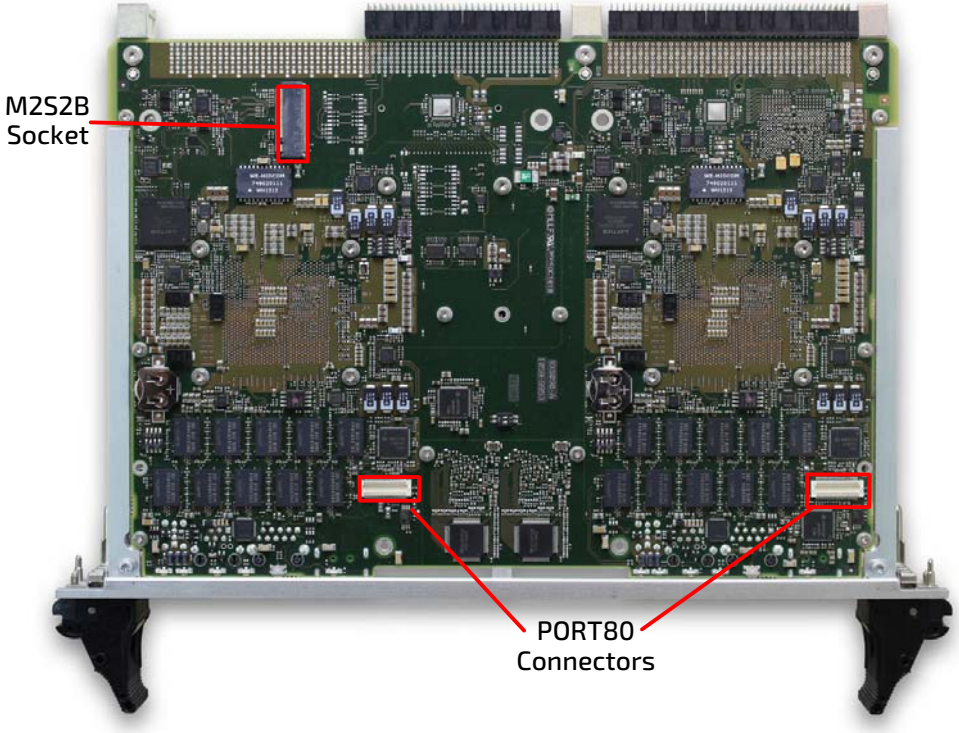


Figure 20: Onboard Connectors (bottom side)

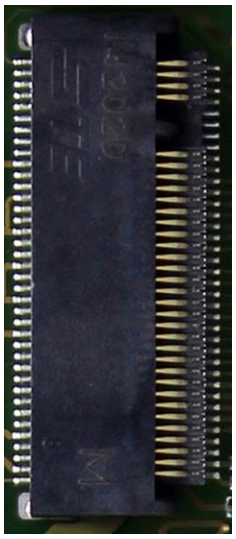


5.2.1 M2 Module Socket

Table 37: M.2 Module Socket Pin Assignment

PIN	SIGNAL	SIGNAL	PIN
		GND	75
74	3.3V	GND	73
72	3.3V	GND	71
70	3.3V	PEDET	69
68	SUSCLK (32kHz)	NC	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	NC (Reserved MFG_clock)	GND	57
56	NC (Reserved MFG_data)	REFCLKP / NC	55
54	PEWAKE# / NC	REFCLKN / NC	53
52	NC (CLKREQ#) / NC	GND	51
50	PERST# / NC	PETp0 / SATA-A+	49
48	NC	PETn0 / SATA-A-	47
46	NC	GND	45
44	NC	PERp0 / SATA-B-	43
42	NC	PERn0 / SATA-B+	41
40	NC	GND	39
38	NC (DEVSLP)	NC (PETp1) / NC	37
36	NC	NC (PETn1) / NC	35
34	NC	GND	33
32	NC	NC (PERp1) / NC	31
30	NC	NC (PERn1) / NC	29
28	NC	GND	27
26	NC	NC (PETp2) / NC	25
24	NC	NC (PETn2) / NC	23
22	NC	GND	21
20	NC	NC (PERp2) / NC	19
18	3.3V	NC (PERn2) / NC	17
16	3.3V	GND	15
14	3.3V	NC (PETp3) / NC	13
12	3.3V	NC (PETn3) / NC	11
10	LED1# / DAS_DSS#	GND	9
8	NC	NC (PERp3) / NC	7
6	NC	NC (PERn3) / NC	5
4	3.3V	GND	3
2	3.3V	GND	1

Figure 21: M.2 Socket 3 (M, H4.2)



When PCI Express and SATA function coexist the following convention applies: PCI_Express_function / SATA_function.

When the name of a signal differs between VX6090 and standard pinout (PCI Express M.2 & PCI Express 3.0), the standard pinout name is shown in parentheses.

Table 38: M.2 Module Socket Signal Description

SIGNAL PCI EXPRESS/SATA	DIRECTION	DEFINITION
3.3V	Output	+3.3V power supply. On VX6090, protected by dedicated 1.5A resettable fuse (one for each M.2 socket).
GND	-	Logic ground.
LED1# / DAS_DSS#	Input	- PCI Express: LED_1# indicator per PCI Express M.2 specification. On VX6090 connected to dedicated CPLD pin. - SATA: Device Activity Signal /Disable Staggered Spinup per SATA 3.2. On VX6090, DAS is not connected to a LED (which is the main purpose of this signal) and DSS is not used since the devices are SSD and not hard drives (no spinup). Signal connected to dedicated CPLD pin. Option: Multiplexed with CONFIG3.
NC	-	Pin NC in specification. NC on VX6090.
NC (CLKREQ#) / NC	Input	- PCI Express: Open drain CLKREQ# signal per PCI Express M.2 specification. Driven by M.2 module to request the platform to activate the PCI Express clock. On VX6090, pulled up and not implemented. - SATA: NC.
NC (DEVSLP)	Output	- PCI Express: NC - SATA: DEVSLP (Device Sleep) per SATA 3.2 indicates the module that it must enter a very low power mode (including transceiver circuitry). On VX6090, this signal is NC.
NC (PERp/n[1..3]) / NC	Input	- PCI Express: Receive differential pairs 1 to 3 per PCI Express M.2 and PCI Express 3.0 specifications. Not implemented on VX6090. - SATA: NC.
NC (PETp/n[1..3]) / NC	Output	- PCI Express: Transmit differential pairs 1 to 3 per PCI Express M.2 & PCI Express 3.0 specifications. Not implemented on VX6090. - SATA: NC.
NC (Reserved MFG_clock)	-	Pin reserved for SSD manufacturing. NC on VX6090.
NC (Reserved MFG_data)	-	Pin reserved for SSD manufacturing. NC on VX6090.
PEDET	Input	PEDET (PCI Express Detect) per PCI Express M.2 specification is driven low by SATA modules and high-Z by PCI Express modules (seen as a logic 1 due to on-board pull-up resistor). On VX6090, this signal is connected to a dedicated CPLD pin.
PERn0 / SATA-B+	Input	- PCIe: Receive differential signal minus per PCIe M.2 & PCIe 3.0 specifications. - SATA: Receive differential signal plus per SATA 3.2.
PERp0 / SATA-B-	Inpqut	- PCI Express: Receive differential signal plus per PCI Express M.2 & PCI Express 3.0 specifications. - SATA: Receive diffential signal minus per SATA 3.2.
PERST# / NC	Output	- PCI Express: PCI Express PERST# per PCI Express M.2 specification. On VX6090 handled by CPLD. - SATA: NC.
PETp/n0 / SATA-A+/-	Output	- PCI Express : Transmit differential pairs per PCI Express M.2 & PCI Express 3.0 specifications. - SATA: Transmit differential pair per SATA 3.2.
PEWAKE# / NC	Input	- PCI Express: Open drain WAKE# signal per PCI Express M.2 specification. Driven by M.2 module to allow the platform to reactivate the link main power rails and reference clock. On VX6090, this signal is wire-ORed with other WAKE# signals from i210 controllers and M.2 modules in the same A or B part. It is connected to SoC WAKE_# and WAKELAN_# pins. - S.ATA: NC
REFCLKP/N / NC	Output	- PCI Express: PCIe differential reference clock (100 MHz) per PCI Express M.2 & PCI Express 3.0 specifications. - SATA: NC.
SUSCLK	output	Suspend Clock for low power mode handling per PCI Express M.2 specification (32.768 kHz, duty cycle between 30% and 70%, 200ppm). On VX6090, connected to SoC SUSCLK_GPIO62.

When PCI Express and SATA function coexist the following convention applies: PCI Express_function / SATA_function.

When the name of a signal differs between VX6090 and standard pinout (PCI Express M.2 & PCI Express 3.0), the standard pinout name is shown in parentheses.

5.2.2 XMC J15 Connector

Table 39: XMC J15 Connector Pin Assignment

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR
2	GND	GND	NC (TRST#)	GND	GND	MRSTI#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR
4	GND	GND	NC (TCK)	GND	GND	NC (MRSTO#)
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR
6	GND	GND	NC (TMS)	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR
8	GND	GND	NC (TDI)	GND	GND	-12V
9	NC (Reserved)	NC (Reserved)	NC (Reserved)	NC (Reserved)	NC (Reserved)	VPWR (1)
10	GND	GND	NC (TDO)	GND	GND	GA0
11	PER0p0	PER0n0	NC (MBIST#)	PER0p1	PER0n1	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PER0p2	PER0n2	3.3V AUX	PER0p3	PER0n3	VPWR
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	NC (Reserved)	PER0p5	PER0n5	VPWR
16	GND	GND	NVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	NC (Reserved)	PER0p7	PER0n7	NC (Reserved)
18	GND	GND	NC (Reserved)	GND	GND	NC (Reserved)
19	REFCLK+0	REFCLK-0	NC (Reserved)	WAKE#	NC (ROOT0#)	NC (Reserved)

Signals active when low.

When the name of a signal differs between VX6090 and standard pinout, the standard pinout name is shown in parentheses.

Table 40: XMC J15 Connector Signals Definition

SIGNAL	DIRECTION	DEFINITION
+12V	Output	+12V power pin. Connected to VPWR by 0402 resistor. Protected by the same fuse as VPWR.
-12V	Output	-12V power pin. Protected by 1.1A, resettable fuse.
3.3V	Output	+3.3V power pins. Protected by 3.5A resettable fuse.
3.3V AUX	Output	Auxiliary +3.3V. On VX6090 connected to +3.3V standby voltage rail V_3V3SBB. Protected by 1.1A fuse.
GA[0..2]	Output	I2C channel select as per VITA 42.0. All GA are set to 0 on VX6090: XMC EEPROM 7bits Addr set to 0x50
GND	-	Logic ground as per VITA 42.3 (driven by VX6090).
MPRESENT#	Input	Module present as per VITA 42.0. This signal allows the carrier to determine whether an XMC is present. Connected to CPLDA and CPLDB on VX6090.
MRSTI#		XMC Reset In as per VITA 42.0 and PCI Express PERST# as per VITA 42.3. As per VITA 42: 10 ms pulse minimum.
MSDA	Bidir	I2C serial data as per VITA 42.0. On VX6090 connected to I2C bus SoC-SMBUS.

SIGNAL	DIRECTION	DEFINITION
MSCL	Output	I2C serial clock as per VITA 42.0. On VX6090 connected to I2C bus SoC-SMBUS.
NC (MBIST#)	Input	XMC Built In Self Test as per VITA 42.0. Not implemented on VX6090.
NC (MRSTO#)	Input	Optional XMC Reset Out driven by XMC as per VITA 42.0. Not implemented on VX6090.
NC (TRST#)	Output	JTAG Reset as per VITA 42.0. This signal is pulled down through 1K resistor on VX6090. XMC JTAG not implemented on VX6090.
NC (TCK)	Output	JTAG Clock as per VITA 42.0. This signal is pulled up to 3.3V through 1K resistor on VX6090. XMC JTAG not implemented on VX6090.
NC (TMS)	Output	JTAG Mode Select as per VITA 42.0. This signal is pulled up to 3.3V through 1K resistor on VX6090. XMC JTAG not implemented on VX6090.
NC (Reserved)	-	Reserved pins as per VITA 42.0 and VITA 42.3. NC on VX6090.
NC (ROOT0#)	Output	Signal ROOT0# as per VITA 42.3 indicating to a Processor XMC that it is designated to be the Root Complex. Not implemented on VX6090.
NC (TDI)	Output	JTAG Data In as per VITA 42.0. This signal is pulled down through 1K resistor on VX6090. XMC JTAG not implemented on VX6090.
NC (TDO)	Input	JTAG Data Out as per VITA 42.0. This signal is pulled up to 3.3V through 1K resistor on VX6090. XMC JTAG not implemented on VX6090.
NVMRO	Output	XMC Write Prohibit as per VITA 42.0 (when high, writes to non-volatile memory on the XMC are prohibited). On VX6090, connected to CPLDB.
PET0p/n[0..7]	Input	PCI Express differential transmit pairs 0 to 7 as per VITA 42.3 (driven by VX6090).
PER0p/n[0..7]	Output	PCI Express differential receive pairs 0 to 7 as per VITA 42.3 (driven by VX6090).
REFCLK+/-0	Ouput	100MHz PCI Express differential reference clock as per VITA 42.3 (driven by VX6090).
VPWR	Output	+12V or +5V power pins defined by VITA 42.0 and set to +12V on VX6090. Protected by a 2.6A resettable fuse.
WAKE#	Input	Open drain WAKE# signal as as per VITA 42.3 to allow the XMC to reactivate the link main power rails and reference clock. On VX6090, this signal is wire-ORed with other WAKE# signals from part B i210 controllers and from M2S1B and M2S2B mezzanine cards. It is also connected to SoCB WAKE_# and WAKELAN_# pins.

When the name of a signal differs between VX6090 and standard pinout, the standard pinout name is shown in parentheses.

5.2.3 XMC J16 Connector

Table 41: XMC J16 Connector Pin Assignment

PIN	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	XMCIO X8d+ 01	XMCIO X8d- 01	XMCIO X38s 37	XMCIO X8d+ 02	XMCIO X8d- 02	XMCIO X38s 38
2	GND	GND	XMCIO X38s 35	GND	GND	XMCIO X38s 36
3	XMCIO X8d+ 03	XMCIO X8d- 03	XMCIO X38s 33	XMCIO X8d+ 04	XMCIO X8d- 04	XMCIO X38s 34
4	GND	GND	XMCIO X38s 31	GND	GND	XMCIO X38s 32
5	XMCIO X12d+ 01	XMCIO X12d- 01	XMCIO X38s 29	XMCIO X12d+ 02	XMCIO X12d- 02	XMCIO X38s 30
6	GND	GND	XMCIO X38s 27	GND	GND	XMCIO X38s 28
7	XMCIO X12d+ 03	XMCIO X12d- 03	XMCIO X38s 25	XMCIO X12d+ 04	XMCIO X12d- 04	XMCIO X38s 26
8	GND	GND	XMCIO X38s 23	GND	GND	XMCIO X38s 24
9	XMCIO X12d+ 05	XMCIO X12d- 05	XMCIO X38s 21	XMCIO X12d+ 06	XMCIO X12d- 06	XMCIO X38s 22
10	GND	GND	XMCIO X38s 19	GND	GND	XMCIO X38s 20
11	XMCIO X8d+ 05	XMCIO X8d- 05	XMCIO X38s 17	XMCIO X8d+ 06	XMCIO X8d- 06	XMCIO X38s 18
12	GND	GND	XMCIO X38s 15	GND	GND	XMCIO X38s 16
13	XMCIO X8d+ 07	XMCIO X8d- 07	XMCIO X38s 13	XMCIO X8d+ 08	XMCIO X8d- 08	XMCIO X38s 14
14	GND	GND	XMCIO X38s 11	GND	GND	XMCIO X38s 12
15	XMCIO X12d+ 07	XMCIO X12d- 07	XMCIO X38s 09	XMCIO X12d+ 08	XMCIO X12d- 08	XMCIO X38s 10
16	GND	GND	XMCIO X38s 07	GND	GND	XMCIO X38s 08
17	XMCIO X12d+ 09	XMCIO X12d- 09	XMCIO X38s 05	XMCIO X12d+ 10	XMCIO X12d- 10	XMCIO X38s 06
18	GND	GND	XMCIO X38s 03	GND	GND	XMCIO X38s 04
19	XMCIO X12d+ 11	XMCIO X12d- 11	XMCIO X38s 01	XMCIO X12d+ 12	XMCIO X12d- 12	XMCIO X38s 02

Table 42: XMC J16 Connector Signals Definition

SIGNAL	DIRECTION	DEFINITION
XMCIO X38s [xx]	Bidir	XMCIO single-ended signal [xx] according to VITA 46.9 configuration X38s
XMCIO X8d+/- [xx]	Bidir	XMCIO differential pair [xx] according to VITA 46.9 configuration X8d
XMCIO X12d+/- [xx]	Bidir	XMCIO differential pair [xx] according to VITA 46.9 configuration X12d

5.2.4 PMC J14 Connector

Table 43: PMC J14 Connector Pin Assignment

PIN	SIGNAL	SIGNAL	PIN
1	PMC IO 01	PMC IO 02	2
3	PMC IO 03	PMC IO 04	4
5	PMC IO 05	PMC IO 06	6
7	PMC IO 07	PMC IO 08	8
9	PMC IO 09	PMC IO 10	10
11	PMC IO 11	PMC IO 12	12
13	PMC IO 13	PMC IO 14	14
15	PMC IO 15	PMC IO 16	16
17	PMC IO 17	PMC IO 18	18
19	PMC IO 19	PMC IO 20	20
21	PMC IO 21	PMC IO 22	22
23	PMC IO 23	PMC IO 24	24
25	PMC IO 25	PMC IO 26	26
27	PMC IO 27	PMC IO 28	28
29	PMC IO 29	PMC IO 30	30
31	PMC IO 31	PMC IO 32	32
33	PMC IO 33	PMC IO 34	34
35	PMC IO 35	PMC IO 36	36
37	PMC IO 37	PMC IO 38	38
39	PMC IO 39	PMC IO 40	40
41	PMC IO 41	PMC IO 42	42
43	PMC IO 43	PMC IO 44	44
45	PMC IO 45	PMC IO 46	46
47	PMC IO 47	PMC IO 48	48
49	PMC IO 49	PMC IO 50	50
51	PMC IO 51	PMC IO 52	52
53	PMC IO 53	PMC IO 54	54
55	PMC IO 55	PMC IO 56	56
57	PMC IO 57	PMC IO 58	58
59	PMC IO 59	PMC IO 60	60
61	PMC IO 61	PMC IO 62	62
63	PMC IO 63	PMC IO 64	64

Table 44: PMC J14 Connector Signals Definition

SIGNAL	DIRECTION	DEFINITION
PMCIO [xx]	Bidir	PMCIO connected to pin J14.[xx] according to VITA 46.9 configuration P64s.

5.2.5 P80 Connector

This connector is a provision and is not equiped. Please contact Kontron.

Table 45: P80 Connector Pin Assignment

PIN	SIGNAL	SIGNAL	PIN
1	GND	NC	2
3	Reserved	12V	4
5	Reserved	12V	6
7	GND	NC	8
9	NC	3.3V StandBy	10
11	GND	NC	12
13	NC	3.3V	14
15	Reserved	3.3V	16
17	CLK_33M_P80	NC	18
19	GND	GND	20
21	LPC_P80_SERIRQ	NC	22
23	LPC_P80_FRAME#	NC	24
25	LPC_P80_LAD3	GND	26
27	LPC_P80_LAD2	Reserved	28
29	LPC_P80_LAD0	Reserved	30
31	LPC_P80_LAD1	GND	32
33	GND	NC	34
35	Reserved	5V	36
37	Reserved	5V	38
39	GND	NC	40

Figure 22: P80 Connector
Board-to-Board SMT socket, 0.5 mm pitch, 20x2 positions

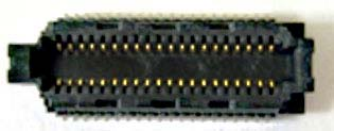


Table 46: P80 Connector Signals Definition

SIGNAL	DIRECTION	DEFINITION
LPC_P80_LAD[0..3]	Output	Port 80 address AD0 to AD3.
LPC_P80_FRAME#	Output	Port 80 FRAME#.
LPC_P80_SERIRQ	Input	Port 80 SERIRQ.
CLK_33M_P80	Output	Port 80 33MHz clock.
Reserved	-	Reserved. Do not connect.
12V	Output	+12V power pins. On VX6090, protected by 1.5A fuse.
3.3V	Output	+3.3V power pins. On VX6090, protected by 0.5A fuse.
3.3V StandBy	Output	+3.3V standby power pins. On VX6090, protected by 0.5A fuse.
5V	Output	+5V power pins. On VX6090, protected by 0.5A fuse.
GND	-	Logic ground.
NC	-	Not Connected.

5.2.6 JTAG Connector

This connector gives access to the CPLD JTAG port for programmation.

Figure 23: JTAG connector, 2 mm pitch, 3x2 positions

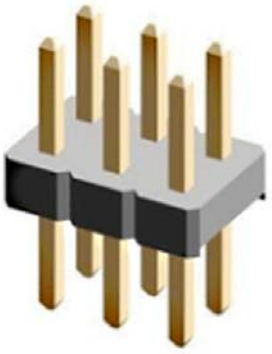


Table 47: JTAG Connector Pin Assignment

PIN	SIGNAL	SIGNAL	PIN
1	PLDAB_JTAG_TCK	PLDAB_JTAG_TMS	2
3	PLD_JTAG_TDO_B	PLD_JTAG_TDI_A	4
5	GND	+3.3V standby	6

Table 48: JTAG Connector Signals Definition

SIGNAL	DIRECTION	DEFINITION
PLDAB_JTAG_TCK	Output	JTAG TCK for CPLD JTAG daisy chain.
PLD_JTAG_TDO_B	Output	JTAG TDO for CPLD JTAG daisy chain.
PLDAB_JTAG_TMS	Output	JTAG TMS for CPLD JTAG daisy chain.
PLD_JTAG_TDI_A	Input	JTAG TDI for CPLD JTAG daisy chain.
3.3V StandBy	Output	+3.3V standby power pin. On VX6090, protected by 0.5A fuse.
GND	-	Logic ground.

5.3 Rear Connectors

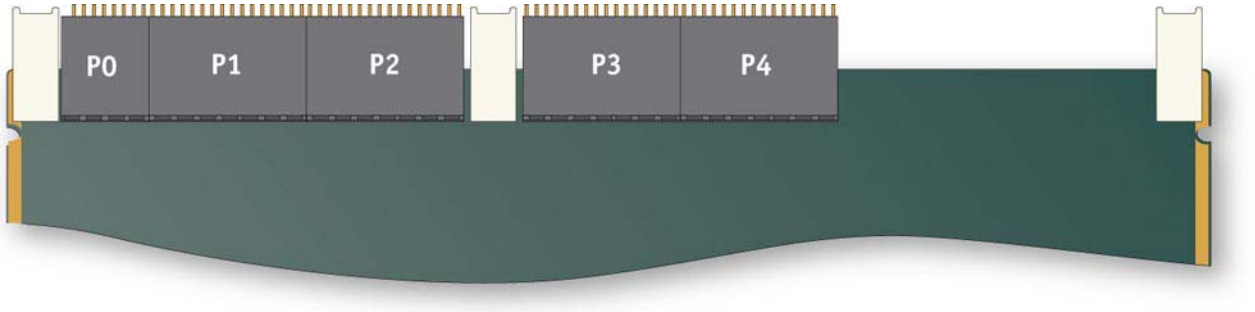
VX6090 rear I/Os mapping is fully compliant with OpenVPX system Specification (VITA 65), Payload Slot Profile SLT6-PAY-2F2U2T-10.2.5.

VPX Bus Interface

The complete 6U VPX connectors configuration comprises seven connectors named P0 to P6:

- P0: 8-wafer 7-row connector.
- P1 - P4: 16-wafer 7-row differential connectors.
- P5 - P6: not equipped.

Figure 24: VPX Connectors



5.3.1 P0 Connector

Table 49: VPX Connector P0 Pin Assignment

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	+12V (VS1)	+12V (VS1)	+12V (VS1)	NC	NC (VS2)	NC (VS2)	NC (VS2)
2	+12V (VS1)	+12V (VS1)	+12V (VS1)	NC	NC (VS2)	NC (VS2)	NC (VS2)
3	NC (VS3)	NC (VS3)	NC (VS3)	NC	NC (VS3)	NC (VS3)	NC (VS3)
4	CPLD-SMB1 CLK (SM2)	CPLD-SMB1 DAT (SM2)	GND	-12V_AUX	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3V3_AUX	GND	CPLD-SMB0 CLK (SM0)	CPLD-SMB0 DAT (SM1)
6	GA3*	GA2*	GND	NC (+12V_AUX)	GND	GA1*	GA0*
7	GPIO5 (TCK)	GND	PCIE_CLK- (TDO)	PCIE_CLK+ (TDI)	GND	GPIO3 (TMS)	GPIO4 (TRST*)
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND
CASE	GND						

* signal active when low

When the name of a signal differs between VX6090 and standard pinout (VITA 46.0), the standard pinout name is shown in parentheses

Table 50: VPX Connector P0 Signals Definition

SIGNAL	DIRECTION	DEFINITION
+12V (VS1)	Input	+12V or +48V power rail as per VITA 46.0. On VX6090, set to +12V.
-12V_AUX	Input	Optional auxiliary -12V power as per VITA 46.0. On VX6090, necessary only if the XMC requires it.
3.3V_AUX	Input	Mandatory auxiliary 3.3V power rail per VITA 46.0. On VX6090, +3.3V_AUX is ORed through ideal diodes with on-board +3.3V voltage regulator to supply CPLD. A true standby mode can only be achieved if 3.3V_AUX is present.
AUX_CLK+/-	Bidir	Optional, differential, auxiliary, reference clock as per VITA 46.0. Defined more precisely by VITA 65 as a 1 PPS (one pulse per second) clock. On VX6090, can be programmed as an output on system controller slot and input in other slots. Handled by CPLDA & CPLDB. Can be used to phase the CPLD timer/counter clocked by REF_CLK+/-.
CPLD-SMB0 DAT (SM1)	Bidir	Optional System Management Connection (Data SM1) as per VITA 46.0. On VX6090, data of SMBus CPLD-SMB0.
CPLD-SMB0 CLK (SM0)	Bidir	Optional System Management Connection (Clock SM0) as per VITA 46.0. On VX6090, clock of SMBus CPLD-SMB0.
CPLD-SMB1 DAT (SM3)	Bidir	Optional System Management Connection (Data SM3) as per VITA 46.0. On VX6090, data of SMBus CPLD-SMB1.
CPLD-SMB1 CLK (SM2)	Bidir	Optional System Management Connection (Clock SM2) as per VITA 46.0. On VX6090, clock of SMBus CPLD-SMB1.
GA[0..4]*	Input	Geographical address pins as per VITA 46.0. On VX6090, handled by CPLDA and CPLDB.
GAP	Input	Geographical address parity as per VITA 46.0. On VX6090, handled by CPLDA and CPLDB.
GND	-	Logic ground.
GPIO3 (TMS)	Bidir	JTAG TMS as per VITA 46.0. On VX6090, JTAG is not implemented and this signal carries GPIO3 (handled by CPLDA and CPLDB)
GPIO4 (TRST*)	Bidir	JTAG TRST* as per VITA 46.0. On VX6090, JTAG is not implemented and this signal carries GPIO4 (handled by CPLDA and CPLDB)
GPIO5 (TCK)	Bidir	JTAG TCK as per VITA 46.0. On VX6090, JTAG is not implemented and this signal carries GPIO5 handled by CPLDA & CPLDB.
NC (+12V_AUX)	-	Optional auxiliary +12V power rail as per VITA 46.0: NC on VX6090.
NC (VS2)	-	+12V or +48V power rail as per VITA 46.0. On VX6090, VS2 pins are NC
NC (VS3)		+5V power rail as per VITA 46.0. On VX6090, VS3 pins are NC.
NVMRO	Input	Non-Volatile Memory Read Only as per VITA 46.0. When asserted (logical 1), prevents any non-volatile memory from being updated. Bussed to all slots. On VX6090, handled by CPLDA and CPLDB.
PCIE_CLK+/- (TDI/TDO)	Input or Output	JTAG TDI and TDO as per VITA 46.0. On VX6090, JTAG is not implemented and these signals may be used as a common 100 MHz PCI Express reference clock connected to SoC (emitter on System Controller) or to PCI Express switch PEX8725 (receiver on non-System-controller boards).
REF_CLK+/-	Input or Output	Optional bussed differential reference clock (25MHz recommended) as per VITA 46.0. On VX6090, output if the board is plugged in the system controller slot, input otherwise. It enables the entire system to synchronize to a common time reference if desired. Counter/timer in the CPLD can use this clock.
SYSRESET	Bidir	VPX System Reset as per VITA 46.0. Input and open collector output. On VX6090, handled by CPLDA and CPLDB.

When the name of a signal differs between VX6090 and standard pinout (VITA 46.0), the standard pinout name is shown in parentheses

5.3.2 P1 Connector

Table 51: VPX Connector P1 Pin Assignment

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	GDISCRETE1	GND	PCIEG3 L0-TX-	PCIEG3 L0-TX+	GND	PCIEG3 L0-RX-	PCIEG3 L0-RX+
2	GND	PCIEG3 L1-TX-	PCIEG3 L1-TX+	GND	PCIEG3 L1-RX-	PCIEG3 L1-RX+	GND
3	P1_VBAT	GND	PCIEG3 L2-TX-	PCIEG3 L2-TX+	GND	PCIEG3 L2-RX-	PCIEG3 L2-RX+
4	GND	PCIEG3 L3-TX-	PCIEG3 L3-TX+	GND	PCIEG3 L3-RX-	PCIEG3 L3-RX+	GND
5	SYS_CON*	GND	PCIEG3 L4-TX-	PCIEG3 L4-TX+	GND	PCIEG3 L4-RX-	PCIEG3 L4-RX+
6	GND	PCIEG3 L5-TX-	PCIEG3 L5-TX+	GND	PCIEG3 L5-RX-	PCIEG3 L5-RX+	GND
7	Reserved	GND	PCIEG3 L6-TX-	PCIEG3 L6-TX+	GND	PCIEG3 L6-RX-	PCIEG3 L6-RX+
8	GND	PCIEG3 L7-TX-	PCIEG3 L7-TX+	GND	PCIEG3 L7-RX-	PCIEG3 L7-RX-	GND
9	USB0A PWR (UD)	GND	SATA0A TX- (UD)	SATA0A TX+ (UD)	GND	SATA0A RX- (UD)	SATA0A RX+ (UD)
10	GND	SATA1A TX- (UD)	SATA1A TX- (UD)	GND	SATA1A RX- (UD)	SATA1A RX+ (UD)	GND
11	USB0B PWR (UD)	GND	USBSSA TX- (UD)	USBSSA TX+ (UD)	GND	USBSSA RX- (UD)	USBSSA RX+ (UD)
12	GND	def USB0A D- opt COM1A RXD (UD)	def USB0A D+ opt COM1A TXD (UD)	GND	USB0B D- (UD)	USB0B D+ (UD)	GND
13	GPIO1 (UD)	GND	ETH2A DB- (TP02_DB-)	ETH2A DB+ (TP02_DB+)	GND	ETH2A DA- (TP02_DA-)	ETH2A DA+ (TP02_DA+)
14	GND	ETH2A DD- (TP02_DD-)	ETH2A DD+ (TP02_DD+)	GND	ETH2A DC- (TP02_DC-)	ETH2A DC+ (TP02_DC+)	GND
15	GPIO2 or Mask. Reset* (Mask. Reset*)	GND	ETH1A TX- (UTP02_TX-)	ETH1A TX+ (UTP02_TX+)	GND	ETH1A RX- (UTP02_RX-)	ETH1A RX+ (UTP02_RX+)
16	GND	ETH0A TX- (UTP01_TX-)	ETH0A TX+ (UTP01_TX+)	GND	ETH0A RX- (UTP01_RX-)	ETH0A RX+ (UTP01 _RX-)	GND
CASE	GND						

* signal active when low

When the name of a signal differs between VX6090 and standard pinout (VITA 65, VITA 46.4, VITA 46.6), the standard pinout name is shown in parentheses

Table 52: VPX Connector P1 Signals Definition

SIGNAL	DIRECTION	DEFINITION
ETH0A RX+/- (UTP01_RX+/-)	Input	Ultra-Thin Pipe Receive Data UTP01 as per VITA 46.6. On VX6090, 10GBASE-KR receive differential pair of port ETH0 of SoCA.
ETH0A TX+/- (UTP01_TX+/-)	Input	Ultra-Thin Pipe Transmit Data UTP01 as per VITA 46.6. On VX6090, 10GBASE-KR transmit differential pair of port ETH0 of SoCA.
ETH1A RX+/- (UTP02_RX+/-)	Input	Ultra-Thin Pipe Receive Data UTP02 as per VITA 46.6. On VX6090, 10GBASE-KR receive differential pair of port ETH1 of SoCA.
ETH1A TX+/- (UTP02_TX+/-)	Output	Ultra-Thin Pipe Transmit Data UTP02 as per VITA 46.6. On VX6090,10GBASE-KR transmit differential pair of port ETH1 of SoCA.

SIGNAL	DIRECTION	DEFINITION
ETH2A DA+/- (TP02_DA+/-)	Bidir	Thin Pipe Bidirectional Data TP02 A as per VITA 46.6. On VX6090, 1000BASE-T BI_DA differential pair of port ETH2 of Side A.
ETH2A DB+/- (TP02_DB+/-)	Bidir	Thin Pipe Bidirectional Data TP02 B as per VITA 46.6. On VX6090, 1000BASE-T BI_DB differential pair of port ETH2 of Side A.
ETH2A DC+/- (TP02_DC+/-)	Bidir	Thin Pipe Bidirectional Data TP02 C as per VITA 46.6. On VX6090, 1000BASE-T BI_DS differential pair of port ETH2 of Side A.
ETH2A DD+/- (TP02_DD+/-)	Bidir	Thin Pipe Bidirectional Data TP02 D as per VITA 46.6. On VX6090, 1000BASE-T BI_DD differential pair of port ETH2 of Side A.
GDISCRETE1	Bidir	General purpose, bussed, open drain signal per VITA 65. On VX6090, this signal is either an open collector output driven by CPLDA or CPLDB (output GDISCRETE1) or an input (SMB_ALERT#) on CPLDA & CPLDB.
GND	-	Logic ground.
GPIO1 (UD)	Bidir	User Defined per VITA 65. On VX6090, GPIO1 is handled by CPLDA & CPLDB.
GPIO2 or Mask. Reset* (Mask. Reset*)	Bidir	Maskable Reset* per VITA 65. On VX6090, GPIO2 or Maskable Reset* handled by CPLDA & CPLDB.
P1_VBAT	Input	Battery Voltage Input, 3V as per VITA 46. On VX6090, optional alternate source for RTC backup voltage
PCIEG3 L[7:0]-TX+/-	Output	Transmit differential pairs of PCI Express lanes L0 to L7 as per VITA 46.4. On VX6090, link(s) speed may be gen1, gen2 or gen3 and link(s) width may be 1 x8, 2 x4 or 4 x2. The VPX PCI Express links are handled by PEX8725 PCI Express switch.
PCIEG3 L[7:0]-RX+/-	Input	Receive differential pairs of PCI Express lanes L0 to L7 as per VITA 46.4. On VX6090, link(s) speed may be gen1, gen2 or gen3 and link(s) width may be 1 x8, 2 x4 or 4 x2. The VPX PCI Express links are handled by PEX8725 PCI Express switch.
SATA0A TX+/- (UD)	Output	User Defined per VITA 65. On VX6090, transmit differential pair of SATA0 port of SoCA.
SATA0A RX+/- (UD)	Input	User Defined per VITA 65. On VX6090, receive differential pair of SATA0 port of SoCA.
SATA1A TX+/- (UD)	Output	User Defined per VITA 65. On VX6090, transmit differential pair of SATA1 port of SoCA.
SATA1A RX+/- (UD)	Input	User Defined per VITA 65. On VX6090, receive differential pair of SATA1 port of SoCA.
SYS_CON*	Input	VPX system controller designator as per VITA 46.0. On VX6090, routed to CPLDA which in turn forwards it to CPLDB.
USB0A PWR (UD)	Output	User Defined per VITA 65. On VX6090, USB +5V power associated to USB0A port. Protected by power switch (rated current: 1A, limit current: minimum 1.3A, typical 1.55A, maximum 1.8A).
USB0B PWR (UD)	Output	User Defined per VITA 65. On VX6090, USB +5V power associated to USB0B port. Protected by power switch (rated current: 1A, limit current: minimum 1.3A, typical 1.55A, maximum 1.8A).
def USB0A D+ opt COM1A TXD (UD)	Bidir / Output	User Defined per VITA 65. On VX6090, depending on configuration: - Default: Data Plus of USB2.0 port USB0A. - Option: TXD signal of serial port COM1A (EIA-232).
def USB0A D- opt COM1A RXD (UD)	Bidir / Output	User Defined per VITA 65. On VX6090, depending on configuration: - Default: Data minus of USB2.0 port USB0A. - Option: RXD signal of serial port COM1A (EIA-232).
USB0B D+/- (UD)	Bidir	User Defined per VITA 65. On VX6090, differential pair of USB 2.0 port of SoCB.
USBSSA TX+/- (UD)	Output	User Defined per VITA 65. On VX6090, transmit differential pair of USB SuperSpeed (ie USB 3.0) port of SoCA.
USBSSA RX+/- (UD)	Input	User Defined per VITA 65. On VX6090, receive differential pair of USB SuperSpeed (USB 3.0) port of SoCA.

When the name of a signal differs between VX6090 and standard pinout (VITA 65, VITA 46.4, VITA 46.6), the standard pinout name is shown in parentheses

"def" and "opt" stand for Default and Option respectively.

5.3.3 P2 Connector

Table 53: VPX Connector P2 Pin Assignment

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	COM2A TXD / COM1A TXD+	GND	SATA2A TX-	SATA2A TX+	GND	SATA2A RX-	SATA2A RX+
2	GND	SATA0B TX-	SATA0B TX+	GND	SATA0B RX-	SATA0B RX+	GND
3	COM1A TXD / COM1A TXD-	GND	USB1A PWR	USB1A PWR	GND	USB1B PWR	USB1B PWR
4	GND	USB1A D-	USB1A D+	GND	USB1B D-	USB1B D+	GND
5	COM2A RXD / COM1A RXD+	GND	Reserved	Reserved	GND	Reserved	Reserved
6	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
7	COM1A RXD / COM1A RXD-	GND	Reserved	Reserved	GND	Reserved	Reserved
8	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
9	COM2B TXD / COM1B TXD+	GND	Reserved	Reserved	GND	Reserved	Reserved
10	GND	prov PCIE1A CLK-	prov PCIE1A CLK+	GND	Reserved	Reserved	GND
11	COM1B TXD / COM1B TXD-	GND	prov PCIE1A TX-	prov PCIE1A TX+	GND	prov PCIE1A RX-	prov PCIE1A RX+
12	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
13	COM2B RXD / COM1B RXD+	GND	Reserved	Reserved	GND	Reserved	Reserved
14	GND	Reserved	Reserved	GND	Reserved	Reserved	GND
15	COM1B RXD / COM1B RXD-	GND	ETH2B DB-	ETH2B DB+	GND	ETH2B DA-	ETH2B DA+
16	GND	ETH2B DD-	ETH2B DD+	GND	ETH2B DC-	ETH2BDC+	GND
CASE	GND						

* signal active when low

Table 54: VPX Connector P2 Signals Definition

SIGNAL	DIRECTION	DEFINITION
COM1A TXD / COM1A TXD-	Output	EIA-232: COM1A Transmit Data / EIA-485: COM1A Transmit Data Minus EIA-485: COM1A Transmit Data Minus
COM1A RXD / COM1A RXD-	Input	EIA-232: COM1A Receive Data / EIA-485: COM1A Receive Data Minus EIA-485: COM1A Receive Data Minus
COM1B TXD / COM1B TXD-	Output	EIA-232: COM1B Transmit Data / EIA-485: COM1B Transmit Data Minus EIA-485: COM1B Transmit Data Minus
COM1B RXD / COM1B RXD-	Input	EIA-232: COM1B Receive Data / EIA-485: COM1B Receive Data Minus EIA-485: COM1B Receive Data Minus
COM2A TXD / COM1A TXD+	Output	EIA-232: COM2A Transmit Data EIA-485: COM1A Transmit Data Plus
COM2A RXD / COM1A RXD+	Input	EIA-232: COM2A Receive Data EIA-485: COM1A Receive Data Plus
COM2B TXD / COM1B TXD+	Output	EIA-232: COM2B Transmit Data EIA-485: COM1B Transmit Data Plus
COM2B RXD / COM1B RXD+	Input	EIA-232: COM2B Receive Data EIA-485: COM1B Receive Data Plus
ETH2B DA+/-	Bidir	1000BASE-T BI_DA differential pair of port ETH2 of SoCB.
ETH2B DB+/-	Bidir	1000BASE-T BI_DB differential pair of port ETH2 of SoCB.
ETH2B DC+/-	Bidir	1000BASE-T BI_DC differential pair of port ETH2 of SoCB.
ETH2B DD+/-	Bidir	1000BASE-T BI_DD differential pair of port ETH2 of SoCB.

SIGNAL	DIRECTION	DEFINITION
GND	-	Logic ground.
PCIE1A CLK+/-	Output	Provision: Clock differential pair of additional PCI Express 1x link PCIE1A of SoCA.
PCIE1A TX+/-	Output	Provision: Transmit differential pair of additional PCI Express 1x link PCIE1A of SoCA.
PCIE1A RX+/-	Input	Provision: Receive differential pair of additional PCI Express 1x link PCIE1A of SoCA.
SATA0B TX+/-	Output	Transmit differential pair of port SATA0 of SoCB.
SATA0B RX+/-	Input	Receive differential pair of port SATA0 of SoCB.
SATA2A TX+/-	Output	Transmit differential pair of port SATA2 of SoCA.
SATA2A RX+/-	Input	Receive differential pair of port SATA2 of SoCA.
USB1A D+/-	Bidir	Differential pair of USB 2.0 port USB1 of SoCA.
USB1B D+/-	Bidir	Differential pair of USB 2.0 port USB1 of SoCB.
USB1A PWR	Output	USB +5V power associated to USB1A port. Protected by power switch (rated current: 1A, limit current: minimum 1.3A, typical 1.55A, maximum 1.8A).
USB1B PWR	Output	USB +5V power associated to USB1B port. Protected by power switch (rated current: 1A, limit current: minimum 1.3A, typical 1.55A, maximum 1.8A).

All pins are user-defined as per VITA 65.

5.3.4 P3 Connector

Table 55: VPX Connector P3 Pin Assignment

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A		
1	5V	GND	J14-1	J14-3	GND	J14-2	J14-4		P64S
2	GND	J14-5	J14-7	GND	J14-6	J14-8	GND		
3	Reserved	GND	J14-9	J14-11	GND	def J16-C1 opt J14-10	def J16-F1 opt J14-12	X38s	
4	GND	def J16-C2 opt J14-13	def J16-C3 opt J14-15	GND	def J16-F2 opt J14-14	def J16-F3 opt J14-16	GND		
5	Reserved	GND	def J16-C4 opt J14-17	def J16-C5 opt J14-19	GND	def J16-F4 opt J14-18	def J16-F5 opt J14-20		
6	GND	def J16-C6 opt J14-21	def J16-C7 opt J14-23	GND	def J16-F6 opt J14-22	def J16-F7 opt J14-24	GND		
7	Reserved	GND	def J16-C8 opt J14-25	def J16-C9 opt J14-27	GND	def J16-F8 opt J14-26	def J16-F9 opt J14-28		
8	GND	def J16-C10 opt J14-29	def J16-C11 opt J14-31	GND	def J16-F10 opt J14-30	def J16-F11 opt J14-32	GND		
9	Reserved	GND	def J16-C12 opt J14-33	def J16-C13 opt J14-35	GND	def J16-F12 opt J14-34	def J16-F13 opt J14-36		
10	GND	def J16-C14 opt J14-37	def J16-C15 opt J14-39	GND	def J16-14 opt J14-38	def J16-F15 opt J14-40	GND		
11	Reserved	GND	def J16-C16 opt J14-41	def J16-C17 opt J14-43	GND	def J16-F16 opt J14-42	def J16-F17 opt J14-44		
12	GND	def J16-C18 opt J14-45	def J16-C19 opt J14-47	GND	def J16-F18 opt J14-46	def J16-F19 opt J14-48	GND		
13	Reserved	GND	J14-49	J14-51	GND	J14-50	J14-52		
14	GND	J14-53	J14-55	GND	J14-54	J14-56	GND		
15	Reserved	GND	J14-57	J14-59	GND	J14-58	J14-60		
16	GND	J14-61	J14-63	GND	J14-62	J14-64	GND		
CASE	GND								

"def" and "opt" stand for Default and Option respectively.

Table 56: VPX Connector P3 Signals Definition

SIGNAL	DIRECTION	DEFINITION
5V	Output	+5V power driven by VX6090. Protected by 0.5A resettable fuse.
GND	-	Logic ground.
J14-[xx]	Bidir	PMCIO connected to pin J14.[xx] according to VITA 46.9 configuration P64s.
def J16-[xx] opt J14-[xx]	Bidir	Default: XMCIO connected to pin J16.[xx] according to VITA 46 X38s configuration Option: PMCIO connected to pin J14.[xx] according to VITA 46.9 configuration P64s.

"def" and "opt" stand for Default and Option respectively.

5.3.5 P4 Connector

Table 57: VPX Connector P4 Pin Assignment

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A	
1	5V	GND	J16-A5	J16-B5	GND	J16-D5	J16-E5	X12d
2	GND	J16-A7	J16-B7	GND	J16-D7	J16-E7	GND	
3	Reserved	GND	J16-A9	J16-B9	GND	J16-D9	J16-E9	
4	GND	J16-A15	J16-B15	GND	J16-D15	J16-E15	GND	
5	Reserved	GND	J16-A14	J16-B17	GND	J16-D17	J16-E17	
6	GND	J16-A19	J16-B19	GND	J16-D19	J16-E19	GND	X6d
7	Reserved	GND	J16-A1	J16-B1	GND	J16-D1	J16-E1	
8	GND	J16-A3	J16-B3	GND	J16-D3	J16-E3	GND	
9	def Reserved prov LAN0_MDIO-I2CSDA_B	GND	J16-A11	J16-B11	GND	J16-D11	J16-E11	
10	GND	J16-A13	J16-B13	GND	J16-D13	J16-E13	GND	
11	def Reserved prov LAN0_MDC-I2CSCL_B	GND	ETH1B TX- (UTP02 _TX-)	ETH1B TX+ (UTP02 _TX+)	GND	ETH1B RX- (UTP02 _RX-)	ETH1B RX+ (UTP02 _RX+)	
12	GND	ETH0B TX- (UTP01 _TX-)	ETH0B TX+ (UTP01 _TX+)	GND	ETH0B RX- (UTP01 _RX-)	ETH0B RX+ (UTP01 _RX+)	GND	
13	def Reserved prov LAN0_MDIO-I2CSDA_A	GND	def ETH3B SrdsSigDet prov ETH3B DB- (TP02_DB-)	def ETH3B SfpI2cClk prov ETH3B DB+ (TP02_DB+)	GND	def ETH3B SfpI2cDat prov ETH3B DA- (TP02_DA-)	def Reserved prov ETH3B DA+ (TP02_DA+)	
14	GND	def ETH3B TX- prov ETH3B DD- (TP02_DD-)	def ETH3B TX+ prov ETH3B DD+ (TP02_DD+)	GND	def ETH3B RX- prov ETH3B DC- (TP02_DC-)	def ETH3B RX+ prov ETH3B DC+ (TP02_DC+)	GND	
15	def Reserved prov LAN0_MDC-I2C_SCL_A	GND	def ETH3A SrdsSigDet prov ETH3A DB- (TP01_DB-)	def ETH3A SfpI2cClk prov ETH3A DB+ (TP01_DB+)	GND	def ETH3A SfpI2cDat prov ETH3A DA- (TP01_DA-)	def Reserved prov ETH3A DA+ (TP01_DA+)	
16	GND	def ETH3A TX- prov ETH3A DD- (TP01_DD-)	def ETH3A TX+ prov ETH3A DD+ (TP01_DD+)	GND	def ETH3A RX- prov ETH3A DC- (TP01_DC-)	def ETH3A RX+ prov ETH3A DC+ (TP01_DC+)	GND	
CASE	GND							

When the name of a signal differs between VX6090 and standard pinout (VITA 46.6), the standard pinout name is shown in parentheses

"def", "opt" and "prov" stand for Default, Option and Provision respectively.

Table 58: VPX Connector P4 Signals Definition

SIGNAL	DIRECTION	DEFINITION
5V	Output	+5V power driven by VX6090. Protected by 0.5A resettable fuse.
Jn6-[xx]	Bidir	XMCIO connected to pin J16.[xx]
ETH0B RX+/- (UTP01 _RX+/-)	P4 to SoC A	Ultra-Thin Pipe Receive Data UTP01 as per VITA 46.6. On VX6090, 10GBASE-KR receive differential pair of port ETH0 of SoCB.
ETH0B TX+/- (UTP01 _TX+/-)	SoC A to P4	Ultra-Thin Pipe Transmit Data UTP01 as per VITA 46.6. On VX6090, 10GBASE-KR transmit differential pair of port ETH0 of SoCB.

SIGNAL	DIRECTION	DEFINITION
ETH1B RX+/- (UTP02 _RX+/-)	P4 to SoC B	Ultra-Thin Pipe Receive Data UTP02 as per VITA 46.6. On VX6090, 10GBASE-KR receive differential pair of port ETH1 of SoCB.
ETH1B TX+/- (UTP02 _TX+/-)	SoC B to P4	Ultra-Thin Pipe Transmit Data UTP02 as per VITA 46.6. On VX6090, 10GBASE-KR transmit differential pair of port ETH1 of SoCB.
def Reserved prov ETH3A DA+ (TP01_DA+)	Bidir	Default: Reserved. Provision: Thin Pipe Bidirectional Data TP01 A+ as per VITA 46.6. On VX6090, 1000BASE-T differential signal DA+ of port ETH3 of Side A.
def ETH3A SfpI2cDat prov ETH3A DA- (TP01_DA-)	Bidir	Default: i210A SFP_I2C_DATA associated with Ethernet Port ETH3A in 1000BASE-KX configuration. Provision: Thin Pipe Bidirectional Data TP01 A- as per VITA 46.6. On VX6090, 1000BASE-T differential signal DA- of port ETH3 of Side A.
def ETH3A SfpI2cClk prov ETH3A DB+ (TP01_DB+)	Bidir	Default: i210A SFP_I2C_CLK associated with Ethernet Port ETH3A in 1000BASE-KX configuration. Provision: Thin Pipe Bidirectional Data TP01 B+ as per VITA 46.6. On VX6090, 1000BASE-T differential signal DB+ of port ETH3 of Side A.
def ETH3A SrdsSigDet prov ETH3A DB- (TP01_DB-)	Bidir	Default: i210A SRDS_SIG_DET associated with Ethernet Port ETH3A in 1000BASE-KX configuration. Provision: Thin Pipe Bidirectional Data TP01 B- as per VITA 46.6. On VX6090, 1000BASE-T differential signal DB- of port ETH3 of Side A.
def ETH3A RX+/- prov ETH3A DC+/- (TP01_DC+/-)	Bidir	Default: Receive differential pair of Side A Ethernet Port ETH3A in 1000BASE-KX configuration. Provision: Thin Pipe Bidirectional Data TP01 C as per VITA 46.6. On VX6090, 1000BASE-T differential pair DC+/- of port ETH3 of Side A.
def ETH3A TX+/- prov ETH3A DD+/- (TP01_DD+/-)	Bidir	Default: Transmit differential pair of Side A Ethernet Port ETH3A in 1000BASE-KX configuration. Provision: Thin Pipe Bidirectional Data TP01 D as per VITA 46.6. On VX6090, 1000BASE-T differential pair DD+/- of port ETH3 of Side A.
def Reserved prov ETH3B DA+ (TP02_DA+)	Bidir	Default: Reserved. Provision: Thin Pipe Bidirectional Data TP02 A+ as per VITA 46.6. On VX6090, 1000BASE-T differential signal DA+ of port ETH3 of Side B.
def ETH3B SfpI2cDat prov ETH3B DA- (TP02_DA-)	Bidir	Default: i210B SFP_I2C_DATA associated with Ethernet Port ETH3B in 1000BASE-KX configuration. Provision: Thin Pipe Bidirectional Data TP02 A- as per VITA 46.6. On VX6090, 1000BASE-T differential signal DA- of port ETH3 of Side B.
def ETH3B SfpI2cClk prov ETH3B DB+ (TP02_DB+)	Bidir	Default: i210B SFP_I2C_CLK associated with Ethernet Port ETH3B in 1000BASE-KX configuration. Provision: Thin Pipe Bidirectional Data TP02 B+ as per VITA 46.6. On VX6090, 1000BASE-T differential signal DB+ of port ETH3 of Side B.
def ETH3B SrdsSigDet prov ETH3B DB- (TP02_DB-)	Bidir	Default: i210B SRDS_SIG_DET associated with Ethernet Port ETH3B in 1000BASE-KX configuration. Provision: Thin Pipe Bidirectional Data TP02 B- as per VITA 46.6. On VX6090, 1000BASE-T differential signal DB- of port ETH3 of Side B.
def ETH3B RX+/- prov ETH3B DC+/- (TP02_DC+/-)	Bidir	Default: Receive differential pair of Side B Ethernet Port ETH3B in 1000BASE-KX configuration. Provision: Thin Pipe Bidirectional Data TP02 C as per VITA 46.6. On VX6090, 1000BASE-T differential pair DC+/- of port ETH3 of Side B.
def ETH3B TX+/- prov ETH3B DD+/- (TP02_DD+/-)	Bidir	Default: Transmit differential pair of Side B Ethernet Port ETH3B in 1000BASE-KX configuration. Provision: Thin Pipe Bidirectional Data TP02 D as per VITA 46.6. On VX6090, 1000BASE-T differential pair DD+/- of port ETH3 of Side B.
Reserved	-	Default: Reserved

When the name of a signal differs between VX6090 and standard pinout (VITA 46.6), the standard pinout name is shown in parentheses

"def", "opt" and "prov" stand for Default, Option and Provision respectively.

5.3.6 P5 & P6 Connectors

P5 & P6 VPX connectors are not equipped.

5.4 LEDs

Status LEDs on Front Panel

There are 10 LEDs (Red/Green/Orange) on the front panel:

- LEDs A1 to A5 are attached to Side A,
- LEDs B1 to B5 are attached to Side B,

Figure 25: Front panel LEDs

LEDs States

There are eight different states for each LED. They are listed in Table 59.

Table 59: LEDs Description

SYMBOL	STATE DESCRIPTION
●	LED OFF
●	Steady Red
●	Steady Green
●	Steady Orange
✳	Blinking Red
✳	Blinking Green
✳	Blinking Orange
✳	Blinking. The color is not relevant. Color and blinking states are totally independant.

LEDs Meaning

In the following table, [X] refers to side A or B in a fully interchangeable way since the LEDs have the same meaning on sides A and B.

Table 60: LEDs meaning

L[X]1	L[X]2	L[X]3	L[X]4	L[X]5	MEANING
●					Permanent system error: the internal power supplies of side [X] are turned off. In this state, LED [X]2 to [X]5 do not carry the meaning described in this table but an error code detailed later in this chapter.
● ✳					Steady: At least one of the two 1GbE links ETH2[X], ETH3[X] is up in 1GbE speed. Blinking: Activity on this interface.
● ✳					Steady: At least one of the two 1GbE links ETH2[X], ETH3[X] is up but not in 1GbE speed. Blinking: Activity on this interface.
●					The two Ethernet interfaces ETH2[X] ETH3[X] are down (no link).
	●				Fatal Error detected on PCI Express switch PEX8725.
	● ✳				Steady: Both 10G Ethernet links are up (ETH0[X] and ETH1[X]). Blinking: Activity on either of these interfaces.
	● ✳				Steady: Only one 10G Ethernet link is up (either ETH0[X] or ETH1[X]) Blinking: Activity on this interface.
	●				Both 10G Ethernet interfaces are down.
		●			Internal power supplies in side [X] are on (all PowerGood signals asserted) and reset signal is asserted (side [X] is in reset).
		●			Internal power supplies in side [X] are on (all PowerGood signals asserted) and reset signal is de-asserted (normal operation side [X]).
		●			Internal power supplies in side [X] are on (all PowerGood signals asserted) but the SoC [X] output PROCPWRGD_PCH is not activated, indicating that the SoC internal power is not valid.
		✳ ✳			Fast blinking RED: Activity to/from CPLD on SMBbus CPLD-SMB0 or CPLD-SMB1 and Platform Reset asserted by CPLD in side [X]. Fast blinking GREEN: Activity to/from CPLD on SMBbus CPLD-SMB0 or CPLD-SMB1 bus and Platform Reset de-asserted by CPLD in side [X]. Slow blinking GREEN (1Hz, 50% duty cycle): internal power supplies in side [X] are OFF (side [X] in standby)
			●		side [X] not in factory test mode and no CPLD watchdog expired. (Normal operation side [X])
			●		Side [X] in factory test mode
			●		Side [X] CPLD Watchdog expired
			✳		Blinking (color not relevant and keeps its steady state meaning): M.2 activity on socket M2S2B (bottom side).
				●	Processor hot event (PROCHOT) (1) Supersedes 1GbE routing information coded in green or orange.
				●	1GbE link ETH2[X] routed to front.
				●	1GbE link ETH2[X] routed to VPX backplane
				✳	Blinking (color not relevant and keeps its steady state meaning): M.2 activity on socket M2S1[X] (top side).

(1) LED is lit red only if PROCHOT signal is activated by SoC to indicate over temperature condition, it is not lit up red if PROCHOT has been asserted by CPLD to force SoC in low frequency operation.

PowerGood Errors

Table 61: LEDs Decoding for PowerGood Errors

L[X]1	L[X]2	L[X]3	L[X]4	L[X]5	POWERGOOD ERRORS
🔴	⚫	⚫	⚫	⚫	PWRGD_VPX
🔴	⚫	⚫	⚫	🔴	VPXPWRGD_UV
🔴	⚫	⚫	🔴	⚫	VPXPWRGD_OV
🔴	⚫	⚫	🔴	🔴	PWRGD_VR5V0
🔴	⚫	🔴	⚫	⚫	PWRGD_VCCSCFUSESUS
🔴	⚫	🔴	⚫	🔴	PWRGD_VCCKRHV
🔴	⚫	🔴	🔴	⚫	PWRGD_VR1V5_PCH
🔴	⚫	🔴	🔴	🔴	PWRGD_VR1V05
🔴	🔴	⚫	⚫	⚫	PWRGD_VR2V5_DDR4
🔴	🔴	⚫	⚫	🔴	PWRGD_VR1V2
🔴	🔴	⚫	🔴	⚫	PWRGD_VTT
🔴	🔴	⚫	🔴	🔴	PWRGD_FET1V05
🔴	🔴	🔴	⚫	⚫	PWRGD_VRPEX
🔴	🔴	🔴	⚫	🟠	PWRGD_VR1V8
🔴	🔴	🔴	⚫	🔴	PWRGD_VR3V3
🔴	🔴	🔴	🔴	⚫	PWRGD_VRVCCIN
🔴	⚫	⚫	⚫	🟠	PWRGD_VR1V8SERDES
🔴	⚫	⚫	🟠	🟠	PWRGD_VR2V5RETIMP1 (E.C. Level 1xxxxxx) PWRGD_VR3V3SUS (E.C. Level 2xxxxxx and above)
🔴	🔴	🔴	🔴	🔴	RESERVED
🔴	🟠	🟠	🟠	🟠	WAKE UP ERROR (timeout on SLP_S4# deassertion)
🔴	🟠	🟠	🟠	⚫	PROCPWRGD ERROR (timeout on PROCPWRGD_PCH assertion)
🔴	🟠	🟠	⚫	🟠	PLTRST# ERROR (timeout on deassertion S5 To S0)
🔴	⚫	⚫	🟠	⚫	LPC CLOCK is 48 MHz (Legacy value is 33 MHz)
🔴	⚫	⚫	⚫	🟠	LPC CLOCK is 25 MHz (Legacy value is 33 MHz)

Critical Erros

Table 62: LEDs Decoding for Critical Errors

L[X]1	L[X]2	L[X]3	L[X]4	L[X]5	CRITICAL ERRORS
🔴	🔴	🔴	🔴	✳	PECI_CRIT#
🔴	🔴	🔴	✳	🔴	CATERR#
🔴	🔴	✳	🔴	🔴	VR1V05_VRHOT#
🔴	✳	🔴	🔴	🔴	VRVCCIN_VRHOT#
✳	🔴	🔴	🔴	🔴	THERMTRIP#

6 / Electrical Specifications

6.1 Input Power Rail VS1

VS1 Specification

The VX6090 is powered by the VPX +12V rail VS1. This supply should comply to the following:

- Voltage: 12V +/- 5% (11.4V to 12.6V) inclusive of ripple (VITA 46.0).
- Power on: monotonic rise time, 20 to 125 ms.
- Power off: no undershoot below 0V (VITA 46.0) and a level of 0V maintained at least one second before the next power on.

VS1 monitoring

The voltage sensor NCT7802Y by Nuvoton is programmed by BIOS to monitor VS1 and asserts the signal PLD_PECI_ALERT_A# or PLD_PECI_ALERT_B# whenever VS1 gets out of the range 12 V +/-5% (VITA 46). This alert is routed to a maskable interrupt in the cPLD.

A second voltage sensor, the LTC2913 by Linear Technology monitors VS1 with a 10% tolerance. The thresholds are set by hardware on the board. Undervoltage and overvoltage conditions are reported to the cPLD which will in turn shut down all VX6090 internal power supplies whenever VS1 gets out the range 12 V +/-10%. There is no software mechanism for masking these alerts.

6.2 Input Power Rail +3.3V_AUX

+3.3V_AUX Specification

The VX6090 implements an ideal diode which forwards to CPLD either +3.3V_AUX from P0 or the internally generated +3.3V supply (derived from VS1). Normal and standby modes for CPLD are summarized in Table 63. The +3.3V_AUX presence is required only when the standby mode for CPLD is needed.

+3.3V_AUX voltage specification: 3.3 V +/- 5% (3.135 V to 3.465 V) inclusive of ripple (VITA 46.0)

+3.3V_AUX current specification: 1 A continuous (VITA 46.0), 1.25 A instantaneous (VITA 65 recommendation).

Table 63: +3.3V_AUX, normal and standby modes for CPLD

P0 VS1 (+12V)	INTERNAL +3.3V (V_P3V3_SB_OUT_A/B)	P0 +3.3V_AUX	CPLD (AND IPMI IF EQUIPED)
OFF	OFF	Absent	Not powered.
ON	ON	Absent	Powered by internal +3.3V (normal mode)
OFF	OFF	ON	Powered by +3.3V_AUX (standby mode)
ON	ON	ON	Powered by +3.3V_AUX (normal mode)

3.3V_AUX Monitoring

The CPLD power supply is monitored by the Nuvoton NCT7802 (input VCC). This power supply reflects either +3.3V_AUX or the internally generated +3.3V supply V_P3V3_SB_OUT_A/B as explained above.

6.3 VBAT

VBAT Specification

Voltage: 3.0 V typical, 2.55 V minimum, 3.5 V maximum (VITA 46.0).

VBAT takes over onboard battery and VPX 3.3V_AUX to power the RV8564 RTC when these supplies are not available. See detailed RTC description in section 4.1.1 page 27.

6.4 Input Powers Protection

The input power rails are protected on the VX6090 by fuse as described in Table 64.

To prevent safety hazards, the chassis power supply must not exceed the Voltage Rating and Interrupt Rating of the fuse.

Table 64: Input Powers Protection

POWER RAIL	VS1	3.3V AUX
LOCATION	P0	P0
VOLTAGE	+12 V	+3.3 V
PROTECTION	Non resettable fuse	Non resettable fuse
RATED CURRENT	20 A	1.5 A
TRIP CURRENT	-	2.1 A min @85°C 3.0 A typ @23°C 3.5 A max @-40°C
TYPICAL MELT I^2T	48.6 A^2s	-
VOLTAGE RATING	24 V	32 V
INTERRUPTING RATING	150 A	35 A
MANUFACTURER / PN	Cooper Bussmann / 3216FF20-R	Littelfuse / 043501.5KR

6.5 Output Powers Protection

On the VX6090, all the output power supplies provided on connectors are protected by fuse or current-limiting devices as described in Table 65.

Table 65: Output Powers Protection

Port	Function	Location	Signal	Voltage	Protection	Hold or Rated Current	Trip current	Characteristics
USB3A USB3B	USB 2.0	Front	VCC	+5 V	Current limited power switch	1 A	1.3 A min 1.55 A typ 1.8 A max	Reverse current blocking Thermal shutdown: 135°C Response time: 2 µs FAULT reported to SoC
HDMIA HDMIB	HDMI	Front	+5 V	+5 V	Resettable fuse	1.1 A	1.03 A min @85°C 2.2 A typ @23°C 2.9 A max @-40°C	Time to trip: 0.3 s @8 A @23°C
USB0A USB0B USB1A USB1B	USB 2.0	Rear P1 Rear P2	USB0A PWR USB0B PWR USB1A PWR USB1B PWR	+5 V	Current limited power switch	1 A	1.3 A min 1.55 A typ 1.8 A max	Reverse current blocking Thermal shutdown: 135°C Response time: 2 µs FAULT reported to SoC
-	VPX	Rear P3 Rear P4	5 V	+5 V	Resettable fuse	0.5 A	min @85°C 1.0 A typ @23°C 1.4 A max @-40°C	Time to trip: 0.1 s max @8 A

XMC	XMC	On board J15	VPWR, +12 V	+12 V	Resettable fuse	2.6 A	2.6 A min @85°C 5 A typ @23°C 6.5 A max @-40°C	Time to trip: 5 s @8 A @23°C
XMC	XMC	On board J15	-12 V	-12 V	Resettable fuse	1.1 A	1.03 A min @85°C 2.2 A typ @23°C 2.9 A max @-40°C	Time to trip: 0.3 s @8 A @23°C
XMC	XMC	On board J15	3.3 V	+3.3 V	Resettable fuse	3.5 A	3.6 A min @60°C 6.3 A typ @20°C 7.5 A max @0°C	Time to trip: 5 s @8 A @20°C
XMC	XMC	On board J15	3.3 V AUX	+3.3 V	Resettable fuse	1.1 A	1.03 A min @85°C 2.2 A typ @23°C 2.9 A max @-40°C	Time to trip: 0.3 s @8 A @23°C
M2S1A M2S1B M2S2B	M.2 socket	On board	VPWR	+3.3 V	Resettable fuse	1.5 A	1.7 A min @85°C 3.0 A typ @25°C 4.4 A max @-40°C	Time to trip: 0.3 s @8 A @23°C

6.6 GPIOs

GPIO Electrical Characteristics

The CPLD features LVCMOS33 cells (0 - 3.3 V), with a drive strength of 8 mA (sink or source), a clamp diode which is not 5 V tolerant and an hysteresis of 250 mV. The CPLD does not implement any internal pull-up or pull-down.

CAUTION: GPIOs are not 5 V tolerant. Maximum voltage on GPIOs is 3.6 V. Absolute maximum voltage is 3.75 V and is not suitable for continuous operation. Appropriate voltage reduction (through resistor divider for instance) must be made to avoid permanent damage to the board.

GPIOs Pull-ups

On the VX6090 board, a pull-up of 47 kOhm is connected to GPIO1, GPIO3, GPIO4 and GPIO5. GPIO2/MaskableReset* has a pull-up of 4.7 kOhm according to VITA 65.

7 / Power and Thermal Management

7.1 Intel® Turbo Boost Technology 2.0

Intel® Turbo Boost Technology automatically allows processor cores to run faster than the base operating frequency if it is operating below power, current, and temperature specification limits.

Dynamically increasing performance: Turbo Boost Technology is activated when the Operating System (OS) requests the highest processor performance state (P0).

The maximum frequency of Turbo Boost is dependent on the number of active cores. The amount of time the processor spends in the Intel Turbo Boost state depends on the workload and operating environment.

Any of the following can set the upper limit of Turbo Boost on a given workload:

- Number of active cores
- Estimated current consumption
- Estimated power consumption
- Processor temperature

When the processor is operating below these limits and the user's workload demands additional performance, the processor frequency will dynamically increase until the upper limit of frequency is reached. Turbo Boost has multiple algorithms operating in parallel to manage current, power, and temperature to maximize performance and energy efficiency.

Intel Turbo Boost Technology 2.0 allows the processor to operate at a power level that is higher than its rated upper power limit (TDP) for short durations to maximize performance.

Learn more about Turbo Boost Technology: http://www.intel.com/technology/turboboost/

- Turbo Boost is handled by the BIOS through the Advanced Power Management Configuration menu.
  Refer to the AMI BIOS for VX6090 User Reference Manual, section “IntelRCSetup Menu”.

7.2 Power Consumption Monitoring

7.2.1 Xeon® D Power Consumption

The Xeon® D core frequency, the dissipated power at package level are closely related. They can be measured using the following tools:

- Intel Performance Tuning Utility tool (PTU) for Xeon-D processors. The core load may be set between 0 and 100%. This is a major tool for characterizing the thermal behavior of a board in a system. In addition, PTU indicates the power dissipated, the temperature and frequency of each core.
- Turbostat, an open-source linux tool which provides monitoring of the temperature, the frequency and the load of each core. Unlike PTU, Turbostat does not generate any core activity and power dissipation must be defined and controlled through user's programs or applications.

7.2.2 VX6090 Board Power Monitoring

The current monitor LTC2945 accessible from SMBus SoC-SMBUS gives the current drawn by the VX6090 on the VS1 power rail (12V):

- Side A: overall current (side A + side B).
- Side B: current drawn by side B only.

7.3 Power Consumption Specification

Table 66 gives the worst case continuous current value on VPX VS1 power rail (12V).

Table 66: VX6090 Maximum Current

VX6090 TYPE	MAX CONTINUOUS CURRENT / POWER ON VS1	TEST CONDITIONS
VX6090RA8G0050010 Dual Xeon® D-1548 TDP 45W No XMC, no VPX PCI Express	12.8 A / 154 W	Full Functionnal Tests on both SoCs (all functions except XMC and VPX PCI Express). Turbo ON. 100% load. No throttle.

Table 67 shows the power consumption of the VX6090 in three different configurations: maximum power consumption with Turbo Boost mode on, maximum power consumption with Turbo Boost mode off and low power consumption with minimum frequency and activity.

Table 67: VX6090 Power Consumption

	POWER MODE	TOTAL CURRENT VS1/12V	TOTAL POWER (1)	SOC POWER (2)	REST OF THE BOARD (3)	TEST CONDITIONS
VX6090 Xeon ® D @ 2 GHz	Turbo On, Max Processor power, TDP 45W	TBD	TBD	TBD	TBD	TBD
	Turbo Off, Max Processor power, TDP 45W @ 2.0 Ghz	TBD	TBD	TBD	TBD	
	Linux idle Linux «on demand» mode Processor frequency TBD GHz	TBD	TBD	TBD	TBD	

(1) The value of the total power dissipated by VX6090 is obtained through VPX VS1 current measurement.

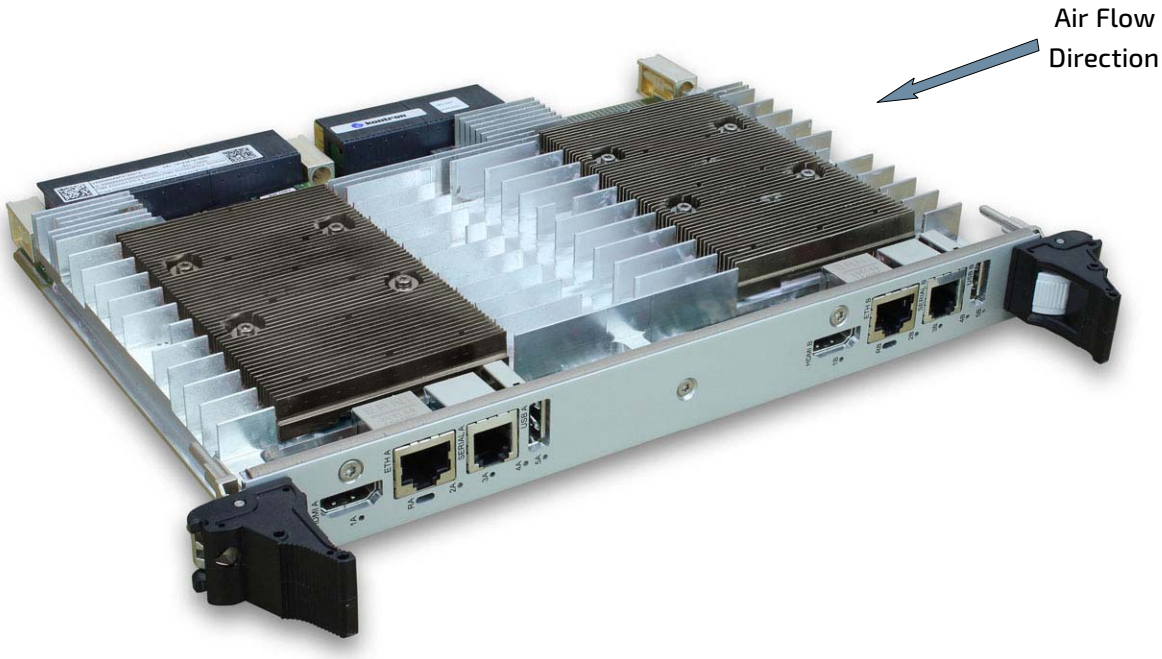
(2) The same tests run on SoCA and SoCB. The SoC power dissipation is the greatest of the power dissipations of SoCA and SoCB. It is measured through PTU tool.

(3) The "Rest of the board" dissipation is the difference between Total Power and SoC Power.

7.4 VX6090 Heatsink and Air Flow Direction

To allow a balanced cooling of the two SoC on VX6090, the heatsink design has been made assymetrical, as shown in Figure 26 with an aluminum vapor-chamber heatsink on SoCB (right side of figure) and a copper vapor-chamber heatsink on SoCA (left side of figure) . The air flow direction cannot be inverted and must flow from side B to side A.

Figure 26: VX6090 heatsink



On bottom side, a plate has been added for improved heat distribution.

7.5 Temperature Monitoring

To ensure long-term reliability of the VX6090, onboard components must not operate beyond their specified maximum temperature. The most critical component is the processor. Operating above the maximum operating limits could result in permanent damage to the board.

7.5.1 Processor Temperature

The Xeon® D SoC features an integrated heat spreader (IHS) which interfaces the die with the board cooling device.

To allow optimal operation and long-term reliability, the Xeon® D must remain within the temperature specifications as defined by Intel. This applies both to the internal temperature measured by the Digital Thermal Sensor (DTS) inside the SoC and the case temperature TCASE.

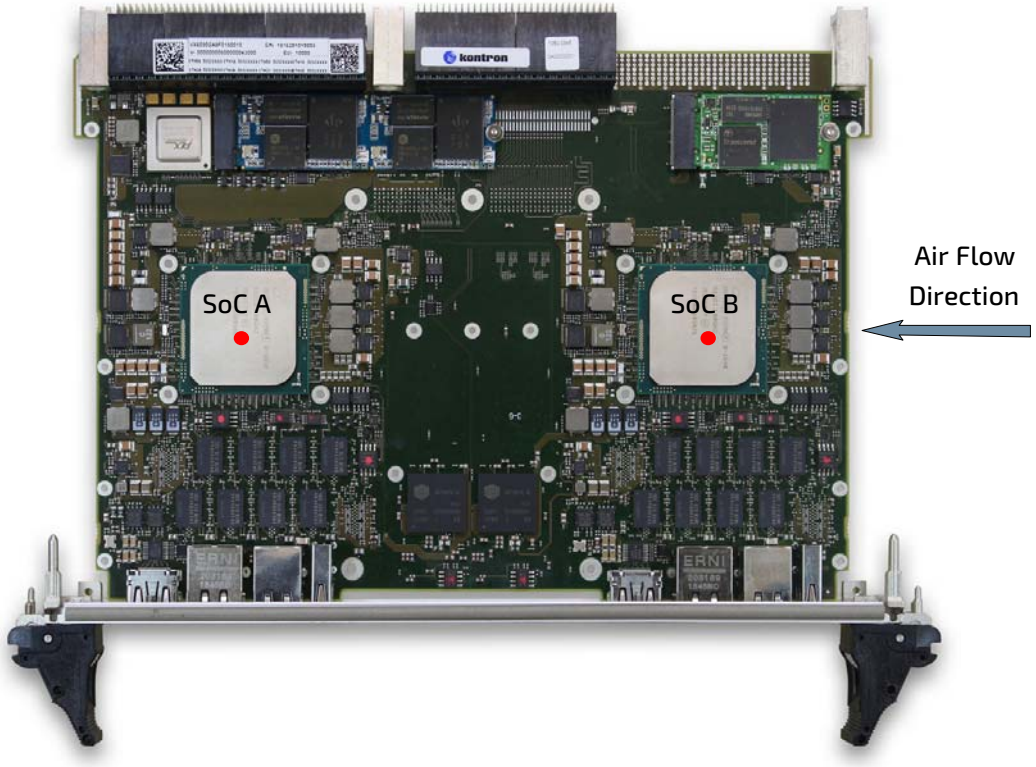
For the 8-core, 2-GHz SKUs with a TDP of 45W on which the VX6090 is based the temperature specifications are:

- DTS max = 104°C (a DTS offset applies)
- TCASE max = 89°C

The DTS can be read back using Linux command **<sensors>**.

TCASE is measured with a thermocouple attached at the center of the IHS as shown on Figure 27.

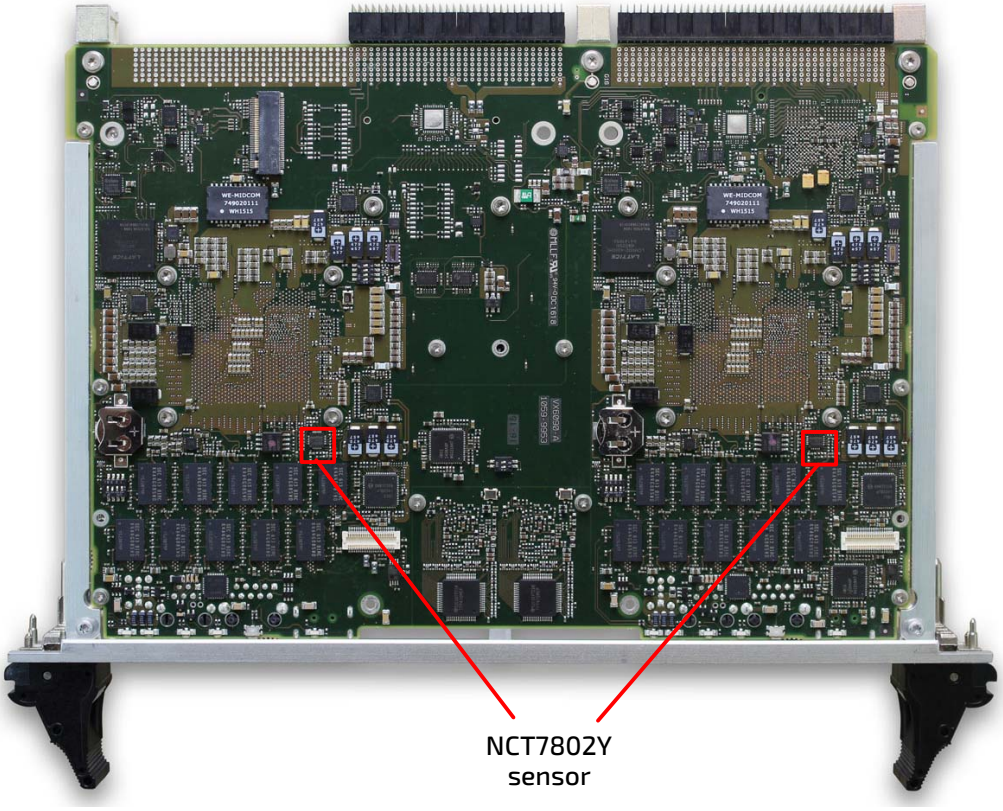
Figure 27: Thermocouple location for TCASE measurement



7.5.2 Board Temperature

The VX6090 implements a temperature sensor (NCT7802Y by Nuvoton) managed by the CPLD through I2C bus CPLD-I2CLOC @ 99.2 KHz and accessible through Linux "sensors" command.

Figure 28: Temperature Sensors Location



The NCT7802Y has two alarm outputs connected to the CPLD:

- ALERT#: logged in CPLD to generate a maskable interrupt.
  The high threshold is set to +85°C by BIOS but may be modified by the BIOS UEFI command

  ```
  VX6090> kpld -i2cw 2 50 36 1 <value>.
  ```

  The low threshold is set to -45°C by BIOS but may be modified by the BIOS UEFI command

  ```
  VX6090> kpld -i2cw 2 50 37 1 <value>
  ```

  The low threshold may also be used as the lower threshold for high temperature hysteresis.
- T_CRIT#: logged in CPLD reg @0x74, leads to fatal error with all internal power supplies being switched off and the error status is being displayed on the front panel LEDs. The T_CRIT# threshold is set to +95°C by BIOS but may be modified by the BIOS UEFI command

  ```
  VX6090> kpld -i2cw 2 50 3D 1 <value>
  ```

The characteristics of the temperature sensor of the NCT7802Y are:

- On-chip Temperature Sensor Accuracy (25~70°C): +- 2°C typ.
- On-chip Temperature Sensor Resolution: 1 °C

7.6 Air Flow Specification

7.6.1 Temperature difference between SoCA and SoCB

The SoCB being located near the side of the incoming air, its temperature is about 5°C below that of SoCA.
The thermal information given in the following paragraphs focuses on SoCA.

7.6.2 High Temperature & High Power Thermal Operating Points

100% Processor Load

Table 68 shows four thermal operating points measured on a VX6090 board without XMC at high temperature and 100% processor load. They include some margin for the SoCA Tj with respect to the 104°C DTS max temperature to account for silicon disparity, DTS accuracy, test environment variations.

Table 68: VX6090 Thermal Operating Points at full Processor Load

VX6090RA8G0050010 - E.C.LEVEL XXXXXE1 - DUAL XEON® D-1548 TDP 45W						
CASE	INCOMING AIR TEMPERATURE	AVERAGE POWER SOCA & SOCB	AVERAGE BOARD POWER	AIR FLOW	AVERAGE TJ SOCA	TEST CONDITIONS
Case 1 VAPC_H27	50°C	42 W	132 W	20 CFM	96°C	Functionnal Tests on both SoCs (all functions except XMC, 10GbE, VPX PCI Express). No Turbo. Fixed Frequency 2.0 GHz. 100% load. No throttle.
Case 2 VAPC_H26	50°C	45 W	136 W	25 CFM	94°C	Full Functionnal Tests on both SoCs (all functions except XMC, 10GbE, VPX PCI Express). Turbo ON. 100% load. No throttle.
Case 3 VAPC_H24	55°C	42.5 W	126 W	25 CFM	96 °C	Full Functionnal tests on both SoCs (all functions except XMC, 10GbE, VPX PCI Express). No Turbo. Fixed Frequency 2.0 GHz.100% load. No throttle.
Case 4 VAPC_H25	55°C	45 W	140 W	30 CFM	96 °C	Full Functionnal Tests on both SoCs (all functions except XMC, 10GbE, VPX PCI Express). Turbo ON. 100% load. No throttle.

80% Processor Load

Table 69 shows the difference between 100% and 80% processor loads using Intel® PTU. A decrease in activity from 100% to 80% saves 4 W per SoC which corresponds either to 4°C for junction temperature (constant flow rate) or to 4 CFM (constant temperature, extrapolated from Flow Rate Curve in chapter 7.6.3).

Table 69: VX6090 Thermal Operating Points at 80% Processor Load

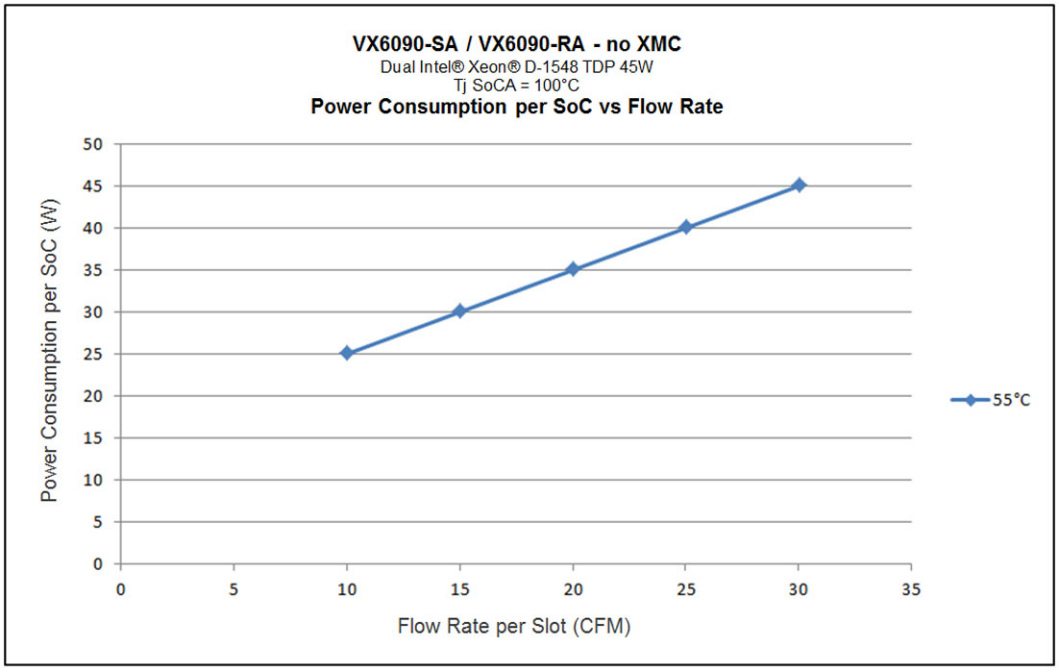
VX6090RA8G0050010 - E.C.LEVEL XXXXXE1 - DUAL XEON® D-1548 TDP 45W - NO TURBO						
CASE	INCOMING AIR TEMPERATURE	AVERAGE POWER SOCA & SOCB	AVERAGE BOARD POWER	AIR FLOW	AVERAGE TJ SOCA	TEST CONDITIONS
Case 5 VAPC_H24	55°C	100%	41 W	25 CFM	96°C	Intel® PTU test with 100% load + Graphics Test. No Turbo. Fixed Frequency 2.0 GHz. No throttle.
Case 6 VAPC_H24	55°C	80%	37 W	25 CFM	92°C	Intel® PTU test with 80% load + Graphics Test. No Turbo. Fixed Frequency 2.0 GHz. No throttle.

7.6.3 Flow Rate Curve

Thermal performance in terms of temperature and flow rate depends essentially on the power dissipated by the Xeon® D and the board. This power in turn varies with the core frequency, the CPU load and the application.

The curve in Figure 29 indicates the allowed Power Consumption per SoC versus Flow Rate to keep the junction temperature of SoCA at 100°C with an incoming air of 55°C. In this curve, "Power Consumption per SoC" means that both SoCs are running and each dissipates the power value shown on the y-axis.

Figure 29: Power Consumption per SoC vs Flow Rate



8 / VPX Backplane

8.1 Backplage Suggestions

Whether for development or deployment, Kontron offer three backplane models: a single-star x4, 8-slot topology, a single-star x4, 5-slot topology and a distributed, 2-slot topology. They are described in the following figures.

Figure 30: Single Star x4, 8-slot Topology

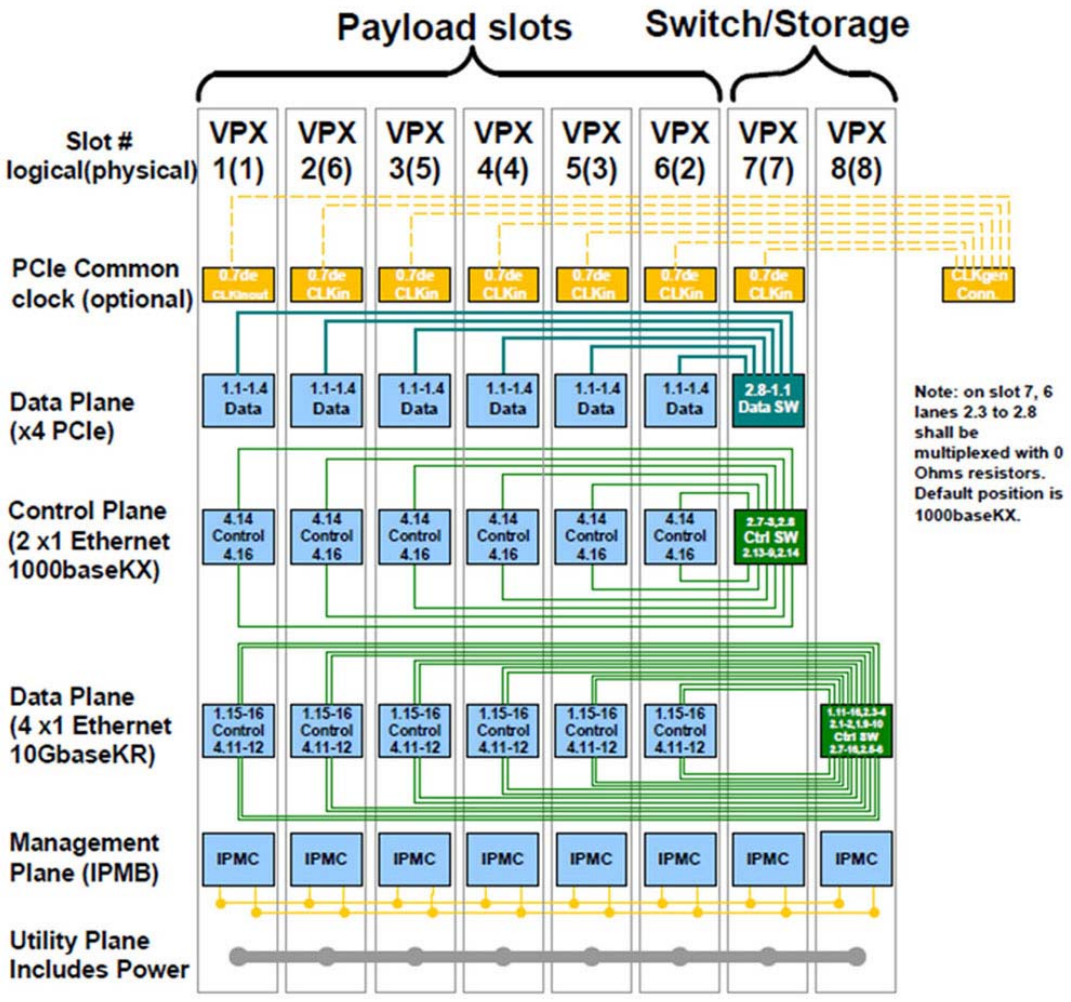


Figure 31: Single Star x4, 5-Slot Topology

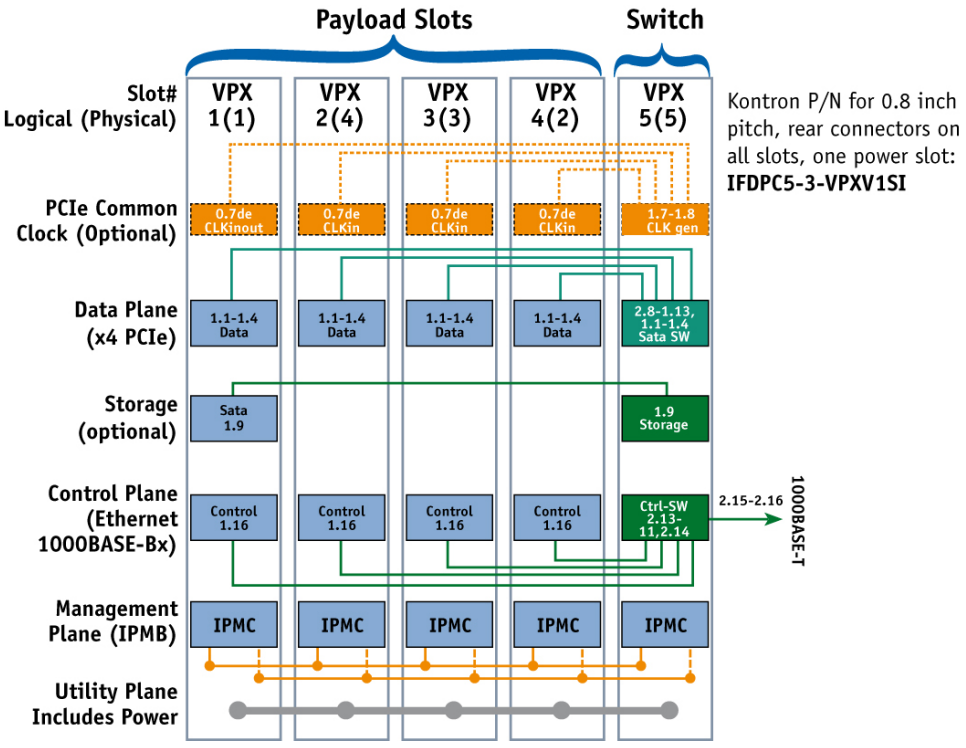
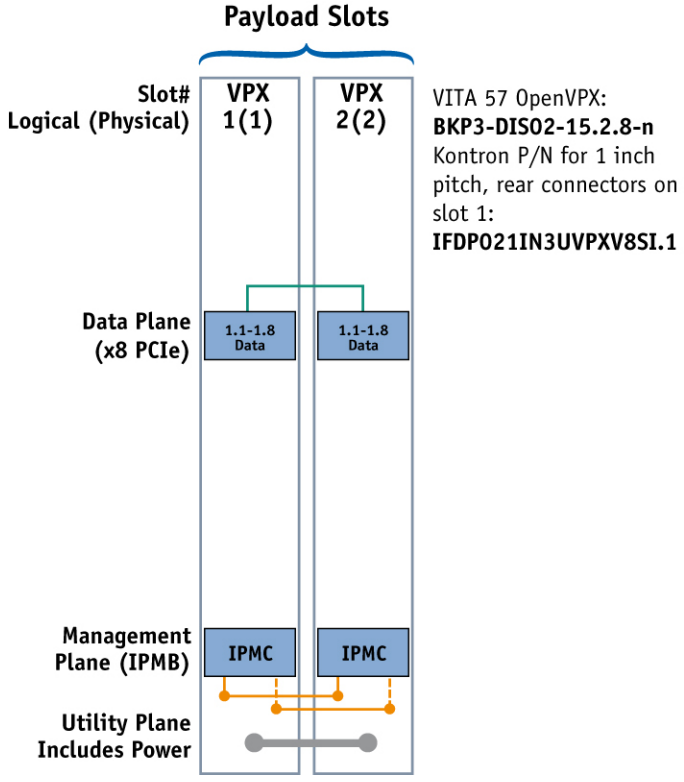


Figure 32: Distributed, 2-Slot Topology



8.2 3U Backplane Compatibility

For test purposes, the VX6090 can operate in a VX3058-like 3U backplane configuration with the following limitations:

- All functions related to connectors P3 and P4 will not be available.
- The VPX alignment key close to P0 should be changed form a 315° orientation to a "no key".

About Kontron

Kontron, a global leader in embedded computing technology and trusted advisor in IoT, works closely with its customers, allowing them to focus on their core competencies by offering a complete and integrated portfolio of hardware, software and services designed to help them make the most of their applications.

With a significant percentage of employees in research and development, Kontron creates many of the standards that drive the world's embedded computing platforms; bringing to life numerous technologies and applications that touch millions of lives. The result is an accelerated time-to-market, reduced total-cost-of-ownership, product longevity and the best possible overall application with leading-edge, highest reliability embedded technology

Kontron is a listed company. Its shares are traded in the Prime Standard segment of the Frankfurt Stock Exchange and on other exchanges under the symbol "KBC".
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