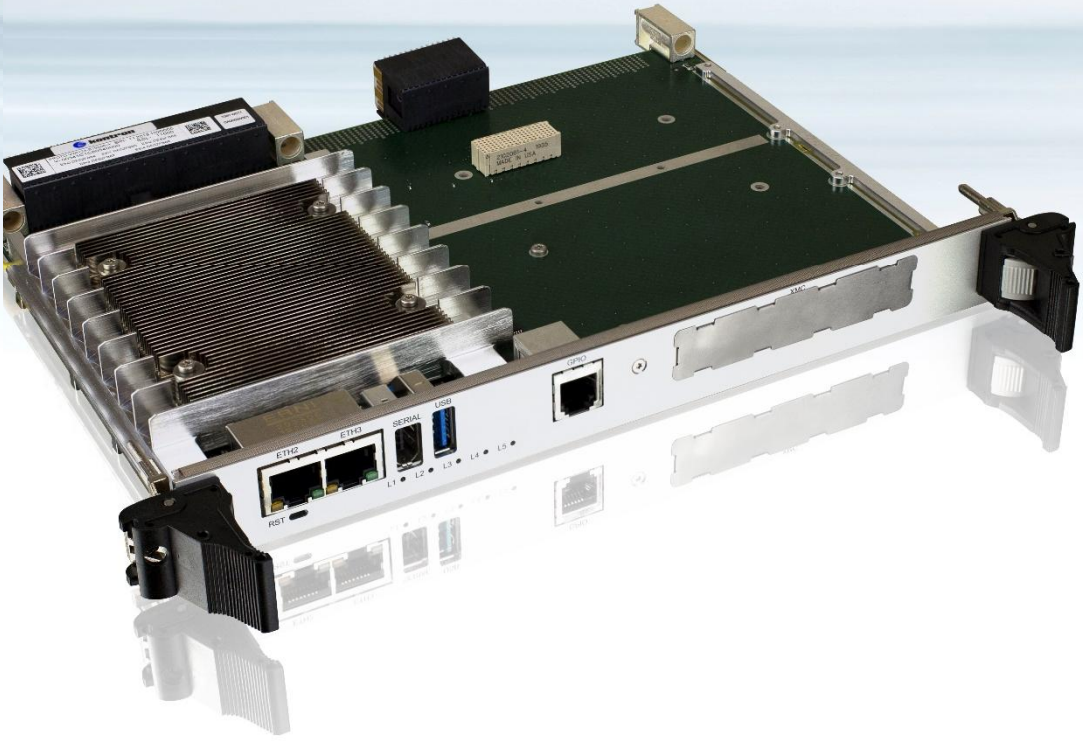
USER'S GUIDE



VX6124 New Generation

6U VPX Computing Node

D280304 -1.0 – March 2023

POSSIBILITIES START HERE kontron S&T Group

VX6124 - User's Guide

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1.0	Initial version.	04-2023

Customer Support

Please contact our support team at support.KFR@kontron.com

Customer Service

As a trusted technology innovator and global solutions provider, Kontron extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly-experienced support enables Kontron to provide exceptional peace of mind to build and maintain successful products.

For more details on Kontron's service offerings such as: enhanced repair services, extended warranty, Kontron training academy, and more visit http://www.kontron.com/support-and-services/services.

Customer Comments

If you have any difficulties using this user guide, discover an error, or just want to provide some feedback, contact Kontron support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user guide on our website.

Symbols

The following symbols may be used in this user guide

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
NOTICE	NOTICE indicates a property damage message.
	**Electric Shock!** This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	**ESD Sensitive Device!** This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	**HOT Surface!** Do NOT touch! Allow to cool before servicing.
	**Laser!** This symbol informs of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol indicates important information which must be read carefully.
	This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!

Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

General Instructions on Usage

In order to maintain Kontron's product warranty and CE compliance, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty and CE compliance.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements where possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled.

Final disposition of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

Environmental protection is a high priority with Kontron.
Kontron follows the WEEE directive
You are encouraged to return our products for proper disposal.

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

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1/ Introduction

The Kontron VX6124 is a high end, low power, 6U VPX 16 Arm® Core blade extending Kontron VPX portfolio of commercial –off-the-shelf computing node segment to focus on signal processing domain.

Featuring QorIQ® Layerscape® LX2160 communication processor with excellent performance of 200k+ DMIPS and 40G Ethernet connectivity, the VX6124 is ideal for applications requiring outstanding bandwidth and digital security. This new architecture can be used as a vehicle for 100G data plane system experiments (with Kontron VX6940 40G/100G switch for example).

The VX6124 is built around the LX2160A processor equipped with 16GByte of DDR4 memory is thermally and mechanically designed to optimize the use of Kontron XMC-GPU91 Radeon™ E9171, which adds to the massive computing power offered by the main CPU, another 1.2 TFlops of computing power via its eight compute units. The architecture boasts a direct x8 PCIe gen3 link to the XMC slot, giving a possibility of 8 GByte/s data bandwidth with the mezzanine silicon.

The Layerscape LX2160A delivers the high-performance needed for compute-intensive networking applications. Equipped with sixteen Arm®v8 Cortex®-A72 CPU cores, this processor supports up to 100 Gbit/s Ethernet, dual DDR4 memory controllers with ECC, @2133 MT/s, high speed configurable Serdes I/O lanes for flexibility (100G Ethernet and 1x PCIe x4 or mixed) and switch function enabling multiple ports Ethernet network.

The VX6124 fits a small power budget to enable efficient use of a mezzanine coprocessor (such as Kontron XMC-GPU91). With the LX2160A processor speed set to 2.2 GHz, the VX6124 power budget does not exceed 45 Watts while offering the performance of 253.4k DMIPS (7.2 DMIPS/MHz/A72core) /154.53k CoreMark (4.39 CM/MHz/A72core)

The VX6124 provides standard front I/O such as two 1000BASE-T ports, one USB3.0 port, Serial line port and GPIOs. In addition to 40Gb Ethernet data plane and 10Gb Ethernet control plane ports matching the requirement of VITA65 / OpenVPX architecture, the VX6124 offers extra backplane I/O capabilities such as 10GBASE-KR, 1000BASE-T, USB2.0/3.0 and 4 x Gen2 PCI Express ports.

The VX6124 embeds a MLC 5.1 eMMC device offering 32GB of onboard storage memory.

The VX6124 board comes with u-boot firmware and Yocto Linux. It is covered by Kontron's long term supply program, which guarantees customers multi-year supply of the product beyond its active life.

Figure 1: VX6124 Overview

1.1. Manual Overview

1.1.1. Objective

This guide provides general information, hardware instructions, operating instructions and functional description of the VX6124 board. The onboard programming, onboard firmware and other software (e.g. drivers and BSPs) are described in detail in separate guides (see section 1.7 "Related Publications").

This hardware technical documentation reflects the most recent version of the product. The "Release Notes" (see section 1.7"Related Publications") might help to keep track of potential evolutions.

Functional changes that differ from previous version of the document are identified by a vertical bar in the margin.

1.1.2. Audience

This guide is written to cover, as far as possible the range of people who will handle or use the VX6124, from unpackers/inspectors, through system managers and installation technicians to hardware and software engineers. Most chapters assume a certain amount of knowledge on the subjects of single board computer architecture, interfaces, peripherals, system, cabling, grounding and communications.

1.1.3. Scope

This guide describes the VX6124-SA/WA variants of the VX6124 new generation series, it does not describe the VX6124 with E.C. Level lower than 20000 (see Hardware Release Note documentation for detail).

1.1.4. Structure

This guide is structured in a way that will reflect the sequence of operations from receipt of the board up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

- Chapter 1 - Introduction (this chapter)
- Chapter 2 - Installation
- Chapter 3 - Additional Board Features
- Chapter 4 - Physical I/O
- Chapter 5 - Power and Thermal Specifications

1.1.5. Terminology, Definitions and Abbreviations

Terminology

In this document, the term VX6124 will be specifically associated to the 6U VPX board including VX6124 modules.

Abbreviations

TBD	To Be Defined. Information not available at the time this document was released.
TDP	Thermal Design Power

1.2. VPX Overview

VPX (VITA 46) specifications establish a new direction for the next revolution in bus boards. VPX is an ANSI standard which breaks out from the traditional connector scheme of VMEbus to merge the latest in connector and packaging technology with the latest in bus and serial fabric technology. VPX combines best-in-class technologies to assure a very long technology cycle similar to that of the original VMEbus solutions. Traditional parallel VMEbus will continue to be supported by VPX through bridging schemes that assure a solid migration pathway.

For further information regarding this standard and its use, visit the home page of the VITA - Open Standards, Open Markets (http://www.vita.com)

1.3. Board Overview

1.3.1. Main Features

NXP QorIQ® 'Layerscape®' LX2160A Architecture

The Layerscape LX2160A 'System on a Chip' (SoC) is equipped with sixteen Arm®v8 Cortex®-A72 CPU cores, 28 GHz SerDes technology and low FinFET power, this processor supports up to 100 Gbit/s Ethernet and the PCIe Gen3 technology. The wire rate I/O processor has 18 integrated MACs including dual 100 Gbit Ethernet ports and a 130 Gbit/s L2 switch. Every Arm®v8 Cortex®-A72 is associated with a 128-bit NEON™ SIMD engine.

The QorIQ LX2160A running at 2.2 GHz with ECC-protected 8Mbyte L2 cache memory embeds a dual DDR4 memory controllers with ECC up to 3200MT/s.

Soldered DDR4 Memories with the Support of ECC

The processor accesses two memory-channels (72-bit) having a total size up to 32 GB. The DDR4 memory technology used operates up to 3200 MT/s. An 8-bit ECC memory is implemented to detect and correct errors.

Numerous Storage Interface and Non Volatile Memories

The following storage features are available:

- An onboard eMMC 5.1 Flash with 32GB capacity (Multiple Levels Cell).
- Redundant 512 Mbits serial NOR flash memories are used to store firmware code.
- Two serial 256 Kbits EEPROMs are dedicated to system and VPD data storage.
- A 1 Mbits ferroelectric, non-volatile random-access memory allows the backup of critical data when the board is powered off. This 1 Mbits ferroelectric RAM is a user memory device.

All the Flash and non-volatile memories onboard have a write protect mechanism taking into account the NVMRO (Non-Volatile Memory read Only) VPX signal. For further details, see section 3.7 "Write Protect Mode".

Extensive I/O Connectivity

The VX6124 provides:

- Two 40G or 100GBASE-KR4 data plane interfaces on P1 depending on SerDes 1 configuration. For further detail about SerDes configuration, refer to Table 31: SerDes 1 RCW configuration, page 58
- One 4x PCI express gen2 expansion plane interface on P2,
- Two 10/100/1000BASE-T(X) Ethernet interfaces; two on front, or one on front and one on rear,
- Two 10GBASE-KR control plane interfaces; one on P1 and one on P4.
- Up to three EIA-232 serial lines and up to one EIA-422/485 serial line,
- One maintenance port,
- Eight general purpose I/Os (GPIO),
- Up to three USB links,

Legacy Compatibility

The VX6124 has been design to offer rear legacy I/O compatibility with Kontron's line of x86 and Power VPX SBCs, supporting the same Rear Transition Module. The net effect of this fit form function compatibility is to allow our customers an easy line replacement policy of the SBC in deployed systems.

Software

Kontron is one of the few compact PCI, VME and VPX vendors providing in-house support for most of the industry-proven real-time operating systems that are currently available.

Thanks to its close relationship with the software editors, Kontron is able to locally produce and support BIOS, BSPs and drivers for the latest operating system revisions thereby taking advantage of the changes in technology which follow silicon evolution.

Finally, Kontron offers to its customer owners of a maintenance agreement a hotline software support and regular software updates.

A dedicated web site is also available for online updates and release downloads.

The VX6124 is delivered with the Open Source U-BOOT firmware.

The VX6124 supports the Open Source Yocto framework for creating Linux distribution for embedded applications.

Contact Kontron for further information regarding other operating systems and software support.

10-years Long Life Cycle

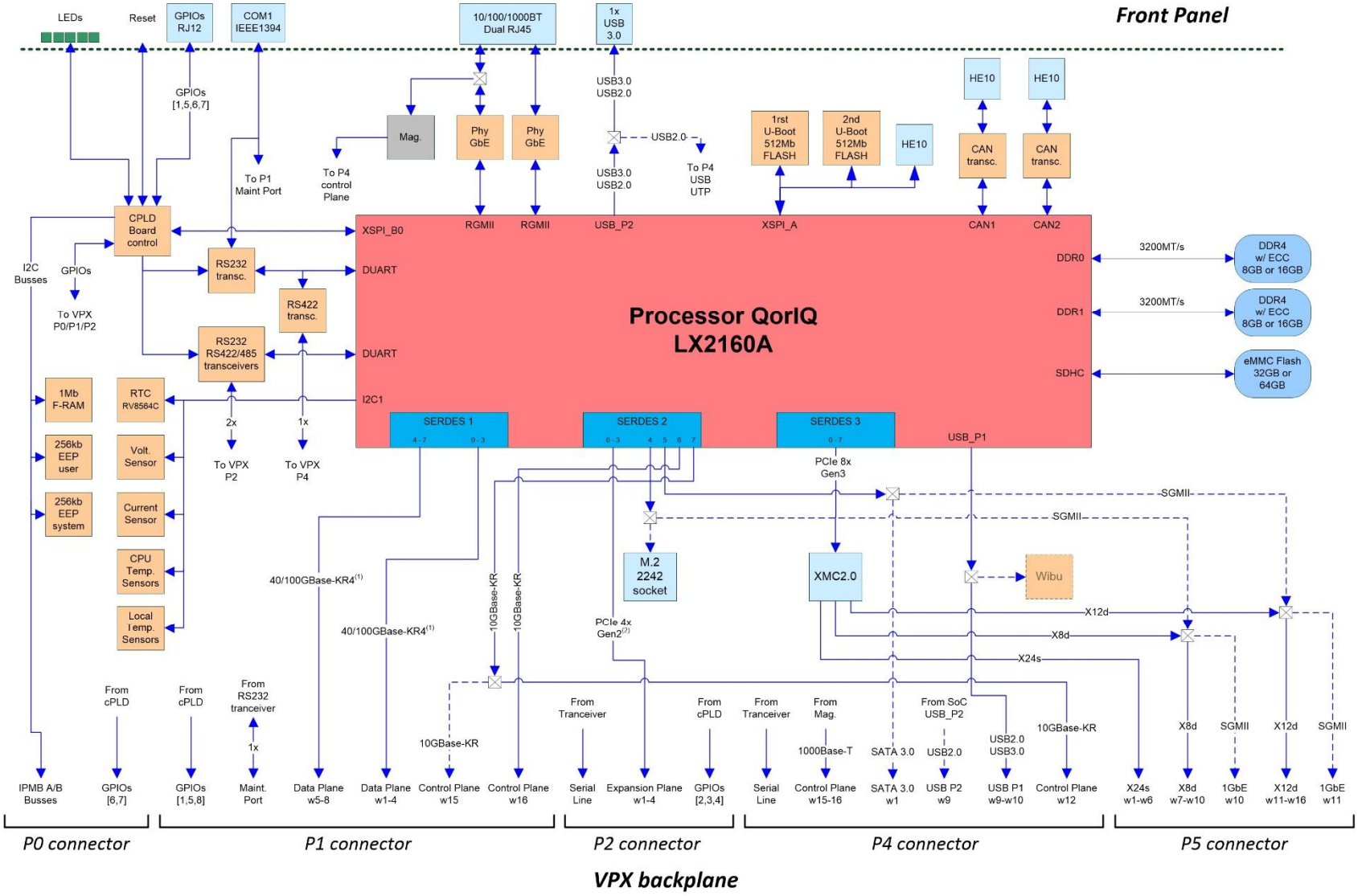
Investing in a new project is always a challenge and risky. Maximizing the lifetime of an application is therefore a critical issue when it comes to saving development investments.

The VX6124 has been designed with long life cycle components. Beyond the use of standard commercially available components, Kontron offers longevity of supply services (LTS) which are designed to make the VX6124 available for over 15 years.

A comprehensive Health Management is optionally available to support easy field maintenance. All this makes the VX6124 the ideal candidate for long term programs.

1.3.1. Block Diagram

Figure 2: VX6124 Functional Block Diagram



Note:
(1) Data plane lanes depend on SerDes 1 configuration. Configuration 13, 20, 18 and 21 are available on VX6124 depending on build option.
(2) Expansion plane lanes depend on SerDes 2 configuration. Configuration 13, 20 and 21 are available on VX6164 depending on build option.

1.3.2. Ordering Information

Table 1: VX6124 Order Code

Environmental Class	Standard Order Codes	Description
SA / Air Cooled	VX6124-SAFF-1020000	6U Single slot 5HP (1") VPX SBC -Air-Cooled 'SA' (0°C to 55°C) - Soldered 32GB eMMC Flash - Standard 6U IO profile - No Secure element - No PBIT **Processor type:** LX2160A sixteen ARM A72 2.2GHz QorIQ LayerScape **Memory size:** 16 GB soldered SDRAM with ECC, 3200MT/s

Table 2: Associated Product Order Codes

Environmental Class	Standard Order Codes	Description
SA / Air Cooled	1064-4995	Serial Console Cable Adapter

1.3.3. I/O Interfaces

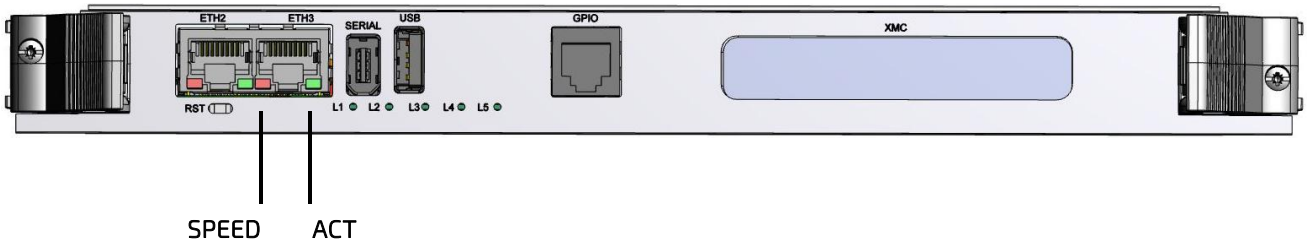
- Front Interfaces

Figure 3: VX6124 Front Panel I/O Interfaces

Table 3: Front I/O Interfaces

FUNCTION	DESCRIPTION	SEE ALSO
Serial Ports	1x simplified EIA-232 UART interface for CPU on IEEE1394 connector (maintenance port).	Section 4.1.1 for Pin Assignment
Gigabit Ethernet	Two 10/100/1000BASE-T(X) ports on RJ45	Section 4.1.2 for Pin Assignment
USB	USB 2.0 or USB 3.0 interface on USB type A connector	Section 4.1.3 for Pin Assignment
GPIO	RJ12 connector for GPIO signals	Section 4.1.4 for Pin Assignment
Reset	Reset push button	
LEDs	5 LEDs reporting the board CPU health status and activity	Section 4.3.1 for LEDs Description

Figure 4: Reset Button and LEDs



Rear Interfaces

Figure 5: VX6124 Rear I/O Distribution

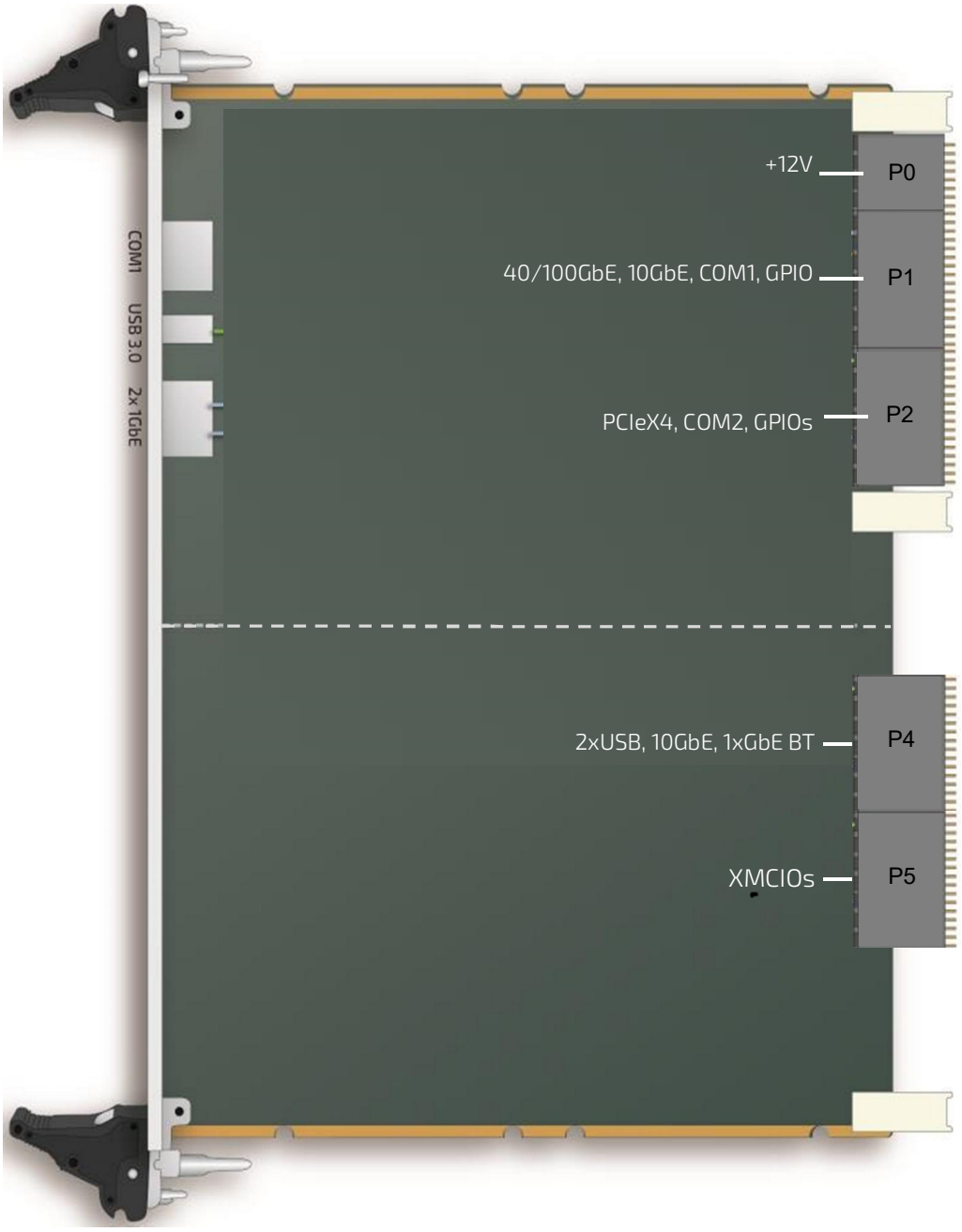


Table 4: Rear I/O Interfaces

FUNCTION	DESCRIPTION	SEE ALSO
Gigabit Ethernet	▸ 2 data plane 40 or 100GBASE-KR4 on P1 connector (SerDes 1 configuration 20 or 13) ▸ 2 control plane 10GBASE-KR on P1 and on P4 VPX connector ▸ 1 control plane 1000BASE-T on P4 VPX connector (exclusive with one of both 1000BASE-T on front panel)	Section 4.3 for VPX Connectors Description
PCI Express	▸ 1 expansion plane x4 PCIe gen 2 on P2 VPX connector	
USB	▸ 2 USB 2.0 and 1 USB 3.0 links on P4 VPX connector	
Serial	▸ 1 maintenance port simplified EIA-232 (or 3.3V level signaling) on P1 VPX connector. ▸ 2 simplified EIA-232 serial lines or 1 EIA-422/485 serial line on P2 (using dynamic configuration)	
GPIOs	▸ 3 GPIOs on P2 ▸ 1 GPIO on P1 (also used as MASKABLE RESET) ▸ 2 additional GPIOs on P1 exclusive with GPIOs on front panel	
Utilities	On P0 and P1: SYSRESET, SYSCON, 6 Geographical Addresses	
I2C	IPMB-A/B I2C busses	
Clocks	25MHZ REFCLK, no AUX_CLK	
Power Supplies	VS1=12V; VS2 not used; VS3=5V not used +12V_AUX is optional in VITA 46 and not connected on VX6124. -12V_AUX is optional in VITA 46. It is only connected to XMC slot. 3.3V_AUX is mandatory in VITA 46. However, if absent, it will be generated internally.	

Peripheral Connectivity

Table 5: Peripheral Connectivity

	VX6124		
	Front Panel	On-board	Backplane
Gigabit Ethernet	Y (up to 2)	-	Y (up to 1)
10Gbit Ethernet	-	-	Y (x2)
40/100Gbit Ethernet (1)	-	-	Y (x2)
USB2.0	Y (x1)	-	Y (up to 2)
USB3.0	Y (x1)	-	Y (x1)
COM1	Y	-	Y
COM2	-	-	Y
COM4	-	-	Y
GPIOs	Y (up to 4)	-	Y
LED	Y (x5)	-	-
Reset Button	Y	-	-
SMB	-	-	Y
PCIe 8x (XMC)	-	Y	-
PCIe 4x (expansion plane)	-	-	Y

(1) Depending on SerDes 1 configuration.
In configuration 13, 2x 100Gbit Ethernet interfaces are available on backplane.
In configuration 20, 40Gbit Ethernet interfaces are available on backplane.

1.3.4. Components Layout

Figure 6: VX6124 Components Layout (Top view)

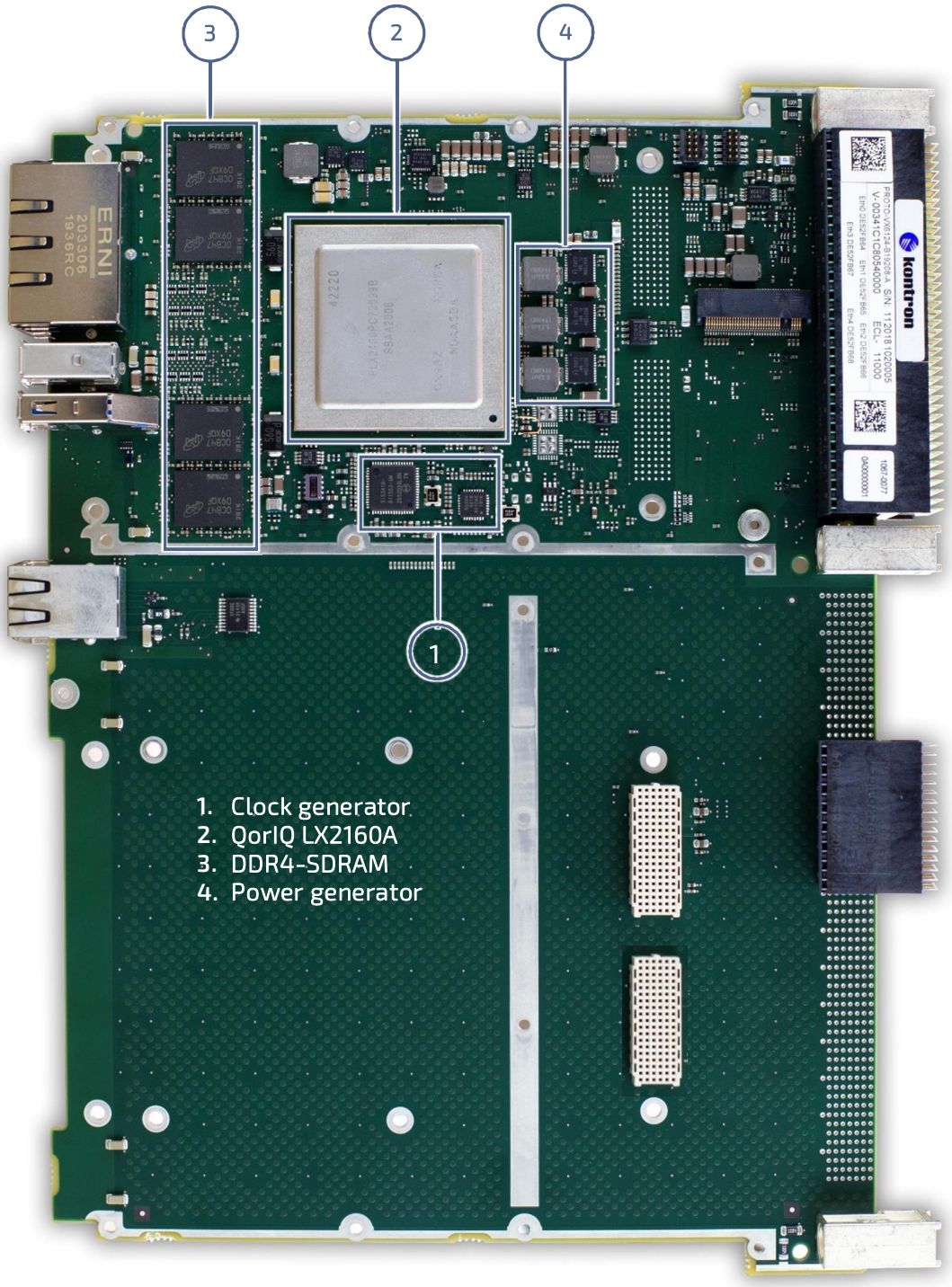
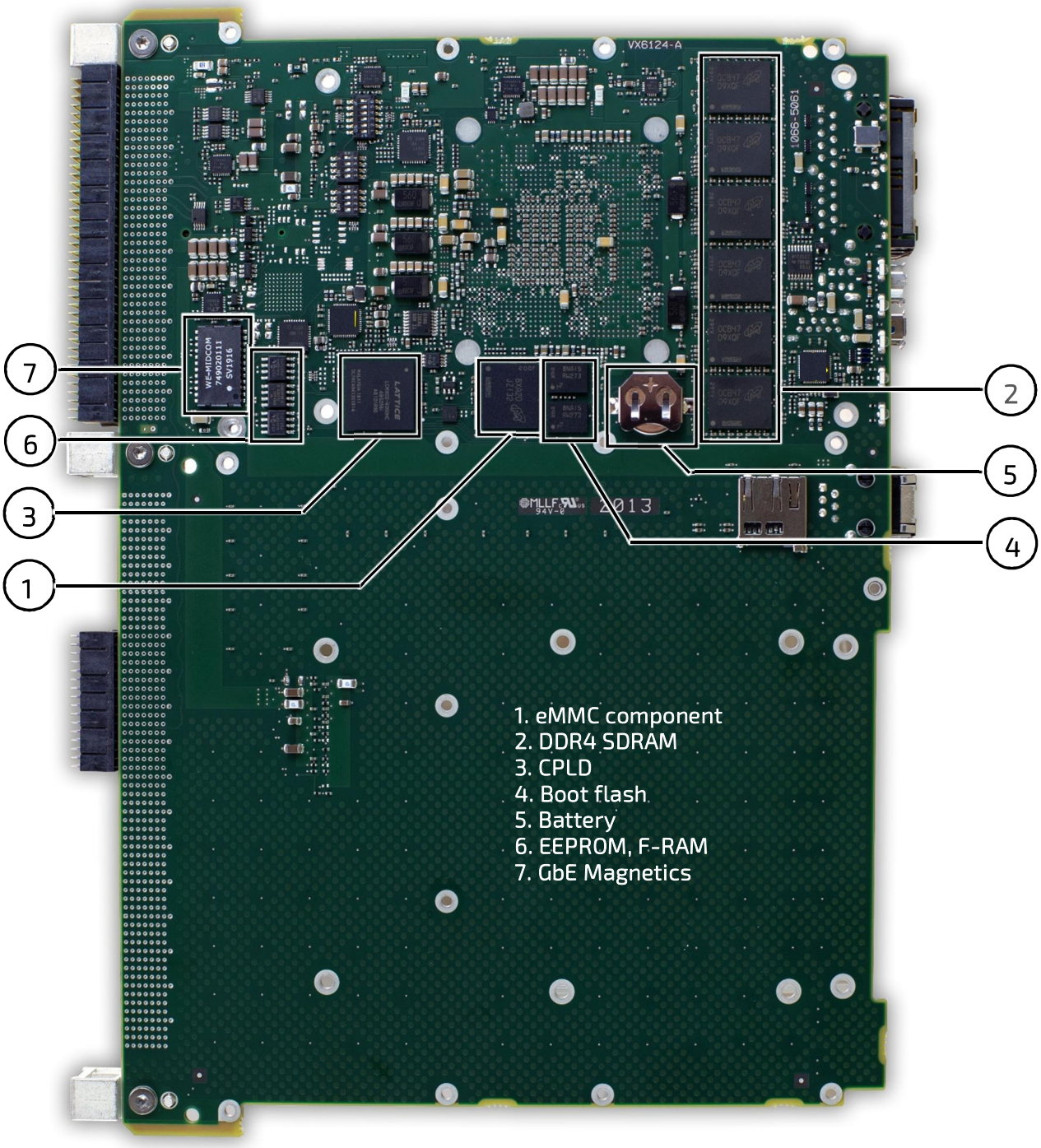


Figure 7: VX6124 Components Layout (Bottom view)



1.3.5. Technical Specification

This section sums up the main specificities of the VM6124 board:

Table 6: VX6124 Main Characteristics

Form Factor	
Form Factor	6U VPX x 160mm, slot pitch: 1.00 inch according VITA 48.1 Type 2
SoC : QorIQ Layerscape	
Processor	One NXP QorIQ Layerscape LX2160A 16-core 64-bit ARM® Cortex®-v8 A72 based processor speed up to 2.2GHz. 8 MB L2 cache Neon SIMD Co-processor Power dissipation lower than 30W. 16-nanometer silicon technology.
Memory Controller	Integrated two 72 bits DDR4 memory controllers with ECC support, up to 3200 MT/s.
PCI Express Interface	4 x lanes 5 GT/s gen2 PCIe on P2 connector
USB	1 USB 2.0 port on P4 or front panel (depending on software setting) 1 USB 2.0 port on P2 1 USB 3.0 on P2 connector 1 USB 3.0 on front panel connector
Ethernet Controllers	Two Gigabit Ethernet controllers using RGMII Interface
SERDES	24 SERDES lanes. Refer to section 4.3 for available SerDes configuration
eMMC Controller	Compatible with the MMC system specification version 5.1
XSPI	2 flash XSPI (512 Mbits each) 1 bus on XPSI connector
DUART	2 DUART interfaces offering up to 4 simplified Tx/Rx serial lines
CAN bus	2 CAN FD bus to on-board connectors (depending on build option)
Package	40 mm x 40 mm, 1 mm pitch, 1517 pins FC-PBGA
Memory / Storage	
System Memory	32 GB DDR4 SDRAM at 2133 MT/s, two memory channel. 16 GB DDR4 SDRAM at 3200 MT/s, two memory channel.
XPI Flash	Firmware Boot Device, 2x 512 Mbytes.
eMMC Flash	32GB 4-bit eMMC 5.1 MLC flash
F-RAM	F-RAM 1 Mbit of non-volatile ferroelectric RAM
EEPROM	1 serial 256 Kbit EEPROM dedicated to VPD data 1 serial 256 Kbit EEPROM dedicated to system data

On-board Controller	
Watchdog	5 watchdog timers with configurable timeout counter with timeout periods from 0.5 to 128 seconds, generates IRQ or reset or IRQ/reset cascaded (cPLD implementation) cPLD watchdog also available.
Ethernet PHY	2 Ethernet PHYs offering Ethernets 10/100/1000 BASE-T(X) port which are connected to the SoC through 2x RGMII links.
System CPLD	1 CPLD Board controller for power sequencing, reset handling, monitoring, failure detection, VPX I2C communication. Provides configuration/status registers on IFC interface
On-board Interconnection	
XMC	XMC2 VITA61
CAN	2 x CANbus FD interface on HE10 10-pins connectors
XSPI	1 x XSPI on HE10 12-pins connector
System Rear Interconnection	
Ethernet	Default rear connection: 2 x 40 or 100G BASE-KR4 on P1 depending on SerDes configuration 2 x 10G BASE-KR on P1 and P4 1 x 10/100/1000Base-T(X) on P4
USB Ports	2 x high-speed USB Ports on P2 1 x super-speed USB Port on P2
Serial Ports	2 x RS232 Serial Ports or one EIA-422/485 on P2 1 x Maintenance Ports on P1
GPIO	4 x GPIOs on rear panel (1 x GPIO on P1, 3 x GPIOs on P2).
VPX SMB buses	Two SMB 100KHz buses from cPLD: one master/slave and one master only available on P0.
Front Interface	
Gigabit Ethernet	2 x 10/100/1000Base-T(X) on dual RJ45 connectors.
Serial Port	1 x RS232 UART interfaces, IEEE1394 connector.
USB Port	1 x USB2.0/USB3.0 port for storage or keyboard/mouse
Reset	One Reset button and Shelf Manager control (SMB command on VPX)
LEDs	Five Bicolor LEDs on front panel.
GPIO	4 x GPIOs available on a RJ12 connector

Various Interfaces	
CPU debug Interface	JTAG debug connector for CodeWarrior TAP
Board Temperature	TMP on-chip thermal sensor and remote processor thermal diode. One for processor temperature and one for board temperature
Miscellaneous	
Battery	CR1220 on board socket,
RTC	External RTC module RV8564C2 with I2C bus
Backplane Power Supply	VS1: +12V +5%/-5% only fully protected by fuse. +3.3V +5%/-5% standby optional voltage VS2 and VS3 not used -12V standby optional voltage used for XMC
Power Consumption	About 50W without mezzanines, without peripherals/devices. This does not include the power dissipation due to the DC/DC efficiency when mezzanines, options and external peripherals/devices are used.
Operating temperature Range	1.0'' SA: 0°C to +55ºC with 1 slot 1.0" passive module heat sink, forced system airflow (depending on the processor frequency)
Humidity	90% RH (non condensing)
Options / Companion board	
CodeWarrior TAP	CPU JTAG emulator probe

1.4. Environmental Specifications

Table 7: VX6124 Environmental Specifications

Cooling Method	Convection
Operating Temperature	0°C to +55°C
Storage Temperature	-40°C to +85°C
Vibration Sine (Operating)	20-500 Hz - 2g Acceleration/Frequency Range
Random vibration	5Hz to 100Hz PSD = $0.04g^2/Hz$
Shock (Operating)	20g/11ms Peak Accel./ Shock Duration Half Sine
Altitude (Operating)	-1,500 to 60,000 ft
Relative Humidity	90% non-condensing

1.5. Board Weight

Table 8: VX6124 Weights

Board Weight	SA /WA
VX6124	805 g

1.6. MTBF Data

Calculations are made according to the standard MIL-HDBK217F-2 for following types of environment:

- Ground Benign (GB)
- Air Inhabited Cargo (AIC)
- Naval Sheltered (NS),
- Air Rotary Wing (ARW)

VX6124 MTBF Data

Table 9: VX6124 MTBF Data

MTBF	MILHDBK217F					
	GB (HOURS)		NS (HOURS)		ARW (HOURS)	AIC (HOURS)
	25 °C	40 °C	25 °C	40 °C	55 °C	40 °C
VX6124	tbd	tbd	tbd	tbd	tbd	tbd

1.7. Related Publications

The following publications contain information relating to this product:

Table 10: Related Publications

PRODUCT	PUBLICATION
Standard	
ANSI/VITA 46.0	VPX Baseline Standard - ANSI/VITA 46.0-2019
ANSI/VITA 46.6	Gigabit Ethernet Control Plane on VPX, Feb 2013
ANSI/VITA 46.9	XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules, March 2018
ANSI/VITA 46.10	Rear Transition Module for VPX - ANSI/VITA 46.10-2009
ANSI/VITA 46.11	System Management on VPX, June 2015
ANSI/VITA 65	OpenVPX™ System Specification ANSI/VITA 65-2019
ANSI/VITA 65.1	OpenVPX™ System Standard – Profile Tables, Nov. 2019
ANSI/VITA 48.1	Mechanical Specification for Microcomputers using REDI, Air cooling, July 2010
ANSI/VITA 48.2	Mechanical Specifications for Microcomputers using REDI Conduction Cooling Applied to VITA VPX
ANSI/VITA 47	Environmental, Design and Construction, Safety, and Quality for Plug-In Unit
Serial ATA	Serial ATA 3.0 Specification, revision 3.0
Mini PCIe	PCI Express Mini Card Electromechanical Specification, Revision 2.0, April 21 2012
Hardware	
VX6124 Boards	VX6124 EFT Release Notes D245265
Firmware	
VX6124 Board	VX6124 U_Boot User Manual TBD
PBIT	
VX6124 Board	VX6124 PBIT Software User Guide D249200
Software	
VX6124 Board	VX6124 Yocto Linux Release Notes D235834

2/ Installation

The VX6124 has been designed for easy installation. However, the following standard precautions, installation procedures, and general information must be observed to ensure proper installation and to preclude damage to the board, other system components, or injury to personnel.

2.1. Safety Requirements

The following safety precautions must be observed when installing or operating the VX6124. Kontron assumes no responsibility for any damage resulting from failure to comply with these requirements.

Special care shall be taken while handling the board: the heat sink or heat frame can get very hot during operation. Do not touch the heat sink when installing or removing the board.

In addition, the board should not be placed on any surface or in any form of storage container before the board and heat sink have cooled down to room temperature

This board contains electrostatically sensitive devices. Observe the necessary precautions to avoid damage to your board:

Discharge your clothing before touching the assembly. Tools must be discharged before use.

- Do not touch components, connector pins or traces.
- We strongly recommend our customers to work in an environment equipped with anti-static workbenches with professional discharging equipment's

2.2. Board Identification

The VX6124 board is identified by labels fitted to the top side of the board.

The E.C. Level format is "xxxxxLy" where

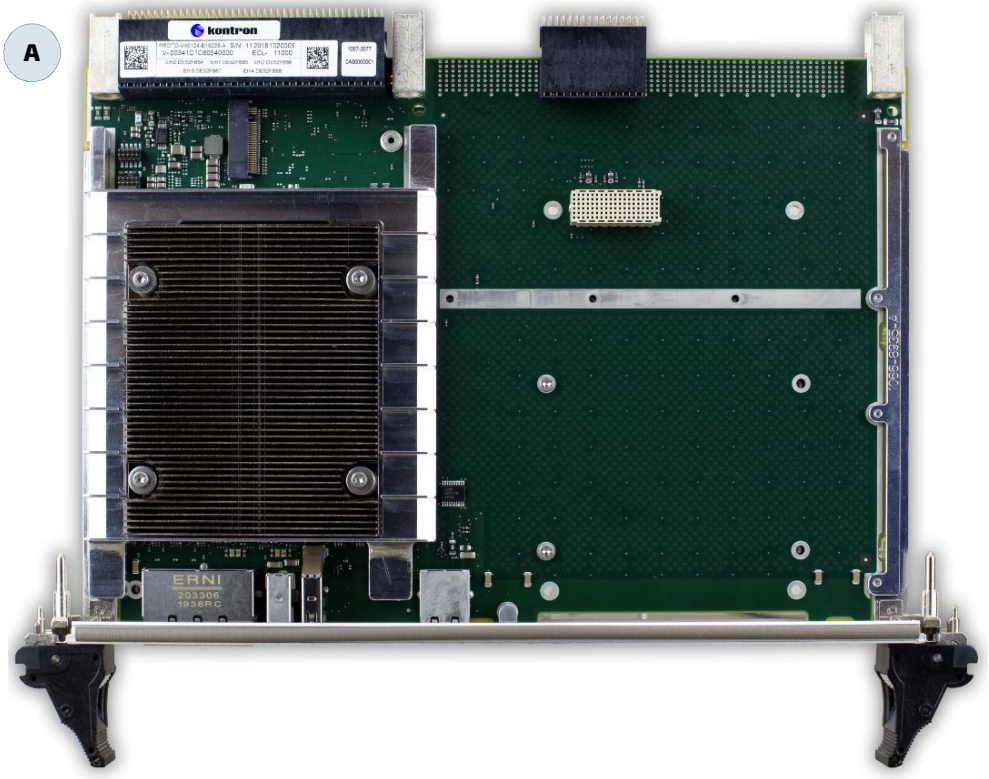
- The five digits "xxxxx" indicate the board E.C. Level (PCB revision included)
- "Ay" indicates the mechanical E.C. Level:
  - letter "A" is for the SA environment class
  - digit "y" gives the mechanical E.C. Level.

See also section "Vital Product Data" in "VX6124 U-Boot User Manual" – TBD to display the VPD information stored in VX6124 EEPROM.

Top Side

A "Identification" label: Order Code, Serial Number, Variant, E.C. Level
Ethernet MAC addresses

Figure 8: VX6124 Identification (Top Side)



2.3. Package Content

The VX6124 is packaged with several components. The packing contents of the VX6124 is the following.

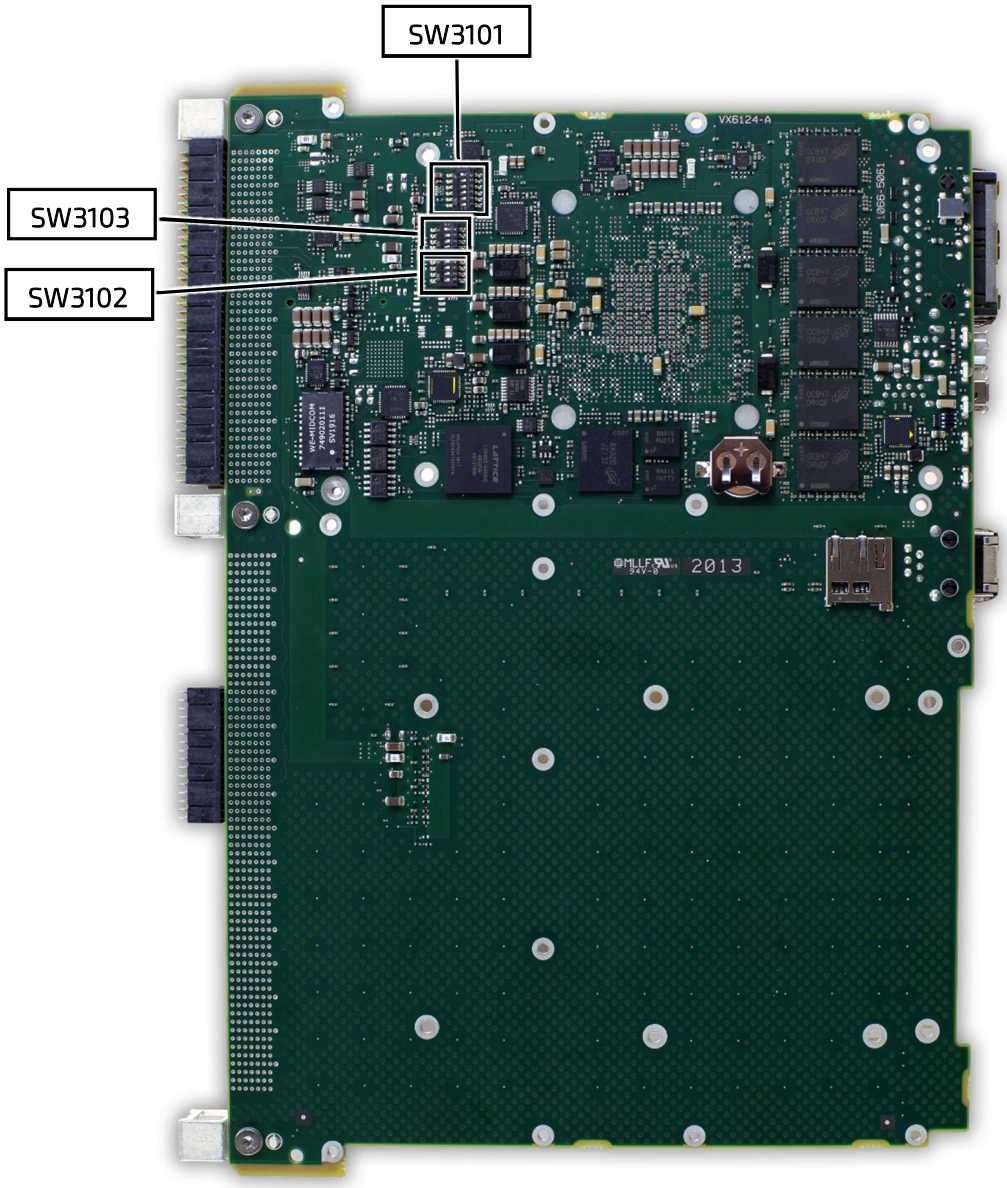
- CPU Module:
  - Order Code: see section 1.3.3 “Ordering Information":
- Serial Cable:
  - Order Code: see section 1.3.3 “Ordering Information".

Figure 9: Serial Cable

2.4. Board Configuration

2.4.1. Microswitches

Figure 10: VX6124 Board Configuration (Bottom view)



Three micros witches are available on the VX6124: SW3101, SW3102 and SW3103.

2.4.2. SW3101 Microswitch Description

Table 11: SW3101 Microswitch Description

FUNCTION	DESCRIPTION
1 - Factory Mode	OFF: Normal Mode ON: Factory Mode (force special config for factory tests)
2 – "VPD" (Vital Product Data)	OFF: protected under condition defined in section 3.7 - "Write Protect Mode" ON : unprotected (even if protection is requested by NVMRO) "VPD" domain controls devices storing factory data : VPD EEPROM
3 – "SYS" domain Write Protection	OFF: unprotected under condition defined in section 3.7 - "Write Protect Mode" ON : protected "SYS" domain controls devices storing runtime data : System (OS) EEPROM, XMC NVMRO
4 - "USER" domain write protection	OFF: unprotected under condition defined in section 3.7 - "Write Protect Mode" ON : protected "USER" domain controls devices impacted by a software update : FRAM (Ferroelectric RAM), XSPI boot flashes, CPLD internal flash
5 – Reserved for fuse programming	Always keep this switch OFF
6 - Debug Mode	OFF : Normal Mode ON : Debug Mode (reset from CPU disabled, LEDs reporting power sequencer state)

See also section 3.7 "Write Protect Mode", page 46, for write protection level description and for knowing the protected devices.

2.4.3. SW3102 Microswitch Description

Table 12: SW3102 Microswitch Description

FUNCTION	DESCRIPTION
1 - System Boot Flash	OFF : boot on "main" XSPI flash ON : boot on "Rescue" XSPI flash for recovery purpose
2 – Firmware Failsafe Boot	OFF : Normal Mode ON : Start in failsafe mode using default CPLD and firmware configuration
3 – Reserved for Serial configuration	Keep this switch OFF
4 – NVMRO force off	OFF: NVMRO not forced to off (level 0) ON : force NVMRO off on backplane, also forcing it off on local board (useful if backplane does not have a switch to disable NVMRO)

2.4.4. SW3103 Microswitch Description

These switches are user defined and their state can be read by software through CPLD register @0xE

Table 13: SW3103 Microswitch Description

FUNCTION	DESCRIPTION
1 – User switch 1	Readback in register 0xE bit 4 (1 when ON)
2 – User switch 2	Readback in register 0xE bit 5 (1 when ON)
3 - User switch 3	Readback in register 0xE bit 6 (1 when ON)
4 - User switch 4	Readback in register 0xE bit 7 (1 when ON)

2.5. Initial Installation Procedures

The following procedures are applicable only for the initial installation of the VX6124 in a system. Procedures for standard removal operations are found in their respective chapters.

To perform an initial installation of the VX6124 in a system proceeds as follows:

1. Ensure that the safety requirements indicated in section 2.1 are observed.

CAUTION: Failure to comply with the instruction below may cause damage to the board or result in improper system operation.

2. Ensure that the board is properly configured for operation in accordance with application requirements before installing. For information regarding the power and thermal specification of the VX6124 see Chapter 5. For the installation of VX6124, specific peripheral devices and Rear I/O devices refer to the appropriate sections in current Chapter.

CAUTION: Care must be taken when applying the procedures below to ensure that neither the VX6124 nor other system boards are physically damaged by the application of these procedures.

3. To install the VX6124 perform the following:
   a. Ensure that no power is applied to the system before proceeding.
   b. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.

When performing the next step, DO NOT push the board into the backplane connectors. Use the ejector handles to seat the board into the backplane connectors

   c. Carefully insert the board into the slot designated by the application requirements for the board until it makes contact with the backplane connectors.
   d. Using the ejector handle, engage the board with the backplane. When the ejector handle is locked, the board is engaged.
   e. Fasten the front panel retaining screws.
   f. Connect all external interfacing cables to the board as required.
   g. Ensure that the board and all required interfacing cables are properly secured.

The VX6124 is now ready for operation. For operation of the VX6124, refer to appropriate VX6124 specific software, application, and system documentation.

2.6. Standard Removal Procedure

ESD sensitive Device! Precautions are listed in chapter 2.1

To remove the board from the chassis proceeds as follows:

1. Ensure that the safety requirements indicated in Section 2.1 are observed. Particular attention must be paid to the warning regarding the heat frame!

CAUTION: Care must be taken when applying the procedures below to ensure that neither the VX6124 nor system boards are physically damaged by the application of these procedures.

2. Ensure that no power is applied to the system before proceeding.
3. Disconnect any interfacing cables that may be connected to the board.
4. Unscrew the front panel retaining screws
5. Disengage the board from the backplane by first unlocking the board ejection handle, press the handle until the board is disengaged.
6. After disengaging the board from the backplane, pull the board out of the slot.

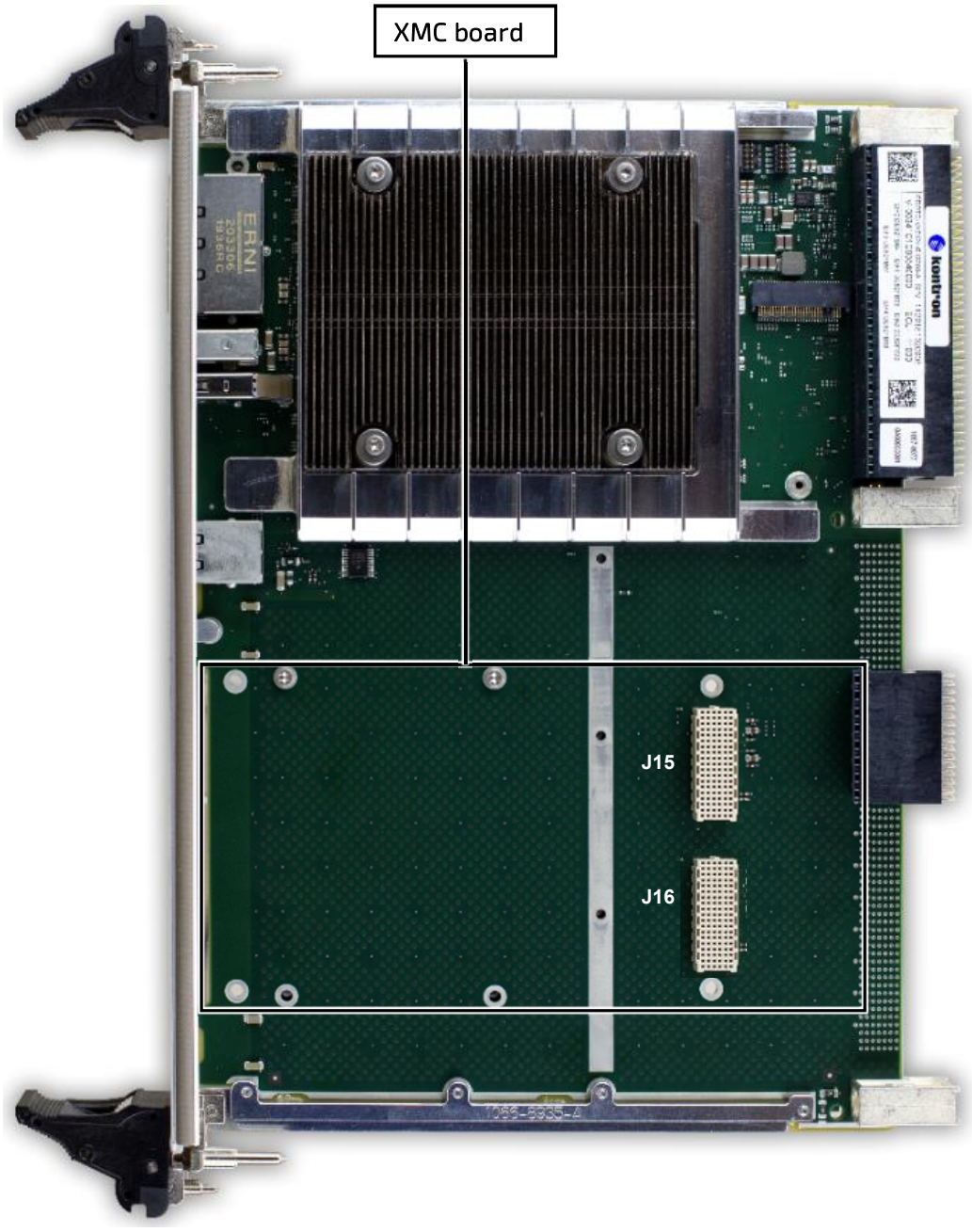
CAUTION: Due care should be exercised when handling the board due to the fact that the heat sink can get very hot. Do not touch the heat sink when changing the board.

7. Dispose of the board as required.

2.7. Installation of Peripheral Devices

The VX6124 is designed to accommodate a variety of peripheral modules whose installation varies considerably. The following chapters provide information regarding installation aspects and not detailed procedures.

Figure 11: VX6124 Peripheral devices on Top side



2.7.1. XMC Installation

Supported XMC type

The default XMC connectors are VITA 61 XMC 2.0 compliant and support x8 PCI-Express 3.0 interface. The VX6124 supports only one XMC slot.

The XMC stack is 12 mm.

XMC installation

ESD Sensitive Device! Precautions are listed in chapter 3.1

Apply "Loctite 222e" threadlock on each screw during re-assembling.

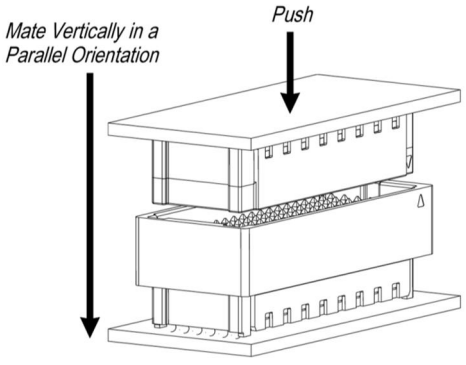
To install a XMC, proceed as follows (see detail in Figure 13):

1. If board is in the chassis, follow the procedure described in section 2.6, “Standard Removal Procedure”, page 35.
2. Remove the blank XMC front panel.
3. Replace the read standoffs of XMC by two M2.5x12 standoffs provided in bolt accessories.
4. Place the two XMC spacers on the VX6124 board in front of XMC bezel.
5. Engage the XMC bezel into the front panel of the VX6124. Align the XMC connectors. Press to fully engage the XMC in the VX6124.

⚠CAUTION

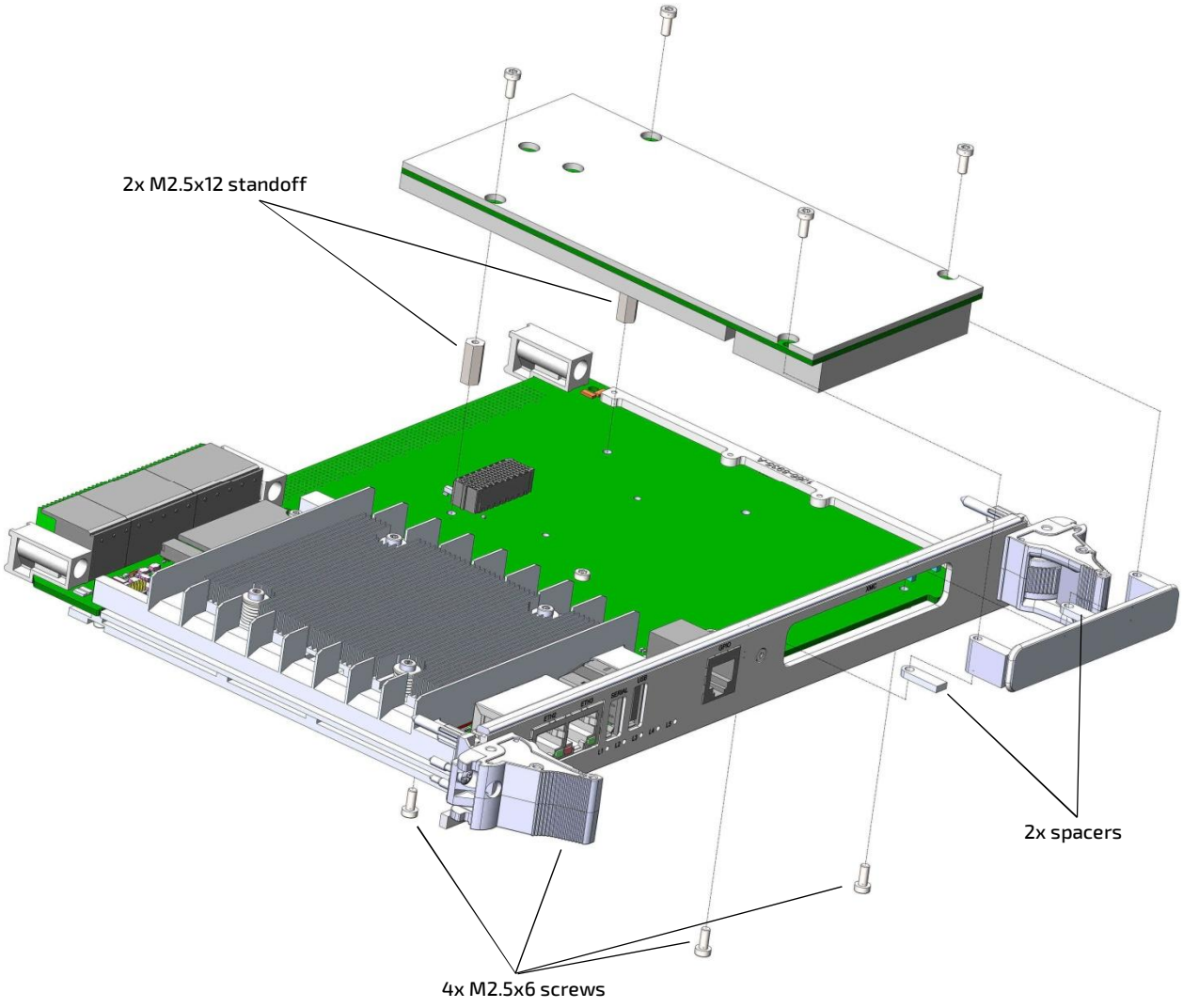
The XMC connectors should be mated straight. Align the connectors and when the keys start to enter the keyways, push at the approximate center of the connector into the mating connector until the face of the receptacle cover bottoms on the face of the plug. Because of the asymmetric keying, reverse mating is impossible (the key end of the receptacle cannot be inserted into the non-keyway end of the plug). Both connectors have a lead-in around the perimeter that will allow blind mating.

Figure 12: XMC module insertion



6. Screw the XMC in place using the four M2.5x6 screws.

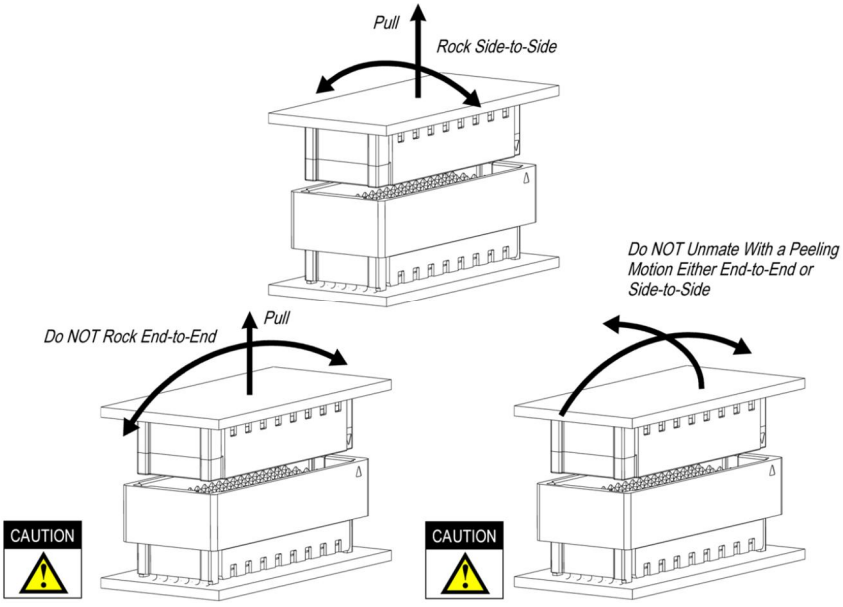
Figure 13: XMC Installation



Unmating

The XMC connectors can be unmated by pulling them straight apart or by "rocking" the connectors from side-to-side while pulling them apart. See Figure 14 for details.

Figure 14: XMC Module Removal



2.7.2. Battery Replacement

The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. The battery is used to run a time of day clock during the absence of power. Operation without the battery is possible but the date and time will not be retained in the absence of power. Alternatively the VBAT signal from P1-G3 can provide a 3.3V voltage from the backplane to retain the date and time.

Battery Part Number

Reference of the battery used on the VX6124: RENATA CR1220 MFR (-30/+70°C)

Battery Replacement

To replace the battery, proceed as follows:

1. If board is in the chassis, follow the procedure described in section 2.6, "Standard Removal Procedure", page 35.
2. Use a thin plastic tool to push the battery out of its holder.

NOTICE **Do not subject the holder to mechanical stress when inserting the tool to eject battery.**

3. Remove the battery.
4. Place the new battery into the socket with positive side (+) upwards and negative side (-) closest to printed circuit board

⚠CAUTION **Danger of explosion when replacing with wrong type of battery. Replace only with the same or equivalent type recommended by the manufacturer. The lithium battery type must be UL recognized.**

Do not dispose of lithium batteries in general trash collection. Dispose of the battery according to the local regulations dealing with the disposal of these special materials, (e.g. to the collecting points for dispose of batteries).

- **Battery Life**

The RTC circuit power consumption is specified at 500 nA, giving an expected duration of more than 8 years in the absence of external power. In case of storage temperature or operating temperature is higher than 55°C or lower than 0°C, the battery life is reduced to 7 years in worst case.

- **Battery Use**

Battery is used to save the date and the hour parameter of external RTC.

See also section 3.1, “RTC, Watchdog, Timers”, page 41. Firmware parameters are saved on system flash EEPROM.

2.8. Software Installation

The installation of all onboard peripheral drivers is described in detail in the relevant Driver Kit files or Board Support Packages (BSP).

The installation of an operating system is dependent of the OS software and is not addressed in this manual. Refer to appropriate OS software documentation for installation.

3/ Additional Board Features

3.1. RTC, Watchdog, Timers

3.1.1. Real-Time Clock (RTC)

The VX6124 offers a standalone, high-precision and low-power Real Time Clocks (RTC) component located on the QorIQ I2C bus (RV8564 by Micro Crystal).

Standby power supplied to the RV8564 RTC

When the VX6124 is powered off, the RTC is powered by the onboard battery and if present through the 3.3V_AUX rail or the VBAT rail of the VPX backplane.

To ensure data retention in the RV8564 RTC, VBAT must be set in the range [2.5V - 5.5V]. The maximum current drawn over the -40 °C/+85 °C temperature range is 500 nA (VBAT= 3 V, no I2C activity) or 550 nA (VBAT=5 V, no I2C activity).

Standalone low-power RTC RV8564

The RV8564C2/B RTC by Micro Crystal features an internal oscillator, date and time keeping module with programmable alarm, timer and interrupt functions. It has an ultra low-power consumption in time keeping mode: 250 nA, typical and 500 nA, maximum. Its stability is 20 ppm at 25 °C.

RTC management by Firmware and OS

At each startup, the Firmware retrieves the date and time information from the high-precision RV8564 RTC.

Any update of date and time in the Firmware settings will be done in RV8564 RTC.

Regarding the RTC management by the OS, the OS should use the high-precision RV8564 RTC driver.

Century flag

For compatibility reasons, the Firmware implements the century flag for the high-precision RTC as follows:

- Century Flag C = 0 for 1900-1999 years
- Century Flag C = 1 for 2000-2099 years.

The user should check that the OS driver implements the same convention.

3.1.2. CPLD Watchdog

In addition to the standard watchdog timer included within the QorIQ, the cPLD implements a hardware watchdog timer that can be used by the operating software to monitor the normal operation of the system.

It is enabled by software, and once enabled must be restarted at regular intervals. If not, its expiration sets off an interrupt (IRQ) to the local processor, a board reset or a board power-cycle.

The watchdog has the following features:

- timeout programmable from 1 to 511 clock periods, by steps of 2 periods
- clock periods of 1s or 1ms
- lock bit: when set, can only refresh (restart) the watchdog, but not change its settings
- 4 modes: timer, reset, interrupt or power-cycle
- restart counter: can manage the remaining number of resets or power-cycles done by the watchdog before giving-up.

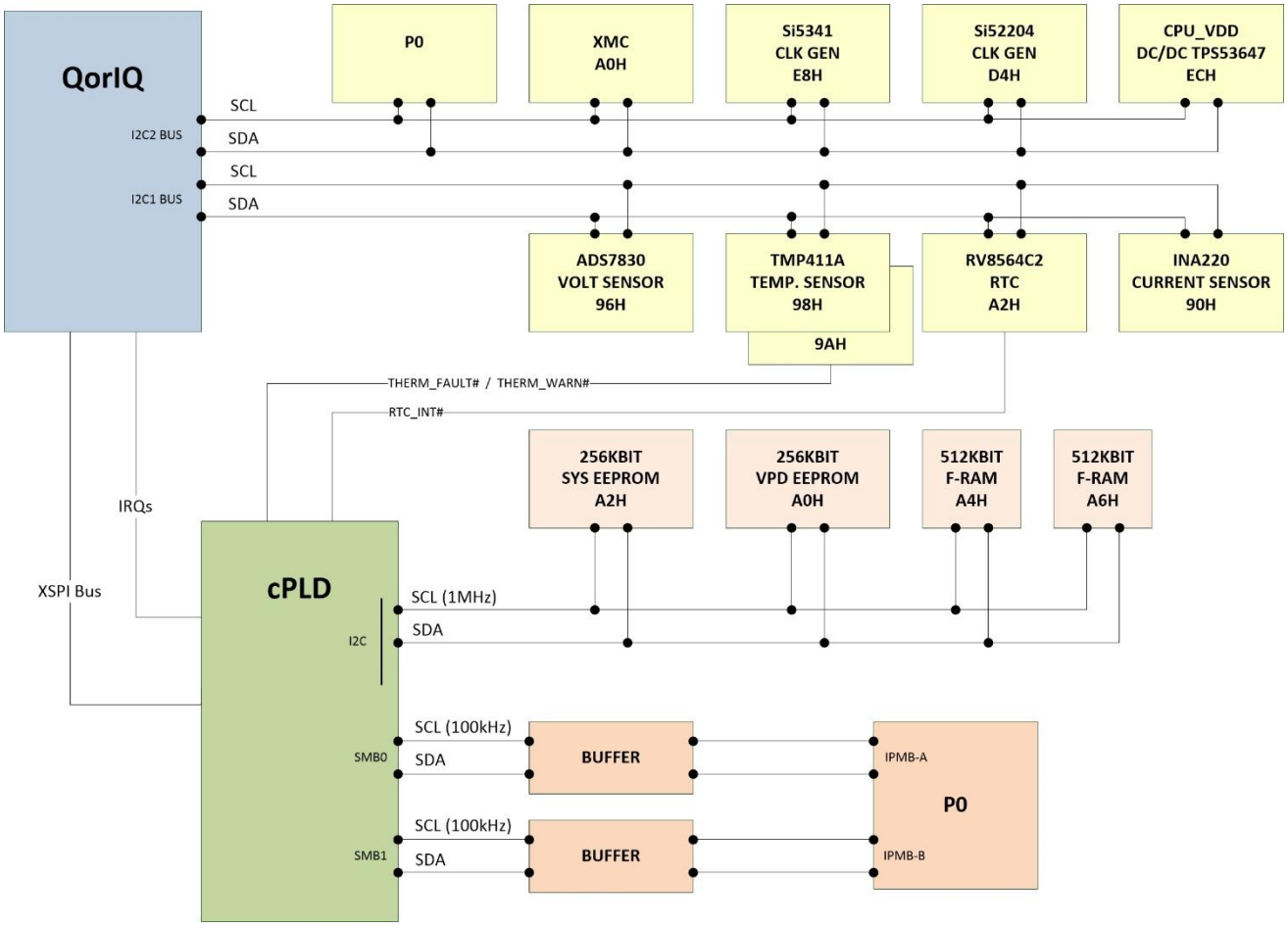
3.2. I2C Structure

The VX6124 features four I2C busses.

- The first two are attached to the QorIQ processor.
- The remaining I2C busses are handled by the CPLD device. The shows the component attached to the different I2C buses.

The I2C addresses shown in Figure 15: I2C Diagram are 8-bit values, which include a read/write bit. Shift one bit to the right to get the 7-bit addresses.

Figure 15: I2C Diagram



QorIQ I2C1 devices (100 KHz)

SLAVE DEVICES ON QorIQ I2C1 INTERFACE	SMBUS 7-BIT BASE ADDRESS (8-BIT BASE ADDRESS)	FEATURES
ADS7830	4BH (96H)	Voltage sensor
INA220	48H (90H)	CPU Current monitor
TMP411	4CH (98H)	CPU temperature sensor top
TMP411	4DH (9AH)	CPU temperature sensor bottom
RV8564-C2	51H (A2H)	External RTC Device

QorIQ I2C2 devices (100 KHz)

SLAVE DEVICES ON QorIQ I2C2 INTERFACE	SMBUS 7-BIT BASE ADDRESS (8-BIT BASE ADDRESS)	FEATURES
TPS53647	76H (ECH)	CPU VDD DC/DC
Si5341/40	74H (E8H)	Clock generator
Si52204	6AH (D4H)	Clock generator
XMC	50H (A0H)	XMC
P0 VPX		P0 VPX connector

cPLD I2C Bus (1 MHz)

SLAVE DEVICES ON CPLD SMBUS INTERFACE	SMBUS 7-BIT BASE ADDRESS (8-BIT BASE ADDRESS)	FEATURES
24FC256-I/SN VPD EEPROM	50H (A0H)	256 Kbits VPD EEPROM
24FC256-I/SN SYS EEPROM	51H (A2H)	256 Kbits SYS EEPROM
FM24V10-G	52H (A4H) / 54H (A8H) /	1 Mbits User FRAM

3.3. CPLD Features

The CPLD manages the following features:

- Power-on/off control
- Reset control
- Local environmental control/monitoring
- XSPI interface to processor
- I2C interfaces to local I2C bus, and backplane SMB busses (rear VPX P0).
- LEDs control
- Serial lines mode selection
- Serial VPD and user memories
- User and system GPIOs
- Internal registers that allow system management

cPLD Register

cPLD registers are accessible from CPU through XSPI bus. See cPLD registers overview in VX6124 Yocto Linux – Release Notes - D235834. Contact Kontron for a detailed description of the CPLD registers.

3.4. Serial Lines Additional Modes

The VX6124 features up to 3 serial lines in EIA-232 mode and up to 1 serial line in EIA-422/485, COM1, COM2 and COM4 in PC parlance.

- COM1: EIA-232 port on IEEE1394 front panel connector or on the rear P1 connector. For further detail about COM1 Maintenance Port front panel pin assignment, refer to section 4.1.1 page 49 - "Serial Connector – COM1".
- COM2: EIA-232/422/485 port on the rear P2 connector
- COM4: EIA-232 port on the rear P2 connector (exclusive with COM2 EIA-422/485 mode)

EIA-422/485 Serial line mode

Two simplified EIA-232 serial lines OR one EIA-422/485 serial line are available on P2 connector, as COM2 and COM4. See section 4.3.3 page 61 - "P2 Connector" for more information on pin assignments.

EIA-232 serial line mode is the default setting for COM2, but EIA-422/485 mode can also be set according to the following table:

Table 14: Serial Lines Additional Modes

MODE	P1 REAR CONNECTOR FRONT PANEL	P2 REAR CONNECTOR	REAR PIN ASSIGNMENT
Default	EIA-232: COM1 Maintenance Port	EIA-232: COM2, COM4	COM1 TXD: pin P1-G9 COM1 RXD: pin P1-G11 COM2 TXD: pin P2-G1 COM2 RXD: pin P2-G5 COM4 TXD: pin P2-G3 COM4 RXD: pin P2-G7
Optional mode COM2 : EIA-422/485	EIA-232: COM1 Maintenance Port	EIA-422/485: COM2	COM1 TXD: pin P1-G9 COM1 RXD: pin P1-G11 COM2 TXD+: pin P2-G3 COM2 TXD-: pin P2-G1 COM2 RXD+: pin P2-G7 COM2 RXD-: pin P2-G5

The EIA-232 or EIA-422/485 modes are selected using firmware commands by the user. When EIA-422/485 is selected on COM2, COM4 EIA-232 serial line is no longer available; it is exclusive with COM2 EIA-422/485 mode.

COM2 serial ports is configurable via Firmware commands and CPLD as EIA-232 or EIA-422 or EIA-485. Each port operates in full duplex mode or in half duplex mode. Fast slew rate is the default mode in EIA-485 mode.

The signaling level of EIA-485 is compatible with EIA-422, so full duplex EIA-485 may also be used for point-to-point communications with an EIA-422 serial port. When port is operating in EIA-485 mode software may configure the termination for V.35, V11 or unterminated using CPLD.

In EIA-232 mode the port is always unterminated register.

3.3V LVCMOS signaling

COM1 maintenance port supports EIA-232 signal level by default and 3V3 LVCMOS level signaling. Selection between these two modes is done by u-boot firmware commands.

Maintenance Port use LVCMOS signaling non-inverted (active high) level with the following characteristics.

Table 15: 3.3V LVCMOS voltage levels

3.3V LVCMOS Voltage levels	
VCC	3.3V +/- 0.3V
Vih	1.7V
Vil	0.7V
Voh	2.0V
Vol	0.4V

3.5. GPIOs and GDISCRETE1

3.5.1. GPIOs

The VX6124 features up to 8 GPIOs managed by the CPLD. Refer to the VX6124 Yocto Linux Release Notes D235834 for further details on the GPIO driver.

- 4 GPIOs are available on front panel RJ12 connector: GPIO1, GPIO5, GPIO6 and GPIO7. For detailed pin assignment, refer to section 4.1.4 - "GPIO connector" page 51.
- 1 GPIOs are available on P1 connector, GPIO8 (maskable reset). See section 4.3.2 “P1 Connector” for detailed pinout.
- 3 GPIOs are available on P2 connector: GPIO2, GPIO3 and GPIO4. See section 4.3.3 “P2 Connector” for detailed pinout.

GPIO electrical characteristics:

- The CPLD features LVCMOS33 cells (0-3V3),
- drive strength = 8 mA (sink or source),
- a clamp diode which is not 5V tolerant,
- an hysteresis of 250mV.

The CPLD does not implement any internal pull-up or pull-down.

On the VX6124 board, a pull-up of 47 KOhms is connected to GPIO1 to GPIO8.

CAUTION: GPIOs are not 5V tolerant. Maximum voltage on GPIOs is 3.6 V. Absolute maximum voltage is 3.75V and is not suitable for continuous operation. Appropriate voltage reduction (through resistor divider for instance) must be made to avoid permanent damage to the board.

The GPIOs share the same interrupt in the CPLD.

3.5.2. GDISCRETE1

GDISCRETE1 is a bussed open-collector GPIO defined by OpenVPX VITA 65 and available on P1. See section 4.3.2 “P1 Connector" for detailed pinout.

It is handled by the CPLD and buffered by a SN74LVC1G125 wired as an Open Collector to meet the electrical characteristics defined in VITA 65.

It has a dedicated interrupt in the CPLD.

3.6. Reset

RESET SOURCE	RESET ACTION	RESET CONTROL	RESET STATUS	NOTE
Front panel reset push button	Board reset Active VPX Sysreset if the board is system controller	Front push button	"I2C_BOARD_STATUS @0x72	Reset propagation options and masks available in cPLD registers
VPX Sysreset	Reset the board if configured in cPLD setting	VPX P0 / Row B/ Wafer 4	"I2C_BOARD_STATUS @0x72	"See VPX Vita46.0 standard Reset propagation options and masks available in cPLD registers"
VPX maskable reset (GPIO8)	Reset the board	VPX P1 / Row G/ Wafer 15	"I2C_BOARD_STATUS @0x72	See VPX Vita46.0 standard
cPLD watchdog reset	Reset the board	See Yocto Linux Release Notes D235834	"I2C_BOARD_STATUS @0x72	See software release notes
Processor watchdog reset	Reset the board	NXP QrIQ watchdog control registers	NXP QorIQ watchdog status registers	
cPLD software reset	Reset the board	I2C_BOARD_CONTROL @0x73	"I2C_BOARD_STATUS @0x72	See register definition in this Yocto Linux Release Notes D235834

3.7. Write Protect Mode

VX6124 non-volatile content is managed in three independent write protection domains.

- **SYS:** Temporary, run time data
- **USR:** Settings data, maintenance under user control
- **VPD:** Kontron driven static data

On top of the domains, two 'top level' settings can override the domains write protection

- **NVMRO:** force all domains to be Write Protected
- **FACTORY:** force all domains to be Writeable

SYS_WP

- **Description:**
  Write protection at system level of run time volatile information (PBIT results)
- **Hardware Write Protection:**
  NVMRO signal is high and SW3101[1] (Factory mode) is OFF for full protection
- **Write Protect Control:**

NVMRO	SW3101[1] Factory mode	SW3101[3] System write protection	CPLD register @09-bit 2	Protection	Mode of Operation
1	OFF	X	X	YES	Normal
0	X	OFF	0	No	Normal
1	ON	ON	1	YES	Factory
1	ON	OFF	0	No	Factory
0	X	OFF	1	YES	Software forced protection

  X = "don't care", CPLD register @09-bit 2 default setting is "0"
- **Protected Devices:**
  - 256 Kbits SYS EEPROM on CPLD I2C bus @0x51
  - XMC EEPROM on QorIQ I2C2 bus @0x50

The System EEPROM contains the PBIT detailed results, so this data may not be updated if protection is active on the "SYS" domain

USER_WP

- **Description:**
  Write protection at user level for maintenance and user driven information
- **Hardware Write Protection:**
  MVMRO signal is high and SW3101[1] (Factory) is OFF for full protection
- **Write Protect Control:**

NVMRO	SW3101[1] Factory mode	SW3101[4] USER write protection	CPLD register @09-bit 3	Protection	Operation
1	OFF	X	X	YES	Normal
0	X	OFF	0	No	Normal
1	ON	ON	X	YES	Factory
1	ON	OFF	0	No	Factory
1	ON	OFF	1	YES	Factory
0	X	ON	X	YES	DIP switch forced protection
0	X	OFF	1	YES	Software forced protection

X = “don't care”, CPLD register @09-bit 3 default setting is “0”

- **Protected Devices:**
  - 1 Mbits User FRAM located on CPLD I2C bus @0x52/53
  - Internal CPLD configuration flash
  - XSPI Boot Flash memories

The XSPI boot flash memories (main & rescue) contains the firmware settings, so this data may not be updated if protection is active on the "USR" domain

VPD_WP

- **Description:**
  Write protection at VPD level of static information vendor/kontron driven.
- **Hardware Write Protection:**
  MVMRO signal is high and SW3101[2] & SW3101[1] are OFF for full protection
- **Write Protect Control:**

NVMRO	SW3101[1] Factory mode	SW3101[2] VPD write protection	CPLD register @09-bit 1	Protection	Protection
X	X	ON	X	No	DIP switch released protection
1	OFF	OFF	X	YES	Normal
1	ON	OFF	0	No	Factory
1	ON	OFF	1	YES	Factory
0	X	OFF	0	No	Software released protection
0	X	OFF	1	YES	Normal

X = "don't care", CPLD register @09-bit 1 default setting is "1"

- **Protected Devices:**
  - 256Kbits VPD EEPROM on CPLD I2C2 bus @0x50

NVMRO

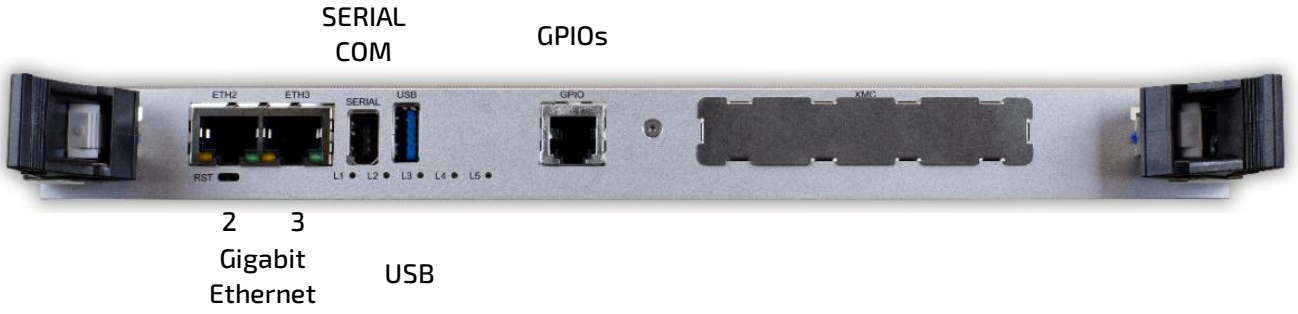
- All non-volatile devices protected.
- NVMRO signal is high and SW3101[3] & SW3101[2] are OFF for full non-volatile devices protection.
- VX6124 offers the capability to drive the NVMRO signal on the backplane by setting SW3102[4] ON.

CAUTION: Set the hardware jumper SW3102 [4] to ON force to ground the NVMRO signal on the backplane. Write protection is de-asserted for all the boards in the chassis.

4/ Physical I/O

4.1. Front Panel Connectors

Figure 16: Front Panel Connectors



4.1.1. Serial Connector – COM1 Maintenance Port

The VX6124 integrates up to three serial communications ports, COM1, COM2 and COM4.

COM1 Maintenance Port is available on IEEE1394 front panel connector and on rear via P1 connector. COM1 Maintenance Port supports simplified EIA-232 signal level by default and 3V3 LVCMOS level signaling. Selection between these two modes is done from u-boot firmware.

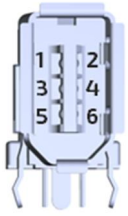
For further details, refer to section 3.4 - "Serial Lines Additional Modes", page 44.

- **Front Serial Connector Description**

Table 16: Serial Connector Pin Assignment

Pin	Signal
1	NC
2	GND
3	COM1_RXD
4	NC
5	COM1_TXD
6	NC

Figure 17: Serial Connector (IEEE 1394 Type)



NOTICE

CAUTION: Serial lines are routed to both front panel connector and rear P1. Plugging a serial device to both connectors will lead to electrical contention. Be sure to use only one connector at a time.

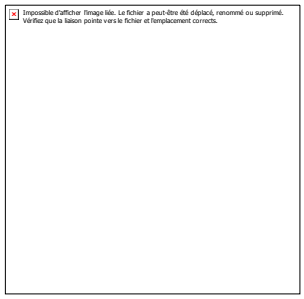
Table 17: Serial Connector Signals Definition

Signal	Dir.	Definition
COM1 TXD	O	EIA-232: Transmit Data of port COM1
COM1 RXD	I	EIA-232 Receive Data of port COM1
Reserved	-	Reserved
GND	-	Logic ground
Shell	-	Chassis ground

Table 18: Serial Cable Description

Pin connector DB9	Signal	Pin connector IEE1394
1	NC	1
5	GND	2
3	RXD	3
4	NC	4
2	TXD	5
6	NC	6

Figure 18: Serial cable



4.1.2. Gigabit Ethernet Connectors

The Ethernet transmission should operate using a CAT5e cable with a maximum length of 50m.

The VX6124 offers two Gigabit Ethernet interface, ETH2 and ETH3 on front panel.

These two Ethernet interfaces are available on RJ-45 connectors with tap down. The interfaces provide automatic detection and switching between 10Base-T, 100Base-TX and 1000Base-T data transmission (Auto-Negotiation). Auto-wire switching for crossed cables is also supported (Auto-MDI/X).

Table 19: Gigabit Ethernet Connectors Pin Assignment

Pin	10BASE-T		100BASE-T		1000BASE-T	
	I/O	SIGNAL	I/O	SIGNAL	I/O	SIGNAL
1	O	TX+	O	TX+	I/O	BI_D
2	O	TX-	O	TX-	I/O	BI_D
3	I	RX+	I	RX+	I/O	BI_D
4	-	-	-	-	I/O	BI_D
5	-	-	-	-	I/O	BI_D
6	I	RX-	I	RX-	I/O	BI_D
7	-	-	-	-	I/O	BI_D
8	-	-	-	-	I/O	BI_D
Shell	CHASSIS GROUND					

Figure 19: Double Ethernet Connector

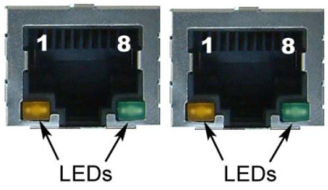


Table 20: Ethernet LEDs Status Definition

STATUS		SPEED LED YELLOW	ACT LED GREEN
Ethernet Link is not established		OFF	OFF
10 Mbps	Ethernet Link Established	OFF	ON
	Ethernet Link Activity	OFF	BLINK
100 Mbps	Ethernet Link Established	OFF	ON
	Ethernet Link Activity	OFF	BLINK
1000 Mbps	Ethernet Link Established	ON	ON
	Ethernet Link Activity	ON	BLINK

► ACT (Green)

This LED monitors network connection and activity. The LED lights up when a valid link (cable connection) has been established. The LED goes temporarily off if network packets are being sent or received through the RJ-45 port. When this LED remains off, a valid link has not been established due to a missing or a faulty cable connection.

4.1.3. USB connector

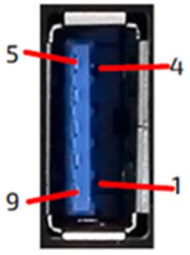
The VX6124 provides an USB front connector carrying USB 2.0 port and USB 3.0 port USBSS.

USB cable shall be compliant to Universal Serial Bus Specification, Revision 3.0.
This USB cable shall have double shielding.
The USB cable length should not exceed 3 m.

Table 21: USB3.0 Connector Pin Assignment

PIN	SIGNAL	FUNCTION	I/O
1	VBUS	+5V Protected by 1.5A fuse	O
2	USB_D-	Differential USB-	I/O
3	USB_D+	Differential USB+	I/O
4	GND	Logic Ground	-
5	STDA_SSRX-	Negative SuperSpeed receiver differential pair	I
6	STDA_SSRX+	Positive SuperSpeed receiver differential pair	I
7	GND_DRAIN	Logic Ground	-
8	STDA_SSTX-	SuperSpeed transmitter differential pair	O
9	STDA_SSTX+	SuperSpeed transmitter differential pair	O

Figure 20: USB Connector



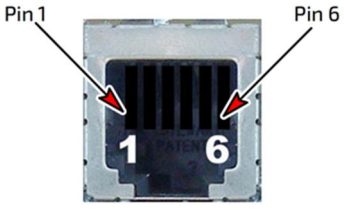
4.1.4. GPIO connector

The VX6124 offers four General Purpose I/Os on front panel through RJ12 connector. For further detail about GPIOs characteristic refer to section 3.5 - "GPIOs and GDISCRETE1", page 45.

Table 22: GPIO Connector Pin Assignment

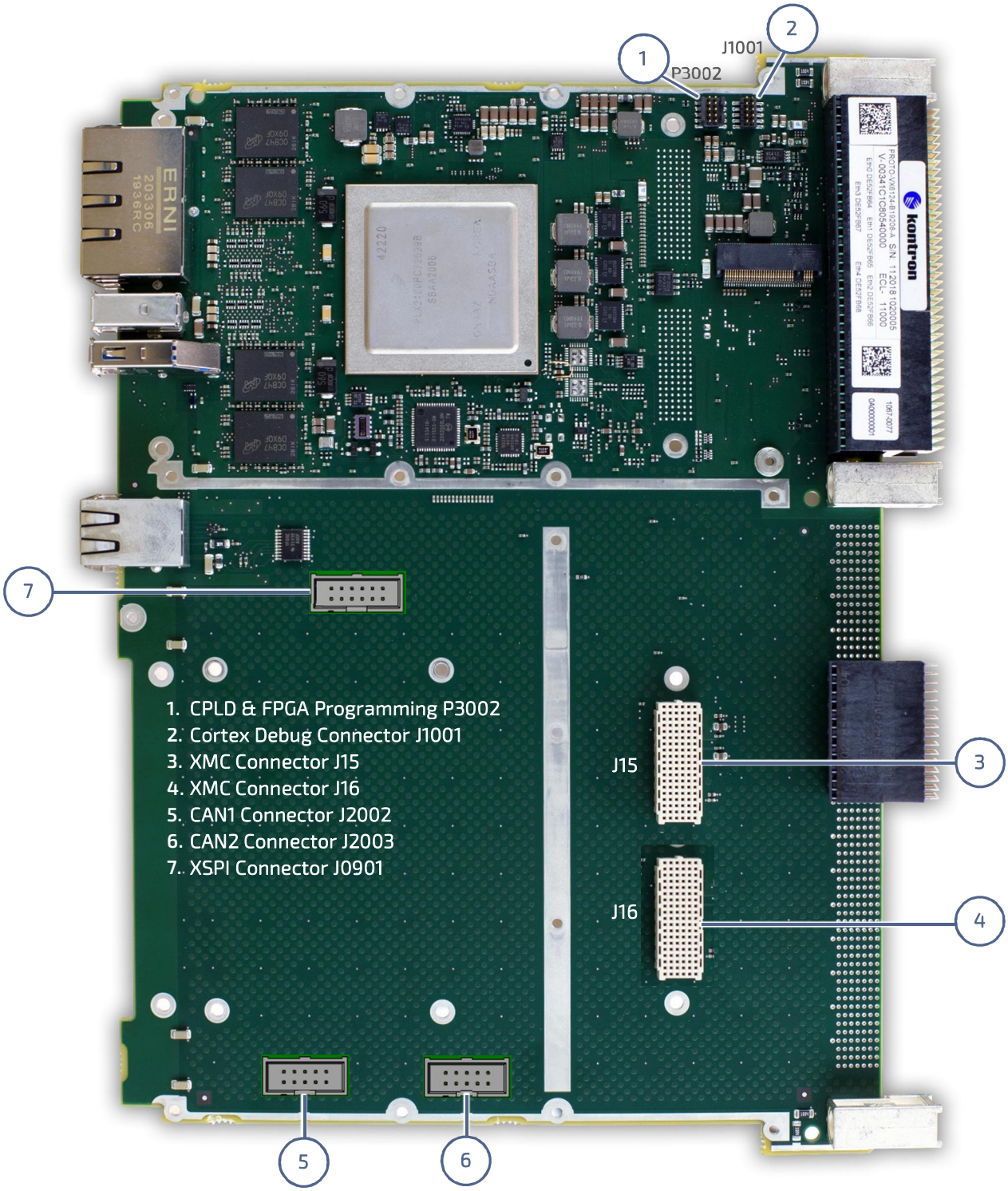
PIN	SIGNAL	FUNCTION	I/O
P1	GPIO1	GPIO	I/O
P2	GPIO5	GPIO	I/O
P3	GPIO6	GPIO	I/O
P4	GPIO7	GPIO	I/O
P5	3.3V	POWER	--
P6	GND	GND	--

Figure 21: RJ12 Connector



4.2. Onboard Connectors

Figure 22: Onboard Connectors



4.2.1. XMC connector J15

The pin assignment of the J15 XMC PCI Express connector is compatible with VITA 61.0 pin definition. This interface is a PCI Express with 8 lanes coming from the CPU.

Table 23: XMC J15 Sockets Pin Assignment

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR (1)
2	GND	GND	TRST#	GND	GND	MRSTI#
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR (1)
4	GND	GND	TCK	GND	GND	N.C.
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR (1)
6	GND	GND	TMS	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR (1)
8	GND	GND	TDI	GND	GND	-12V AUX
9	RFU	RFU	N.C.	RFU	RFU	VPWR (1)
10	GND	GND	TDO	GND	GND	GA0
11	PER0p0	PER0n0	N.C.	PER0p1	PER0n1	VPWR
12	GND	GND	GA1	GND	GND	MPRESENT#
13	PER0p2	PER0n2	3.3V AUX	PER0p3	PER0n3	VPWR (1)
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	N.C.	PER0p5	PER0n5	VPWR (1)
16	GND	GND	NVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	N.C.	PER0p7	PER0n7	N.C.
18	GND	GND	N.C.	GND	GND	N.C.
19	REFCLK+0	REFCLK-0	N.C.	WAKE#	N.C.	N.C.

(1) VPWR is connected to +12V via a fuse.

Signals active when low.

Table 24: XMC Connector J15 Signal Description

Signal	Dir.	Definition
+12V	O	+12 Volts DC power pin.
-12V AUX	O	Auxiliary -12 Volts DC power pin.
3.3V	O	+3.3 Volts DC power pin.
3.3V AUX	O	Auxiliary +3.3 Volts.
GA[0..2]	O	I2C channel select as per VITA42.0.
GND	-	Ground
MRSTI#*	O	XMC Reset In as per VITA42.0 (10 ms pulse min.) and PCIe PERST# as per VITA42.3.
MSDA	I/O	I2C serial data as per VITA42.0.
MSCL	O	I2C serial clock as per VITA42.0.
MPRESENT#	O	Module present as per VITA42.0.
N.C.	-	Not Connected
NVMRO	O	XMC Write Prohibit as per VITA42.0.
TCK	O	JTAG Clock as per VITA42.0.

Signal	Dir.	Definition
TDI	O	JTAG Data In as per VITA42.0.
TDO	I	JTAG Data Out as per VITA42.0.
TMS	O	JTAG Mode Select as per VITA42.0.
TRST#	O	JTAG Reset as per VITA42.0.
PET0p0/n[0..7]	I	PCIe differential transmit pairs 0 to 7 (as per VITA42.3)
PER0p0/n[0..7]	O	PCIe differential receive pairs 0 to 7 (as per VITA42.3)
REFCLK+/-0	O	100MHz PCIe differential reference clock as per VITA42.3.
RFU	-	Reserved For User
VPWR	O	+12V power pins.
WAKE#	I	Open drain WAKE# signal.

4.2.2. XMC J16 Connector Pin Assignment

XMC I/O signals are routed to the VPX P5 connectors according to P5w1-X24s+X8d+X12d signal assignment as per VITA 46.9.

Table 25: XMC J16 Connector Pin Assignment

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	XMCIO_DP1-	XMCIO_DP1+	NC	XMCIO_DP2-	XMCIO_DP2+	NC
2	GND	GND	NC	GND	GND	NC
3	XMCIO_DP3-	XMCIO_DP3+	NC	XMCIO_DP4-	XMCIO_DP4+	NC
4	GND	GND	NC	GND	GND	NC
5	NC	NC	NC	NC	NC	NC
6	GND	GND	NC	GND	GND	NC
7	XMCIO_DP7-	XMCIO_DP7+	NC	XMCIO_DP8-	XMCIO_DP8+	NC
8	GND	GND	XMCIO_SE23	GND	GND	XMCIO_SE24
9	XMCIO_DP9-	XMCIO_DP9+	XMCIO_SE21	XMCIO_DP10-	XMCIO_DP10+	XMCIO_SE22
10	GND	GND	XMCIO_SE19	GND	GND	XMCIO_SE20
11	XMCIO_DP11-	XMCIO_DP11+	XMCIO_SE17	XMCIO_DP12-	XMCIO_DP12+	XMCIO_SE18
12	GND	GND	XMCIO_SE15	GND	GND	XMCIO_SE16
13	NC	NC	XMCIO_SE13	NC	NC	XMCIO_SE14
14	GND	GND	XMCIO_SE11	GND	GND	XMCIO_SE12
15	XMCIO_DP15-	XMCIO_DP15+	XMCIO_SE9	XMCIO_DP16-	XMCIO_DP16+	XMCIO_SE10
16	GND	GND	XMCIO_SE7	GND	GND	XMCIO_SE8
17	XMCIO_DP17-	XMCIO_DP17+	XMCIO_SE5	XMCIO_DP18-	XMCIO_DP18+	XMCIO_SE6
18	GND	GND	XMCIO_SE3	GND	GND	XMCIO_SE4
19	XMCIO_DP19-	XMCIO_DP19+	XMCIO_SE1	XMCIO_DP20-	XMCIO_DP20+	XMCIO_SE2

- XMCIO signals are routed to VPX P5, see VPX P5 pin assignment table.
- NC pins are not connected on VX6124 board

Table 26: XMC J16 Connector Signals Definition

MNEMONIC	DIRECTIO	SIGNAL DEFINITION
XMCIO_DPn+/-	I/O	XMCIO differential pair n
XMCIO_SEn	I/O	XMCIO single-ended signal n

4.2.3. LX2160A Cortex Debug Connector

The VX6124 implements legacy 10-pin Cortex-M Debug connector. This connector supports JTAG debug for QorIQ processor by enabling the connection of CodeWarrior TAP target system debugging tool. The CodeWarrior TAP allows you to debug and control of the LX2160A processor using the CodeWarrior IDE.

For further information about CodeWarrior TAP, visit NXP web site: https://www.nxp.com

Table 27: Cortex Debug connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
9	GND Detect	10	RESET#
7	NC	8	TDI
5	GND	6	TDO
3	GND	4	TCK
1	1.8V	2	TMS

Figure 23: Cortex Debug Connector

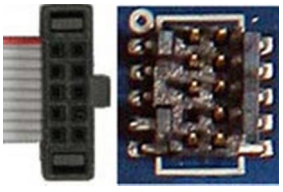


Table 28: Cortex Debug connector Signal Description

SIGNAL	DIRECTIO N	DEFINITION
1.8V	Output	+1.8V only used to indicated to the TAP that power is applied on connector.
GND	-	Logic Ground
TDI	Input	JTAG TDI for QorIQ processor
TDO	Output	JTAG TDO for QorIQ processor
TCK	Input	JTAG TCK for QorIQ processor
TMS	Input	JTAG TMS for QorIQ processor
GND Detect	Input	GNDDetect is an optional board feature. Not used on VX6124.
RESET#	Input	Processor reset from CodeWarrior TAP.

4.2.1. CAN BUS connectors

The VX6124 provides two CAN bus connectors through two 10-pin HE10 connectors. FD-CAN bus feature depends on SoC part number. Contact Kontron support to know availability of this feature.

Table 29: CAN BUS connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	NC	2	CANx_L
3	GND	4	NC
5	EARTH	6	GND
7	CANx_H	8	NC
9	5V	10	NC

X meaning 1 or 2 depending on CAN bus interface

Figure 24: CAN BUS Connector

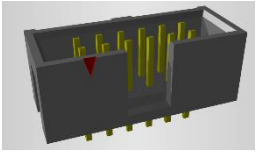
4.2.1. XSPI connector

The VX6124 provides one XSPI connector through 12-pin HE10 connector.

Table 30: XSPI connector Pin Assignment

PIN	SIGNAL	PIN	SIGNAL
1	XSPI1_A_CS#	2	XSPI1_A_SCK
3	XSPI1_A_D0	4	CPU_IRQ03
5	XSPI1_A_D1	6	RESET#
7	XSPI1_A_D2	8	GND
9	XSPI1_A_D3	10	GND
11	XSPI1_A_DQS	12	3.3V

Figure 25: XPSI Connector



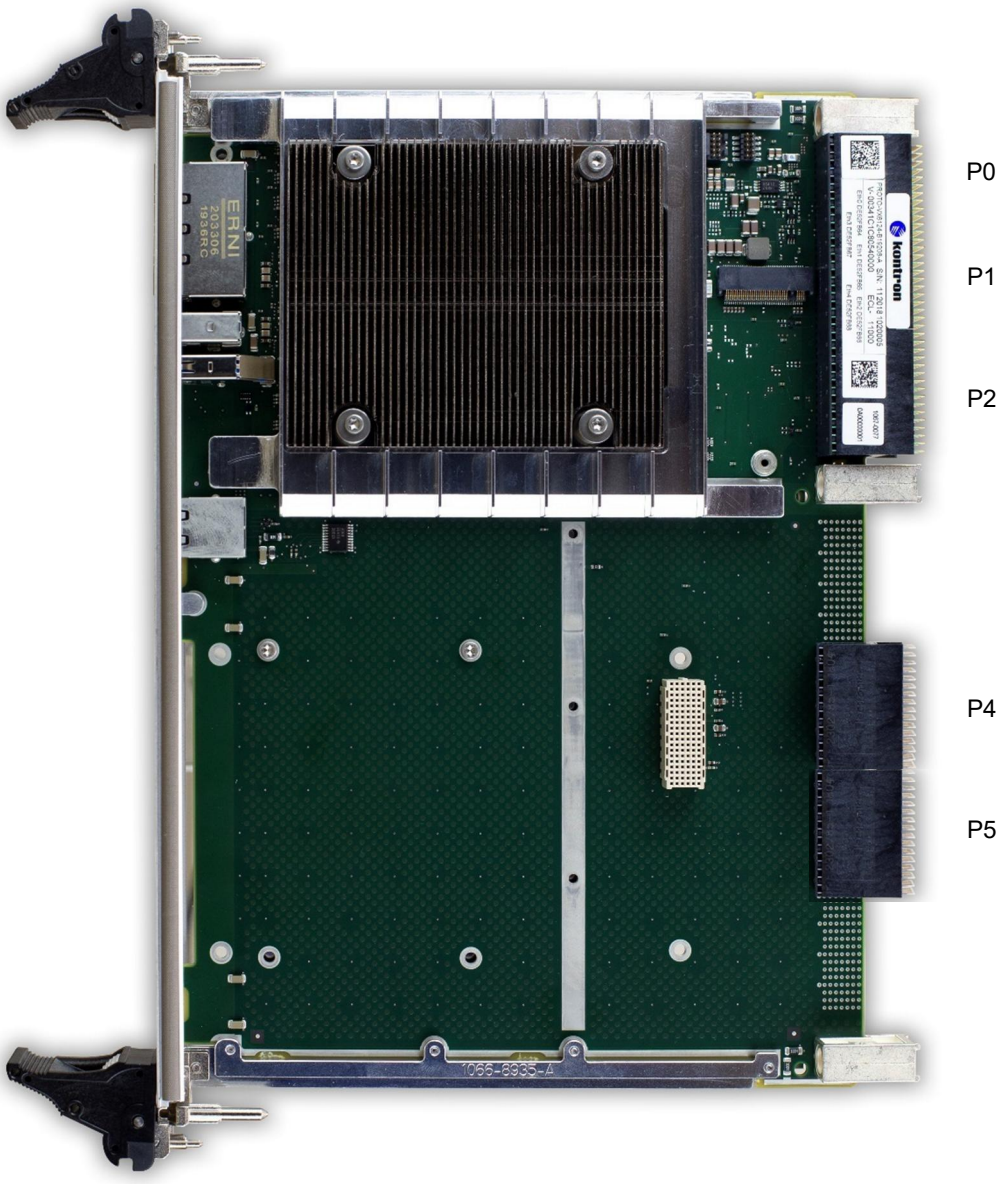
4.3. Rear Connectors

VPX Bus Interface

The 6U VPX connector configuration comprises four connectors named P0, P1, P2 and P4:

- P0: 8 wafers, 7 rows connector.
- P1 - P2 - P4 – P5: 16 wafers, 7 rows differential connectors.

Figure 26: VPX Connectors



SERDES Configuration

Some rear interfaces, such as networking, PCIe and SATA interfaces are LX2160A SERDES 1 and SERDES 2 configurations dependent. Contact Kontron support for knowing SerDes configuration availability.

The available SerDes 1 and SerDes 2 configuration are the following (Table 31 & Table 32):

Table 31: SerDes 1 RCW configuration

RCW Config #	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7
Config 13	100GE.1				100GE.2			
Config 20 (default)	40GE.1				40GE.2			
Config 18	XFI.3	XFI.4	25GE.5	25GE.6	XFI.7	XFI.8	XFI.9	XFI.10
Config 21	25GE.3	25GE.4	25GE.5	25GE.6	PCIE.4 x2 Gen3		25GE.9	25GE.10

Table 32: SerDes 2 RCW configuration

RCW Config #	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7
Config 13 (default)	PCIE.3 x4 Gen2				SGMII.15	SGMII.16	XFI.13	XFI.14
Config 20	X	X	SATA.1	SATA.2	SATA.3	SATA.4	XFI.13	XFI.14
Config 21	PCIE.3 x1 Gen2	SGMII.12	SGMII.17	SGMII.18	PCIE.4 x1 Gen2	SGMII.16	XFI.13	XFI.14

4.3.1. P0 Connector

Table 33: VPX Connector P0 Wafer Assignment

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	+12V	+12V	+12V	NC	NC	NC	NC
2	+12V	+12V	+12V	NC	NC	NC	NC
3	NC	NC	NC	NC	NC	NC	NC
4	IPMB_B_CLK	IPMB_B_DAT	GND	-12V_AUX	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3V3_AUX	GND	IPMB_A_CLK	IPMB_A DAT
6	GA3*	GA2*	GND	NC	GND	GA1*	GA0*
7	NC	GND	NC / MDC (2)	NC / MDIO (2)	GND	NC / GPIO6 / I2C2_SCL (1)	NC / GPIO7 / I2C2_SDA (1)
8	GND	REF_CLK-	REF_CLK+	GND	NC	NC	GND
CASE	GND						

* signal active when low

(1) depending on build option, default is NC (not connected).

(2) depending on build option, default is NC (not connected).

Table 34: VPX Connector P0 Signal Definition

MNEMONIC	SIGNAL DEFINITION
+12V	+12 Volts DC power (VS1 VPX supply). NC (+12V) pins are not connected (VS2 VPX supply)
-12V_AUX	-12 Volts auxiliary power. Only used to supply XMC if needed.
NVMRO	Non-Volatile Memory Read Only. When asserted (logical 1), prevents any non-volatile memory from being updated.
GAi	Geographical address pins
GAP	Geographical address parity
GND	Ground
IPMB_A/B	Intelligent Platform Management Bus, defined by VITA 46.11.
REF_CLK+/-	The Reference Clock is a bussed differential pair. Output if the VX6124 is plugged in the system controller slot, input otherwise. It enables the entire system to synchronize to a common time reference if desired. Counter/timer in the CPLD can use this clock
SYSRESET*	System Reset. Input and open collector output.
GPIOx*	General purpose I/O (handled by CPLD). Not connected by default, contact Kontron support for availability.
I2C2_SCL/SDA	Clock and data I2C bus 2 from LX2160A – 3.3V Signalling
MDC/MDIO	Ethernet management bus from LX2160A

4.3.2. P1 Connector

Table 35: VPX Connector P1 Wafer Assignment

- Legend for Table 35: VPX Connector P1 Wafer Assignment:

P1_VBAT	Battery Voltage	GPIOx	General Purpose I/O x (handled by the CPLD)
P1_SYS_CON*	System Controller	SD1_TX/RX[0..3]	SERDES 1 four-first lanes (40GBASE-KR or 100GBASE-KR depending on RCW SERDES 1 configuration)
GDISCRETE1	x4 PCI-Express	SD1_TX/RX[4..7]	SERDES 1 four-last lanes (40GBASE-KR or 100GBASE-KR depending on RCW SERDES 1 configuration)
COM1	Maintenance Port	ETH0/1 TX/RX	10GBASE-KR links from SERDES2 of SoC

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	GDISCRETE1	GND	SD1_TX0-	SD1_TX0+	GND	SD1_RX0-	SD1_RX0+
2	GND	SD1_TX1-	SD1_TX1+	GND	SD1_RX1-	SD1_RX1+	GND
3	VBAT	GND	SD1_TX2-	SD1_TX2+	GND	SD1_RX2-	SD1_RX2+
4	GND	SD1_TX3-	SD1_TX3+	GND	SD1_RX3-	SD1_RX3+	GND
5	SYS_CON*	GND	SD1_TX4-	SD1_TX4+	GND	SD1_RX4-	SD1_RX4+
6	GND	SD1_TX5-	SD1_TX5+	GND	SD1_RX5-	SD1_RX5+	GND
7	NC/ GPIO5 (2)	GND	SD1_TX6-	SD1_TX6+	GND	SD1_RX6-	SD1_RX6+
8	GND	SD1_TX7-	SD1_TX7+	GND	SD1_RX7-	SD1_RX7+	GND
9	COM1 TXD	GND	NC	NC	GND	NC	NC
10	GND	NC	NC	GND	NC	NC	GND
11	COM1 RXD	GND	NC	NC	GND	NC	NC
12	GND	NC	NC	GND	NC	NC	GND
13	NC / GPIO1 (2)	GND	NC	NC	GND	NC	NC
14	GND	NC	NC	GND	NC	NC	GND
15	Maskable Reset*	GND	NC / ETH0 TX- (1)	NC / ETH0 TX+ (1)	GND	NC / ETH0 RX- (1)	NC / ETH0 RX+ (1)
16	GND	ETH1 TX-	ETH1 TX+	GND	ETH1 RX-	ETH1 RX+	GND
CASE	GND						

* signal active when low

(1) depending on build option, default is NC (not connected).

(2) depending on build option, default is NC (not connected). GPIO1 and GPIO5 are routed to front panel by default.

* Signal active when low

Table 36: VPX Connector P1 Signal Definition

MNEMONIC	SIGNAL DEFINITION
SD1_RX[0..7]+/-	SERDES1 Lane 0-7 :Receive data +/- (see Table 31 for SERDES 1 lanes configuration)
SD1_TX[0..7]+/-	SERDES1 Lane 0-7 : Transmit data +/- (see Table 31 for SERDES 1 lanes configuration)
ETH0 RX+/-	10GBASE-KR Ethernet port 0: Receive data +/-. Not connected by default, contact Kontron support for availability.
ETH0 TX+/-	10GBASE-KR Ethernet port 0: Transmit data +/-. Not connected by default, contact Kontron support for availability.
ETH1 RX+/-	10GBASE-KR Ethernet port 1: Receive data +/-
ETH1 TX+/-	10GBASE-KR Ethernet port 1: Transmit data +/-
GDISCRETE1	Open VPX GDISCRETE1 signal

MNEMONIC	SIGNAL DEFINITION
GPIO1, GPIO5	General Purpose I/O 1 and 5 (handled by the CPLD). Not connected by default, contact Kontron support for availability.
Maskable Reset(1) or GPIO8	Reset input or Optional general purpose I/O 8 (handled by CPLD) (may be left unconnected if not used).
GND	Ground
SYS_CON	System Controller Slot Indication
VBAT	Battery Voltage Input, 3V. Optional alternated source for RTC backup voltage.
COM1	Maintenance port : serial Lines EIA-232 or 3V3 signal leveling

(1) See section 3.5 - GPIOs and GDISCRETE1 – page 45.

4.3.3. P2 Connector

Table 37: VPX Connector P2 Wafer Assignment

- Legend for Table 37: VPX Connector P2 Wafer Assignment:

SD2_TX/RX[0..3]	SERDES 2 four-first lanes (PCIe x4 depending on RCW SERDES 2 configuration)	GPIOx	General Purpose I/O x (handled by the CPLD)
COM2/COM4	Serial lines		

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	COM2_TXD-	GND	SD2_TX0-	SD2_TX0+	GND	SD2_RX0-	SD2_RX0+
2	GND	SD2_TX1-	SD2_TX1+	GND	SD2_RX1-	SD2_RX1+	GND
3	COM2_TXD+ COM4_TXD	GND	SD2_TX2-	SD2_TX2+	GND	SD2_RX2-	SD2_RX2+
4	GND	SD2_TX3-	SD2_TX3+	GND	SD2_RX3-	SD2_RX3+	GND
5	COM2_RXD-	GND	NC	NC	NC	NC	NC
6	GND	NC	NC	GND	NC	NC	GND
7	COM2_RXD+ COM4_RXD	GND	NC	NC	NC	NC	NC
8	GND	NC	NC	GND	NC	NC	GND
9	NC	GND	NC	NC	GND	NC	NC
10	GND	NC	NC	GND	NC	NC	GND
11	GPIO2	GND	NC	NC	GND	NC	NC
12	GND	NC	NC	GND	NC	NC	GND
13	GPIO3	GND	NC	NC	GND	NC	NC
14	GND	NC	NC	GND	NC	NC	GND
15	GPIO4	GND	NC	NC	GND	NC	NC
16	GND	NC	NC	GND	NC	NC	GND
CASE	GND						

* signal active when low

Table 38: VPX Connector P2 Signal Definition

MNEMONIC	SIGNAL DEFINITION
SD2_RX[0..3]+/-	SERDES 2 Lane 0-3 :Receive data +/- (see Table 32 for SERDES 2 lanes configuration)
SD2_TX[0..3]+/-	SERDES 2 Lane 0-3 : Transmit data +/- (see Table 32 for SERDES 2 lanes configuration)
GPIO2, GPIO3, GPIO4	General Purpose I/O 2, 3 and 4 (handled by the CPLD).
GND	Ground
COM2	Serial Lines, EIA-232/EIA-485.
COM4	Serial Lines, EIA-232, exclusive with COM2 EIA-485 mode

* See section 3.5.2 GDISCRETE1 -- page 45.

4.3.4. P4 Connector

Table 39: VPX Connector P4 Wafer Assignment

- Legend for Table 40: VPX Connector P4 Signal Definition:

SD2_TX/RX[5]	SERDES 2 lane 5 (SATA depending on RCW SERDES 2 configuration)	GPIOx	General Purpose I/O x (handled by the CPLD)
ETH2 DA/DB/DC/DD	1000BASE-T link from Realtek GbE phy	USB port 1 (USB2.0/3.0) USB port 2	USB links from SoC
USB1, USB2 PWR	USB1 and USB2 5V power	COM3	Serial line
ETH0 TX/RX	10GBASE-KR link from SERDES2 of SoC		

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	NC / COM3_TXD- (1)	GND	NC / SD2_TX5- (3)	NC / SD2_TX5+(3	GND	NC / SD2_RX5-(3	NC / SD2_RX5+(3
2	GND	NC	NC	GND	NC	NC	GND
3	NC / COM3_TXD+ (1)	GND	NC	NC	GND	NC	NC
4	GND	NC	NC	GND	NC	NC	GND
5	NC	GND	NC	NC	GND	NC	NC
6	GND	NC	NC	GND	NC	NC	GND
7	NC	GND	NC	NC	GND	NC	NC
8	GND	NC	NC	GND	NC	NC	GND
9	USB1 PWR	GND	USB2 D-	USB2 D+	GND	USB1 D-	USB1 D+
10	GND	USB1 TX-	USB1 TX+	GND	USB1 RX-	USB1 RX+	GND
11	USB2 PWR	GND	NC	NC	GND	NC	NC
12	GND	NC / ETH0 TX- (2)	NC / ETH0 TX+ (2)	GND	NC / ETH0 RX- (2)	NC / ETH0 RX+ (2)	GND
13	NC / COM3_RXD- (1)	GND	NC	NC	GND	NC	NC
14	GND	NC	NC	GND	NC	NC	GND
15	NC / COM3_RXD+ (1)	GND	ETH2 DB-	ETH2 DB+	GND	ETH2 DA-	ETH2 DA+
16	GND	ETH2 DD-	ETH2 DD+	GND	ETH2 DC-	ETH2 DC+	GND
CASE	GND						

* signal active when low

(1) depending on build option, default is NC (not connected).

(2) depending on build option, default is ETH0 TX/RX.

(3) depending on build option, default is NC (not connected).

Table 40: VPX Connector P4 Signal Definition

MNEMONIC	SIGNAL DEFINITION
SD2_RX5+/-	SERDES2 Lane 5 :Receive data +/- : Serial ATA. Receive +/-. Not connected by default.
SD2_TX5+/-	SERDES2 Lane 5 : Transmit data +/- : Serial ATA. Transmit +/-. Not connected by default.
ETH0 RX+/-	10GBASE-KR Ethernet port 0: Receive data +/-
ETH0 TX+/-	10GBASE-KR Ethernet port 0: Transmit data +/-
GND	Ground
COM3	Serial Lines, EIA-232/EIA-485. Not connected by default. Contact Kontron support for availability.
ETH2 DA+/-	Ethernet 1000BASE-T: First pair of transmit/receive data.
ETH2 DB+/-	Ethernet 1000BASE-T: Second pair of transmit/receive data
ETH2 DC+/-	Ethernet 1000BASE-T: Third pair of transmit/receive data.
ETH2 DD+/-	Ethernet 1000BASE-T: Fourth pair of transmit/receive data
USBx PWR	USBx Power
USB1 TX+/- RX+/-	Differential Data transmit and receive of USB1 link
USBx D+/-	Differential Data pair of USB x

4.3.1. P5 Connector

Table 41: VPX Connector P5 Wafer Assignment

- Legend for Table 41: VPX Connector P5 Wafer Assignment:

XMCIO_DP5-10 XMCIO_DP15-20	Differential XMC IO pins as per VITA46.9 X12d	XMCIO_DP1-4 XMCIO_DP11-14	Differential XMC IO pins as per VITA46.9 X8d
XMCIO_SE1-16	Single ended XMC IO according VITA46.9 X16s		

WAFER	ROW G	ROW F	ROW E	ROW D	ROW C	ROW B	ROW A
1	NC	GND	XMCIO_SE23	XMCIO_SE21	GND	XMCIO_SE24	XMCIO_SE22
2	GND	XMCIO_SE19	XMCIO_SE17	GND	XMCIO_SE20	XMCIO_SE18	GND
3	NC	GND	XMCIO_SE15	XMCIO_SE13	GND	XMCIO_SE16	XMCIO_SE14
4	GND	XMCIO_SE11	XMCIO_SE9	GND	XMCIO_SE12	XMCIO_SE10	GND
5	NC	GND	XMCIO_SE7	XMCIO_SE5	GND	XMCIO_SE8	XMCIO_SE6
6	GND	XMCIO_SE3	XMCIO_SE1	GND	XMCIO_SE4	XMCIO_SE2	GND
7	NC	GND	XMCIO_DP1-	XMCIO_DP1+	GND	XMCIO_DP2-	XMCIO_DP2+
8	GND	XMCIO_DP3-	XMCIO_DP3+	GND	XMCIO_DP4-	XMCIO_DP4+	GND
9	NC	GND	XMCIO_DP11-	XMCIO_DP11+	GND	XMCIO_DP12-	XMCIO_DP12+
10	GND	XMCIO_DP13-/ SD2_TX4- (1)	XMCIO_DP13+ / SD2_TX4+ (1)	GND	XMCIO_DP14-/ SD2_RX4- (1)	XMCIO_DP14+/ SD2_RX4+ (1)	GND
11	NC	GND	XMCIO_DP5- / SD2_TX5- (1)	XMCIO_DP5+ / SD2_TX5+ (1)	GND	XMCIO_DP6- / SD2_RX5- (1)	XMCIO_DP6+ / SD2_RX5+ (1)
12	GND	XMCIO_DP7-	XMCIO_DP7+	GND	XMCIO_DP8-	XMCIO_DP8+	GND
13	NC	GND	XMCIO_DP9-	XMCIO_DP9+	GND	XMCIO_DP10-	XMCIO_DP10+
14	GND	XMCIO_DP15-	XMCIO_DP15+	GND	XMCIO_DP16-	XMCIO_DP16+	GND
15	NC	GND	XMCIO_DP17-	XMCIO_DP17+	GND	XMCIO_DP18-	XMCIO_DP18+
16	GND	XMCIO_DP19-	XMCIO_DP19+	GND	XMCIO_DP20-	XMCIO_DP20+	GND
CASE	GND						

* signal active when low

(1) depending on build option, default is XMCIO.

Table 42: VPX Connector P5 Signal Definition

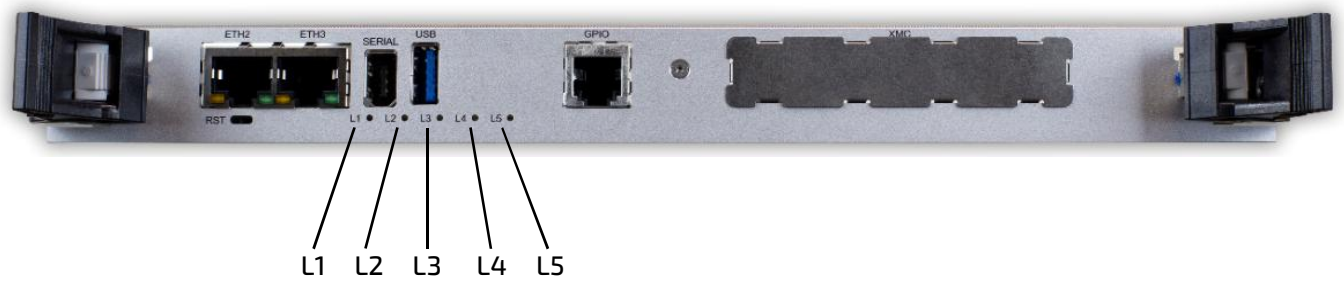
MNEMONIC	SIGNAL DEFINITION
XMCIO_SE1-24	Single ended XMC I/O 1 to 24 as per VITA 46.9 X24s
XMCIO_DP1-4 XMCIO_DP11-14	Differential pairs XMC I/O 1 to 4 and 11 to 14 as per VITA 46.9 X8d
XMCIO_DP5-10 XMCIO_DP15-20	Differential pairs XMC I/O 5 to 10 and 15 to 20 as per VITA 46.9 X12d
GND	Ground
SD2_RX4+/-	SERDES2 Lane 4 : Receive data +/- : SGMII port 15 Receive +/-. Not connected by default.
SD2_TX4+/-	SERDES2 Lane 4 : Transmit data +/- : SGMII port 15 Transmit +/-. Not connected by default.
SD2_RX5+/-	SERDES2 Lane 5 : Receive data +/- : SGMII port 16 Receive +/-. Not connected by default.
SD2_TX5+/-	SERDES2 Lane 5 : Transmit data +/- : SGMII port 16Transmit +/-. Not connected by default.

4.4. LEDs

Status LEDs Normal Operation

There are five bicolor LEDs (Red/Green) on the front panel of the VX6124 6U VPX board.

Figure 27: LEDs Front panel



4.4.1. LEDs Activity

Table 43: LEDs Description

CPU LED	DESCRIPTION
●	LED OFF
●	Red LED
●	Green LED
●	Orange LED
✳	Red blinking LED
✳	Green Blinking LED
✳	Orange blinking LED
✳	Not blink: Indicates that the corresponding LED gives an additional information if any LED is blinking at the same time

The following table describes the information that the LED can report:

Table 44: LEDs Activity

L1	L2	L3	L4	L5	MEANING
●	Not Blink	Not Blink	Not Blink	Not Blink	Permanent system error. Internal VX6124 power is off. In this state L2, L3, L4 and L5 do not carry the meaning described in this table but an error code.
● ✳					Internal power supplies power-up or standby mode CPLD activity
●					Reset state on subsystem.
●					Normal operation. No error, no reset, no CPLD activity
	●				CPLD watchdog reset timer expired.
	●				Normal operation.
	●				Factory test mode

L1	L2	L3	L4	L5	MEANING
		●			Hot temperature event
		● ✳			1000Base-T rear ETH2 interface: 1000Base-T link-up. Blinking when activity on this links
		● ✳			1000Base-T rear ETH2 interface: 100M or 10Base-T link-up. Blinking when activity on this links
			●		PBIT failed
			●		PBIT succeeded
			●		No PBIT result
				●	Normal operation

- Status LEDs for permanent error

Table 45: LEDs: Errors Codes

L1	L2	L3	L4	L5	POWER GOOD ERRORS
●	●	●	●	●	Not used
●	●	●	●	●	ERR_5V0_PWRGD
●	●	●	●	●	ERR_3V3SB_PWRGD
●	●	●	●	●	ERR_3V3_PWRGD
●	●	●	●	●	ERR_3V3SB_SRC
●	●	●	●	●	ERR_CLOCK_LOCK
●	●	●	●	●	ERR_1V8_PWRGD
●	●	●	●	●	ERR_1V2_DDR4_PWRGD
●	●	●	●	●	ERR_VR2V5_DDR4_PWRGD
●	●	●	●	●	ERR_0V9_PWRGD
●	●	●	●	●	ERR_CPU_VDD_PWRGD
●	●	●	●	●	ERR_CPU_VDD_FAULT
●	●	●	●	●	ERR_THERM_FAULT
●	●	●	●	●	ERR_BP_UV_PWRGD
●	●	●	●	●	ERR_BP_OV_PWRGD

5/ Power and Thermal Specifications

5.1. Power Consideration

The considerations presented in the ensuing sections must be taken into account by system integrators when specifying the VX6124 system environment.

5.1.1. Backplane

Backplanes to be used with the VX6124 must be adequately specified and comply with VITA 65.0. The backplane must provide optimal power distribution for the VPX VS1, VS2, VS3 and 3V3 AUX power inputs.

Input power connections to the backplane itself should be carefully specified to ensure a minimum of power loss and to guarantee operational stability. Long input lines, under dimensioned cabling or bridges, high resistance connections, etc. must be avoided.

5.1.2. Power Supply Units

Power supplies for the VX6124 must be specified with enough reserve for the remaining system consumption. In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires.

An industrial power supply unit should be able to provide at least twice as much power as the entire system requires. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires.

Where possible, power supplies which support voltage sensing should be used. Depending on the system configuration this may require an appropriate backplane. The power supply should be sufficient to allow for die resistance variations.

Tolerance

The following table provides information regarding the required characteristics for each board input voltage.

Table 46: Input Voltage Characteristics

POWER RAIL	NOMINAL VALUE	TOLERANCE*	MAX RIPPLE (p-p)	REMARKS
12V (VS1)	+12.0 VDC	+/-5%	50mV over a range 0-20Mhz	Main voltage
3.3V (VS2)	+3.3 VDC	3.25V min 3.45V max	50mV over a range 0-20Mhz	Not used on the VX6124
5.0V (VS3)	+5.0 VDC	+%5/-2.5%	50mV over a range 0-20Mhz	Not used on the VX6124
3.3Vaux	+3.3 VDC	+/-5%	50mV over a range 0-20Mhz	Not mandatory for the VX6124
GND	Ground not directly connected to potential earth (PE) on the VX6124 board			

(*)Tolerance values include ripple.

The output voltage overshoot generated during the application (load changes) or during the removal of the input voltage must be less than 5% of the nominal value. No Voltage of reverse polarity may be present on any output during turn-on or turn-off.

Rise time

As per VITA 46.0, section 3.2.2, the system power supply ramp-up phase should be between 20 and 150 msec. However, Kontron recommend a ramp-up phase below 25ms.

Regulation

The system power supplies should be monotonic as they ramp to their specified final values during power up conditions as per VITA 46.0, section 3.2.2.

The system power supply shall be unconditionally stable under line, load, unload and transient load conditions including capacitive loads. The operation of the power supply must be consistent even without the minimum load on all output lines.

If the main power input is switched off, the supply voltages will not go to 0V instantly. It will take a couple of seconds until capacitors are discharged. If the voltage rises again before it went below a certain level, the circuits may enter a latch-up state where even a hard RESET will not help any more. The system must be switched off for at least 3 seconds before it may be switched on again. If problems still occur, turn off the main power for 30 seconds before turning it on again.

5.1.3. Power Supplies Monitoring

The VX6124 embeds two voltage sensors monitoring power rails and internal power supply voltages.

- ADS7830 by Texas Instrument
- LTC2913 by Linear Technology

The voltage sensor ADS7830 is used to sample internal voltages on system request and display them to the user. Refer to VX6124 Yocto Linux Release Notes - D235834 for further details and know how to proceed.

The voltage sensor LTC2913 monitors VS1 voltage with a 10 % tolerance. The thresholds are set by hardware on the board. Undervoltage and overvoltage conditions on VS1 are reported to the cPLD which in turn shuts down all VX6124 internal power supplies. There is no mechanism for masking these alerts.

5.1.4. Output Powers Supplies Protection

On the VX6124, all the output power supplies provided on connectors are protected by fuse or current-limiting devices as described in Table 47.

Table 47: Output Powers Supplies Protection

Port	Function	Location	Voltage	Protection	Rated Current*	Trip current	Characteristics
VPX P1 Rear USB power pins	P1 USB Power	Rear P1	+5 V	USB power-distribution switches	1.2 A	1.2115 A min 1.295 A typ 1.375 A max	-
Front USB or Rear P2 VPX USB power pins	Front/P2 USB Power	Front or Rear P2	+5 V	USB power-distribution switches	1.2 A	1.2115 A min 1.295 A typ 1.375 A max	-
GPIO	GPIO additional power supply	On board	+3.3 V	Polyswitch resettable fuse	0.5 A	1.1 A typ	Derating of 50% should be applied
M2. Slots	M2 slot power supply	On board	+3.3 V	Non resettable fuse	4.5 A	-	-
XMC Slot	VPWR XMC slot power supply	On board	+12 V	Non resettable fuse	3 A	-	-
XMC Slot	12V XMC slot power supply	On board	+12 V	Non resettable fuse	2 A	-	-

Port	Function	Location	Voltage	Protection	Rated Current*	Trip current	Characteristics
XMC Slot	3.3V XMC slot power supply	On board	+3.3 V	Non resettable fuse	3 A	-	-
XMC Slot	3.3V XMC slot auxiliary power supply	On board	+3.3 V	Non resettable fuse	2 A	-	-
XMC Slot	-12V XMC slot auxiliary power supply	On board	+12 V	Non resettable fuse	2 A	-	-
CANbus Header	Optional 5V power supply	On board	+5.0 V	Polyswitch resettable fuse	0.5 A	1.1 A typ	Derating of 50% should be applied
XSPI Header	Optional 3.3V power supply	On board	+3.3 V	Polyswitch resettable fuse	0.5 A	1.1 A typ	Derating of 50% should be applied

* Worst Case Hold Rated Current for maximum operation temperature: a minimum of 20% Derating should be applied on fuse rated current.

5.2. VPX Input Power Rails Specification

The VX6124 board has been designed for optimal power input and distribution. Still it is necessary to observe certain criteria essential for application stability and reliability.

Absolute Maximum Input Voltage

The table below indicates the absolute maximum input voltage ratings that must not be exceeded. Power supplies to be used with the VX6124 should be carefully tested to ensure compliance with these ratings.

Table 48: Maximum Input Power

SUPPLY VOLTAGE	ABSOLUTE MAXIMUM PERMIT VOLTAGE
3.3V aux	3.5V
+12V (VPX VS1)	13V

⚠WARNING **The maximum permitted voltage indicated in the table above must not be exceeded. Failure to comply with these figures may result in damage to your board.**

Recommended Operating Input voltage

The following table specifies the recommended operating conditions of the different input power voltages within the board as per VITA46.0, section 3.2.2. The VX6124 is not guaranteed to function if the board is not operating within the prescribed limits.

Table 49: Recommended Operating Input Voltage

POWER RAIL	RECOMMENDED OPERATING INPUT VOLTAGE
VPX 3.3V AUX	3.3V +/- 5%
+12V VPX VS1	+12V +/- 5% inclusive of ripple

VPX 3.3V AUX shall be used on VX6124 boards as per VITA 46.0 and VITA 65.0.
However, this power rail input could be optional on VX6124 boards because it is internally generated from the +12V VS1 power input when it is not present on the backplane.

Input Power Supply Protection

The input power rails are protected on the VX6124 by fuse as described in Table 50.

To prevent safety hazards, the chassis power supply must not exceed the Voltage Rating and Interrupt Rating of the fuse.

Table 50: Input Powers Supplies Protection

POWER RAIL	VPX VS1	VPX 3.3 V AUX
LOCATION	P0	P0
VOLTAGE	+12 V	+3.3 V
PROTECTION	Non resettable fuse	Non resettable fuse
RATED CURRENT	12 A	1.5 A
TRIP CURRENT	-	2.20 A @ 85 °C 3.00 A @ 25 °C 3.54 A @ -40 °C
TYPICAL MELT I^2T	7.0	-
VOLTAGE RATING	24 V	6 V
INTERRUPTING RATING	150 A	100 A
MANUFACTURER / PN	3216FF12-R	NANOSMDC150F-2

5.3. Power Consumption Specification

5.3.1. VX6124 Thermal Power

The following tables below list the voltage and power specifications for the VX6124 board. The values were measured using an 8-slot passive VPX backplane.

Table 51: VX6124 Thermal Power: board power based on current measurements

PRODUCT	POWER MODE	MAX TOTAL POWER CONSUMPTION	TEST CONDITION
VX6124 QorIQ LX2160A @2.2GHz	Normal mode: 100 % all cores @2.2 GHz	TBD	Linux, CoreMark® 100%, processor junction temperature lower than 100°C, 2x Gigabit Ethernet links (front), 6 x 25GbE links and 2x 10GbE links, 16 GB dual bank DDR4-2133 memory configuration, no module on-board.
	Linux idle	TBD	Linux idle, processor junction temperature lower than 100°C, no Ethernet links, 16 GB dual bank DDR4-2133 memory configuration, no module on-board.

5.3.1. VX6124 Maximum Peak Current

The following data provide maximum continuous and worst case current values on VPX VS1 (12V) power supply. These maximum includes margin to guarantee worst-case part behavior.

Table 52: Maximum VS1 Current

Product	Max VPX VS1 current	Peak VPX VS1 current
VX6124 QorIQ LX2160A 2.2GHz	2.5 Amps	3 Amps (<5ms)

Maximum and peak current draw are intended as without mezzanine card or USB device plugged on board.

5.4. Thermal Considerations

The following chapters provide system integrators with the necessary information to satisfy thermal and airflow requirements when implementing VX6124 applications.

5.4.1. Board Thermal Monitoring

The following chapters provide system integrators with the necessary information to satisfy thermal and airflow requirements when implementing VX6124 applications.

To ensure optimal and long-term reliability of the VX6124, all onboard components must remain within the maximum temperature specifications. The most critical components on the VX6124 are the processor and the memory. Operating the VX6124 above the maximum operating limits will result in permanent damage to the board.

The VX6124 embeds two temperature sensors to measure:

- Internal processor die temperatures (diode remote sensor)
- Onboard temperature sensors

The on-board temperature sensors (Texas Instrument TMP411) are located on the I2C bus, and managed by the processor. Refer to VX6124 Yocto Linux Release Notes - D235834 for knowing how to proceed to get temperature sensor values.

Figure 28: One temperature sensor is located on top side

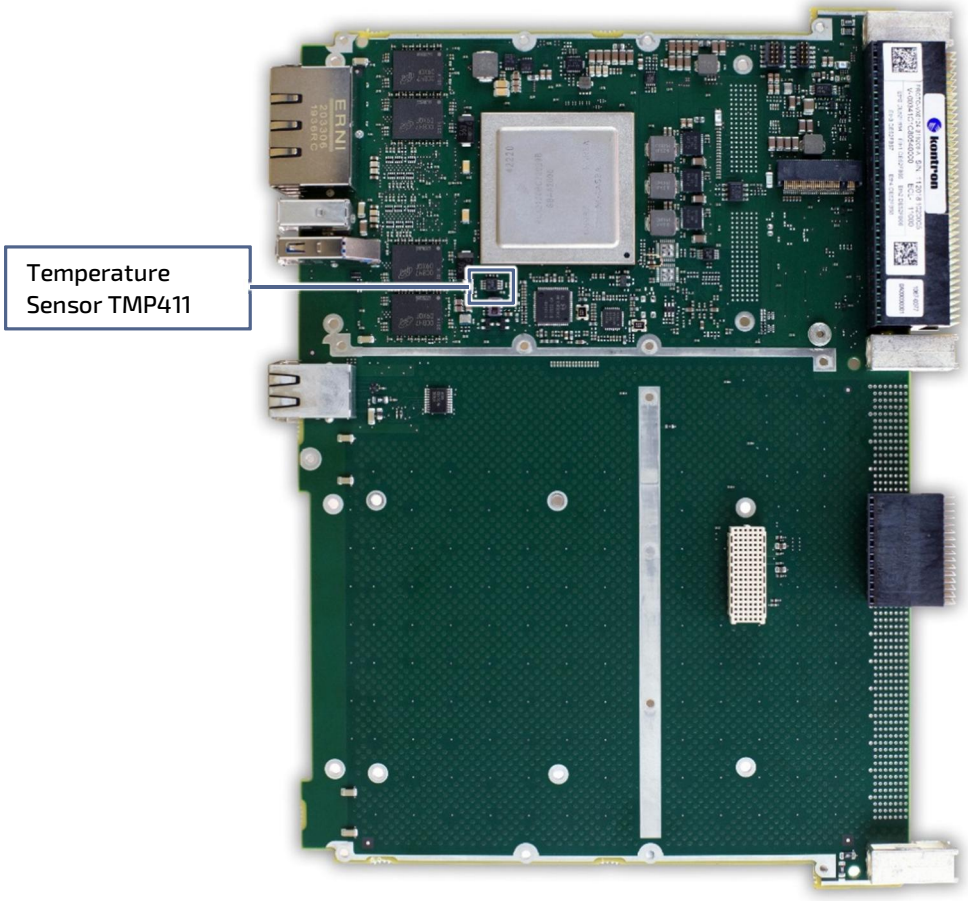
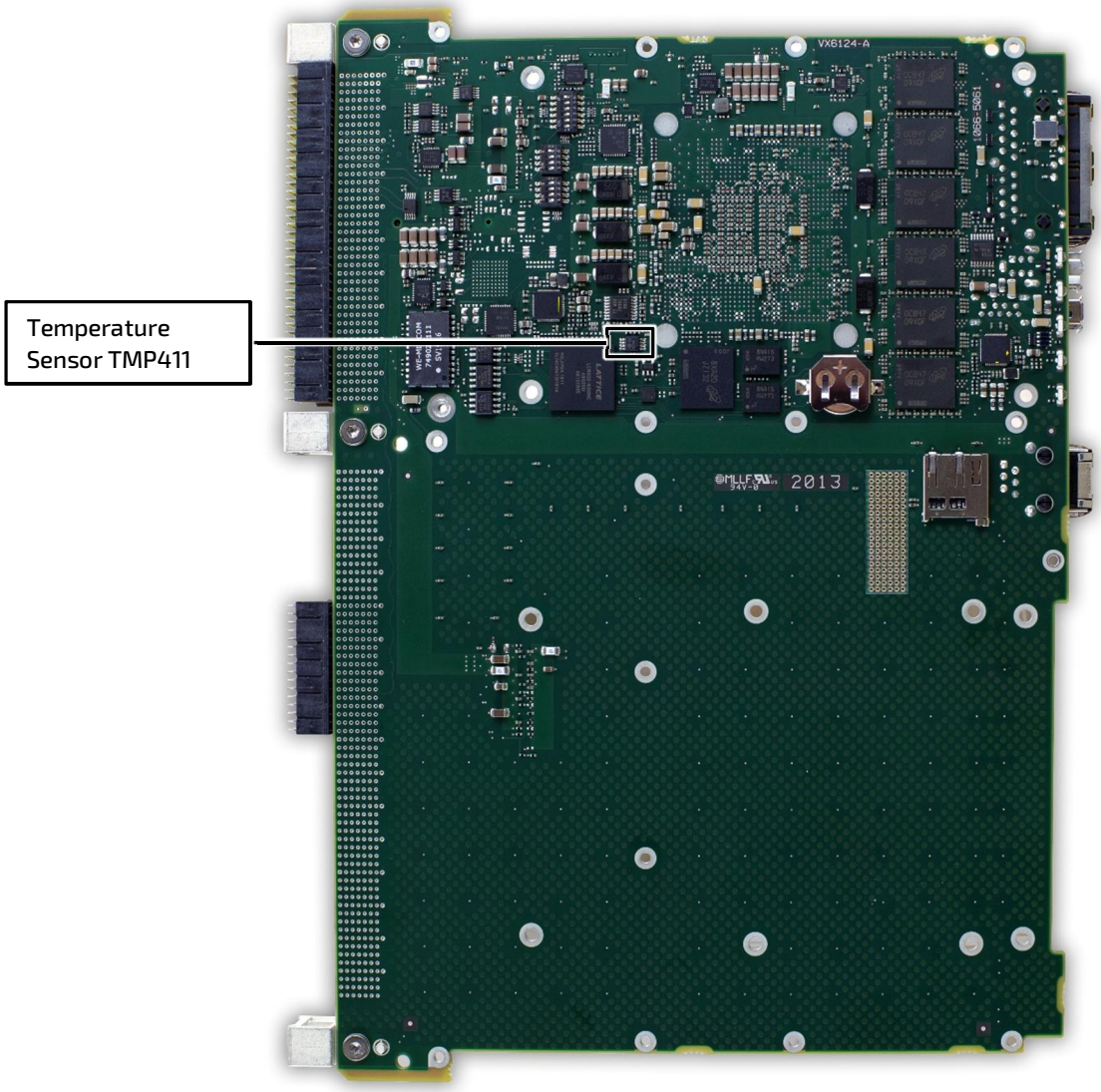


Figure 29: One temperature sensor is located on bottom side



TMP411 Key specifications:

TMP411 supports local and remote temperature sensor. TMP411 supports two alarm outputs: ALERT#, THERM# signals to activate system protection, connected to cPLD for event reporting.

- Remote temperature resolution / accuracy: 0.0625°C / ±1.25°C Typ (MAX ±2.5°C)
- Local temperature resolution / accuracy : 0.5°C / ±1°C Typ (MAX ±3°C)
- Operating temperature: –40°C to +125°C
- IC2 address of the sensor located on top side : 0x4C
- IC2 address of the sensor located on bottom side: 0x4D

When the LED3 on the front panel is lit red after boot-up, it indicates that one of the processor temperature sites is above its programmed threshold value.

5.4.2. SoC Thermal Monitoring

To allow optimal operation and long-term reliability of the VX6124, the QorIQ Layerscape LX2160A processor must remain within the maximum die temperature specification. The maximum operating temperature for the processor die (TJMAX) is 105°C.

The QorIQ LX2160A processor implements a Thermal Monitoring Unit (TMU) to monitor and report the temperature from one or more remote temperature measurement sites located inside the processor.

- One Temperature Sensor ID0 near core A72 clusters 6 and 7
- One Temperature Sensor ID1 near DDR1 controller and core A72 cluster 5
- One Temperature Sensor ID2 near WRIOP
- One Temperature Sensor ID3 near DCE, QBMAN and HSIO2
- One Temperature Sensor ID4 near CCN508, DPAA and TBU
- One Temperature Sensor ID5 near core A72 cluster 4 and HSIO3
- One Temperature Sensor ID6 near core A72 clusters 2 and 3

The TMU monitors these sensor sites and signals an alarm if a programmed threshold is ever exceeded, two levels of thresholds (normal/critical) are available. The current and average temperatures are continuously captured for each temperature sites and logged in register set.

Exceeding critical threshold

The critical thresholds implemented in TMU are used to protect processor from overheating.

The critical thresholds are set to 108°C. When a local temperature sensor of processor will exceed this value, the processor will send an interrupt to CPLD for performing a shutdown of the internal power supplies. Once activated, the event remains latched until the VX6124 undergoes a power-on restart (all power off and then on again).

Refer to VX6124 Yocto Linux Release Notes - D235834 for further details and know how to proceed

5.4.3. External Thermal Regulation

To ensure the best possible basis for operational stability and long-term reliability, the VX6124 is equipped with a heat sink (SA and WA classes only). Coupled together with system chassis, which provides variable configurations for forced airflow, controlled active thermal energy dissipation is guaranteed.

The physical size, shape, and construction of the heat sink ensures the lowest possible thermal resistance. In addition, the VX6124 has been specifically designed to efficiently support forced airflow as found in modern VPX systems.

Volumetric Flow Rate

The volumetric flow rate refers to an airflow through a fixed cross-sectional area (i.e. slot width x depth). The volumetric flow rate is specified in cfm (cubic-feet-per-minute).

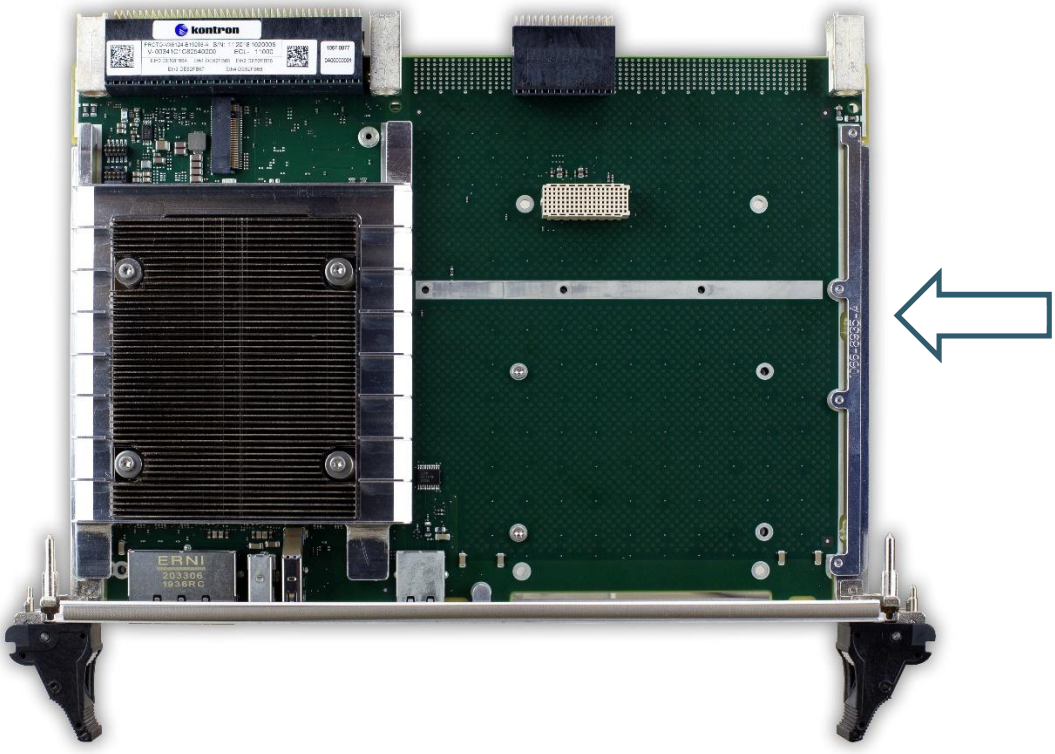
Airflow

At a given cross-sectional area and a required flow rate, an average, homogeneous airflow speed can be calculate using the following formula:

Airflow = Volumetric Flow Rate / Area

The airflow is specified in m/s (meter-per-second).

Figure 30: Airflow Direction



The following table illustrates the operational limits of the VX6124 taking into consideration processor dissipation vs. ambient air temperature vs. airflow rate.

Table 53: VX6124 Thermal operating limits

BOARD	TJMAX ALL CORES	TAMB	MIN AIRFLOW	CALCULATED INPUT AIR SPEED FOR 1" INPUT SECTION
VX6124-SA LX2160A @ 2.2 GHz	< 85°C	55°C	TBD	TBD
	< 105°C	55°C	TBD	TBD

The above table indicates the minimum air flow required for VX6124 cooling.

⚠CAUTION

Operating the VX6124 boards outside its operational limits defined in Table 53 could result in board damage. Even if the SoC device may adapt quickly to the situation with frequency reduction, the board behavior cannot be guaranteed and this is not recommended.

Mezzanine Hosting

When determining the thermal requirements for a given application, peripherals to be used with the VX6124 must also be considered. Devices which are directly attached to the VX6124 must also be capable of being operated at the temperatures foreseen for the application. It may very well be necessary to revise system requirements to comply with operational environment conditions.

In most cases, this will lead to a reduction in the maximum allowable ambient operating temperature or even require active cooling of the operating environment.

⚠CAUTION

As Kontron assumes no responsibility for any damage to the VX6124 or other equipment resulting from overheating of the CPU, it is highly recommended that system integrators as well as end users confirm that the operational environment of the VX6124 complies with the thermal considerations set forth in this document.

About Kontron – An S&T Company

Kontron is a global leader in embedded computing technology (ECT). As a part of technology group S&T, Kontron offers a combined portfolio of secure hardware, middleware and services for Internet of Things (IoT) and Industry 4.0 applications. With its standard products and tailor-made solutions based on highly reliable state-of-the-art embedded technologies, Kontron provides secure and innovative applications for a variety of industries. As a result, customers benefit from accelerated time-to-market, reduced total cost of ownership, product longevity and the best fully integrated applications overall.

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