Application note

Number	33
Date	12-OKT-2000
Author	C. Hoch
Subject	Design Guide: Connecting an external Super I/O controller to ETX or PC/104
Related Products	**Kontron** ETX-Modules and MOPSlcd6 / MOPS/686+

Date	Edited by	Alteration to previous document revision
12.10.00	C. Hoch	Initial release
08.10.01	C. Hoch	Added ETX-P3/C3
23.01.02	C. Hoch	Added ETX-P3E/CE
15.05.02	D. Gunter	English proofreading
23.08.02	H. Bruhn	Changed to Kontron style

Application note

1.   TABLE OF CONTENTS

Application note

2. HARDWARE RESOURCES

As an expansion of the I/O functions on ETX- and PC/104-Modules, it is possible to design one external Super I/O chip (SMSC FDC37C669) on the customer's backplane. There are different I/O functions which are supported by the BIOS of the respective Kontron boards. The Super I/O chip is initialized by the BIOS if the following hardware resources are assigned to the chip:

2.1. ETX-Module (ETX-P3E/C3E, ETX-P3/C3, ETX-P1, ETX-mgx)

ISA configuration base address SMSC FDC37C669: 370h (pull up on pin 91 of SMSC).

Function	Interrupt	I/O Address	DMA channel
Floppy	IRQ6	-	2
LPT *)	IRQ7 (IRQ5)	378h (278h, 3BCh)	-
COM3	IRQ10 (IRQ11)	3E8h (3F8h, 2F8h, 2E8h)	-
COM4	IRQ11 (IRQ10)	2E8h (3F8h, 2F8h, 3E8h)	-

*) ECP-mode not possible (no DMA channel assigned).

2.2. PC/104 (MOPS/686+ and MOPSlcd6)

ISA configuration base address SMSC FDC37C669: 370h (pull up on pin 91 of SMSC).

Function	Interrupt	I/O Address	DMA channel
COM3	IRQ10 (IRQ11)	3E8h (3F8h, 2F8h, 2E8h)	-
COM4 / IRDA	IRQ11 (IRQ10)	2E8h (3F8h, 2F8h, 3E8h)	-

3. CONNECTION DIAGRAMS

(See page 4 and 5)

Application note

kontron
... always a Jump ahead!

RSTDRV — RSTDRV 57 RESET
IOW# — IOW# 45 IOW
IOR# — IOR# 44 IOR
AEN — AEN 46 AEN

DACK2# — DACK2# GND 27 CS
DRQ2 — DRQ2 36 DACK_B
TC — TC 52 DRQ_B
35 TC
VCC 58 PWRGD

IRQ[3..15] — IRQ[3..15]
IRQ11 37 IRQ_C
IRQ10 38 IRQ_D
IRQ7 39 IRQ_E
IRQ6 40 IRQ_F

SA[0..19] — SA[0..19]
SA0 28 A0
SA1 29 A1
SA2 30 A2
SA3 31 A3
SA4 32 A4
SA5 33 A5
SA6 34 A6
SA7 41 A7
SA8 42 A8
SA9 43 A9
SA10 97 A10

SD[0..7] — SD[0..7]
SD0 48 D0
SD1 49 D1
SD2 50 D2
SD3 51 D3
SD4 53 D4
SD5 54 D5
SD6 55 D6
SD7 56 D7

clock termination
C1 C68pS03 GND

clock buffer
R1 R5%33RS03
R3 R5%47RS03
OSC
OSC_SMC 20 CLK14

R2 R5%33RS03
OSC_ISA

IOCHRDY — IOCHRDY 100 IOCHRDY

21 DRQ_A
19 IRQ_A
18 DRVDEN1
IRQ5 94 DRV2/ADRX/IRQ_B DRVDEN0
96 DACK_C
99 DRQ_C
98 NC

U1
FDC37C669

RXD1 78 RXD3 RXD3
TXD1 79 TXD3 TXD3
CTS1 82 CTS3# CTS3#
RTS1 81 RTS3# RTS3#
DSR1 80 DSR3# DSR3#
DTR1 83 DTR3# DTR3#
DCD1 85 DCD3# DCD3#
RI1 84 RI3# RI3#

RXD2 88 RXD4 RXD4
TXD2 89 TXD4 TXD4
CTS2 92 CTS4# CTS4#
RTS2 91 RTS4# RTS4#
DSR2 90 DSR4# DSR4#
DTR2 93 DTR4# DTR4#
DCD2 87 DCD4# DCD4#
RI2 86 RI4# RI4#

ACK 62 ACK# ACK#
BUSY 61 BUSY# BUSY#
PE 60 PE PE
SLCT 59 SLCT# SLCT#
ERROR 75 ERR# ERR#
PD0 71 PD0 PD0
PD1 70 PD1 PD1
PD2 69 PD2 PD2
PD3 68 PD3 PD3
PD4 66 PD4 PD4
PD5 65 PD5 PD5
PD6 64 PD6 PD6
PD7 63 PD7 PD7
STROBE 77 STB# STB#
AUTOFD 76 AFD# AFD#
INIT 74 INIT# INIT#
SLCTIN 73 SLIN# SLIN#

DSKCHG 17 FDCDSKCHG# FDCDSKCHG#
HDSEL 11 FDCHDSEL# FDCHDSEL#
RDATA 16 FDCRDATA# FDCRDATA#
WRTPRT 14 FDCWRPRT# FDCWRPRT#
TRK0 13 FDCTRK0# FDCTRK0#
WGATE 10 FDCWGATE# FDCWGATE#
WDATA 9 FDCWDATA# FDCWDATA#
STEP 8 FDCSTEP# FDCSTEP#
DIR 7 FDCDIR# FDCDIR#
MTR1 5 FDCMTR1# FDCMTR1#
DS0 4 FDCDS0# FDCDS0#
DS1 3 FDCDS1# FDCDS1#
MTR0 2 FDCMTR0# FDCMTR0#
INDEX 12 FDCIDX# FDCIDX#

HDCS0 25
HDCS1 26
IRQIN 23
IDEEN/IRQ_H 24
DACK_A 22

VCC
R4 R5%4K7S03

COM3-Seriell-Interface
COM4-Seriell-Interface
Centronics-Drucker-Interface
FDD-Interface

RN1 RN510RPUD8
VCC

Title
Size B
Number
Revision
Date: 30-Aug-2000
File: C:\Datenbank Protel\MyDesign.ddb
Sheet of
Drawn By: CH

FDC

X1

FDCIDX#
FDCMTR0#
FDCDS1#
FDCDS0#
FDCMTR1#
FDCDIR#
FDCSTEP#
FDCWDATA#
FDCWGATE#
FDCTRK0#
FDCWRPRT#
FDCRDATA#
FDCHDSEL#
FDCDSKCHG#

FDCIDX#
FDCMTR0#
FDCDS1#
FDCDS0#
FDCMTR1#
FDCDIR#
FDCSTEP#
FDCWDATA#
FDCWGATE#
FDCTRK0#
FDCWRPRT#
FDCRDATA#
FDCHDSEL#
FDCDSKCHG#

GND
XST34Q

VCC
RN2
FDCWRPRT#
FDCRDATA#
FDCHDSEL#
FDCDSKCHG#
FDCIDX#
FDCSTEP#
FDCWDATA#
FDCTRK0#
RN330RPUD8

LPT

X2

ACK#
BUSY#
PE
SLCT#
ERR#

ACK#
BUSY#
PE
SLCT#
ERR#

PD7
PD6
PD5
PD4
PD3
PD2
PD1
PD0

PD7
PD6
PD5
PD4
PD3
PD2
PD1
PD0

RN4 RN33RVF

PD7_RN
PD6_RN
PD5_RN
PD4_RN
PD3_RN
PD2_RN
PD1_RN
PD0_RN

RN5 RN33RVF

STB#
AFD#
INIT#
SLIN#

STB#
AFD#
INIT#
SLIN#

/STB_RN
/AFD_RN
/INIT_RN
/SLIN_RN

JBUDSUB25R

RN3
RN4K7VF

RN6 RN33RVF

CN1
CN220pVF16K
CN2
CN220pVF16K
CN3
CN220pVF16K

VCC

GND

GND

COM3 (RS232)

C2 C1PC3
C100n05
C1MC3
C2PC3
C100n05
C3 C2MC3

U2
C1+
C1-
C2+
C2-
V+
V-

VPC3
VMC3

C4
C5
C100n05

VCC

GND

RTS3#
DTR3#
TXD3

RTS3#
DTR3#
TXD3

T1IN
T2IN
T3IN
T4IN

T1OUT
T2OUT
T3OUT
T4OUT

RTS3_C
DTR3_C
TXD3_C

RXD3
DCD3#
DSR3#
CTS3#
RI3#

RXD3
DCD3#
DSR3#
CTS3#
RI3#

R1OUT
R2OUT
R3OUT
R4OUT
R5OUT

R1IN
R2IN
R3IN
R4IN
R5IN

RXD3_C
DCD3_C
DSR3_C
CTS3_C
RI3_C

EN
SHDN
GND

GND
MAX211E

X3
RI3_C
DTR3_C
CTS3_C
TXD3_C
RTS3_C
RXD3_C
DSR3_C
DCD3_C

GND
GND

JSTDSUB9R

COM4 (RS485/422)

U3
RXD4
DTR4#
RTS4#
TXD4

RXD4
DTR4#
RTS4#
TXD4

RO
/RE
DE
DI

VCC
B
A
GND

VCC

485_xXD- (422_RXD-)
485_xXD+ (422_RXD+)

R9
R5%120RS03

GND

U4
CTS4#
RI4#
DCD4#
DSR4#

CTS4#
RI4#
DCD4#
DSR4#

RO
/RE
DE
DI

VCC
B
A
GND

VCC

VCCO
VCCO

TXD4
MAX483

R10
R5%240RS03

R11
R5%120RS03

R12
R5%240RS03

422_TXD-
422_TXD+

GND

GND

X4
GND

485_xXD-
422_TXD-

485_xXD+
422_TXD+

GND

JSTDSUB9R

4xR5%10KS03
R5 R6 R7 R8

VCCO

RS485 (half duplex): only U3 is used

RS422 (full duplex): U3 and U4 are used

Title		
Size B	Number	Revision
Date:	30-Aug-2000	Sheet of
File:	C:\Datenbank Protel\MyDesign.ddb	Drawn By: CH