Related Products	ETX
Subject	Interrupt Latency
Document Name	ETX_INT_LATENCY.doc
Usage	Common

1. REVISION HISTORY

Date	Document Name	Subjects added, changed, deleted	Changed by
24-Feb-04	ETX_INT_LATENCY.doc	Created Application Note	BHA
27-Feb-04	ETX_INT_LATENCY.doc	Added remarks MGX, USB legacy, DMA	BHA

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3. INTRODUCTION

This document describes the minimum latency for the interrupts. This document contains preliminary and not approved information.
Testsoftware: IRQ_TRIQ.EXE with MS-DOS 6.22
All other interrupts are not active. The software assert a IRQ-Line (via LPT-Port D0) and set a other LPT-Line (D1). The CPU detected the interrupt request and start the interrupt service routine. The interrupt service routine clear the LPT-Line (D1).
ISA IRQ: Latency is from the rising edge of IRQ to falling edge of D1.
PCI INT: Latency is from the falling edge of INT to falling edge of D1.
For the ISA IRQ is necessary that no PCI device use this interrupt. For the PCI INT is necessary that the BIOS configurated a device with this interrupt. Please check this with a PCI-Configuration tool.

4. LATENCY

ETX	Project	Grafik	ISA IRQ Latency	ISA IRQ Latency sporadic	PCI INT Latency	PCI INT Latency sporadic
VE 800MHz	MOD9	UMA	2.3µs	+1µs	2µs	+1µs
VE 400MHz	MOD9	UMA	2.3µs	+1µs	2µs	+1µs
P3M 800MHz	MOD8	UMA	2.3µs	+1µs	2µs	+1µs
P3M 1.2GHz	MOD8	UMA	2.2µs	+1µs	1.9µs	+1µs
P3E 700MHz	MOD7	UMA	2.3µs	+1µs	2.1µs	+1µs
C3 400MHz	MOD6	AGP	3.1µs±0.8µs		2.3µs±0.2µs	
P3 500MHz	MOD6	AGP	3µs±0.5µs		2.2µs±0.2µs	
P3 700MHz	MOD6	AGP	2.9µs±0.5µs		2µs±0.2µs	
P1 266MHz	MOD5	AGP	1.8µs±0.2µs		1.8µs±0.1µs	
MGX 200MHz	MOD1	UMA	3µs±0.5µs	+50µs	0.8µs±0.1µs	+50µs
MGX 300MHz	MOD1	UMA	3µs±0.3µs	+50µs	3.2µs±0.2µs	+50µs
PM 1.1GHz	MODB	UMA			1.8µs±0.1µs	
PE 133MHz	MODE	No	7µs±0.5µs		8µs±2µs	

Most of the latency time dependent on the operating system. That is the reason why we use MS-DOS. If a higher level interrupt occur and stop the interrupt or block the interrupt, then the latency time increase dramatically. An example if a higher interrupt occure and the service routine of this interrupt must set one bit and then return (RTI), this need typically 20..40 µs.

Only for MGX MOD1: The big sporadic latency time, depend on the graphic mode. If the graphic mode not from the hardware support, then the software must emulate the mode. This block the interrupt for a time.

Problem with USB legacy: If the USB legacy enabled, then the system start from time to time the SMI. This block all interrupts. If a PS/2-Mouse generate interrupts, this also start the SMI (only if USB legacy enabled), so the mouse activity increase the latency time of a real time system.

DMA: If an busmaster use the bus with DMA, then the interrupts are blocked for this time. If it possible don't use DMA. Switch the harddisk (IDE) in PIO mode. If it necessary to use DMA, perhaps it's possible to optimize the PCI configuration register latency timer.